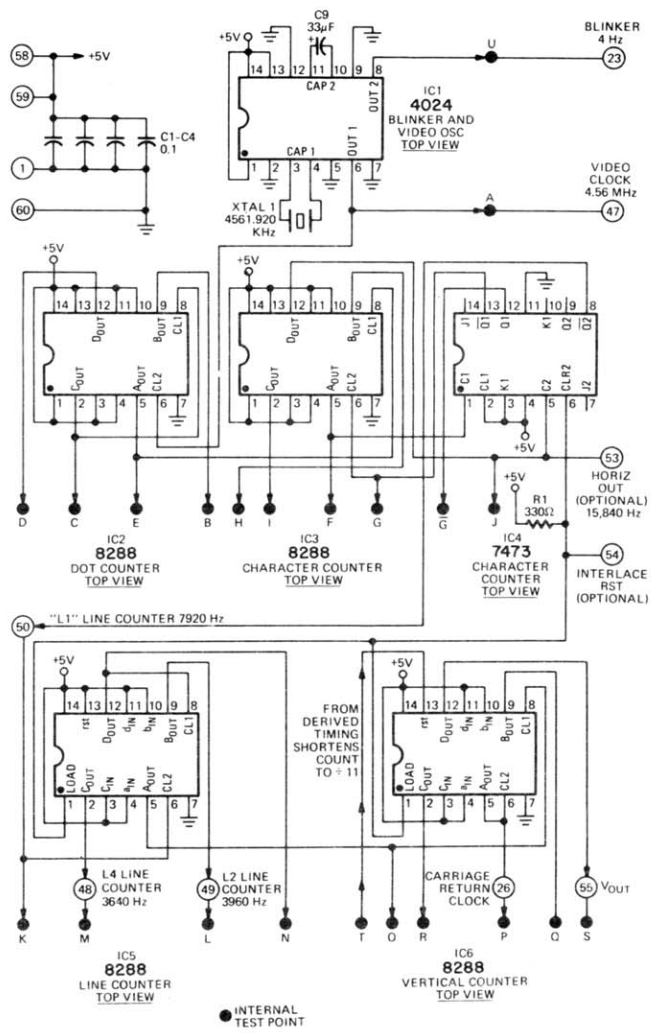
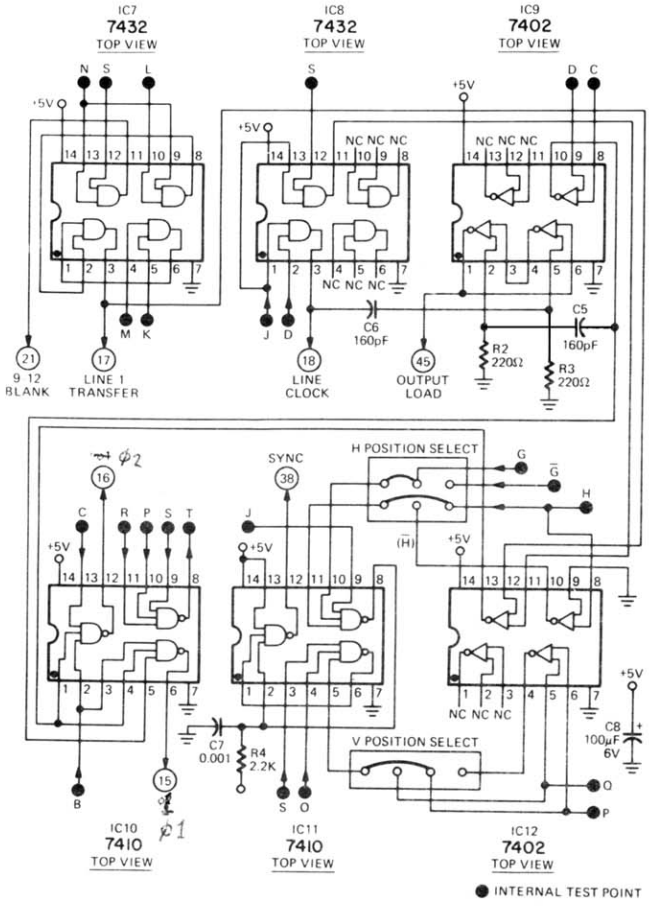
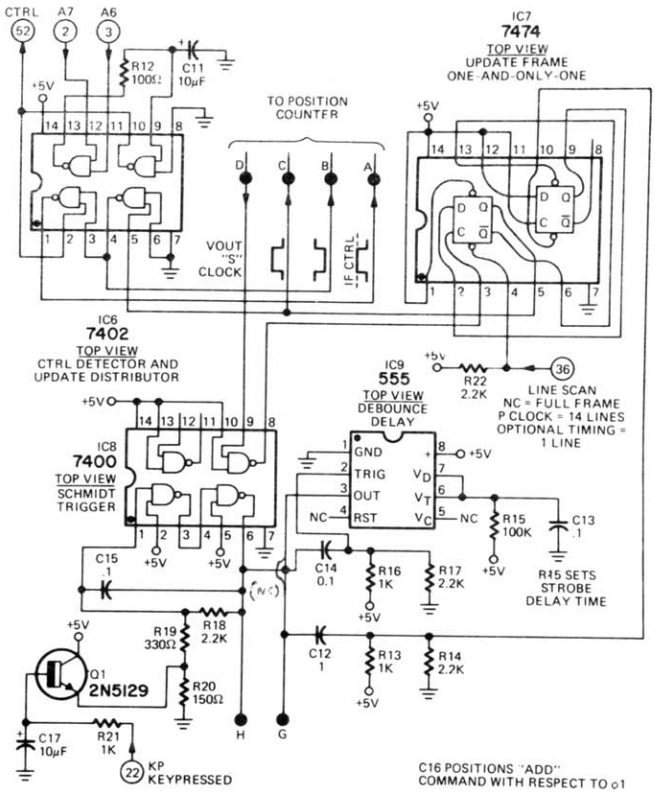




TOP LEFT
FIG. 6 -- MAIN TIMING CHAIN schematic.



ABOVE
FIG. 7 -- DERIVED TIMING schematic.

LEFT
FIG. 8 -- CURSOR INPUT conditioning and sequencer circuit.