PERCOM

SBC/9™

USERS MANUAL

PERCOM DATA COMPANY
211 N. KIRBY
GARLAND, TEXAS 75042

the SBC/9(tm)
Single-Board Computer/MPU Card

USERS MANUAL

050-0150-001
Revision B

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Section I
INTRODUCTION

The Percom SBC/9(tm) is a 6809 upgrade CPU for SS-50 bus computers as well as a complete single-board computer with serial and parallel I/O channels, and on-card ROM, RAM and power regulators.

As an upgrade CPU, the SBC/9(tm) is fully plug-in compatible with the SS-50 bus, requiring no modification of the motherboard, memory or I/O.

The SBC/9(tm) will also accommodate, without changes, either a 6802 or 6808 microprocessor. Both the 6802 and 6808 use 6800-code, and an enormous selection of application and system software is available to choose from. A 6802 or 6808 version of the SBC/9(tm) may be ordered from Percom, or the user may retrofit a standard 6809 SBC/9(tm) by merely removing the 6809 IC and installing a 6802 (or 6808) in the special "quad-in-line" socket.

The SBC/9(tm) is supplied with a 1-Kbyte ROM monitor which provides the usual monitor commands and functions, but which is far more versatile than other monitors because it is specially structured to be easily extended and customized. Moreover, I/O is easily directed to any peripheral device in a way in which the details of I/O software are left to the individual I/O device drivers.

The SBC/9(tm) will directly address a 65-Kbyte memory space, and will address up to one Mbyte of memory -- using four system bus serial baud lines -- without disabling the on-card bit rate generator. Using a memory management system, 16 Mbytes or more may be addressed through the parallel port.

The extraordinary versatility of the SBC/9(tm) is underscored by the full-capability, inexpensive word processing system described in Appendix A7. In this system, the SBC/9(tm) provides the central processing function as well as I/O interfacing to the keyboard, printer and a modem. A Percom LFD-400(tm) mini-disk system is used for storage, and a Percom WINDEX(tm)-driven ELECTRIC WINDOW(tm) video display generator is used to generate and control the monitor display. For memory, the system uses two Percom SS-50 bus RAM cards.

In addition to the MC6809 Instruction Set Summary (green card) included with the SBC/9(tm), a Motorola MC6809 Preliminary Programming Manual is also available from Percom. The price is $15.00. Refer to the next-to-last page of this manual for procedures for ordering products from Percom Data Company.

Section II
SYSTEM DESCRIPTION

This section includes a physical description of the SBC/9(tm), a functional block diagram discussion of hardware features and an overview of the PSYMON(tm) operating system.

2.1 PHYSICAL DESCRIPTION

The SBC/9(tm) card is double-sided, plated through FR4-G10 epoxy-glass. The printed wiring is tin-lead plated two-ounce copper.

All complex ICs and memory chips are socket-mounted. A "quad-in-line" socket, near the center of the board, accepts either a type 6809 microprocessor IC or a type 6802 (or 6808) microprocessor.

In addition to the 6802 option, the SBC/9(tm) may be easily configured to accommodate most system peripheral requirements by strapping between jumper-wire contacts. Terminal strips (TS) for configuration strapping have hexagonal contact pads.

The SBC/9(tm) is fully plug-in compatible with the SS-50 bus which is described in detail in Appendix A1.

2.2 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

A functional block diagram of the SBC/9(tm) is shown in Figure 2.1. The following discussion is keyed to this figure. The component reference designators are shown in the Parts Position Diagram and Circuit Schematic of Section IV.

2.2.1 The SBC/9(tm) Microprocessor

The SBC/9(tm) will accommodate -- without circuit modification -- either the new, powerful MC6809 microprocessor or the MC6800-software-compatible MC6802 (or MC6808). The standard SBC/9(tm) includes a 6809 IC. The 6802 reconfiguration is covered in Section III. An addendum to this manual is supplied when the 6802 option is purchased.

2.2.2 Serial I/O

The principal components of the serial I/O interface circuit are an Asynchronous Communications Interface Adapter (ACIA) chip, U35, and transistors Q5 and Q6. The ACIA chip interfaces serial asynchronous data to bus-organized systems. Transistors Q5 and Q6 level shift signals for compatibility with EIA RS-232-C voltage level specifications.

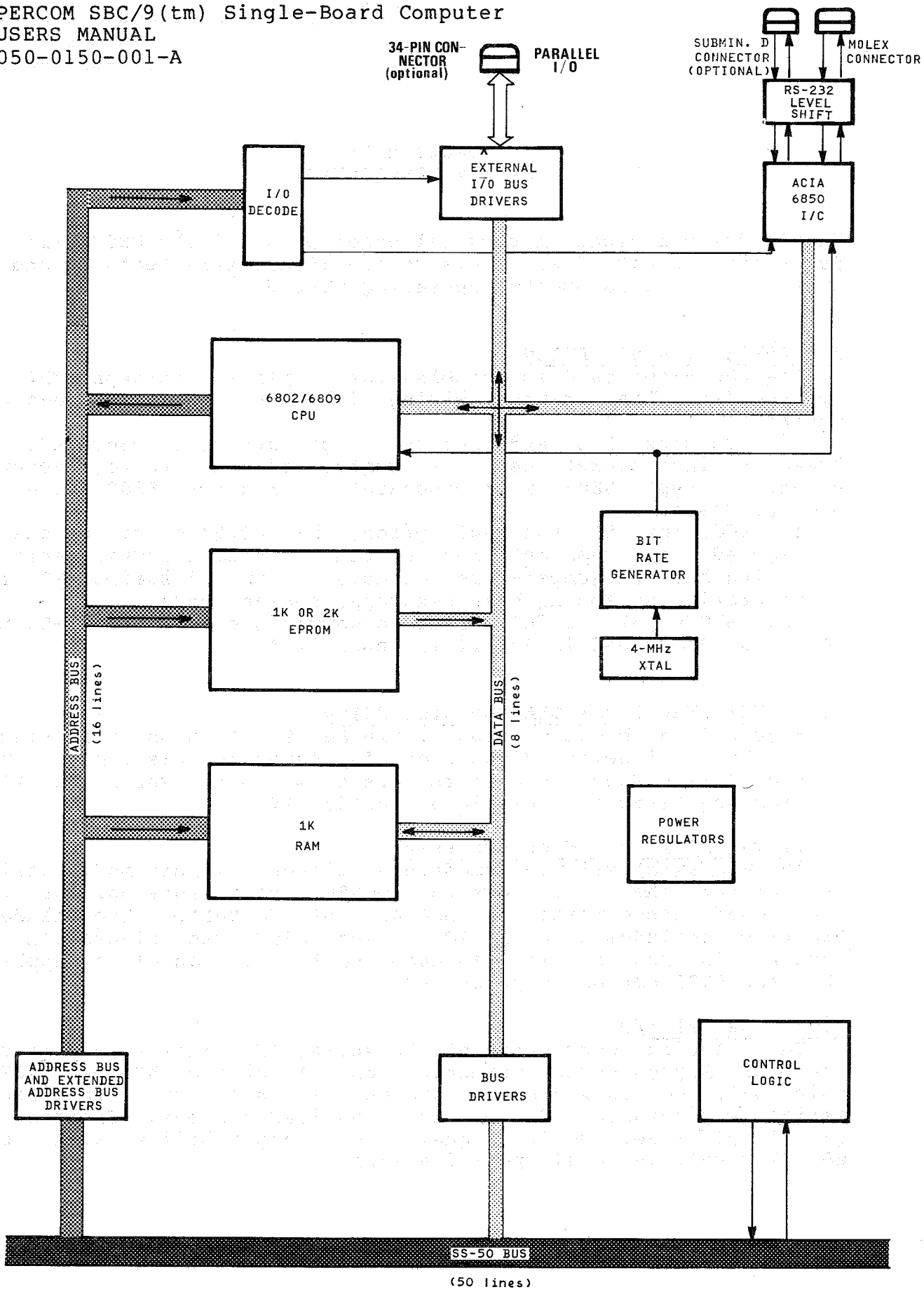


FIGURE 2.1 SBC/9™ FUNCTIONAL BLOCK DIAGRAM

The side-edge-mounted Molex connector provides SWTP MP-C or MP-S type interface compatibility. An optional subminiature 'D' connector may be installed in the contacts provided for full RS-232 interfacing.

Several conductors used on SWTP serial interface cards to support a current loop data terminal have been redefined to permit fuller RS-232 type "handshake" with the ACIA of the SBC/9(tm).

The procedure for adding a subminiature 'D' connector is covered in Section III and Appendix A4.

2.2.2.1 Bit Rate Generator

The SBC/9(tm) on-card bit rate generator (BRG) generates a 16X clock for both the serial I/O interface and the 50-pin system bus. All standard rates from 110 b/s to 19.2 kb/s are generated, and are available at Terminal Strip TSm.

If the extended address option of the SBC/9(tm) is enabled, the 150, 300 and 600 bauds are not available. Refer to Section III for procedures on bit rate selection and strapping.

2.2.3 Parallel I/O

The SBC/9(tm) 8-bit parallel channel is a well-buffered, bi-directional, non-latched multi-address extension of the data bus. Because it provides an electrically well-buffered bidirectional I/O channel, it is more flexible than a Peripheral Interface Adapter (PIA). The connection is made via an optional 34-conductor ribbon cable socket which may be installed in contacts provided near the top left edge of the PC card. The line buffer drivers and interdigitated quiet lines -- signal lines separated by grounded lines on even-numbered pins -- permit connection to external modules via cables of up to three feet in length.

2.2.4 EPROM

The SBC/9(tm) is configured for two type 2708, 1-Kbyte EPROM ICs. The SBC/9(tm) system monitor, PSYMON(tm), is normally installed as U29 in the first ROM position, and a second 2708 (optional), which may be used to customize or extend PSYMON(tm), is installed in the second position (U30). The PSYMON(tm) operating system is described in paragraph 2.3.

The EPROM circuit may be reconfigured to accommodate either a single- or triple-voltage 2716 EPROM as discussed in Section III.

An SBC/9(tm) memory map is included as Appendix A2.

2.2.5 RAM

The SBC/9(tm) includes 1-Kbyte of static RAM in two type 2114 chips (U31 & U32). These are addressed at F000 - F3FF, as shown in the SBC/9(tm) memory map.

2.2.6 I/O Address Decoding

The I/O address decoding circuitry is comprised of the gates and inverters of U12 through U21 (except U14) and U25. On-card address decoding eliminates contention between I/O addressing and adjacent memory space addresses.

2.2.7 Power Regulators

Two type LM340 heat-sink-mounted regulators, Q7 and Q8, provide regulated +5-volt power from an unregulated +8-volt input. Transistor Q2 and diode regulator CR1 together drop the -16-volt input to a regulated -5-volt level, and Q1, Q3, Q4 and associated components provide a regulated +12 volts from the unregulated +16-volt input. The regulated +12-volt and -5-volt levels are for EPROMs. (As mentioned above, either single- or triple-voltage 2716 EPROMs may be installed in the SBC/9(tm).) The SBC/9(tm) power regulators minimize the need for power regulation at the supply and therefore simplify power supply design.

2.3 PSYMON(tm): THE SBC/9(tm) OPERATING SYSTEM

The SBC/9(tm) 1-Kbyte ROM operating system, PSYMON(tm), provides the usual monitor commands and functions. It is, however, far more versatile than other 1K monitors because it is easily extended and customized. A unique "look-ahead" program structure first causes PSYMON(tm) to search for an alternate ROM command table. This table, if implemented by the user, may be employed to redefine and/or extend the primary PSYMON(tm) command set. Moreover, I/O is easily directed to any peripheral device -- including a disk system -- through a Device Control Block (DCB) table located in memory. This technique relegates the details of I/O software to the individual I/O device drivers, making PSYMON(tm) very easy to interface to.

For a full description and operating details of PSYMON(tm), refer to the PSYMON(tm) users manual which is provided with the purchase of an SBC/9(tm). A complete source listing of PSYMON(tm) is included therein.

The ROM operating system for the SBC/9(tm) 6802 configuration is covered in the SBC/9(tm) 6802 addendum. This addendum is included if the 6802 option is ordered, or it may be purchased separately. Information for ordering parts, manuals, etc., is included on the next-to-last page of this manual.

Section III
INSTALLATION & CONFIGURATION OPTIONS

3.1 6802/6808 RECONFIGURATION

The standard SBC/9(tm) uses the 6809 MPU chip. A 6808/6802 version may be ordered from Percom, or the standard 6809 version may be field-retrofitted with a 6808 or 6802 as follows:

1. Remove the 6809 IC and install a 6802 (or 6808) in that portion of the "quad-in-line" socket designated for U7. (Refer to the parts position diagram of Section IV.)
2. Remove the 6809 monitor ROMs (U29 & U30) and install a 6802/6808 monitor. The 6809 and 6802/6808 are not machine code compatible.
3. Restrap the TSn terminal strip, located near U28, as follows:
   a. Remove the link between TSn-1 and TSn-2.
   b. Remove the link between TSn-3 and TSn-4.
   c. Connect a jumper wire between TSn-2 and TSn-3.

3.2 SERIAL I/O and BIT RATE SELECTION

Either the 10-pin, side-edge-mounted Molex connector or an optional subminiature 'D' connector (AMP 206584-1 or equivalent) may be used to connect to the serial I/O channel. The 25-pin right-angle 'D' connector is mounted at the top of the PC card in contacts provided.

3.2.1 Serial I/O Connections

The SBC/9(tm) serial I/O interface is discussed in detail in Appendix A4. Pins 8, 9 and 10 of the Molex connector, which are used on SWTP serial interface I/O cards to support a current loop data terminal, have been redefined as Data Carrier Detect (DCD), Request-to-Send (RTS) and Clear-to-Send (CTS) lines to permit a more complete RS-232 type "handshake" with the on-card ACIA chip. Refer to Appendix A4 for details.

Most of the serial I/O lines may be restrapped via terminal strip contacts to satisfy individual system I/O pinout requirements.

3.2.2 Bit Rate Selection

The outputs from the on-card Bit Rate Generator (BRG) are available at terminal strip TSm. To connect a selected bit rate, connect a jumper wire between contact 10 of TSm and one of the other TSm contacts as follows:

BIT RATE (bits/sec)	FREQUENCY (kHz)	TSm
110	1.760	2
150*	2.400	8
300*	4.800	6
600*	9.600	4
1200	19.20	1
2400	38.40	3
4800	76.80	5
9600	153.6	7
19200	307.2	9

The rates marked by an asterisk are not available if the Extended Address option, discussed in paragraph 3.4, is enabled. If the Extended Address capability is not used, connect TSg-2 to TSg-3 and TSk-1 to TSk-2 to enable the 150, 300 and 600 baud outputs.

Several of the BRG outputs are brought out to the SS-50 bus connector. The pin assignments are given in Appendix A1.

3.3 PARALLEL I/O

Connection to the 8-bit parallel I/O port is made via an optional 34-pin ribbon cable (Winchester Header connector type 52-1134-50 or equivalent) which may be installed in the contacts provided at the top left of the PC card. The pin assignments are as follows:

PIN	FUNCTION	PIN	FUNCTION
1	I/O SELECT	--	--
3	ENABLE	19	D0
5	IRQ*	21	D1
7	R/W	23	D2
9	A0	25	D3
11	A1	27	D4
13	A2	29	D5
15	A3	31	D6
17	A4	33	D7

*To enable IRQ, jumper TSm-11 to TSm-12.

All even numbered pins are grounded "quiet" lines.

3.4 EXTENDED MEMORY ADDRESSING

The SBC/9(tm) may be configured to address up to 1 Mbyte of memory space via system bus lines, or to address 16 Mbytes or more through the buffered parallel I/O channel.

3.4.1 One Megabyte Extension

If the SS-50 bus serial bit rate lines are not required, they may be reconfigured as address lines A16 through A19 to provide an addressing capability of 1 megabyte. Address lines A16 through A19 are program controlled by any 6802/6809 instruction which causes a memory WRITE to addresses hex FC00 - FFFF. Such an instruction causes the state of address lines A0 through A3 to be captured in the extended address latch, U27, in the following order:

A0	determines	A16
A1	"	A17
A2	"	A18
A3	"	A19

To enable the extended 1-Mbyte address feature:

1. Remove the link between TSg-2 and TSg-3.
2. Remove the link between TSk-1 and TSk-2.
3. Remove the link between TSp-1 and TSp-2.
4. Connect a jumper wire from TSg-1 to TSg-2.
5. Connect a jumper wire from TSk-2 to TSk-3.
6. Connect a jumper wire from TSp-2 to TSp-3.

3.4.2 16 Megabyte Extension

The buffered parallel I/O channel may be cabled to a memory controller or to suitably designed memory cards to "bank select" up to 256 65-Kbyte memory arrays.

3.5 DMA/BUS REQUEST

The 110-baud output from the SBC/9(tm), which is routed to conductor 5 of the SS-50 bus, may be redefined as a DMA/BUS REQUEST input for the 6809 microprocessor.

To implement this redefinition:

1. Remove the link between TSh-1 and TSh-2.
2. Connect a jumper wire from TSh-2 to TSh-3.

3.6 TYPE 2716 EPROM RECONFIGURATION

The SBC/9(tm) is configured for two 2708 EPROMs, but it may be reconfigured for a single 2716 EPROM or equivalent ROM. The 2716 IC must be installed in place of U29, and if a ROM is in U30 it must be removed and the socket left vacant. To reconfigure the SBC/9(tm) for a 2716 EPROM:

Connect:		2708 (default)		2716 (5-volt)		TMS-2716 (triple volt.)
TSr-2	to	TSr-1	or	TSr-1	or	TSr-5
TSr-4	to	TSr-3	or	TSr-9	or	TSr-3
TSr-6	to	TSr-5	or	TSr-5	or	TSr-9
TSr-8	to	TSr-7	or	TSr-10	or	Tsr-7
TSf-2	to	TSf-1	or	TSf-3	or	TSf-3

3.7 RECONFIGURATION FOR SELF-CLOCKING CASSETTE

The serial I/O channel transmit and receive clocks, TxC and RxC, are conected together, as required if a self-clocking cassette interface system is not used. Sever the printed wiring link between TSe-1 and TSe-2 to separate these lines for interfacing a self-clocking cassette system such as the Percom CIS-30+.

3.8 ACIA IRQ RECONFIGURATION

The ACIA (U35) Interrupt Request output signal to the system bus and MPU may be disconnected at the ACIA chip by severing the printed wiring link between TSt-1 and TSt-2.

3.9 DATA ACCESS TIME CONTROL: MRDY OPTION

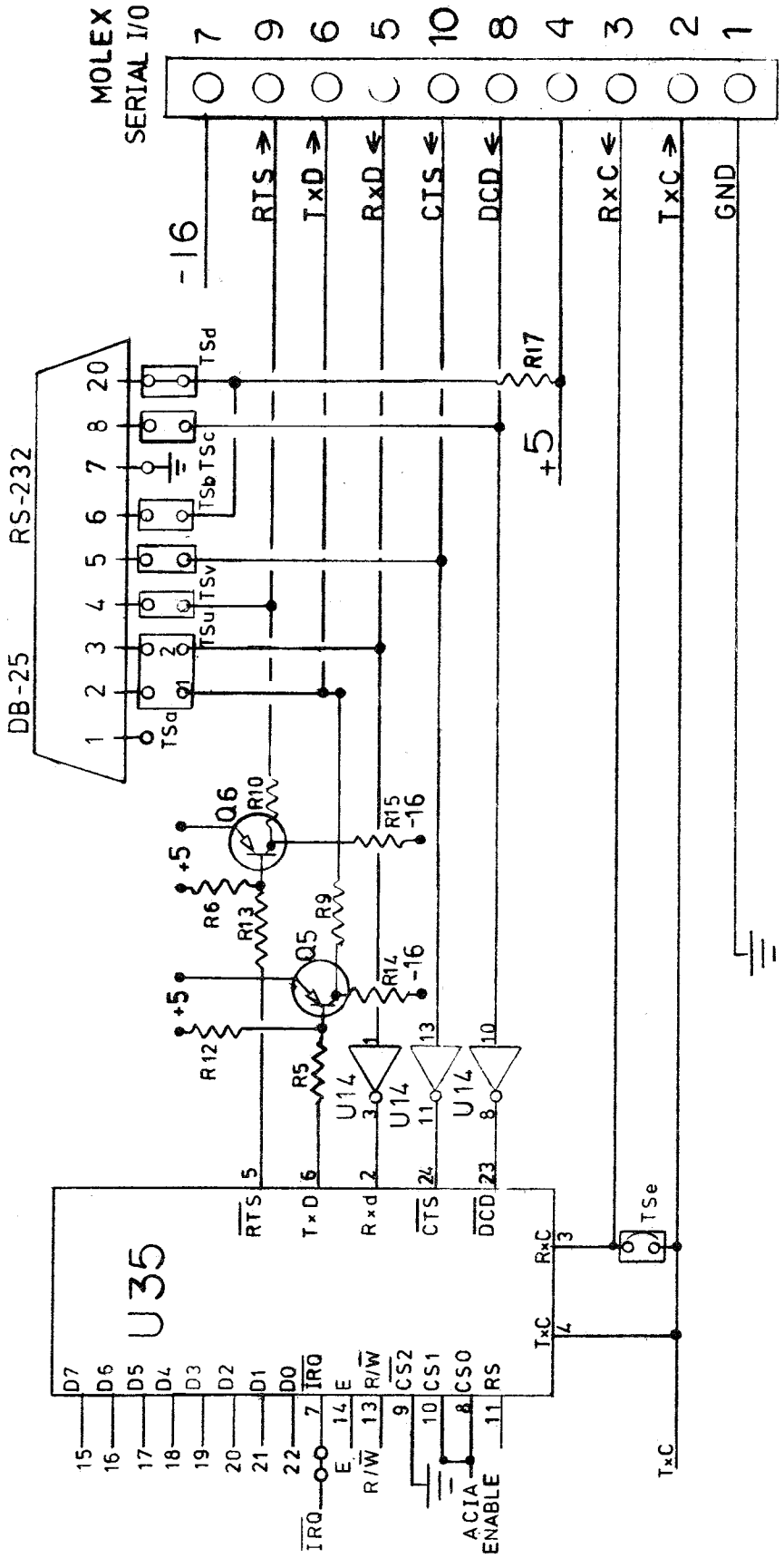
The SBC/9(tm) as shipped is configured so that the MPU MRDY line is pulled up to +5 volts (memory always ready), and MRST is wire-ORed to RESET for the MPU reset input. For slow memory, the data access time may be extended up to 10 microseconds under control of an MRDY input from the memory system. This capability is enabled by

1. severing the printed wiring link between TS_s-1 and TS_s-2, and
2. connecting a jumper wire from TS_s-2 to TS_s-3.

3.10 RESET LINE PULL-UP RESISTOR

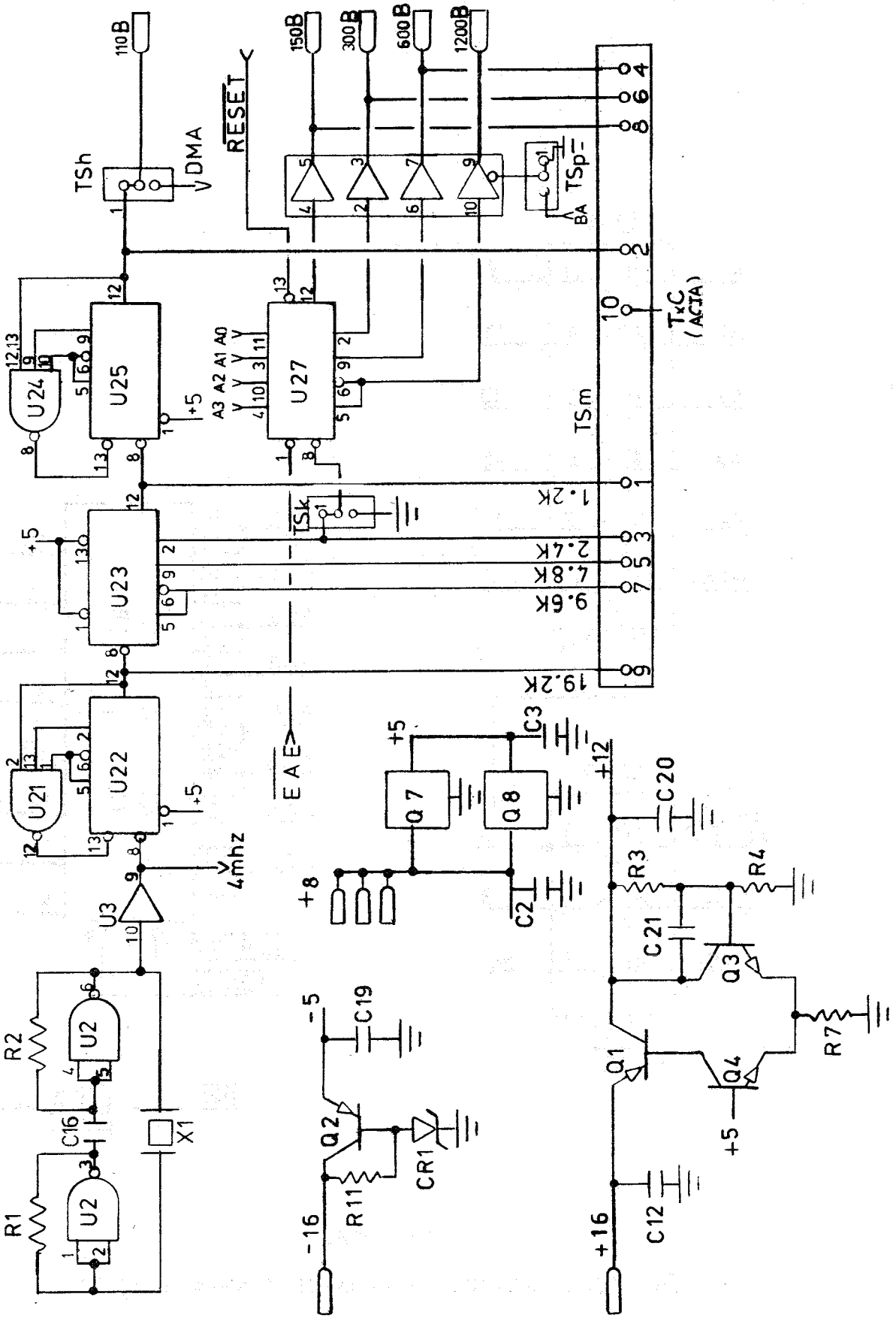
Some SS-50 bus motherboards do not include a RESET line pull-up resistor on the motherboard as does the SWTP motherboard. In these cases, a 1-kohm 1/4-watt pull-up resistor may be installed on the SBC/9(tm). Connect one end of the resistor to TS_s pin 1. Connect the other end to integrated circuit U28, pin 16 (+5 Vdc). If the reset time is excessive, reduce the value of capacitor C22 to 47 or 50 microfarads.

IV SERVICE SHEETS



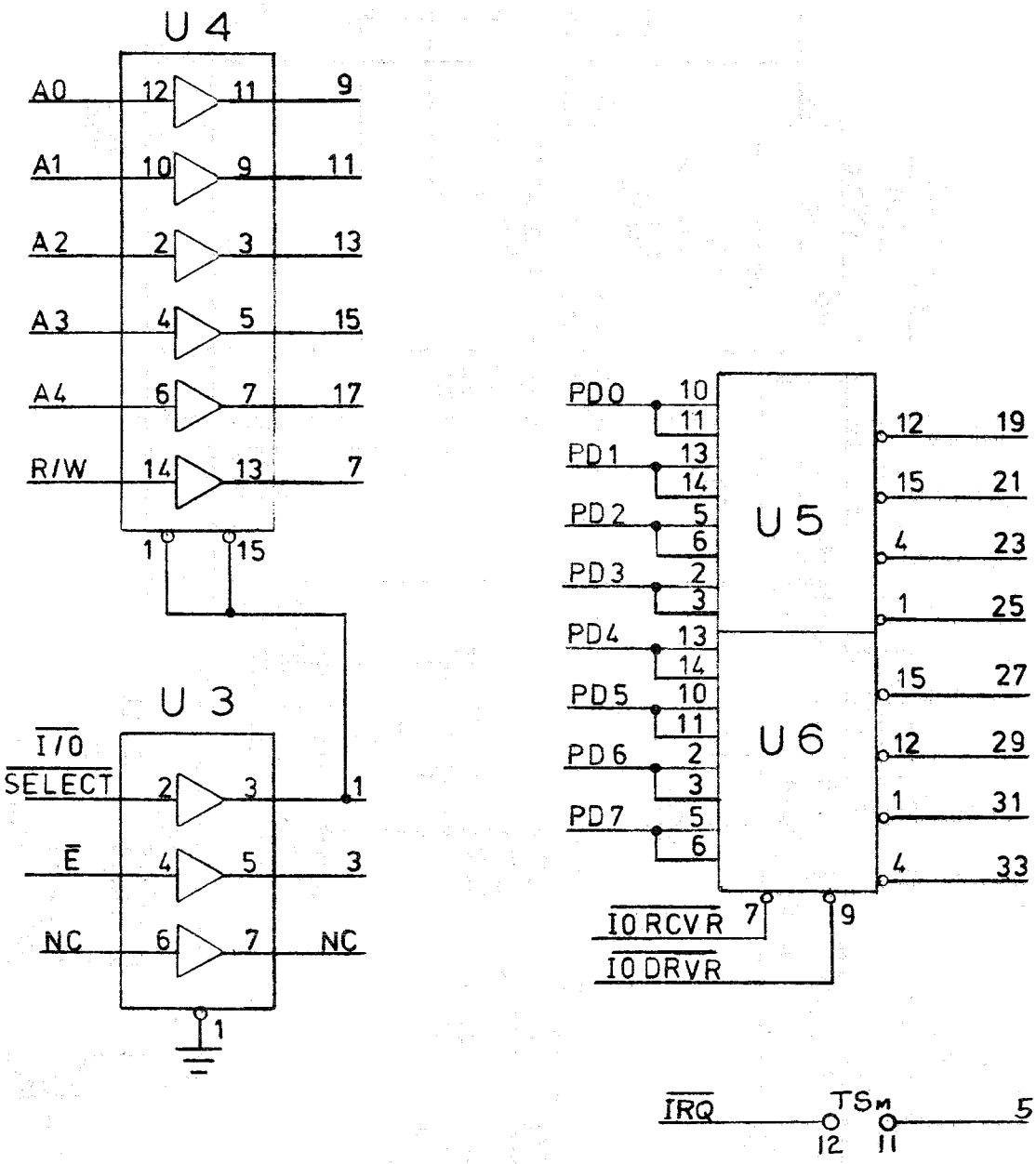
SERIAL INTERFACE

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 1 of 7)



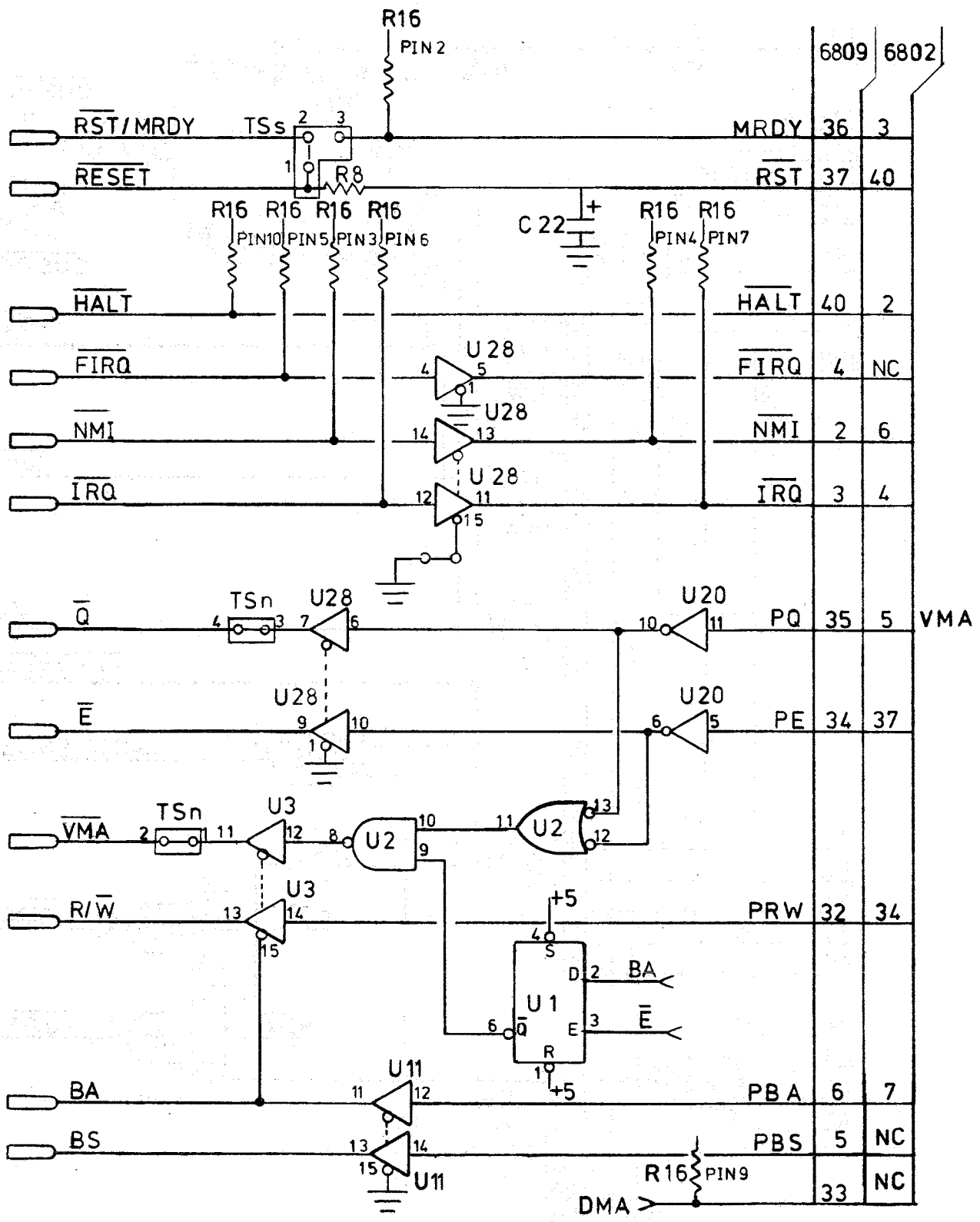
BAUD RATE GENERATOR

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 2 of 7)



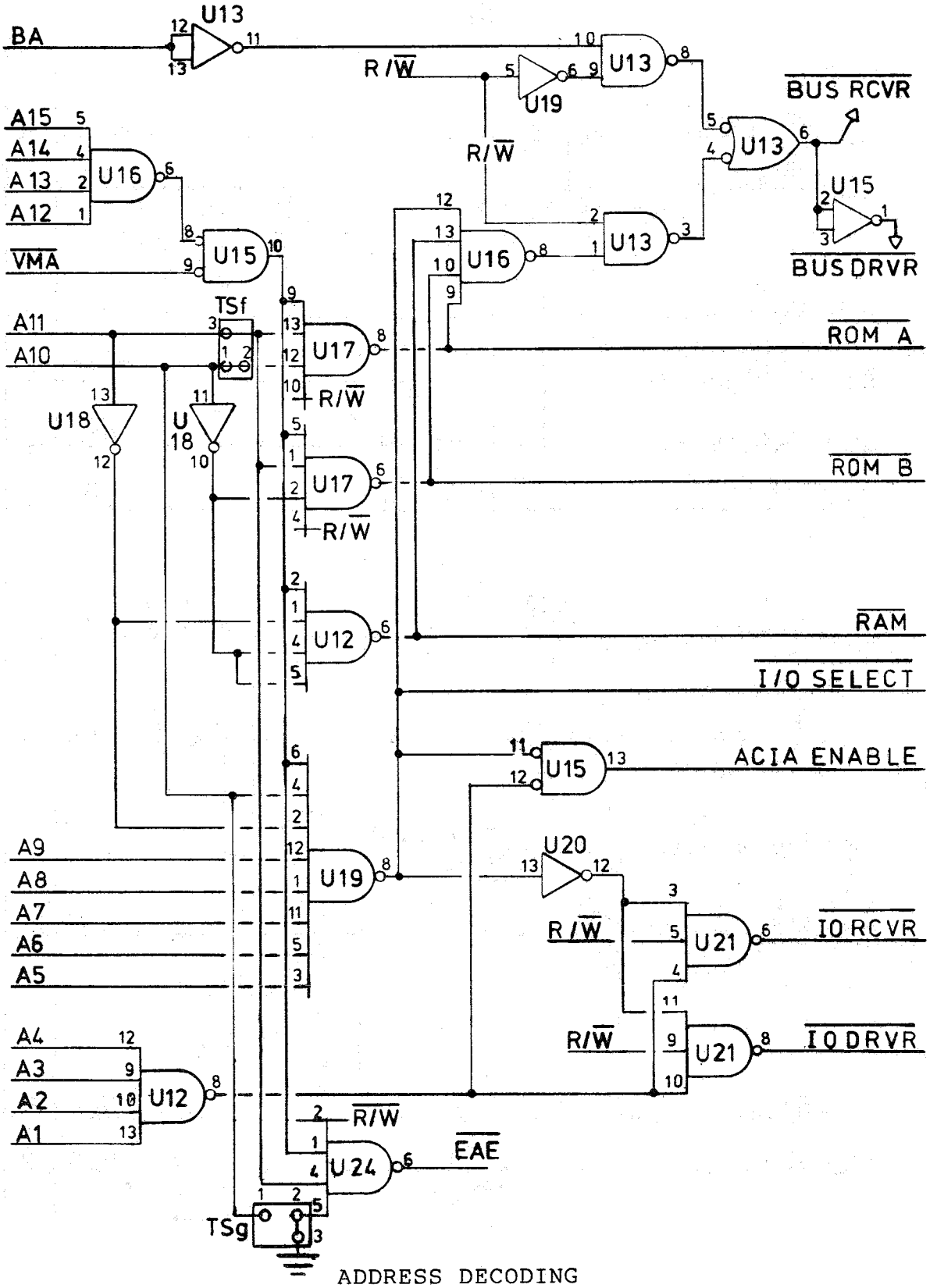
I/O PORT

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 3 of 7)



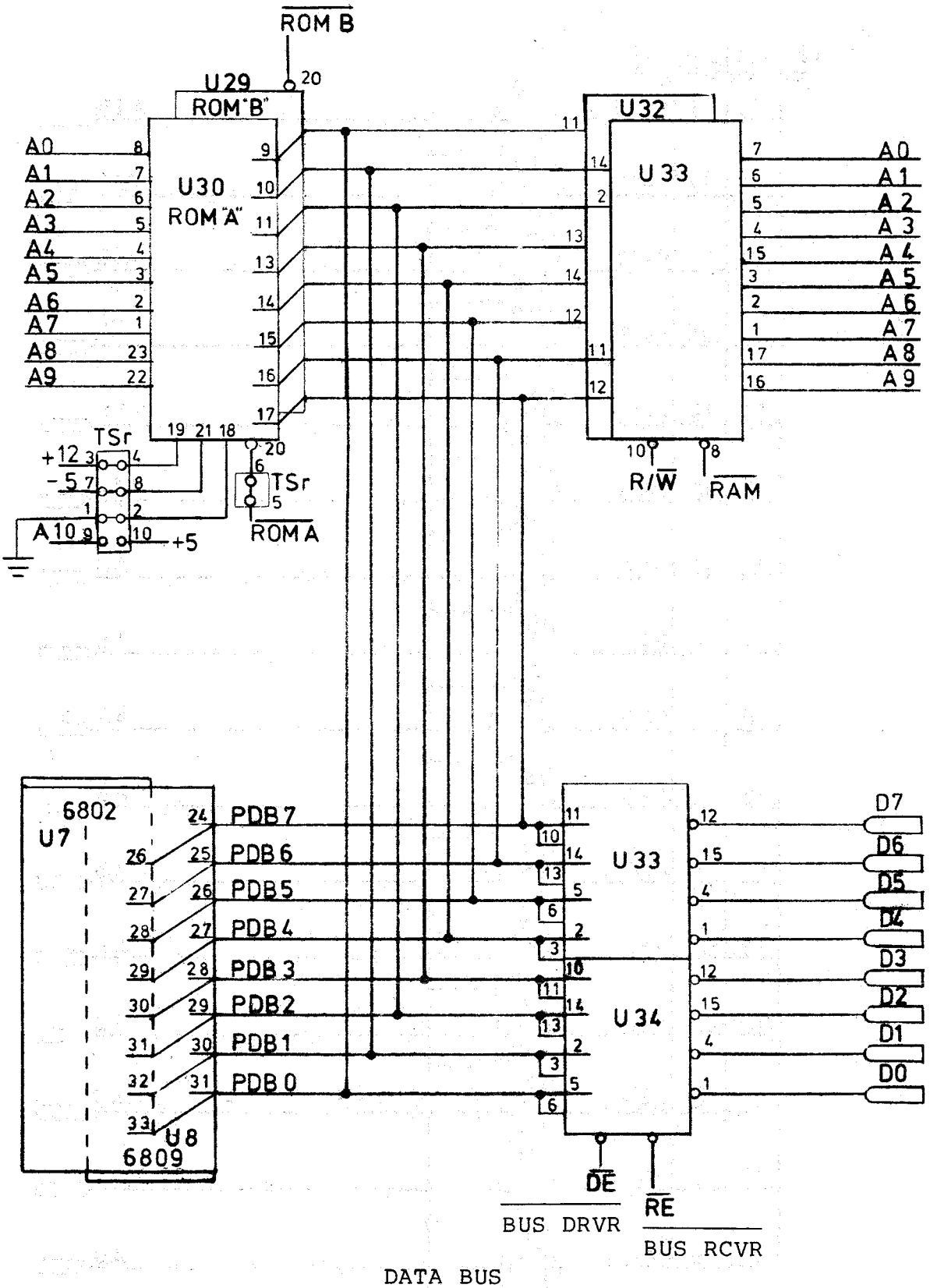
CONTROL

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 4 of 7)

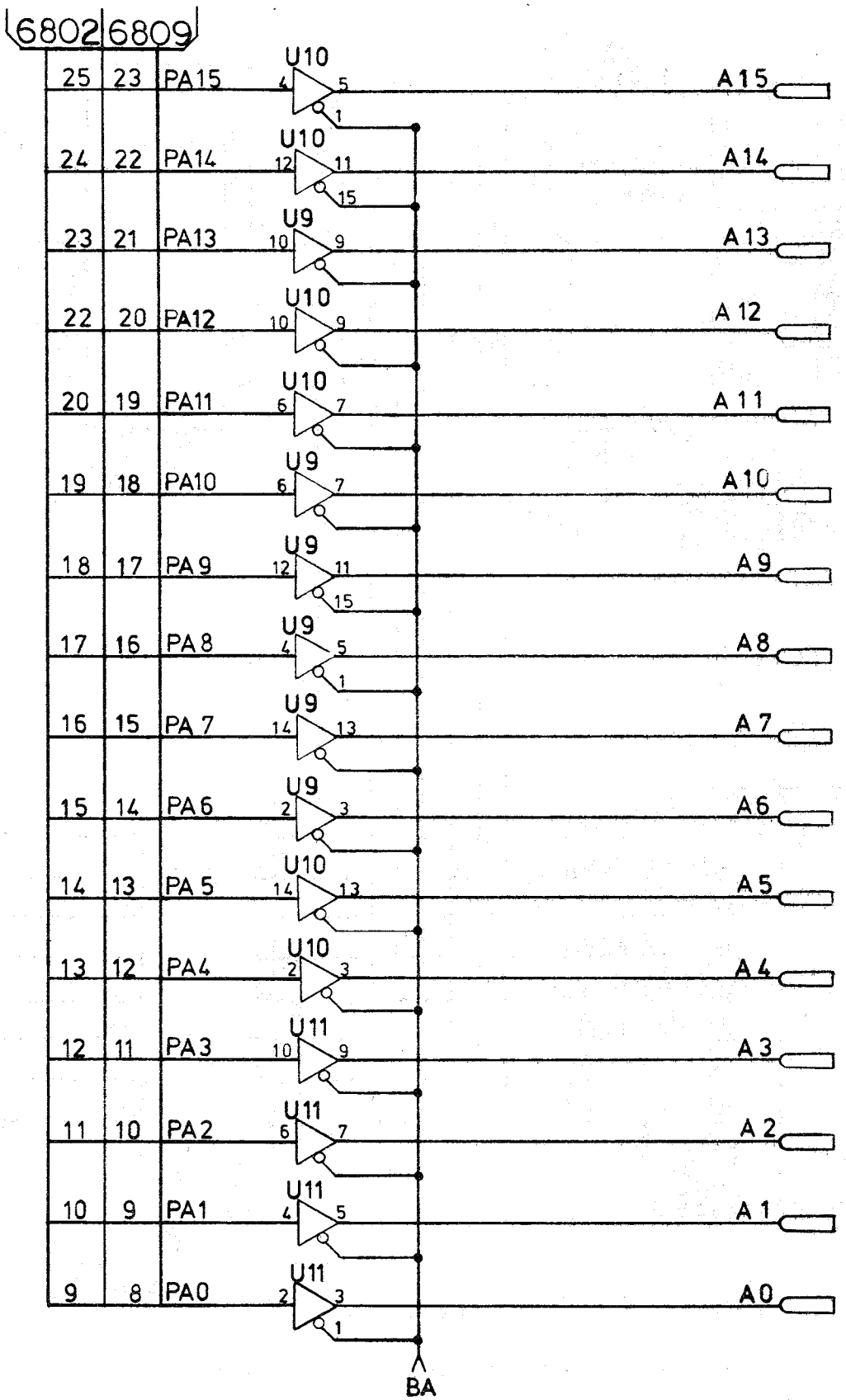


ADDRESS DECODING

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 5 of 7)

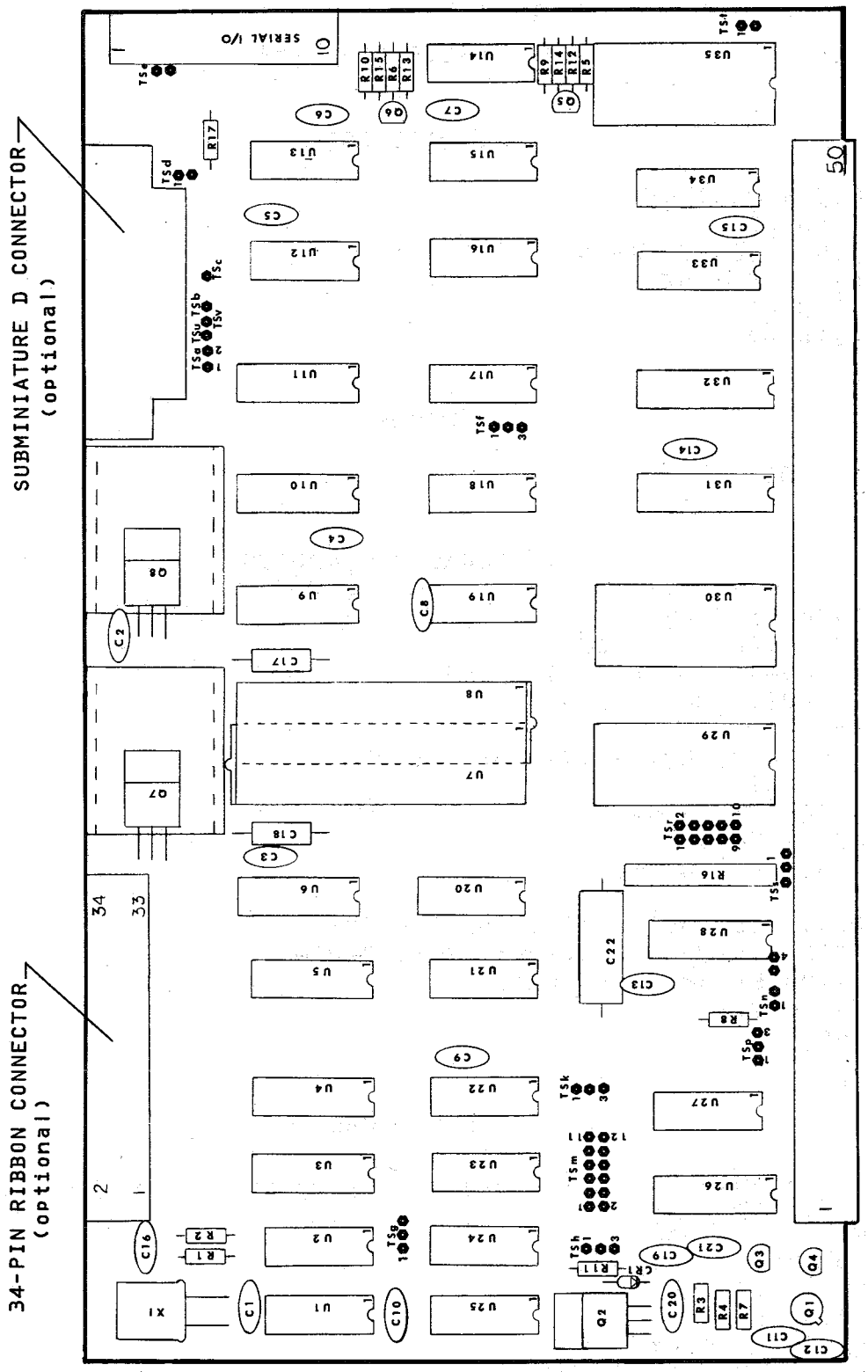


SBC/9(tm) CIRCUIT SCHEMATIC (sheet 6 of 7)



ADDRESS BUS

SBC/9(tm) CIRCUIT SCHEMATIC (sheet 7 of 7)



SBC/9(tm) PARTS POSITION DIAGRAM

*** PARTS LIST ***

CAPACITORS

C1 - C15 - 0.01 uF
C16 - 750 pF
C17, C18 - 33 uF, 16 V
C19, C20 - 0.1 uF
C21 - 220 pF
C22 - 220 uF

DIODES

CR1 - 1N752

INTEGRATED CIRCUITS

U1 - 7474 or 74LS74
U2, U13 - 7400 or 74LS00
U3, U4, U9-U11, U26, U28 - 74367
U5, U6, U33, U34 - 8835
U8 - 6809
U12, U16, U17, U24 - 7420 or 74LS20
U14 - UA1489
U15 - 7402 or 74LS02
U18, U20 - 7404
U19 - 7430 or 74LS30
U21 - 7410
U22, U23, U25, U27 - 74197 or 74LS197
U29 - 2708 EPROM or optional 2716 EPROM
U30 - 2708 EPROM (optional)
U31, U32 - 2114
U35 - 6850

RESISTORS

R1, R2 - 1 kohm
R3 - 5.6 kohm
R4 - R6 - 4.7 kohm
R7 - 180 ohm
R8 - R10 - 100 ohm
R11 - 470 ohm
R12, R13 - 10 kohm
R14, R15, R17 - 2.7 kohm
R16 - 10 kohm (SIP)

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TRANSISTORS

Q1, Q2 - 2N2904
Q3, Q4 - 2N5135
Q5, Q6 - 2N5138
Q7, Q8 - LM340T5

MISCELLANEOUS

X1 - Crystal, 4 Mhz

-end-

Appendix A1
*** SYSTEM BUS ***

CON-DUCT-OR	MNEMONIC or FUNCTION	OPTIONAL FUNCTION	DESCRIPTION
1	1200b	--	System 1200 baud bit rate for serial I/O channel.
1	--	A19	Extended Address line. Refer to section 3.4.1.
2	600b	--	System 600 baud bit rate for serial I/O channel.
2	--	A18	Extended Address line. Refer to section 3.4.1.
3	300b	--	System 300 baud bit rate for serial I/O channel.
3	--	A17	Extended Address line. Refer to section 3.4.1.
4	150b	--	System 150 baud bit rate for serial I/O channel.
4	--	A16	Extended Address line. Refer to section 3.4.1.
5	110b	--	System 110 baud bit rate for serial I/O channel.
5	--	DMABRQ	Wired-OR bus request line. When brought low, suspends processor execution and "tri-states" the bus for DMA data transfers (e.g.). Unlike the halt sequence, DMABRQ is granted immediately. Refer to section 3.5.

6	$\overline{HALT}$	--	Wired-OR line halts the processor and frees the system information bus for external control.
7	BS	--	Bus Status line. Goes high to acknowledge a halt, bus grant or interrupt. BS and BA, which are valid on the falling edge of Q, determine the status of the processor:

BA	BS	STATUS
0	0	Normal
0	1	Interrupt acknowledge
1	0	Sync acknowledge
1	1	Halt acknowledge or bus grant

8	BA	--	Bus Available line. Goes high to acknowledge a processor halt, bus grant or sync.
9	$\overline{RESET}$	--	When low, resets the MPU registers and interfaces, and loads the ROM operating system.
10	R/$\overline{W}$	--	READ/$\overline{WRITE}$ line. Reads from memory or I/O when high; writes to memory or I/O when low.
11	$\overline{VMA}$	--	Valid Memory Address. Normally high line that goes low when a valid processor address is output onto the bus.
12	$\overline{E}$	--	Clock line. Data out of the processor is valid during a WRITE on the rising edge of $\overline{E}$. Data is clocked into the processor during a READ on the rising edge. Identified as Ø2 for the 6800 SS-50 bus.

13	$\overline{Q}$	--	Clock line. Leads $\overline{E}$ by approximately 90 degrees. High-to-low transition indicates a valid address has been output on the address bus. Data is latched on the rising edge of $\overline{E}$. Identified as UD1 for the 6800 SS-50 bus.
14	$\overline{FIRQ}$	--	Wired-OR maskable single-level Fast Interrupt ReQuest to the processor card. Has priority over $\overline{IRQ}$. Stacks only condition code register and program counter.
15	$\overline{IRQ}$	--	Wired-OR Interrupt Request line. Maskable, single-level interrupt request to the processor. Stacks entire machine state.
16	$\overline{NMI}$	--	Non Maskable Interrupt. A negative edge on this input signal initiates a non-maskable interrupt. $\overline{NMI}$ cannot be inhibited by the program and has a higher priority than $\overline{FIRQ}$, $\overline{IRQ}$ or software interrupts. Saves the entire machine state on the hardware stack.
17	$\overline{MRST}$	--	Master Reset. Unconditioned input from panel Reset switch on 6800 SS-50 bus computers.
17	--	MRDY	Memory Ready. Bus wired-OR control line "stretches" the $\overline{E}$ clock up to 10 microseconds to accommodate slow memory or peripheral devices.

-more-

18		--	Index pin. Unused line.
19	+16 VDC	--	Filtered but unregulated.
20	-16 VDC	--	Filtered but unregulated.
21-23	+9 VDC	--	Filtered but unregulated.
24-26	GND	--	Ground.
27-42	A0 - A15	--	Address lines.
43-50	$\overline{D7}$ - $\overline{D0}$	--	Data lines.

-end-

Appendix A2
SBC/9(tm) MEMORY MAP

ADDRESS (hex)	FUNCTION
0000-EFFF	Reserved for external memory (61 Kbytes)
F000-F3FF	RAM (1 Kbyte, two on-card 2114 ICs)
F400-F7DF	Reserved for external I/O or RAM
F7E0-F7FD	Buffered parallel I/O
F7FE-F7FF	RS-232-C Serial I/O (ACIA)
F800-FBFF	ROM #2 (optional)
FC00-FFFF	ROM #1 (operating system)

end - Appendix A2

Appendix A3
(Reserved)

Appendix A4
SERIAL I/O PIN ASSIGNMENTS & CONNECTIONS

MNEMONIC		PIN ASSIGNMENT		
Percom	SWTP	Molex Conn.	'D' Conn.	Term. Strip
TxC	CO	2	--	TSe-2
RxC	CI	3	--	TSe-1
RxD	RI	5	3	TSa-2
TxD	RO	6	2	TSa-1
DCD	*	8*	8	TSc
RTS	*	9*	4	TSu
CTS	*	10*	5	TSv

* Pins 8, 9 and 10 are SS-30 bus TTY lines TO, RC and TI, respectively.

Molex pins 1, 4 and 7 are ground (GND), +5 vdc and -16 vdc, respectively.

Pins 6 and 20 of the optional subminiature 'D' connector are connected via TSb and TSd, respectively, to +5-volt through pull-up resistor R17.

Data Carrier Detect (DCD) and Clear-to-Send (CTS) inputs, which must be at HIGH for proper operation of the ACIA, may be connected to either the Data Terminal Ready line -- from the data terminal -- or to the +5 vdc line at pin 4 of the Molex connector.

TxC - Transmit Clock
ACIA Tx Clk input. Used to clock transmitted data. SWTP MP-C/S mnemonic is CO. TxC is connected to RxC (CI) unless a self-clocking cassette interface is used. See paragraph 3.7.

RxC - Receive Clock
ACIA Rx Clk input. Used to sync received data. See paragraph 3.7.

RxD - Receive Data
ACIA Rx Data line through which serial data is received. SWTP MP-C/S mnemonic is RI. Used when interfacing to data terminal or modem. If RxD is not used, jumper to ground (pin 1 of Molex connector).

TxD - Transmit Data
Line used for serial data output to data terminal, modem or other devices. SWTP MP-C/S designation is RO. If TxD is not used, leave open.

-more-

DCD - Data Carrier Detect
ACIA input. Inhibits and initializes receiver section. High-to-low transition interrupts MPU to indicate carrier is lost.

RTS - Request-to-Send
ACIA output. Enables MPU to control a modem or peripheral via the data bus. A HIGH level should be interpreted as ON.

CTS - Clear-to-Send
ACIA input. When CTS goes low, transmission of data to ACIA from processor is inhibited, but characters currently in ACIA buffers are transmitted to the modem or other peripheral. A HIGH level should be interpreted as ON and a low level as OFF.

end - Appendix A4

Appendix A5
USING THE PERCOM LFD-400/800 MINI-DISK SYSTEM WITH THE SBC/9(tm)

The Percom MPX/9(tm) program is a 6809 disk operating system (DOS) for the Percom series of LFD disk storage systems.

The MPX/9(tm) is designed to operate with PSYMON(tm), the system monitor for the Percom SBC/9(tm) Single-Board Computer/MPU card.

*** CAUTION ***

MPX/9(tm) works only with PSYMON(tm) version 1.10 or later. A version printed in '68' Micro Journal magazine will not work with MPX/9(tm).

MPX/9(tm) consists of a 1-Kbyte ROM with low-level drivers accessible through device control blocks (DCBs), and a minidiskette containing the command and utility processor plus a "boot" for loading the minidiskette code into system RAM.

The MPX/9(tm) features position-independent code. This allows the user to install the MPX/9(tm) ROM in any of the three sockets provided on the LFD disk system controller card. Moreover, it means the minidiskette code may be loaded into any unprotected RAM space.

Besides position-independent code, the MPX/9(tm) also features mnemonic error reporting codes; file manipulation by name instead of by drive and sector numbers as is done under MINIDOS/MPX, the Percom 6800 two-ROM DOS; and, the accommodation of disk-resident transient commands which permit MPX/9(tm) to be extended indefinitely.

For Percom LFD disk systems presently equipped with MINIDOS/MPX, the addition of MPX/9(tm) will extend the disk system for operation with either a 6800 or 6809 computer, without contention between systems.

The MPX/9(tm) ROM may be installed in any of the three ROM sockets provided on the LFD controller card. However, if the MINIDOS/MPX system is presently installed, the MPX/9(tm) ROM must be installed in socket 3 for harmonious operation with either the 6800 MINIDOS/MPX system or the 6809 MPX/9(tm) system.

The MPX/9(tm) ROM code resides in 1-Kbyte of memory space, and is addressed at C000, C400 or C800 (hex) depending on whether the ROM IC is installed in socket 1, 2 or 3 on the LFD controller card. The program initializes RAM and loads the "boot" on the minidiskette into 0100 (hex).

The minidiskette code self-loads into 4-Kbytes, beginning at the first unprotected 4-Kbyte boundary below the disk controller. The LFD controller (MINIDOS/MPX) is normally mapped at C000 (hex).

*** CAUTION ***

The MPX/9(tm) minidiskette program requires a full 4 Kbytes of RAM. An error will result if the starting point found by the "boot" is less than four Kbytes.

end - Appendix A5

Appendix 6
WINDEX(tm) DRIVER PROGRAM AS OPTIONAL EPROM

WINDEX(tm) is a driver program for the ELECTRIC WINDOW(tm), Percom's SS-50 bus memory-resident video display generator/conroller**. A WINDEX(tm) ROM may be installed in the second EPROM socket of the SBC/9(tm).

The ELECTRIC WINDOW(tm), WINDEX(tm), a parallel keyboard and a video monitor together comprise a software-controlled video data terminal that far exceeds the adaptability of most terminals, and costs much less.

When PSYMON(tm) is initialized (by reset, for example) its "look-ahead" feature checks for the presence of a second ROM -- in this case, WINDEX(tm). Since the WINDEX(tm) ROM is present, PSYMON(tm) executes a subroutine call to the WINDEX(tm) initialization routine and the I/O vectors initially set up by PSYMON(tm) -- for I/O operation through the on-card serial interface -- are re-vectored to the I/O drivers in WINDEX(tm). The WINDEX(tm) drivers, therefore, control the ELECTRIC WINDOW(tm) display.

WINDEX(tm) source code is available on Percom LFD-400(tm) mini-disk compatible disks from the Percom Users Group.

** The fast, memory resident ELECTRIC WINDOW(tm) generates all ASCII displayable characters plus Greek letters and other symbols and provides for an optional character generator for user-defined symbols. Characters are in easy-to-read 7x12-dot format with true baseline descenders. Character-store memory is included on the controller card.

end - Appendix A6

Appendix A7
A WORD PROCESSING SYSTEM USING THE SBC/9(tm)

The Percom SBC/9(tm) is both a 6809 upgrade MPU card and a stand-alone computer. In the application discussed below, the SBC/9(tm) is used as the computer for an inexpensive, full-capability word processing system. A functional block diagram of the system is shown in Figure A7-1.

As shown in the figure, the SBC/9(tm) provides the system interface for the keyboard, printer and a modem, in addition to performing the central processing function. The on-card 1-Kbyte RAM is used for system stacks, I/O buffers and I/O configuration parameters.

The video display generator/controller is a Percom ELECTRIC WINDOW(tm). A Leedex Video 100-80 is one of many B/W monitors suitable for this application. The ROM WINDEX(tm) driver for the video card is installed as U30 in the second on-card EPROM socket of the SBC/9(tm), and the I/O vectors initially set up by PSYMON(tm) (for the SBC/9(tm) ACIA) are re-vectored to WINDEX(tm) I/O drivers. See Appendix A6.

A Percom dual LFD-400(tm) mini-disk system is used for storage. The two-drive version accommodates word processing tasks such as the merging of selected segments of an input file to automatically create a new file and store it to an output disk. This is accomplished under control of MPX, the LFD-400(tm) disk operating system, as discussed in Appendix A5.

The keyboard, a Keytronic 60-key Word Processor keyboard or similar, is interfaced through the SBC/9(tm) parallel I/O channel.

Both the printer and modem are interfaced through the SBC/9(tm) serial channel. Both operate at the same baud. When two I/O devices are connected to the SBC/9(tm) serial port, as in this case, care must be taken to strap the different "handshaking" signals of each device in a way which prevents the inadvertent control of one device by the control signals of the other. Also, the parallel load should not decrease the transmit data levels to less than +3 volts for a Space or more than -3 volts for a Mark.

Two Percom 16-Kbyte RAM cards are used for memory. These provide ample memory for system programs and file buffer space.

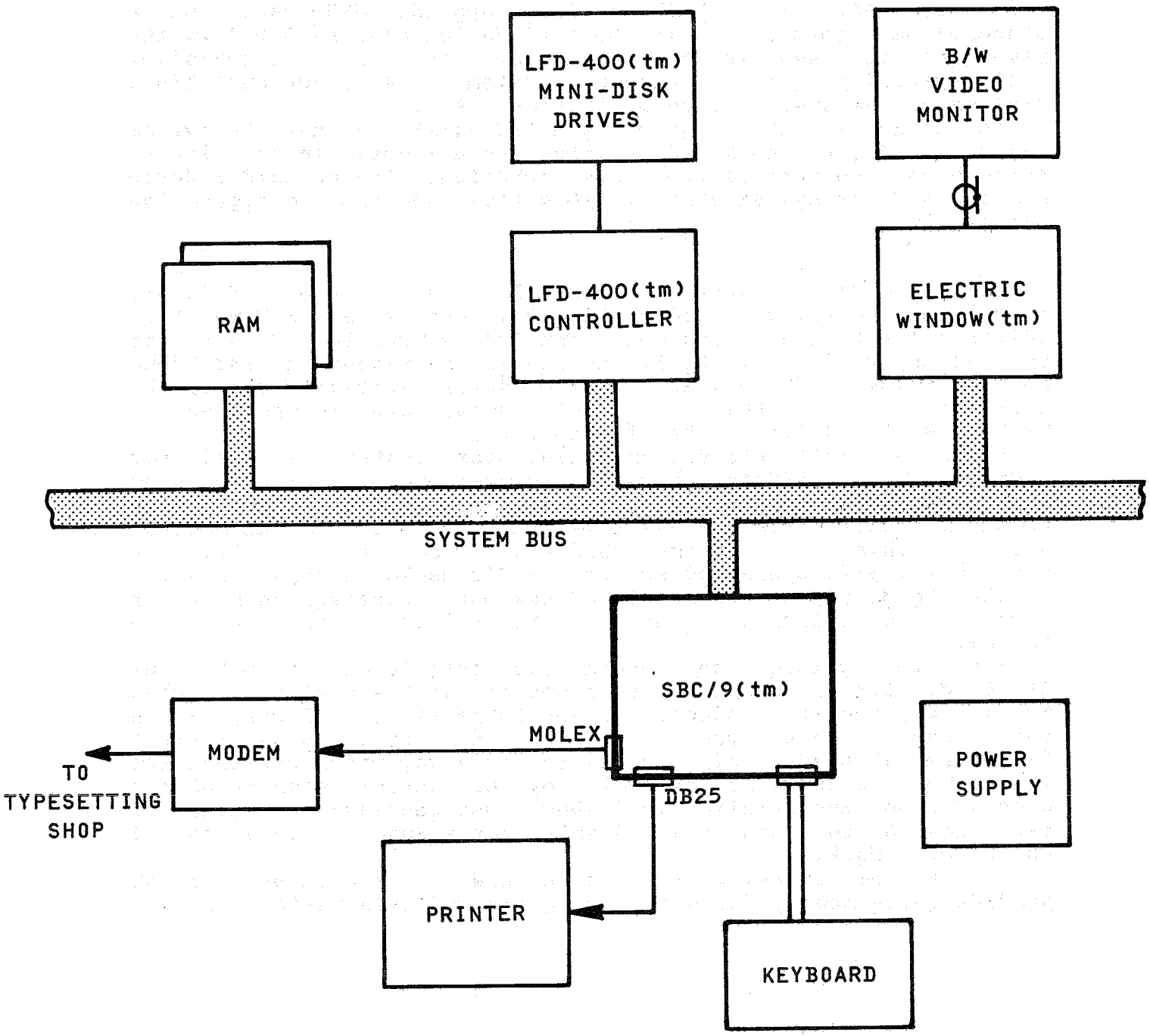


Figure A7-1 WORD PROCESSING SYSTEM FUNCTIONAL BLOCK DIAGRAM

-end Appendix A7-

*** HOW TO ORDER PARTS AND OPTIONAL ITEMS ***

HOW TO ORDER: Order by mail...we're as near as your mailbox... or order by phone.

TOLL-FREE PHONE ORDERS: To save you money and insure prompt service, we've installed a toll-free number: 1-800-527-1592 FOR PLACING ORDERS ONLY. In Texas, and for Customer Service, dial (214) 272-3421. We cannot transfer calls received on our toll-free number to other departments -- please help us serve you better by dialing the correct number.

PROMPT SERVICE: We ship the cheapest, fastest way. We use UPS up to 50 lbs. per item, 100 lbs. per shipment. We use truck-freight for large or heavy shipments. Transportation charges collected on delivery.

COD ORDERS: COD orders are accepted where possible.

OPEN ACCOUNT TERMS: Net 10 days to rated firms.

TEXAS SALES TAX: Texas law requires that we collect 5% sales tax on all shipments in Texas.

MINIMIUM ORDERS: We will add a handling charge of $2.00 to all orders totalling less than $15.00.

DAMAGED SHIPMENTS: Have carrier note if received in damaged condition, then file claim. About concealed damage: contact carrier for inspection, then file claim. Save the shipping carton.

*** HOW TO RETURN A UNIT FOR REPAIR ***

You have done everything you know how to do. You have read and reread the instruction manual and technical memos but you still can't get the ^$(&@ thing to work!

Then it is time to let us help. We have yet to find a sick unit that cannot be restored to full health and vigor.

There are a few things you can do to help us when you return a unit for repair.

1. Write or call for return authorization before returning any merchandise. RETURNS WITHOUT AUTHORIZATION WILL BE REFUSED.

2. When you return a unit for repair, enclose a complete description of the problem.

*** NOTE ***

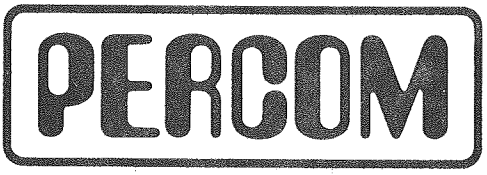
Questions that do not relate to the reason the unit is being returned for repair must be sent in under separate cover.

3. OUT-OF-WARRANTY repairs are performed for a labor charge of $30.00 plus parts and shipping. If we find that a unit is functioning properly as received and does not require any service, the CHECKOUT CHARGE is $15.00 plus return shipping and insurance. Do not enclose any payment. The unit will be returned C.O.D. for authorized repairs and shipping.

4. When returning a unit for repair, pack it in a large carton with at least 3" of padding on all sides. We will not attempt to service any unit if there is shipping damage until the claim is settled (a real hassle). Ship prepaid by UPS or INSURED PARCEL POST to:

Percom Data Co.
Service Dept.
211 N. Kirby
Garland, TX 75042

We try to turn most repairs around within one week.



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