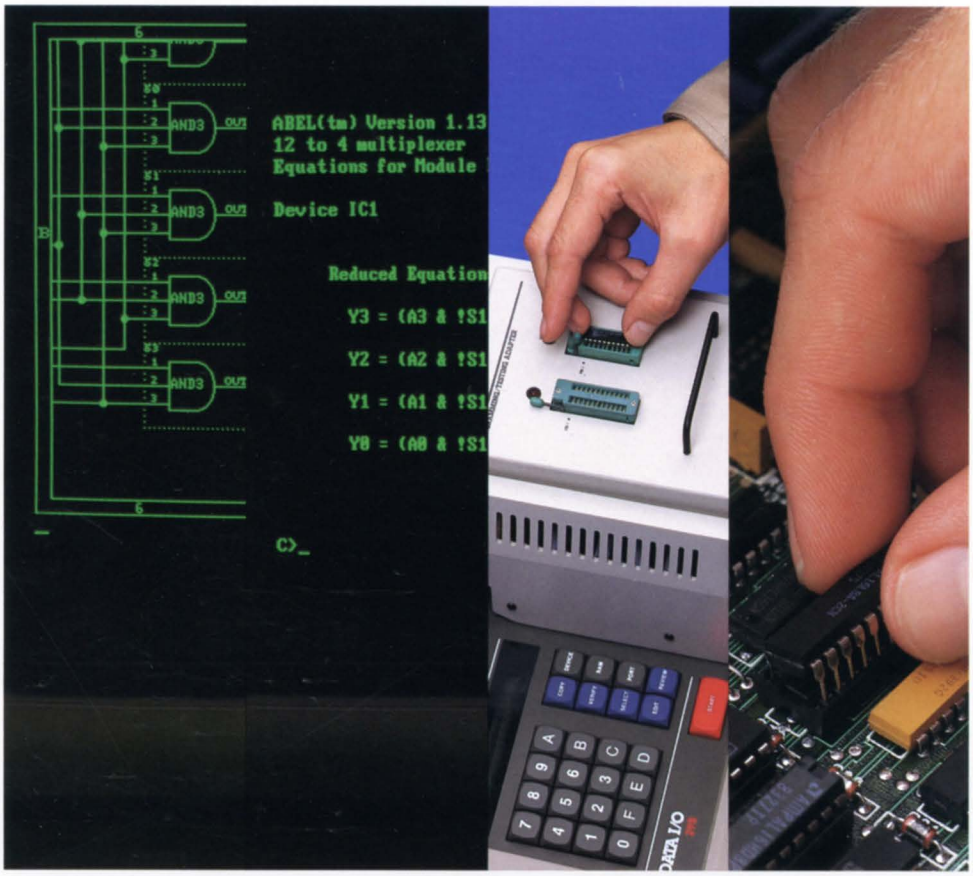
CONCEPT TO SILICON



AN INTRODUCTION TO THE PERSONAL SILICON FOUNDRY.™

DATA I/O

WHAT IS A PERSONAL SILICON FOUNDRY?

A complete Personal Silicon Foundry fits on your desk and contains all the hardware and software needed for design, programming and testing of PLDs.

Designing with programmable logic devices (PLDs) has changed dramatically over the past few years. Devices are more powerful and complex than ever, and more people are using PLDs in more ways. Gone are the days when PROMs were just for storing program data and PAL®s were for simple collection of extra random logic on a board.

Advanced design and programming tools as well as PLDs with programmable I/O, feedback, and registered outputs have made programmable logic the solution to many design problems. But what does all this mean to the engineer?

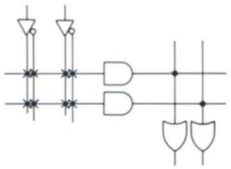
It means dealing with an increasing number of choices—and decisions. Not only must a designer choose an appropriate PLD for an application, he or she is also faced with implementation questions: What design tools are available? From what manufacturer? Will the tools I buy let me use the devices I want to? What programmer should I use to program my PLD? Will the PLD work the way I want it to once it's programmed?

Data I/O's Personal Silicon Foundry™ provides simple answers to these questions by providing complete design, programming and testing of almost every PLD and PROM on the market. In one comprehensive system that fits on a desk, the Personal Silicon Foundry contains all the software and hardware tools you need to fully utilize PLD and PROM technology. And because many processes are automated, using this technology is faster than ever before. In a matter of hours, a Personal Silicon Foundry lets you transform design concepts into programmed and tested devices. Taking concept to silicon easily—the Personal Silicon Foundry.

WHY AND WHEN TO USE PLDS.

For any given design problem, there's a variety of possible solutions. PLDs are just one of these; there are also full-custom ICs, standard cells, semi-custom gate arrays, and, at the opposite end of the spectrum, random logic. When to use which technology is a decision based on many factors. Even among the PLDs—PALs, FPLAs, FPLSs or PROMs—each type of device is better suited to certain types of applications. Let's take a look at the advantages and disadvantages of using PLDs to solve design problems.

PALs, with a programmable AND array and fixed OR array, lend themselves to easy implementation of sum-of-products logic equations.

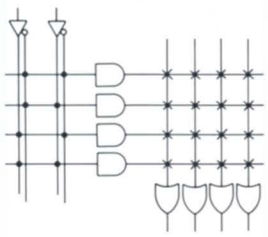


× indicates programmable fuselink

Historically, PLDs were often used merely to reduce the chip count on a board by collecting random logic gates into one IC. Or, in the case of PROMs, the device provided convenient storage for program data.

Though these are still useful applications of PLDs, the powerful programmable devices available today have many more uses. For example, FPLSs have allowed complete state machines to be programmed into one IC, thus putting PLDs at the heart of many designs. Other features like programmable polarity, programmable inputs and outputs, and simple increases in the number of product terms make PLDs a viable alternative even to custom gate arrays.

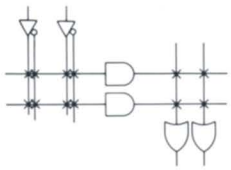
A PROM's fixed AND array and programmable OR array makes it ideal for storage of program data. The AND array provides fixed addresses by which data programmed into the OR array can be accessed. PROMs can also implement sum-of-products logic.



× indicates programmable fuselink

The case for choosing PLDs over random logic is a simple one. In almost any design, the primary concern is to reduce chip count, power consumption and board space. Because one PLD can hold the equivalent of anywhere from four to 20 fixed-function TTL devices, they certainly satisfy these needs. PLDs used in place of fixed-function random logic devices also can reduce your parts inventory because a relatively small selection of PLDs can provide the function needed for a large number of designs.

FPLAs (Field Programmable Logic Arrays) offer even more flexibility with programmable AND and OR arrays. FPLSs (Field Programmable Logic Sequencers), like some PALs, also have registered outputs and feedback paths.



× indicates programmable fuselink

Can PLDs be used instead of semi-custom gate arrays, standard cells, and full-custom ICs? Yes, and no. In the sense that PLDs and the other higher-level ASICs (Application Specific ICs) can implement general logic functions, they are similar. However, in architecture, cost, and development time, they differ greatly.

For frozen designs that are to be produced in quantities of thousands or millions, gate arrays, standard cells, and custom ICs are usually the best choice. They are extremely small and efficient implementations of the desired logic function. Their high initial development costs are generally offset by the large quantities produced.

It is when design changes are probable or production quantities are low that PLDs are the better solution than gate arrays and custom ICs. Even when it may take several PLDs to implement the same logic as one gate array, the low cost of PLDs (usually less than $5.00) makes them economically attractive.

PLDs also can be used for prototyping designs that eventually will be produced as semi-custom or custom ICs. In this way, a complete system can be designed, prototyped, and debugged without the high prototype cost of other ASICs. Once the design is frozen and ready for production, the PLD design can be converted to an ASIC. For a more comprehensive comparison of PLDs and other ASICs, see the accompanying chart.

FACTOR	PLD	SEMI-CUSTOM GATE ARRAY	STANDARD CELL, CUSTOM IC
Second Sources	Numerous	Limited	Limited to Very Limited
Design Time	Hours	Weeks	Months
Prototyping Time	½ Day	Weeks	Weeks
Development Cost	Cost of Device $2-$50	$10K-$50K	$25K Min. (Std. Cell) $160K Min. (Custom IC)
Redesign Costs	Design + Prototyping Time + Development Cost (Low)	Design + Prototyping Time + Development Cost (High)	Design + Prototyping Time + Development Cost (Higher)
Min. Viable Purchase Quantity	1	Thousands	Tens of Thousands to Millions
Design Tools Required	Low-cost PC, Programmer, Low-cost PLD Development and Testing Software	Specialized Workstation, Minicomputer, Sophisticated Autorouting Software	Specialized Workstation, Minicomputer, Sophisticated Autorouting Software

Comparison of PLDs With Other Application Specific ICs.

Courtesy of EE Times.

USING PLDS: THE TOOLS REQUIRED.

Using a PLD is a process of describing the desired logic and programming a device. How this process is accomplished can, however, significantly affect the outcome. For best results, all of the following steps should be performed:

Describe the design.

Reduce the design so it uses as few product terms as possible.

Simulate the design to verify its logic functions before the PLD is programmed.

Perform fault analysis to determine device testability.

Generate test vectors to test the PLD once it's programmed.

Program the PLD.

Test the PLD.

Document the design.

These steps will ensure that PLDs are used accurately and efficiently. Let's look at each step in detail.

DESIGN DESCRIPTION. The description of PLD designs should be as easy and as natural as possible. The less translation that takes place between the way you conceive a design and the way you describe it, the less chance there is for error. PLD designs can be described by older methods such as marking Xs on a PLD schematic or using assembly-type languages; or, newer tools can be employed such as sophisticated high-level design languages and CAE schematic design systems. High-level languages and CAE schematic design packages that support a wide range of devices generally offer the most flexibility and are more natural expressions of a design.

REDUCTION. PLDs have a finite number of product terms that can be used up quickly by large or complex designs. Therefore, your design should be reduced so it uses as few product terms as possible. Logic reduction can be performed manually using Karnaugh maps and DeMorgan's theorem, or automatically with logic reduction software. Automatic logic reduction is faster and less tedious than manual methods.

SIMULATION. A good logic simulator can make big differences in overall results with PLDs. A simulator can detect and report design errors before a device is programmed, thus saving the cost and time of misprogramming a device. If the simulator is fast and easy to use, it can also

encourage designers to experiment with new designs or techniques, resulting in better solutions to design problems. Simulation is accomplished by applying sets of inputs to a design and checking the simulated outputs against expected results.

FAULT ANALYSIS AND TEST VECTOR GENERATION. When testability of programmed devices is a concern, fault analysis and automatic test vector generation are invaluable tools. The goal is to ensure that a programmed device can be adequately tested for correct operation. Fault analysis should pinpoint portions of a design that will make a device untestable so the design can be corrected.

Once the device is determined to be testable, the tests that check its operation must be developed. Because test generation is a long, tedious process if done manually, automatic methods are preferred. Fast, automatic fault analysis and test generation encourage designers who might otherwise overlook this step to make sure a device can be fully tested.

PROGRAMMING. The PLD programmer is the final link between a design concept and the PLD that implements that concept. Each different type of device—PALs, FPLAs, FPLSs, PROMs, EPROMs, EEPROMs—requires different programming techniques. Many different types of programmers exist on the market. Some program only one type of PLD or PROM; other programmers offer comprehensive support for a wide variety of devices. Programmers should be accurate, easy-to-use and fast.

TESTING. Programmed devices should always be tested for correct operation. Testing is most easily accomplished if it is performed by the PLD programmer subsequent to programming. Errors reported by device testing routines should be clear and comprehensive.

DOCUMENTATION. Design documentation should be performed throughout all the previous steps. Design documentation should include readable design descriptions, device pinouts, net lists (for larger systems), fault-analysis reports and any other information needed to fully document your design.

THE PERSONAL SILICON FOUNDRY—TAKING CONCEPTS TO SILICON.

The Personal Silicon Foundry is the first comprehensive system to meet every requirement of the PLD development process. Developed by Data I/O and FutureNet, the Personal Silicon Foundry combines PC-based CAE and PLD design tools that are recognized industry leaders into one complete package.

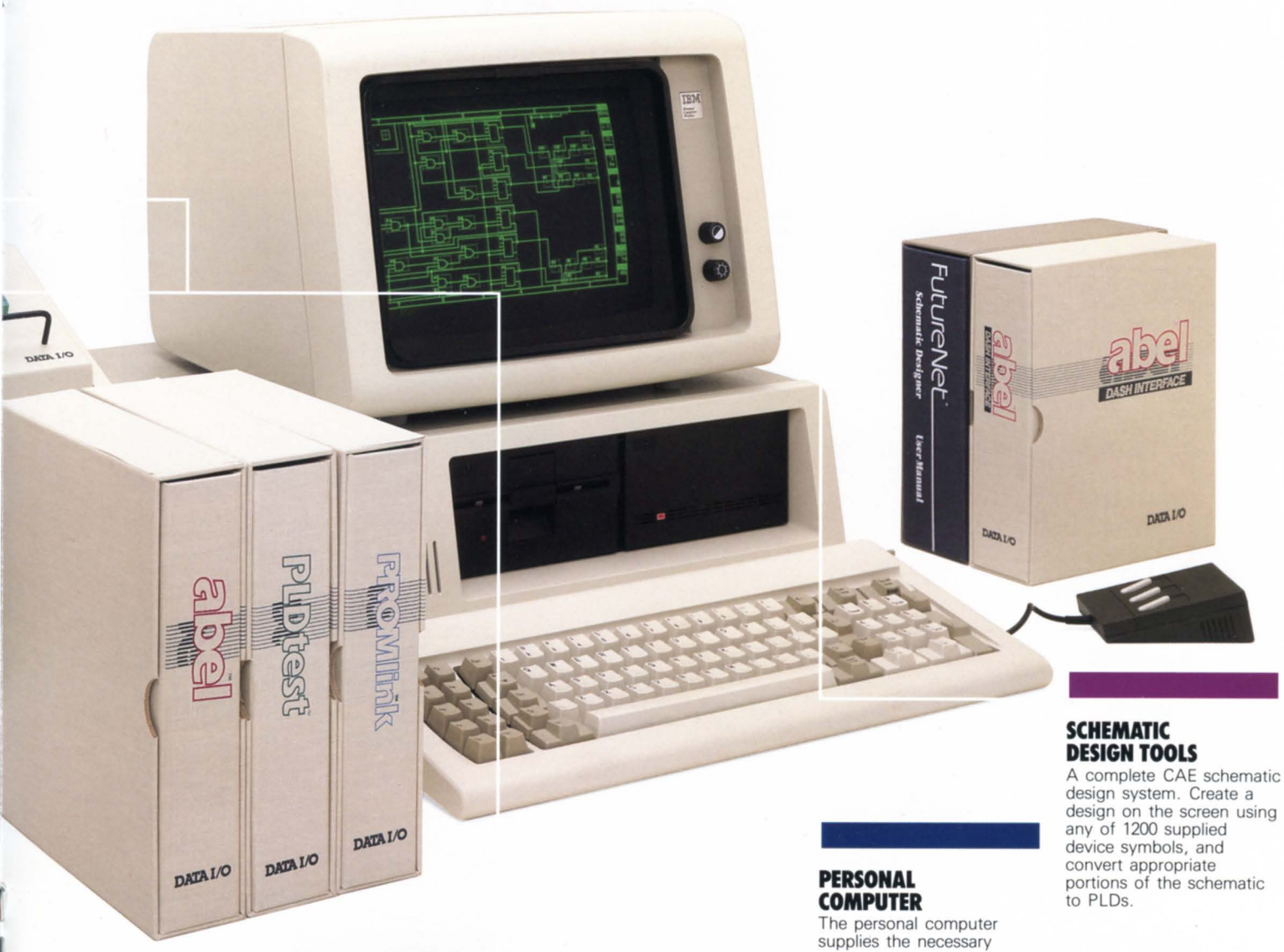
A Personal Silicon Foundry (PSF™) encompasses and optimizes every step of the design process: design description, reduction, simulation, fault analysis, test vector generation, programming, and testing. PLD designs can be entered using any combination of Boolean equations, truth tables, state diagrams or schematics. Every process that can be

PLD PROGRAMMER
A choice of two programmers offers complete programming and testing support for virtually every PLD on the market.

automated is automated and complete documentation is generated from start to finish.

The Personal Silicon Foundry frees designers to do what they do best—design—and relegates tedious mechanical tasks such as logic reduction and test vector generation to automated tools. The result is easy, efficient PLD design development, with a complete design cycle often taking less than half a day.

A COMPLETE PSF ON ONE DESK. The Personal Silicon Foundry is a specialized system of hardware and software tools surrounding an IBM® XT or AT personal computer. The major components of a PSF are the personal computer, PLD design software, schematic design tools and a PLD programmer. A complete PSF fits easily on a standard size desk and can be tailored to meet your specific needs.



DESIGN SOFTWARE
This portion of the PSF provides a high-level design language, logic reduction, simulation, fault analysis, test vector generation, and full screen control of the PLD programmer.

PERSONAL COMPUTER
The personal computer supplies the necessary processing power and storage for the PSF. It can also be used for project management and other related tasks using your existing software.

SCHEMATIC DESIGN TOOLS
A complete CAE schematic design system. Create a design on the screen using any of 1200 supplied device symbols, and convert appropriate portions of the schematic to PLDs.

DESIGN SOFTWARE

CONCEPT

PROGRAM

Purpose: Design entry, processing, and implementation support.
Features: High-level design language, logic reduction, simulation, fault analysis, test vector generation, full-screen programmer control.
Options: None. Entire package included with every PSF.

The design software includes three leading PLD design development tools from Data I/O: ABEL™, PLDtest™ and PROMlink™ ABEL is a high-level design language with logic reduction and simulation capabilities. ABEL lets you describe designs using any combination of Boolean equations, truth tables, or state diagrams, and includes macros, set notation and a full set of operators.

PLDtest provides complete fault analysis to determine a device's testability, quickly identifying untestable portions of a design. PLDtest can grade user-supplied test vectors, or can automatically generate complete sets of test vectors for combinatorial or registered devices with preload capability to fully test a device. PLDtest accomplishes in minutes what used to take hours.

PROMlink provides control of the PLD programmer from the PC screen, including menus for selection of devices and manufacturers, as well as full-screen editing of programmer RAM data.

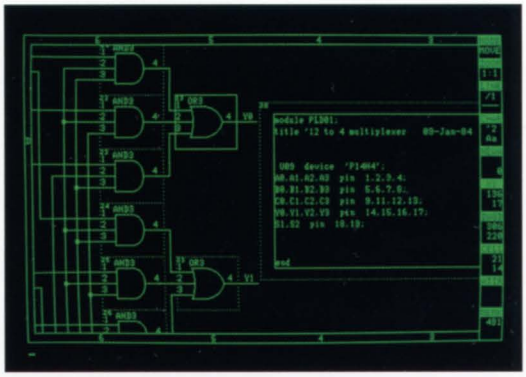
SCHEMATIC DESIGN TOOLS

Purpose: Design entry and editing on the PC screen.
Features: High-resolution graphics, mouse, library of 1200 logic elements, sophisticated schematic editing. Automatic translation of schematic data into the ABEL language format.
Options: Monochrome or Color.

Schematic design tools are provided by FutureNet's DASH™-2 or DASH-3C systems. Both systems provide entry and editing of design schematics directly on the PC screen.

Editing capabilities include "tag and drag" and "rubber banding" for easy movement of symbols or text on the screen, area definition, zoom, windows and on-line logic element selection. Complete net lists, lists of materials and design check reports are generated automatically. Choose DASH-2 for monochrome systems, DASH-3C for schematic design in color.

Also included with the schematic design tools is DASH-ABEL™, a tool that converts portions of a DASH schematic to the ABEL design language. This lets you use PLDs to implement logic you've created with DASH schematics. Because the schematic is converted to the ABEL language format, you can use all of ABEL's features, including logic reduction and simulation.



PLD PROGRAMMERS

Purpose: Programming and testing of PLDs.
Features: Fast, accurate programming using algorithms approved by semiconductor manufacturers. Complete testing using test vectors, Logic Fingerprint™, and fuse verification.
Options: Varying levels of device support. Support for PROMs.

Programming and testing of PLDs is provided by the Data I/O 29B or 60A programmers. Both programmers provide complete, accurate programming and testing. The 29B Universal programmer with LogicPak™ and UniPak™ 2B provides comprehensive support for virtually every PLD and PROM on the market—over 1000 devices. The 29B can be configured without the UniPak 2B if PROM support is not needed.

29B

Universal Programmer with expandable support

LogicPak — Support for 20-, 24-, 28- and 40-pin PLDs

UniPak 2B — Adds PROM, EPROM and EEPROM support

The 60A Logic Programmer is a lower-cost alternative, supporting most popular PLDs (PROMs excluded).

60A

Support for all available 20-, 24- and 28-pin PLDs

Note: See the 29B and 60A specification sheets available from Data I/O for complete lists of supported devices.

PERSONAL COMPUTER

Purpose: Computing support for PSF software and hardware.
Features: General purpose personal computer with hard disk and floppy disk data storage. Includes C-Itoh printer.
Options: IBM XT or IBM AT

The personal computer is required for the design software, schematic design tools and data storage. It can also help with other personal computing tasks such as project management or word processing using your existing software.

Configuration options include the choice of an IBM XT or AT and the choice of enhanced color or monochrome displays for either.

IBM XT includes: 256k RAM, 10M-byte hard disk, 360k-byte floppy disk drive, display, keyboard and PC-DOS.

IBM AT includes: 512k RAM, 20M-byte hard disk, 1.2M-byte floppy disk drive, 360k-byte floppy disk drive, display, adjustable display stand, keyboard and PC-DOS.

A C-Itoh Prowriter 2, Model 1550 SPN 15" printer and cable is included with either PC.

HOW TO CONFIGURE YOUR OWN PERSONAL SILICON FOUNDRY.

The Personal Silicon Foundry is easily configured to meet a variety of needs. Each Personal Silicon Foundry comes standard with the design software (see previous page), but beyond that the choices are yours.

There are three basic questions to consider in configuring your PSF: (1) What devices do you want to program? (This determines the PLD programmer.) (2) Do you want to take advantage of schematic input capabilities? and (3) Do you already have an XT or AT personal computer?

For your convenience, these questions and the possible answers have been organized into a table (see below). Answer each question and you'll have configured your own custom Personal Silicon Foundry. It's that easy. And if you decide that a Personal Silicon Foundry will help you with your PLD development needs, contact one of our sales representatives. He or she will use this same information to place your Personal Silicon Foundry order.

QUESTION	ANSWER	PSF OPTION
What devices do I want to program?	Popular PLDs	60A PLD programmer
	Most Available PLDs	29B with LogicPak
	PROMs and Most Available PLDs	29B with LogicPak and UniPak 2B
Do I want schematic design input capabilities?	Yes, Enhanced Color	DASH 3C
	Yes, Monochrome	DASH 2
	No	—
Do I need a PC?	Yes, XT	XT System
	Yes, AT	AT System
	No	—

Use this table to configure your Personal Silicon Foundry. Answer each question by circling the appropriate answer. Then, look in the PSF option column to see which PSF options you need. Questions are color coded to correspond with option descriptions on the previous page.

IF YOU PURCHASE A COMPLETE SYSTEM. You can purchase a PSF as a complete system including an IBM XT or AT and the DASH schematic design tools, or you can add what you need if you already have a personal computer. Complete systems include a C-Itoh printer and DASH-STRIDES™ (see box), and all software is installed on the hard disk drive before shipment.

DASH-STRIDES! This hierarchical design aid for use with DASH-2 or DASH-3 is included with complete system purchases. DASH-STRIDES allows top-down organization of even the most complex systems and schematics. Changes to one level of a schematic are automatically reflected on all related levels.

AFTER-THE-SALE SUPPORT. To keep you abreast of the ever-changing PLD market and to make sure you have minimal downtime, Data I/O offers a wide range of PSF support and service. Choose from programmer calibration and update services, software update services, and complete service contracts with on-site or carry-in service for your IBM PC. PC service is provided by the Xerox® Service Group, with 82 service centers nationwide. PSF support and service, including technical support via telephone, is provided by our customer support centers nationwide.

DATA I/O, FUTURENET AND THE PSF. The Personal Silicon Foundry combines Data I/O's leadership in PLD support tools with FutureNet's expertise in PC-based CAE technology. Both Data I/O and FutureNet* have set standards in their fields—for products and for customer support. Representatives are located worldwide to answer any questions you may have about the Personal Silicon Foundry or other Data I/O or FutureNet products. See the back of this brochure for a listing of sales offices.

*FutureNet is a Data I/O company.

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MEXICO
Christensen, S.A. ..... 546-25-95 or 546-29-55
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OR

Contact the nearest Hamilton Avnet Office.

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