Interoffice Correspondence

- ☐ For Your Comments
- ☐ For Your Approval
- ☐ Please Take Action
- Due Date _____
- ☐ Call Me
- ☐ See Me
- ☐ Per Our Conversation
- ☐ Read, Initial & Return
- ☐ Please Route
- ☐ For Your Information
- ☐ Note & Return
- ☐ Note & File
- ☐ For Your Signature
- ☐ Please Advise Status
- ☐ Per Your Request
- ☐ Please Advise Appropriate Employees In Your Department

To: Bill Ellis, Gary Reilly, Bill To, Kyu Lee, George James

Date: January 15, 1983

CC:

From: Vic Belmondo

Subject: Trip Report, Visit to Silicon Valley December 14 through December 17

The attached notes are from my trip to JEDEC meetings and various semi houses in Silicon Valley. The trip was very valuable. Data I/O was received well by all customers. I will be requesting various people to follow up on specific action items.

VEB:lc VEB

Tuesday, December 14, 1982

JEDEC Bipolar:

No unexpected results. No work was done on JEDEC registration on bipolar logic devices.

I presented 3 suggested editorial changes to our format. Two of the three

1. A clarification of link numbering, and
2. Specification of legal ASCII characters

were OK'd. The third,

3. Keying off manufacturer part number

was not accepted for programming algorithm I.D.

Action:

1. Make changes to format, get copy to Jack Kinn
2. Work with Nap and Warren on alternate ideas for I.D. of programming algorithm.

L.S.I. Technology: (P.M.)

Keith Lobo, Mike, Kyu and I discussed computers, programs and software tools used in VLSI (6000 gate gate array design and production).

We discussed size of computers and languages.

In a discussion of testing of LSI gate array devices, Keith said that they only do the amount of testing requested by the customer - no more - or costs would increase. Testing is limited, therefore, in comparison to microprocessors because volume is lower. He suggests there may be a niche market for us, but can't guarantee.

He gave us a lead on a Ph.D. who worked with Distmeyer at Madison who is now at Bell Labs. Kyu will follow up.

Wednesday, December 15, 1982

M.M.I. Cyrus Tsu

Discussed current status - all OK. Started redesign of Fast PAL die. Wants to figure out one good fix and implement it.

Wants to qualify only 2 programmer manufacturers, and a maximum of 3.

M.M.I. (continued)

Concerned about telling the field about fix. Told him we can work in parallel, factory and field, after we get approval. Probably can tell field first week in January.

Says to expect to always reduce heating.

ECN control of approvals at M.M.I.: engineer to talk, but commitments will be through Charlie Bannon and Cyrus.

Expect parts with more pins than we have.

Wants confidence adapter for control - in field.

Corporate goal is 99% yield. Redundancy will be used to achieve this.

Textool sockets.

Wants people to calibrate their programmers; will add this to data sheets if we ask.

Ralph Burlock - Intersil 6716

P120 sold without 67C16. Need to add software to 120. Promised a temporary fix before Christmas, algorithm by January 15.

Cliff Biggers, A.M.D.

See new Data Book for new specifications.

Talked about PLDS vs. UniPak implementation of X4 registered parts. Need action and decision.

Cliff will have parts in March, customers in April - this is important.

We need to contact Bill Sievers to decide on procedures regarding who standardizes fuse maps for programmable Logic devices.

Bob Osan, Assisted Technology (Kyu, Mike Mraz, Mike Holley, Vic, Charlie)

Expressed proprietary nature of software and what it runs on, after several questions by Kyu. Made arrangements with Charlie to get equipment to him for checkout. Need to follow up this week to see if it happened.

SEEQ, Dan Leonard, Bill Smith

Implement Silicon signatures using one family for SEEQ. Approvals are OK. Dan wants to see a P120 in mid-February for approval.

Needs some clarification all machines, etc. Send him the bulletin we send to customers for P19 update, UniPak II, Gang II and PLDS.

SEEQ (continued)

See if we can get the Intel 2816 and the SEEQ 2816 at the same erase voltage. One is 9-15V, the other is 14-21V - - this allows the same code for both parts.

Die trace could be added via a select code. I suggested we supply select code to access it, then SEEQ can supply the hex decode to their customers. I forgot what pin is required to go to VHH to read these; it is a completely separate array. See Dan Leonard sheet.

Bill Smith (formerly of Signetics) said that Nap Cavlan probably will make the decisions behind Bob Barker at Signetics.

Source III - Bob Hartman, Art Aronson 

Thinking of large pinout programmable gate array devices. They are still in concept stage. They design 1000 gate gate arrays now. We suggested they bring address out like a PROM, making easier access to fuses. This would avoid programmer development charges.

They are a 4-person company.

Thursday, December 16, 1982

JEDEC MOS

Various ballots on nonvolatile RAMs and EEPROMs were passed. See attached sheets.

The Byte Wide task group was split up between strategic and tactical.

Don Knowlton from Intel will take strategic portion to define pinouts for word wide PROMs, etc.

Bill Owens of Xicor will probably replace Larry Jordan as chairman of Strategic Task Group. This covers electronic signature and other byte wide pinouts, etc., and X9 parts.

Little of interest was discussed. However, Bill Johnston of Fujitsu said that Fujitsu had approved the Intel algorithm for their parts.

Friday, December 17, 1982

Signetics - Bob Barker, Bruno, Dave Yeaton, George, George, George James

The meeting split into 2 groups - hardware and software.

Hardware issues:

1. PROMs

    82S135 = 1/2 of 82S147. Taken care of, just add to charts, assign codes. Charlie will get us samples.

2. 82S159, etc.

   They gave us new fuse address map. We owe them new software to implement.

3. In first quarter of '83 they will present us with all information on 24-pin skinny devices. We told them if it requires hardware development we have 6-9 month lead time.

The design diskette could save Bruno a lot of time. He is willing to be a B site. We send diskette and letter with limitations.

They think SD is hurting them. They want us to build a low-cost programmer. I said we can't, but were interested in educational board/package.

They have some parts that pass fuse verify but don't work in customer circuit. They said they fail fingerprint as well. We will evaluate samples if they send them and help out the customer. More advertising for us.

New AIM Algorithm

We discussed algorithm, they need 1 usec and 2 usec - 5 usec pulses on a #6 line. See attached specs. Gary Reilly will study problem and see if there is any way to implement on UniPak.

They still want us to keep total programming energy low. They made a comparison between Data I/O and other manufacturers. See attached sheet.

Intel - Bill Carney, Bob Davis, Don Knowlton:

Silicon Signature - Double-check method is OK. (Key in Family Pinout code and programmer checks if OK.)

256K bit parts out in March, need 256K bit RAM.

Still interested in joint promotions of intelligent programming.

Three items discussed were: intelligent identifier
87128 authenticated PROM
87100 operating system PROM

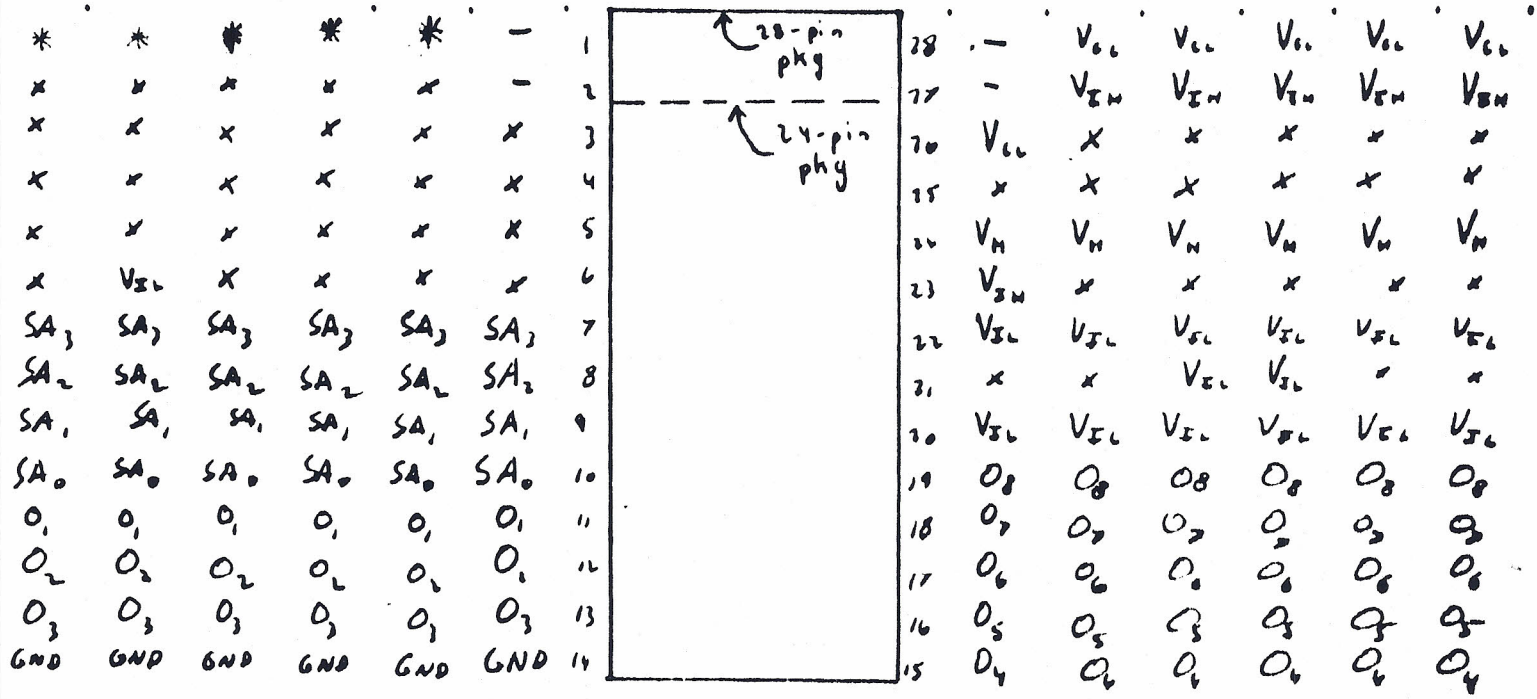
We spent three hours discussing these devices. They will visit in January. We will respond then with questions and schedules.

The other issue discussed was bipolar approval on UniPak. Don Knowlton promised to kick it up a level to get cooking on approval again. We should follow up early in January.

VEB:lc
Attachments

PIN ASSIGNMENTS - SILICON SIGNATURE™

SEEQ TECHNOLOGY, INC.



*	*	*	*	*	–	1	28	–	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
x	x	x	x	x	–	2	27	–	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}
x	x	x	x	x	x	3	26	V_{CC}	x	x	x	x	x
x	x	x	x	x	x	4	25	x	x	x	x	x	x
x	x	x	x	x	x	5	24	V_H	V_H	V_H	V_H	V_H	V_H
x	V_{IL}	x	x	x	x	6	23	V_{IH}	x	x	x	x	x
SA_3	SA_3	SA_3	SA_3	SA_3	SA_3	7	22	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
SA_2	SA_2	SA_2	SA_2	SA_2	SA_2	8	21	x	x	V_{CC}	V_{IL}	x	x
SA_1	SA_1	SA_1	SA_1	SA_1	SA_1	9	20	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
SA_0	SA_0	SA_0	SA_0	SA_0	SA_0	10	19	O_8	O_8	O_8	O_8	O_8	O_8
O_1	O_1	O_1	O_1	O_1	O_1	11	18	O_7	O_7	O_7	O_7	O_7	O_7
O_2	O_2	O_2	O_2	O_2	O_2	12	17	O_6	O_6	O_6	O_6	O_6	O_6
O_3	O_3	O_3	O_3	O_3	O_3	13	16	O_5	O_5	O_5	O_5	O_5	O_5
GND	GND	GND	GND	GND	GND	14	15	O_4	O_4	O_4	O_4	O_4	O_4

* - Function Pin, defined for device.

SA_{0-3} : Signature Address Lines

ameter inition	STAG	Data I/O Revx PIDS	Data I/O Logic Pack
Address			
VIH	4.5V	4.5V	4.5V
VIL	0V	0V	0
Tpp	350µs	1ms	1.4ms
td9	200µs	NA	NA
VCC			
VCCP	8.4V	8.4V	8.4V
Tvccp	120µs	200µs	240µs
td1	25µs	140µs	50µs
tr1	1.2µs	14µs	10µs
tf1	<1µs	50µs	480µs*
ogram/Verify			
td2	24µs	30µs	10µs
VIH	4.5V	4.5V	4.4V
VIL	0V	0V	0V
using Supply			
td3	26µs	25µs	40µs
tr2	20µs	12µs	20µs
td5	14µs	16µs	30µs
tf2	<1µs	≤1µs	35µs
td6	40µs	NA	NA
trobe			
td4	1-2µs	30µs	36µs
Pwe	16µs	24µs	14µs
td7	NA	NA	NA
unloaded data I/O	See picture		

*(32 µs LOADED)

S.B.
Dec 17 1982

12-16-82

Proposed 82A$195 (A.I.M.) Fusing Algorithm

1. Select address to be programmed.
2. Verify the output is in the "one state".
3. Raise Vcc to 8.75v
4. Raise output to 17v no faster than 1v/μsec.
5. Enable CE for 1 μsec.
6. Lower the output voltage, then Vcc.
7. Sense the output for a "0".
8. If the output is a "1" repeat fusing procedure steps 3 to 7 with increasing CE pulse width (1 μsec per step until the output is in the "0 state" - 5 μsec max.
9. When pattern is complete, readdress each programmed address and reprogram with a single 2 μsec CE pulse.

diode will not clamp

max = 110
min = 120

Proposed 82H$195 (A.I.M.) Fusing Algorithm

Comarco
George 407-746 1348