To: Sumner Averett
Vic Belmondo
Bill Ellis
David Hannaford
Mike Holley
Mike Mraz

From: Steve Witten

Subject: Signetics ABEL Contract

Bill Ellis, Mike Mraz and I will meet this Friday with Bill Smith of Signetics. The purpose of the meeting is to discuss the possibility of a contract from Signetics to develope an ABEL type language.

Here is some background:

- Bill Smith thinks it will take 3-6 man months of effort to develope the software.

- Signetics and Harris have a second source agreement on IFL. This means that any work we do for Sig. will also have the ownership of Harris.

- Russ DePina and Bill Smith discussed Bill's ideas for ABEL and Russ feels that they are basically sound. (See attached memos.)

- Bill Smith needs software which can be used in Data I/O programmers and also in Apples, DEC etc. Any software we develope would have to be capable of meeting this requirement.

- Bill Smith has $500K to spend on software. Besides ABEL he also will contract for a logic minimization program and a test vector generation program. (see attached Signetics writeup.)

The meeting at 3:30 in Sumner's office should cover these topics:

1. Are we interested in such a contract.

$30K 2. Under what business conditions should we accept it.

3. What kinds of contract definition should we insist on so that we avoid misunderstandings.

4. What resources would we use and what schedule could we meet.

Please be prepared to discuss these issues so that Bill Ellis and I will have guideline for our discussion with Signetics.

Steve Witten

5/11/82

Wayne Paulson
Vic Belmondo
Russ DePina

for your evaluation!

Steve Witten

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a subsidiary of U.S. Philips Corporation

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May 5, 1982

DATA I/O
10525 Willows Road N.E./C-46
Redmond, WA 90852

ATTENTION: STEVE WITTEN

Dear Steve:

Attached is a proposal for a different method of implementing Boolean Equation Entry for IFL. I believe that it solves the user interface problems that I have encountered using the current input method.

Please evaluate the proposal and contact me for a time at which we can discuss what it will mean for your equipment. You may contact me directly at (408) 746-3407.

Yours truly,

Bill Wiley Smith

BILL WILEY SMITH
Applications Manager
Bipolar Memory Division

BWS:vjo
cc
Enc.
I.D. #2334B

PROPOSED REVISIONS TO BOOLEAN ENTRY FORMAT

The current format for Boolean Equation Entry in support of IFL as proposed by Signetics in 1980 has some difficulties in use. This proposal addresses these problems. It may be used as an addition to work already completed or substituted for the previous submission in its entirety. The format given here for the FPLS should be considered as a minimum.

The problems that I have encountered with the present format relate to the ease of use and the structure of the entry method. This proposal is much more "user friendly" and is recognizable by logic designers as the equation structure that is normally used. I have underlined the user responses to the computer generated prompts.

HEADER: Same as previous proposal.

PIN LIST: Same as previous format except in the programming of multi-function pins. As the user changes the function associated with a pin in the PIN LIST, the fusing required is automatically done. Using the bidirectional pins of the 82S153 as an example:

PIN LIST:

PIN	FUNCT	LABEL
9	B	(MNEUMONIC)

INTERMEDIATE TERMS: (MNEUMONIC)

The user now has the option of making the function either an input, I, an output, O or /O, or leaving it a bidirectional port, B or /B. The change to an I would cause all of the of the fuses in the DO term to be left intact. A change to an O or /O would cause all fuses in the DO term to be blown. Leaving the function as a B or /B would create the requirement that the programmer prompts the user in the EQUATION BLOCK for an equation for the DO term. This prompting will eliminate the possible error mode of not properly programming the direction control term for the various conditions.

The INTERMEDIATE TERM shown in the example would be where the name for a common logic block is specified. The equation for the common term would be entered with a prompt in the EQUATION BLOCK and could then be used in any other equation. This will reduce the time required for entry of equations.

EQUATION BLOCK: This is totally different from the previous format. For the FPLS, this format allows entry in either equation or state machine modes. The level of computer prompts is also shown at a more interactive level.

EQUATION BLOCK:

EQUATION, EQ, OR STATE MACHINE ENTRY, SM, MODE ? SM

TRANSITION 0:
IF PS=: (EXPRESSION)
& INPUT=: (EXPRESSION)
THEN NS=: (EXPRESSION)
& OUTPUT=: (EXPRESSION)

TRANSITION 1:

This input structure would then continue for all transitions until a NULL line is entered to terminate the entry mode.

The structure for the FPLA device would be:

COMMON (MNEUMONIC)=: (EXPRESSION)

OUTPUT B9=: (EXPRESSION)

TERM B8=: (EXPRESSION)
CONTROL D8=: (EXPRESSION)

A null entry in response to an equation prompt would result in that ouput being left unprogrammed with all fuses intact. The entry would continue through all outputs or until the user exits via a control entry. Each output expression could contain input variables and/or intermediate variables as presented in the PIN LIST and defined in the EQUATION BLOCK.

RDP 5/11/82

To: Steve Witten.

From: Russ de Pina

Subject: Signetics' Proposal for Boolean Entry Format.

From my conversation with Bill Smith and after reading the proposal you gave me, here are my inputs:

1) The interactive method of data entry proposed is by far the most user friendly method of entry since the user can be walked through the entire sequence for Boolean equation entry. However, the editor for the PLDS does not support this interactive method of processing since the editor and the PALASM and HEL processors are separate programs. which work on a text butter in RAM.

2) The idea of separate modes for state machine equations and for standard boolean equations is very attractive. Since, first talking about this with Bill Smith in April, I have worked on trying to implement this in the ABEL software.

3) The ABEL compiler could be redesigned in certain places to support this definition. The current definition of ABEL supports a large part of this proposal. This proposal has tremendous impact on our current programmable logic development software since it does not support any facet of the proposal. We must recognize that this syntax is extremely friendly to IFL devices (obviously). Even though PAL devices could be considered as a subset of the IFL devices, (based on internal complexity and function,) there are special considerations that must be made for PALs and these have been investigated, however, I am still in the process of working on fixes for these differences between IFL and PAL. I would like to get more involved with Bill Smith and the other semiconductor manufacturers for their inputs.

OBJECTIVES:

1. To enable a designer to enter into an IFL design from whatever level is comfortable.

2. To provide a "user friendly environment" in which a designer can achieve maximum efficiency with minimum relearning.

STRATEGY:

Establish upwardly compatible programs that are funded by Signetics (if necessary) and supplied by a third party (if possible). Release the programs in a highly transportable format to allow the user to enter the program on "any" machine in his company. These programs could be developed in parallel with modular programming.

IFL DEVELOPMENT SYSTEM NEEDS

LOWER LEVEL

BOOKKEEPING (HAND HOLDING) - PROGRAMMER ENTRY FROM BOOLEAN EQUATIONS OR STATE MACHINES. THIS COULD BE RESIDENT IN THE PROGRAMMER BUT SHOULD BE DESIGNED INTO A μ COMPUTER WITH INTERFACE TO A PROGRAMMER. THE MOST USEABLE INTERFACE WOULD BE ON THE TRUTH-TABLE LEVEL WITH H'S AND L'S. THE PROGRAMMER COULD BE TOTALLY OR PARTIALLY "DUMB".

Mid Level

Logic Simulation

Similar in function and structure to TEGAS and PHILSYM. It will accept inputs from input listings or from the graphics entry package. Will output test patterns for combinational circuits and will grade submitted patterns for sequencers.

Graphics Entry

Macros will be selected and placed on the terminal for a "board mock-up". Connections on the screen and new macros may be defined at the terminal.

Higher Level

Logic Minimization

Will perform parallel miminization with large (depending on machine) number of inputs and outputs. It will be able to minimize combinational equations and sequential logic in equation or state machine format.