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PAL10L8                                                    PAL DESIGN SPECIFICATION
MIL                                                          BIRKNER/COLI 07/21/81
MEMORY INTERFACE LOGIC FOR 6800 MICROPROCESSOR BUS
MMI SUNNYVALE, CALIFORNIA
A10 A12 A13 A14 A15 PHASE2 VPHASE2 RW 9 GND
11 CSOD1 CSOD0 NC NC /CE1 /CE0 WEOE1 WEOE0 VCC


/WEOE0 = /A10*/A12*/A13* A14*/A15* PHASE2* VPHASE2*/RW ;DEC WRITE ENABLE CHIP 0

/WEOE1 =  A10*/A12*/A13* A14* A15* PHASE2* VPHASE2*/RW ;DEC WRITE ENABLE CHIP 1

/CSOD0 = /A10*/A12*/A13*/A14*/A15* PHASE2          ;DECODE OUTPUT DISABLE CHIP 0

/CSOD1 =  A10*/A12*/A13* A14*/A15* PHASE2          ;DECODE OUTPUT DISABLE CHIP 1

   CE0 = 9   ;ENABLE CHIP 0 (COMPLEMENT OF CSOD0)

   CE1 = 11  ;ENABLE CHIP 1 (COMPLEMENT OF CSOD1)


FUNCTION TABLE

A10 A12 A13 A14 A15 PHASE2 VPHASE2 RW 9 11 WEOE0 WEOE1 /CE0 /CE1 CSOD0 CSOD1

;ADD BUS
; 11111   PHASE R PINS  WRITE-ENABLE  CHIP-ENABLE  OUTPUT-DISABLE
; 02345   2  V2 W 9 11     0    1        0   1        0      1     COMMENTS
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  LLLHL   H  H  L H H      L    H        L   L        H      H     WRITE EN 0
  HLLHH   H  H  L H H      H    L        L   L        H      H     WRITE EN 1
  LLLLL   H  X  X L H      H    H        H   L        L      H     OUTPUT EN 0
  HLLHL   H  X  X H L      H    H        L   H        H      L     OUTPUT EN 1
  LLLHL   H  H  H H H      H    H        L   L        H      H     RW=H
  HLLHH   H  H  H H H      H    H        L   L        H      H     RW=H
  XXXXX   L  X  X H H      H    H        L   L        H      H     PHASE2=L
  LLLHL   H  L  L H H      H    H        L   L        H      H     VPHASE2=L
  HLLHH   H  L  L H H      H    H        L   L        H      H     VPHASE2=L
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DESCRIPTION

THIS DEVICE PROVIDES THE INTERFACE LOGIC BETWEEN A 6800 MICROPRESSOR BUS
AND FOUR STATIC 4k MEMORY CHIPS.  ADDRESS BUS (A), READ/WRITE (RW), PHASE 2
CLOCK (PHASE2), AND VALID MEMORY ADDRESS (VPHASE2) ARE DECODED TO PRODUCE
THE PROPER WRITE ENABLE (WEOE), CHIP ENABLE (CE), AND OUTPUT DISABLE (CSOD)
SIGNALS FOR MEMORY DATA TRANSFERS.

NOTE THAT /CE0 AND /CE1 ARE THE COMPLEMENTS OF CSOD0 AND CSOD1, RESPECTIVELY.
THESE FUNCTIONS ARE IMPLEMENTED BY THE EXTERNAL CONNECTIONS CSOD0 TO PIN 9 AND
CSOD1 TO PIN 11.
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