ABEL 1.1 Will support over 95 devices, handle FPLS state diagrams, and have new reduce method. Will take a lot of engineering hours to meet the Oct 15 target release date.

ABEL 1.2 Will add support for MMI 20RA10 asynchronous PAL, new devices from VTI, Altera, EXEL, and others. May have new features to counter CUPL 2.0 (expected in Oct 84). Target release date March 85.

PROMlink with logic support. Will require 1 or 2 man-months. Requires major editing of users manual. Target release date of Dec 84.

Fault Grading and Automatic Test Vector Generation. A separate ABEL product for release in Q1 1985. Requires Fault Grading modification to ABEL simulator. First version may only generate test vectors for PALs. PAL version is a defined task with talent in house.

Interactive Logic Device Debugger. An separate ABEL product. Present ABEL simulator is a batch process requiring a complete rerun of ABEL after changing test vectors. There have been request from the field and in-house to add interaction to the simulator. First version would be IBM PC based. User could run a simulation, halt on an error, edit test vectors, and single step forward or backwards to determine the cause of the error. The results could be displayed as chip diagram, in symbolic values, or as a waveform. The same program could work with the LogicPak or the Model 60 allowing interactive debugging of the actual programmed device. Depending on features, first version could be done with 2 to 6 man-months. Would require an detailed manual. The is a defined task with the talent in house.

Logic Analyzer Driver A PC software interface between a simulator such as ABEL or HILO2 and a logic analyzer such as Northwest Instruments.

PC based Logic Development System Would include ABEL, Model 29B, LogicPAK, RS-232 cable, Term, and logic version PROMlink. Future versions would include Interactive Debugger and Automatic Test Vectors.

PC based Software Development System Would include Model 29B, UniPak, cable, PROMlink and other utilities. A IBM ".EXE" format to Intel Hex utility has been requested from the field. This would allow standard IBM PC languages (Macro Assembler, PASCAL and C) to be used for 8086 embedded systems. To reduce field support, suggest cross development tool, but require customers to purchase separately.

Dash-1 Schematic Entry for ABEL Would convert a schematic of basic gate and certain logic functions into Boolean equations. This would be for new design and manual conversion of existing designs. Would have manual device selection and partitioning. Would not provide general design translation of 74LSxx circuits to programmable logic devices. May require help from FutureNet's engineering staff for extracting desired devices from database and may require modifications to DASH-1. The target date of Jan 15, 1985 will determine the capabilities included in first version. This will require a detailed manual, an ABEL quality manual will require 8 to 10 weeks.

Board Level Functional Simulation The HILO2 simulator allows the engineer to define a logic element with a Boolean language. With a conversion utility these Boolean equations could be used as a input to ABEL. Another method to tie into HILO2 would be a ABEL reduced equation to HILO2 conversion. The main purpose is functional simulation, not timing analysis. These would not require any modification to HILO2. This method would not require a HILO2 source license and would not require a large support effort of each device type. CADAT may work for this application. This task is basically understood but full definition requires access to the target simulator.

Logic Device Simulation Models Would provide a library of complete logic device models for one or more simulators. This would allow full timing analysis of logic devices in circuit. The simulator would use the JEDEC load file to configure the logic device. Many simulators have models for the 4 popular PALs (16L8, 16R4, 16R6, and 16R8). The number of devices and the performance variations make this a large task. The ABEL library is up to 100 devices with no distinction of performance. There are probably 20 versions of the PAL16L8 alone, ABEL considers all PAL16L8s the same. This product would require an extensive support effort to keep up with new devices.

ABEL as a custom PLA design tool This would allow users to define their own ABEL logic devices, and then use ABEL to design the PLA portion of their custom IC. We have had request for this and is was in the original ABEL specification. We have a in-house "lint" program that checks the device files for errors and internal documentation for device file specifications. We may test this concept with FLUKE. This would take very little effort to release this product.

State Machine Analysis and Simulation ABEL supports state diagram entry and simulates the reduced equations, however the logic reduction often takes a long time. This tool would allow interactive state diagram design. It would provide optimum state assignment, detect ambiguous state transitions, and ensure unused states return to a defined path. The design would be entered with a mixture of text and graphics. The graphics could show the main flow with the details entered a textual "footnotes". The simulator would allow the trace the flow on the diagram. The user could define 2 or more state machines and determine their interactions. This program is a computational based program with graphics used to enhance the user interface. It is quite feasible with normal terminal graphics. The main benefit will be interaction, a spreadsheet for state machines.

Logic Device Selection Aids In the general case, automatic device selection is not possible and it may not be desirable for Data I/O to recommend Signetics devices over MMIs. The wide range of programmable logic device architecture prevents the engineer from expressing a detailed design with first specifying a particular architecture. The designer have a reasonable knowledge of the logic device before he starts the design process. This problem could be minimized by a printed summary of all devices available. The present ABEL package includes logic diagrams for all devices but a cross reference chart could be added. Today ABEL will tell if a design fits into the select device and reports the number of product terms used, this information could be expanded. Many of the criteria for device selection have nothing to do with the function description required for ABEL or other design languages. The device speed, power consumption, second sourcing, and other important features could be listed on a printed chart or stored in a database. The most useful device selection aid may be a simple printed cross reference chart and a set of architecture or logic diagrams.

Logic Tools Group Projects for 1984

Michael Holley
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PROMlink
- First Release
- Logic support
- Set programming
- Screen Editor
- Termnial Emulator

H&L Design Adapter
- Software Release

ABEL Version 1.00
- MS-DOS 1.04
- UNIX 4.2
- APOLLO
- CP/M 86 (Japan)

ABEL ports Version 1.10
- MS-DOS
- VAX/VMS
- VAX/UNIX
- APOLLO
- CP/M 86 (Japan)
- 3B2/UNIX (in-house use)
- CP/M 68K (in-house use)
- MAC (in-house use)

ABEL 1.xx enhancments
- Fault Grading (PALs)
- EXEL devices
- MMI 20RA10
- IFL fusemap display
- TERM

Programmable Logic Development Enviroment (VAX, PC, 3B2)
- State Machine Analysis and Simulation (text and graphics)
- Automatic Vector Generation (PALs)
- Board Level Simulation (HILO2)
- Device Selection Database

Interactive Logic Debugger
- Simulation
- Device Testing on PLDS and DLP
- Logic Analyzer