Interoffice Correspondence

- ☐ For Your Comments
- ☐ For Your Approval
- ☐ Please Take Action
- ☐ Call Me
- ☐ See Me
- ☐ Per Our Conversation
- ☐ Read, Initial & Return
- ☑ For Your Information
- ☐ Note & Return
- ☐ Note & File
- ☐ For Your Signature
- ☐ Please Advise Status
- ☐ Per Your Request
- ☐ Please Advise Appropriate Employees In Your Department

To: ABEL™ Team Members Mike

Date: March 8, 1983

CC:

From: Mike Mraz

Subject: ABEL™ PRODUCT DESCRIPTION

Dear Team,

Some of the information in this document is company private, hence the stamp on the cover page. Please treat the document as confidential.

So that I can assure all team members receive the latest revisions to this document, I am keeping a log of its recipients. Please do not make copies of this document, therefore, but see me if you require copies.

Thanks,

Mike

PRODUCT DESCRIPTION

ADVANCED BOOLEAN EXPRESSION LANGUAGE (ABEL™)

COMPANY
CONFIDENTIAL

Michael A. Mraz

February 13, 1983

(v.B)

1. PURPOSE

This document describes the ABEL™ series of software products, and includes preliminary market data and associated information.

2. BACKGROUND

The ABEL™ series of software products are computer-aided design (CAD) tools for logic designers. ABEL™ products will be designed to execute on standard small computers and personal computers which use any one of several standard operating systems. See section 4 for a listing of the operating systems under which ABEL™ products will run.

Computer-aided design (CAD) tools have been in existence for nearly as long as computers themselves. CAD software may be defined as any program or set of programs which assist or automate one or more design functions traditionally done manually (without machine aid). According to the 1983 Electronics world markets survey, the U.S. market for CAD software will increase from $450.9million (1982) to $744.6million (1983) to $1,801million (1986).

The increasing popularity of programmable logic devices has prompted the development of several "standard" CAD tools, most notably PALASM by Monolithic Memories, Inc. Although crude, CAD programs such as PALASM have gained acceptance due largely to a lack of anything more elegant.

In parallel with the development of programmable logic devices and associated CAD programs, the explosion in popularity of semi-custom logic arrays (also known as semi-custom gate arrays) has resulted in the development of many large and complex CAD programs in support of these silicon products.

A semi-custom gate array is basically a standard set of logic gates placed on a silicon chip without the final layers of metallization which connect the individual gates to form a logic system. The number of gates on a semi-custom gate array may range into the thousands. All popular logic families are currently being implemented in semi-custom arrays, including Schottky TTL, CMOS and ECL.

A semi-custom gate array is used in a design for one of two basic reasons: (1) production quantities are high enough, usually in the hundreds of thousands, to warrant the extremely large design cost, since this cost is amortized over many units, or (2) the design requires such high performance (especially ECL designs) that conventional circuit board techniques are totally unacceptable because of signal propogation delay.

An example of (1) is a the Apple III personal computer, which uses a semi-custom array based upon the 6502 microprocessor. An example of (2) is the IBM 3033 mainframe computer, which relies heavily on ECL semi-custom arrays to obtain the necessary performance.

Now, CAD is used heavily in the design and production of semi-custom logic arrays simply because the traditional breadboard approaches of logic design using discrete components* are not applicable to designing an entire system on a single piece of silicon. The CAD tools are used to:

(1) specify the design, usually in some high-level format,

(2) simulate the design to eliminate potential errors,

(3) generate routing information from which the final metallization layers for the IC are produced,

(4) generate complete test data which will be used to test the devices as they are produced.

Of course, this is a highly simplistic summary of gate array design, but it does illustrate the use of CAD in one application. The gate array application is very similar to the programmable logic application, and CAD tools for both are similar.

* 'discrete components' as used here means discrete ICs, not discrete resistors, capacitors, and transistors.

Contrast the gate array CAD application with the typical PALASM application. PALASM is used to:

(1) specify a design, using Boolean equations,

(2) simulate the design using a table of data entered by the designer (not a true simulation),

(3) generate a fuse map for the programmable device ("autorouting")

(4) derive functional test data ("test vectors") from the simulation table.

PALASM is a fairly crude CAD tool, as mentioned earlier. Its drawbacks are:

(1) PALASM is very device-specific, hence designs are not easily transferable to other programmable logic devices,

(2) PALASM is not available as a standard product. It is a "give-away" from MMI, and is not supported as a true product.

(3) Unlike a multitude of spreadsheet programs, word processors, and video game programs, PALASM is not available for use with personal computers.

(4) PALASM does not support useful concepts such as macros, and other desirable features.

(5) PALASM does not truly simulate a logic design.

(6) PALASM does not automatically generate test information.

(7) PALASM does not generate sophisticated error messages, hence the designer becomes inefficient when attempting to find a problem.

Clearly, a more useful CAD tool is required by the programmable logic user.

3. ABEL™ DESCRIPTION

ABEL™ is a CAD tool which will be designed to:

(1) Allow entry of a combinational logic designs using the most efficient form of input for these designs, Boolean equations.

(2) Allow entry of sequential, or state machine, logic designs using an efficient syntax developed by Data I/O.

(3) Perform equation minimization to reduce the apparent complexity of the design.

(4) Simulate the logic design in software.

(5) Allow several separate and self-contained designs to be contained in one device.

(6) Segment a large design requiring multiple devices into several different devices.

(7) Support designs using PALs®, FPLAs, FPLSs, and PROMs.

(8) Generate standardized fuse maps and documentation.

(9) Communicate with programmer equipment using the JEDEC ASCII-logic format developed by Data I/O.

For a more complete description of the initial ABEL™ product and following enhancements, refer to Appendix 1.

4. COMPUTERS, OPERATING SYSTEMS, AND LANGUAGES

An operating system is a collection of software used as the interface between a computer and application software. Because one operating system may be written to operate on several different computers while still maintaining compatibility with all application software, selection of operating system which will run a particular application program is more critical than selection of computer hardware.

Transportability is a characteristic of a particular piece of software which determines how easily it is adapted to run under various operating systems and on various collections of computer hardware. It is always desirable to write an application program in a highly transportable language so that it can be easily adapted to run on a multitude of computers and operating systems.

ABEL™ will be written in a highly transportable language, either PASCAL or C. In this way, ABEL™ will be easy to modify ("install") for execution on many different operating systems.

Initially, ABEL™ will be offered for use with DOS (PC-DOS, MS-DOS) operating system by Microsoft. This system is used on the IBM personal computer. ABEL™ will also be initially offered for use under the VMS operating system used by Digital Equipment's VAX computer. As ABEL™ development proceeds, and more data become available concerning operating system installed bases, more operating systems will be added to this list, with target dates for inclusion.

The decision to initially support DOS and VMS was made because of the popularity of the IBM personal computer (PC) for business applications and the popularity of the VAX computer for engineering applications. Data I/O will have immediate access to both an IBM PC and a DEC VAX for development and testing of ABEL™ products.

5. PROGRAMMABLE LOGIC DEVICES

Programmable logic devices include the following:

(1) PAL-type devices from AMD, Harris, MMI, Motorola (future), National, and Texas Instruments (TI).

(2) IFL-type devices from Fairchild, Harris, Signetics, and TI.

(3) PROMs from many sources.

To be marketable products, the ABEL™ series must support most of the popular logic devices, and it must support peculiarities of those devices resulting from manufacture by several different sources. The list in Table 1 is a guide to the devices which the initial ABEL™ product should support. This list will be updated as more data are made available.

TABLE 1 LOGIC DEVICE SUPPORT OF ABEL™ INITIAL RELEASE

PART NUMBER	CLASS	MANUFACTURER(S)
16L8	PAL	AMD, Harris, MMI, National, TI
16R8	"	" " " " "
16R6	"	" " " " "
16R4	"	" " " " "
16H8	PAL	AMD, Harris
16LD8	"	" "
16HD8	"	" "
16P8	PAL	Harris
82S100/1	FPLA	Signetics
82S104/5	FPLS	"
82S158/9 (93458/9)	FPLS	Signetics (Fairchild)
82S152/3	FPLA	Harris, Signetics
74FP333/5	FPLS	TI
74FP839/40	FPLA	"

6. RELEASE SCHEDULE

The initial ABEL™ product is to be released in February, 1984. Release dates for the follow-on products are to be determined (TBD).

7. PRELIMINARY FORECAST AND PRICING

By initial release of ABEL™, the installed base of LogicPaks™ should be approximately 2000-2400 units. Each of these customers is easily accessible and would be a prime customer for ABEL™ and any development system ("workstation") product built around the computer, ABEL™, and programmer/LogicPak™.

ABEL™ products will communicate with programmers in the JEDEC logic format, hence they will also be compatible with other programmers supporting this format. Each copy of ABEL™ sold to a customer with a non-Data I/O programmer will generate a highly qualified lead for a high-end programmer sale.

New LogicPak™/ABEL™ customers will be generated at an accelerating rate through 1984-1985 due to the fact that programmable logic is just starting to be designed into digital systems. As more semiconductor manufacturers jump on the programmable logic bandwagon, its popularity increases even faster. Data I/O can benefit by this snowball effect by providing fast support for new logic devices, thus protecting LogicPak™/ABEL™ market share.

A gross estimate of new customers for programmable logic products in the first year of ABEL™ availability (Feb. '84 to Feb. '85) would be 2500. Using this estimate, the projected installed base, and applicable correction factors:

LogicPak™ installed base	(2000)	X 25%	= 500	units
New customers	(2500)	X 50%	= 1250	units
Misc. sales (other programmers, etc.)	(100)		= 100	units

TOTAL ABEL™ SALES, FIRST YEAR = 1850 units, approximately.

Assuming a target price of $500 per unit, $925,000 would be generated by ABEL™ sales alone. This does not take into account the hardware sales generated through ABEL™ leads, systems or OEM sales, or any other source of revenue. All figures are extremely preliminary, but should be fairly representative of the opportunity.

8. PRELIMINARY FINANCIAL ANALYSIS

The financial analysis of the ABEL™ products is TBD.

9. COMPETITIVE OVERVIEW

CAD is a lucrative market, especially in fast-growing niches such as the ABEL™ product occupies. As programmable logic gains in popularity, many competitors should be expected to enter the game. At present, the only possible competitor to the ABEL™ series is Assisted Technology, a small startup in Silicon Valley. Data I/O has approached Assisted with the idea of a joint venture of some sort. Should this happen, Assisted's product, called CUPL, could be used as a gap-filler until the release of ABEL™.

CAD tools such as PALASM and other device-specific packages will still find some popularity. However, the overwhelming advantages of a general non-device specific tool such as ABEL™ should far outweigh any advantages of the PALASM-type products, with the exception of initial cost (PALASM is free).

A more complete assessment of ABEL™'s competitive situation will be made as more data become available.

APPENDIX 1

ABEL™ PROJECT SPECIFICATION

Note: all information is preliminary.