NORTHWEST COMPUTER NEWS

3-3 NORTHWEST COMPUTER SOCIETY
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MEETINGS

The Northwest Computer Society meets at the Pacific Science Center, in Seattle, on the first and third Thursday of each month at 7:30 PM. The first meeting of the month normally is held in room 200, on the East side of the Science Center Court. This meeting usually features a formal presentation by a speaker or speakers. The second meeting of the month is normally held in the math room, at the Southeast corner of the Science Center Court, two flights down. This meeting is usually more informal with freewheeling discussion and problem solving.

Thursday, May 4 - Room 200
"Video Brain, the Home Control Computer" by Max Cook, Computerland of South King County

Thursday, May 18 - Math Room
Informal meeting with no speaker scheduled.

Thursday, June 1 - Room 200
"Operating Systems" by Roger Atlas of Boeing Computer Services

FAIR

Over 5,000 people attended the Personal Computer Fair held the weekend of April 8-9 at the Science Center. The Fair was a cooperative effort of the Northwest Computer Society and the Pacific Science Center, with the Fair exhibits an extension of the Science Center's regular exhibition. There were 13 commercial exhibitors, five of them local computer stores, and two colleges. Several members of the Society brought in and exhibited their own computer systems. The Society's timesharing arrangement with Nordata was demonstrated, with four terminals in simultaneous use.

Sixty-one computers or terminals were up and running simultaneously in the Eames Theater and the adjacent balcony during the Fair, according to Bob Wallace. This number must be some kind of a record, particularly as almost all of the 61 were there to be touched and used by the visitors.

The crowds were greatest on Saturday, with the Fair area filled to capacity most of the day. Sunday saw the area well-filled, but the crowds came later and generally were not as numerous. While this event was aimed at the general public, rather than at those who are technically oriented, exhibitors and Society volunteers noted a high level of interest and understanding on the part of many of the visitors. There was also considerable evidence that computing "comes naturally" to young people. It is no surprise, today, to see high schoolers who are already familiar with BASIC or another computer language. Quite a few young ones of elementary school age, however, were using the keyboards successfully, while Daddy or Mommy held back, afraid to try!

Additional pictures of the Fair will be found on Page 3.

RCA-INTEL EXCHANGE TECHNOLOGY

RCA Corporation and Intel Corporation have signed an agreement whereby RCA will design high-density SOS (silicon-on-sapphire) versions of the Intel 8085 and 8048 microprocessors. Conversely, Intel will receive information which will allow it to manufacture CMOS SOS versions of these components.

Under the terms of the non-exclusive agreement, which was signed March 19, Intel will provide information to assist RCA in designing CMOS SOS versions of Intel's NMOS 8085A microprocessor, 8155 RAM I/O, 8355 ROM I/O and 8048 single-chip microprocessor.

In making the announcement, Carl R. Turner, RCA's Division Vice President, Integrated Circuits, said, "RCA sees a double benefit to this agreement, namely, the opportunity for strengthening the industry acceptance and use of CMOS silicon-on-sapphire as a viable IC technology and the enhancement of RCA's position as a supplier of low-power microprocessors." He stressed that the agreement offers RCA the opportunity to supplement its existing CDP1800 CMOS microprocessor family. "We are fully committed to the CMOS SOS versions of the Intel family of microcomputer devices in addition to the continuation of our CDP1802 microprocessor program and of our plans to introduce the CDP1804 CMOS SOS single-chip microcomputer later this year," Mr. Turner stated.

Leslie L. Vadasz, Vice President and General Manager of Intel's Microcomputer Components Division, said, "the realization of Intel's 8085 and 8048 microcomputers incorporating RCA's CMOS SOS technology will allow many customers to whom power considerations are paramount to use these industry standard product families."

—RCA News Release dated 3 April 78

Northwest Computer Society
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Seattle, Wa 98104

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DATA GENERAL microNOVA TO BE STOCKED LOCALLY

by John P. Aurelius

The microNOVA microprocessor is a NOVA CPU in a single 40-pin ceramic package. With its supporting chips, it becomes a complete 16 bit microcomputer, compatible with the NOVA minicomputer line and using the NOVA-3 instruction set. It is available as a chip, as a chip set, as a one-board computer, and in complete, packaged systems. The microNOVA line is stocked by the Wyle Distribution Group, of which Liberty Electronics of Bellevue, Washington, is a member. Liberty can supply these products from its stock or within days from one of the other stores.

The line is, of course, a downward extension of Data General's line of NOVA minicomputers. The design philosophy follows traditional minicomputer principles. For example, there is a heavy emphasis on analog to digital and digital to analog interfaces for the instrumentation and process control applications. There are obvious advantages for those already using NOVA minicomputers and familiar with Data General software. It can be configured into a business system, with CRT and hard copy terminals, floppy disks, and a recently announced 10 megabyte hard disk. Business and scientific versions of BASIC are offered, and FORTRAN is available.

The following general description of the mN601 CPU chip is quoted from the data sheet:

> The microNOVA mN601 microprocessor is a full 16-bit high performance NMOS microprocessor that provides the central processing function for Data General's microNOVA family. The mN601 features NOVA 16-bit architecture including hardware multiply/divide; multiple addressing modes including absolute, relative, index, deferred, and auto increment/decrement; multiple accumulators, including two that can be used as index registers; hardware stack and frame pointers with stack overflow protection; programmed priority interrupt to 16 levels; and separate memory and I/O buses.

With a clock running at 4.166 MHz, some typical instruction execution times (in microseconds) are:

Load or store accumulator	2.88
Add or subtract	2.4
Increment skip if zero	3.84
Jump to subroutine	3.36
Multiply	41.28
Divide	59.04
I/O Input instructions	7.2
I/O Output instructions	4.8

Memory is dynamic, and the microNOVA system is set up to provide refresh from the CPU (or a Direct Memory Access controller, if used). There are 15 bits in a memory address, so only 32k words (but that's 64k bytes) can be addressed. There are 16 levels of interrupt, and a real time clock is inherent (but an external real time clock is needed if direct memory access is used). Direct memory access transfers data to and from memory without using the CPU, at very high speed. A separate DMA controller is required, which disables the CPU when it is active.

Extensive software is available, including real time and disk operating systems, a FORTRAN IV compiler which generates assembly language code that can be optimized by the programmer if desired, DOS BASIC and Business BASIC, Text Editor, Assembler, Symbolic Debugger, Communications Access Manager, Sensor Access Manager, HASP II Workstation Emulator, and RJE80 which lets microNOVA computers do remote job entry tasks and communication with other Data General computers and 2780/3780 IBM compatible systems.

The reader may have guessed by now that the microNOVA is not a direct competitor to the PET or TRS-80! The board computer with 4k RAM is $950, and the 9-slot microNOVA MOS Minicomputer with 4k RAM sells for $1995. A packaged development system, with the 9-slot computer, 16k RAM, dual diskette, asynchronous interface, console debug, half bay cabinet, DOS software and utilities and a 60 CPS KSR hard copy terminal costs $11,270. Note that memory capacity is in 2 byte words. FORTRAN is $500, and BASIC is $1,000. Business application software is not available from Data General, but there is a User's Group library.

NORTHWEST COMPUTER SOCIETY PHONE
284-6109

This phone number is a new service to our members and others interested in the Northwest Computer Society. There is an answering machine on the line, so it operates 24 hours a day. Callers receive a short message about the Society, telling when and where we meet, etc. The machine also records callers' messages of any length. The message service is a good way to reach club officers. The messages are checked frequently by remote control, by Roy Gillette, Treasurer, and by Joe Pizzorno, Program Chairman, and they will forward the information to the appropriate persons. So try it!

OFFICERS

President	John Marshall
Newsletter Editor	John Aurelius
Treasurer	Roy Gillette
Program Chairman	Joe Pizzorno
Secretary	John Aurelius
Board Members	Randyl Britten
	Jay Wicklund
	David Smith

S-100 BOARDS - 8K and 16K static memory, Prototyping, Front Panel Replacement. Also keyboards, software, etc. Catalog from Sargent's Dist. Co., 4209 Knoxville Ave., Lakewood, CA 90713 (213) 421-9521.

FREE TV - 19" B & W, tuner and sound bad, raster and picture OK. Mike Voris, Seattle WA, 284-1492.

FOR SALE - KIM-I microcomputer, almost new, with warranty - $165. Dan Weller, Silverdale WA, 692-6463.

SOFTWARE - can be bought or sold through the catalog of this firm. Authors can list a program for $10 per year (12 issues); a commission is charged on sales. Catalogs are in six categories @$1.50 each. National Software Exchange, Inc., 1000 Lake St. Louis Blvd. 248, Lake Saint Louis, MO 63367.

RECYCLED COMPUTER EQUIPT - a catalog of terminals, monitors, modems, keyboards, etc. is available from Pacific Office Systems, Inc., 2600 El Camino Real 502, Palo Alto, CA 94306.

FOR SALE - Processor Tech GPM board with CUTER monitor in ROM; Processor Tech CUTS cassette tape interface board; Tu-Art serial / parallel board; Tarbell disk controller with software. All assembled. David Tibbot, Issaquah WA, 392-6697.

FOR SALE - Tally 100 line per minute printer $550; one half of a Wunderbuss (ground plane both sides between lines) with 10 connectors and active terminating components $60; Intel factory prime 2708s $9. Joe Pizzorno, Seattle WA, 284-1566 home, 284-6040 work.

THIS MESSAGE WAS WRITTEN THROUGH A $35 MODEM. THE PLANS ARE IN NOV 77 KILOBAUD. THIS CIRCUIT REQUIRES NO TEST EQUIPMENT TO GET IT WORKING. I USED A MC 6860 IN PLACE OF THE MC 14412 SO I CAN INTERFACE IT TO MY COMPUTER FOR AUTO ANSWER. THE FILTER CAN BE BUILT WITH 5% RESISTORS AND STILL WORK FINE.

MICHAEL HOLLEY 487-2819/488-7513

HEURISTICS 'SPEECHLAB' SET - $195 COMPLETE. HAS BEEN USED A FEW TIMES AND WORKS FINE. THIS IS A $299 VALUE. INCLUDES FULL DOCUMENTATION, PLUS EXTRA PROGRAMS TO GET YOU STARTED IN VOICE INPUT EXPERIMENTS. CALL ROY GILLETTE EVENINGS (524-0596)

BASIC CLASS - Beginner level. Minimum of 6 people to schedule the class. If interested call Dick Curtiss, Seattle WA, 784-8018.

TDL AND SEALS products are offered at discount prices. SASE for catalog from Barnes Electronics, P.O. Box 673, Oak Ridge, TN 37830.

IC'S, SOCKETS, PARTS - free catalog from G. F. Components, P.O. Box 225, Santa Barbara, CA 93102 (805) 963-2933.

WANTED - Spare Solenoid type bar for T-132 line printer. Greg White, Port Angeles WA, 457-3315 days, 457-3917 eves.

HELP WANTED - Part time or after hours programming for SWTP 6800 system or Honeywell 316 or Microdata Reality (BASIC). R.V. Thomas, Renton WA, 235-4602 days, 767-5370 eves.

FOR RENT - Apple II computer, $18 for 2 days. Longer time periods at lower daily rates. Also available is a modem so the Apple can be used as a terminal. Dick Curtiss, Seattle WA, 784-8018.

COMPUTER STORES

Almac/Stroum Electronics
5811 - 6th Ave. S
Seattle, WA 98108
763-2300

Altair Computer Center
14100 NE 20th St.
Bellevue, WA 98007
641-8800

Byte Shop
14701 NE 20th St.
Bellevue, WA 98007
746-0651

Computerland
14340 NE 20th St.
Bellevue, WA 98007
746-2070

Computerland
1500 S 336th St.
Federal Way, WA 98003
838-9363 Tacoma 927-8585

Computerland
8791 S. Tacoma St.
Tacoma, WA 98499
581-0388

Empire Electronics
616 SW 152nd St.
Seattle, WA 98166
244-5200

Heathkit Electronic Ctr
505 - 8th Ave. N
Seattle, WA 98109
681-2172

Micro Computer Center
11822 NE 8th St.
Bellevue, WA 98005
455-3710

Omega Northwest, Inc.
839 - 106th Ave. NE
Bellevue, WA 98004
455-2126

Radio Shack - many stores in Seattle area

Retail Computer Store
410 NE 72nd St.
Seattle, WA 98115
524-4101

Seawell Marketing, Inc.
315 NW 85th St.
Seattle, WA 98117
782-9480

The Sixteen Bit Chauvinist

by C. R. Britten

TECHNICO ENTERS FIELD WHERE GODBOUT FEARS TO TREAD

The prospect of a low cost personal computer with a sixteen bit word size is fascinating to me and I suspect there are many who share this feeling. I waited patiently for the Morrow and Godbout PACE computer and visited George Morrow twice to see his prototype and check on its progress. But the Morrow/Godbout partnership effort encountered some difficulties with suppliers and, for various reasons, they were unable to bring their product to the marketplace.

When it became clear that George's PACE computer would not be available I chose the Technico Super Starter because it provides the best bang for the buck available in sixteen bit systems. The Super Starter System with the Texas Instruments TMS-9900 chip is the result of a joint development between Technico Incorporated and Rosse Corporation. Rosse designed the board and wrote the software and Technico handles the manufacturing, marketing and distribution. The Rosse consulting organization has a good background in microcomputer design and implementation including both eight and sixteen bit microprocessor types. Technico is a Maryland based electronics distributor handling Texas Instruments products as well as other standard lines of equipment. Technico has a toll free WATS line that you can use to order equipment, ask questions, or get help with a problem. It is a nice trend to see companies adopting this service.

Technico Incorporated
9130 Red Branch Road
Columbia, MD 21045
Phone: (800) 638-2893

Rosse Corporation
9218 Brian Drive
Vienna, VA 22180
Phone: (703) 369-2734

EVALUATION

The Super Starter Kit is built around the Texas Instruments TMS-9900 CPU chip with the sixteen bit minicomputer architecture and instruction set. The basic kit for $299.00 includes 512 bytes of RAM using TMS-4042s with room on the board to expand to 2k bytes. Technico's RAM expansion package consists of twelve additional TMS-4042 chips for $49.00.

The Mighty Monitor is contained in 1k bytes in a pair of 74S472 fuse link ROMs. Table 1 summarizes the monitor commands. Beside the monitor ROMS there is room on the board for an additional pair of 74S472s and Technico offers an Instant Input Assembler for $49.00 to fill this space. I chose this option as a worthwhile addition to my system. Table 2 outlines the features of this interactive assembler. You must maintain your own symbol table by hand with this type of assembler and calculate displacements with the monitor's hexadecimal arithmetic command.

A special feature of Technico's single board computer is its 2708 EPROM programmer. The 2708s are programmed in pairs with the left byte of a pair in one and the right byte in the other, for a total of 2k bytes in EPROM. Notice the monitor command provided for EPROM programming. There is also an ENABLE / DISABLE switch provided on the board to control the 28v programming power source. If you plan to do much 2708 programming you might want to consider installing zero insertion force sockets in place of the ones provided.

A memory map is given in Figure 1 showing the locations of the various memory parts in address space. A map of this kind can be handy to locate a bad memory part if a stuck bit develops. The board is provided with a system of jumpers that can be changed to move RAM and ROM to different areas of address space for special applications.

The Super Starter is a large board measuring 7 by 16 inches. It is well designed and nicely laid out with all of the ICs oriented the same way, with pin one to the upper left. That makes it much easier to see at a glance that all of the ICs are in the right way -- a nice touch that I appreciate. Texas Instruments ICs are used throughout.

Unfortunately TI marks their plastic DIPs in a way that is especially confusing for novices. They put a round notch in the wrong end of their plastic packages and everybody else puts a similar round notch in the end with pin one. TI plastic parts have a rectangular

FIGURE 1

Technico Super Starter Memory Map

HEX ADDRESS	BIT POSITION 0 . . . 4 . . . 8 . . . 12 . . .				
0000	U19	U34	U15	U30	TMS-4042-2 or NEC 2111-4 Static RAM
0200	U20	U35	U16	U31	
0400	U21	U36	U17	U32	
0600	U22	U37	U18	U33	
07FF					
F000	U50	U51			2708 EPROM
F7FF					
F800	U49	U47			74S472 ROM Instant Input Assembler
FC00	U48	U46			74S472 ROM Mighty Monitor
FFFF					

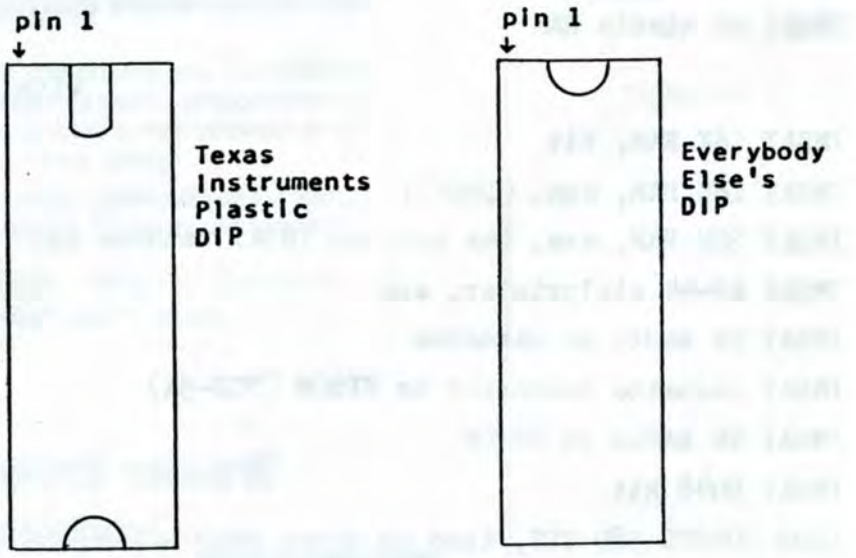

FIGURE 2

Texas Instruments Plastic DIP Orientation

notch in the end with pin one, so if you get in the habit of orienting on a round notch, look out. See what I mean in Figure 2.

THE DIP16 BUS

The board includes plenty of 74LS367 buffers with address and data buffers provided for the on-board memory, and additional buffers for the off-board memory expansion. Technico offers a 32k byte dynamic memory board for $699.00 in fully populated kit form. Partially populated boards can be obtained and a factory assembled version is available for an additional $100.00.

There are no edge connectors on these boards. All communication between boards and to the outside world is by way of 16 pin DIP sockets and ribbon cable jumpers. This is a good idea for inexpensive construction. Technico has all of the cables to jumper their boards together, but experimenters can easily make their own cables with 16 line ribbon cable and Ansley (or equivalent) DIP plugs.

The disadvantage of this idea is that you must be extra careful to orient plugs to sockets correctly, since it is possible to plug them in the wrong way. In the case of the power plug this can be a disaster. You should mark your plugs and cables clearly for proper orientation.

NIT PICKING

The board is silk screened for parts identification on the component side, however the markings are located in such a way that the parts cover the markings when they are installed. This is especially annoying where the IC sockets mask the identification of the IC to be installed. The silk screen identifications should be immediately adjacent to the part location, not under it. The board is not solder masked and does not really need it, however many companies are now including this quality touch at no extra cost to users. The Technico boards would also be enhanced by this feature.

A full set of sockets is provided with the kit, but most of them are of a poor quality. These sockets have only one sided electrical contact for each pin and this increases the chance that a bent IC pin will fail to make contact. Another annoying property of this type of socket is its high outside shoulder that prevents use of a glomper clip for convenient hardware troubleshooting. I regret that I installed any of these sockets in my board. I should have replaced them with Texas Instruments low profile sockets, and I recommend that Technico do the same in future production.

The kit instructions apparently were written before full sockets were provided because they say to mount some sockets and then some other parts. No, all sockets should be installed before any of the other parts because this will give a better result and save time. Just place all the sockets in place, cover the board with another piece of flat board and turn the whole thing over. Then solder all the sockets. Any other technique will just waste your time and make it more difficult to seat the sockets to the board.

There is a mistake in the assembly instructions. The instructions specifically say to omit R29, a 10K resistor. However R29 is needed as a pull up resistor for the 74251 CRU input selector. The factory assembled boards include this resistor and you will need it too.

The TMS-4042 static RAMs seem a poor choice because they cost more than twice the current price for the industry standard 2102 type. The 4042s used are 256 by 4 bit RAMs with a 450 nanosecond access time and are functionally equivalent to 2111s. The board would have been more cost effective if it had been designed around the 2102s, but then a full 2k bytes (16 RAM chips) would have to be installed since the 2102s are configured 1024 by 1, and 16 bit words are required.

I expanded the on-board RAM area with Nippon Electric NEC-2111-4s obtained tested and guaranteed from SemCom for $2.75 each. This is considerably less than the Technico price for 4042s, but still about twice the going price for 2102s.

SemCom, Incorporated
325 South Winding Drive
Pontiac, MI 48054
Phone: (313) 682-3869

The use of 74S472 ROMs is a poor choice, especially for experimenters, because you will probably want to modify the ROM based software at some time, and the 74S472s cannot be reprogrammed. The Super Starter makes modification attractive because you can copy the software to RAM with a monitor command, patch the copy with the Instant Input Assembler, and then program the result into a pair of 2708 EPROMs. Then you can change jumpers on the board to run from your new version. In my opinion it would have been even better to use the available board space for four 2708s, as TI has done with their TM990/100M boards, and omit the use of non-reprogrammable 74S472s. Another argument against the 74S472s is that they are high power dissipation plastic parts, and these tend to have a lower reliability than comparable ceramic packages such as 2708s.

I have to admit that many of my suggestions would increase costs, but I believe they would be worth any necessary price increase. Here is a suggestion to reduce costs. Technico's documentation is in a large format three ring binder with double space type that must be expensive to produce. This document could be produced inexpensively by modern printing technology, without loss of any of its quality contents. And besides, I sometimes like to take a book to lunch to study some fine point, and this is impractical with the large format binder. Technico's book contains listings of the monitor and interactive assembler (if you buy the IIA option) as well as a set of games including Blackjack.

CRB

TABLE 1

Mighty Monitor Commands

A aaaa	Alter location aaaa
B aaaa,n	Set Breakpoint at location aaaa, where n is 1, 2 or 3, the number of words in the instruction being replaced by the breakpoint
C ssss,eeee,dddd	Copy memory to memory starting at ssss and ending at eeee, the destination starts at dddd.
D ssss,eeee	Dump memory in hex format starting at ssss and ending at eeee
G aaaa	Go to location aaaa
H aaaa,bbbb	Hex arithmetic gives the sum xxxx and difference yyyy=aaaa-bbbb printed as H+=xxxx H-=yyyy
I bb	Inspect CRU bit number bb
L	Load into memory from paper tape or cassette, using the format produced by the Dump command
M bb,v	Modify CRU bit bb to the value v, where v is either 0 or 1
P ssss,eeee,dddd	Program a pair of 2708 EPROMS from a source starting at ssss and ending at eeee, the destination dddd is normally 0000 for programming
S ffff,iiii,nnnn R r1,r2 M m1,m2	Snapshot of registers r1 to r2 and memory locations m1 to m2, the first exacution of a breakpoint is snapped at ffff, then incremented by iiii, and snapped a total of nnnn times

TABLE 2

Instant Input Assembler

$string	Assemble string of ASCII characters
+number -number	Assemble number in decimal, hex, or binary where number may be: dd..d decimal digits 0..9 >hh..h hex digits 0..F %bb..b binary digits 0 or 1
/hhhh	Set new program counter to hhhh hex
mnem opnd	Assemble a TMS-9900 instruction where mnem is an instruction mnemonic and opnd is any valid operand for the instruction

Operands may be of the form:

Rn	Register n, 0..15
*Rn	Register indirect
*Rn+	Register indirect with auto increment
@d(Rn)	Indexed by Rn with displacement d
dd..d	Decimal constant
>hh..h	Hex constant
%bb..b	Binary constant
's' or 'ss'	Character constant of 1 or 2 ASCII characters

Bob's Bits

or, rumblings by Bob Wallace

Intel 8086

Intel expects to win back the "most sophisticated microprocessor" award from Zilog with the 8086, due out this summer. It will be an entire quantum leap above anything available now (including the 9900 and the LSI-11), and bring micro power into the high-end minicomputer range. Zilog will counter with the Z-8000 (about which I know little), and Motorola with the 6809, but the 8086 will be a hard act to follow.

To start with, the 8086 provides a 20 bit address bus, allowing addressing of over a million bytes. To do this, each memory reference instruction first calculates a 16 bit "offset" address, using the normal range of addressing modes. Then the offset address is added to a 20 bit "segment" register to get the final physical address. There are four segment registers: one for the instruction stream, one for the data area, one for the stack, and one "extra". This means programs can be located anywhere in memory; a BASIC interpreter (say) can be shared by many users just by changing data and stack registers; and in general multi - programming is easier. In other words, the chip is designed for time - sharing.

Besides four segment registers, there are four pointer / index registers, and four accumulators, all also be used as eight 8 - bit registers. One pointer register (BP) acts as the stack pointer (within the stack segment), another (BX) as a base register for the data segment. An offset address within a segment can be calculated by adding a base register, one of two index registers (SI and DI), and an 8 or 16 bit displacement. All memory reference instructions allow this four part (segment, base, index, displacement) addressing. This also allows "stack - relative" addressing, in which a program's variables are kept on the stack. PASCAL, ALGOL, and other modern languages use stack - relative addressing to allow recursion and reentrant operation. The chip is designed for PASCAL, as well.

The instruction set is orthogonal; that means it is straightforward and logical, unlike the 8080. Generally, if you can do an operation using one accumulator or addressing mode, you can do the same operation using another one. There are fewer inconsistancies, like allowing some register exchanges but not others. This means assembly language programming is easier, and compilers are simpler and generate more efficient code. The instruction set includes the usual range of move, push, pop, exchange, add, subtract, multiply, divide, and logical operations, on 8 or 16 bit values. Multiply and divide can be signed or unsigned, and "ASCII adjusted" to let you multiply and divide ASCII digits (!). Add and subtract can be "ASCII adjusted" or "decimal adjusted". Flags include carry, half - carry, zero, minus, parity, and overflow. Also, old 8080 programs can be translated to run on the 8086.

Some powerful instructions are included, as in the Z-80. The XLAT instruction will translate a character in one code to another (say, ASCII to EBCDIC), using a 256 byte lookup table. LEA will load the effective address of an operand (important for data structure work), and other instructions support various segment addressing operations. Memory blocks up to 130K bytes long can be moved, compared, scanned for a byte or word value, or set to a value, in a couple of bytes. Controlling a loop with a counter or the zero flag takes one instruction. A "repeat" prefix allows an instruction to be repeated until some termination condition is reached.

Multi-processing (several microprocessors sharing memory) is supported with a prefix instruction that locks the memory bus for the duration of the instruction. One instruction, like an exchange, may take several bus cycles. To share the memory and other resources, an exchange instruction is used as a "request semaphore" operation, which synchronizes the different microprocessor requests. This synchronization must be "indivisible" as far as the memory bus is concerned, hence the need for a lock instruction prefix.

Calls and jumps can go either within the current code segment, or between segments. Intersegment calls apparently allow indirect addressing, so a program in one segment can call a program in another segment through some sort of intersegment jump table. This supports dynamic program relocation. If a program leaves the segment registers alone, and it has not called another program, it can literally be moved to a different section of memory while it is executing, by changing the segment registers and the jump table.

Intel has also discovered signed arithmetic; conditional jumps using flag combinations allow comparing either signed or unsigned values, and jumping appropriately.

Hardware performance has not been overlooked, either. It looks like two versions of the 8086 will be offered, one using a 5 Mhz clock and one running at 8 Mhz. Using the faster clock, two 16 bit values in registers can be added in 375 nanoseconds! Naturally, some addressing modes take time to compute; for example, addressing with a base register, index register, and 16 bit displacement adds 12 clock cycles. Operating on 16 bit values in memory not on an even byte boundary, although allowed, takes additional time, too. Memory cycle time required is 500 nsec; access time 295 nsec. (with the 8 Mhz clock). A 6 byte instruction stream fetch - ahead allows instruction fetch overlapped with execution, and may allow very fast execution of loops less than 6 bytes long. It's a 40 pin package (5 volt supply) with 16 pins multiplexed between data and the lower address bus. Two possible pinouts are provided on the chip, selected by tying one pin high or low. One pinout allows a minimum system, and the other requires an 8288 bus control chip but allows a more complex system. Support chips include the 8284 clock generator (required), 8282 octal latch for bus demultiplexing, and others.

The interrupt structure has been expanded. There are two external interrupt pins (maskable and non - maskable), as well as internal interrupts (traps) for overflow and zero - divide. Any external interrupt can be simulated with a special instruction. A reasonable single - step facility is provided using another internal interrupt and single - step flag. One single - byte subroutine call (restart) is provided which will probably be used for operating system calls.

Intel reserves several interrupt vectors, memory blocks, and input / output locations for their operating system. I hope they provide a standard operating system (like the mini- and maxi- computer manufacturers do). Both Intel and

BOB's BITS

Zilog are getting large programming teams together; they've learned that powerful micros for data processing require software support. Intel has already announced an 8080 to 8086 conversion program, PL/M-86 compiler, macro assembler, and linker / loader.

Zilog has not released as much information about the Z-8000; however, a couple of items have surfaced. It will also provide 16 bit arithmetic (including multiply and divide), and even hints at some 32 bit capabilities. Addressing range is 8 megabytes, implying a 23 bit address bus. There will be 418 instruction combinations, and 16 general purpose 16-bit registers, 15 of which can be used as index registers (sounds like an IBM 360 or Interdata). Zilog also promises support for multi - programming, advanced interrupt / trap facilities, and the speed of a PDP-11/45. Program relocation, and memory protection (which Intel doesn't offer), will be handled with a separate memory - management chip. Finally, the Z-8000 will be bus compatible with the Z-8, a low - end chip useful as a peripheral controller.

I don't know anything about Motorola's 6809 (except that it's a "16 bit microprocessor"). NEC will be announcing a high speed NMOS / CMOS single - chip 16 bit microprocessor at the International Solid State Circuits Conference in February. At the same conference, 5 (five) 65K dynamic RAM's will be announced (right on schedule), as well as an 8K static RAM (1K x 8) by EMM/SEMI. Since integrated circuitry density goes up by a factor of four every two years, we will probably hear about 256K dynamic RAMs and a full size (mid - range) computer on a chip at the 1980 ISSCC conference.

Of course, a full size computer on a chip will not be much use without software to support it and demand from lots of people for that much power. Food for thought.

CONTEST

This software contest is for any previously unpublished program of 2K bytes or less object code, written in the assembly language of any common 8 bit microprocessor.

PROGRAM

1. Any type of program may be entered. An interpreter for a tiny language, a text processor, a monitor, a graphics controller, a game, or some dedicated application could be entered for example.

2. The program must be written for any common 8 bit microprocessor. If the program is written for a CPU other than 8080, Z-80, 6502 or 6800, be prepared to supply your own hardware to demonstrate the program. The same applies for application programs that require unique hardware.

3. The program must be submitted in assembly language. A commented source listing, a source tape and an object tape should be submitted. The tapes may be 8 channel paper or an appropriate audio cassette (KC standard preferred). The program may be written in a high level language like FORTRAN, PL/M or FORTH, provided that it compiles to assembly language and that the compiled assembly language listing and tape contain understandable comments. Any run-time modules must be included with the entry and count towards the 2K of object code.

DOCUMENTATION

The program should be self - documenting, or typed documentation should be provided. A typed program description should be sent prior to the program entry. The program description will be included in the contest catalog of entered programs.

ELEGIBILITY

This contest is open to anyone: hobbyist, student or professional. The program submitted should be previously unpublished and should belong to you. Group entries are OK.

WINNERS / JUDGING

Everybody wins; everybody judges. Each entrant chooses 10 programs from those submitted, and receives them as winnings on paper tape or audio cassette. The 10 programs that are most chosen by the entrants will be declared grand prize winners.

ENTRY FEE

There is a $7 entry fee. The fee will cover the cost of duplicating and mailing your 10 programs plus documentation. The remainder of the fee will go towards the grand prize.

PRIZES

Everybody wins 10 programs of their choice. The authors of the 10 most chosen programs will win grand prizes, which are yet to be determined. We are open for suggestions, perhaps Texas Instruments PROGRAMMERS (or an all expense paid trip to Sumas, Milpitas or Goshen).

LICENSE

Submitting your program will constitute license for the Northwest Computer Society to distribute your program to all entrants of this contest only. You may optionally license the Northwest Computer Society to distribute the software for you on a royalty basis. Or, you can be a nice guy and put your program in the public domain.

DEADLINES

15 July 1978 - Eligibility Deadline. We must have your name, address and $7 by this date.

9 September 1978 - Description Deadline. We must have your program description typed in the proper format for inclusion in the descriptions catalog.

23 September 1978 - Entry Deadline. We must have your program entry, including assembly language source listing, source tape, object tape, and sufficient documentation to test the program.

4 October 1978 - We will mail the catalog of descriptions of all entered programs along with a form for you to choose your 10 programs.

21 October 1978 - Judging Deadline. We must have your order for your 10 programs. The winners will be declared, and we will start sending out tapes.

PROGRAMMING HINTS

1. Common I/O drivers (console, list, reader, punch, cassette) need not be included in the 2K of object code.

2. It would be desirable to have a jump table for the I/O drivers at the front of the program.

3. Constants and globals that affect what memory the program uses should follow the I/O jump table.

ADDRESS FOR ENTRIES

Northwest Computer Society
Mr. John Marshall
P.O. Box 242
Renton, WA 98055

SLOT MACHINE

```
LIST
 10 REM  SLOT MACHINE
 20 REM PALO ALTO TINY BASIC
 30 REM BY MICHAEL HOLLEY
 40 REM
 90 T=0
100 P=0; T=T-1
120 IN. "ENTER 1 AND RETURN"Q
130 IF Q=0 STOP
140 GOSUB 600
160 GOSUB 700
180 GOSUB 800
220 IF A=1 P=3; IF B=1 P=5
240 IF A=2 IF B=2 IF C=6 P=15
260 IF A#B GO. 530
280 IF A#C GO. 530
320 IF A=2 P=18
330 IF A=3 P=8
340 IF A=4 P=10
350 IF A=5 P=20
360 IF A=6 P=200
530 T=T+P
540 P.
550 P."YOU WON $",#1,P
560 P."YOUR TOTAL =",#1,T
570 P.
599 GO. 100
600 X=RND(20)
610 A=6
620 IF X<20 A=5
630 IF X<17 A=4
640 IF X<14 A=3
650 IF X<10 A=2
660 IF X<5 A=1
670 X=A
680 GO. 900
700 X=RND(20)
710 B=6
720 IF X<20 B=5
730 IF X<19 B=4
740 IF X<17 B=3
750 IF X<11 B=2
760 IF X<7 B=1
770 X=B
780 FOR N=1 TO 999
785 NEXT N
790 GO.900
800 X=RND(20)
810 C=6
820 IF X<19 C=5
830 IF X<17 C=4
840 IF X<13 C=3
850 IF X<8 C=2
870 X=C
880 FOR N=1 TO 2000
890 NEXT N
900 P."    ",
910 GO. 920+X
921 P."CHERRY",;R.
922 P."ORANGE",;R.
923 P." BELL ",;R.
924 P."LEMON ",;R.
925 P."  $$  ",;R.
926 P." BAR  ",;R.

OK
.RUN
ENTER 1 AND RETURN:1
   LEMON    LEMON    ORANGE
YOU WON $0
YOUR TOTAL =-1

ENTER 1 AND RETURN:1
   ORANGE   ORANGE   LEMON
YOU WON $0
YOUR TOTAL =-2
```

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