MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Advance Information

1.5 MHz 2.0 MHz

MC68A00•MC68B00
MPU

MC68A21•MC68B21
PIA

MC68A50•MC68B50
ACIA

MCM68A10•MCM68B10
RAM

1.5 AND 2.0 MHz COMPONENTS FOR THE M6800 MICROCOMPUTER SYSTEM

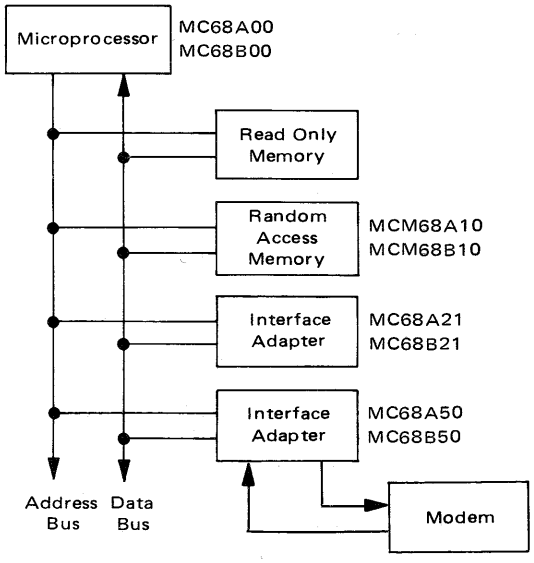
The eight devices described in this data sheet extend the operating frequency of the M6800 Microcomputer Family. The block diagrams and device operation are the same as for the basic M6800-series components.

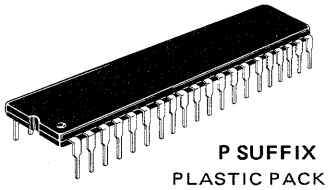
- Fully Hardware and Software Compatible with the M6800 Family
- Power Dissipation Approximately 20% Lower Than on Standard MC6800 Series
- Clock Specification Improved for Reduced Complexity of Clock Generator/Driver Circuitry
- The MC6821 and its higher-frequency versions provide drive capability of two TTL loads on all A- and B-side buffers, improving the drive capability of the MC6820.

MOS
(N-CHANNEL, SILICON-GATE)

MICROPROCESSOR SYSTEM COMPONENTS

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM





P SUFFIX
PLASTIC PACKAGE
CASE 711

NOT SHOWN: **L SUFFIX**
CERAMIC PACKAGE
CASE 715

For additional information on these devices—including block diagrams, signal descriptions, device operation and pin assignments—refer to the *M6800 Microcomputer System Design Data* brochure.

MICROPROCESSING UNIT (MPU)
MC68A00 • MC68B00

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic	V_{IH}	V_{SS} +2.0	–	V_{CC}	Vdc
	$\phi1, \phi2$	V_{IHC}	V_{CC} - 0.6	–	V_{CC} + 0.3	
Input Low Voltage	Logic	V_{IL}	V_{SS} - 0.3	–	V_{SS} + 0.8	Vdc
	$\phi1, \phi2$	V_{ILC}	V_{SS} - 0.3	–	V_{SS} + 0.4	
Input Leakage Current		I_{in}				μAdc
(V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic*		–	1.0	2.5	
(V_{in} = 0 to 5.25 V, V_{CC} = 0.0 V)	$\phi1, \phi2$		–	–	100	
Three-State (Off State) Input Current	D0–D7	I_{TSI}	–	2.0	10	μAdc
(V_{in} = 0.4 to 2.4 V, V_{CC} = max)	A0–A15, R/W		–	–	100	
Output High Voltage		V_{OH}				Vdc
(I_{Load} = -205 μAdc, V_{CC} = min)	D0–D7		V_{SS} + 2.4	–	–	
(I_{Load} = -145 μAdc, V_{CC} = min)	A0–A15, R/W, VMA		V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, V_{CC} = min)	BA		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Power Dissipation		P_D	–	0.5	1.0	W
Capacitance#		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	$\phi1$		–	–	35	
	$\phi2$		–	–	70	
	D0–D7		–	10	12.5	
	Logic Inputs		–	6.5	10	
	A0–A15, R/W, VMA	C_{out}	–	–	12	pF
Frequency of Operation	MC68A00	f	0.1	–	1.5	MHz
	MC68B00		0.1	–	2.0	
Clock Timing (Figure 1)	MC68A00	t_{cyc}	0.666	–	10	μs
Cycle Time	MC68B00		0.50	–	10	
Clock Pulse Width	$\phi1, \phi2$ – MC68A00	$PW_{\phi H}$	230	–	9500	ns
(Measured at V_{CC} -0.6 V)	$\phi1, \phi2$ – MC68B00		180	–	9500	
Total $\phi1$ and $\phi2$ Up Time	MC68A00	t_{ut}	600	–	–	ns
	MC68B00		440	–	–	
Rise and Fall Times (Measured between V_{SS} + 0.4 and V_{CC} -0.6)		$t_{\phi r}, t_{\phi f}$	5.0	–	100	ns
Delay Time or Clock Separation (Measured at V_{OV} = V_{SS} + 0.6 V)		t_d	0	–	9100	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require a 3.0 kΩ pullup load resistor for wire-OR capability at optimum operation.

#Capacitances are periodically sampled rather than 100% tested.

READ/WRITE TIMING

Characteristic	Symbol	MC68A00			MC68B00			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Delay	t_{AD}							ns
C = 90 pF		–	–	180	–	–	150	
C = 30 pF		–	–	165	–	–	135	
Peripheral Read Access Time $t_{ac} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	–	–	360	–	–	250	ns
Data Setup Time (Read)	t_{DSR}	60	–	–	40	–	–	ns
Input Data Hold Time	t_H	10	–	–	10	–	–	ns
Output Data Hold Time	t_H	10	25	–	10	25	–	ns
Address Hold Time (Address, R/W, VMA)	t_{AH}	10	75	–	10	75	–	ns
Enable High Time for DBE Input	t_{EH}	280	–	–	220	–	–	ns
Data Delay Time (Write)	t_{DDW}	–	165	200	–	–	160	ns
Processor Controls								
Processor Control Setup Time	t_{PCS}	200	–	–	200	–	–	ns
Processor Control Rise and Fall Time	t_{PCr}, t_{PCf}	–	–	100	–	–	100	ns
Bus Available Delay	t_{BA}	–	–	270	–	–	270	ns
Three-State Enable	t_{TSE}	–	–	40	–	–	40	ns
Three-State Delay	t_{TSD}	–	–	270	–	–	270	ns
Data Bus Enable Down Time During $\phi 1$ Up Time	$t_{\overline{DBE}}$	150	–	–	70	–	–	ns
Data Bus Enable Rise and Fall Times	t_{DBEr}, t_{DBEf}	–	–	25	–	–	25	ns

FIGURE 1 – CLOCK TIMING WAVEFORM

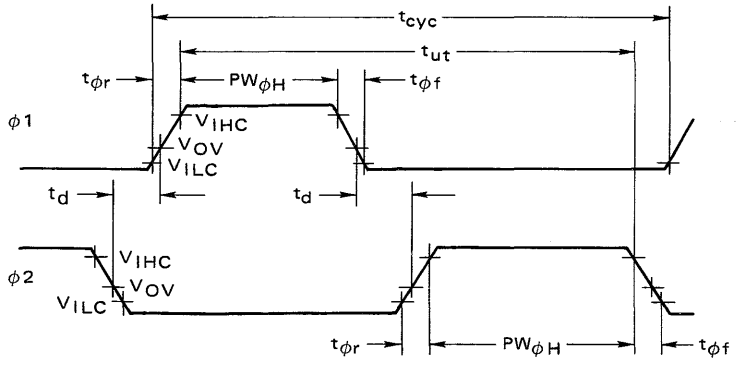
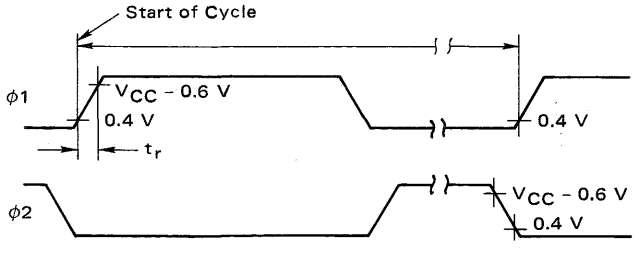


FIGURE 2 – READ/WRITE TIMING WAVEFORM

Measurement point for $\phi 1$ and $\phi 2$ are shown below.
Other measurements are the same as for MC6800.



PERIPHERAL INTERFACE ADAPTER (PIA)
MC68A21 • MC68B21

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	—	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} - 0.3	—	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, $\overline{\text{CS2}}$, CS1, CA1, CB1, Enable	I_{in}	—	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	D0—D7, PB0—PB7, CB2	I_{TSI}	—	2.0	10	μAdc
Input High Current (V_{IH} = 2.4 Vdc)	PA0—PA7, CA2	I_{IH}	-200	-400	—	μAdc
Input Low Current (V_{IL} = 0.4 Vdc)	PA0—PA7, CA2	I_{IL}	—	-1.3	-2.4	mAdc
Output High Voltage		V_{OH}				Vdc
(I_{Load} = -205 μAdc)	D0—D7		V_{SS} + 2.4	—	—	
(I_{Load} = -200 μAdc)	Other Outputs		V_{SS} + 2.4	—	—	
Output Low Voltage		V_{OL}				Vdc
(I_{Load} = 1.6 mAdc)	D0—D7		—	—	V_{SS} + 0.4	
(I_{Load} = 3.2 mAdc)	Other Outputs		—	—	V_{SS} + 0.4	
Output High Current (Sourcing)		I_{OH}				
(V_{OH} = 2.4 Vdc)	D0—D7		-205	—	—	μAdc
	Other Outputs		-100	—	—	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base)	PB0—PB7, CB2		-1.0	-2.5	-10	mAdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$	I_{LOH}	—	1.0	10	μAdc
Power Dissipation		P_D	—	—	550	mW
Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0—D7		—	—	12.5	
	PA0—PA7, PB0—PB7, CA2, CB2		—	—	10	
	Enable, R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1		—	—	7.5	
	$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$	C_{out}	—	—	5.0	pF

NOTE:

The PA0—PA7 Peripheral Data lines and the CA2 Peripheral Control line can drive two standard TTL loads. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	MC68A21		MC68B21		Unit
		Min	Max	Min	Max	
Peripheral Data Setup Time	t_{PDSU}	135	–	100	–	ns
Peripheral Data Hold Time	t_{PDH}	0	–	0	–	ns
Delay Time, Enable negative transition to CA2 negative transition	t_{CA2}	–	0.670	–	0.5	µs
Delay Time, Enable negative transistion to CA2 positive transition	t_{RS1}	–	0.670	–	0.5	µs
Rise and Fall Times for CA1 and CA2 input signals	t_r, t_f	–	1.0	–	1.0	µs
Delay Time from CA1 active transition to CA2 positive transition	t_{RS2}	–	1.35	–	1.0	µs
Delay Time, Enable negative transition to Peripheral Data Valid	t_{PDW}	–	0.670	–	0.5	µs
Delay Time, Enable negative transition to Peripheral CMOS Data Valid (V_{CC} – 30%, V_{CC}; Figure 6, Load C) PA0—PA7, CA2	t_{CMOS}	–	1.35	–	1.0	µs
Delay Time, Enable positive transition to CB2 negative transition	t_{CB2}	–	0.670	–	0.5	µs
Delay Time, Peripheral Data Valid to CB2 negative transition	t_{DC}	20	–	20	–	ns
Delay Time, Enable positive transition to CB2 positive transition	t_{RS1}	–	0.670	–	0.5	µs
Peripheral Control Output Pulse Width, CA2/CB2	PW_{CT}	550	–	550	–	ns
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	–	1.0	–	1.0	µs
Delay Time, CB1 active transition to CB2 positive transition	t_{RS2}	–	1.35	–	1.0	µs
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	t_{IR}	–	1.1	–	0.85	µs
Interrupt Response Time	t_{RS3}	–	1.0	–	1.0	µs
Interrupt Input Pulse Width	PW_I	500	–	500	–	ns
Reset Low Time*	t_{RL}	0.66	–	0.5	–	µs

*The Reset line must be high a minimum of 1.0 µs before addressing the PIA.

BUS TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

READ

Characteristic	Symbol	MC68A21		MC68B21		Unit
		Min	Max	Min	Max	
Enable Cycle Time	t_{cycE}	0.666	–	0.50	–	µs
Enable Pulse Width, High	PW_{EH}	0.280	–	0.22	–	µs
Enable Pulse Width, Low	PW_{EL}	0.280	–	0.21	–	µs
Setup Time, Address and R/W Valid to Enable positive transition	t_{AS}	140	–	70	–	ns
Data Delay Time	t_{DDR}	–	220	–	180	ns
Data Hold Time	t_H	10	–	10	–	ns
Address Hold Time	t_{AH}	10	–	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	25	–	25	ns

WRITE

Enable Cycle Time	t_{cycE}	0.666	–	0.50	–	µs
Enable Pulse Width, High	PW_{EH}	0.280	–	0.22	–	µs
Enable Pulse Width, Low	PW_{EL}	0.280	–	0.21	–	µs
Setup Time, Address and R/W Valid to Enable positive transition	t_{AS}	140	–	70	–	ns
Data Setup Time	t_{DSW}	80	–	60	–	ns
Data Hold Time	t_H	10	–	10	–	ns
Address Hold Time	t_{AH}	10	–	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	25	–	25	ns

NOTES:

1. Figures shown are only those needed to define new measurements *not* specified on the MC6820 data sheet (page 39 of M6800 Microcomputer System Design Data). Refer to that data sheet, or to the new MC6821 data sheet, for further information.
2. On all tests, measurements on the Enable pulse are at 0.8 V and 2.0 V.

FIGURE 3 – PERIPHERAL DATA HOLD TIME (Read Mode)

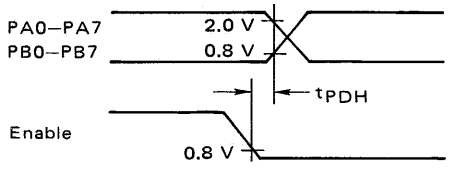


FIGURE 4 – PERIPHERAL CONTROL OUTPUT PULSE WIDTH

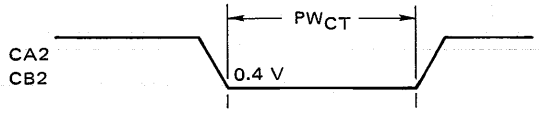
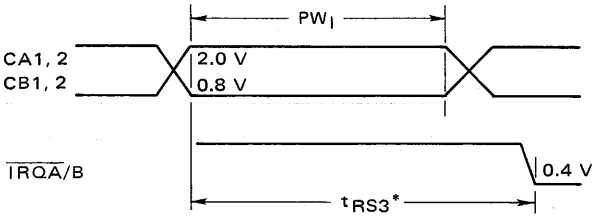


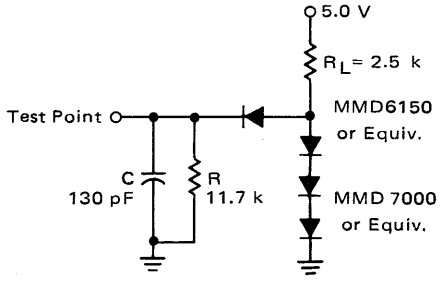
FIGURE 5 – INTERRUPT PULSE WIDTH and $\overline{IRQ}$ RESPONSE



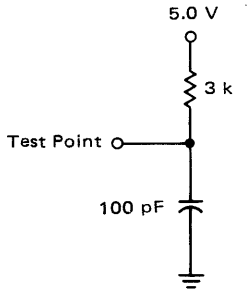
*Assumes Interrupt Enable Bits are set.

FIGURE 6 – BUS TIMING TEST LOADS

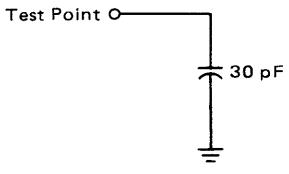
Load A (D0–D7)



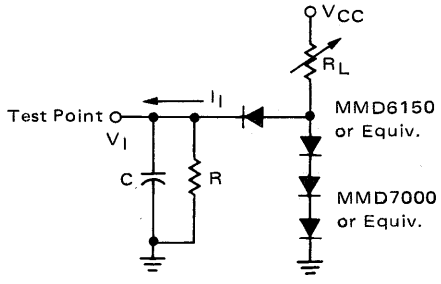
Load B ($\overline{IRQ}$ Only)



Load C (CMOS Load)



Load D (PA0–PA7, PB0–PB7, CA2, CB2)



C = 40 pF, R = 12 k
Adjust R_L so that I_I = 3.2 mA
with V_I = 0.4 V and V_{CC} = 5.25 V

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)
MC68A50 • MC68B50

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	R/W,CS0,CS1,$\overline{CS2}$,Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	D0-D7	I_{TSI}	–	2.0	10	μAdc
Output High Voltage	D0-D7	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width <25 μs)			V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs)	Tx Data, $\overline{RTS}$		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width <25 μs)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation		P_D	–	300	525	mW
Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		–	10	12.5	
	E, Tx Clk, Rx Clk, R/W, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$		–	7.0	7.5	
	$\overline{RTS}$, Tx Data	C_{out}	–	–	10	pF
	$\overline{IRQ}$		–	–	5.0	
Minimum Clock Pulse Width, Low	÷16, ÷64 Modes	PW_{CL}	600	–	–	ns
Minimum Clock Pulse Width, High	÷16, ÷64 Modes	PW_{CH}	600	–	–	ns
Clock Frequency	÷1 Mode	f_C	–	–	500	kHz
	÷16, ÷64 Modes		–	–	800	
Clock-to-Data Delay for Transmitter		t_{TDD}	–	–	1.0	μs
Receive Data Setup Time	÷1 Mode	t_{RDSU}	500	–	–	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	500	–	–	ns
$\overline{Interrupt\ Request}$ Release Time		t_{IR}	–	–	1.2	μs
$\overline{Request\text{-}to\text{-}Send}$ Delay Time		t_{RTS}	–	–	1.0	μs
Input Transition Times (Except Enable)		t_r,t_f	–	–	1.0*	μs

*1.0 μs or 10% of the pulse width, whichever is smaller.

BUS TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

READ

Characteristic	Symbol	MC68A50		MC68B50		Unit
		Min	Max	Min	Max	
Enable Cycle Time	t_{cycE}	0.666	–	0.50	–	μs
Enable Pulse Width, High	PW_{EH}	0.28	25	0.22	25	μs
Enable Pulse Width, Low	PW_{EL}	0.28	–	0.21	–	μs
Setup Time, Address and R/W Valid to Enable positive transition	t_{AS}	140	–	70	–	ns
Data Delay Time	t_{DDR}	–	220	–	180	ns
Data Hold Time	t_H	10	–	10	–	ns
Address Hold Time	t_{AH}	10	–	10	–	ns
Rise and Fall Time for Enable input	t_{Er},t_{Ef}	–	25	–	25	ns

WRITE

Enable Cycle Time	t_{cycE}	0.666	–	0.50	–	μs
Enable Pulse Width, High	PW_{EH}	0.28	25	0.22	25	μs
Enable Pulse Width, Low	PW_{EL}	0.28	–	0.21	–	μs
Setup Time, Address and R/W Valid to Enable positive transition	t_{AS}	140	–	70	–	ns
Data Setup Time	t_{DSW}	80	–	60	–	ns
Data Hold Time	t_H	10	–	10	–	ns
Address Hold Time	t_{AH}	10	–	10	–	ns
Rise and Fall Time for Enable input	t_{Er},t_{Ef}	–	25	–	25	ns

RANDOM ACCESS MEMORY (RAM)
MCM68A10 • MCM68B10

DC CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (A_n, R/W, CS_n, $\overline{CS}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = −205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 0.8 V or $\overline{CS}$ = 2.0 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, all other pins grounded, T_A = 0°C)	I_{CC}	–	–	80	mAdc

AC CHARACTERISTICS

READ CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	
Read Cycle Time	$t_{cyc(R)}$	360	–	250	–	ns
Access Time	t_{acc}	–	360	–	250	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Data Delay Time (Read)	t_{DDR}	–	220	–	180	ns
Read to Select Delay Time	t_{RCS}	0	–	0	–	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Output Hold Time	t_H	10	–	10	–	ns
Data Hold from Write	t_{DHW}	10	60	10	60	ns

WRITE CYCLE (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	MCM68A10		MCM68B10		Unit
		Min	Max	Min	Max	
Write Cycle Time	$t_{cyc(W)}$	360	–	250	–	ns
Address Setup Time	t_{AS}	20	–	20	–	ns
Address Hold Time	t_{AH}	0	–	0	–	ns
Chip Select Pulse Width	t_{CS}	250	–	210	–	ns
Write to Chip Select Delay Time	t_{WCS}	0	–	0	–	ns
Data Setup Time (Write)	t_{DSW}	80	–	60	–	ns
Input Hold Time	t_H	10	–	10	–	ns