MP-ID Interface Driver Board Introduction

The MP-ID interface. driver board is designed to provide the necessary buffering and address decoding for all interface boards attached to the 30-pin I/O bus in SWTPC S/09 computer systems. The MP-ID also contain a parallel output port for attaching a printer or other parallel device to the computer system, an interrupt timer/clock using the 6840 timer for critical timing applications or to be used as a clock and a baud rate clock generator for the various interface, boards installed in the system.

Each function of the MP-ID is discussed separately in some detail. For those users having extra serial terminals and printers connected to the system, the Baud Rate Generator section should be read carefully. To avoid initial confusion for those persons just wishing to use, the board in its standard configuration the various jumpers on the board should be set as follows:

Jumper	Position	
Slow Per/Norm	NOR	
0 - 7	0	selects correct
48-56/56-64	56-64	address range
X1/8	X1	sets correct baud rate multiplier
EX/INT	INT	selects correct clock mode
150/9600	9600	selects 9600 baud
6/12	12	selects 1200 baud
PIA IN/OUT	OUT	selects proper PIA direction

Baud Rate Generator

The MP-ID board contains a baud rate generator necessary to drive the five clock lines on the 30-pin bus of a S/09 computer system. There are three jumpers associated with the baud rate generator. Two clock lines "share" baud rates--one line can be either 600 or 1200 baud and another can be either 150 or 9600 baud. Both of these are jumper selectable. Another jumper provides for a x4 (the board may be labeled x8) multiplication of all rates. This jumper in the x1 position will select the LOW baud rate while the x8 position will select the HIGH baud rates.

BAUD RATE LINE	LOW BAUD	HI BAUD
110	110	440
300	300	1200
600/1200	600 or 1200	2400 or 4800
4800	4800	19,200
150/9600	150 or 9600	600 or 38,400

Jumper positions should be selected in accordance with the serial devices connected to the system

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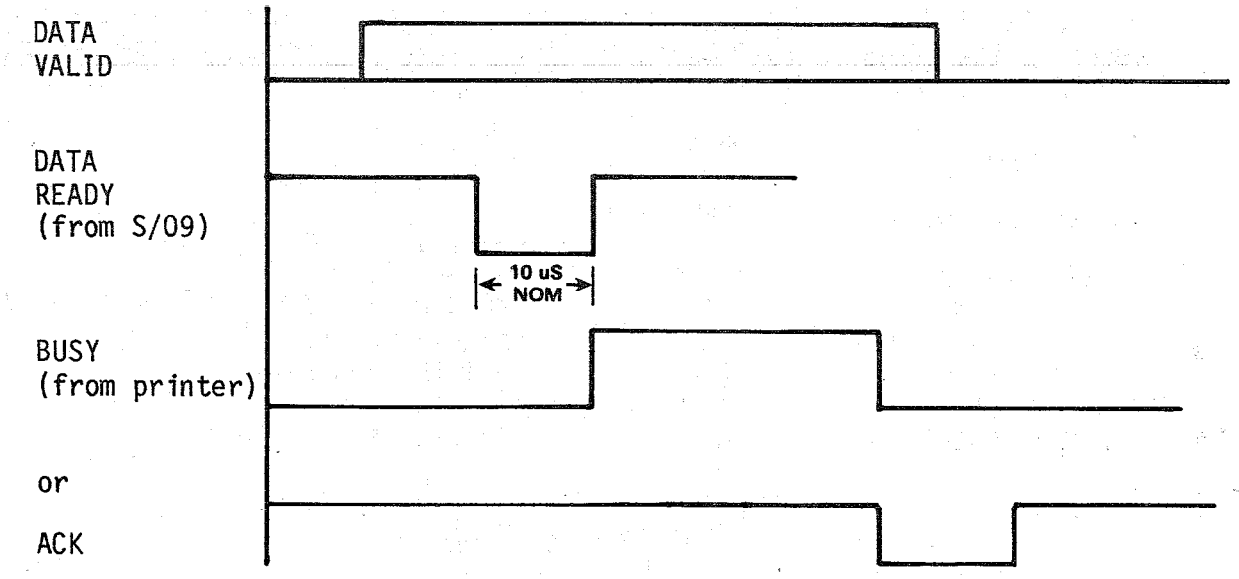
Parallel Output Port

The MP-ID has a built-in parallel interface to connect an 8-bit parallel printer to the system. Connection to the interface is via the 25-pin DB-25 connector on the MP-ID board which is accessible on the S/09 system rear panel. There is one jumper block associated with the interface, the PIA DIR jumper. This jumper should normally be in the OUT position to select the port as an output. All SWTPC supplied software will support a printer using 8 data lines and two handshake lines. Data and handshake timing are as shown below: (either a Printer BUSY or ACKNOWLEDGE line may be used)



Below is a wiring diagram showing the connections for the DB-25 parallel connector:

DB-25	PRINTER
14	DATA BIT 0
15	DATA BIT 1
16	DATA BIT 2
17	DATA BIT 3
18	DATA BIT 4
19	DATA BIT 5
20	DATA BIT 6
21	DATA BIT 7
22	DATA READY
23	BUSY or ACK
1-13	GROUND

All output lines are TTL compatible and are capable of sourcing 15mA and sinking 24mA.

Address Decoding

The MP-ID contains all the circuitry necessary to assign addresses to the I/O ports on the motherboard. Jumper blocks are provided to change the I/O address range as required by the system. One jumper block (48K-56K) assigns the I/O's to an 8K block starting at hex address 0000 (jumper in the 48K-56K position) or at E000 (jumper in the 56K-64K position). Another eight position jumper block (labeled 0 - 7) narrows this 8K range down to 1K byte segments. The various address combinations are shown on the-Address Assignment Table. Individual I/O slots are further decoded to the 16 byte blocks per slot within the selected 1K space.

Address Assignment Table

JUMPER POSITIONS		I/O ADDRESS RANGE
48K-56K	0	C000-C3FF
48K-56K	1	C400-C7FF
48K-56K	2	C800-CBFF
48K-56K	3	CC00-CFFF
48K-56K	4	D000-D3FF
48K-56K	5	D400-D7FF
48K-56K	6	D800-DBFF
48K-56K	7	DC00-DFFF
56K-64K	0	E000-E3FF
56K-64K	1	E400-E7FF
56k-64K	2	E800-EBFF
56K-64K	3	EC00-EFFF
56K-64K	4	F000-F3FF
56K-64K	5	F400-F7FF
56K-64K	6	F800-FBFF
56K-64K	7	FC00-FFFF

I/O Port Addresses are assigned as follows (E000 range for example):

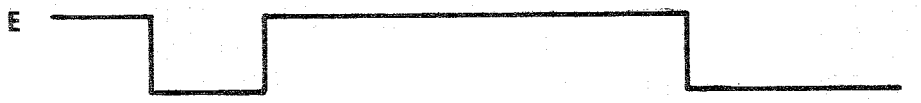
PORT 0	E000	
PORT 1	E010	
PORT 2	E020	
PORT 3	E030	
PORT 4	E040	
PORT 5	E050	
PORT 6	E060	
PORT 7	E070	
PORT 8	E080	(PIA on MP-ID Board)
PORT 9	E090	(6840 on MP-ID Board)

Interrupt Timer/Clock

The MP-ID interface driver contains the circuitry necessary to function as an interrupt timer or as a time of day clock. Clock updating and synchronization is done thru the 50/60 Hz power line thus giving excellent long term accuracy. All operations concerning the timer is handled in the system's disk operating system -- no attempt should be made to directly access the timer's registers. There is one jumper associated with the clock circuitry -- the INT/EXT jumper should normally be left in the INT position. There is also an extra connector on the MP-ID board associated with the timer -- this is for future updating and is not used at this time.

Slow Peripherals

With systems operating at 2 MHz it is sometimes desirable to operate peripheral boards which have a maximum operating frequency' of 1 MHz. By placing the SLOW PER jumper in the SLOW PER position the memory ready bus line will be pulled low each time an access is made to any of the I/O ports. Having this jumper in the SLOW PER position will change the system's E clock as follows:



Normally at 2 MHz and always at 1 MHz this jumper should be in the NORM position.

MP-ID Interface Driver Board
Parts List

Resistors

R1	470 ohm 1/4 watt resistor	R15	6.8K ohm 1/4 watt resistor
R2	"	R16	470
R3	"	R17	1K
R4	"	R18	10K
R5	"	R19	1M
R6	"	R20	10K
R7	"	R21	820K
R8	"	R22	100K
R9	"	R23	100K
R10	"	R24	10K ohm 1% 1/4 watt
R11	"		resistor
R12	"	R25	1K ohm 1/4 watt resistor
R13	"	R26	1M
R14	6.8K ohm 1/4 watt resistor	R27	4.7

Capacitors

C1	20 pfd disc capacitor	C7*	60 or 62 pfd 2%
C2	0.1 mfd disc capacitor		polystyrene capacitor
C3	0.05 mfd disc capacitor	C8	0.1 mfd disc capacitor
C4	0.22 mfd mylar capacitor'	C9	"
C5*	220 mfd 10-volt	C10	"
	electrolytic capacitor	C11	1000 pf polystyrene
C6	0.1 mfd disc capacitor		capacitor
		C12	0.01 mfd mylar capacitor

Semiconductors

Q1*	2N5210 silicon transistor	DI*	1N4148 silicon diode
Q2*	"	D2*	"
Q3*	"		

Integrated Circuits

IC1*	1411 baud rate generator	IC9*	74367 hex buffer
	(MOS)	IC10*	74LS640 octal bi-direc-
IC2*	74LS240 octal buffer		tional transceiver
IC3*	74LS138 3 to 8 decoder	IC11*	74LS32 quad OR gate
IC4*	74LS42 4 to 10 decoder	IC12*	74LS00 quad NAND gate
IC5*	6840 timer	IC13*	96S02 one shot
IC6*	6820/6821 PIA	IC14*	555 timer
IC7*	74LS393 dual 4-bit counter	IC15*	74367 hex buffer
IC8*	74LS245 octal bi-		
	directional transceiver		

Miscellaneous

Y1 1.8432 MHz crystal

All components flagged with a (*) must be oriented as shown in the component layout drawing.