INSTRUCTION MANUAL

D64KB - 64K DYNAMIC MEMORY BOARD

FOR THE SS-50/50C BUS

BOAZ CO.
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TERMS OF SALE

Boards are sold on an "as is" basis with no expressed or implied warranty of any kind.

RETURN PRIVILEGE

This board and the documemtation for it are designed for the advanced computer kit builder. If you should decide that it is beyond your skill level to assemble and checkout this board, you may return it within 15 days after it is received. Full purchase price less handling charge will be refunded to you. All parts were tested before shipping and found to be operational in a correctly assembled board. If you feel that a part is bad or you have problems making the board run, you may call (at your expense) for assistance.

There are no warranties of fitness or merchantibility, either expressed or inplied. In no case are we liable for more than the purchase price of the board.

This documentation is new and could contain errors. If you do find any errors or ommissions of helpful information, please forward them to us. Your board has a registered serial number and any updates will be forwarded to you should any occur.

IMPORTANT NOTICE

ANY RETURN ITEMS MUST BE AUTHORIZED BY BOAZ Co. OR THEY WILL NOT BE ACCEPTED. PLEASE CALL BEFORE YOU RETURN ANY ITEM.

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CHARACTERISTIC	SPECIFICATION
Memory type *	NMOS Dynamic 4116 (200ns) RAM
Memory organization	64K X 8 bits
Memory selectability	Lower 32K is always selected Upper 32K is selected by 4K blocks (except $F000-$FFFF) Upper and lower 32K blocks are interchangable
System clock speed	1 MHz (range of 898.5KHz to 1MHz)
Refresh type	Transparent - during Ø1
Refresh rate	66.67KHz (E/15)
Power requirements *	+5V - 500mA (typical average) +12V - 150mA (typical average) -5V - 7mA (typical average)
Bus compatibility	SS50 or SS50C (boards prior to Rev. 1 or have not been modified do not support extended addressing)
Input signals	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
P.C. Board	Double sided plated-through holes Silkscreen on component side Clear solder mask on wire side
Width & height	9 inches X 5.8 inches
Thickness	0.062 inches
Operating Temperature *	0 to 70 C

*Depends on component selection.

ASSEMBLY INSTRUCTIONS

This memory board was designed for certain components which will be used as a basis for these assembly instructions. However, the use of equivalent devices is not discouraged, even if they are a different physical size.

The following are general recommendations which may make the assembly of this board easier.

A. Read the complete manual before assembly.
B. Use sockets for all IC (Uxx) locations.
C. Use a low wattage soldering iron.
D. Solder only on the bottom side of the board, except in the special case of CR1.
E. Become aware of all assembly operations and component type/placement before you begin.
F. Obtain all parts needed before you begin to assemble the board.
G. Check both sides of the board for manufacturing problems - incomplete etching and trace bridges or breaks (the board manufacturer is good but still only human).
H. Test all capacitors for shorts with an ohmmeter before you install them.
I. Use component carriers for mounting jumpers and resistors in the Uxx locations.

Tools required for assembly.

1. Long nose pliers
2. Diagonal cutters
3. Soldering iron
4. Rosin-core solder

The pliers and cutters should be small for fine work. The soldering iron should have a fine tip (grounded if you are not using sockets for the memory IC's) and use a fine solder (such as Kester .031 diameter 60/40 rosin-core). Correct soldering techniques will result in an operating memory board, whereas, poor workmanship results in a mess which may never work correctly.

1. INSTALL ALL RESISTORS

R1	1Kohm,1/4 watt	(BROWN-BLACK-RED)
R2	1Kohm,1/4 watt	(BROWN-BLACK-RED)
R3	330 ohm,1/4 watt	(ORANGE-ORANGE-BROWN)

An extra row of pads is available at U64 and U65 to mount resistors R11-R23 (10 ohms) and R24 (100 ohms) directly to the board. If you are not using sockets/component carriers for mounting the resistors and jumpers, you should install them at this point. See Figure AI1 for the details on mounting the resistors/jumpers. The jumper assignments are given in Tables 1 and 2.

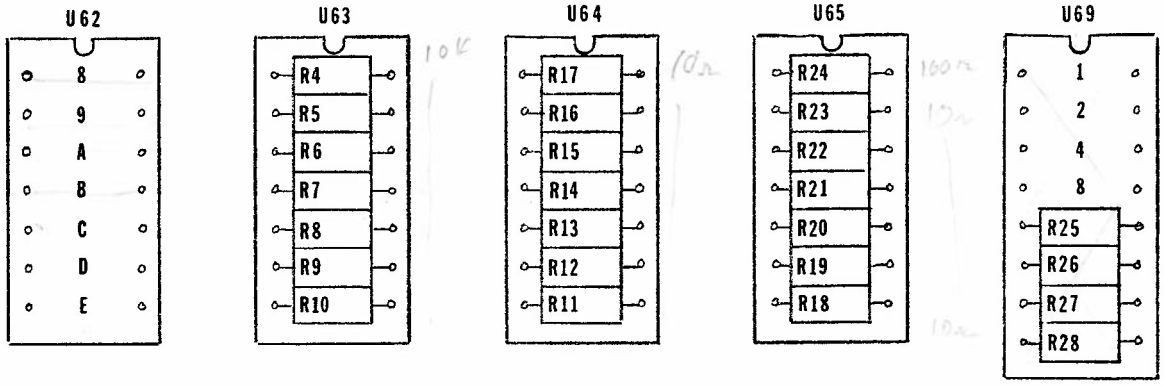


Figure AI1. Resistor/jumper mounting on Component Carriers.

U62 JUMPER	SELECTS
1 - 14	$8000-$8FFF
2 - 13	$9000-$9FFF
3 - 12	$A000-$AFFF
4 - 11	$B000-$BFFF
5 - 10	$C000-$CFFF
6 - 9	$D000-$DFFF
7 - 8	$E000-$EFFF

TABLE 1. UPPER 32K SELECT

U69 JUMPER

1 - 16 = 1
2 - 15 = 2
3 - 14 - 4
4 - 13 = 8

INSTALL JUMPER
Y = YES
N = NO

U69 JUMPER 8 4 2 1	BLOCK NUMBER
Y Y Y Y	0
Y Y Y N	1
Y Y N Y	2
Y Y N N	3
Y N Y Y	4
Y N Y N	5
Y N N Y	6
Y N N N	7
N Y Y Y	8
N Y Y N	9
N Y N Y	A
N Y N N	B
N N Y Y	C
N N Y N	D
N N N Y	E
N N N N	F

TABLE 2. EXTENDED ADDRESSING BOARD SELECT

2. ASSEMBLE THE RESISTOR/JUMPER COMPONENT CARRIERS

IC locations U63, U64, U65 and part of U69 are for resistor pack component carriers (CC). These CC's are plastic and will melt if the pins get too hot. Figure AI1 and Tables 1 and 2 show the mounting for these CC's.

U63	7	10K ohm resistors	(R4-R10)	(BROWN-BLACK-ORANGE)
U64	7	10 ohm resistors	(R11-R17)	(BROWN-BLACK-BLACK)
U65	6	10 ohm resistor	(R18-R23)	(BROWN-BLACK-BLACK)
	1	100 ohm resistor	(R24)	(BROWN-BLACK-BROWN)
U69 *	4	10K ohm resistors	(R25-R28)	(BROWN-BLACK-ORANGE)

IC locations U62 and part of U69* are for jumper selection of memory block and extended addressing, respectively. If you plan on changing these often, you may install dip switches. Otherwise, a wire jumper will work fine. Do not install the CC's into the memory board at this point.

* Install U59 and U69 for extended addressing ONLY!!!!

3. INSTALL ALL IC SOCKETS *

Do not bend any socket leads - this could cause short circuits. Insert all sockets into the board, place a stiff material (clip board, book, etc.) on top of the sockets, then turn over (while holding the sockets in place with the material) and solder two corner pins of each socket. Next solder all pins of all sockets. Be carefull when soldering IC pins which also connect to bypass capacitor leads (there are several in the memory array). Too much solder may fill the hole for the capacitor lead (you might wait to solder these until you have installed the caps).

4. INSTALL THE FOUR VOLTAGE REGULATORS

Refer to Figure AI2 and the parts list to be sure you have the right regulator in the right location. Figure AI2 is on page 8.

5. INSTALL THE CONNECTORS

Insert each of the 5 connectors from the top side of the board. Be sure that each connector seats firmly against the board with no alignment problems. The connectors should be aligned such that no looseness, valley-peak or gap between connectors exists.

6. INSTALL ALL CAPACITORS

NOTE: There are several different value caps and several different voltage ratings for the tantalums (along with the polarity).
BE CAREFULL!!!!!!!

Room has been provided at the upper edge of the board to lay the caps down on the board. This will protect them from movement and the resulting broken leads. All the other caps are to be mounted perpendicular to the board. C17 through C32 and C35 through C48 may require lead bending (depending on the type you use) for proper fit. If so, form the leads before inserting the caps into the board, otherwise, you may destroy the caps. Polarity for the tantalums is indicated on the silkscreen component layout. Follow the layout when inserting the tantalum caps.

7. INSTALL CR1

Be sure the cathode is at the line end as marked on the board. The leads on CR1 must be soldered on both the top and bottom sides of the PC board.

8. INSTALL K1

Isolated jumper posts for selecting A15 or A15 must be installed. Connecting pin 1 to pin 2 selects the normal (A15) configuration for the memory array, pin 3 to pin 4 causes the 32K shift. One configuration must be selected for the board to operate.

NOTE: IF YOU ARE NOT USING EXTENDED ADDRESSING YOU
SHOULD INSTALL A JUMPER FROM U58-4 TO U58-15.
This supplies a pull-up for the open input at
U58-4.
IF YOU LATER DECIDE TO USE EXTENDED ADDRESSING
THIS JUMPER MUST BE REMOVED!!!!!!!!!!!!!!!!!!

9. WORKMANSHIP CHECK!!!!!!

Your memory board is assembled - except for inserting the IC's! Now is the time to go back over all your work to insure no errors have been made.

A. Are all the components in the right place?
B. Are all the caps installed with the correct polarity and the correct voltage rating?
C. Is CR1 installed correctly?
D. Are the voltage regulators in the right locations?
E. Check EACH solder connection - do they all have a bright and shiny apperance? Are any traces shorted together due to your soldering?

10. POWER TEST

With all power off, remove all 50 pin boards from the motherboard. Insert the memory board. Turn on the power and measure the output voltage of each regulator. If you have an abnormal voltage, you should again check your work for errors. Remove the memory board from the computer. Do not proceed any further in the assembly until all voltages are correct. After any errors are corrected, plug the memory board back into the computer and check the voltages. When each voltage is correct, check each voltage pin on a memory IC location to insure that the memory array has the correct voltages connected to it. If all is correct continue in the assembly, if not you must resolve the problem before you can insert any more components!

11. INSTALL IC'S U50 THROUGH U69*

All of these are TTL IC's, component carriers or delay lines and are powered from voltage regulator, VR+5L. Insert the memory board, along with the CPU board, into the computer motherboard and turn on the power. Check pins 8 through 14 on U64 and 8 through 11 and 1 on U65 (resistor packs). There should be pulse activity on each of these pins. If there is not, you have an error in the assembly or a device which is not operating correctly. The error or failure must be found before you can proceed any further. Repeat this process until the signals are there.

*Install U59 and U69 for extended addressing only!!!!

12. INSTALL THE MEMORY IC'S

Load the board with at least one set of 8 memory IC's. These should cover the area required by your monitor progarm. Reinsert the memory board into the computer with the CPU board and power on the computer. If you get no response, power down and recheck your work (the only fault should lie in workmanship or address jumpers). See Table 1, on page 4, to verify your jumper selections. The next section in this manual is on system configuration, read through it and check your selections with it also. Once the computer responds correctly you may install the remaining memory IC's and begin testing for complete operation with memory test programs.

13. CONGRATULATIONS!!!!!!!!!!!!!!

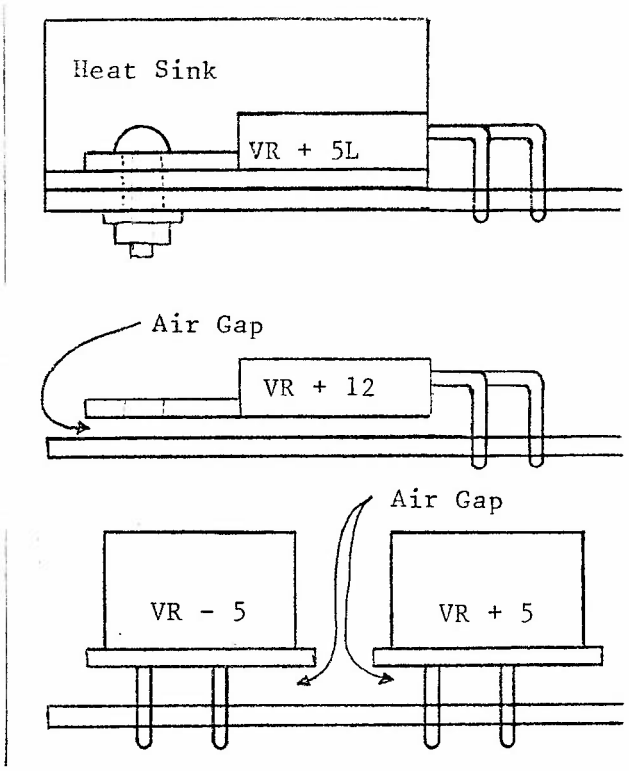


Figure AI2. Voltage regulator assembly.

SET UP PROCEDURE

There are several operational mode selections which must be made before the D64KB is used. The memory areas reserved by your operating system can not be enabled on the memory board. Also, only the memory actually installed and being used should be selected by the on board jumpers. There are three sets of jumper selection areas on the D64KB. The first is for the memory within a 64K Byte board, the second is for the extended addressing mode and the last is the logical 32K shift at K1.

BOARD MEMORY SELECTIONS

The memory on the baord is selected at jumper (or switch, if used) location U62. The following table shows the selections:

U62 JUMPERS	SELECTS	STANDARD ASSIGNMENTS 6800	6809
1 - 14	$8000-$8FFF	I/O*	USER
2 - 13	$9000-$9FFF	I/O*	USER
3 - 12	$A000-$AFFF	DOS	USER
4 - 11	$B000-$BFFF	DOS	USER
5 - 10	$C000-$CFFF	USER	DOS
6 - 9	$D000-$DFFF	USER	DOS
7 - 8	$E000-$EFFF	MON*	I/O*

A selection is made by connecting the pins of U62 as shown in the table. Lets take an example:

> You have 48K of memory on the board in a 6800 system and you want to select only the lower 32K and the memory required by the disk operating system.
>
> U62 jumpers 3 - 12 $A000-$AFFF
> 4 - 11 $B000-$BFFF

This gives you memory from $0000 to $7FFF and from $A000 to $BFFF. The memory in the standard I/O area ($8000-$9FFF) and monitor area ($E000-$FFFF) is not selected.

* SELECTING ANY OF THESE WILL CAUSE A CONFLICT ON THE DATA BUS AND YOUR SYSTEM WILL NOT OPERATE!

EXTENDED ADDRESSING (applies only to Rev. 1 or Mod. boards)

Extended addressing uses four more address lines than the normal 16 of the 6800 or 6809. The primary use of these lines is to select one memory board of several. The four jumper selections on U69 sets up a comparison for these lines and it is a simple four bit binary code. Making a connection between the listed pins on U69 gives a zero value code and no connection gives a one value code.

U69 JUMPER CODES
1 - 16 = 1
2 - 15 = 2
3 - 14 = 4
4 - 13 = 8

JUMPER INSTALLED
Y = YES
N = NO

U69 JUMPERS 8 4 2 1	CARD NUMBER
Y Y Y Y	0
Y Y Y N	1
Y Y N Y	2
Y Y N N	3
Y N Y Y	4
Y N Y N	5
Y N N Y	6
Y N N N	7
N Y Y Y	8
N Y Y N	9
N Y N Y	A
N Y N N	B
N N Y Y	C
N N Y N	D
N N N Y	E
N N N N	F

To set a memory card to a desired extended memory area you should install the jumpers as needed. To set a card for memory area $40000-$4FFFF you would install the following jumpers: 1, 2 and 8 or U69 pins 1 - 16, 2 - 15 and 4 - 13.

APPLIES TO ALL BOARDS

IF YOU ARE NOT USING EXTENDED ADDRESSING YOU MUST

1). REMOVE COMPONENTS AT U59 AND U69
2). CONNECT A JUMPER BETWEEN U58 PIN 4 AND U58 PIN 15

TO LATER USE EXTENDED ADDRESSING

1). REMOVE THE JUMPER (FROM 2 ABOVE)
2). INSTALL THE COMPONENTS IN U59 AND U69

32K SELECTION JUMPER

The jumper at K1 should normally connect K1 pin 1 to K1 pin 2. This routes A15 to U55 and the Row Address Strobe (RAS) lines to the memory chips are ordered (1-2-3-4). By moving the jumper from 1 - 2 to 3 - 4 on K1 the order of the RAS lines shifts around by two (3-4-1-2). What has happened is that $\overline{A15}$ is now routed to U55 and it "thinks" that you are addressing the other half of the 64K memory board.

The Component Placement diagram shows a double address for each set of eight memory chips, ie, U10 to U17 is $0000/$8000. The first address is for K1 jumper at 1 - 2 and the second is for K1 jumper at 3 - 4.

Note also that the memory chips are numbered for the normal configuration of K1. U10 to U17 are controlled by RAS1 and are data bits 0 to 7, respectively. This arrangement is neat if you have memory problems in the area of your monitor or operating system scratch RAM, just move the jumper to the other setting and then test the area of memory that you think is the problem.

Use the above information in configurating your system. It should be very straightforward in most cases.

THEORY OF OPERATION

The memory board is most easily understood by looking at it as several blocks which perform certain logical functions. There is, of course, the memory array itself, which is all important but a slave to the other logic on the board. It is simply assumed to operate as required. The next smaller logic block is the memory management section. Included in this section is the address multiplexing and all memory timing control elements. Add to these the decoding and buffering logic and you have it all. Now we will look at each section in detail.

BUS BUFFERS

Bus buffers are used to isolate the memory board from the computer motherboard bus and to provide some protection for the components on the board. U50 and U60 isolate the computer data bus from the memory board and are controlled by the decode logic. This control ensures that memory data is never applied to the motherboard bus except when the CPU executes a read from the memory board. The address decode, E, VMA and R/W all get combined in the single line which controls the data bus buffers. These buffers are 8T26 inverting transceivers, but could as well have been 8T28 non-inverting buffers since the memory does not care if the data is inverted or not.

The address lines which drive more than one load or must be inverted are buffered by U51. Again a 8T26 works out well for both these requirements. The extended address lines are applied to U59, a comparator (74LS85), which acts as a one TTL load buffer and bank address select comparator. The bank address is set by the jumper connections on U69. 16 banks, hex 0 to F, may be selected. If extended addressing IS NOT used for bank selection of boards, the components should not be put in either U59 or U69. In such case it would be advisable to jumper U58 pin 4 to U58 pin 15, which is connected to a pull-up resistor.

The three control lines, E, VMA and R/$\overline{W}$ are buffered by U58 and inverted as required.

ADDRESS DECODE LOGIC

A five chip address decode is used to enable the memory controller and data bus buffers. U52, U53, U61, U62 and U63 are used to select the lower 32K ($0000-$7FFF) and any or all 4K blocks in the upper 32K, except the top 4K ($F000-$FFFF). The $ sign notation indicates that the number is in hexadecimal. These 4K block selections are made by jumpers (or switches) on U62, which connect the outputs of the decoder, U61, to U52, an 8 input NAND gate. The 10K ohm resistor pack at U63 provides the pull-ups for the unused inputs of U52. The output of U52 goes high when any of it's inputs goes low.

This signal gets combined with VMA in U53A and causes the memory controller to be selected for all valid addresses in the lower 32K and the jumper selected 4K blocks of the upper 32K. This select signal gets combined with R/$\overline{W}$ via U53B, C and D and becomes the data direction control for the data buffers.

To allow complete testing of the memory board (since this may be the only memory board in a system) K1 can be used to exchange the logical address of the upper and lower 32K memory blocks. When A15 is input to the A15 pin of the memory controller (U55) the Row Address Strobe signals are ordered, but when $\overline{A15}$ is used for this input a 32K logical slip occures. We now have addresses $0000-$7FFF slipped up to $8000-$FFFF and, of course, $8000-$FFFF logically slipped down to $0000-$7FFF. Table 1 shows this logical memory shift.

MEMORY MANAGEMENT

The memory management logic group consists of U54-U57 and U66-U68. All timing and conrtol signals required for refresh and processor accesses to the memory are handled by these elements. The refresh clock is derived by dividing the 1MHz system E clock by 15. A refresh access occurs once every 15 cycles or at a rate of 66.7KHz. The minimum specified rate is 64KHz. Operating above the minimum specified rate is acceptable, but higher rates increase the memory power dissipation. Therefore, it is best to operate the refresh function as close to 64KHz as possible.

The refresh clock drives the seven bit refresh counter in the Address Multiplexer IC (U54 pin 1) and is the refresh signal to the Memory Contorller IC (U55 pin 21). Each negative edge increments the counter and each positive edge initiates a refresh access. The additional timing signals for memory control are generated by U56, U57, U66 and U67. These signals are applied to the memory controller IC as inputs t1, t2, t3, t4 and t5. All memory timing signals are based on these five lines. A step-by-step walkthrough of all the events in both a refresh and normal CPU memory access is the best way to understand it all, and that is next.

READING, WRITING AND REFRESHING

The memory timing diagram, Figure TD1, shows how and why the events occur for a write, refresh and read access. The sequence in which they are shown relates only to how such operations function and do not imply a certain instruction execution sequence. In relation to the system clock, E, a refresh always begins and finishes within an $\overline{E}$ time and a CPU access always begins and finishes within an E time. Follow both the logic diagram and the timing diagram closely while studying this section.

The non-expanded portion of the timing diagram shows the relationship of the refresh signals to the system clock, E. The expanded portion shows the memory management/interface signals in relation to E. The illustrated sequence is a CPU

write access, a refresh access, a CPU read access and an idle time. Each of these occupy one-half cycle of E, with the CPU accesses during E and the refresh/idle accesses during $\overline{E}$.

Many times the memory must respond to a double access during one system clock time. This timing requires that the memory IC's have a cycle time (NOT ACCESS TIME) less than 1/2 the system clock period. a 4116 with an access time of 150ns has a cycle time of 375ns and one with a 300ns access time requires 660ns per cycle. The former may be used in transparent refresh at 1MHz, but the latter has too long a cycle time. Memory IC's with 200ns access time is recommended for use in this design. With a system clock speed of 1MHz, the memory cycle time must be less than 500ns.

In the non-expanded portion, the refresh clock (RC) is 1/15th the rate of E (66.7KHz.) because of the divide by 15 in U68. The Refresh Grant (RG) signal is $\overline{E}$ (inverted by U55). The rising edge of the RC causes the Refresh Request ($\overline{RR}$) output line of U55 to go low and it is set again by signal t1 into U55. Every negative edge of RC causes the 7-bit refresh counter in U54 to increment. Note that during the time $\overline{RR}$ is low the RG signal goes positive, this is important and not shown in the expanded portion of the timing diagram.

WRITING

The expanded portion picks up at the point one-half clock (E) period before a refresh access takes place and continues one full cycle after it. Certain events must occur in precise timing relationships, follow the timing diagram very carefully.

The positive edge of E clocks the low (grounded) level through U56B forcing U57-3 to go high. This starts a positive transition down the delay line at U67-2. 100ns later this positive edge is applied to U55-t1 input, which causes the Row Address Strobe ($\overline{RAS}$) line (decoded from A14 and A15 inputs to U55) to go low. Using the control lines Row/Column Select (R/C) and Refresh Address Enable (RA), U55 determines the address type (Row, Column or Refresh) to output to the memory IC's. RA is overriding and any time it is high it forces the refresh address to be output. When RA is low a row or column address is output. A row address is output when R/C is high and a column address is output when it is low. R/C is now high and the row address is output. The row address (A0-A6) of the memory location is latched into the memory IC's. 25ns later the positive edge sets U56B via U57-11 and also is applied to U55-t4 input. t4 enables the memory write ($\overline{WE}$) output of U55 to go low for a write data into memory if the system R/$\overline{W}$ line is low. The t4 signal may occur any time after t1 is activated. If T4 always preceeds t3, a special mode called "write early" may be ulitized with the memory IC's. The write early mode allows the data in and data out pins of the memory IC's to be connected together. We now have the $\overline{WE}$ line low since R/$\overline{W}$ is low.

As a result of U56B being set, the input to the delay line goes low and a true positive pulse is now moving down the delay

line with a width of 125ns. Another 75ns later the rising edge of the delay line pulse is applied to t2, which causes R/C to go low. The column address (A7-A13) is now output from U54. 50ns later the pulse is applied to t3, which causes the $\overline{CAS}$ line to go low, latching the column address of the memory location into the memory IC's.

Also, since the write early mode is used, the data to be written into the memory is latched in by the $\overline{CAS}$ signal. We now have the 14 address lines and the data latched into the memory IC's. All that remains is for the access to be terminated by the pulse applied to t5 of the memory controller to return all signals to their idle state. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and R/C all return high terminating the CPU write access. That is how the writing is done.

REFRESHING

The next half-cycle ($\overline{E}$ time) is a refresh access. A positive transition of the refresh clock initiates a refresh access to the memory board. When this occurs the refresh request output of U55 immediately goes low, which enables the internal circuitry of the memory controller to allow a memory refresh by the refresh grant activation. This causes several reactions. The R/C line is forced low but is overriden by the RA line which goes high. This ensures that a refresh address will be output from the address multiplexer to the memory array. Also, the $\overline{RR}$ low level is clocked through U56A by RG. This low level is inverted by U57A and starts a positive transition down the delay line. From here on it is similar to a CPU access, but several important differences exist.

Timing signal t1 causes $\overline{RR}$ to return high and ALL FOUR $\overline{RAS}$ outputs of U55 to go low. This latches the refresh address into the memory IC's (all 32). This is all that is required for refreshing the total memory array. 25ns later the positive transition causes U56A to be set and t4 input to enable the memory controller for a write (this always occurs for the write early mode). The big difference in the refresh access is that the timing signals t2, t3 and t4 result in NO action by the memory controller (U55). The refresh is accomplished by the 4 $\overline{RAS}$ lines only, so there is no need for any other signals to the memory array. The refresh access must be terminated and again t5 takes care of this. All four $\overline{RAS}$ lines return high as does Row/Column Select while Refresh Address Enable is taken low.

READING

A read access by the CPU is accomplished exactly the same as a write access except that the system R/$\overline{W}$ line is high and, therefore, the memory $\overline{WE}$ output of U55 does not go low.

MISCELLANY

Questions always arise about the reason for the resistors between the output of the memory management IC's (U54 and U55) and the memory array. The resistors form a type of line termination called series damping. They reduce the over/under shoot (ringing) by matching the impedance of the TTL drivers to that of the MOS memory IC's. This technique is very effective. Also, this type of line termination does not increase the power dissipation as do other types.

The 4116 memory IC uses -5V as a substrate bias voltage. This voltage must be more negative than any other voltage applied to the memory IC. CR1 is a Schottky rectifier diode which has a switching time of 10ns and can handle current up to 1A. This is not for prolonged protection but the momentary kind of odd-ball happenings, like when checking points on the board with a scope probe, and you short a line to Vbb (-5V).

If you are not using extended addressing two things must be done. First, do not istall U59 and U69. Secondly, you must jumper U58-4 to U58-15 (provides a pull-up resistor for the open input). However, if you later use extended addressing, you must reomve this jumper.

MEMORY TESTING

A disadvantage to a single RAM board for all the memory in a system is that it is impossible to do anything if you have a memory failure in the monitor scratch storage area. An easy way around this is to logically shift the memory so that the upper 32K becomes the lower 32K and the lower 32K shifts up to the upper 32K. Jumper K1 allows the use of address bit A15 or $\overline{A15}$ to be applied to the memory controller IC (U55). This makes the logical shift of 32K by re-defining the RAS outputs. Now you can test any part of the memory board by this logical shift. Table 1., shows how this logical slip takes place. The system does not realize that a change has taken place since only the line to the memory controller has been changed.

A15	A14	$\overline{RAS}$	$\overline{A15}$	A14	$\overline{RAS}$
0	0	1	1	0	3
0	1	2	1	1	4
1	0	3	0	0	1
1	1	4	0	1	2

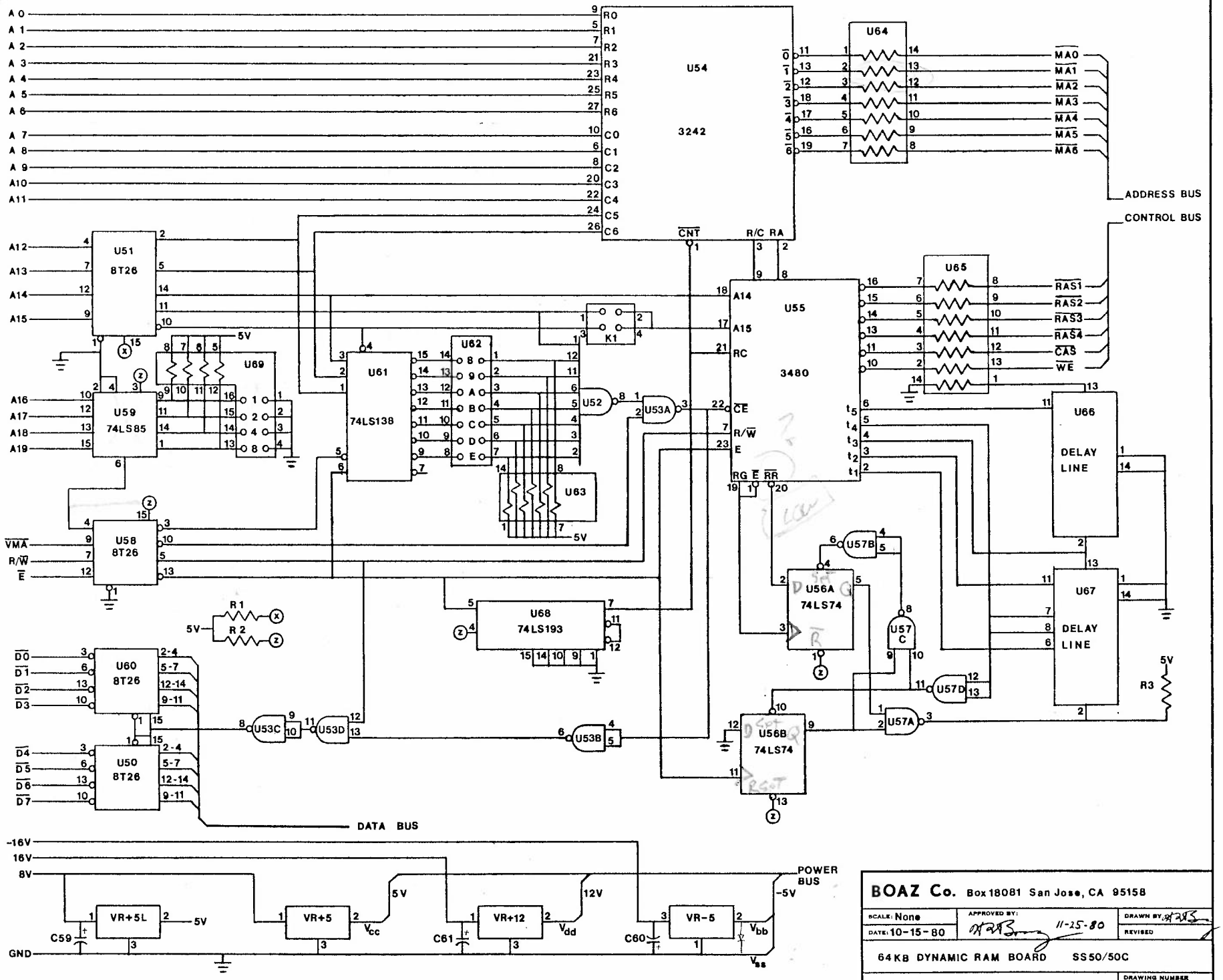
Table 1. Inverting A15 shifts the memory blocks and changes the order of the RAS outputs.

MEMORY ORGANIZATION

The memory IC's are organized into an array of four rows of eight columns. Each row is a 16K block of memory and each column is one data bit. The memory IC's are numbered by row (tens digit) and column (units digit); U10-U17, U20-U27, U30-U37 and U40-U47. The tens digit represents a specific 16K block of memory while the units digit represents a data bit. Row 1 is block $0000-$3FFF, Row 2 is $4000-$7FFF, Row 3 is $8000-$BFFF and Row 4 is $C000-$FFFF. Therefore, U10 is data bit 0 in the memory block $0000-$3FFF, U35 is bit 5, $8000-$BFFF and U47 is bit 7, $C000-$FFFF. $\overline{RAS1}$ selects Row 1 and is connected to only Row 1 IC's, $\overline{RAS2}$ to Row 2, $\overline{RAS3}$ to Row 3 and $\overline{RAS4}$ to Row 4. However, the seven address lines ($\overline{MA0}$-$\overline{MA6}$), $\overline{CAS}$ and $\overline{WE}$ connect to the appropreate pins of all 32 memory IC's.

Due to the exclusive use of the write early mode ($\overline{WE}$ asserted prior to $\overline{CAS}$) the data in and data out pins of each memory IC are connected together.

The power connections to the memory array requires special attention. To those who do not believe in the value of decoupling capacitors - BEWARE!!! Almost all the circuitry in the memory IC's is dynamic and takes greater power when an address edge occurs. These edges are very fast causing peak currents 10 times the normal level. Also, the duration of this peak power is very short. It is the capacitors which supply this instantaneous power. The decoupling capacitors controls the current transients and prevents voltage spikes which could cause loss of data and soft errors. The larger capacitors in the memory array provide energy storage to prevent power supply droop.



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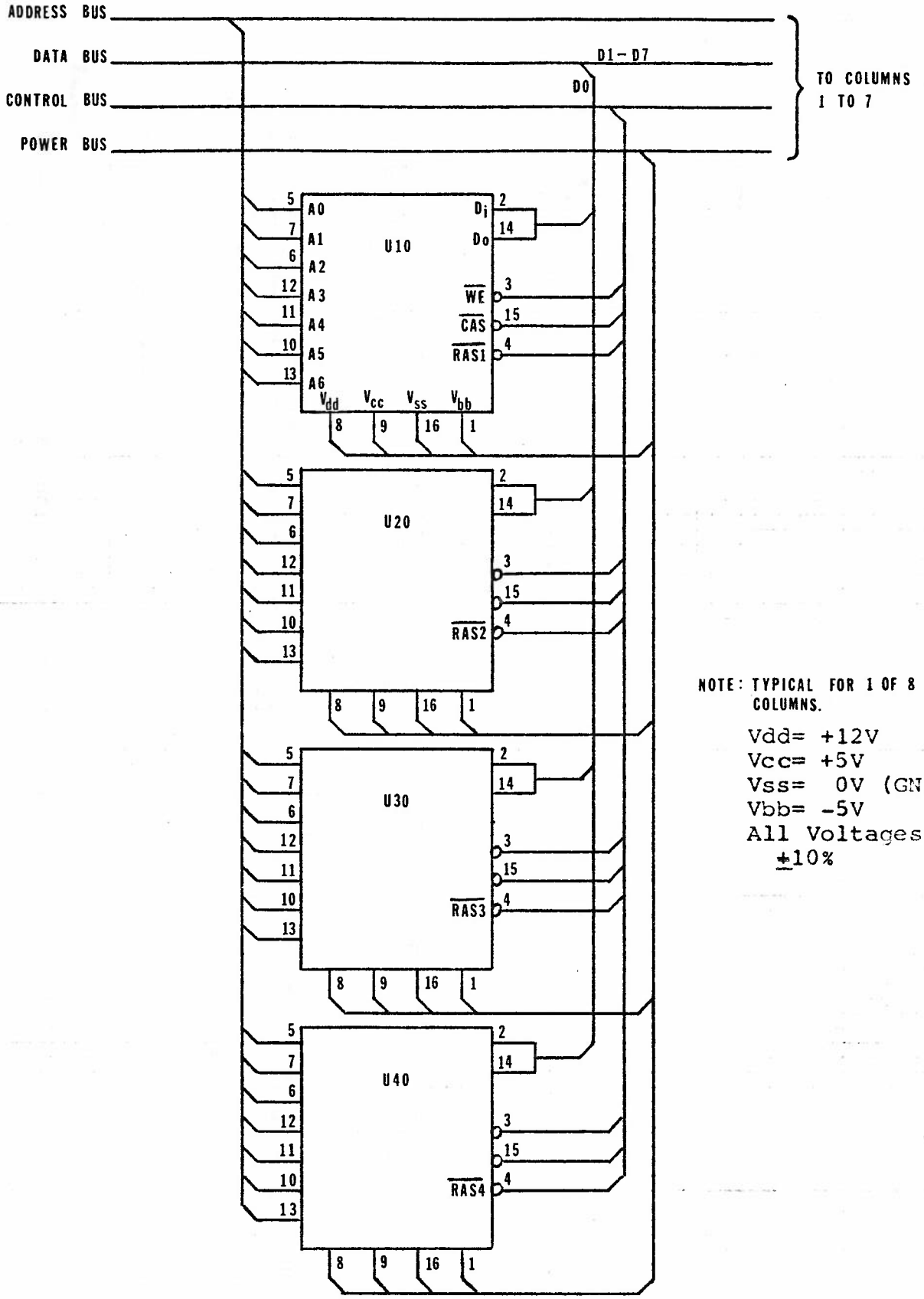
SCALE: None	APPROVED BY:		DRAWN BY:
DATE: 10-15-80		11-25-80	REVISED

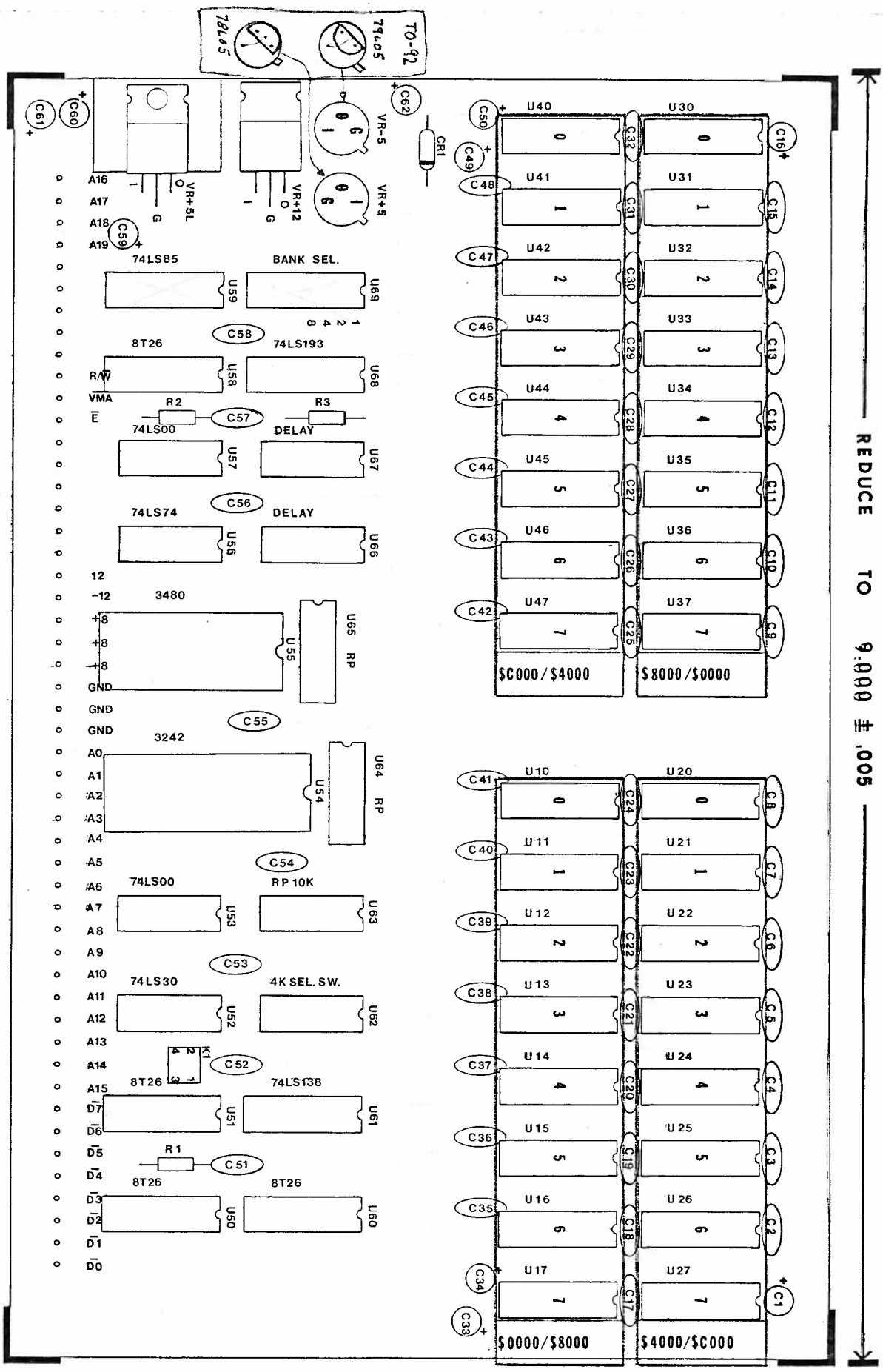
64KB DYNAMIC RAM BOARD SS50/50C

DRAWING NUMBER LD 1028 1/2



NOTE: TYPICAL FOR 1 OF 8 COLUMNS.

Vdd= +12V
Vcc= +5V
Vss= 0V (GND)
Vbb= -5V
All Voltages ±10%



REDUCE TO 9.000 ± .005

COMPONENT PLACEMENT

ITEM	QUAN	REFERENCE DESIGNATION	PART NUMBER/VALUE	DESCRIPTION
1	1		D64KB	Printed Circuit Board
2	32	U10-U17, U20-U27 U30-U37, U40-U47	MC4116C20	16Kx1 Dynamic Memory IC
3	4	U50,U51,U58,U60	MC8T26P	TTL Quad Bus Transceiver
4	1	U52	74LS30	TTL 8-input NAND Gate
5	2	U53,U57	74LS00	TTL Quad 2-input NAND Gate
6	1	U54	MC3242AP	TTl Mem. Addr. Multiplexer/Ref. Cntr.
7	1	U55	MC3480P	TTL Dynamic Memory Controller
8	1	U56	74LS74	TTL D-type Flip-Flop
9	1	U59	74LS85	TTL 4-bit Magnitude Comparator
10	1	U61	74LS138	TTL 3-to-8 Decoder
11	2	U66,U67	DL1601	Delay Line, 250ns
12	1	U68	74LS193	TTL 4-bit Sync. Up/Down Cntr.
13	1	VR+5L	MC7805CT	Voltage Regulator, +5V @1.5A.
14	1	VR+5	MC78L05CG	Voltage Regulator, +5V @.1A.
15	1	VR+12	MC7812CT	Voltage Regulator, +12V @1.5A.
16	1	VR-5	MC79L05CG	Voltage Regulator, -5V @.1A.
17	1	CR1	1N5817/MBR120P	Diode, Schottky Rectifier
18	7	C1,C16,C33,C34 C49,C50,C62	33uF	Capacitor, Tantalum,Dipped, 16WV
19	52	C2-C15,C17-C32 C35-C48,C51-C58	0.1uF	Capacitor, Disk (bypass) 16WV
20	3	C59-C61	2.2uF	Capacitor, Tantalum,Dipped, 25WV
21	2	R1,R2	1K ohm	Resistor, 1/4Watt
22	1	R3	330 ohm	Resistor, 1/4Watt
23	11	R4-R10,R25-R28	10K ohm	Resistor, 1/4Watt
24	13	R11-R23	10 ohm	Resistor, 1/4Watt
25	1	R24	100 ohm	Resistor, 1/4Watt
26	1			Heat Sink, W/Hareware
27	4			Component Carrier, 14 pin
28	1			Component Carrier, 16 pin
29	5			Connector, Molex, Female, 10 pin
30	10			Socket, Solder, 14 pin
31	40			Socket, Solder, 16 pin
32	1			Socket, Solder, 24 pin
33	1			Socket, Solder, 28 pin
34	2	K1		Jumper Block, 2 position

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PARTS LIST
D64KB MEMORY BOARD

DATE 10-15-90 | DE

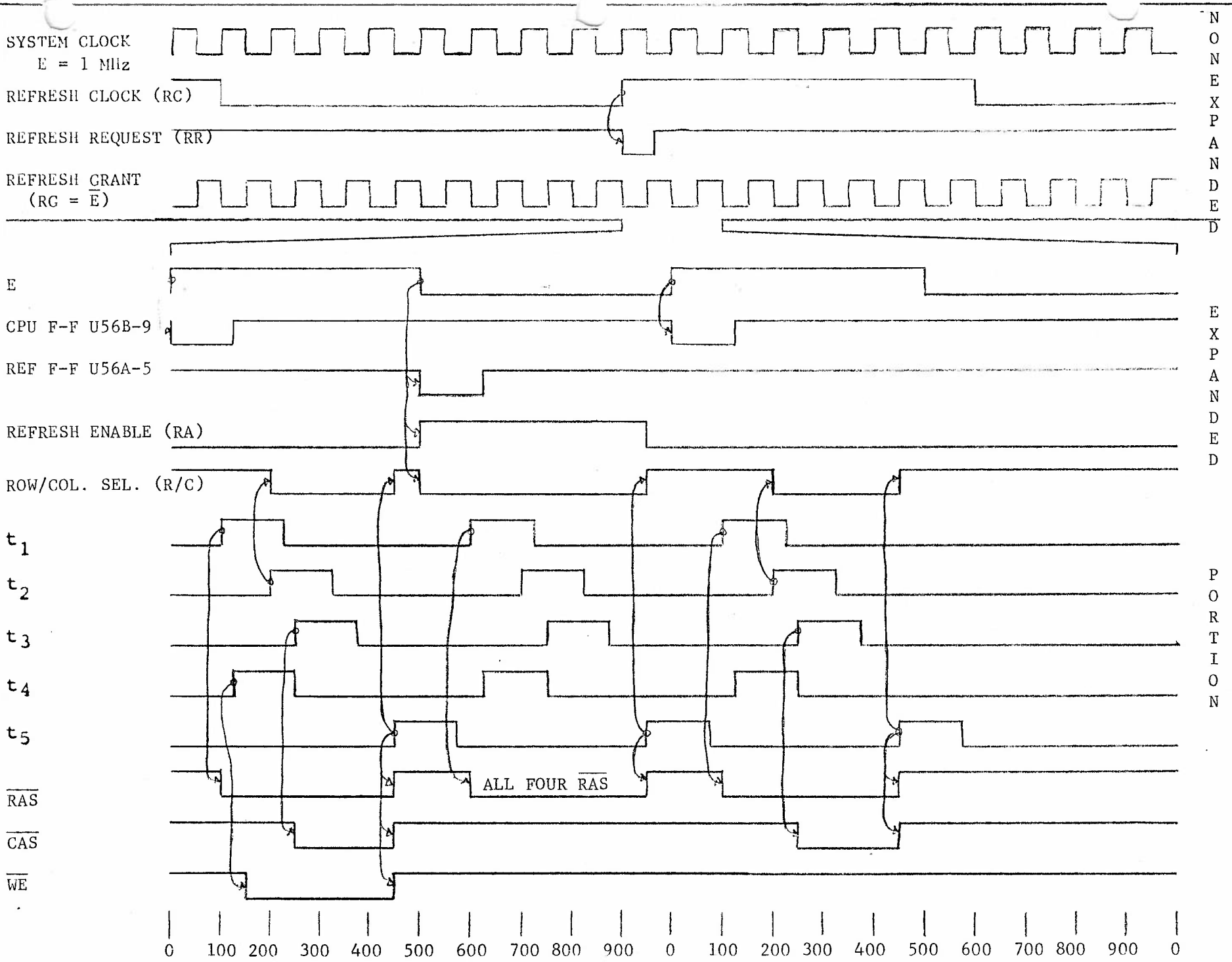


Figure TD1. Timing Diagram

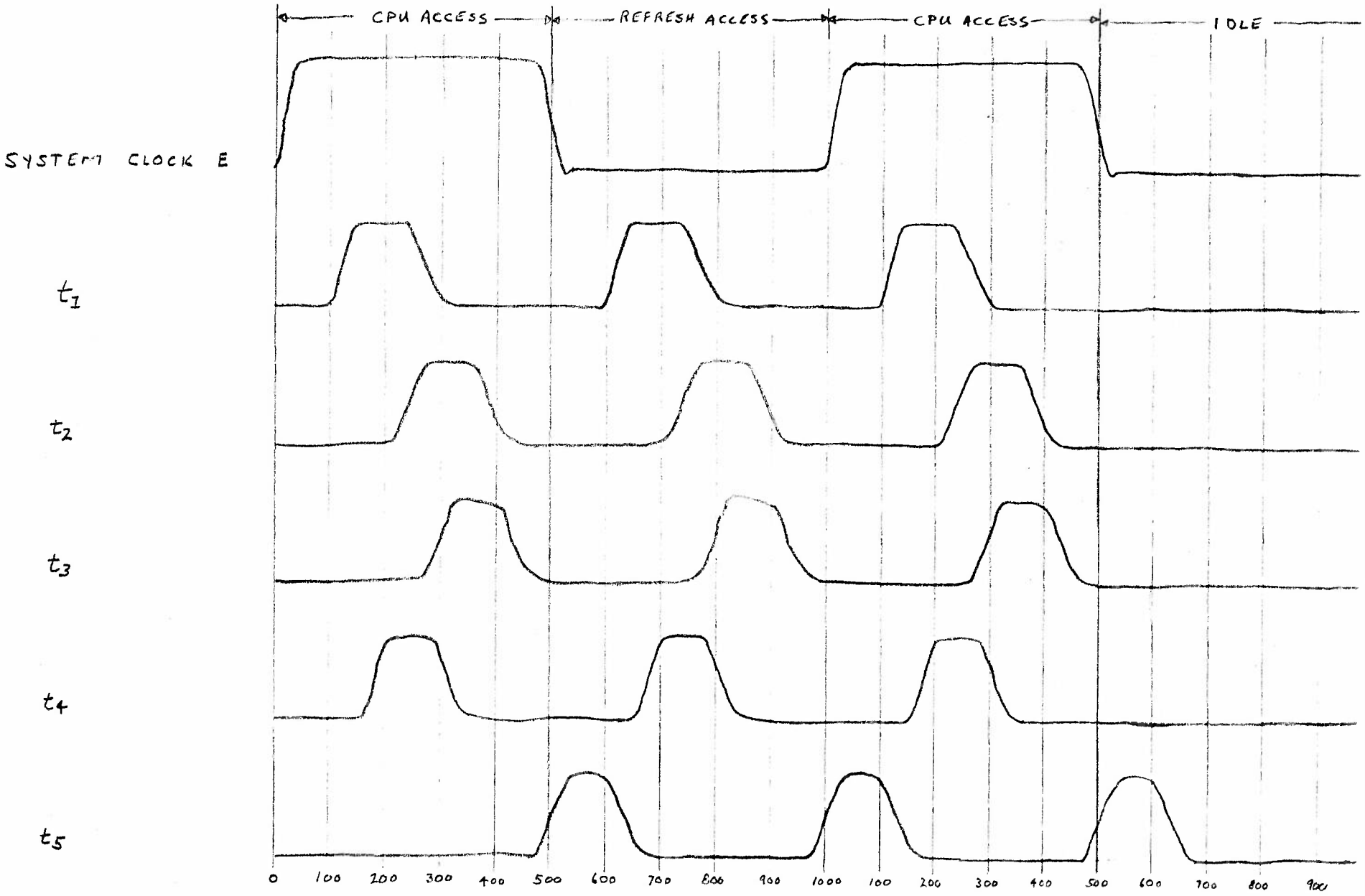


FIGURE TD2. ACTUAL TIMING RELATIONSHIP OF E TO "t" SIGNALS (1MHz OPERATION)

HINTS ON CONSTRUCTION AND BRING-UP

1. Tantalum capacitors operate best at close to (above) their rated voltage, ie, on the +12V line a cap rated at 16V is better than one rated at 35V.

2. The value for the tantalum caps C1, C16, C33, C34, C49, C50 and C62 is a conservative value, however, do not go below 22uF @ 16V.

3. When using an elecrolytic (not tantalum) cap you should use at least three times the value capacitance called for in a tantalum capacitor.

4. A tantalum cap installed reversed will tend to cause problems in several ways:

   (a) It may explode!
   (b) if rated at many times the applied voltage it may act as a capacitor for a long period of time.
   (c) It most likely will feel warm to hot.
   (d) It may pull down the voltage line it is on.
   (e) In any of these cases it will likely generate errors in the memory IC contents.

5. One unconnected power supply pin on one IC can cause the entire board to appear bad. Be sure all pins are soldered and the solder joints are bright and shiny - a soldered connection with a dull appearence is almost always an indication of a "cold" or bad solder joint.

6. An address is always being output to the memory array via U54 and U64. If no accesses are made to the memory array RAS1, RAS2, RAS3 and RAS4 will go active (low) every 15 clock (E) cycles. CAS and WE will remain high.

7. The data buffer direction control is normally high, allowing data on to the memory board and goes low to allow a CPU read from the board.

8. No jumpers on U62 allows only the lower 32K to be used ($0000-$7FFF). Consider the following in making your selection of jumper connections:

   1-14 = $8000-$8FFF - I/O area
   2-13 = $9000-$9FFF - I/O area
   3-12 = $A000-$AFFF - Monitor scratch area and
   4-11 = $B000-$BFFF - Disk Operating System
   5-10 = $C000-$CFFF - User
   6-9 = $D000-$DFFF - User
   7-8 = $E000-$EFFF - Monitor ROM

INSTRUCTIONS TO MODIFY THE D64KB TO REV. 1.

The D64KB was designed for a 6800 SS-50 bus system and requires a modification for SS-50C operation. Enclosed are the instructions to modify your D64KB to Rev. 1. However, if you will NOT be using extened addressing, you should DO NOTHING! In all SS-50 bus systems using the 6800/01/09, the D64KB fills the need for the maximum read/write memory you can use.

YOU MAY CREATE A PROBLEM BY ATTEMPTING A MODIFICATION YOU DO NOT NEED!!!!!!!!!!!!!!!!

Should it be required, do the following:

1. Cut traces as shown in red on the printed wiring artwork sheet.

   There are 8 traces to cut! On the bottom side of the board the cuts should be exactly as shown. On the top side, if the sockets are not yet installed, cut the traces at the end points on the trace. If the sockets are already installed, make the cuts between the end points as shown.

2. Add the following (all on the bottom side):

   a. U61-1 to U51-5
      U54-26 (via feedthrough under U36)

   b. U61-2 to U51-14
      U55-18 (via cut traces under U62)

   c. U61-3 to U51-11

   d. U61-4 to U61-5 OR U61-8 (ground)

   e. U61-7 to U62-9 (new hole)

   f. U51-2 to U54-24

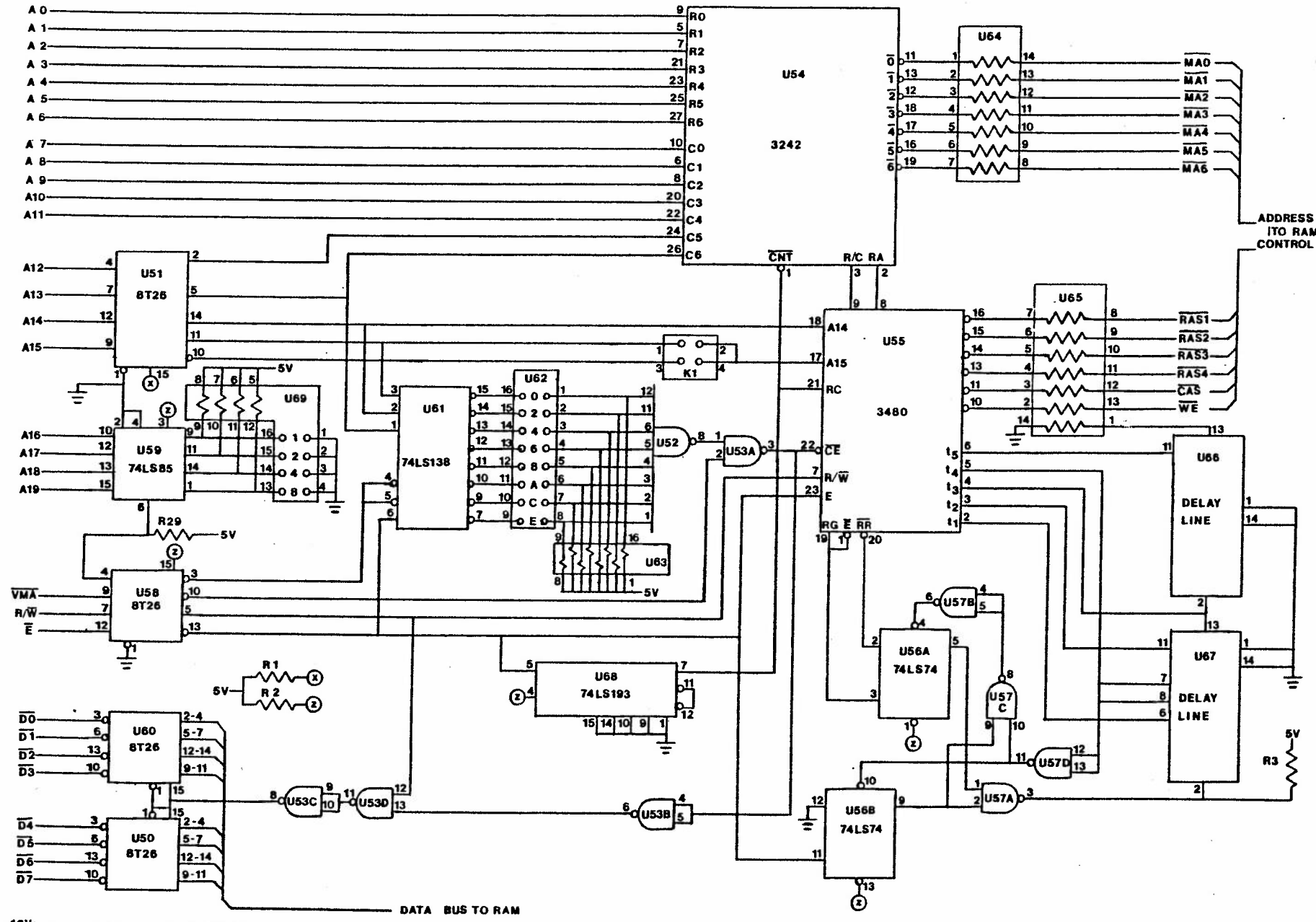
   g. U52-1 to U62-8 (new hole)
      a 10K ohm, 1/4 watt resistor to +5V.

3. Add R29 a 10K ohm 1/4 watt resistor between +5V and U59-6 (new hole for R29 near U59). Install on the top side of the board.

Your D64KB now provides full extended addressing and selection of the 64K in blocks of 8K each.

IF these modifications ARE installed, the selection of memory within the 64K board at U62 will be as listed:

U62 pins jumpered	MEMORY SELECTED
1 to 16	0000-1FFF
2 to 15	2000-3FFF
3 to 14	4000-5FFF
4 to 13	6000-7FFF
5 to 12	8000-9FFF
6 to 11	A000-BFFF
7 to 10	C000-DFFF
8 to 9	E000-FFFF



REVISION: 1 - DECODE/E.A. 5-10-81

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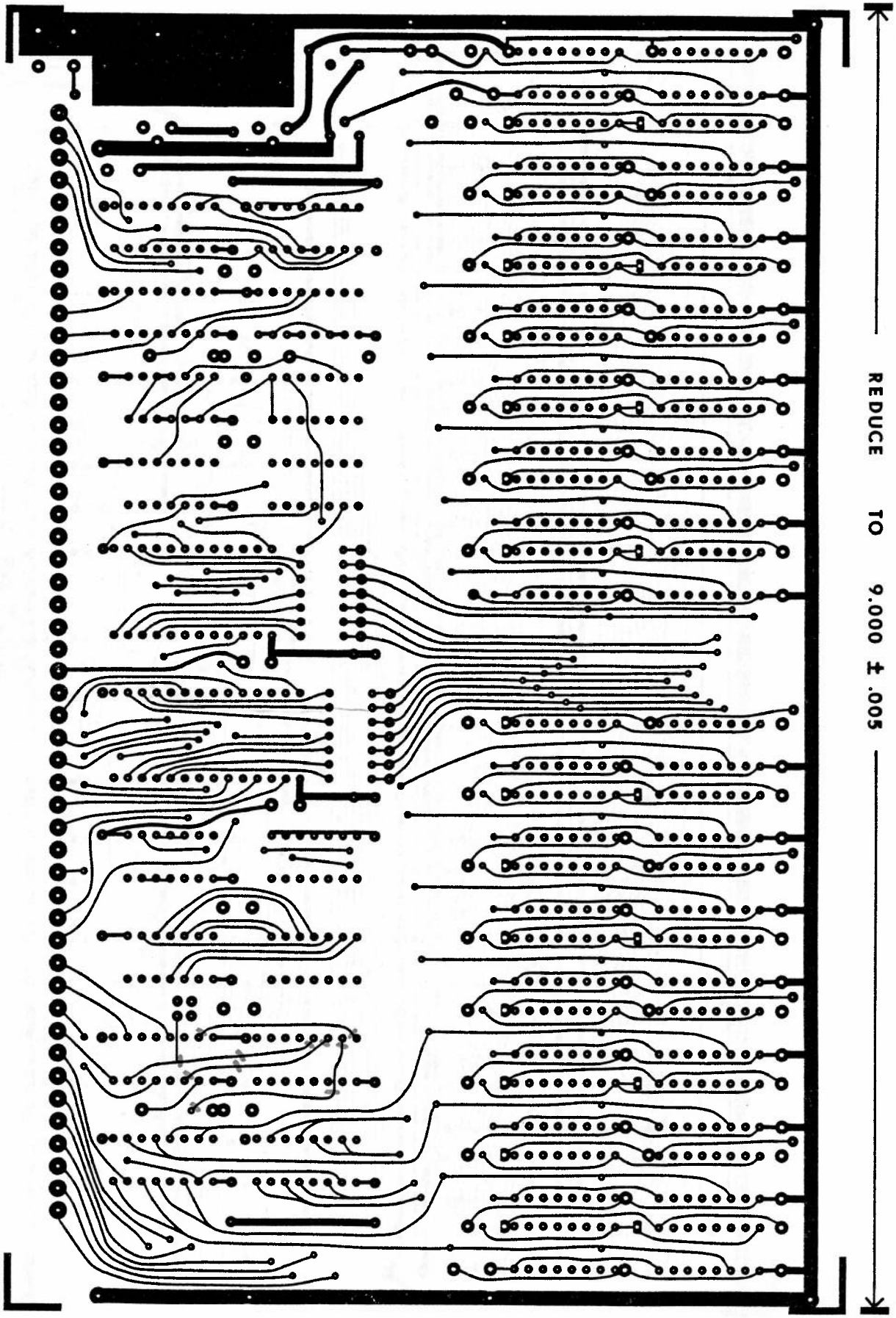
SCALE: None	APPROVED BY:		DRAWN BY:
DATE: 10-15-80		11-25-80	REVISED

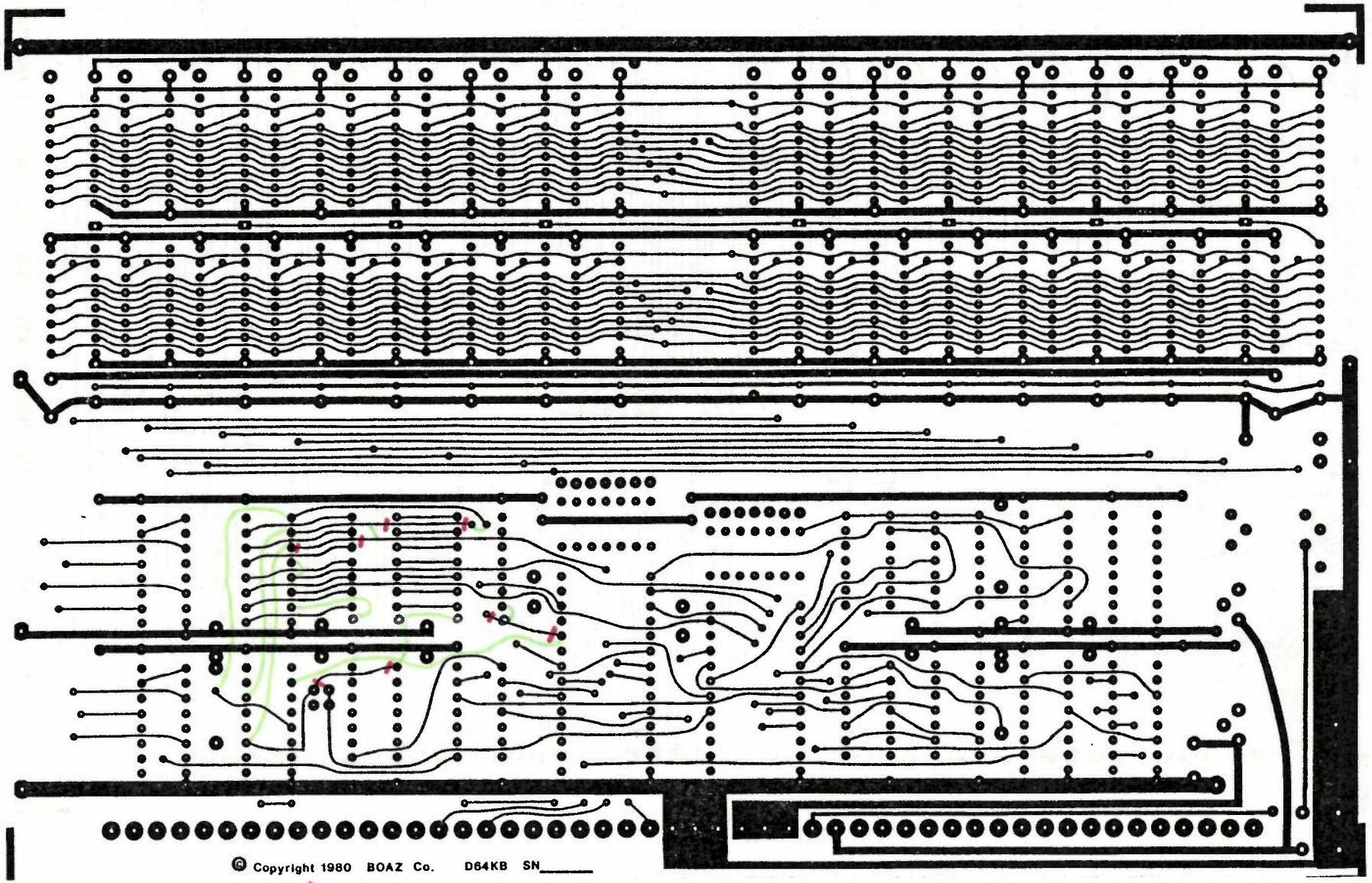
64KB DYNAMIC RAM BOARD SS50/50C

DRAWING NUMBER: LD 1028 1/2

M-3


REDUCE TO 9.000 ± .005
COMP. SIDE

REDUCE TO 9.000 ± .005



RED = CUTS (8)
GREEN = ADDS (11)

MOD'S TO REV 1

M-4

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MODIFICATION OF THE D64KB TO USE 65K BIT MEMORY CHIPS

The D64KB may be extended to use the new 65K by 1 bit dynamic memory chips very easily. While these chips are quite expensive currently, the price will soon be dropping to the point where you may want to have a 256K Byte memory board in place of the 65K Bytes on the D64KB. Of course extended addressing MUST be used to access more than one of the 65K Byte blocks on the board. This also requires the modification to Rev. 1 or a Rev. 1 level D64KB.

The instructions below, along with the PC artwork, shows how to make the D64KB into a 256K Byte Dynamic Memory Board.

DO NOT INSTALL THESE COMPONENTS (OR REMOVE THEM):

Capacitors: 2,4,6,8,10,12,14,16,17,19,21,23,25
27,29,31,33,49,60,61,62

Diode: CR1

Voltage Regulators: VR+12, VR-5, VR+5

DO THE FOLLOWING:

Modify (if needed) D64KB to Rev. 1 level.

Jumper the output pin (O) of VR+5L to the output pin (O) of VR+12 (which is not installed).

Cut these traces on the bottom side of the board:

U59-10
U59-13
U55-17
U55-18

Add jumpers (see artwork and logic diagram)

Pad (under U59 which was connected to U59-10) to U55-17

Pad (under U59 which was connected to U59-12) to U55-18

U54-3 to U01-1,2,13 (new chip)

U01-14 to a +5 volt trace

U01-7 to a Ground trace

U51-11 to U01-5 (Address bit 15)

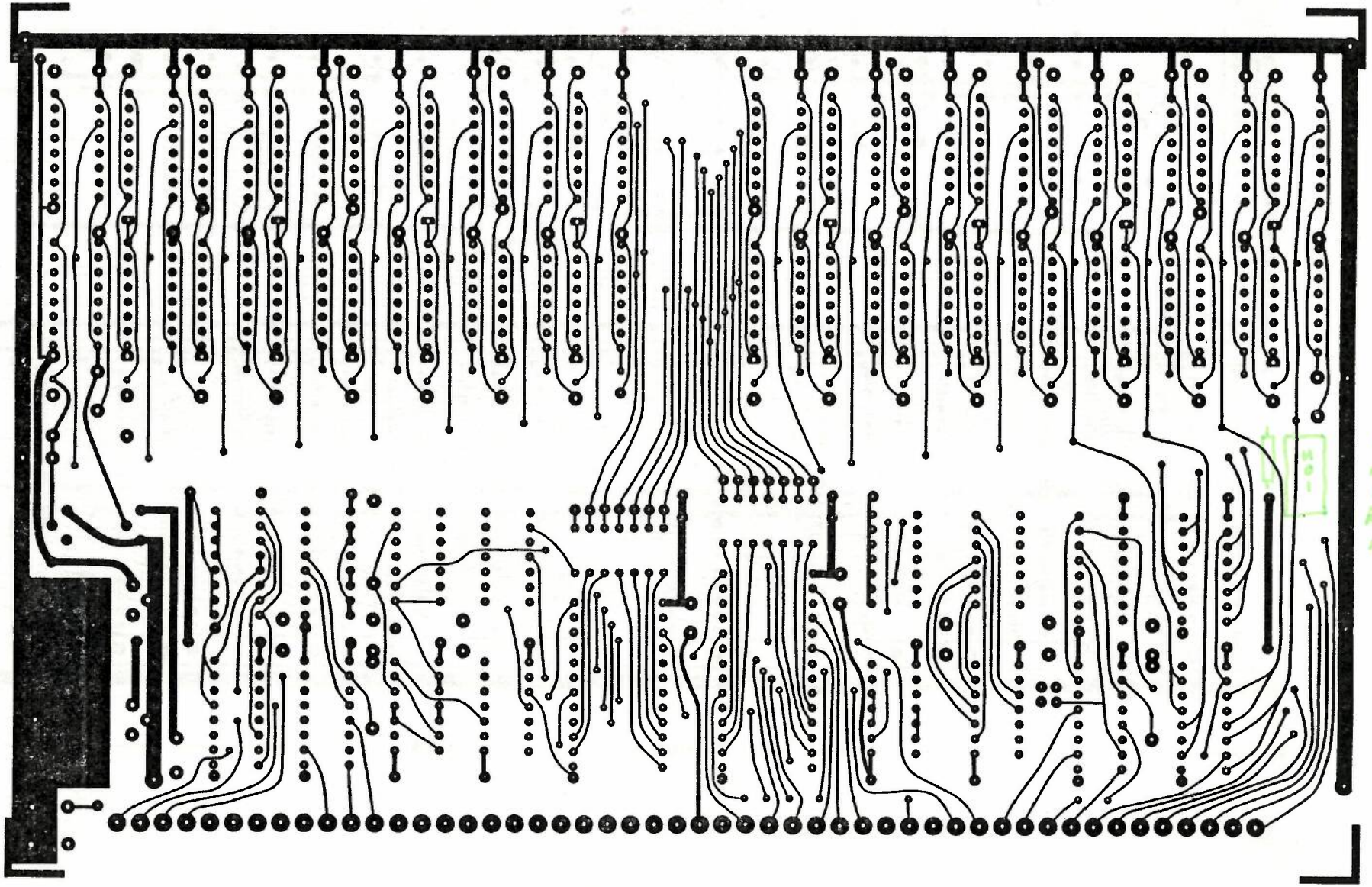
U51-14 to U01-12 (Address bit 14)

Make the connections as shown for U01

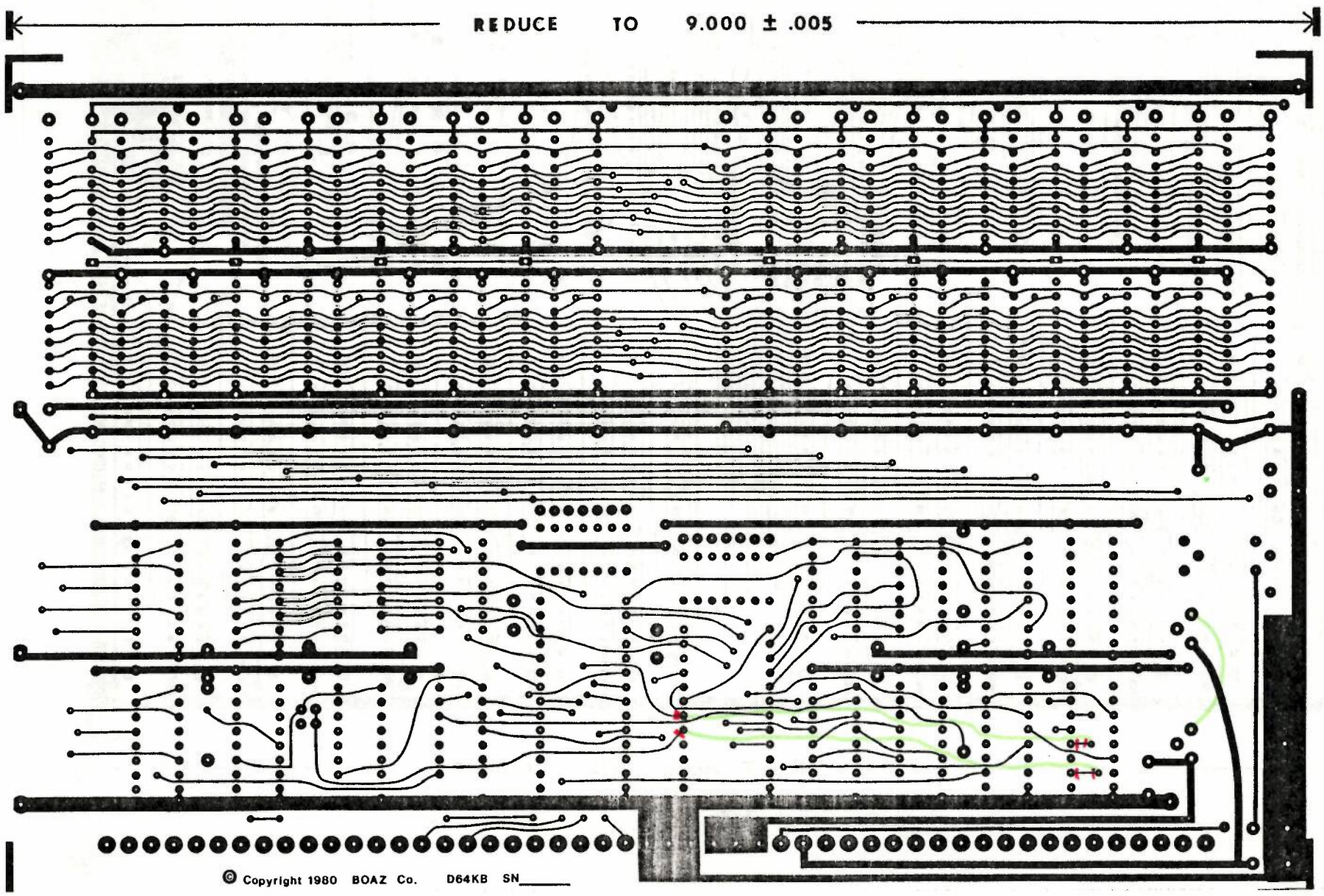
U01-8 to one end of a 10 ohm resistor

Connect the other end of the 10 ohm resistor to U17-9

REDUCE TO 9.000 ± .005



COMP. SIDE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