DA1

D2 UPGRADE MANUAL

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GENERAL INFORMATION

The DA-1 upgrade kit is designed to convert the Motorola Evaluation Kit 2 (MEK6800D2) to a terminal-based microcomputer system. With the addition of external memory, the D2 kit may be used with most popular development software available for M6800 computers.

The two main components of the D2 upgrade kit are the RT/68MX operating system read-only-memory and the serial interface adaptor card. The RT/68 ROM replaces the J2UG monitor supplied with the D2 kit and provides an operating system and I/O facilities to drive a terminal. The interface adaptor card is connected to the user PIA on the D2 kit and contains timing circuits and level translators to interface to terminal at 110-300 baud (10-30 CPS).

This manual is primarily devoted to assembly and installation of the interface circuit and ROM; and other operating features that are specific to the D2 kit. A more complete description of software applications and operating system functions are contained in the RT/68 SYSTEMS MANUAL which is supplied with each DA-1 kit (except when ordered without ROM - board only).

The RT/68 ROM is a most versatile device in terms of the wide number of possible interfaces and options available and the DA-1 is oriented towards a specific configuration that is most straightforward to implement on the D2 kit. It may be desired to implement other features described in the RT/68 manual, which is not directly supported by the DA-1 kit.

If difficulties are encountered in construction and/or installation of the DA-1, you may wish to write or call Microware at (515) 279-9856 for technical information. In addition, comments regarding Microware products and documentation are always welcomed and contribute to our ability to provide better products and service.

This manual was prepared and edited on an M6800 computer system using the RT/68 operating system.

Part Number DA1M

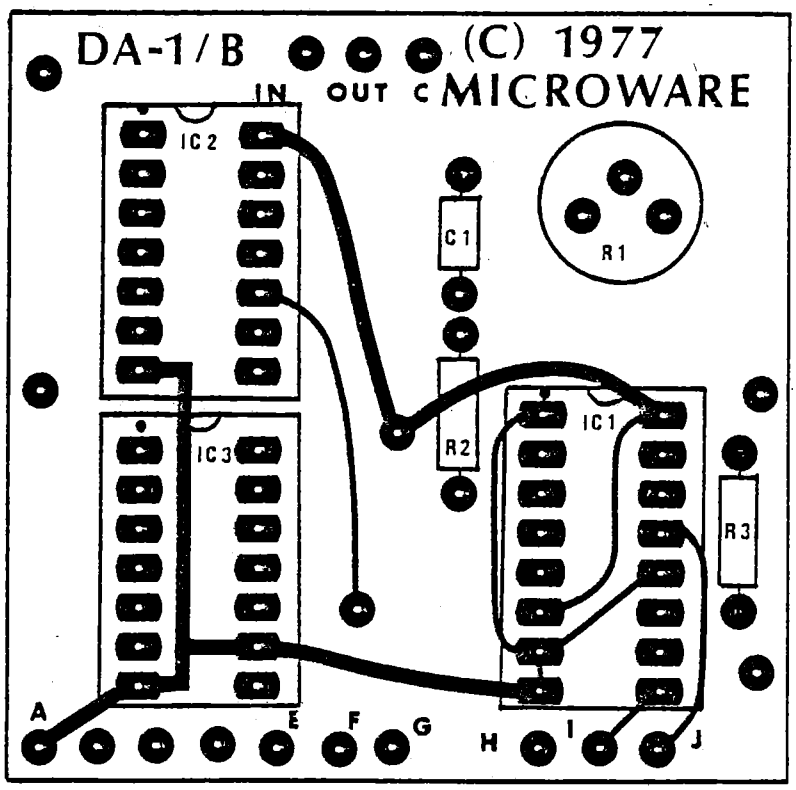
ASSEMBLY INSTRUCTIONS

1. Carefully examine the printed circuit board for broken or shorted foils, etc.

2. All components are installed on the side of the PC board which has the letterins etched.

3. Install the components as per the placement diagram below. Make sure the three integrated circuits are properly oriented so the notched end points toward the top of the board.

4. Inspect for solder bridges, etc.



PARTS LIST

IC1	MC14536 PROGRAMMABLE TIMER
IC2	MC1489 RS232 RECEIVER
IC3	MC1488 RS232 DRIVER
R1	50K 4 TURN TRIMMER RESISTOR
R2	91K 1/4 W RESISTOR
R3	10K 1/4 W RESISTOR
C1	620 pF POLYSTYRENE CAPACITOR

INTERFACE CIRCUIT INSTALLATION

The Rs-232 interface and timing logic is contained on the small circuit board provided. The DA-1 circuit board has holes drilled around the perimeter of the card designed to fit over the D2 kit's wire wrap area adjacent to the user PIA. When oriented correctly the input/output pads are adjacent to the gold edge connector on the top of the D2 board. The adaptor may be secured over the wirewrap area by using pins or stiff wire to suspend it above the circuit board. Care should be taken to prevent shorts from the interface adaptor circuit to the D2 card beneath.

The interface adaptor may be installed elsewhere if required (if the wirewrap area is occupied, etc.). For optimum performance the circuit should be located as close to the PIA as possible.

Before connecting the interface circuit, carefully remove the PIA from its socket to prevent damage during installation of the adaptor. Use the MOS handling procedures recommended in the D2 manual.

The circuit connections pads on the D2 MPU card next to the PIA are small and offset somewhat so careful examination of the correct PIA pin/circuit pad correspondence is important.

Using the table below and the wiring diagram in this manual make the following interconnections between the DA-1 and the PIA (U20).

FROM DA-1 PAD	TO D2 PIA U20
B	PIN 19
E	PIN 2
F	PIN 9
H	PIN 10
I	PIN 12
J	PIN 17

Interconnect the PIA pins as listed below:

FROM PIN	TO
19 (2nd)	15
16	Ground for 1 stop bit (TTY) or + 5 for 2 stop bit (30 CPS-up)
39	abort switch (see text)
40	system clock (see text)
38	system NMI (see text)

Make the following connections between the DA-1 and the system power supply:

FROM DA-1	TO
A	GROUND
C	- 12 V
D	+ 12 V
G	+ 5 V

INTERFACE CIRCUIT INSTALLATION, CONT'D

Three of the connections listed are optional and are used to enable various options of the RT/68 system. If a resistor and switch are connected to PIA input CA1 (pin 40) the ABORT function may be used. The RT/68 real-time clock and task time slicing is enabled by connected a clock signal to input CA2 (pin 39). A 150 Hz signal may be found on the D2 MPU circuit on pin 7 of U17, the cassette timing generator. While slightly fast for some applications, it is usable for the clock signal.

If either option is desired, the interrupt request lines must be modified slightly. The IRQ A and IRQ B outputs of the control PIA (U20 pins 37 and 38) are connected to the system IRQ request line but must be moved to the NMI request line. This line is accessable on the interrupt output pins of the other PIA (U21 pins 37 and 38) so the foil must be cut near U20 and a jumper used to connect to the NMI line.

The number of stop bits transmitted/received by the terminal interface is determined by the jumper on input PB5. Most RS-232 terminals will use 1 stop bit. If the built-in cassette interface is to be used, install the jumper between PB5 and CB2 to allow automatic interface switching under software control. If another type of tape I/O device on the serial data line will be used such as the SWTPC AC-30, jumper PB5 to ground.

The +/- 12 V power supply is used for the RS-232 interface and does not have to be perfectly regulated, so a simple filter circuit may be used in the power supply.

RT/68 ROM INSTALLATION

CAUTION - THE RT/68 ROM IS SENSITIVE TO STRAY STATIC CHARGES THAT MAY DAMAGE OR DESTROY IT IF NOT HANDLED PROPERLY. REFER TO THE RT/68 MANUAL FOR PROPER HANDLING PROCEDURES.

Remove the JBUG ROM (U8) from its socket. The RT/68 ROM is installed in the same socket after the modifications to the circuit board listed below are performed.

The modifications are required because the JBUG ROM has two chip select inputs that are active low while all RT/68 chip selects are active high. Use care in determining the proper place to cut and/or jumper on the D2 circuit board before cutting foils. Use an X-acto knife or similar instrument to cut PC foils and make sure the cut is complete and no copper fragments remain. Use of fine wire (30 AWG wire wrap wire works well) and a fine-tip soldering pencil will result in excellent jumper connections.

The foil on the D2 circuit must be cut in two places to isolate pins 10 and 11 of the ROM. Pin 10 is connected to ground via a wide foil on the top side of the board underneath the socket. Most D2 kit were shipped with sockets that do not cover much of the foil below, and the foil to be cut is accessable if the sockets are of this type. If not, the socket will have to be removed to gain access to this foil. Use great care ! ! ! Solder-absorbing braid sold at most electronic supply stores works well.

Cut the wide foil on the top that runs between U8-pin 1 and U8-pin 10. On the bottom of the board, locate a thin foil that runs from U8-pin 11 around the corner of the IC to a feed-through hole. Cut this foil between the hole and pin 11.

Make the jumper connections listed below. Note that part of an unused 7400 NAND gate (U22) is used to invert one chip select input of the ROM.

FROM	TO
U8-PIN 11	U22-PIN 8
FEEDTHROUGH HOLE FORMERLY CONNECTED TO U8-PIN 11	U22-PIN 9
U22-PIN 10	U22-PIN 14
U8-PIN 10	U8-PIN 12

The RT/68 ROM may now be installed in the socket U8.

TERMINAL CONNECTIONS

The DA-1 will interface to any RS-232 device at 110-300 baud (10-30 CPS). The serial output to the terminal is available at the hole labelled OUT and the serial input is marked IN. The ground is marked COM.

The terminal may require a standard RS-232 connector (such as Cinch DB-25S, not supplied) in which case the DA-1 connects.to the following pins of the plug:

OUT to pin 3
IN to pin 2
COM to pin 1 and 7
Jumper pin 4 to 5
Jumper pin 6 to 20

INTERFACE ALIGNMENT

The DA-1 interface circuit has one trimmer resistor that adjusts the baud rate of the interface. After the interface circuit and RT/68 ROM have been installed the following procedures may be used to set up the interface.

Using an Oscilloscope:

Probe pin 13 of IC1 (timer output). Reset the D2 kit and adjust R1 for a 0 level duration of 3.3 ms. for 30 CPS operation or 9.1 ms. for 10 CPS operation. Turn on the terminal and depress the system reset button. A line feed and "$" prompt should be displayed. If not, fine adjustment of R1 should correct this. When the prompt is printed reliably after each reset, type an "R" on the terminal. The system should respond with a formatted resister dump. If an "ERR 6" message is printed, further adjustment of R1 is required until the system responds to the "R" command properly each time.

Without Instruments:

If a scope is not available to make the initial adjustment of R1, you can slowly rotate R1 while continuously depressing the reset button until the prompt "$" is displayed. Then the fine adjustment of R1 described above can be performed. R1 is a four-turn trimmer so several turns may be required.

SYSTEM OPERATION

After power-up, the RESET switch on the D2 CPU board must be depressed to start the RT/68 program. The RT/68 monitor will print a $ prompt character and is ready to accept a command from the console terminal. Refer to the RT/68 SYSTEMS MANUAL for details of the various functions.

Cassette Tape Input/Output

RT/68 can use the D2 kit's built-in audio cassette interface to read or write Kansas City standard tapes using the Motorola standard data format. As explained in section 8 of the RT/68 manual, the monitor can use either an ACIA or PIA-type interface for I/O. The D2's cassette circuitry is interfaced using an ACIA at address $8008-$8009 (U23). When PB5=0 the PIA (terminal) interface is selected, and when PB5=1 the ACIA (cassette interface) is selected. The control PIA's output CB2 is connected to PB5 to allow the selection to be software-controlled. Additionally, two bytes in the scratch-pad RAM are used to specify the ACIA address, and these must be set to correspond to the address of the cassette interface ACIA.

Loading Programs From Cassettes

RT/68 will assert CB2 during the tape load function, so the interface selection is automatic. The two following steps must be followed after each system reset to initialize the ACIA and the address pointer. This need only be performed after the system is powered up or reset.

1. Reset the computer.
2. Use the M function to set the following memory locations to the values indicated:

```
A012 - 80   (SET ACIA ADDRESS POINTER)
A013 - 08
8008 - 03   (RESET ACIA)
8008 - 10   (SET ACIA CONTROL REGISTER)
```

Note that because the ACIA control resister is not a read/write resister, a "no change" error message will be displayed when address $8008 is altered.

To load memory from cassette, turn the cassette machine to "play" and type "L" to start the RT/68 tape load program. When the tape load is finished, the RT/68 program will print a $ prompt or an error message if a load error occurred. Note that the tape must have an "S9" at the end to stop the load function.

Writing Cassettes From Memory

Unlike the tape load function, the RT/68 tape write routine will not automatically switch CB2 during a tape write. In addition, the D2's cassette interface circuit is set up in such a way that the ACIA control register must be set to a different value to alter the clock divide rate and word length.

Fortunately, the RT/68 tape write routine is written as a subroutine so a very short program may be loaded into the D2's RAM to perform the necessary functions to write a cassette without modification of any hardware. A listing of the program called "PUNCH" is included in this manual.

The program may be moved to any address in memory without reassembly or modification. The first time the program is to be used, it must be loaded into memory using the RT/68 memory examine/change function. It may then be used to write a cassette tape of itself so it may be loaded quickly when needed. If other programs do not overwrite the punch program it may be loaded once when the system is first started.

The PUNCH program is started using the RT/68 "E" execute program function. To write a cassette tape, place a blank cassette in the cassette recorder and manually advance the tape past the leader. Turn the cassette recorder to "record" and enter the following on the terminal:

E,0100,BBBB,EEEE

BBBB is the four hex character beginning address for the tape write and EEEE is the ending address. If the PUNCH program has been relocated, the new starting address of the program must be substituted for "0100". After the desired memory locations have been written on the tape, PUNCH will write an "S9" end-of-file record to terminate the file. If this is not desired (for example, to make a tape of non-continuous memory locations) NOP instructions may be inserted in PUNCH to inhibit writing of the "S9". When the tape write is complete, the terminal will display a $ prompt and the recorder may be turned off.

Automatic Cassette Motor Control

When the system is configured as described in this manual and the tape read/write procedures specified are used, the PIA output CB2 will be at a "1" whenever a tape read or write is in progress. This output can drive up to 1 TTL load and drive a reed relay driver circuit to control tape recorders which have a remote control facility. This will automatically turn the recorder motor on and off when appropriate. A delay loop is included in the tape write routine to allow the motor adequate startup time before data is written on the tape.

ACIA-BASED INTERFACE OPTION

The DA-1 may be used with an ACIA-type interface as the primary I/O device to the console terminal if an ACIA and extra decoding for addresses $8000-$8001 are supplied. The circuitry should be built in the D2's wirewrap area. The user PIA (U20) is still used by RT/68 for jumper-selected options and interrupt inputs.

A schematic of the necessary interconnections and additional address decoding logic is shown in this manual. The number of connections to the D2 main buss is rather extensive and careful attention to location of the various signals on the main circuit board is required.

The schematic shown requires that another ACIA be added to the system, however the address decoding of the cassette interface ACIA may be changed to convert to a terminal interface at the expense of the use of the cassette interface.

Another possibility is the addition of CMOS data selectors to switch the serial input/output and clocks of the ACIA between the DA1 adaptor circuit and the audio cassette interface circuit.

To enable the ACIA input/output option, PIA U20 must have input PB5 tied to +5. Also note that the cassette input/output routines (LOAD and PUNCH) must be called from a short subroutine that initializes the ACIA before the first operation, and sets the ACIA address vector used by RT/68 to the correct value. See section 8 of the RT/68 SYSTEMS MANUAL.

D2 KIT EXPANSION

Motorola sells a line of memory cards that are compatible with the D2 kit including a low cost ($400) 16K RAM system specifically designed for the D2. In addition, the entire line of Motorola Micromodules (TM, Motorola, Inc.) may be used to implement many special and input/output functions.

An application note AN-771, "MEK6800D2 Microcomputer Kit Expansion Techniques" is available from any Motorola sales office and contains much valuable information concerning memory expansion and other useful information.

$A050

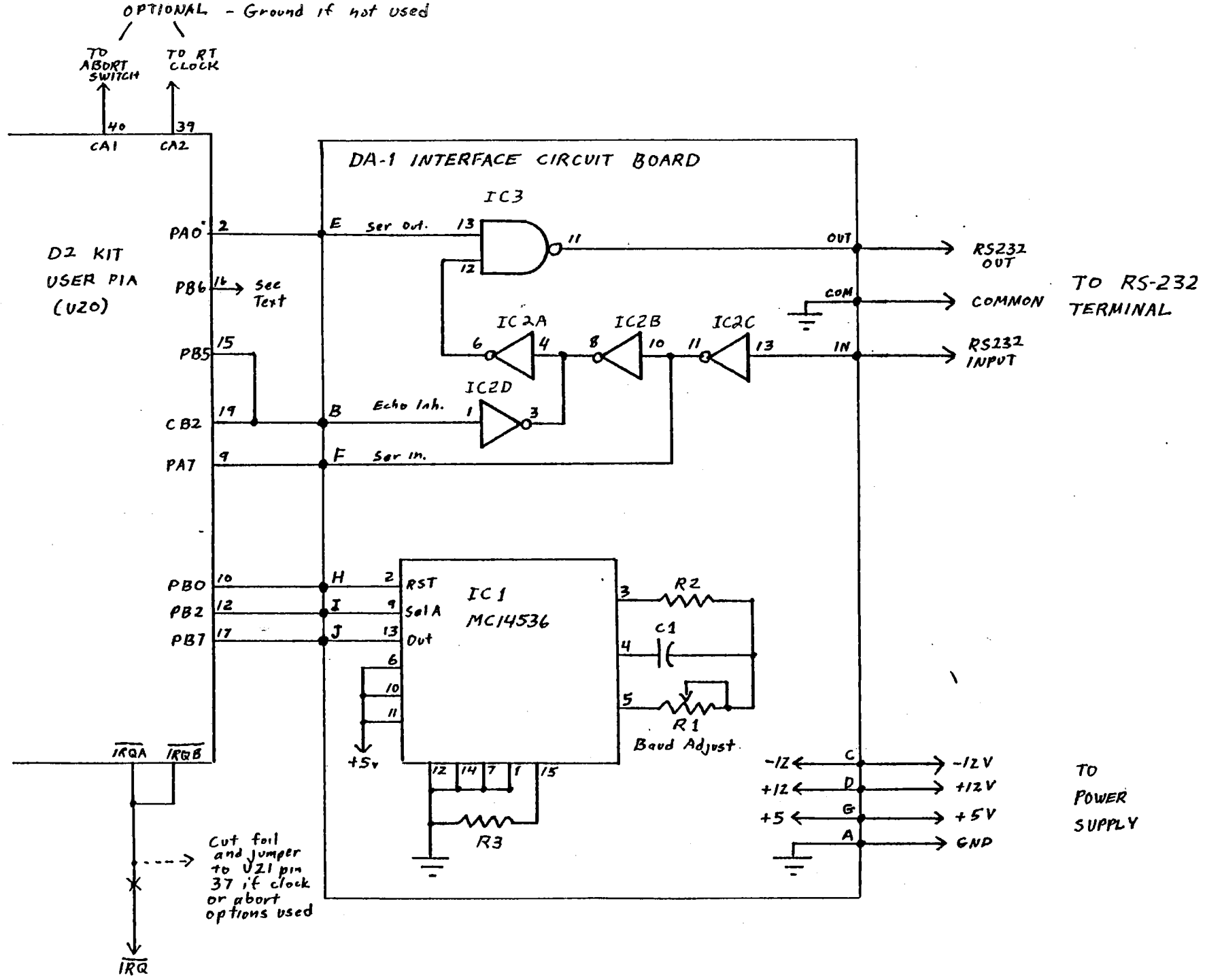
```
00001                    NAM    PUNCH


00003                * PROGRAM TO WRITE A CASSETTE TAPE USING THE D2
00004                * KIT CASSETTE INTERFACE WITH RT/68
00005                *
00006                * TO RUN ENTER:  E,0100,BBBB,CCCC
00007                *
00008                * WHERE BBBB = BEGINNING ADDRESS OF DUMP
00009                *       CCCC = ENDING ADDRESS OF DUMP


00011 0100                    ORG    $0100
00012 0100 BD E1D4 PUNCH      JSR    $E1D4     GET BEG + END ADDR
00013 0103 86 51              LDA A  #$51      ACIA CONTROL BYTE
00014 0105 C6 3C              LDA B  #$3C      PIA CONTROL BYTE
00015 0107 8D 11              BSR    TAPCOM
00016 0109 BD E0EE            JSR    $E0EE     WRITE TAPE
00017 010C 86 53              LDA A  #'S
00018 010E BD E1D1            JSR    $E1D1     WRITE E.O.F
00019 0111 86 39              LDA A  #'9
00020 0113 BD E1D1            JSR    $E1D1
00021 0116 86 10              LDA A  #$10      ACIA OLD CONTROL BYTE
00022 0118 C6 34              LDA B  #$34      PIA RDR OFF BYTE
00023 011A B7 8008 TAPCOM     STA A  $8008     SET ACIA C. R.
00024 011D F7 8007            STA B  $8007     SET PIA C.R
00025 0120 39                 RTS
00026                         END

TOTAL ERRORS 00000
```

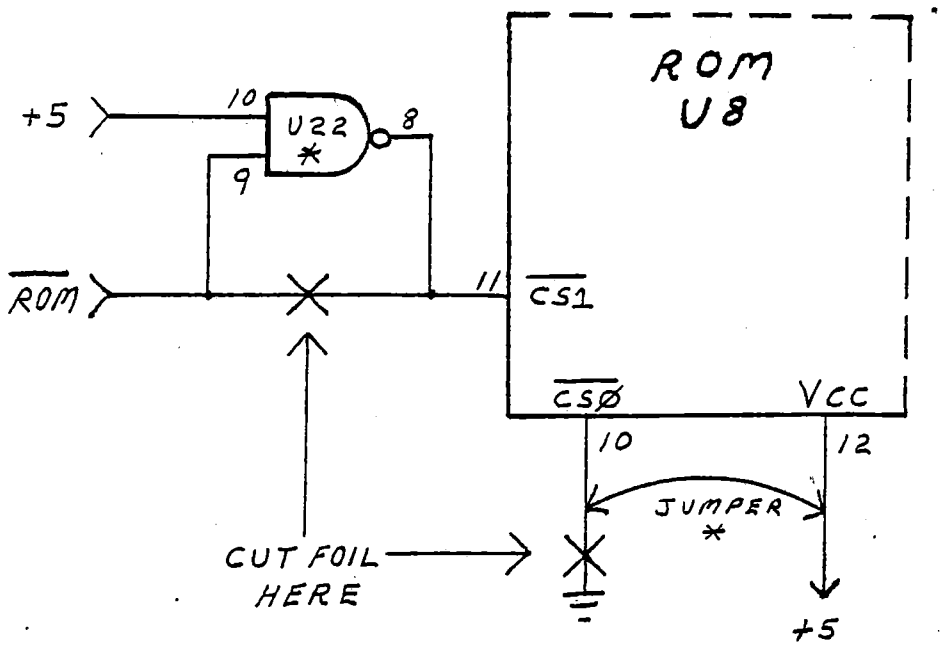
CLA

JSR E1D1

CLA

JSR E1D1


OPTIONAL - Ground if not used
TO ABORT SWITCH
TO RT CLOCK
40
39
CA1
CA2
DA-1 INTERFACE CIRCUIT BOARD
IC3
D2 KIT USER PIA (U20)
PA0
2
E
Ser out.
13
11
OUT
RS232 OUT
PB6
16
See Text
12
COM
COMMON
TO RS-232 TERMINAL
IC2A
IC2B
IC2C
PB5
15
6
4
8
10
11
13
IN
RS232 INPUT
IC2D
CB2
19
B
Echo Inh.
1
3
PA7
9
F
Ser In.
PB0
10
H
2
RST
IC1
MC14536
PB2
12
I
9
Sel A
3
R2
PB7
17
J
13
Out
C1
4
6
10
11
5
R1
Baud Adjust
+5v
12
14
7
1
15
R3
IRQA
IRQB
-12
C
-12V
+12
D
+12V
+5
G
+5V
A
GND
TO POWER SUPPLY
Cut foil and jumper to U21 pin 37 if clock or abort options used
IRQ



* - Additional connections

ROM SELECTION MODIFICATIONS

ADDENDUM TO DA-1 MANUAL - DA1P VERSION

The DA1P version of the D2 upgrade kit is identical to the standard DA-1 kit described in the DA1 Manual except it is supplied with an RT68MXP ROM instead of the RT68MX.

Because the RT68MXP has different electrical connections only, all information in the DA-1 Manual that relates to software and interface circuit installation also applies to the DA-1P. Only the ROM installation procedures described on the page titled "RT/68 ROM Installation" is different and the installation procedures described in the attached sheet are to be substituted.

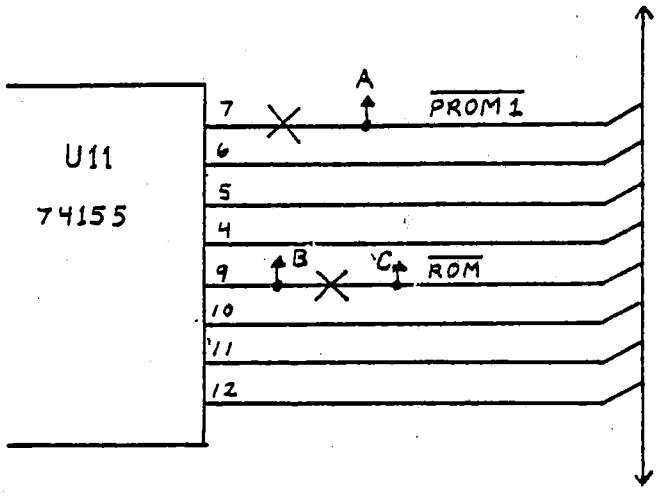
Note that the DA-1P may be installed as either an RT/68-only configuration OR a dual-monitor configuration if a switch and two resistors are added.

When a dual monitor coniguration is used, the monitor switch may not be changed during execution of a program. When monitor modes are changed from RT/68 to JBUG or vica versa, the RESET switch must be depressed to start up the monitor. A dual monitor configuration is mutually exclusive, i.e., only one monitor can be used at a time and usually programs that call subroutines in one monitor will not work if run with the other monitor active.

RT/68 does not use the D2 keyboard or LED display but programs may be written for RT/68 that use them because RT/68 does not require them to be disconnected or modified.

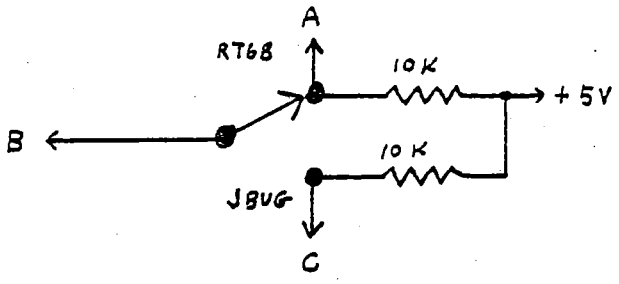
Also note that the cassette tape format used by each monitor is different and tape created by one may not be loaded by the other. To convert tape formats, load the tape program into memory using the monitor that created it, then switch to the other monitor and use its punch function to write it on a new tape.

RT68MXP ROM INSTALLATION (DA-1P)



partial schematic of D2 kit MPU card

The diagram above shows where the foil on the CPU card must be cut (marked X). Three points: A, B and C are where wires are to be connected depending on how the kit is to be configured. For RT68-only operation, simply install a short jumper from point B to point A. The switch circuit shown below is used to create a dual-monitor system. The switch position determines whether JBUG or RT68 is to be used as the operating system.



switch = SPDT
resistors = 10K 1/4W

This circuit functions by switching the $\overline{ROM}$ signal to either ROM chip enable input. The ROM not selected is disabled.

The RT68MXP ROM must be installed in the socket PROM 1 (U12) which is now addressed form $E000 to $FFFF. If you have not previously installed optional components R5, CR1, C26 and C27 they must be installed, and a +12 volt and -12 volt power supply connection to the D2 buss connector added. The jumpers to enable the 2708 ROM must also be installed:

E1 to E2 E3 to E8 E4 to E6 E5 to E9

These connections are shown in the D2 kit manual on page A3-3 and listed in note 3 of the schematic. Though Motorola suggests that 10K resistors be added from +5v to CS1 and AØ - A9 our experience has been that these are not required, particularly if the optional buss drivers have been added to the kit.

RT68MXP OPERATING SYSTEM ROM - SUPPLEMENT TO RT68 MANUAL

THE RT68MXP IS IDENTICAL TO THE STANDARD RT68MX ROM EXCEPT IT IS PROVIDED ON ROM WITH 2708-TYPE ELECTRICAL CHARACTERISTICS AND PIN CONNECTIONS. THIS IS USEFUL FOR SYSTEMS THAT ARE DESIGNED FOR OR HAVE PROVISIONS FOR 2708-TYPE EPROMS.

NOTE - THOUGH THE RT68MXP IS FUNCTIONALLY IDENTICAL TO A 2708 EPROM, IT DOES NOT HAVE A WINDOW FOR ERASURE AND THE PROGRAM SUPPLIED CANNOT BE MODIFIED.

ALL INFORMATION CONCERNING OPERATION AND SOFTWARE FOR RT68MX IS APPLICABLE TO RT68MXP EXCEPT FOR INSTALLATION PROCEDURES, WHICH ARE DEPENDENT ON THE SYSTEM TO BE USED.

FOR MSI 6800 SYSTEMS: RT68MXP MAY BE USED TO REPLACE THE MONITOR SUPPLIED IF:

1) THE SCRATCHPAD RAM AND I/O PORT ADDRESSES ARE JUMPERED TO THE RT68 STANDARD ADDRESS ASSIGNMENT.
2) THE HIGHER ADDRESS PROM IS MODIFIED OR REPLACED SO THE RESTART, IRQ, NMI, AND SWI VECTORS JUMP INTO THE RT68 ROM AS SHOWN IN THE PROGRAM LISTING.

FOR MOTOROLA MEK6800D2 SYSTEMS: RT68MXP MAY BE INSTALLED AS A REPLACEMENT FOR JBUG OR USED TO IMPLEMENT A SWITCH-SELECTABLE, DUAL MONITOR SYSTEM WHERE JBUG OR RT68 MAY BE SELECTED TO BE USED AS THE SYSTEM MONITOR.

IT IS SUGGESTED THAT THE MICROWARE "DA-1 UPGRADE KIT" BE INSTALLED TO PROVIDE THE NECESSARY INTERFACE FOR THE TERMINAL. THE DA-1 MANUAL AND SPECIAL APPLICATION NOTE FOR RT68MXP ARE AVAILABLE AND DESCRIBE SOFTWARE AND HARDWARE TECHNIQUES FOR THIS APPLICATION.

ELECTRICAL INFORMATION : THE RT68MXP REQUIRES THE USUAL 2708 SUPPLY VOLTAGES +5V, +12V AND -5V. DATA INPUTS AND OUTPUTS ARE ALSO THE SAME.

PIN CONFIGURATION