LMB-1A MOTHERBOARD

INTRODUCTION

The Smoke Signal Broadcasting (SSB) Motherboard (LMB-1A) provides the capabilities for interfacing a wide variety of SS-50 bus products: 16K/32K STATIC MEMORY BOARDS, FLOPPY DISK CONTROLLERS, INTELLIGENT VIDEO DISPLAYS, COLOR GRAPHICS, CPU, INPUT/OUTPUT DEVICES, etc. The LMB-1A provides for interfacing nine fifty-pin boards and eight thirty-pin I/O boards.

PRINTED CIRCUIT LAYOUT

The LMB-1A layout is designed to incorporate the SS-50C bus features. The I/O decoder includes address decoding for the extended address bus (A16-A19) which is jumper selectable by W1-8. The I/O slot decoding for the SS-50 bus is setup to provide 4 bytes per I/O slot with address lines A0 and A1 connected to each slot. The SS-50C bus provides for 16 bytes per I/O slot via two additional address lines A2 and A3. Selecting between 4 bytes per slot and 16 bytes per slot may be made by cutting and jumpering the wire jumper block W2. The jumper block is layed out so that by installing wire jumpers on a 16 pin dip header plug with all odd pins jumpered, the user may remove and rotate the dip header block 180 degrees to configure for 4/16 bytes per slot. (refer to the OPTIONS section for further details).

All control lines (VMA, E, R/W, NMI, IRQ, FIRQ, RESET, HALT, BS, BA) are connected by the pullup resistor networks Z1, 2 and 5 to +5Vdc. The DATA bus is terminated by the pulldown resistor network Z4 to ground and buffered and inverted by IC U6 (DP8303).

BAUD RATES

The LMB-1A also has a buffered baud rate generator U8 that supplies five separate baud rates to the thirty-pin I/O slots. The outputs of the BAUD rate generator are connected to five inverter/buffers (IC U7 74LS04) by wire jumpers W4-1,2,3,4 and 5 with four additional BAUD rates available at W4-6,7. The BUAD rate generator, as supplied, generates times-64 clock pulses. The wire jumpers W5-1 and 2 allow the selection of times-1,8,16 or 64 clock pulses.

OUTPUT CLOCK RATES

W5-2	W5-1	RATE
0	0	X1
0	1	X8
1	0	X16
1	1	X64

"0" => wire jumper installed
"1" => wire jumper removed

I/O ADDRESS ASSIGNMENTS

The I/O address is decoded by IC's U1, 2, 4 and 5 (74136). These IC's are open collector Exclusive-Or-Gates meaning that when all outputs of the gates are high, an I/O slot is selected. The memory address assignment of the I/O slots can be changed to any desired location by reprogramming the wire jumpers W1-1 through 7 and W3-1 through 8, the present address assignment of the LMB-1A is set for $F7E0 to F7FF with I/O slot 0 occupying memory locations $F7E0 to $F7E3 and I/O slot 7 occupying memory locations $F7FC to $F7FF. The One-Of-Eight decoder U3 (74LS138) selects one of the eight I/O slots according to the address lines A2-4 if the LMB-1A is configured to select I/O slots on a 4 byte boundary, if the LMB-1A is configured to select I/O slots on a 16 byte boundary, address lines A4, 5 and 6 control the One-Of-Eight decoder.

OPTION SELECTION

The LMB-1A contains a number of optional features the user may select.

Wire jumpers W1-1 to 7 and W3-1 to 8

These jumpers control the address decoders of the LMB-1A. With the jumper installed, the corresponding address must be at a logic 1 (active high state) for the I/O section to be selected. With the jumper removed, the corresponding address line mustt be at a logic 0 for the I/O section to be selected.

Wire jumper W1-8

Wire jumper W1-8 controls the extended address decoding section. With jumper W1-8 removed the I/O decoding is accomplished with the lower address lines (Address A5 to A15). With jumper W1-8 installed, the address decoding for the I/O slots is controlled by Address lines A5 to A19.

Wire jumpers W2-1 to 8

Wire jumper W2 is a special jumper block. It has been layed out so that the user may install a 16 pin dip header plug to control the size of the I/O slots from 4 bytes per slot to 16 bytes per slot along with increasing the I/O map from $F7E0 to $F7FF for the 4 bytes per slot to $F780 to $F7FF for the 16 bytes per slot. If a dip header plug is used, jumpering pins 1 to 16, 3 to 14, 5 to 12 and 7 to 10 will allow the user to install the header plug, such that, pin 1 of the plug is aligned with pin 1 of the socket. This selects the 4 byte per slot. Removing and rotating the header plug 180 degress so the pin 1 of the plug is aligned with pin 9 of the socket selects the 16 bytes per slot.

Wire jumpers W4-1 to 7

Wire jumper block W4 allows the user to reconfigure the BAUD rates to the I/O slots from one of nine available rates.

Wire jumpers W5-1 and 2

Wire jumpers W5-1 and 2 provide the user to select from 1 of 4 available output rate for the BAUD rate generator.

Wire jumpers W5-3 and 4

Wire jumpers W5-3 and 4 redirects the RESET function from being generated on the CPU cards and directed out on the bus to being generated on the LMB-1A and directed to all cards. SSB has designed its cpu cards (SCB-68 and SCB-69) with wire jumpers to allow the reset signal to be directed onto the cpu card from the bus (refer to the appropriate cpu documentation for further details). By removing the jumper from W5-3 and installing a jumper in W5-4, the reset signal can be generated by the One-Shot IC U11 (74LS221).

NOTICE: The capacitor C7 (.1 uf) has been omitted from the LMB-1A assembly due to the effect on the 6809's MEMORY-READY signal. Install C7 only if generating the RESET signal from this circuitry on the motherboard.

Wire jumper W5-6

Wire jumper W5-6 allows the user to supply an optional ABORT function to the LMB-1A. This signal is directed to the Non-Maskable-Interrupt (NMI) line on the cpu.

Wire jumper W5-7 and 8

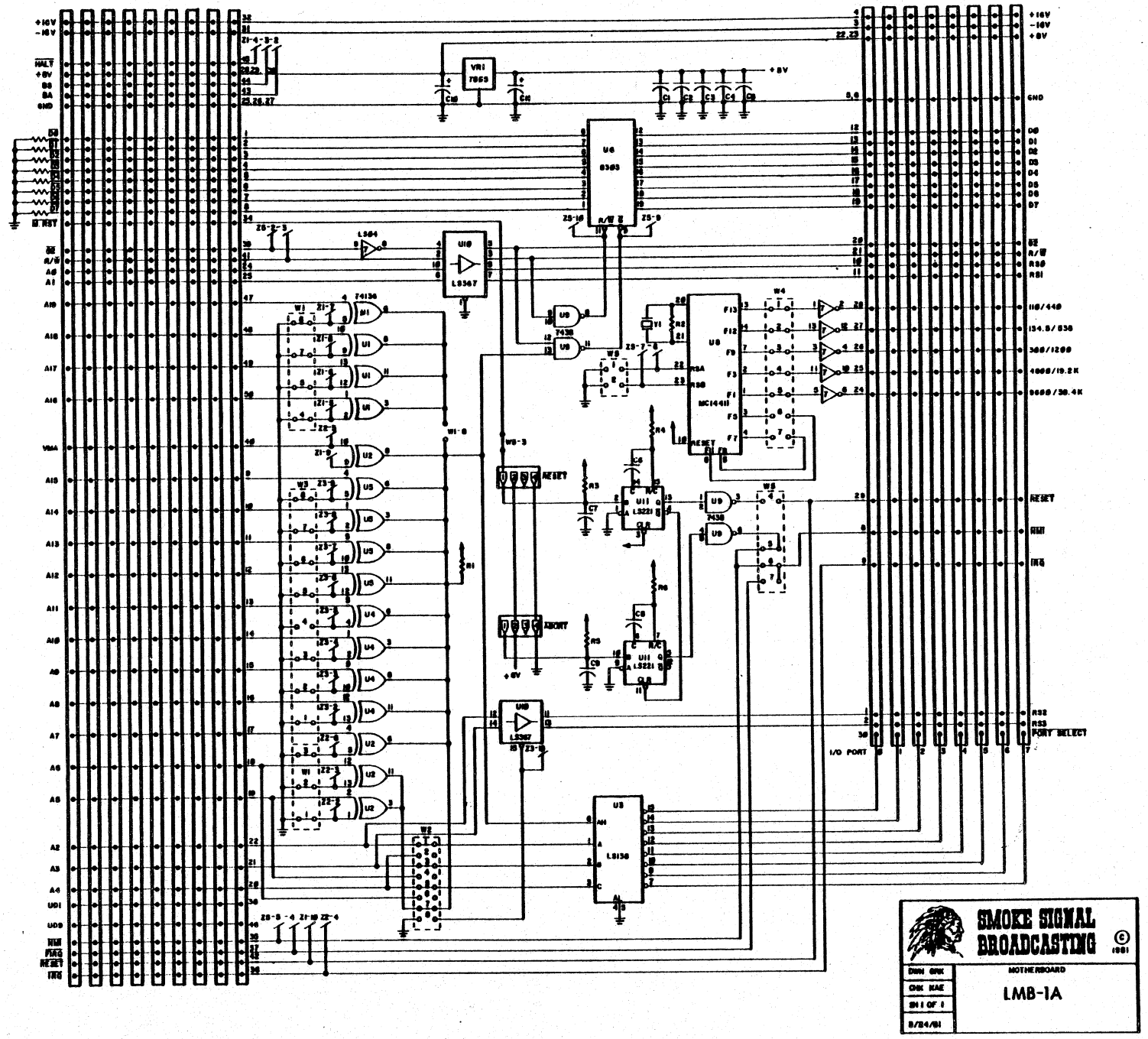
Wire jumpers W5-7 and 8 allow the user to modify the I/O slots to access the Fast-Interrupt-Request signal on the main fifty-pin bus.

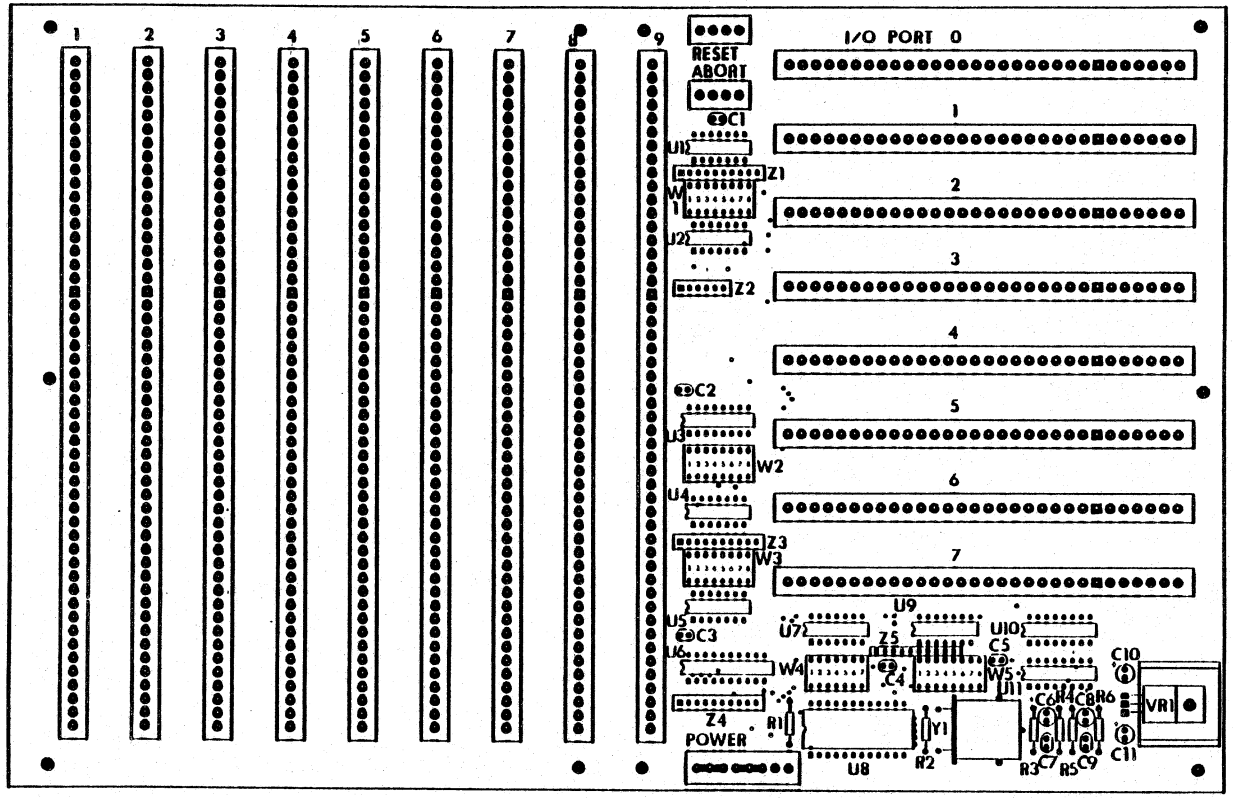
POWER

The LMB-1A Motherboard uses the +8V and +/- 16V unregulated voltages supplied by the power supply. A 7805 +5V regulator VR1 supplies the +5V for Vcc. The +8V and +/-16V are fed directly to the +8V and +/-16V pins on all fifty-pin and thirty-pin slots.

PARTS LIST

U1	74136	QUAD EXCLUSIVE OR GATE
U2	74136	QUAD EXCLUSIVE OR GATE
U3	74LS138	ONE OF EIGHT DECODER
U4	74136	QUAD EXCLUSIVE OR GATE
U5	74136	QUAD EXCLUSIVE OR GATE
U6	DP8303	BI-DIRECTIONAL OCTAL DATA BUFFER
U7	74LS04	HEX INVERTER
U8	14411	BAUD RATE GENERATOR
U9	7438	QUAD OPEN COLLECTOR NAND GATE
U10	74LS367	HEX TRI-STATE INVERTER BUFFER
U11	74LS221	DUAL ONE-SHOOT
VR1	7805	+5V REGULATOR
C1	.1uf	CAPACITOR
C2	.1uf	CAPACITOR
C3	.1uf	CAPACITOR
C4	.1uf	CAPACITOR
C5	.1uf	CAPACITOR
C6	10uf	CAPACITOR
C7	.1 uf	CAPACITOR (NOT INSTALLED)
C8	1 uf	CAPACITOR
C9	.1 uf	CAPACITOR
C10	10uf	CAPACITOR
C11	10uf	CAPACITOR
R1	270	RESISTOR
R2	1M	RESISTOR
R3	470K	RESISTOR
R4	10K	RESISTOR
R5	470K	RESISTOR
R6	10K	RESISTOR
Y1	1.8432MHz	CRYSTAL
Z1	1K	10 PIN RESISTOR NETWORK
Z2	1K	6 PIN RESISTOR NETWORK
Z3	1K	10 PIN RESISTOR NETWORK
Z4	1K	10 PIN RESISTOR NETWORK
Z5	1K	10 PIN RESISTOR NETWORK


SMOKE SIGNAL BROADCASTING
©
1981
MOTHERBOARD
LMB-1A
DWN BRK
CHK KAE
SH 1 OF 1
8/24/81



SMOKE SIGNAL BROADCASTING

© 1979

DWN BY: ARTMASTER DESIGN SERVICES	TITLE: MOTHER BOARD		
APPD BY: G A E			
DATE: 2/27/81	SHEET 1 of 1	DWG NO: SMB-1A	REV 1