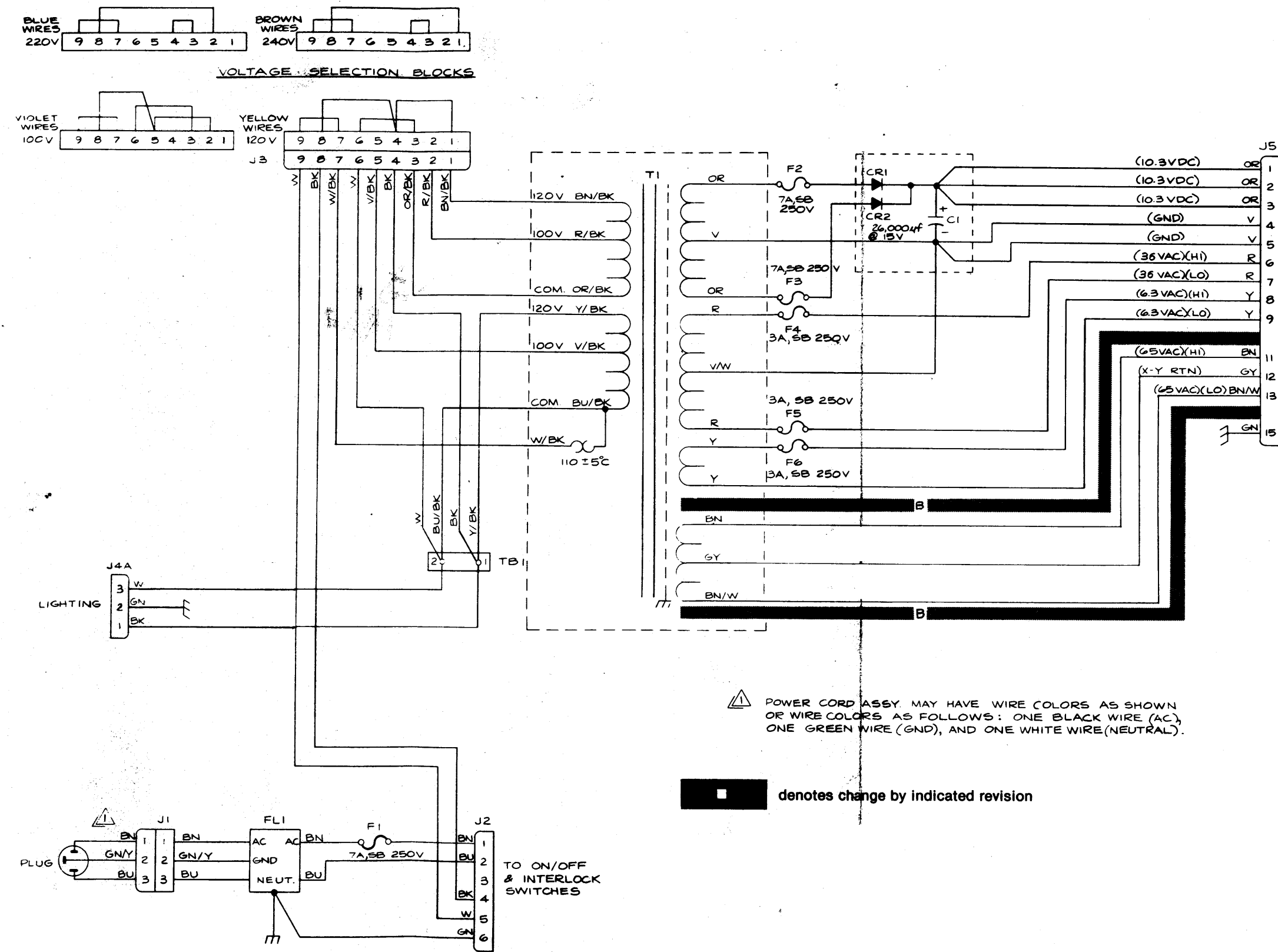


VIDEO POWER SUPPLY WIRING DIAGRAM (034633-01 B)



REGULATOR/AUDIO PCB SCHEMATIC (034485-01 G)

Regulator/Audio PCB 034485-01 G

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and -SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

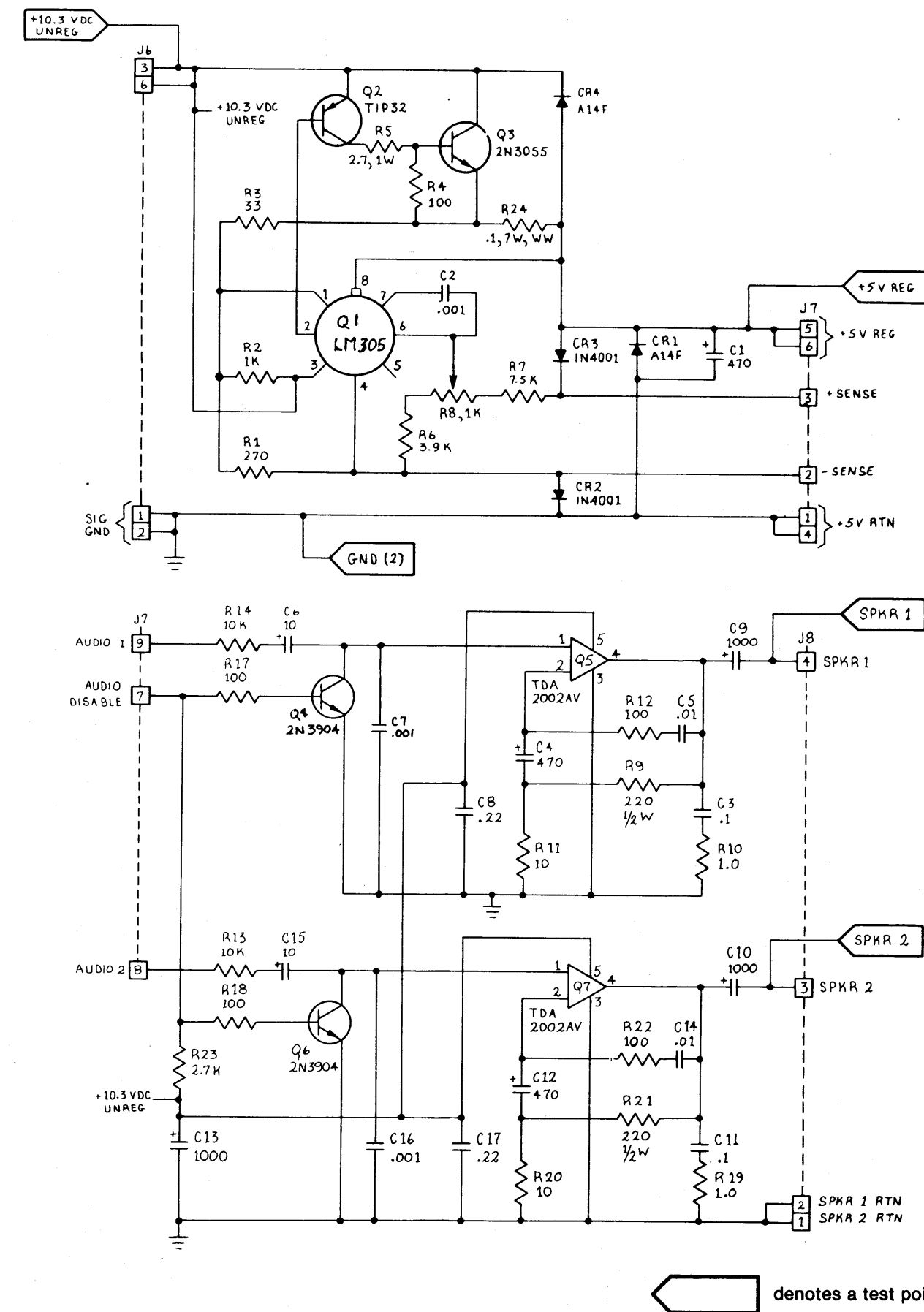
Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 V REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten. In Asteroids, the AUDIO DISABLE input to the PCB is permanently grounded. Therefore, this audio circuit is always on, even while the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, including more information about its operation.



Drawing Package Supplement

to

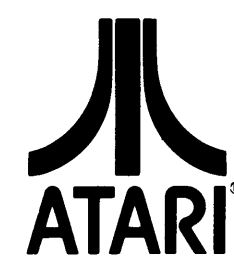
ASTEROIDS

Operation, Maintenance, and Service Manual

Contents of this Drawing Package

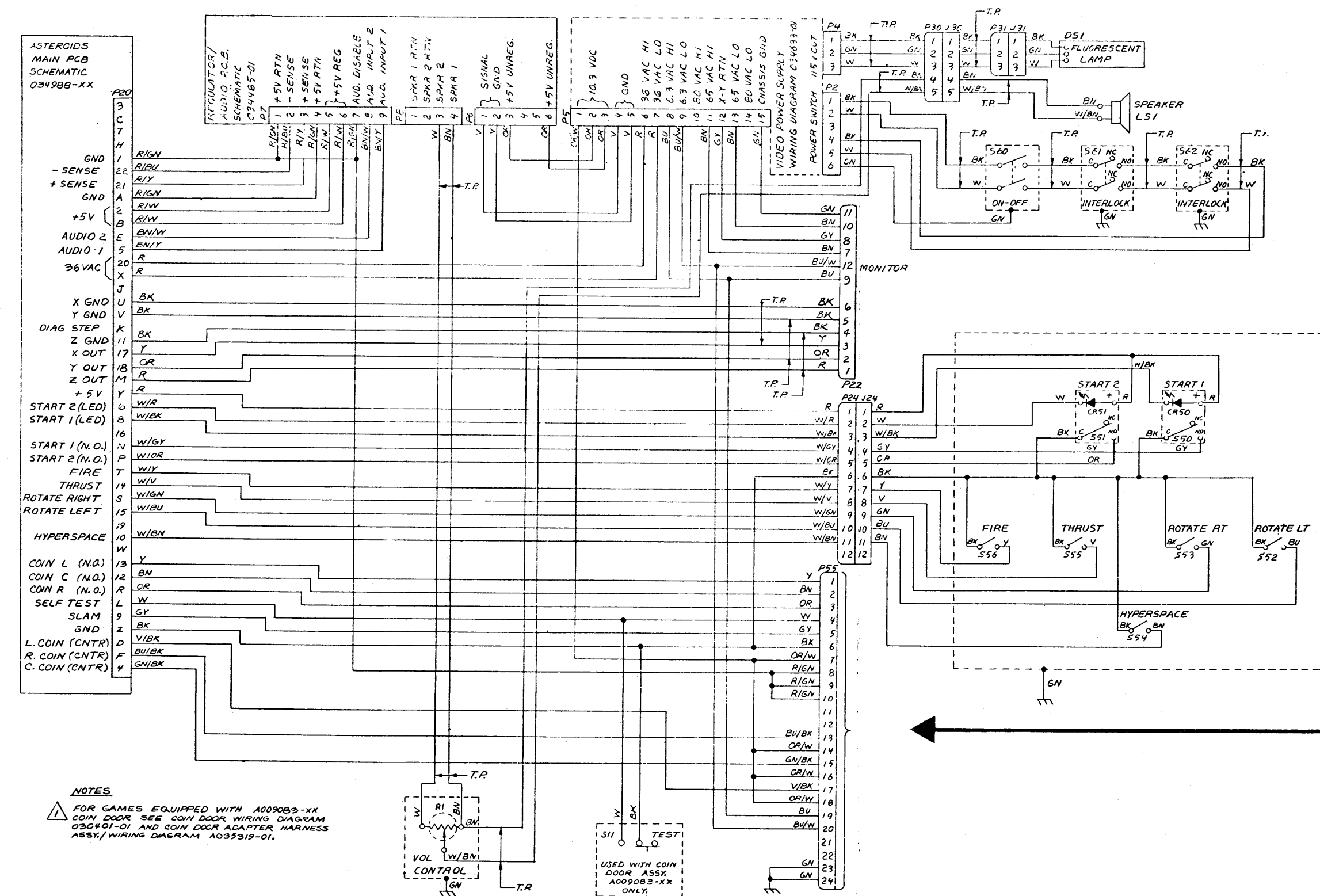
- Game Wiring Diagram, Coin Door and Power Supply
- Microprocessor
- Video Generator
- Switch Inputs, Coin Counter, LED and Audio Outputs

- Sheet 1, Side A
- Sheet 1, Side B
- Sheet 2, Side A
- Sheet 2, Side B

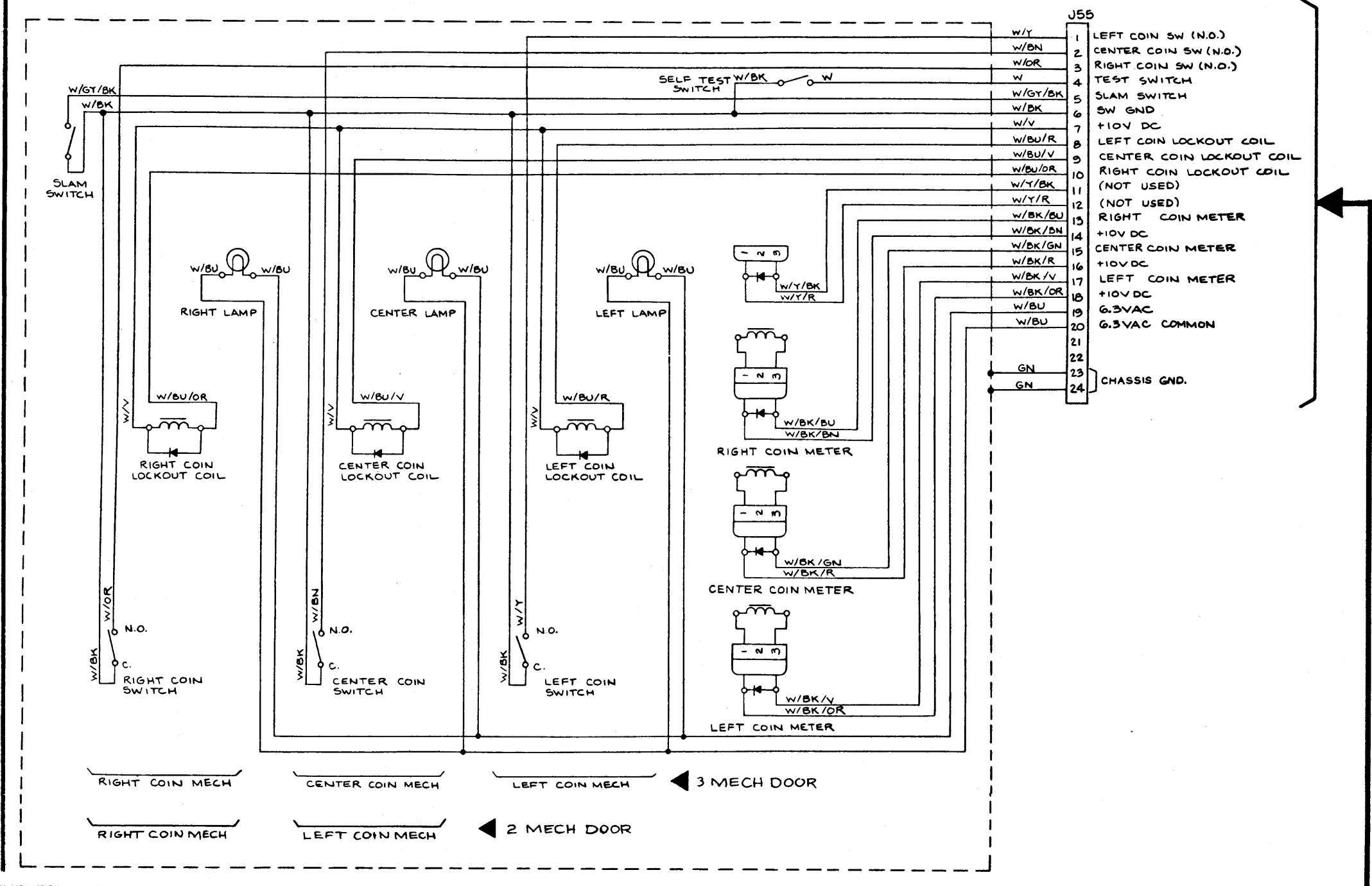


A Warner Communications Company

ASTEROIDS WIRING DIAGRAM (035156-02 A)



COIN DOOR SCHEMATIC (034988-01 A)



CLOCK CIRCUIT

The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Asteroids game.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C25 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding RESET input to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D5 will count up to the RESET state and cause the MPU to return to its initialization routine.

■ denotes change by indicated revision
○ denotes a test point

NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE 8002A. THE 8002'S MAXIMUM FREQUENCY IS 1 MHZ AND IS NOT COMPATIBLE WITH THIS GAME.

MPU CIRCUITRY

NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES.

NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

NOTE:
EITHER A 74LS246 OR AN AM9304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESIS ARE FOR 74LS246. PIN NUMBERS IN PARENTHESIS ARE FOR AN AM9304B.

ADDRESS DECODING CIRCUITRY

The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

HEXADECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
000001FF	0	0	0	0	0	0	0	1	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	ZERO & ONE PAGE RAM
000002FF	0	0	0	0	0	0	0	1	0	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	PLAYER 1 RAM
000003FF	0	0	0	0	0	0	0	1	0	0	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	PLAYER 2 RAM
2001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	3 KHZ
2002	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	HALT
2003	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	HYPERSPACE SW
2004	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	FIRE SW
2005	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	DIAG SW
2006	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	SLAM SW
2007	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	SELF TEST SW
2400	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	RIGHT COIN SW
2401	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	LEFT COIN SW
2402	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	THURST SW
2403	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	1 PLYR START SW
2404	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	2 PLYR START SW
2405	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	ROT SW
2406	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	ROT RIGHT SW
2407	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	ROT LEFT SW
2800	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	OPT SW (SW1, SW7)
2801	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	OPT SW (SW6, SW5)
2802	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	OPT SW (SW4, SW3)
2803	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	OPT SW (SW2, SW1)
3000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	DMAGO
3200	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	2 PLYR START LAMP
3201	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	1 PLYR START LAMP
3202	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	RAMEL
3203	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	COIN CNTRL LEFT
3204	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	COIN CNTRL CENTER
3205	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	COIN CNTRL RIGHT
3400	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	WDOG
3600	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	EXPLOSION PITCH
3601	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	EXPLOSION VOLUME
3602	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	TRUMP VOLUME
3603	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	TRUMP FREQUENCY
3C00	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	SAUCER SOUND
3C01	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	SAUCER FIRE SOUND
3C02	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	SAUCER SOUND SELECT
3C03	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	SHIP THRUST SOUND
3C04	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	SHIP FIRE SOUND
3C05	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	LIFE SOUND
3E00	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	D	NOISE RESET
4000-47FF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	VECTOR RAM
5000-57FF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	VECTOR ROM
6000-7FFF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	PROGRAM

POWER INPUT

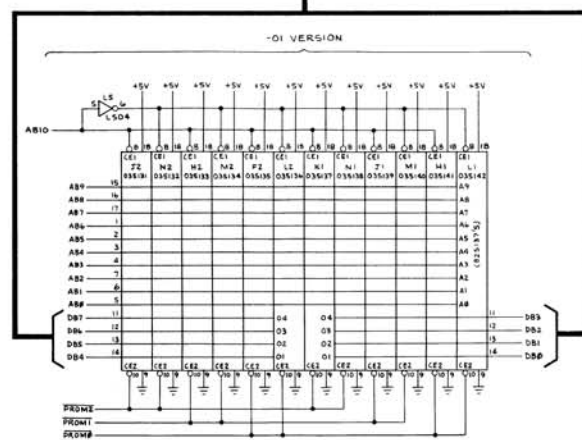
This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

FROM SWITCH INPUTS SHEET 2, SIDE B

ROM/PROM CIRCUITRY

Program Memory for the Asteroids game is contained in PROMs for the -01 version of the PCB and ROMs for the -02 version of the PCB. One ROM is equivalent to four PROMs. All PROMs connected to a common enable must be removed before replacing with a ROM. For example, remove PROMs at locations F2, H1, L2 and L1 before replacing with ROM at location F1.



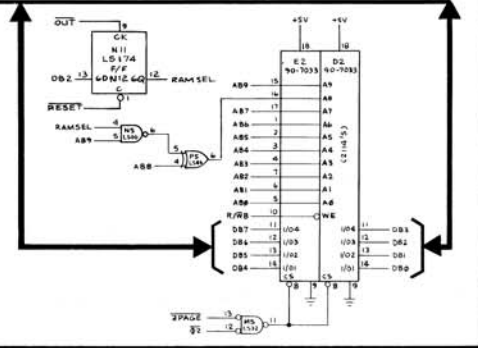
NOTE:
All reference designations in red are for the -05 and -06 PCB assemblies only. For example, the 8316E ROM above is at location F1 on the -01 thru -04 PCB, but is at location J2 on a -05 and -06 PCB.

The reference designations, used in the circuit descriptions, refer to the -01 thru -04 PCB assemblies only.

RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.

The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.

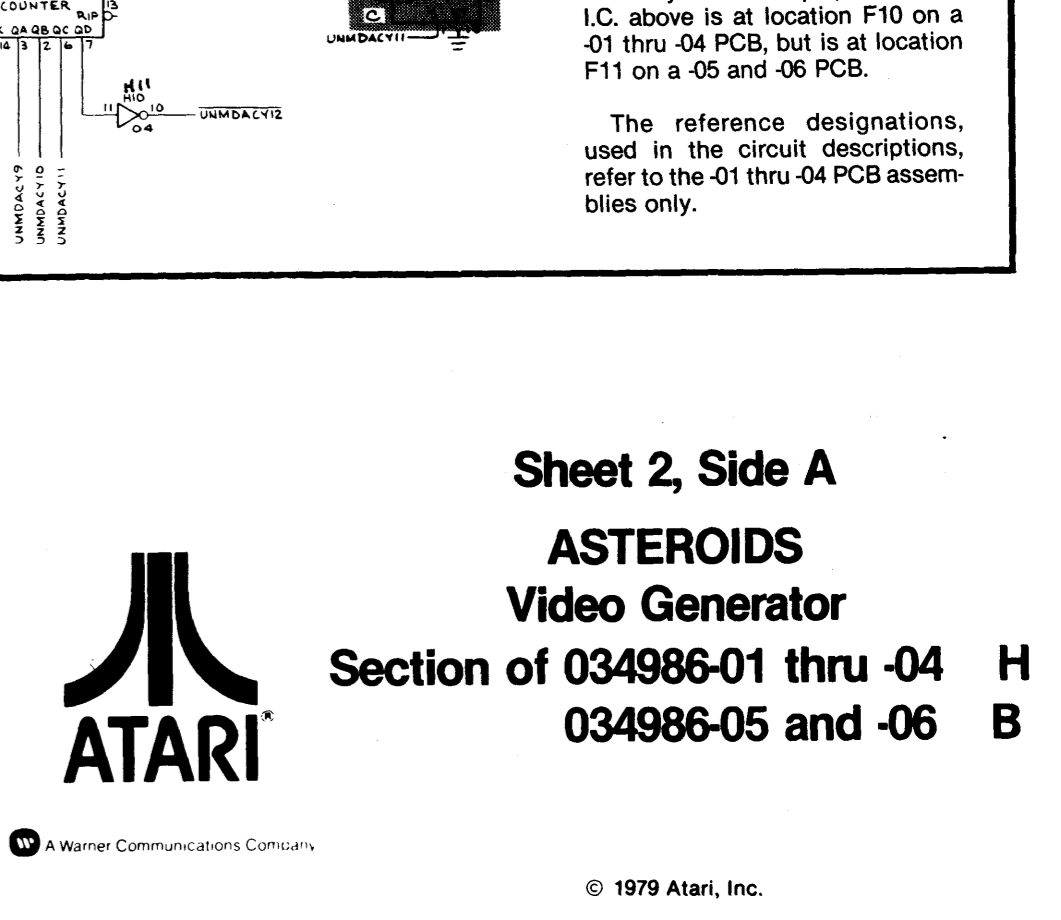
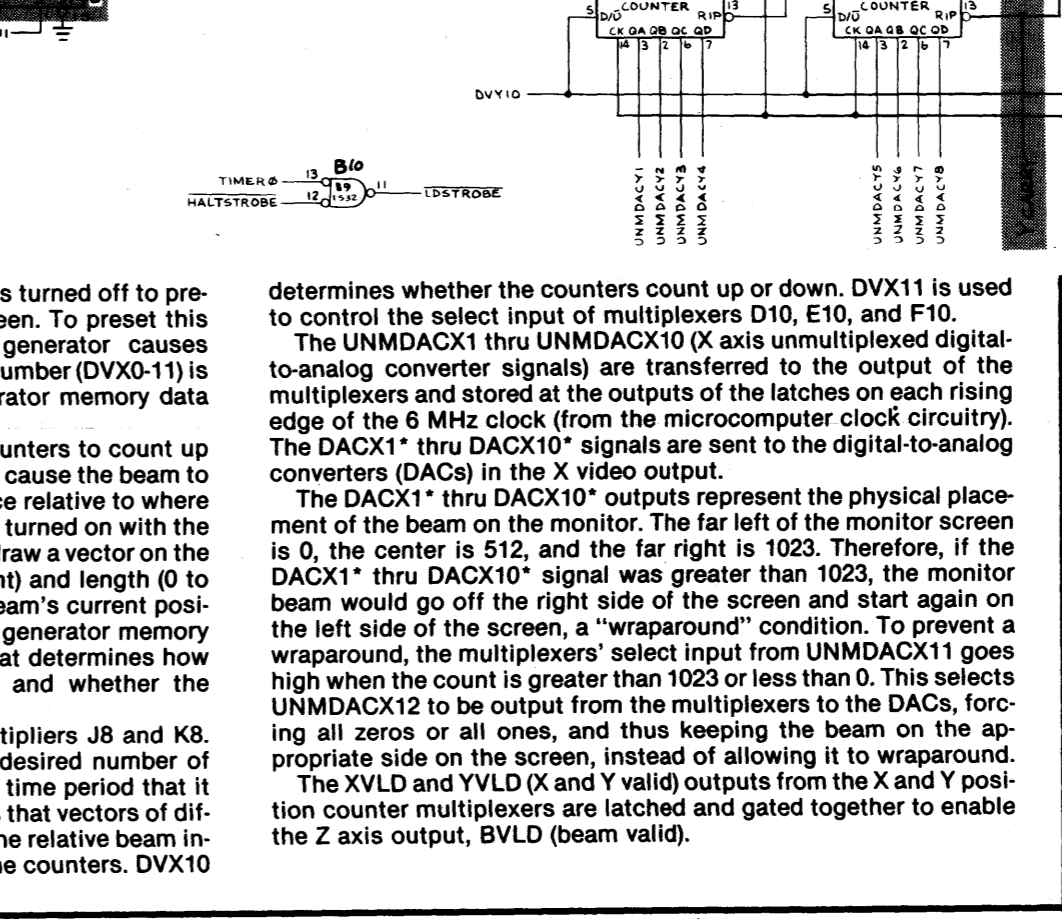
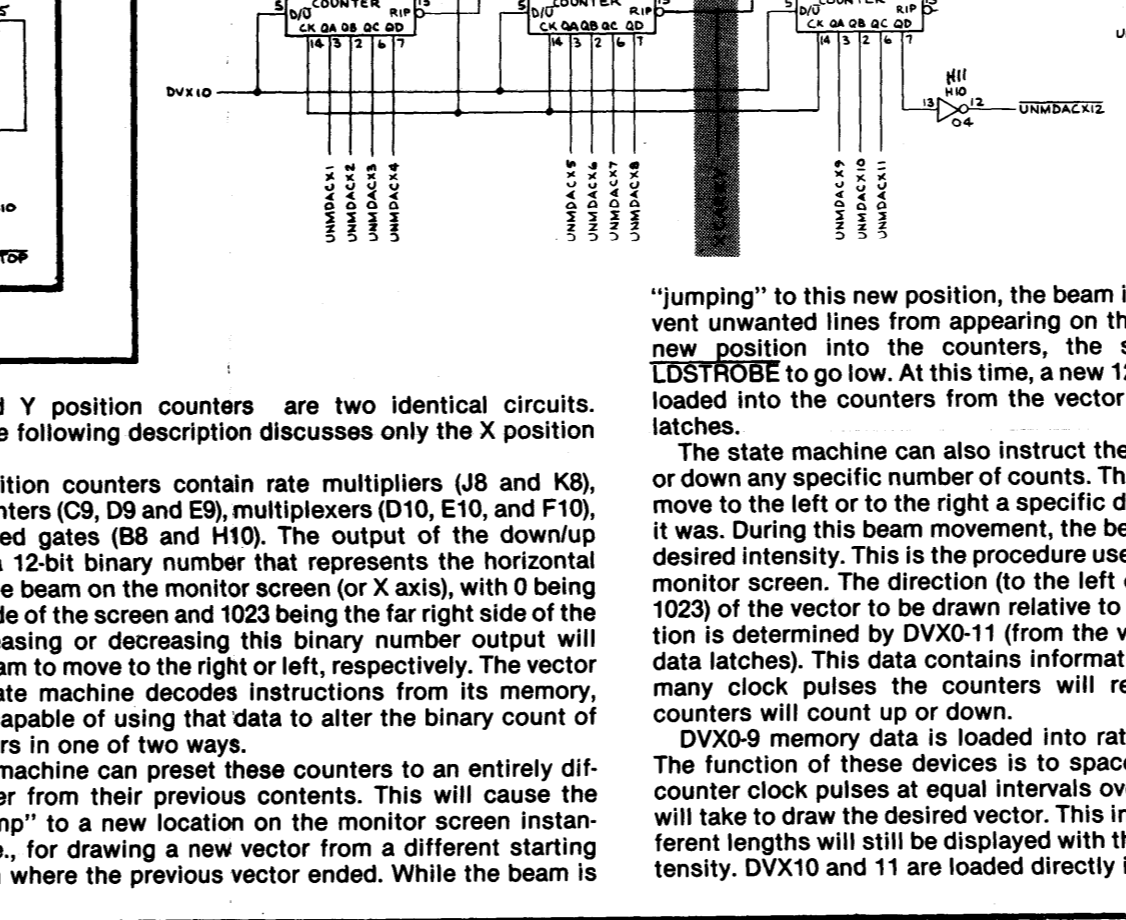
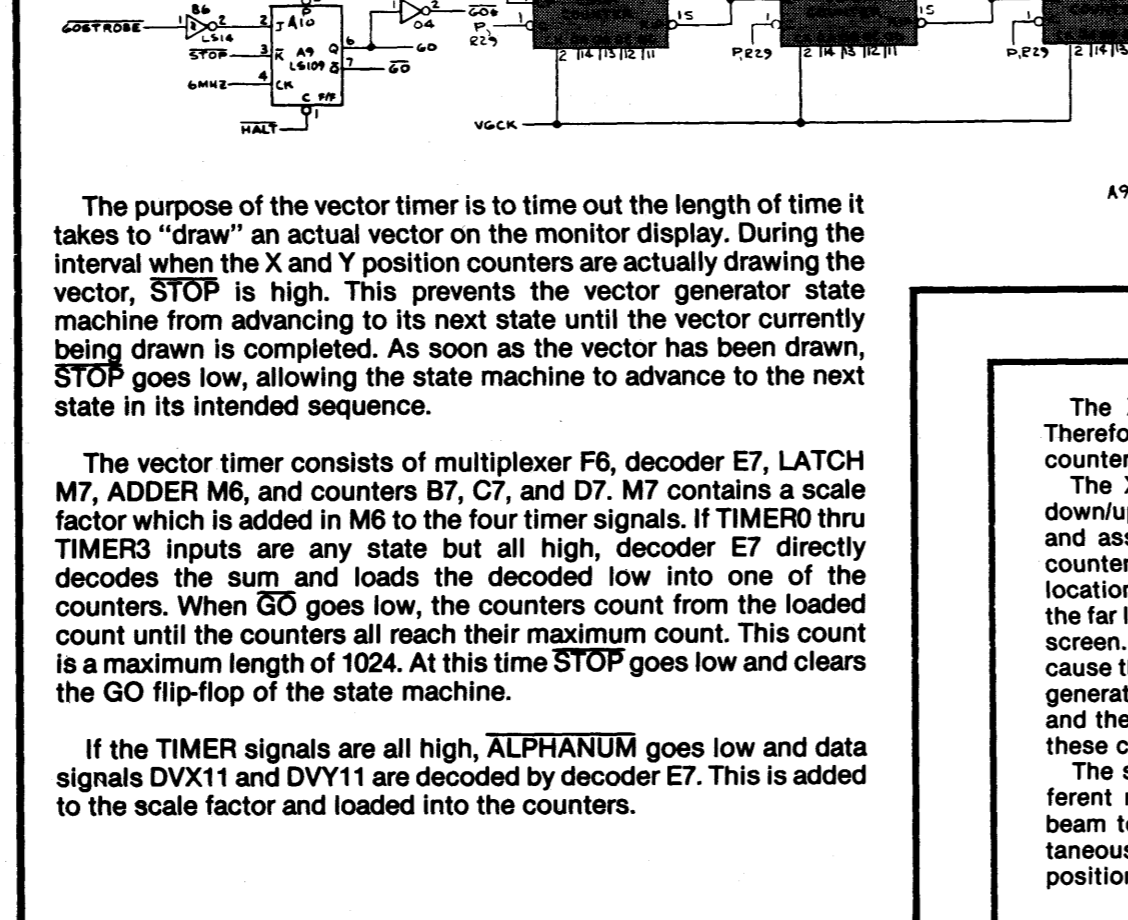
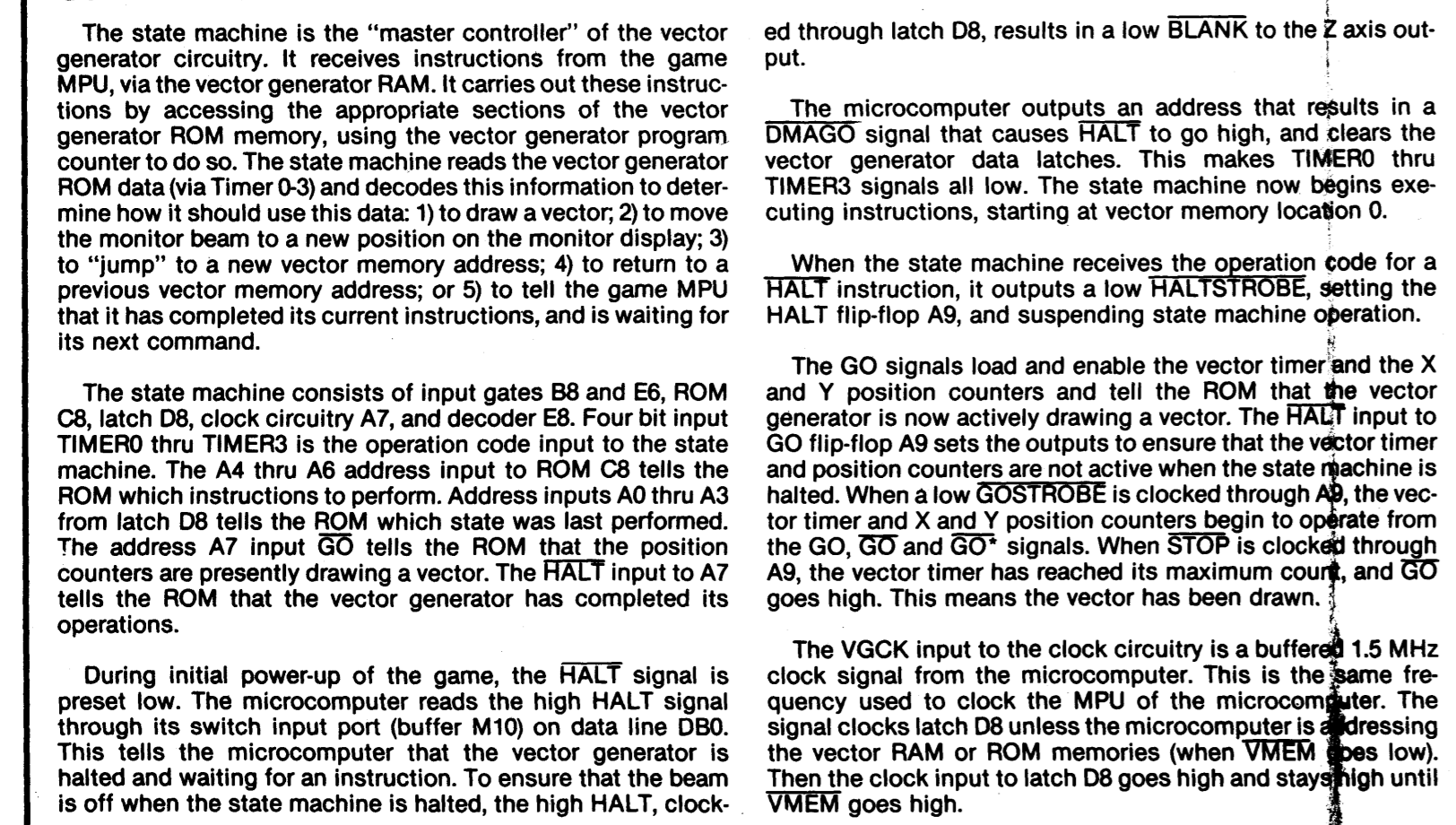
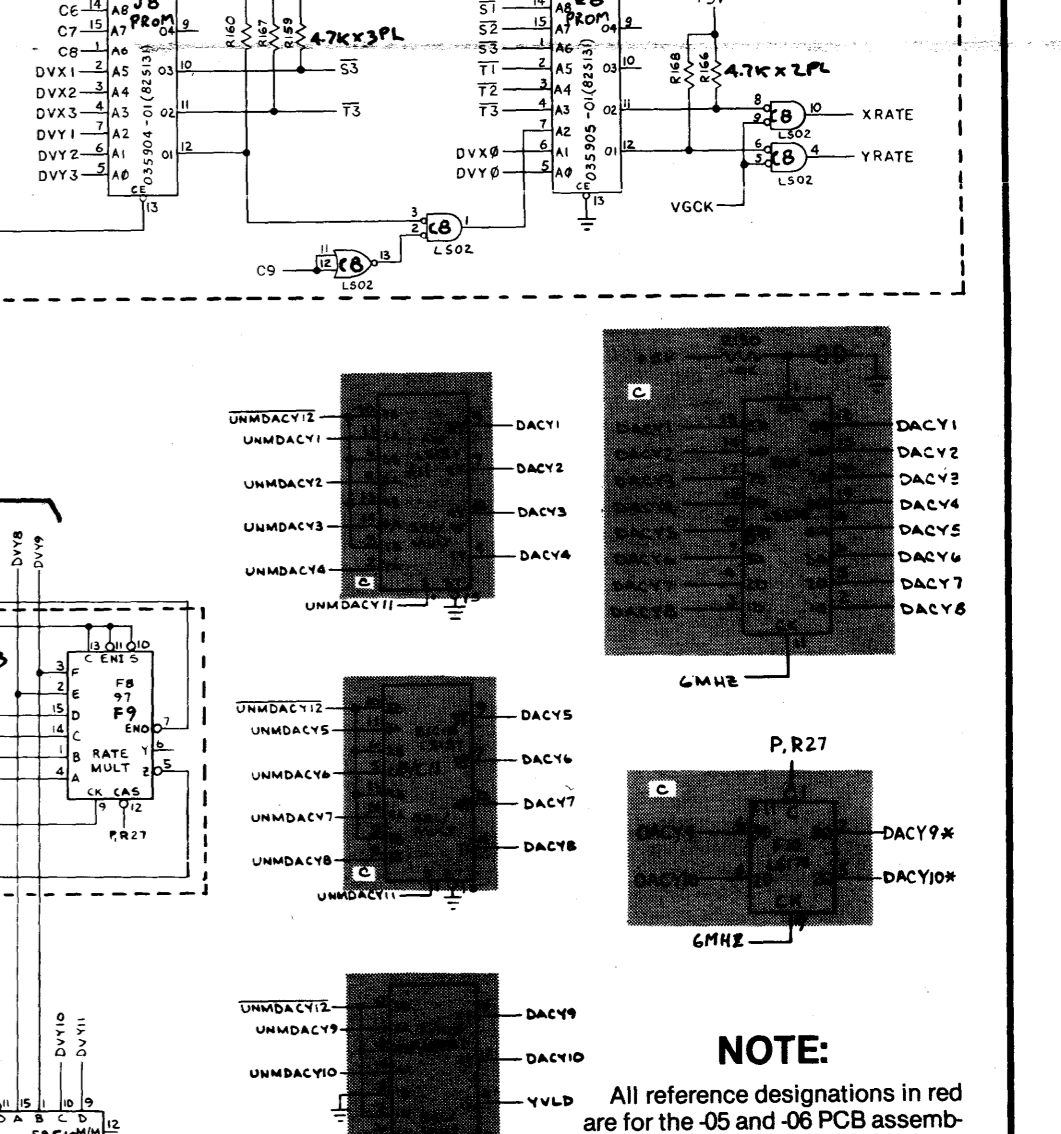
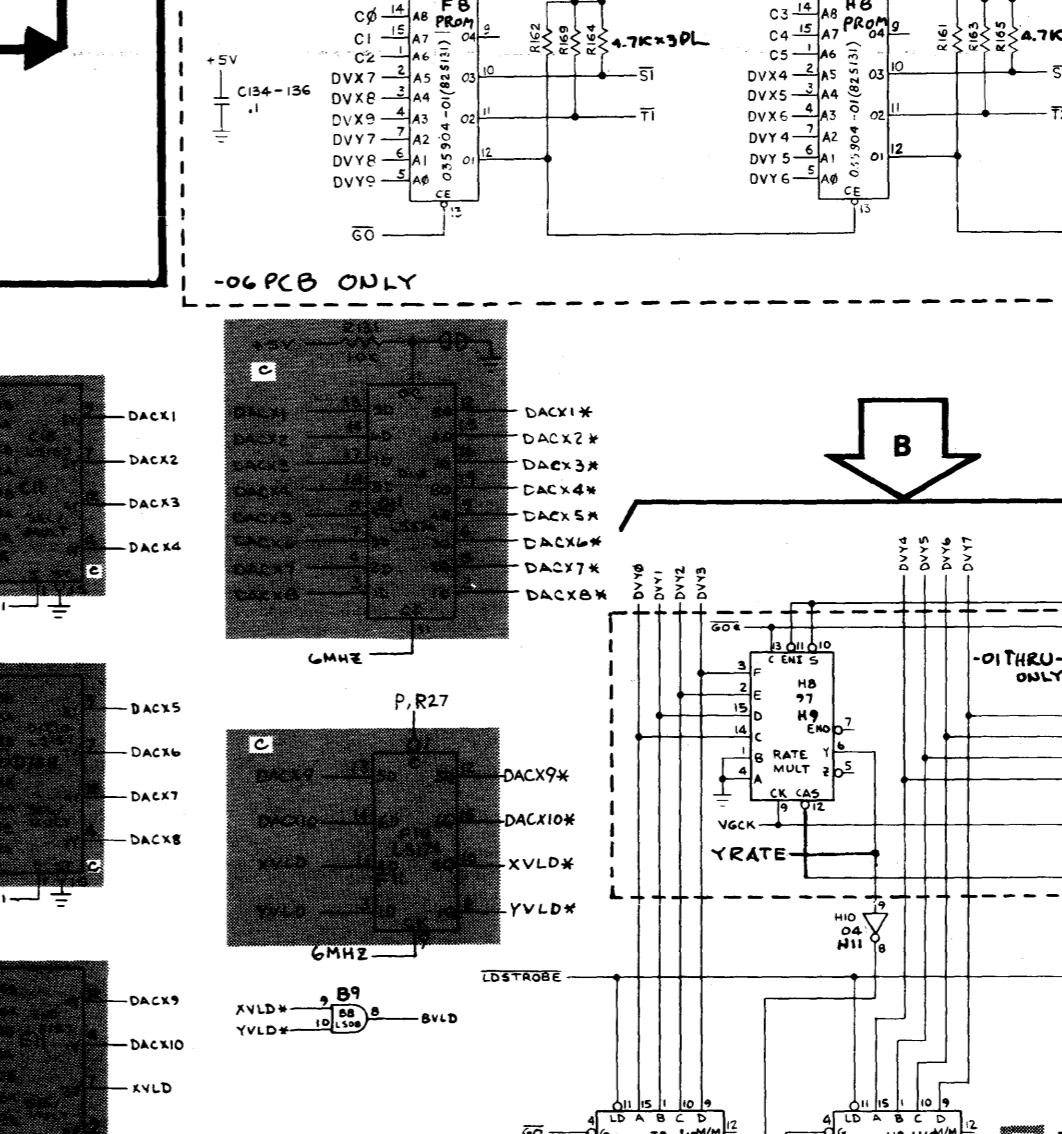
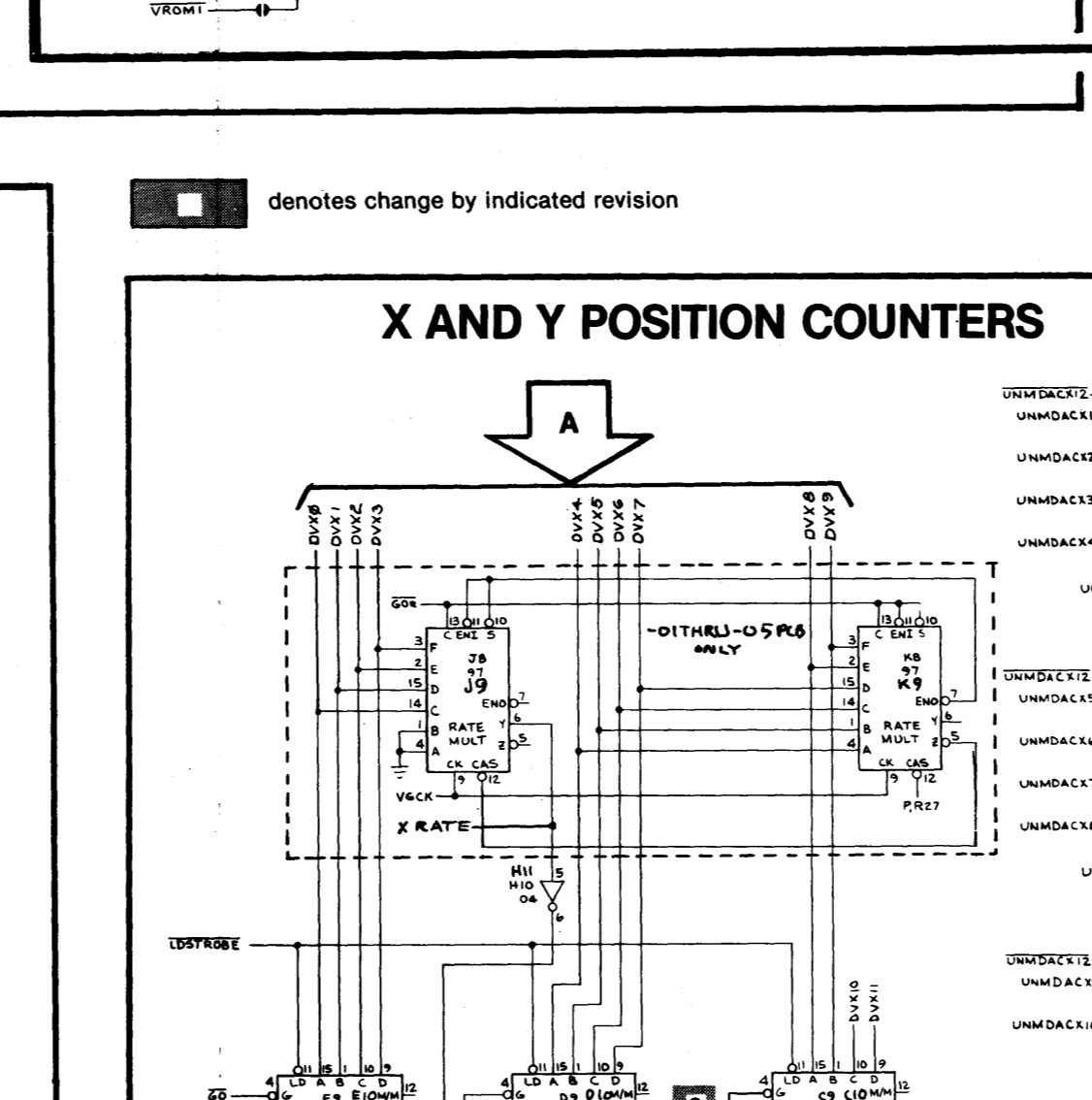
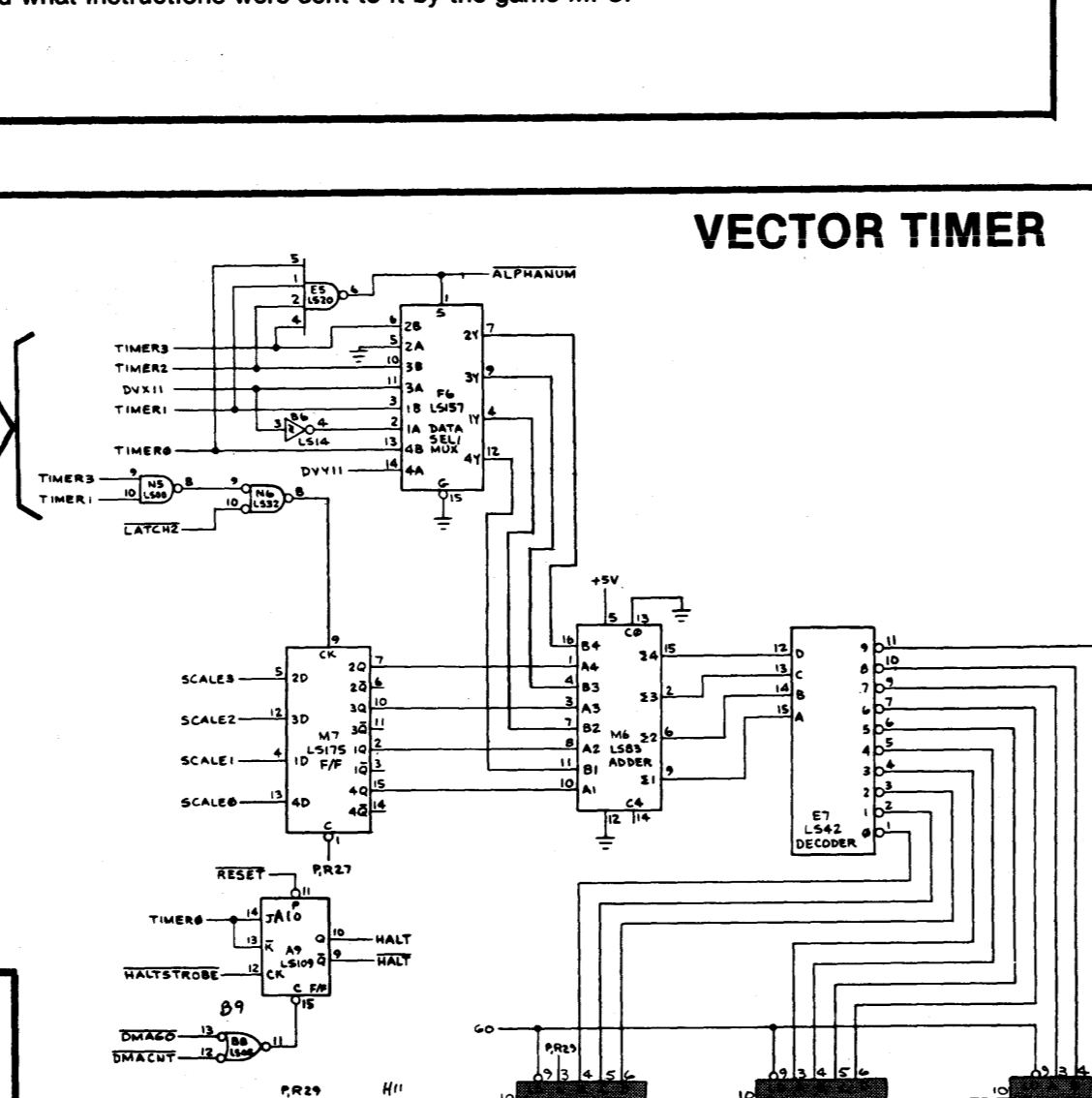
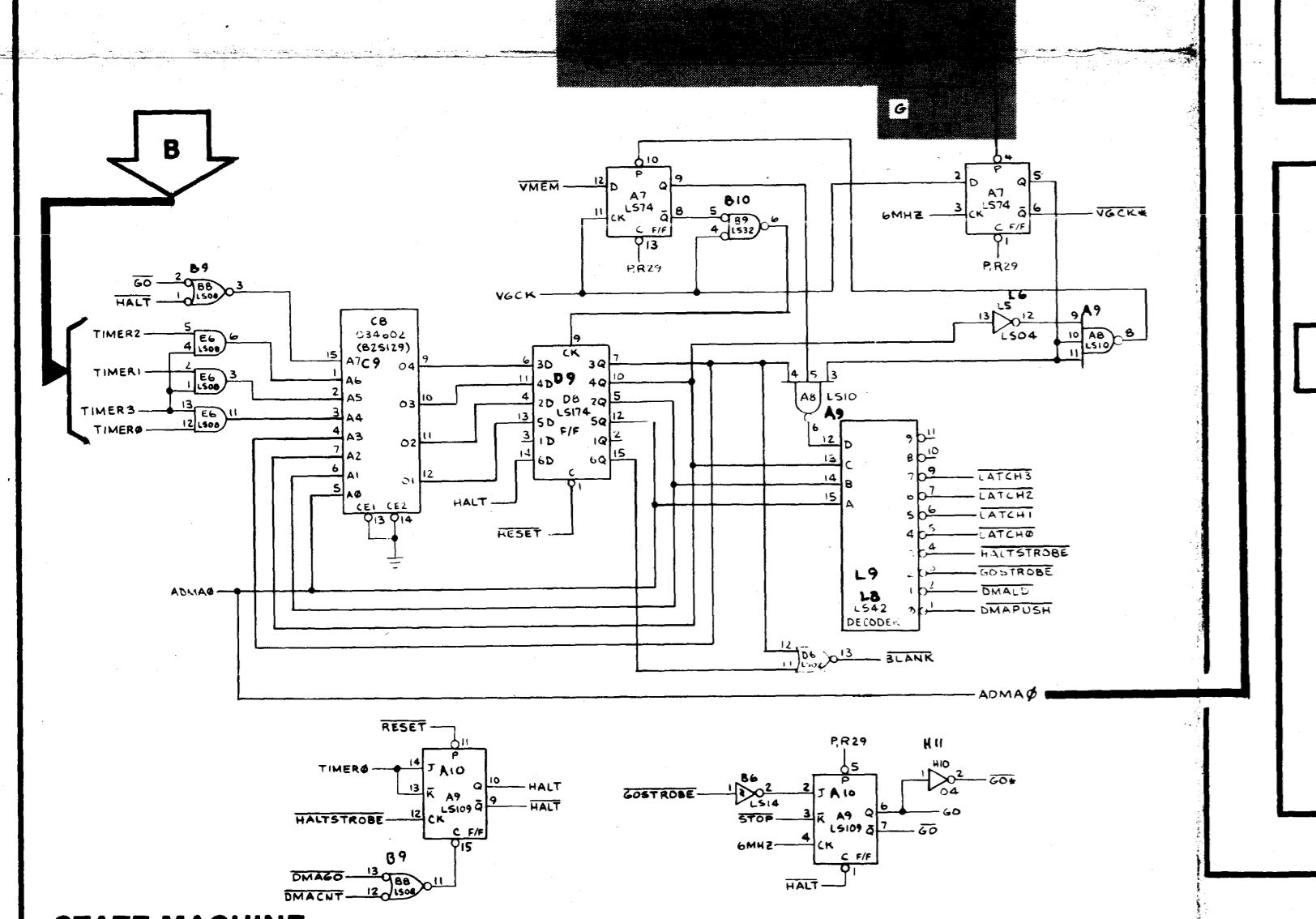
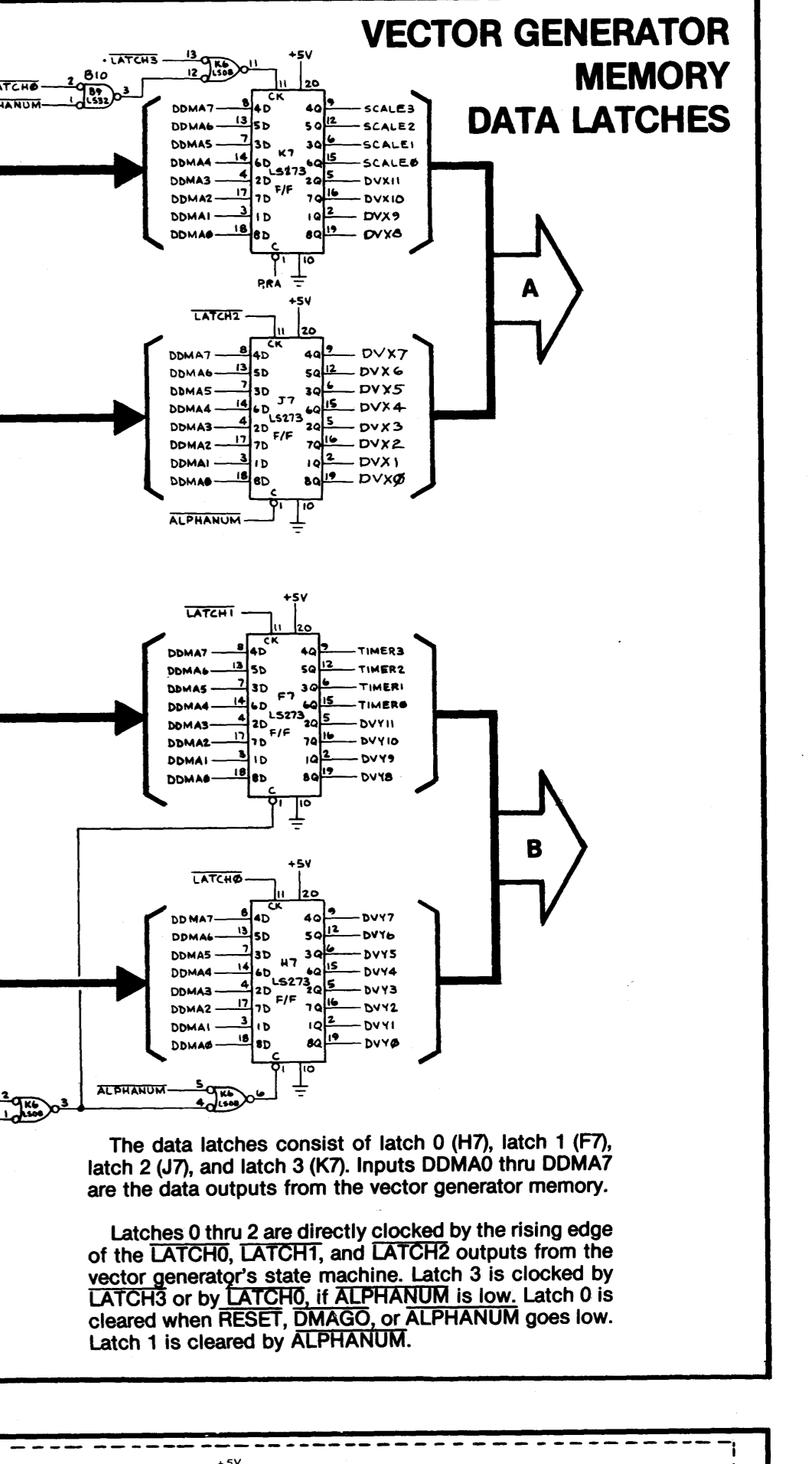
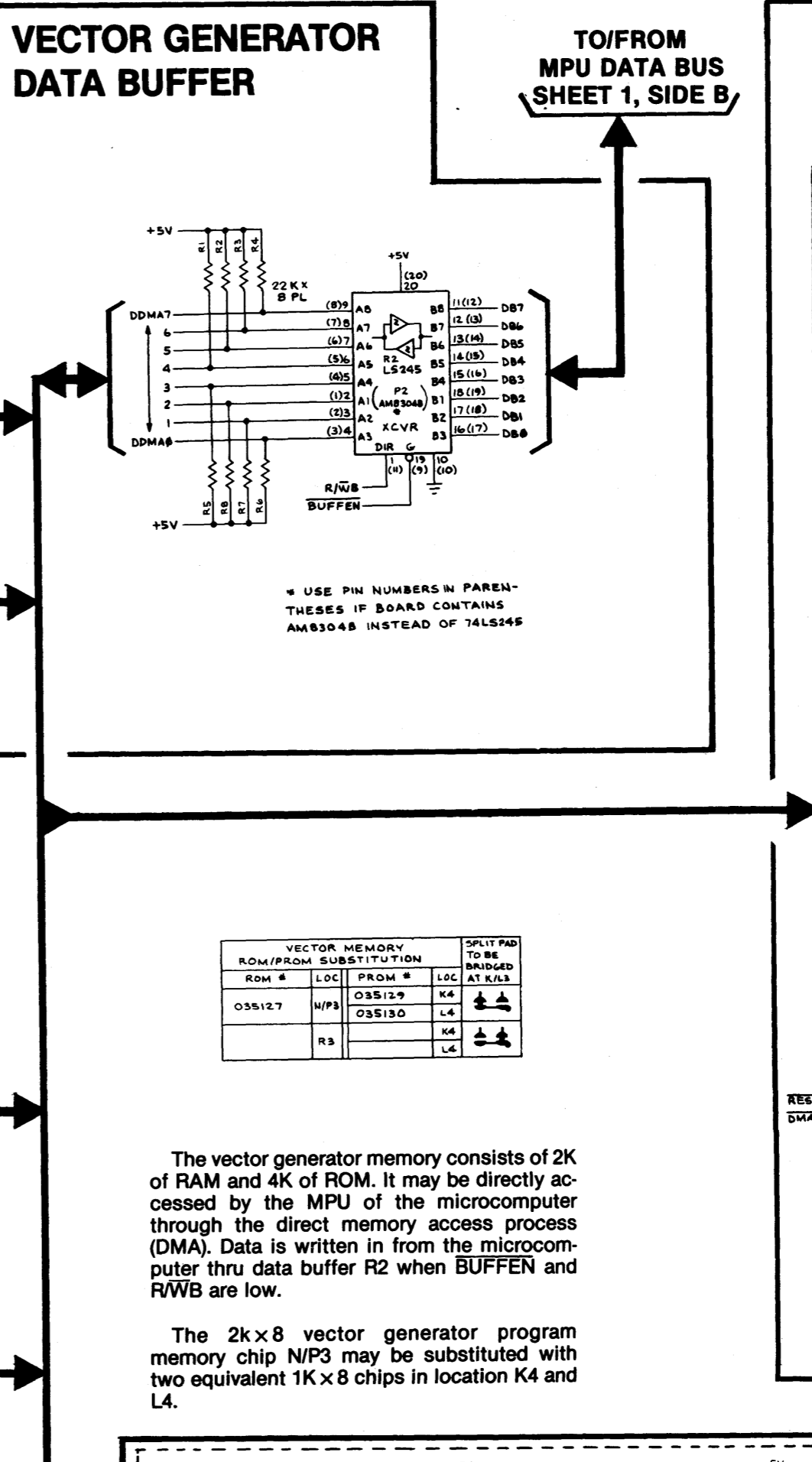
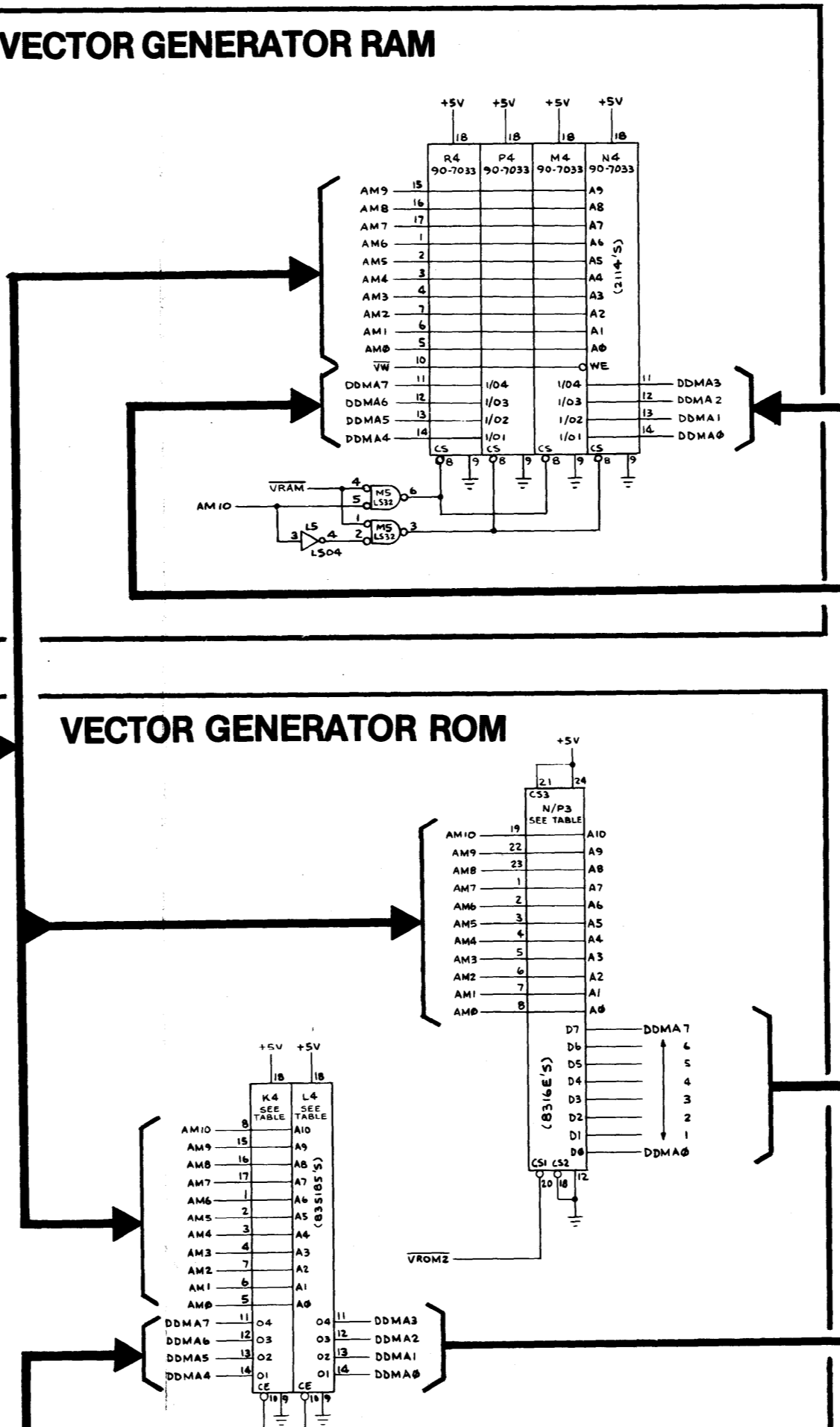
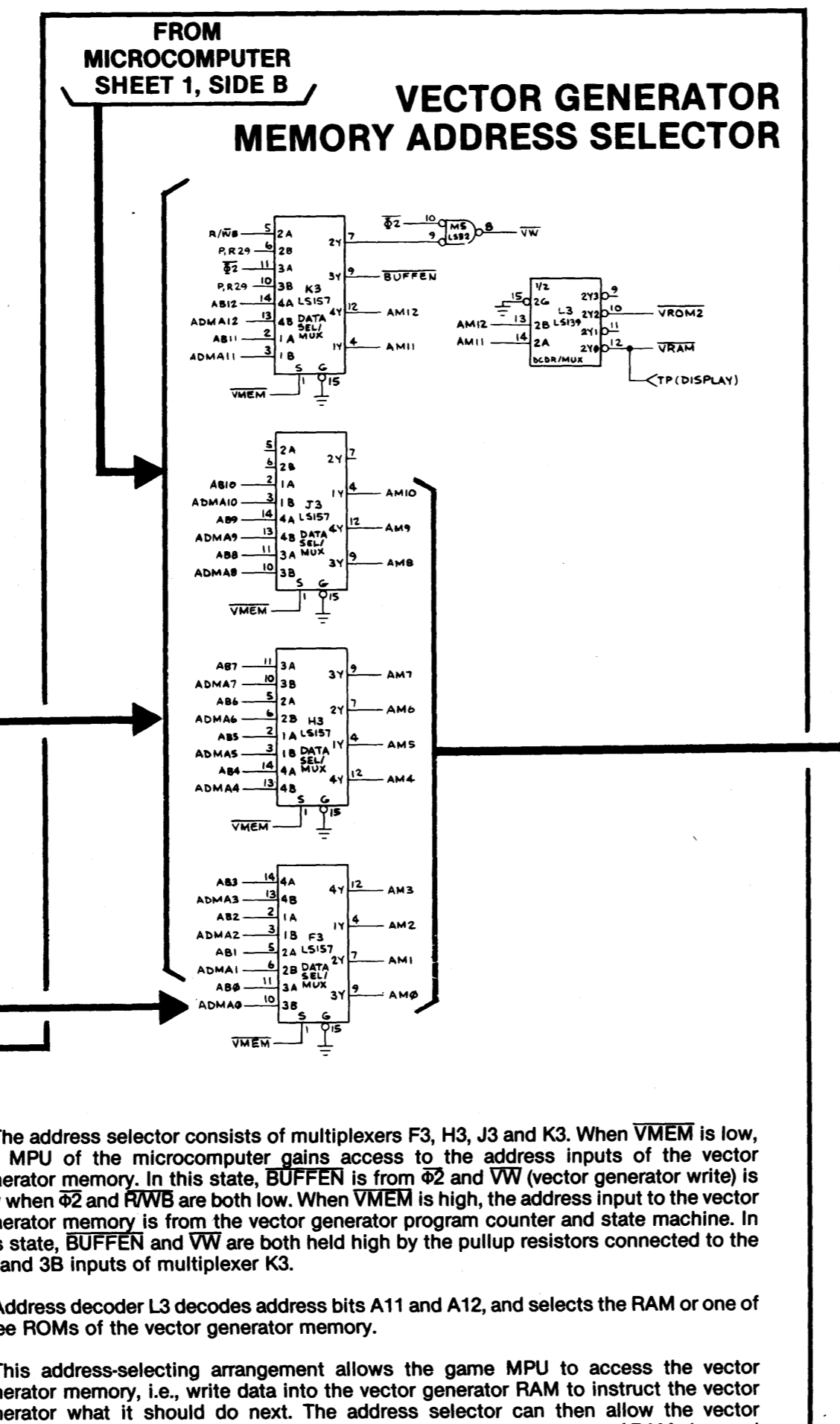
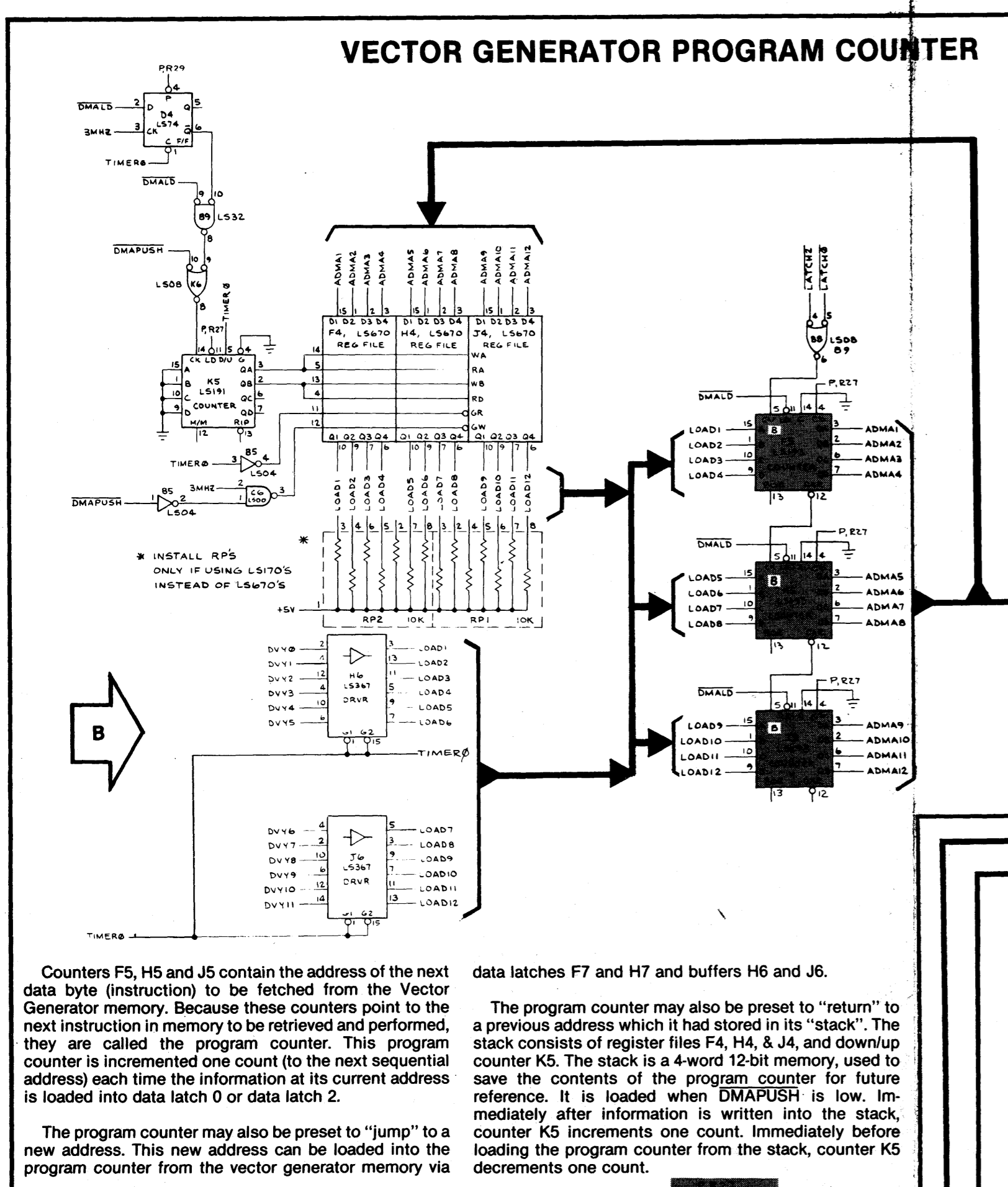


-03 P.C. Boards (PROMs)	Alternate -03 P.C. Boards (PROMs)	-04 P.C. Boards (ROMs)	-05 and -06 P.C. Boards (ROMs)
035131-02 J2	035150-02 J2		
035132-02 N2		035143-02 C1	035143-02 EIF2
035137-02 K1	035153-02 K1		
035138-02 N1			
035133-02 H2	035151-02 H2		
035134-02 M2		035144-02 DIE1	035144-02 H2
035139-02 J1			
035140-02 M1	035154-02 J1		
035135-02 F2			
035136-02 L2	035152-02 F2		
035141-02 H1		035145-02 F1	035145-02 J2
035142-02 L1	035155-02 L1		

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Sheet 1, Side B
ASTEROIDS
Microprocessor
Section of 034986-01 thru -04 H
034986-05 and -06 B



Sheet 2, Side A
DP-143-02 7th printing

The X and Y position counters are two identical circuits. Therefore, the following description discusses only the X position counters.

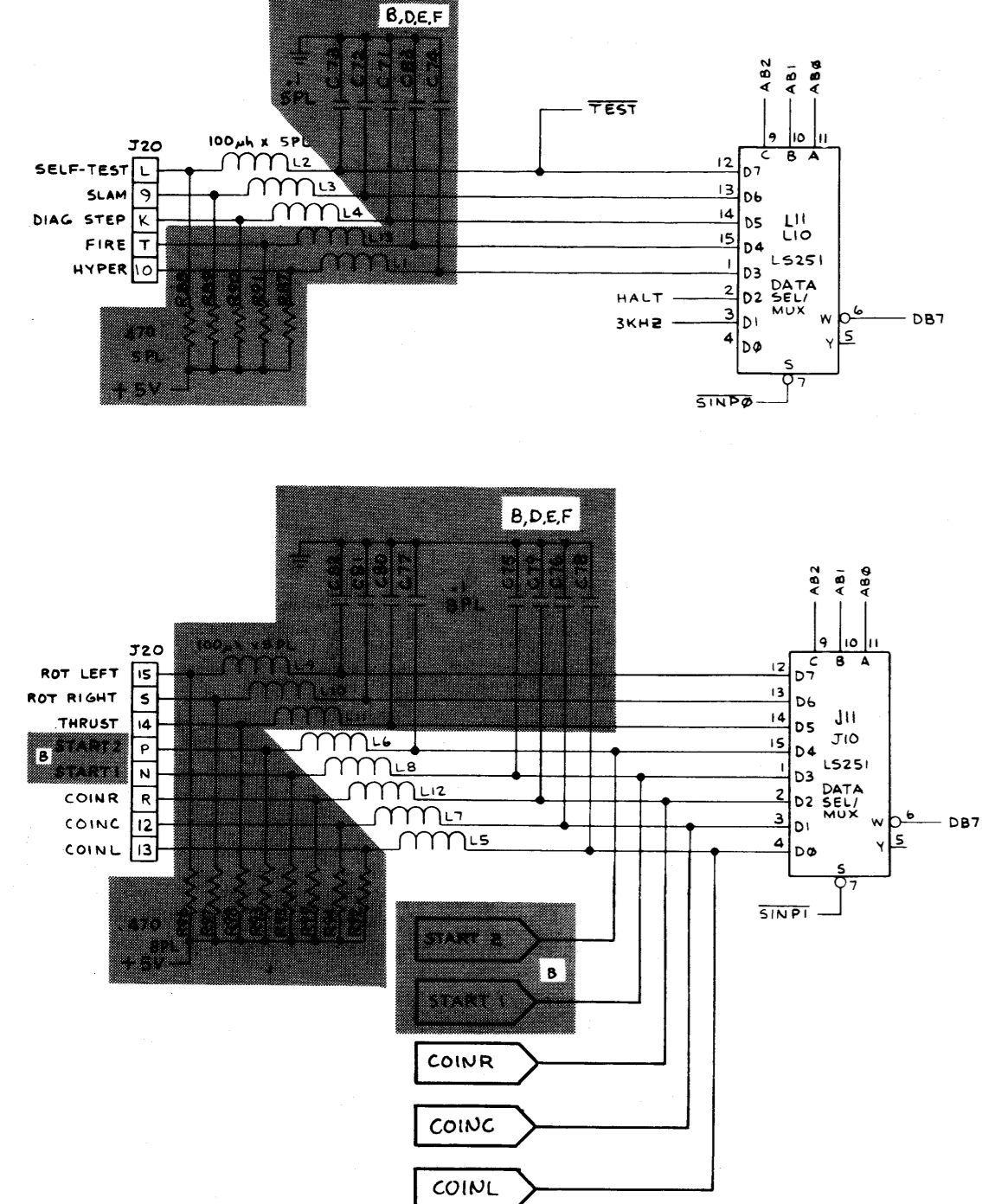
The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

The vector generator memory consists of 2K of RAM and 4K of ROM. It may be directly accessed by the MPU of the microcomputer through the direct memory access process (DMA). Data is written in from the microcomputer thru data buffer R2 when BUFFEN and RWB are low.

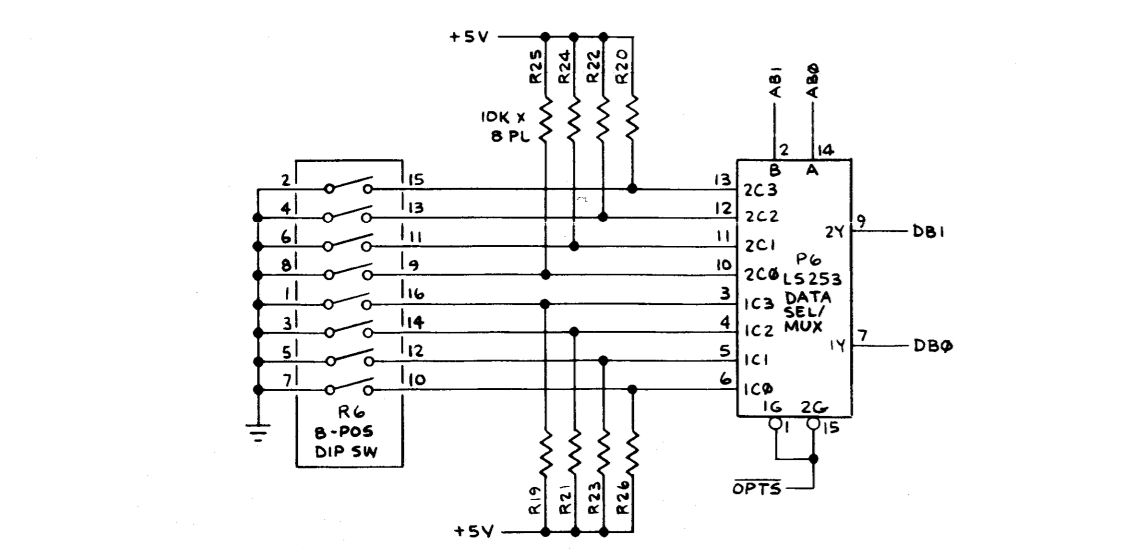
The reference designations, used in the circuit descriptions, refer to the -01 thru -04 PCB assemblies only.

INPUTS

PLAYER INPUT CIRCUITRY

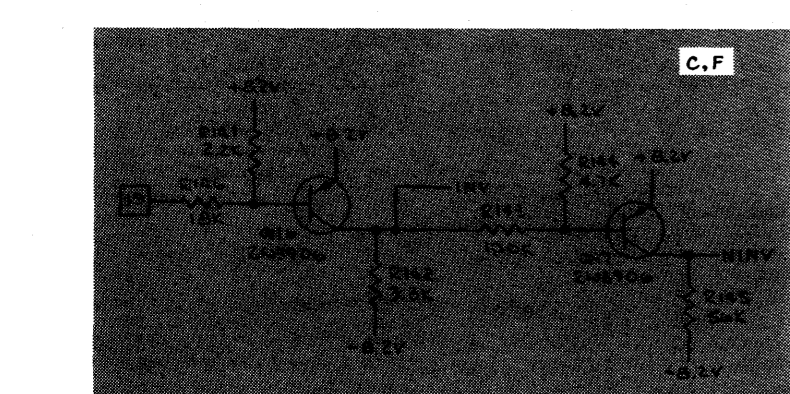


OPTIONS INPUT CIRCUITRY



denotes change by indicated revision

VIDEO INVERTER



The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, INV is -8.2 VDC and NONINV is about +8.2 VDC. The result is a non-inverted X-axis and Y-axis output.

In a cocktail game, the wiring harness shorts connector J20's output pin 7 input pin 19. When the video of player 1 is being displayed, pins 7 and 19 are +5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is +8.2 VDC and NONINV is -8.2 VDC. The result is an inverted X-axis and Y-axis output, causing the monitor's display to be upside down.

OUTPUTS

DIAG STEP (diagnostic step), 3 KHz, SELF-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when SINPT (switch input zero enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

The coin door and some control panel switches are read by the MPU when SINPT (switch input zero enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

The game option switches are read by the MPU when OPTS (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5, and 7 are read on data line DB0 and toggles 2, 4, 6, and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.

M10 latches control signals to enable different sounds.

The Fire sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contain a 555 operating as a voltage-controlled oscillator. The Saucer Fire sound is initiated by SAUCRFIREEN, and the Space Ship Fire sound is initiated by SHPFIREEN. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C38 & 39 for Saucer Fire Sound; C47 & 48 for Ship Fire Sound).

The EXPLODE sound is heard when any object explodes. Noise is sampled at a frequency determined by P8, and control bits EXPITCH0 and EXPITCH1. Changing the sampling rate changes the pitch of the explosion. The noise is amplitude-modulated in R7 by EXPAUD0-EXPAUD3.

R9 and P9 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.

The THUMP sound is heard throughout play. The 555 is connected as an oscillator, enabled by N7 pin 2. The frequency is determined by the current coming out of Q2. This depends on its base voltage, which is derived from the four-bit code in N7.

The SAUCER sound is heard when an enemy saucer appears. The 556 is a voltage-controlled oscillator. Its modulating voltage is derived from the 555. The 555 is a low frequency oscillator. The effect is a warbling sound. SAUCRSEL changes some component values, in order to provide for 2 different saucer sounds.

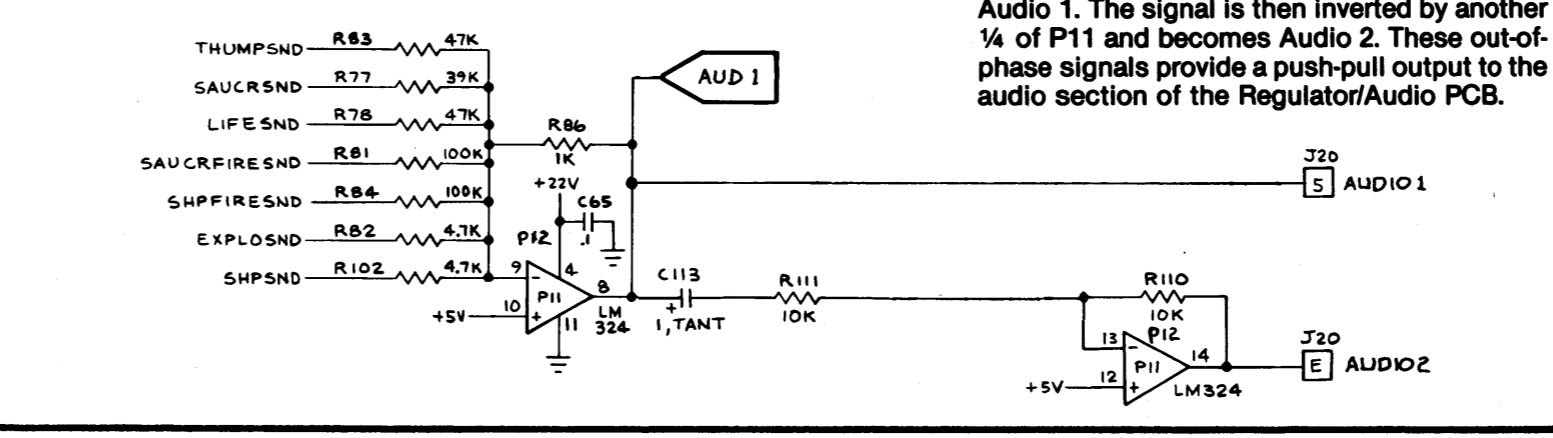
LIFE sound is heard when an extra life is gained. It is merely 3 KHz from the clock circuitry.

The EXPLODE sound is heard when any object explodes. Noise is sampled at a frequency determined by P8, and control bits EXPITCH0 and EXPITCH1. Changing the sampling rate changes the pitch of the explosion. The noise is amplitude-modulated in R7 by EXPAUD0-EXPAUD3.

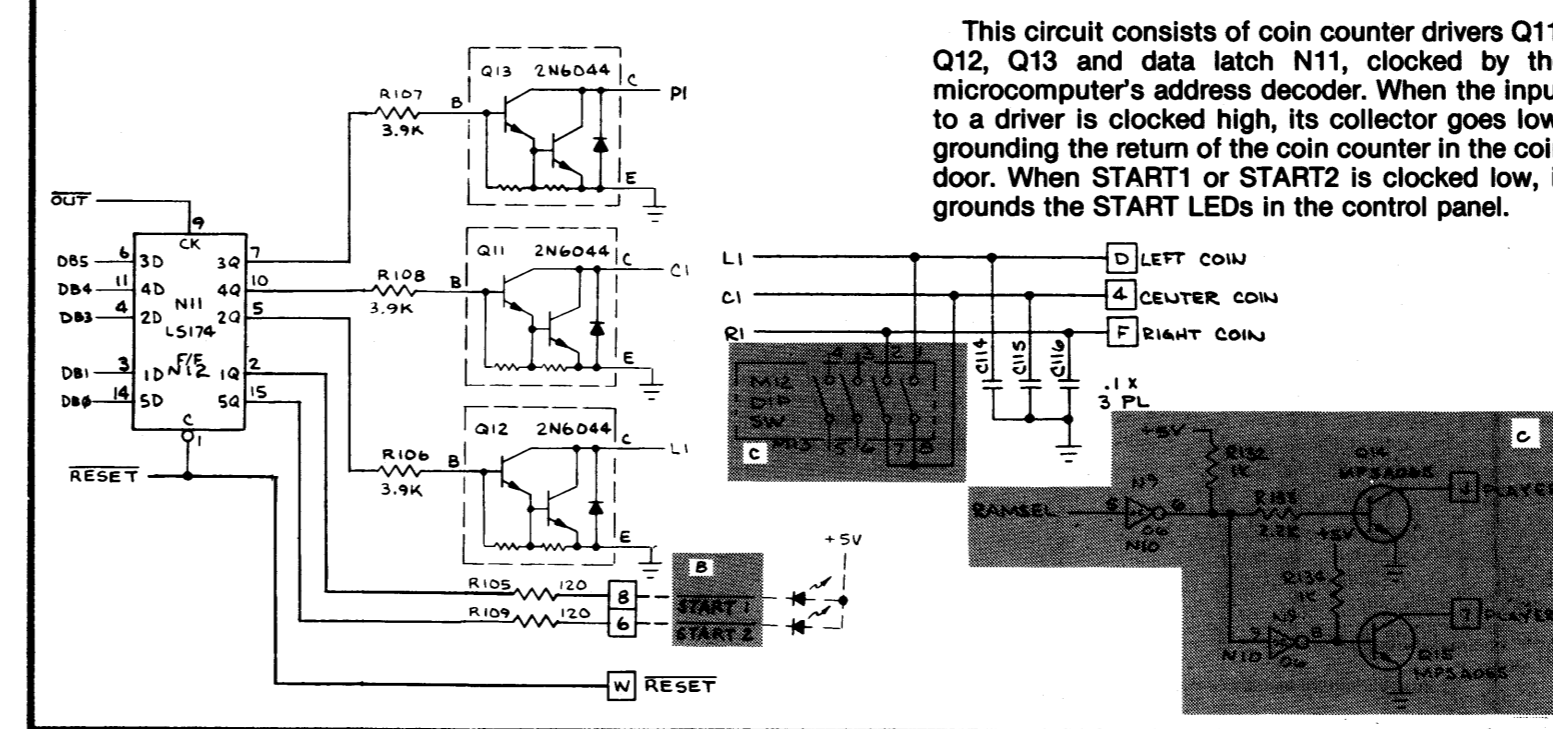
R9 and P9 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.



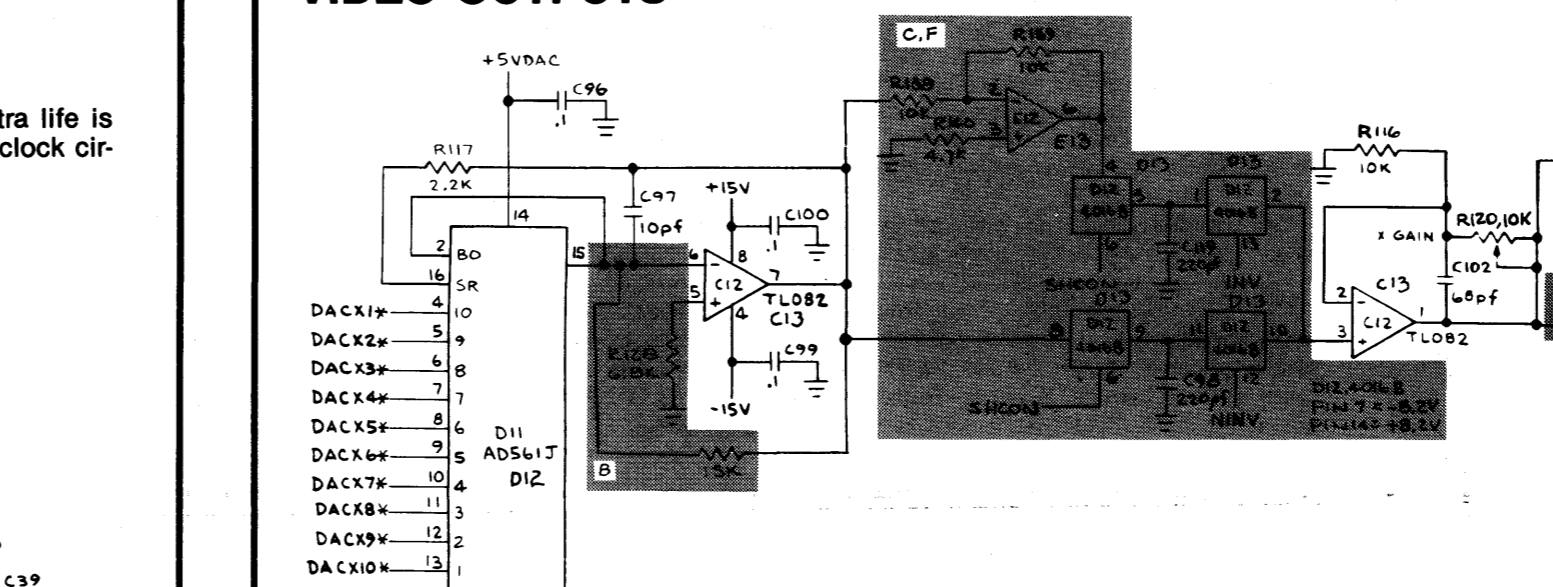
AUDIO OUTPUT



LAMP, LED, AND COIN COUNTER OUTPUT



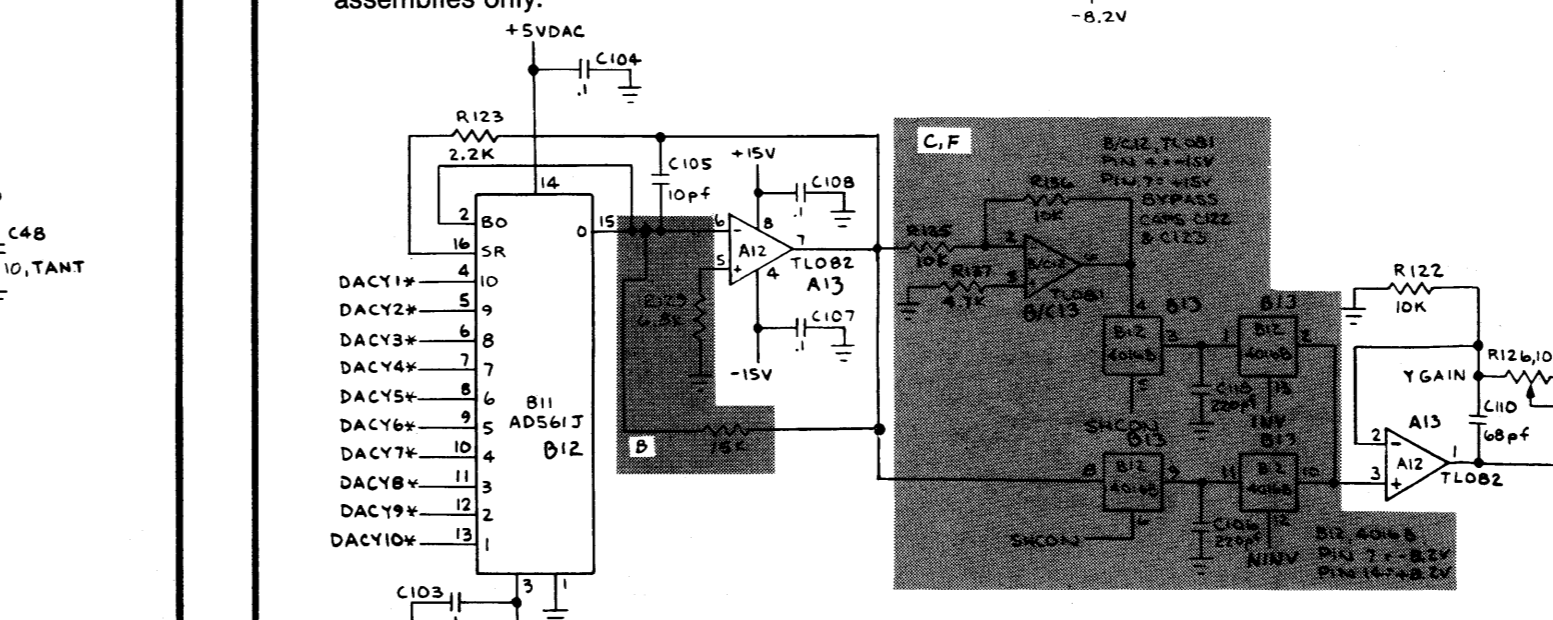
VIDEO OUTPUTS



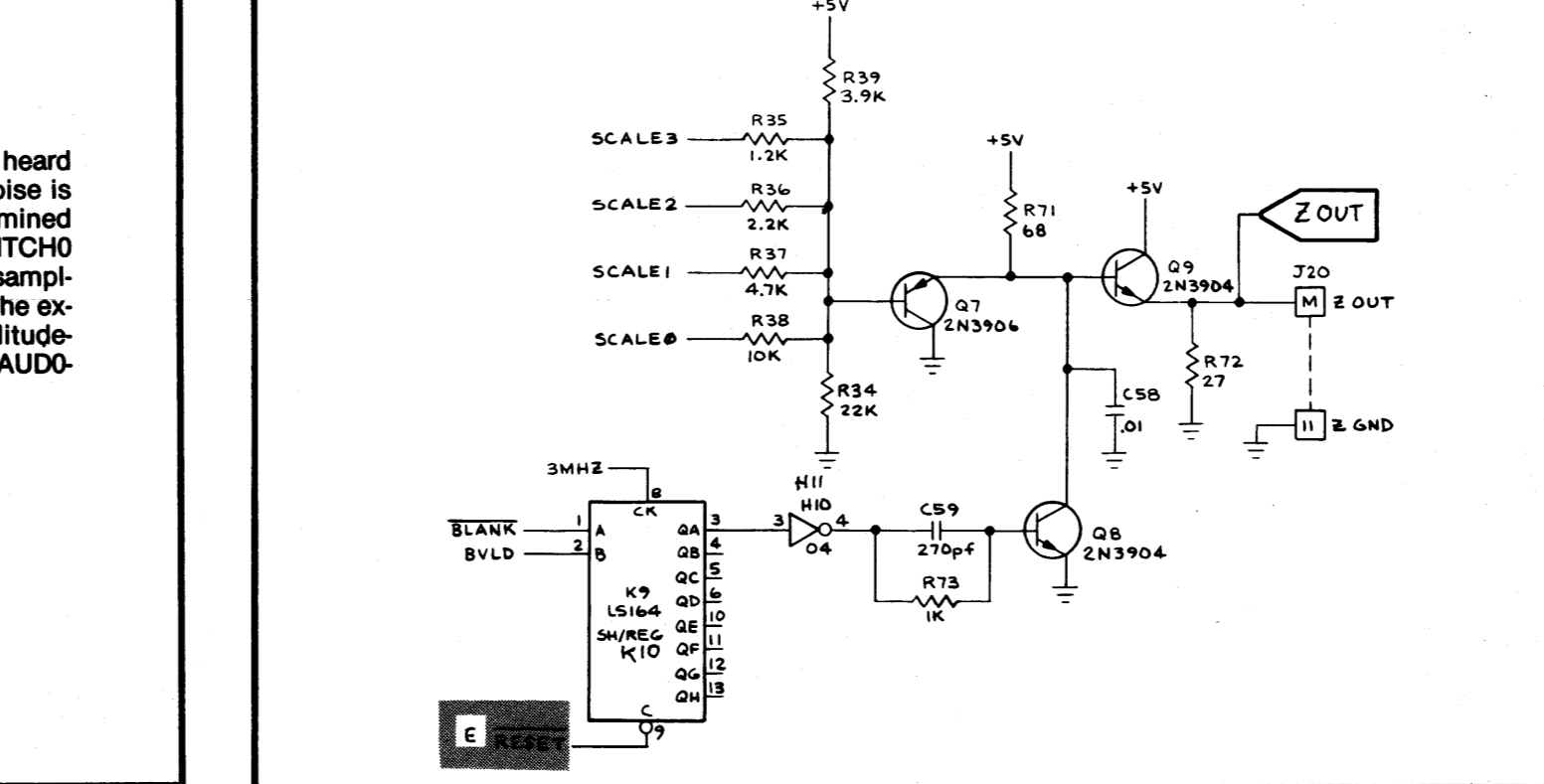
NOTE:

All reference designations in red are for the -05 and -06 PCB assemblies only. For example, the AD564J I.C. above is at location D11 on a -01 thru -04 PCB, but is at location D12 on a -05 and -06 PCB.

The reference designations, used in the circuit descriptions, refer to the -01 thru -04 PCB assemblies only.



Z Output



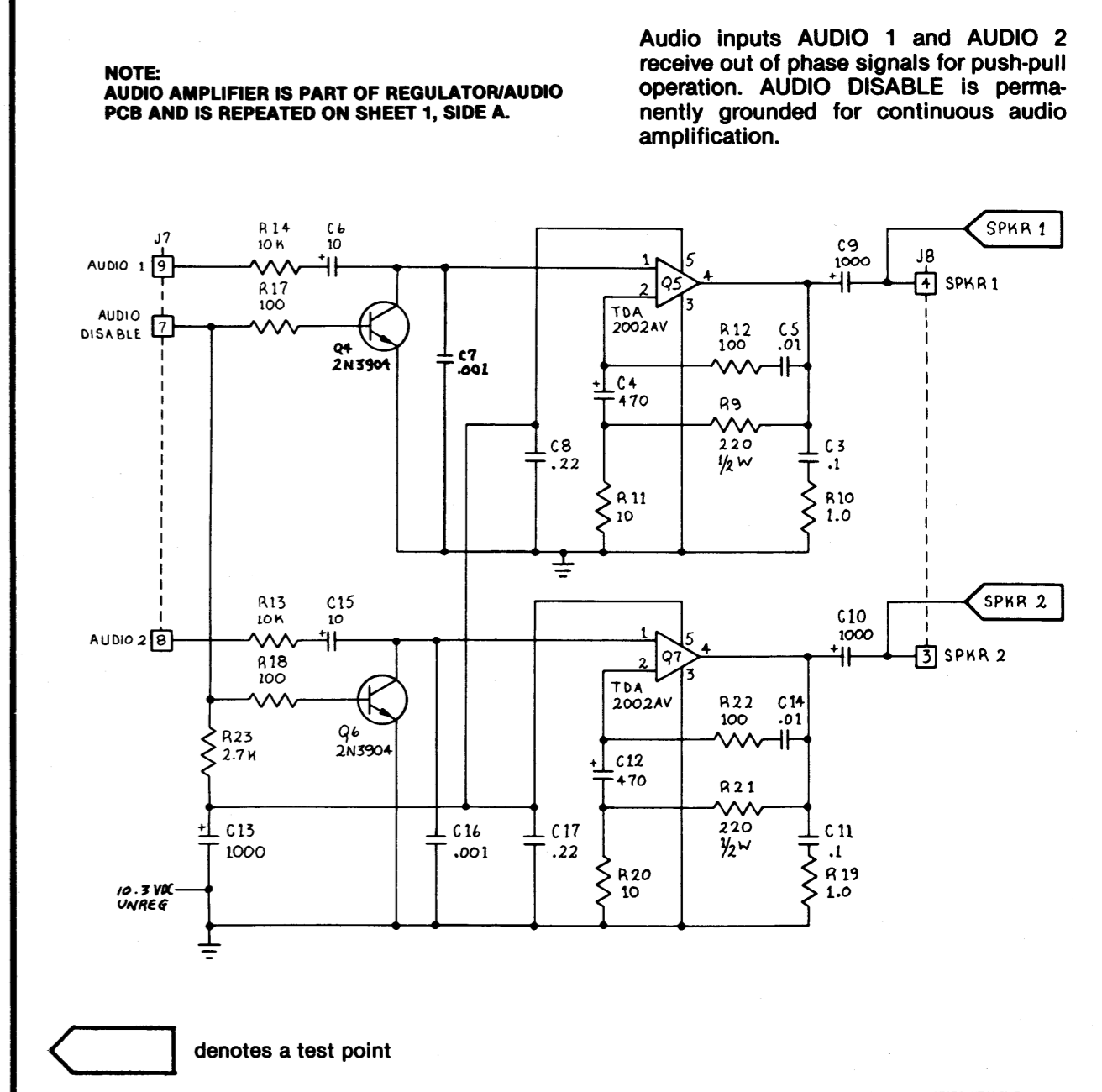
When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALED thru SCALES3 resistors R38 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

All sounds are mixed in 1/4 of P11. This is Audio 1. The signal is then inverted by another 1/4 of P11 and becomes Audio 2. These out-of-phase signals provide a push-pull output to the audio section of the Regulator/Audio PCB.

This circuit consists of coin counter drivers Q11, Q12, Q13 and data latch N11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

PART OF REGULATOR/AUDIO PCB



denotes a test point

The video output circuit consists of three individual circuits; X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and B11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y axis, the numbers range from 128 to 996, where 128 is at the bottom of the monitor screen, 512 is at the center, and 996 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs' current outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits. One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C98 for the X axis, and B12 and C106 for the Y axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C119 for the X axis and B/C12, B12 and C118 for the Y axis.

The sample and hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insures that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample and hold capacitors.

The output swing of SHCON is -8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to the X and Y analog output value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

Z Output

The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALED thru SCALES3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.

When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALED thru SCALES3 resistors R38 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

Sheet 2, Side B
ASTEROIDS
Switch Inputs, Coin Counter,
LED and Audio Outputs
Section of 034986-01 thru -04 H
034986-05 and -06 B



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