SYSTEM 19
UNIVERSAL PROGRAMMER
990-1902

REV J MAR 83 **026-1902**

FOREWORD

The System 19 is available in several configurations of operating software. Each configuration consists of the same System 19 mainframe, but they differ in their capabilities for I/O and remote control.

All System 19 manuals are composed of the basic Operation and Maintenance manual and either one or two addendum manuals which describe the I/O and, if so equipped, remote control capabilities of your System 19 configuration.

The Programmer Configuration sheet on the reverse side of this page lists the included hardware, software, and instruction manuals which explain the operation of the basic System 19 equipped with Computer Remote Control. The manuals listed in part A of the sheet are bound together in this cover.

1. **The System 19 Operation and Maintenance Manual** contains all instructions for the stand alone operation and care and maintenance of the System 19. These instructions cover installation of programming modules.

2. **The Translation Format Package Specifications Manual** describes the input and output requirements of the many data translators recognized by the programmer. Complete instructions for I/O operations with these formats are given.

3. **The Computer Remote Control Manual** describes the commands which the programmer will recognize for remote control by a computer or development system.

The lower right-hand corner of the Programmer Configuration sheet lists a unique Software Configuration Check number, which verifies the identity of the System 19's software. The System 19 will also display this number; after inspection and installation of the unit according to Sections 1 and 2 of the Operation and Maintenance Manual, turn ON the system 19 and press SELECT, key in B2 and press START. The Software Configuration number in the display should agree with the number on the configuration sheet.

Also check that the serial number on the Programmer Configuration sheet matches the serial number on the back of the unit.

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SECTION 1
INTRODUCTION

1.1 GENERAL

The Data I/O System 19 produces reliably programmed semiconductor devices from data received from any one of a number of sources, or a combination of sources. The design philosophy is universality — both in the device to be programmed and the forms of data which are accepted. To this end, Data I/O manufactures a full line of programming modules which allow the System 19 to program all commercially available programmable memory and logic devices. Consideration of the similar characteristics of a single manufacturer's range allows a single module, together with a number of inexpensive socket adapters, to be capable of programming all the devices in a "generic family."

Data I/O regularly publishes a "Comparison Chart of Programmable Devices." This is a ready reference for users to help them keep abreast of programmable device technology. It lists the available devices against the Data I/O part number for the programming module and socket adapter.

The System 19 provides a full duplex serial port for connection to sources of serial data, such as modems and paper tape readers. When the serial port is connected to a terminal, the Remote Control option allows data manipulations and complete remote control of all programmer functions. All the commonly encountered data transmission formats are available to allow quick and easy interface to any data source.

A comprehensive front panel allows keyboard data entry and manipulation. This basic concept of storing data in internal programmer memory allows for data preparation.

The System 19 is a microprocessor controlled instrument and performs a large number of automatic operations to ensure correct programming. All Data I/O programming techniques are approved by the device manufacturer. A number of tests (sum-check, blank check, illegal bit, etc.) are automatically performed to ensure that the device will perform to manufacturer's specifications under minimum and maximum voltages and varying load conditions.

Sophisticated software techniques and generalized hardware design allow the System 19 to respond to future developments in programmable device technology.

1.2 SPECIFICATIONS

1.2.1 MAJOR COMPONENTS

Control Electronics. The unit is microprocessor controlled, with 4Kx8 bit RAM and RS232C or 20mA current loop serial input/output (I/O). RAM and program memory expansion are possible.

Programming Electronics. Interchangeable programming modules, including Programming Paks, the Gang Module and the UniPak, contain all interface electronics and select appropriate control software. Voltages are current limited and monitored to meet the device manufacturer's programming specifications.

1.2.2 POWER REQUIREMENTS

Operating Voltage. Operating voltage is selectable from 100, 120, 220 and 240 VAC, 50-60 Hz, single phase, grounded.

Voltage Tolerances.

100 VAC ±10%
120 VAC ±14%
220 VAC ±14%
240 VAC ±10%

Power Consumption. 35 Watts.

Fuse Protection. A circuit breaker is an integral part of the ON/OFF power switch on the back of the unit. The power supply is separately fused on the main electronics board. Blown fuses indicate a need for factory service.

1.2.3 PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

Dimensions. 38.1 cm x 15.2 cm x 27.3 cm (15" x 6" x 10.75").

Weight. 6.4 kg (14 lbs).

Operating Temperature Range. 0 to 40°C (32 to 104°F)

Storage Temperature Range. -40 to 55°C (-40 to 131°F).

1.3 PROGRAMMER CONFIGURATIONS

The System 19 is available in several software configurations. The standard programmer (990-1900) includes Serial I/O capability using the ASCII-Hex (Space) data translation format. The Data Translation Format Package (990-1901) is available to allow data transmission in over 20 additional formats. Also available are system configurations providing Computer Remote Control (990-1902) and Terminal Remote Control (990-1903).

The following hardware options may be added to the System 19:

UniPak. Allows programming of most popular bipolar and MOS PROMs.

Gang Module. Allows programming of up to 8 MOS PROMs in parallel.

Paper Tape Reader/Punch. Allows high-speed entry of tape-punched data to programmer RAM, as well as punched-tape storage of RAM data.

Memory Expansion.

a. 4K RAM, P/N 950-1533-1. This add-on feature provides a total of 8K bytes, used to program larger devices.

b. 12K RAM, P/N 950-1533-2. This feature enlarges RAM to a total 16K.

Port Multiplier. Provides 2 additional serial ports and 1 parallel port for expanded I/O capabilities.

1.4 LIMITED WARRANTY

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period for the System 19 is one year. The warranty period for programming electronics is 90 days. The warranty period begins upon receipt of the equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. The service shall not apply to equipment that has been subject to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

NOTE

For shipment for warranty service, package the unit in accordance with the instructions in paragraph 2.6. Improper packing will void the warranty. For information regarding proper return location and procedure, contact your local Data I/O representative.

1.5 SERVICE

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses and shipping. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation, is billed at standard service labor rates when implementing approved, customer-requested modifications.

1.6 ORDERING

Orders for parts should contain the following information:

- Description of part(s) and Data I/O part number(s)
- Quantity of each item ordered
- Programmer serial number and model number
- Corporate name of customer firm
- Shipping address of firm, including zip code
- Full name of person ordering the part(s)
- To whose attention the part(s) are to be shipped
- Billing information
- Purchase order number
- Method of shipment

All parts orders may be sent to your local Data I/O representative.

SECTION 2
INSTALLATION

2.1 INTRODUCTION

The following paragraphs present information needed for connecting the System 19 to a power source, including power and fuse requirements, and information for serial interface connection of the unit.

2.2 INSPECTION

The System 19 was inspected and tested both electrically and mechanically before it was shipped. Proper adjustment was made for the intended line voltage. For trouble-free initial operation, it is important to verify that the equipment is in the best possible condition upon receipt.

The System 19 was carefully packaged to prevent any possible shipping damage. It should, therefore, arrive free of any defect, electrical or mechanical, without marks or scratches, and in perfect operating condition. Carefully inspect the unit for any damage that may have occurred in transit, and also check that the accessories listed in Table 2-1 are present. If any physical damage is noted, file a claim with the carrier and notify Data I/O.

Table 2-1. Standard Equipment Supplied

Description	QTY	Data I/O P/N
System 19 main unit	1	901-1900
Power Cord (U.S.A.) or	1	416-1577
(Europe)	1	416-0010
Serial Port Mating Connector	1	401-3064
Connector Hood	1	401-3069
Instruction Manual	1	026-1900

Check System 19 operation only after completing the installation as described in the following paragraphs.

2.3 POWER CONNECTION

2.3.1 REMOVING AND INSTALLING THE PROTECTIVE SHIELD

First, remove the programming module by pulling gently to disconnect it from the mating connector. The protective shield is then loosened by pulling the two snap-lock connectors and lifting the back edge out first and then pulling the plate up slightly and turning it to the left until it clears the opening on the programmer's front panel.

Be sure to install the shield again after adjusting the line voltage.

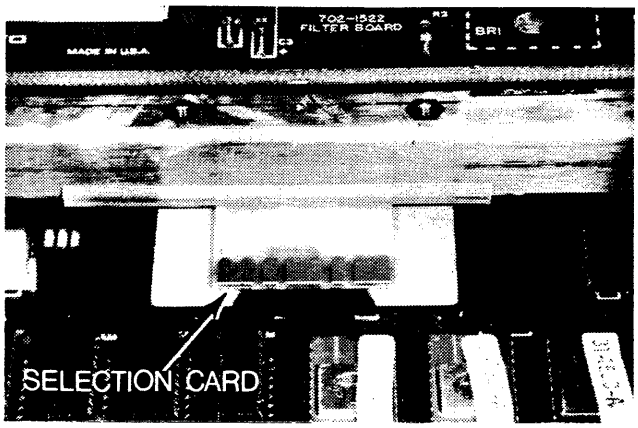


Figure 2-1. Operating Voltage Selection Card.

2.3.2 ADJUSTING THE SYSTEM 19 TO THE OPERATING VOLTAGE

CAUTION

Attempting to operate the unit at operating voltages outside the selected voltage limits will damage the unit.

The proper voltage has been selected at the factory according to customer specification. The unit will operate when the operating voltage is within the proper tolerance of the voltage marked on the sticker on the unit. If actual operating voltage is not within tolerance, change the voltage using the selection card on the power supply assembly. Refer to Figure 2-1. Access to the card may be gained by removing the protective shield. The operating voltage displayed is the voltage in effect.

WARNING

Inserting anything other than the voltage selection card into the slot may allow a shock hazard to exist. The inserted end of the card connects raw line voltage to the power supply transformer. Always disconnect the programmer's power cord before changing the voltage selection card.

2.3.3 GROUNDING THE SYSTEM 19

The System 19 power cord contains three conductors as shown in Table 2-2. When the power cord is connected to a three-wire AC power system, the round connector serves to ground the Programmer's chassis and keyboard, eliminating potential shock hazards. If a three-to-two wire adapter is used, connect the ground lead of the adapter to earth (ground) to complete the ground system.

WARNING

Failure to ground the machine may allow a shock hazard to exist.

2.3.4 FUSE ACCESS

There are no fuses accessible to the user. The System 19 has one circuit breaker in line, which acts as the power ON/OFF switch. Other fuse protection is resident on the main board; if any of the latter fuses burn out, a need for service is indicated.

Table 2-2. Conductor Colors by Country/Continent

	US	EUROPE	U.K.
LINE	Black	Blue	Brown
NEUTRAL	White	Black	Blue
GROUND	Green & Yellow	Green & Yellow	Green & Yellow

2.4 PROGRAMMING ELECTRONICS INSTALLATION

2.4.1 THE PROGRAMMING PAK

The programming module installation is shown in Figure 2-2. See the Comparison Chart for selection of the appropriate module.

The System 19 is reset when the power is ON with no programming electronics installed. The display is blank and the beeper emits a quiet tone. RAM data remains intact.

To install the module, slide it into the opening and lower it into position. Press gently on the module to ensure connector mating. The System 19 returns with KEYBD selected.

2.4.2 THE SOCKET ADAPTER

The appropriate socket adapter is installed as shown in Figure 2-3. See the Comparison Chart for selection of the appropriate socket adapter.

Some programming electronics have integral programming sockets and thus do not require socket adapters.

2.5 SERIAL INTERFACE

2.5.1 ACCESS TO THE SERIAL INTERFACE

The status switches, for selecting parity and stop bits, are accessed by removing the programming module and the protective shield. See Figure 2-4 (a). Baud rate selection is accomplished using the rotary switch illustrated in Figure 2-4 (b).

2.5.2 CABLING

The System 19 should be connected to peripherals according to standard RS232C or 20 mA current loop specifications. Refer to Figure 2-5 for proper wiring in specific applications. Table 2-3 describes the functions of the various pins in the interface.

2.6 REPACKAGING FOR SHIPMENT

If the instrument is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by serial number, model number and name.

If the original shipping container is to be used, place the instrument in the container with appropriate packing material and seal the container well, with strong tape. If some other container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

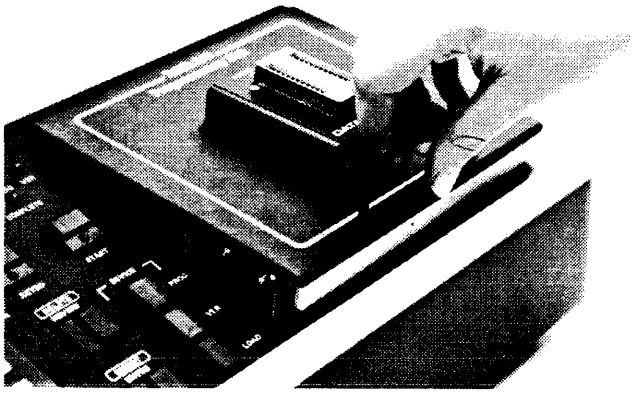


Figure 2-2. Programming Pak Installation

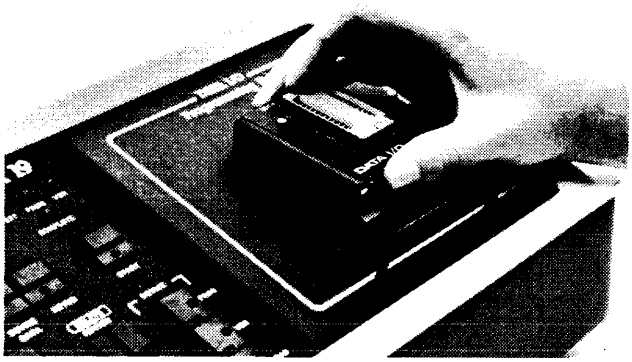
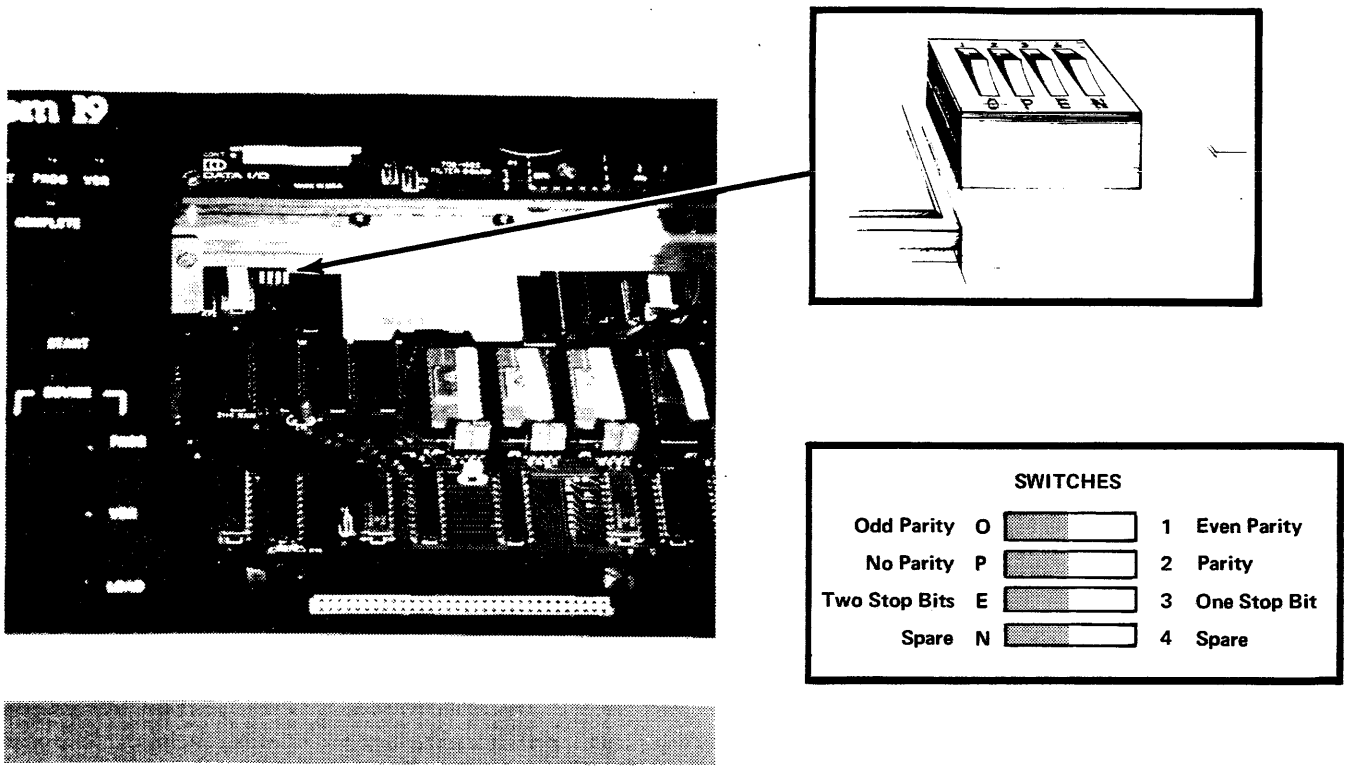
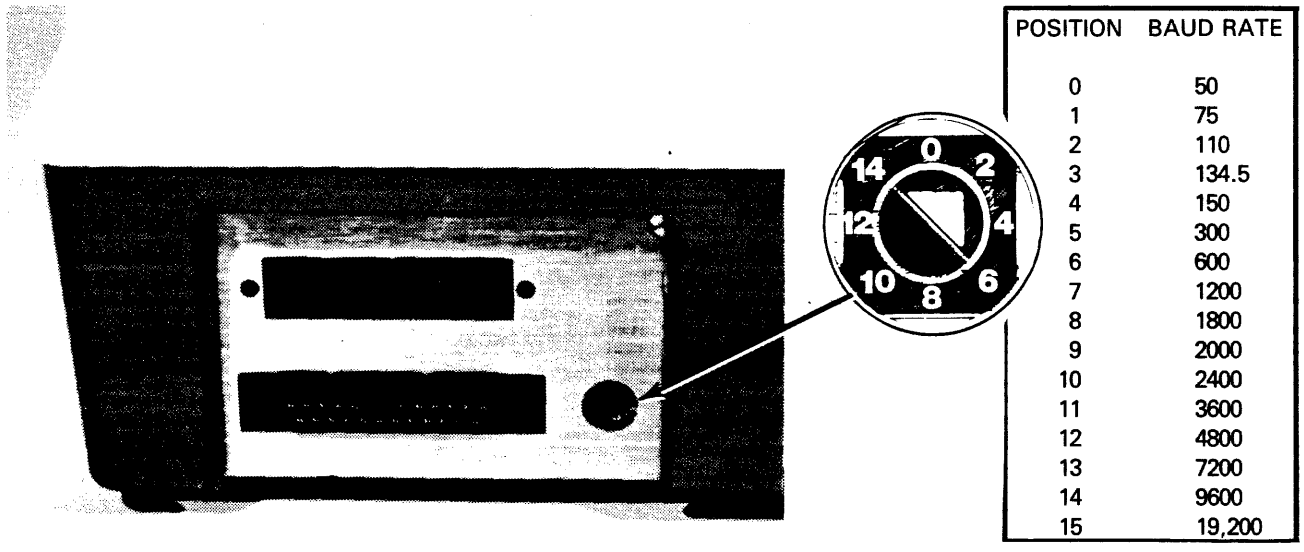


Figure 2-3. Socket Adapter Installation



(a) The status switches on the Controller are used to select parity and stop bits. Remove the programming electronics and protective shield for access to the switches.

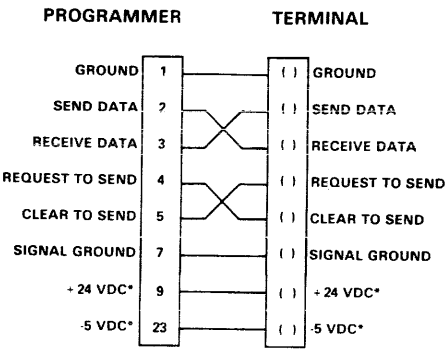


(b) 16 baud rates may be selected using the rotary switch next to the I/O connector on the back panel.

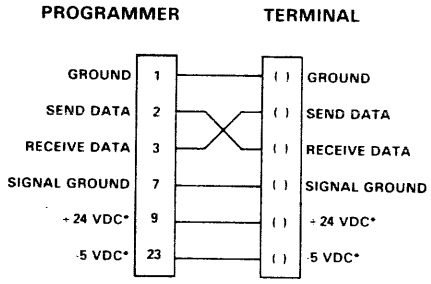
Figure 2-4. Serial-Interface Selection Switches

Table 2-3. Connector Pin Assignment

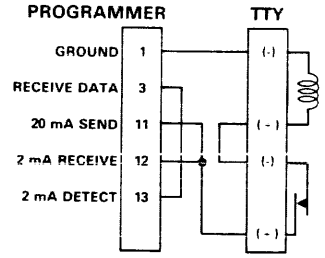
Pin No.	Signal Mnemonic	Description
1	Ground	In the RS232C environment this line is common for the -12 volt source and provides a safety ground connection to the RS232C compatible terminal. In the TTY environment, this -12 VDC signal line provides the signal return for a TTY terminal.
2	Send Data	Transmits data using RS232C voltage levels (+12 V and -5 V).
3	Receive Data	Accepts data using RS232C voltage levels.
4	Request to Send	This line is normally held high by the programmer. It is dropped to inhibit data transmission from the terminal.
5	Clear to Send	A high level on this line allows the programmer to transfer data. A low level inhibits data transfer.
6	Data Set Ready	Connected by internal jumper to data ready (pin 20): simulates indication that the programmer is operating.
7	Signal Ground	This line provides a common signal connection to the RS232C data terminal.
8	Carrier Detect	This line is positive when terminal detects a carrier signal. This line is sampled by programmer if used.
9	+24 VDC	Available for external use if required.
10		Not Used.
11	20 mA Send	Transmits data using 20 mA current loop to TTY peripheral.
12	2 mA Receive	Accepts data using 2 mA current loop from TTY peripheral.
13	2 mA Detect	Presents RS232C voltage level data, with response to data received on 2 mA receive line. For TTY operation, it is tied to receive data line by external jumper.
14		Not used.
15		Reserved for future use.
16-19		Not used.
20	Data Ready	Connected by internal jumper to data set ready. A high level on this line from the RS232C data terminal indicates that the data terminal is ready.
21		Not used.
22	+5 VDC	Available for external use if required.
23	-5 VDC	Available for external use if required.
24		Not used.
25		Not used.



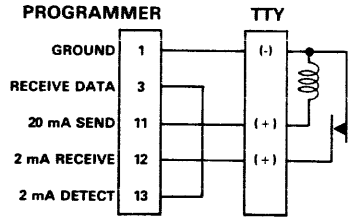
a)RS232 Connection, Half/Full Duplex, with Handshake



b)RS232 Connection, Half/Full Duplex, w/o handshake



c)20 mA Current Loop Connection, Half Duplex



d)20 mA Current Loop Connection, Full Duplex

NOTES:

1. *All signals are named with respect to the originating unit.*
2. *All undesignated pins are to be left open.*
3. *For applications that do not require handshaking, the programmer's clear to send line is pulled up internally.*

Figure 2-5. Serial-Interface Interconnection Methods

SECTION 3
OPERATION

3.1 PROGRAMMING OVERVIEW

The first step in programming any type of device is to prepare the programmer's RAM with data. The source of this can be:

- a master device
- the serial port
- the programmer's keypad

The second step is programming.

3.1.1 PREPARING RAM

Data can be loaded into RAM from a master device, input through the serial port, or entered from the keypad. Loading from a master device is the simplest method. The serial port is useful for entering data from a computer, terminal or microprocessor development system. Key entry is slow, and for this reason the keypad is useful mainly for making changes to data already in RAM.

3.1.2 PROGRAMMING

Programming is the process of actually "burning" the bits into the device. With devices of most types, this is done by applying a high current to burn a fusible link or semiconductor junction. MOS (Metal Oxide Semiconductor) device bits are programmed by repeatedly applying voltage to a "floating" MOSFET gate until the gate is "charged."

The program cycle may be as short as a few seconds for bipolar devices or as long as a couple of minutes for MOS devices.

3.1.3 PROCEDURES

While most Data I/O programming accessories require no special operating considerations, the procedure is occasionally modified by the particular programming electronics you are using. Before attempting any operation with the System 19, examine the *Operation* section of the manual for the programming electronics you will be using. Note any special considerations involving data preparation or device selection.

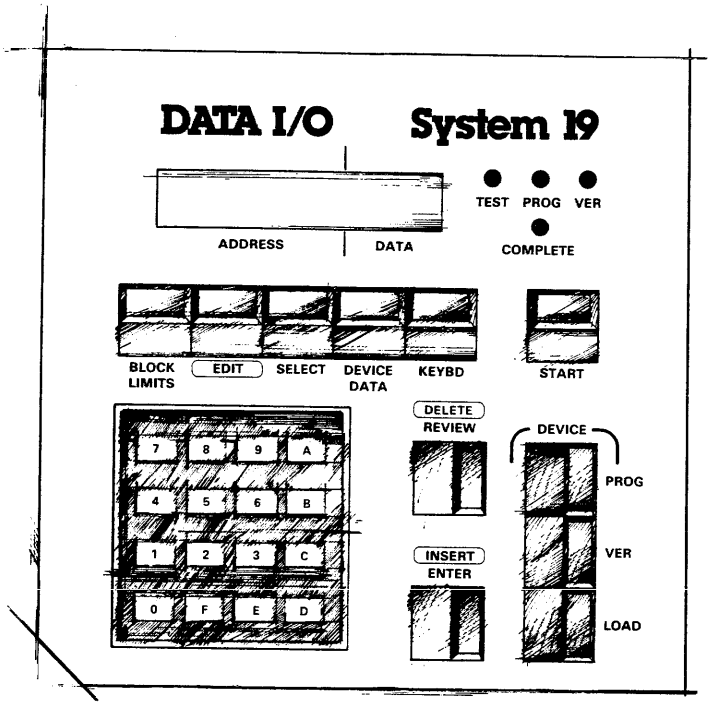


Figure 3-1. Front Panel, System 19

3.2 GENERAL DESCRIPTION

3.2.1 DEFINITIONS

All data transfers or comparisons occur between the programmer's internal RAM and the serial port or the device in the System 19's socket adapter. The following statements define the operations performed:

- Data transfer from the device to RAM is a LOAD operation;
- Data comparison between the device and RAM is a VERIFY operation;
- Data transfer from RAM to the device is part of the PROGRAM operation;
- Data transfer from the serial port to RAM is an INPUT operation;
- Data comparison between the serial port and RAM is an INPUT COMPARE operation;
- Data transfer from RAM to the serial port is an OUTPUT operation

Table 3-1. Control Key Index

KEY	NO.	TITLE
BLOCK LIMITS	3.3.4	Setting BLOCK LIMITS
	3.4.2	Loading a Device into RAM
	3.4.3	Programming a Device
	3.4.4	Device Verification
	3.6.1	Data Manipulation Commands
	3.6.3	Serial Interface Operation Commands
EDIT	3.5.3	Editing Data in RAM
SELECT	3.6	Select Code Operations
	3.6.1	Data Manipulation Commands
	3.6.2	Utility and Inquiry Commands
	3.6.3	Serial Interface Operation Commands
DEVICE DATA	3.4.5	Device Data Key
KEYBOARD	3.5	Keyboard Data Entry
	3.5.1	Keyboard Selection and Address Specification
	3.5.2	Entering Data from the Keyboard to RAM
START	3.4.2	Loading a Device into RAM
	3.4.3	Programming a Device
	3.6.2	Utility and Inquiry Commands
	3.6.3	Serial Interface Operation Commands
REVIEW/ DELETE	3.5.2	Entering Data from the Keyboard to RAM
	3.5.3	Editing Data in RAM
ENTER/ INSERT	3.5.1	Keyboard Selection and Address Specification
	3.5.2	Entering Data from the Keyboard to Ram
	3.5.3	Editing Data in RAM
(DEVICE) PROG	3.4.1	Mode Selection
	3.4.3	Programming a Device
(DEVICE) VERIFY	3.4.1	Mode Selection
	3.4.4	Device Verification
(DEVICE) LOAD	3.4.1	Mode Selection
	3.4.2	Loading a Device into RAM

3.2.2 THE KEYBOARD

Refer to Figure 3-1 or to the front panel of the programmer. The function of each key is described in the relevant paragraphs. These are:

- Paragraph 3.4 for device-related operations.
- Paragraph 3.5 for manual data entry.
- Paragraph 3.6 for input, output and special data manipulations.

Since control key functions have subtle changes when used in different operations, straight definitions of these keys could be misleading. Therefore, Table 3-1 is included to identify the keys by listing them in relation to the various operations. The table serves as an index, with references to paragraphs where the keys are used. Table 3-2 shows the key steps required for several basic operations.

3.2.3 SELECT CODES

Many of the System 19's functions are initiated by alpha-numeric Select Codes. These codes instruct the instrument's software to perform tasks such as RAM data manipulation, I/O functions, and a number of miscellaneous utility operations. Use of these codes is explained in subsection 3.6.

3.2.4 PROGRAMMER RAM

The System 19 is shipped as standard with 4096 8-bit bytes of internal data RAM. This RAM is addressed in hexadecimal notation and occupies addresses in the range Ø to FFF. The RAM may be extended by the addition of an option board with either 4K or 12K of additional RAM. In these cases the last address is 1FFF or 3FFF, respectively. Device addresses are considered to start at Ø and extend to the size of the device. The last device address is numerically one less than the size of the device. Device size is counted starting at one and addresses start with zero. For a device having *n* address lines the last device address is 2^n-1.

The System 19 is informed of the device size and word width by the socket adapter or by the Four Bit or Eight Bit Select Code commands. The word width is always 4 or 8. The programmer RAM takes on the characteristics of the word width indicated by the installed socket adapter. With a 4-bit socket adapter on a standard 4K machine, data entry, manipulation, insertions and deletions occur on only 4 bits of RAM. The remaining RAM (4Kx4) is available as a back-up store. It is also used when assembling 4-bit data into 8-bit form.

3.2.5 TREATMENT OF ERRORS

The System 19 treats similar errors in a like manner. Operating instructions which follow assume operations in which no errors occur. In the event an error occurs, however, the machine will communicate a problem in one of three ways:

- An audible beep will occur whenever an incorrect key is pressed
- An error condition causes five beeps, the display "Err" and an error number. Refer to Appendix 1 for a list of errors and suggested actions. The operation may be repeated after rectifying the problem, or a different operation may be attempted
- The display will flash a response to certain conditions; a beep will also occur. The display and status lights will prompt for a decision by the operator

3.2.6 SUM-CHECK

To ensure the integrity of data transfers, the System 19 calculates a "sum-check" value. This consists of the binary summation of all the data transferred. This calculated value, available after every data transfer, is always the same with the same data. This value should be written on a label

Table 3-2. Synopsis of Basic Key Operations

NOTE: This table does not present optional decisions in key sequences. See the individual operation descriptions.

ENTER DATA

Load
(Master device to RAM)

1. Insert device
2. Press LOAD
3. Press START

Input
(Serial port to RAM)

1. Press SELECT
2. Key in Select Code for data format (optional)
3. Press START
4. Press SELECT
5. Key in Select Code for Input operation
6. Press START

Manual Entry
(Keyboard to RAM)

1. Press KEYBD
2. Key in desired address
3. Press ENTER
4. Key in desired data
5. Press ENTER to advance one address, or press REVIEW to back up one address

EDIT

Insert

1. Press KEYBD
2. Key in desired address
3. Press ENTER
4. Press EDIT
5. Key in the data to be inserted at the displayed address
6. Press INSERT

Delete

1. Press KEYBD
2. Key in desired address
3. Press ENTER
4. Press EDIT
5. Press DELETE

PROGRAM
(RAM to Device)

1. Insert device
2. Press PROG
3. Press START

affixed to a device to be used as a master. Subsequent copies of the master device are certain to be identical if the sum-check value displayed after the load compares with the value on the label.

The sum-check is also useful for Input and Output operations. The chosen data format may not have inherent error detection. Making a note of the sum-check value will ensure that future transfers are successful. These procedures will help guard against incorrect data caused by damaged or erased devices, line noise or other problems when using a remote data base. The sum-check appears in the address display with all the decimal points ON.

3.2.7 INTERNAL RAM DATA INTEGRITY CHECK

The foregoing description of sum-check is not to be confused with the internal RAM data integrity check maintained by the System 19. This is a value calculated in a way similar to sum-check, but extending over the whole of RAM. This value is used to continously monitor the RAM memory. If a change in data contents occurs for any spurious reason, such as memory failure or power outage, the operator is immediately informed.

3.2.8 DATA LOCK

The System 19 has a data lock feature to protect the data in RAM for a series of identical programming operations. While data lock is in effect, keys used to

manipulate data are disabled. The only possible operations are:

- Program
- Verify
- Abort Program in process (using the KEYBD key)
- Release data lock

Depression of any disabled key causes an error reminder.

Changing the programming module is allowed; the programmer displays an error message to remind the operator that RAM data is being preserved.

The data lock is engaged with a Select Code (Table 3-3), using the Utility and Inquiry Command procedure in paragraph 3.6.2.

The following key sequence is the pass code for releasing the data lock.

a. Press SELECT (the display shows a "P").
b. Press EDIT.
c. Hold the DEVICE DATA key while pressing REVIEW.

3.3 PREOPERATIONAL PROCEDURES

CAUTION

Follow the procedures as written in the following paragraphs to avoid damage to the System 19 or devices to be programmed.

3.3.1 TURN-ON

CAUTION

Make sure that foreign objects do not obstruct airflow through the programmer's cooling fan.

With the System 19 disconnected from any power source, make sure that the present operating voltage is correct. Refer to paragraph 2.3.

Install programming electronics per the procedure in paragraph 2.4.

CAUTION

Voltage transients can cause device damage. Be sure all sockets are empty when switching power ON and OFF and when changing programming electronics.

Turn ON the System 19 with the switch at the rear. A self-test procedure is automatically performed. The System 19 considers itself functional when the TEST and COMPLETE lights are illuminated. The size of the RAM is displayed in the address field.

3.3.2 PROGRAMMING ELECTRONICS

Make sure the correct programming electronics are installed for the device to be used. Refer to the Data I/O Comparison Chart or the programming electronics manual for specific information on applicability of programming hardware. Check the *Operation* section of the programming electronics manual in particular to determine whether there are any special procedures you need to be aware of.

Installation may be accomplished with the System 19 power ON. This feature allows RAM data to remain intact while changing types of devices. With the programming electronics removed, the unit will sound a continuous quiet tone. When new programming electronics are installed, the programmer returns with KEYBD selected. If data retention is not desired, it is suggested that power be turned OFF when changing programming electronics.

3.3.3 DEVICE INSERTION

A good electrical connection between the device and socket is essential; the device pins must be clean and undamaged. Insert the device in the socket with the lever in the upright position. Ensure that pin 1 of the device is adjacent to the dot on the socket adapter. Lock the device in the socket by pushing the lever down.

CAUTION

Never insert or extract a device from the socket when the START light is ON.

3.3.4 SETTING BLOCK LIMITS

In some cases, it is helpful to perform a partial data transfer. The System 19 can move a block of data (several adjacent bytes) from one RAM location to another (RAM-RAM Block Move), between a device and RAM, and between RAM and the I/O port. The block size and location are defined by BLOCK LIMITS. There are three such limits, designated L1, L2 and L3.

- L1 is the Begin RAM Address (RAM-Source Address when used in a RAM-RAM Block Move). This is the first RAM address to or from which data will move in I/O or device-related operations. The default value is Ø. L1 may be specified alone or in conjunction with L2 and/or L3.

- L2 is the number of bytes (block size) to be transferred. L2 has different default values, depending on the operation involved. For device-related operations, L2 defaults to the word limit of the programming electronics. For I/O operations, L2 defaults to the value of the difference between L1 and the total RAM size. For RAM-RAM block moves L2 has no default value; it must be specified. In any case, L2 must be greater than Ø, if not allowed to default. L2 can be specified alone, or in conjunction with L1 and/or L3. If L1 is changed after L2 has been set, L2 must be respecified.

- L3 is the Begin Device Address (RAM-Destination Address when used in a RAM-RAM Block Move). This is the first address to or from which data will be transferred in device-related operations. The default value is Ø. L3 is not specified for I/O operations.

To specify L1, L2 and L3:

a. Press BLOCK LIMITS. The data display will show "L1".

b. Key in the desired Begin RAM Address (or RAM Source Address for RAM-RAM Block Moves). This value will appear in the address display.

c. Press ENTER. The data display will show "L2", and the BLOCK LIMITS keylight will come ON.

d. Key in the number of bytes to be moved. This value will appear in the address display.

e. Press ENTER. The data display will show "L3".

f. Key in the Begin Device (or RAM Destination, for the RAM-RAM Block Moves) Address. This value will appear in the address display.

g. Press ENTER. The limits are now in effect, and you are ready to select and initiate the desired transfer.

NOTE

When using BLOCK LIMITS to establish a limited Program operation for 3-voltage MOS PROMs, L2 must be a minimum of 16 bytes. Otherwise, the device to be programmed may be damaged by excessive heat.

So long as the BLOCK LIMITS keylight is ON, the specified limits remain in effect. If no limits are desired, be sure that the BLOCK LIMITS light is OFF. The limits are nullified when you press the BLOCK LIMITS key again or shut OFF the programmer.

3.4 DEVICE RELATED OPERATIONS

3.4.1 MODE SELECTION

Press the PROG, LOAD or VER key. A light on the key indicates a selection has been made. Press the START key to initiate the selected operation. The START light on the START key is ON during execution. All data transfers or comparisons occur between RAM and the device in the socket.

The operation is complete when the COMPLETE status light is ON. This is accompanied by the START light going OFF.

Any errors during execution are communicated by the display of an error number. See Appendix 1 for error descriptions by number.

NOTE

To reset the programmer while an operation is in progress or during an error condition, press the KEYBD key.

Any decisions required of the operator are prompted by a flashing display.

3.4.2 LOADING A DEVICE INTO RAM

Follow the preoperational procedures of paragraph 3.3 and then proceed as follows:

a. Set the BLOCK LIMITS if required (para 3.3.4).

b. Ensure that the device is correctly inserted in the socket.

c. Press the LOAD key.

d. Press the START key.

The device data at the Begin Device Address (L3) is stored into RAM at the Begin RAM address (L1). Subsequent words are stored into sequential RAM locations until specified number of bytes (L2) has been transferred.

The START light will go OFF and the COMPLETE light will come ON to indicate that the System 19 is ready for the next operation.

The address display shows the sum-check value for the data just loaded. If the whole device was loaded, this should be compared to the previously recorded value on the device label. If there is no sum-check value on the device, refer to paragraph 3.2.6 for information on how to ensure valid data transfers.

With most programming electronics, the load operation performs a transfer from device to RAM with nominal values of voltages and load. This enables pin-compatible devices to be loaded with an incorrect programming module. The Verify operation performs worst case testing. Do not assume that a device that was loaded successfully will verify correctly. The sum-check feature should be used to ensure data integrity.

3.4.3 PROGRAMMING A DEVICE

Follow the preoperational procedures in subsection 3.3, and then proceed as follows:

a. Set the BLOCK LIMITS if required (para 3.3.4).

b. Ensure the device is correctly inserted in the socket.

c. Press the PROG key.

d. Press the START key.

During the programming procedure the START light

will be ON, and the status indicators will show which stage of the automatic programming sequence is in effect.

The System 19 will always indicate errors as they occur. To indicate continuous operation the data display will show an action symbol.

Status indicators during the automatic programming sequence are as follows:

- **TEST light ON.** The System 19 is performing an illegal bit test and a blank check of the device in the socket. If the display flashes in this condition then the device is not blank. The RAM address and data corresponding to the first nonblank device address are displayed. Holding down the DEVICE DATA key causes display of the corresponding device address and data. If the nonblank condition is acceptable, press START to continue to the next stage of the programming sequence.

- **PROGRAM light ON.** The device is being programmed with data from RAM. The data display will show an action symbol to reassure the operator that the System 19 is operating. This stage may take several minutes, depending the type of device being programmed.

- **VERIFY light ON.** The System 19 compares every device data word with the corresponding RAM data. If any mismatch occurs, then an error message will be displayed. When the whole device has been verified, the COMPLETE light will come ON. Also, certain parametric voltage checks are made of the device during this verify sequence. For details, see the programming electronics manual. For further information on any of the verify errors, perform the VERIFY operation. See paragraph 3.4.4.

- **COMPLETE light ON.** If there were no verify errors the address display will show the sum-check value. The data display will show a decimal count of the devices programmed since power ON or the last Clear Device Counter command. See Table 3-3.

3.4.4 DEVICE VERIFICATION

a. Follow the preoperational procedures in paragraph 3.3.

b. Set the BLOCK LIMITS (para 3.3.4) if required.

c. Ensure that the device is correctly inserted in the socket.

d. Press the VERIFY key.

e. Press the START key.

During verification, the START light will be ON.

The programmer performs a comparison of the device data against the RAM data. A mismatch will cause the display to flash with the RAM address and data displayed. Depression of the DEVICE DATA key causes display of the corresponding device address and data. Verification will continue upon depressing START. The display will flash and show the address and RAM data at every mismatch.

After the device has been verified, the START light is OFF and the COMPLETE light is ON. The address field shows the sum-check of the data in the device. The sum-check will not be displayed if there were any verify errors.

NOTE

Some programming modules perform a two-pass verify sequence. In this case, mismatch addresses may be displayed two times.

3.4.5 DEVICE DATA KEY

Whenever the System 19 displays a RAM address and data, it is possible to examine the equivalent device address and data. Holding down the DEVICE DATA key will cause the display of the data at the device address that corresponds to the displayed RAM address. The device address is only equal to the RAM address when the Begin RAM Address (L1) and the Begin Device Address (L3) are equal.

3.5 KEYBOARD DATA ENTRY

Data may be entered from the keyboard in hexadecimal notation. It is possible to jump to an address and step forward or backward. The data at the displayed address may be changed or deleted, or new data may be inserted at the displayed address.

- **Change.** Data at the displayed address is lost. New data from the keyboard is stored at that address. No other addresses are affected.

- **Delete.** Data at the displayed address is lost, and the data from each higher address is moved down one address, filling the vacancy. The highest address is filled with zero.

- **Insert.** All the data from the displayed address to the highest memory address is moved up one location. The inserted data is stored at the displayed address. The data at the highest RAM address is lost.

3.5.1 KEYBOARD SELECTION AND ADDRESS SPECIFICATION

a. Follow the preoperational procedures in paragraph 3.3.

b. Press the KEYBD key. The light on the key verifies that the keyboard has been selected, and the address display shows the address in RAM at which keyboard operation will occur.

c. If the address is acceptable, press ENTER. The RAM data at the address is displayed.

d. If the address is not acceptable, key in a new address between zero and the maximum RAM address; if the value was incorrectly keyed, press KEYBD to start again; if the value was correctly keyed, press ENTER. If an out-of-range address has been keyed in, pressing the ENTER key will cause an audible beep.

3.5.2 ENTERING DATA FROM THE KEYBOARD TO RAM

a. Select keyboard operation at the desired address (para 3.5.1).

b. To advance from the displayed address to a higher address, press ENTER. The displayed address increases by one each time ENTER is pressed.

c. To advance from the displayed address to a lower address, press REVIEW. The displayed address decreases by one each time REVIEW is pressed.

d. Change data at any address by keying in a new value. The right-hand decimal point will be ON whenever data has been keyed in. This data must be either accepted or rejected.

e. To accept the data, press ENTER. The data is accepted and the address is advanced by one. Or, press REVIEW. The data is accepted and the address is decreased by one.

f. To reject the data (because of keying errors), press KEYBD. The data field will go blank. Pressing ENTER at this time displays the original data.

All other keys are inoperative while the right-hand decimal point is ON; pressing them will merely cause a beep to inform the operator that he has attempted an illegal operation.

3.5.3 EDITING DATA IN RAM

With an address and data displayed the EDIT key may be pressed. This key redefines the functions of the ENTER and REVIEW keys. The ENTER key is now the INSERT key, and the REVIEW key is now the DELETE key.

To INSERT data at an address, first set that address by pressing the KEYBD key, keying in the address of interest, and pressing ENTER. Then proceed as follows:

a. Press EDIT. The keylight comes ON, confirming that an EDIT is occurring.

b. Key in the data to be inserted at the displayed address. If a mistake is made, press EDIT and start again. If the data is correct, continue.

c. Press INSERT. The new data is inserted at the address of interest, and the display shows the next higher address. The data which was previously at the address of interest is now at the new displayed address. In a like manner, all data above the inserted data has moved up one address. Data which was in the highest possible RAM address has been lost.

Steps "b" and "c" may be repeated as required.

To DELETE data at an address, first access the address by pressing the KEYBD key, keying in the address of interest, and pressing ENTER. Then, proceed as follows:

a. Press EDIT. The light on the key comes ON, confirming that an EDIT is occurring.

b. Press REVIEW. The data at the address is deleted. The data from the next higher address is moved down and displayed, and the data from all higher addresses move down one address. The highest address is filled with zero. Successive depressions of the DELETE key cause further deletions. To escape EDIT, press KEYBD.

3.6 SELECT CODE OPERATIONS

The SELECT key is used to access a range of operations. Each operation has a unique Select Code. Those codes available in a standard System 19 are listed in Table 3-3 of this manual. Select codes for other capabilities are covered in supplementary manuals.

Select Code commands fall into three groups:

- Data manipulation commands.
- Utility and inquiry commands. These are used both for selecting data translation formats and for setting or examining machine parameters.
- Serial interface operation commands.

Pressing the SELECT key informs the System 19 that a Select Code command is to follow. Some Select Codes require additional parameter specification as given in Table 3-3. The following paragraphs give the key sequence for each type of command.

NOTE

Press SELECT again after miscuing a Select Code, and enter the correct code.

3.6.1 DATA MANIPULATION COMMANDS

a. Set BLOCK LIMITS, if required (para. 3.3.4)

b. Press SELECT. The display shows the mnemonic "SEL" in the otherwise blank display.

c. Key in the desired Select Code (Table 3-3).

d. Press ENTER.

Table 3-3. System 19 Select Codes

NOTE

Additional Select Codes associated with optional programmer capabilities are covered in the option manuals bound in the back of this cover.

CODE	NAME	PARAMETER (Default Value)	DESCRIPTION
		A) Data Manipulation Commands	
A1	Swap Nibbles	—	Exchanges high- and low-order halves of every word in RAM.
A2	Fill RAM with Variable	Variable (Ø)	Fills memory upward from current keyboard address with the value specified after ENTER.
A3	Complement Memory	—	Performs the ones complement of 4 or 8 bits of each word as determined by the word size in effect.
A4	Clear RAM	—	Clears all of RAM to zeros.
A5	Split RAM Data	Center Point (RAM Midpoint)	Complement of Shuffle (A6). This command "splits" odd- and even-addressed bytes in RAM about a specified center point, dividing them into two adjacent blocks occupying the same original amount of RAM. Center point must be some power of 2 between Ø and RAM midpoint.
A6	Shuffle RAM Data	Center Point (RAM Midpoint)	Complement of Split (A5). This command merges or "shuffles" the block of RAM addresses immediately above the center point with the block below, placing the lower-block bytes at even-numbered addresses starting at Ø and the upper-block addresses at odd-numbered addresses starting at 1. Center point must be some power of 2 between Ø and RAM Midpoint.
A7	RAM-RAM Block Move	—	Moves block of data beginning at a specified address (L1) to a new location, beginning at a second specified address (L3). BLOCK LIMITS must be set. See paragraph 3.3.4.
		B) Utility and Inquiry Commands	
BØ	Device Size	—	Displays the number of device words and the word width.
B1	RAM Sum-check	—	Displays the check of all RAM data.
B2	Configuration Number	—	Displays a unique number to identify the software configuration revision level.
B3	Format Status	—	Programmer displays three 2-digit numbers. From left to right: 1. The select Code of the format in effect 2. The hex number of nulls selected 3. The hex number of bytes per output record selected.
B5	Input Compare Error Count	—	Displays the decimal number of input compare errors.
B6	Input-Buffer Overflow Errors	—	Displays the decimal number of characters received by the serial-input port buffer after the programmer sent a stop signal to the sending instrument.
B9	Display Test	—	Lights all the display LED's.
CØ	Calibrate OFF	—	Deselects calibration software.

Table 3-3. Continued

C1	Calibrate ON	—	Selects calibration software for calibration of programming modules which lack resident calibration software.
C2	Calibrate ON	—	Selects calibration software resident on those programming modules which contain it.
FØ	Clear Device Counter	—	Clears the count of program operations since power ON or the last FØ command.
F3	Data Lock	—	Protects RAM data for repeated programming operations. Paragraph 3.2.8 explains the data lock and its release pass-code.
F4	4-Bit Word	—	Selects a 4-bit word size to override 8-bit programming electronics.
F8	8-Bit Word	—	Nullifies the "4-Bit" command. Allows the programming electronics word size to take effect.
F9	Disable Timeout	—	Disables the 25 second I/O timeout.

C) Serial Interface Operation Commands

FA	ASCII Character Output	ASCII Character Hex Code (no default)	After this code is entered, key in the hex code for an ASCII character and press START. The character is transmitted from the serial port each time START is pressed.
DØ	Output (With Remote Control)	Address Offset (Ø)	Prepares the programmer to output data on receipt of X-ON character, DC1 (Control Q), from remote instrument. Programmer will halt operation when remote instrument sends X-OFF character, DC3 (Control S).
D1	Input	Address Offset (First Input Address)	Initiates the input of data to RAM via the serial port.
D2	Input (With Instrument Control)	Address Offset (First Input Address)	Initiates the input of data to RAM via the serial port. THe machine outputs the X-ON character, DC1 (Control Q), to start the remote instrument, and outputs the X-OFF character, DC3 (Control S), to stop the instrument.
D3	Compare	Address Offset (First Remote Address)	Initiates comparison of RAM data with data presented at the serial port.
D4	Compare (With Instrument Control)	Address Offset (First Remote Address)	Initiates the comparison of RAM data with data presented at the serial port. The machine outputs the X-ON character, DC1 (Control Q), to start the remote instrument, and outputs the X-OFF character, DC3 (Control S), to stop the instrument.
D5	Output	Address Offset (Ø)	Initiates data output from the programmer.
D6	Output (With Instrument Control)	Address Offset (Ø)	Initiates data output from the programmer. The programmer outputs the punch-on character, DC2 (Control R), prior to data transfer and the punch-off character, DC4 (Control T), on completion.
D7	Output Nulls	—	Sends 50 nulls from the serial port.
D8	Select Record Size	—	Changes the number of bytes per output record. The keyed-in number must be in hex notation.
D9	Set Nulls	Number of Nulls (1)	Allows selection (in hexadecimal notation) of up to 254 nulls (FE) following each data record. Selecting 255 (Hex FF) sends no nulls and no line feed.

e. Key in parameters as required.

f. Press START.

3.6.2 UTILITY AND INQUIRY COMMANDS

a. Press SELECT. The display shows the mnemonic "SEL" in the otherwise blank display.

b. Key in the required Select Code (Table 3-3).

c. Press ENTER or START.

1. ENTER causes the data in the address display to show the default value of a parameter used by the operation. Key in a new value if the default is not acceptable.

2. START executes the desired function.

3.6.3 SERIAL INTERFACE OPERATION COMMANDS

a. Set BLOCK LIMITS, if required (para 3.3.4).

b. Press SELECT.

c. Key in the desired Select Code (Table 3-3).

d. If an address offset is desired, (See subsection 3.7) press ENTER. If no address offset is desired, skip this step. The display will show the default value for the address offset value if the format specified has an address field. If the default value is not correct, key in the desired value. If no address offset is desired, skip step d.

e. Press START.

3.7 I/O ADDRESS CONTROL

Address control:

- Address offset — adjusts RAM addresses to addresses expressed in a larger memory.
- Begin RAM (BLOCK LIMIT L1) — defines the first address in RAM to or from which data is to be transferred.
- Block size (BLOCK LIMIT L2) — defines the number of bytes to be transferred.

3.7.1 ADDRESS OFFSET

Although the programmer is capable of recognizing addresses up to 65K (FFFF), the programmer RAM is not this large. Therefore, when larger-than-RAM address are input, it is necessary to redefine them to be within the programmer RAM address limits. Similarly, to output larger addresses, programmer RAM addresses must be redefined. This can be done by specifying an address offset in the I/O operation command.

The address offset is subtracted from all addresses input to the programmer and is added to all addresses output from the programmer. The address offset defaults to the value of the first incoming address on input; in essence, the programmer sees the first data byte as having address Ø. On output, the offset defaults to Ø; the first data byte output will have address Ø.

3.7.2 BEGIN RAM ADDRESS AND BLOCK SIZE

BLOCK LIMITS can be used to specify the first RAM address to or from which data will be transferred in an I/O operation (L1), as well as the number of bytes to be transferred (L2).

On **input**, L1 is the address where data storage will begin. Subsequent bytes will be stored at successively higher addresses up to the limit set by L2.

On **output**, L1 is the RAM location of the first byte to be output. Data will be output from successively higher addresses until the specified number of bytes (L2) have been output.

3.7.3 ADDRESS OFFSET AND BEGIN RAM INTERACTION

After the address offset is subtracted from the incoming address, the resulting difference is added to the Begin RAM Address (L1) to determine the RAM location where that data byte will be stored. If the address offset is allowed to default, the first input byte will be stored at the Begin RAM address. Subsequent bytes are stored at successive RAM addresses. Stated algebraically:

$$A_S = L1 + (A_I - AO)$$

where

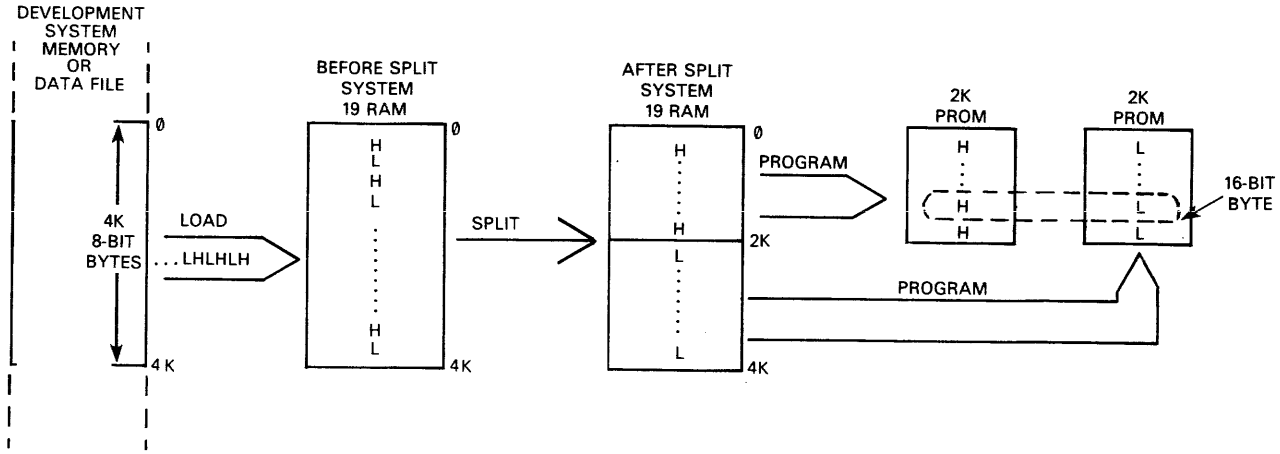
A_S = RAM address where the data byte will be stored

L1 = Begin RAM Address

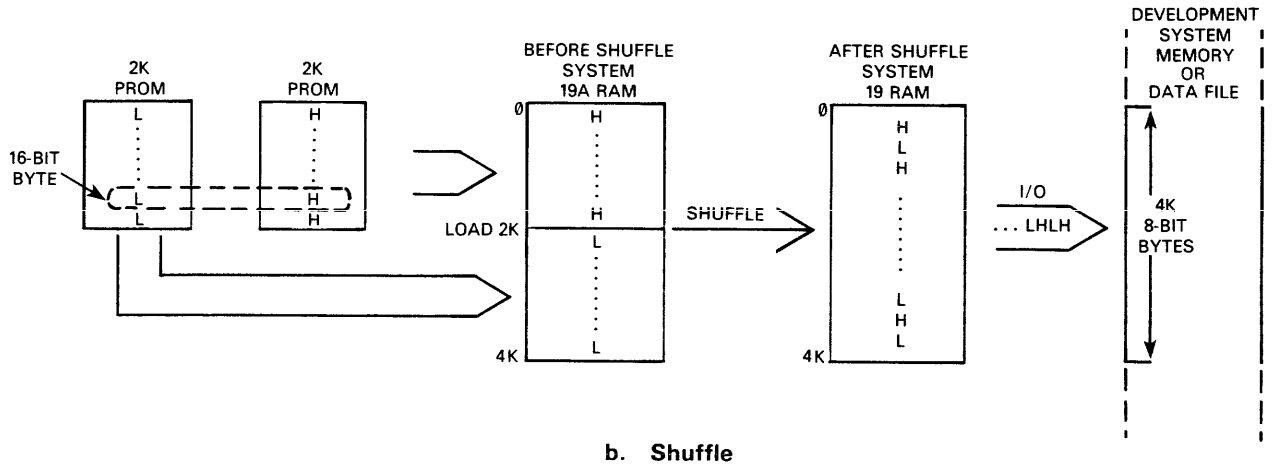
A_I = input address of the first data byte

AO = address offset

On output, L1 and the address offset are independent of each other. L1 determines the RAM location of the first data byte to be output. The address offset alone determines the address to be transmitted with that data byte. Subsequent bytes are addressed accordingly.



a. Split



b. Shuffle

Figure 3-2. 16-Bit Data

3.8 16-BIT MICROPROCESSOR DATA

Data for 16-bit microprocessors can be edited and programmed into PROM with the System 19. 16-bit data is commonly stored in two parallel-addressed 8-bit PROMs, designated "High Order" and "Low Order". When data for 16-bit processors is input through the serial port as pairs of 8-bit words, it must be split into high- and low-order blocks of 8-bit words for programming. This is done with the "Split" Select Code. When PROMs containing high- and low-order half words are loaded to the machine for transmission through the serial port, these data blocks must be recombined into a single block of alternating high- and low-order 8-bit words. This is done with the "Shuffle" Select Code.

3.8.1 SPLIT

16-bit data is loaded into RAM through the serial port in a development-system format as high- and low-order pairs of 8-bit words. Each pair will occupy two adjacent RAM addresses with even numbered addresses containing one half of each pair and odd-numbered addresses containing the other. (See Figure 3-2a.)

Select Code A5 is used to split the odd and even address words into two blocks. Note that words located in even-numbered addresses will be stored in one block, below the specified center point, and words in odd numbered addresses will be stored in a second block above the center point.

To split data:

a. Press SELECT.

b. Key in A5.

c. Press ENTER.

d. Key in the center-point value. This must be some power of 2. Typically, this center point will be the size of the devices you are programming. The default value is the center point of RAM.

e. Press START. The COMPLETE light coming ON indicates that the split has been accomplished, and the data is now ready to be programmed into PROMs, one each for the high- and low-order blocks.

3.8.2 SHUFFLE

To shuffle data, that is to load it from two PROMs, re-match high- and low-order word pairs, and transmit it through the serial port:

a. Be sure the BLOCK LIMITS key light is OFF.

b. Insert the first PROM into the socket.

c. Press LOAD.

d. Press START. The COMPLETE light coming on indicates that data from the PROM is now stored in RAM. The size of the device will determine your center-point value and Begin RAM Address. The latter must be specified before loading the second PROM.

e. Press BLOCK LIMITS. "L1" will appear in the data display.

f. Key in the Begin RAM Address. (the device size or a power of it).

g. Press ENTER. (L2 and L3 need not be specified.)

h. Insert the second device.

i. Press LOAD.

j. Press START. The COMPLETE light coming on indicates that data from the second PROM is now stored in RAM, beginning at the Begin RAM Address.

k. Press BLOCK LIMITS to cancel the Begin RAM Address.

l. Press SELECT.

m. Key in A6.

n. Press ENTER.

o. Key in the center-point value. This will be the same as the Begin RAM Address.

p. Press START. The COMPLETE light coming on indicates that the data has been shuffled and is now ready to be transmitted through the serial port.

If the high-order PROM is loaded first, then the pairs of words will be transmitted through the I/O port high-order first, and vice-versa.

Note that for either of the above operations, RAM size must be at least twice the number of 16-bit microprocessor words to be handled.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration of the System 19, limited to checking and adjusting the power supplies, is normally performed as part of the calibration of a Programming Pak; proper card set operation depends on system power supplies. See the System 19 Calibrator Manual, 025-1521, and the appropriate Program Card Set Manual for complete card set calibration instructions. This section explains calibration of the System 19 power supplies without a calibration fixture.

4.2 EQUIPMENT REQUIREMENTS

- Digital Voltmeter (DVM): Fluke Model 3000A, or equivalent.
- Potentiometer adjustment tool.
- Jumper wire approximately 12 inches in length.

4.3 POWER SUPPLY MEASUREMENT

The System 19 power supplies can be calibrated without the Universal Calibrator using the alternate test points shown in Table 4-1.

a. Ground the DVM to the programmer chassis.

b. Jumper TP4 to ground.

c. Measure the supplies according to Table 4-1, using Figure 4-1 to locate test points.

4.4 ADJUSTMENT PROCEDURE

To make any necessary adjustments:

a. Turn OFF the power and unplug the programmer. Remove calibration equipment, if installed.

b. Remove the cabinet per paragraph 5.2. Remove the option card located under the front panel.

c. Remove the front panel by taking out the four flat head screws in the corners, plus the two screws holding the center brace to the power supply assembly and base.

d. Disconnect the front panel cable and set the front panel aside.

e. Apply power.

CAUTION

Extreme care is required to avoid short-circuiting discrete components while making measurements and adjustments.

f. Adjust the supplies according to Table 4-1, using Figure 4-1 to locate adjustments.

If any supply cannot be adjusted within the tolerances of Table 4-1, refer to the Troubleshooting portion of this manual (Section 6).

Table 4-1. Calibration Voltages, Power Supply

Supply Test	Min	Nom	Max	Adjust	Alternate Test Points, 1520 Controller
+5V Supply	5.10	5.12	5.14	R18	+5
+24V Supply	23.5	24.0	24.5	R26	+24
+48V Supply	49.4	49.7	49.8	R24	+48
-9V Supply	-9.5	-9.0	-8.5	R40	-9
+PROG V Supply[2]	4.9	5.0	5.1	N/A	+PROG

[1] Alternate test points for measuring supply without a Universal Calibrator are located on the Controller, 702-1520. Refer to Figure 4-1 for locations.

[2] If adjustment is required, ground the right side of R63 on the Controller, 702-1520. Use R30 to adjust PROG V to $+21.6 \pm 0.2$ volts.

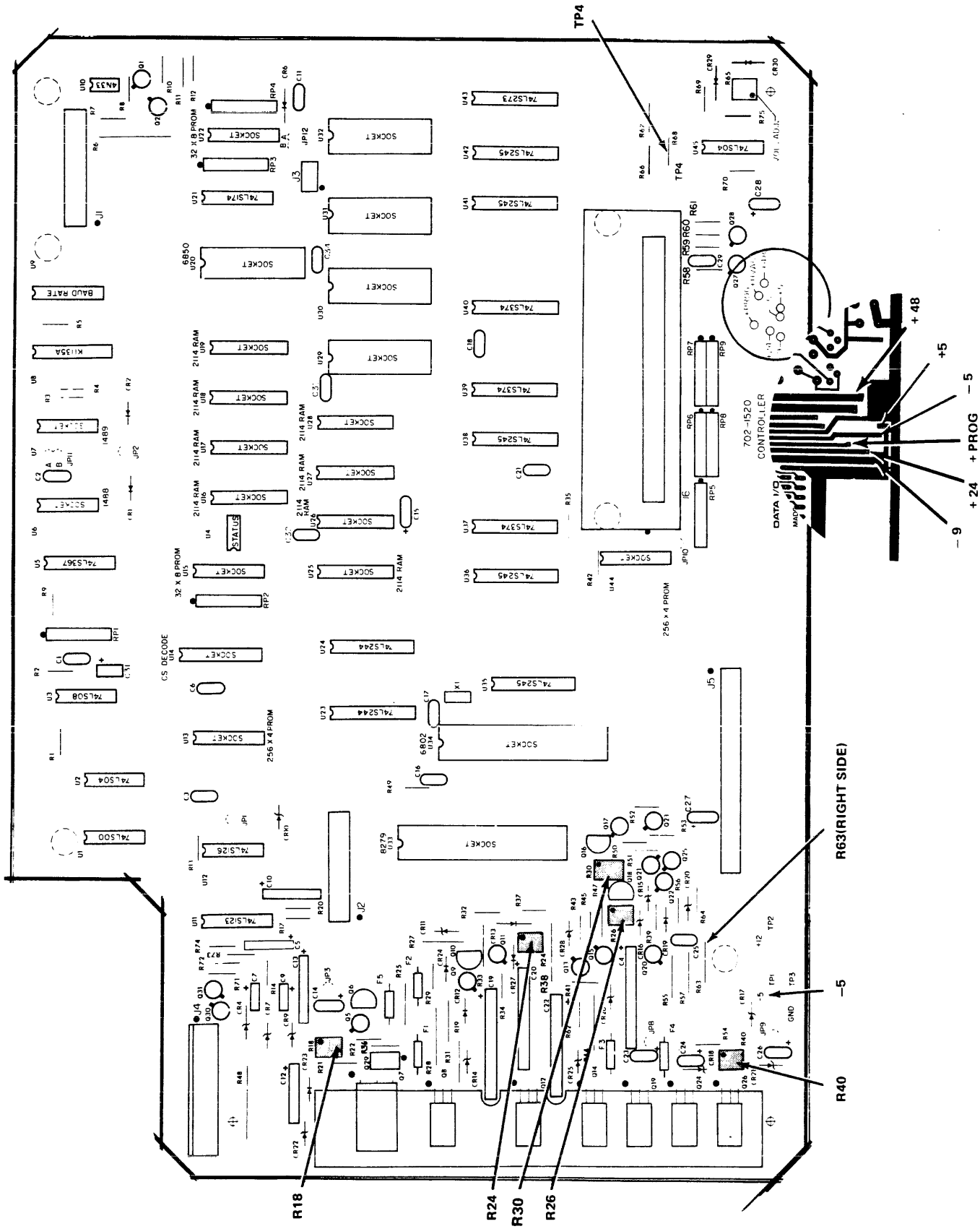


Figure 4-1. Adjustment Test Locations, 1520 Controller

SECTION 5
MAINTENANCE

5.1 INTRODUCTION

The primary maintenance requirement is for periodic cleaning of the fan filter on the System 19. The interior of the machine should also be cleaned as necessary.

CAUTION

Avoid operating the System 19 with the cover removed. The cover serves to direct airflow for cooling, as well as to protect the unit against dust and damage.

5.2 COVER REMOVAL

Turn the power OFF and disconnect the power cord. Remove the four screws at the corners of the base. Remove the cover.

5.3 CLEANING

5.3.1 GENERAL CLEANING

Clean the unit with a mild detergent on a damp cloth or brush. Use a cotton-tipped swab for reaching cramped areas such as the component side of circuit boards.

CAUTION

Do not use caustic or abrasive agents; these will damage the System 19.

5.3.2 CLEANING THE FAN FILTER

Clean the fan filter (located on the top of the unit) every three months with normal usage, and up to twice a month with heavy usage. Remove the filter by plucking it out from its recess. Clean the filter in running water to rinse out accumulated dust. Dry it thoroughly before reinstalling. Reinstall the filter by pressing it back into its recess, first one side and then the other.

5.4 INSPECTION

Periodic inspection of the System 19 can be a hedge against malfunction. A good time to schedule inspection is before every calibration. Check cable connections, card seating, mounting of discrete components, etc., for shorts, opens or unstable continuity.

Particular care is required if heat damaged components are found. It is important to find and correct the cause of overheating, in order to prevent recurrence of the damage.

SECTION 6
TROUBLESHOOTING

6.1 INTRODUCTION

The following troubleshooting information is an aid to interpreting malfunctions and locating hardware failures in the System 19. Section 6.2 gives the procedure for establishing the type of trouble in the unit, and the steps needed for further servicing. Section 6.3 directs the service technician to the portion of the circuitry implicated when the machine displays a hardware error condition. Specific components are not isolated for the repair of such condition; however, the information in this section, along with normal troubleshooting and service techniques, should lead to the solution of most hardware failures.

Section 7, "Circuit Description," and Section 8, "Schematics," provide additional information useful in troubleshooting. Reference to the calibration instructions of Section 4 also is frequently required. Table 3-3 contains Select Codes which may assist during troubleshooting.

After successful troubleshooting, perform a complete calibration of the System 19 per Section 4.

6.2 PRELIMINARY TROUBLESHOOTING

After each of the following steps, confirm that the fault still exists.

6.2.1 NO INDICATION OF OPERATION OR SYSTEM PERFORMANCE ERRATIC

a. Check AC power selection against the working voltage.

b. Check that the Programming Pak is fully seated in the socket. Pin HH of J6, TP4, must be grounded by the Pak or a clip lead.

c. Remove any serial interface connectors.

d. Check the power supplies according to the calibration procedure in section 4.2. If a problem is revealed, refer to paragraph 6.3.1.

e. Check installation of hardware. Check cable orientation and connection as well as seating of the PC boards, and check that jumpers JP3, JP8, and JP9 are installed on 702-1520.

f. Check the Controller as described in paragraph 6.3.2.

g. If steps "a" through "f" do not reveal the problem, contact your Data I/O Service Center.

6.2.2 SERIAL INTERFACE OPERATION FAILURES

a. Check for proper installation of the serial interface according to section 2.5.

b. Verify the operation of the peripheral equipment per manufacturer's procedures.

c. Refer to the serial interface circuitry trouble-shooting portion of this section (para 6.3.3).

6.3 TROUBLESHOOTING SPECIFIC AREAS

6.3.1 POWER SUPPLIES

Portions of the power supply employ foldback over-current protection. If a supply becomes overloaded, it will remain OFF, even after the overload is eliminated. The protection circuits can be reset by turning the programmer's power switch OFF for 30 seconds and then ON again.

If one of the power supplies is at the wrong potential and cannot be adjusted, refer to Table 6-1 to locate the circuitry causing the problem. Check the components listed in this table, along with other associated components.

Table 6-1. Power Supply Voltages

Supply	Pin on Universal Calibrator	Associated Circuitry 702-1522	702-1520
+5	+5	BR1	F1, Q7, CR10
+24	+24	CR3, CR4	F3, Q12, CR25
+48	+48	CR1, CR2	F2, Q8, CR14
-9	-9	CR5, CR6, CR7, CR8	Q24, CR18
-5	TP1 on 702-1520	CR5, CR6, CR7, CR8	Q26, CR21
+Prog	+Prog	CR3, CR4	F3, Q14, CR26
+12	TP2 on 702-1520	CR5, CR6, CR7, CR8	Q19, CR17

NOTE

If a Programming Pak is not installed or TP 4 is not grounded, the 24 V, 48 V and + Prog V supplies will be shut down.

If any components associated with +5 V, -5 V or +12 V supplies are replaced, jumpers JP3, JP8 and JP9 should be removed until the supplies are determined to be at the proper voltage levels. The jumpers can then be replaced and the calibration procedure of section 4.2 can be performed.

6.3.2 CONTROLLER

a. Visually check that all socketed devices are seated firmly. Check that jumpers JP3, JP8 and JP9 are installed.

b. With an oscilloscope, determine if the V.Ø2 timing signal is present by observing pin 11 of U12 on the 702-1520 board. If it is not present, check that the Programming Pak is grounding pin HH (TP4) on J6, the Programming Pak interface.

c. If steps "a" and "b" do not reveal the problem, contact your Data I/O Service Center.

6.3.3 SERIAL INTERFACE CIRCUITRY

To inspect operation of the serial interface circuitry on the 702-1520 Controller, proceed as follows:

a. Prepare the serial interface connector test fixture as illustrated in Figure 6-1, and install on the serial port. The +5 V required at pins 3, 5 and 8 is available at pin 22.

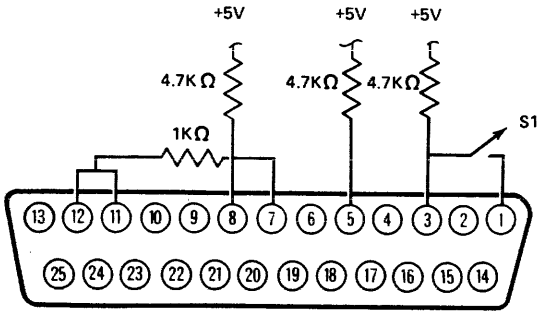


Figure 6-1. Serial Interface Test Fixture

b. Short the Echo Jumper (JP2 on the Controller).

c. 1) Open S1 on the serial interface test fixture. Pin 13 should read -4 V.

2) Close S1. Pin 13 should read +4 V.

3) An improper voltage noted in step c (1) and (2) indicates that troubleshooting the circuitry associated with Q1, Q2, U7 and U10 is necessary.

d. With an oscilloscope, observe U20, pin 3 on the Controller. The frequency of the signal at pin 3 should be 16 times the selected baud rate. (Baud rate = 1/time, divided by 16.)

A failure in step "d" indicates a problem with U8, and associated circuitry.

Example: At 110 baud, the observed pulse period should be .57 ms.

$$\text{Baud Rate} = (1/t) \div 16$$

$$= \frac{1 \div (5.7 \times 10^{-4}\text{s})}{16}$$

$$= (1754) \div 16$$

$$\text{Baud Rate} = 109.6 \text{ baud (110 baud)}$$

e. 1) Select serial interface Output mode. Refer to Table 3-3 for the proper Select Code.

2) Check the voltages at U20, pins 24 and 23. Both should read Ø V to 0.5 V.

3) Press START.

4) Use the oscilloscope to observe pin 2 of the serial interface test fixture. The System 19 should be transmitting data at the selected baud rate.

A failure in step "e" (1 through 4) indicates a failure in the ACIA.

SECTION 7
CIRCUIT DESCRIPTION

7.1 INTRODUCTION

This section describes the System 19 in general terms. It outlines the Address map, general assembly cabling and architecture of the unit.

7.1 GENERAL ARCHITECTURE

The System 19 utilizes bus architecture with a 6802 microprocessor. See the system block diagram, Figure 7-1. Each block is discussed separately in paragraph 7.4.

7.2.1 BUS

The bus consists of a 16-bit address bus, 8-bit data bus, and several control lines. See Table 7-1. All communications between portions of the circuitry are handled in the same manner over this bus. A write operation is accomplished according to the timing diagram of Figure 7-2, and a read operation is accomplished according to the timing diagram of Figure 7-3.

The bus is directly available at the option port (J5) of the Controller. The buffered bus is available at the Programming Pak Interface (J6).

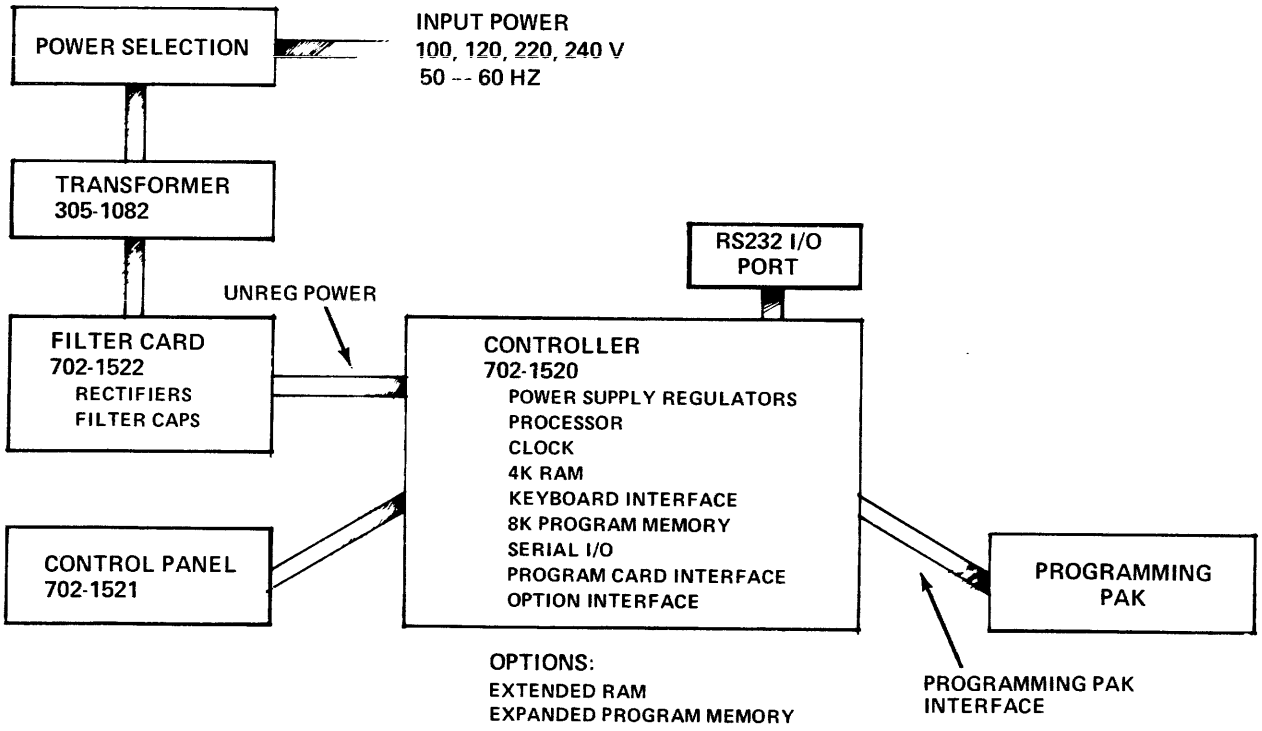


Figure 7-1. Block Diagram, System 19 Electronics

Table 7-1. System 19 Bus (At J5)

PIN	FUNCTION		PIN	FUNCTION
1	N.A.		27	Halt
2			28	N.A.
3	A_0		29	$\overline{V.\emptyset_2}$
4	A_1		30	$R/\overline{W}$
5	A_2		31	N.A.
6	A_3		32	$\overline{R}$
7	A_4		33	TOR
8	A_5		34	$\overline{NMI}$
9	A_6		35	$\overline{IRQ}$
10	A_7		36	N.A.
11	A_8	Address	37	N.A.
12	A_9		38	N.A.
13	A_{10}		39	+5
14	A_{11}		40	+5
15	A_{12}		41	N.A
16	A_{13}		42	N.A.
17	A_{14}		43	-5
18	A_{15}		44	-5
19	D_0		45	+12
20	D_1		46	+12
21	D_2		47	+24
22	D_3	Data	48	+24
23	D_4		49	GND
24	D_5		50	GND
25	D_6			
26	D_7			

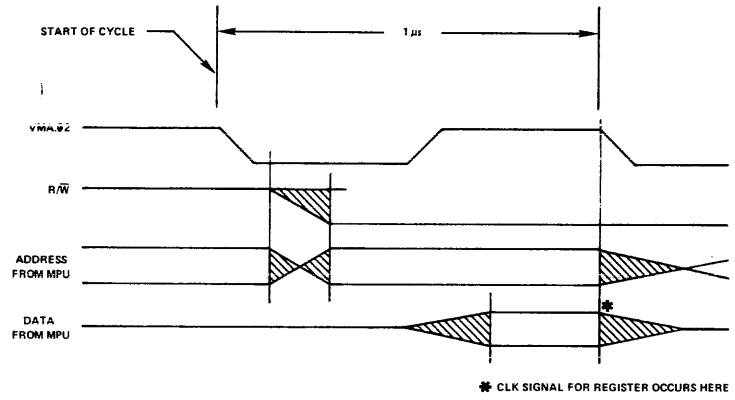


Figure 7-2. Write Timing

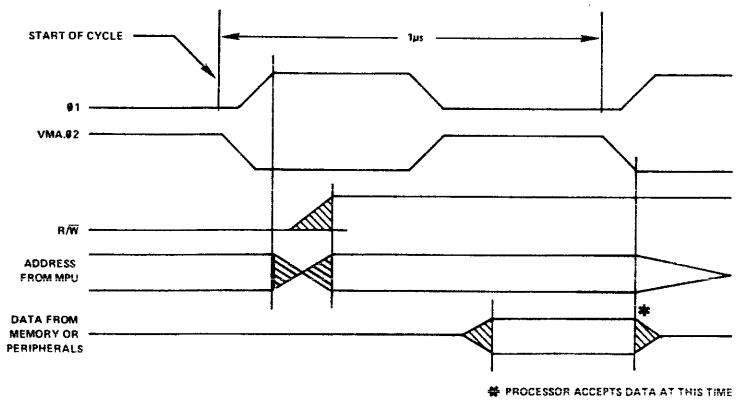


Figure 7-3. Read Timing

7.2.2 ADDRESS MAP

The address map of Table 7-2 shows the location in hexadecimal of each decoded function of the System 19.

Table 7-2. System 19 Address Map

0000	007F	6802 RAM
0000	03FF	Optional RAM (disable internal)
0400	1FFF	Unassigned
2000	5FFF	Data RAM (16K maximum)
6000	8FFF	Extended Software Cardsets
9000	BFFF	Alternate Program Area (12K)
C000	DFFF	Normal Program Area (8K)
F800	FFFF	Restart Vector (2K)
E200	E2FF	S 19/17 Serial I/O Area
E200		Address Reg. HO
E201		Address Reg. LO
E202		Data Gate/Data Register
E203		Control Register/Status Gates
E204 – E205		KBD/Display
E206 – E207		Serial I/O
E000	E0FF	Interface Cont. Reg
E100	E1FF	Switch Gates

7.3 COMPONENT LAYOUT

Figure 7-4 shows the cabling between assemblies, along with associated connector numbers and cable type.

The System 19 component layout is shown in Figure 7-5.

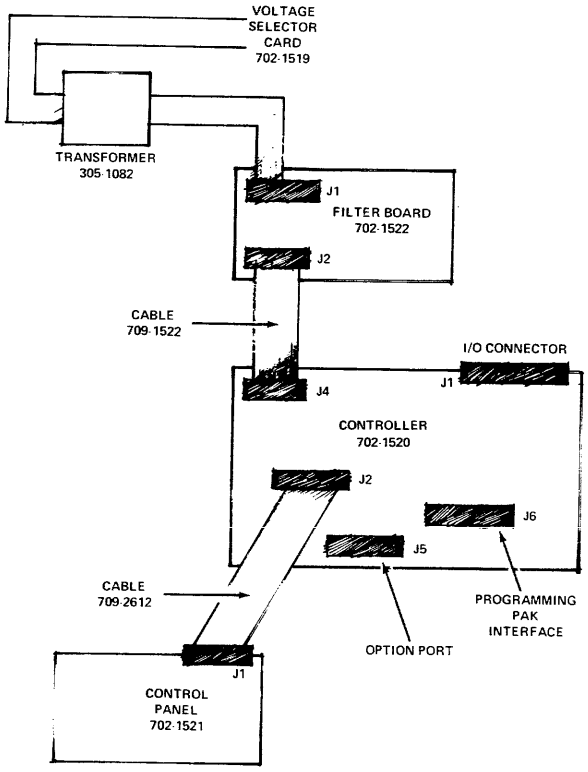


Figure 7-4. System 19 Interconnection Diagram

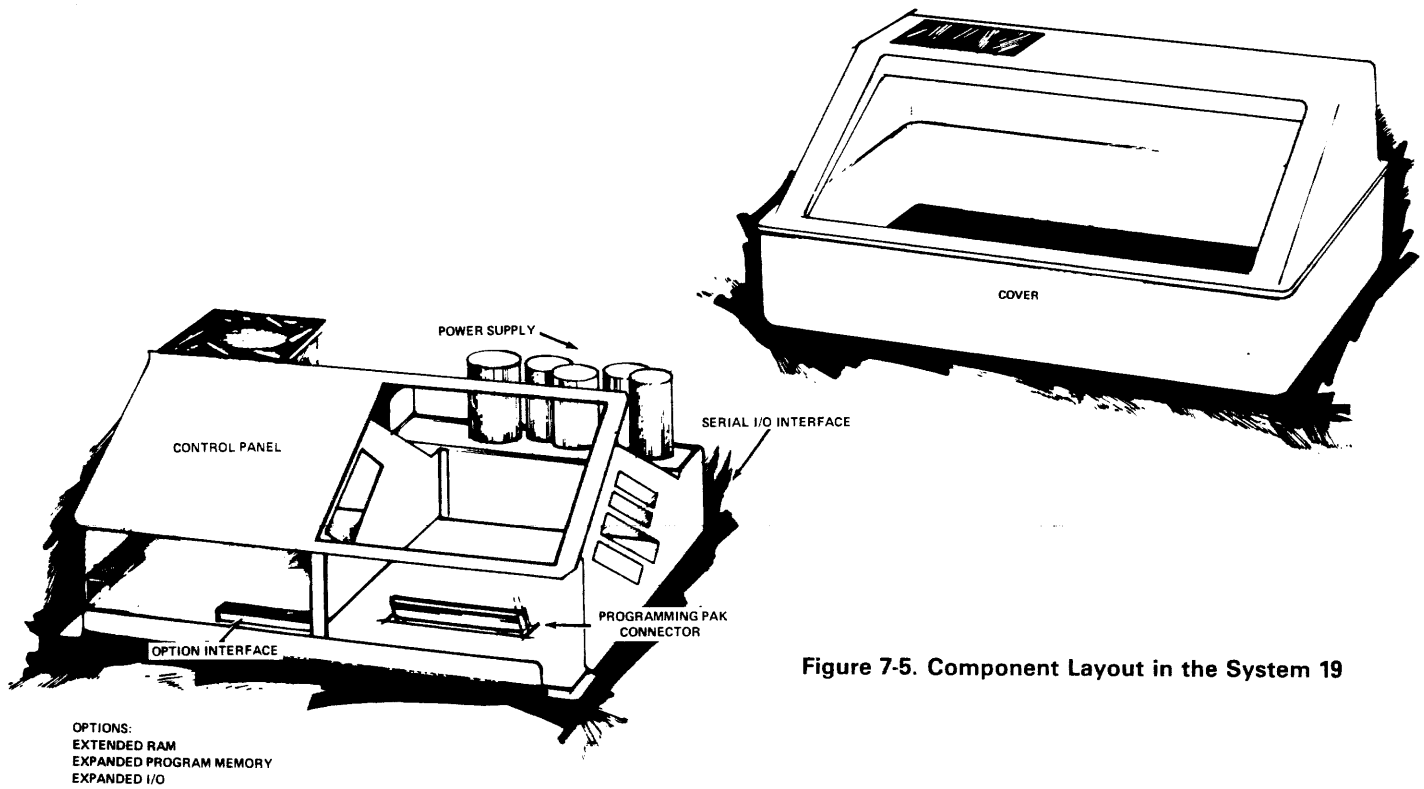


Figure 7-5. Component Layout in the System 19

7.4 INDIVIDUAL BLOCK DIAGRAM DESCRIPTION

Individual card function and flow are discussed in the following paragraphs. References are made to the individual block diagrams. The schematic for each card assembly is located in the rear of the manual.

7.4.1 POWER SUPPLIES

All of the major power supply components are shown in Figure 7-6. Each will be discussed separately.

The AC power switch has a built-in overload circuit breaker, reset by turning the equipment OFF, pausing, and turning it ON again.

Paragraph 2.3.2 explains the configuration of the AC voltage selector for various AC input voltages. See paragraph 5.3.2 for fan maintenance.

The power transformer has multiple primary windings for various input voltages, plus an electrostatic shield between primary and secondary windings, which is connected to chassis ground. The secondary develops appropriate voltages for the rectifier and filter card.

Four rectifier and capacitor filter networks are contained on the filter card to provide the DC voltages for the various regulators. See Figure 7-7. PNP transistor Q1 is connected to the center tap of the high voltage winding of the transformer. When Q1 is turned OFF by the High Voltage Shutdown Control, no current can flow to the +40 V and +HV unregulated voltage outputs.

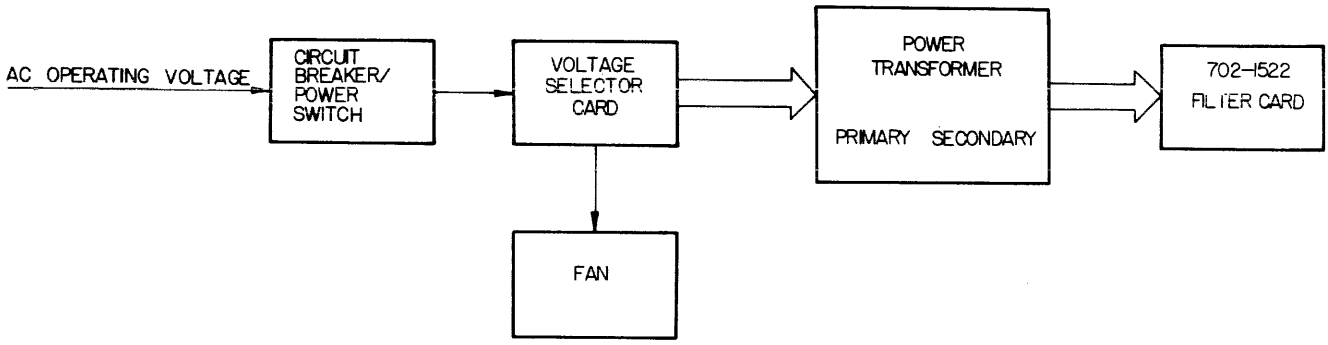


Figure 7-6. Block Diagram, Power Supply

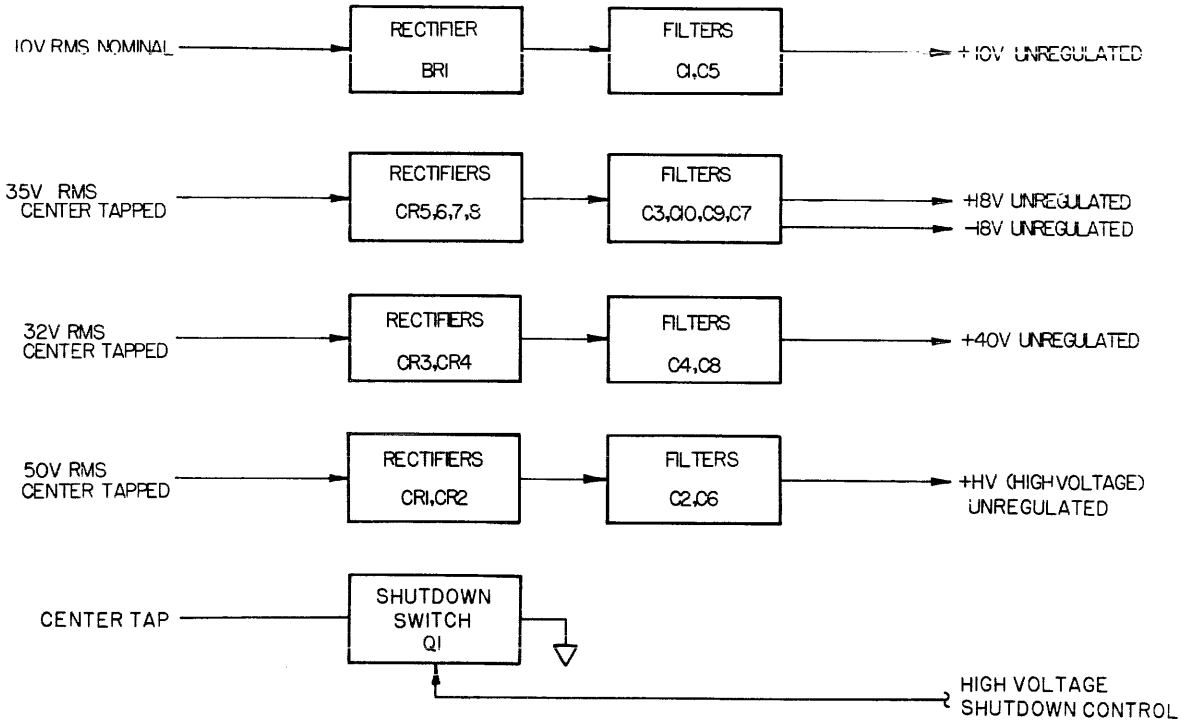


Figure 7-7. Block Diagram, Filter Card

The voltage regulator blocks are shown in Figure 7-8. Each block will be discussed below.

The 5-volt regulator consists of a TL430 shunt regulator driving an MJE240 which, in turn, drives the TIP 35A pass transistor. Feedback is provided to the TL430 by the voltage adjusting potentiometer R18. Foldback current limiting is achieved by sensing both output current and output voltage. If an overcurrent condition exists, Q5 senses the increased voltage across R30 and reduces the base drive to the pass transistor, which drops the output voltage. When the output voltage goes below the CR22 zener reference, base current flows through CR23 to Q5, further dropping the output voltage. To reset the regulator from its foldback condition, input power must be removed for an interval long enough for C12 to discharge.

The 24 V and 48 V supplies work on the same principle as the 5 V supply. The only major difference is that a current source, rather than an emitter follower, is used to supply pass transistor base current.

The programmable supply uses a Darlington differential pair, Q21, Q25 and Q17, Q23, working into a current source (Q22). The pass transistor, Q14, follows the current source voltage. A TL430 shunt regulator provides a 5-volt reference for the plus input of the differential pair (Q17). Two feedback nodes are connected to the sense and operate lines. By connecting various resistors to these lines the output voltage can be "programmed" to any level between 5 and 40 volts. Foldback current limiting is provided in the same manner as in the 5 V supply.

The -9 V and -5 V supplies use standard monolithic regulators.

The Shutdown control signals the 1522 card to turn OFF the +HV and +40 V unregulated supplies when the Programming Pak is removed. This in turn shuts down the +48 V, +24 V, +Prog V and +70 V supplies.

Fuses F1 - F5, in conjunction with the crowbar zeners on all supply outputs, protect the system electronics from an overvoltage condition on the supply lines, which could occur from power-supply component failure.

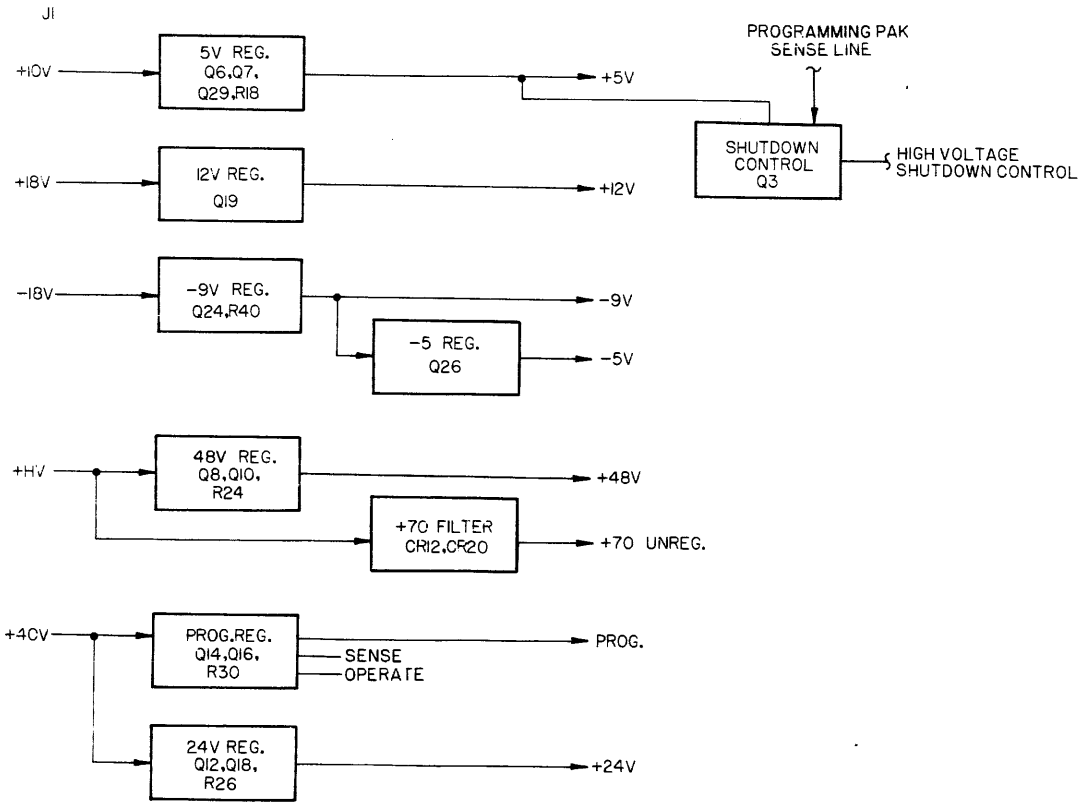


Figure 7-8. Block Diagram, Regulator Portion of Controller

7.4.2 CONTROLLER

The Controller is shown in block diagram form in Figure 7-9. Each block will be discussed below.

The processor drives the bus (para 7.2.1) through address buffers U23 and U24 and data buffer U35. Control signals are also developed by the processor and sent through buffers to the bus.

The decode PROMs U13, U14, U15, U22 and U44 inspect the Address Bus and R/W to select the various gates, registers and other devices connected to the Data bus. Refer to the memory map of Table 7-2. V.Ø2 is connected to the CS of each decode PROM to provide the correct timing for writing to registers or reading gates or other memory. Refer to the timing diagrams, Figure 7-2 and 7-3.

The Program Card Set interface is provided by the address registers, status gates, data register, data gates and control register. These gates and registers allow the System 19 to use standard Data I/O 909 series Program Card Sets (PCS) packaged as 919 series Programming Paks.

As the Programming Pak is removed, the processor is held reset by a high on pin HH of J6. When the Programming Pak is installed, line HH of J6 is grounded, removing the reset after a short delay. This feature allows Programming Paks to be changed with the power ON while preserving RAM data.

Additional flexibility of the PCS interface can be gained with software control of the interface control register. The PCS interface can be set up so that the processor bus is buffered and directly available at the port. This is accomplished by disabling the address register outputs, enabling the address gates in the outward direction, and connecting the data gate direction to the R/W line. The data gate is enabled at the appropriate address by decoding done external to the port over the data gate enable line.

The serial interface is controlled by the 6850 ACIA and appropriate software. The timing signal for the ACIA is provided by the baud rate generator, U8. The baud rate is selected by rate select switch U9. The status switch provides for selecting parity and stop bits; the ACIA occupies two addresses (Table 7-2) and communicates with the processor, using the interrupt request line (IRQ).

The keyboard/display interface is provided by an 8279. This device contains a small RAM and first in, first out (FIFO) register, along with scanning control circuitry. The 8279 is configured for N-key rollover. The 8279 occupies two address locations (Table 7-2) and uses IRQ to interface with the processor.

The on-board program memory occupies up to 8K bytes of PROM decoded in 2K segments. An additional 8K bytes are available. See paragraph 7.4.4.

Temporary storage on the Controller consists of 4K bytes of RAM decoded in 1K segments, and 128 bytes of data internal to the 6802 CPU. An additional 12K bytes are available. See paragraph 7.4.5.

The option port provides access to the unbuffered processor bus for service and the addition of optional RAM.

7.4.3 CONTROL PANEL

The control panel consists of a hexadecimal keypad plus 11 control keys and six 7-segment displays plus 10 status LEDs.

Scan lines from RS0 through RS3 of the 8279/U33 on the Controller are continuously counting in binary (4 bits). These lines are decoded by the decode PROMs which select a cathode driver for a particular 7-segment display or one of two banks of status LEDs. The data (up to 8 bits) associated with each scan count is buffered through the data drivers to drive the desired anodes. This combination lights the desired segments.

The decode PROMs also provide two lines for scanning the hexadecimal keypad and one line for the control keys. If a key is pressed the data out lines send this data (up to 8 bits) to the 8279 on the Controller for storage. After debouncing is accomplished by the 8279 an interrupt (IRQ) is generated for attention by the processor. See Figure 7-10.

7.4.4 PROM EXPANSION CAPABILITY
(Expanded Program Memory, P/N 950-1580)

The System 19 Controller Board has capacity for 16K of program memory. 8K is resident on the controller, and up to 8K of additional program memory is accommodated on the Expanded Program Memory Board, 702-1580. 1K of RAM is resident on the board as scratch-pad memory expansion.

The board is connected under the keyboard and display panel to J5 on the Controller.

7.4.5 RAM EXTENSION CAPABILITY
(4K Additional RAM, P/N 950-1533-1)
(12K Additional RAM, P/N 950-1533-2)

The standard System 19 includes 4K of RAM on the Controller Board but is capable of addressing 16K of RAM. RAM in excess of 4K resides on the optional Extended Memory Board, 702-1533. This board has the capacity for 24 low-power 1Kx4 RAMs, for a total of 12Kx8 bits of memory. Decoding is accomplished on the card by use of a PROM driving two 74LS138 devices. The 74LS138 outputs are tested by V.Ø2 and are always active high or low, requiring no pull-ups.

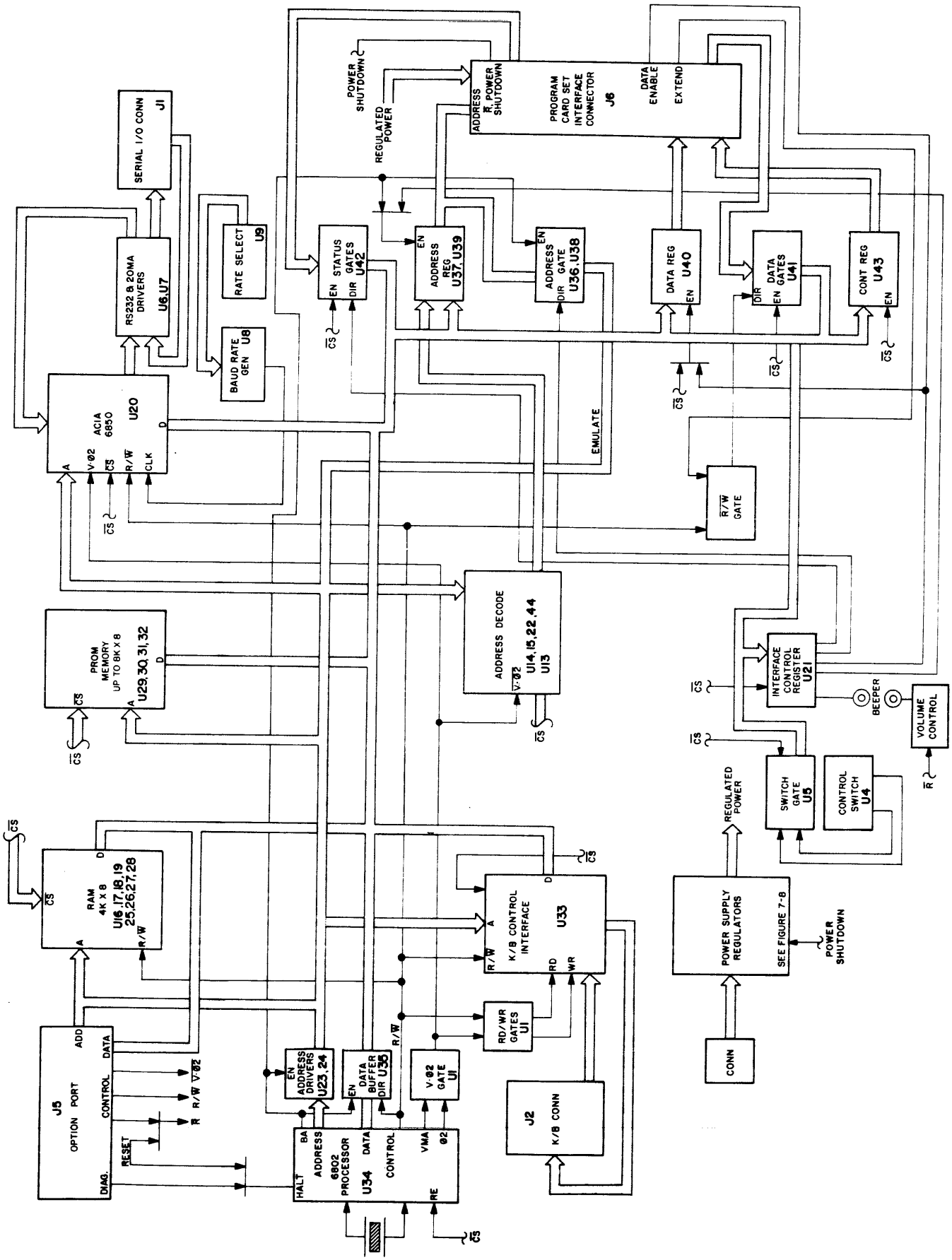


Figure 7-9. Block Diagram, Controller

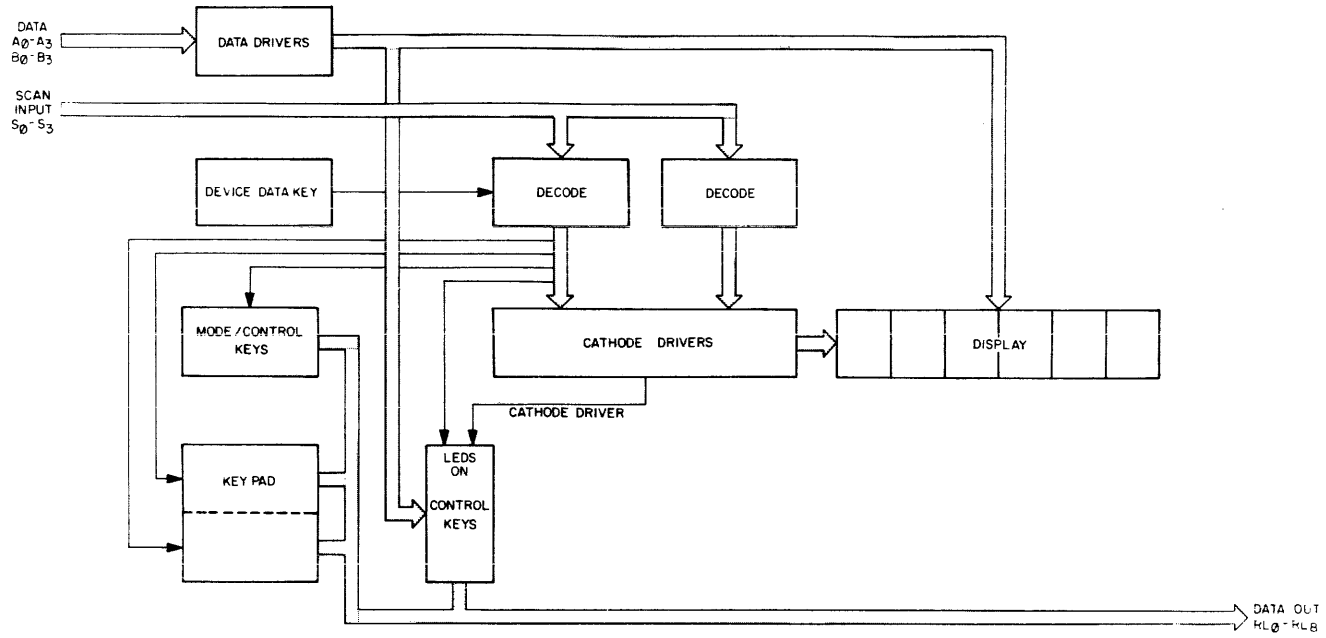
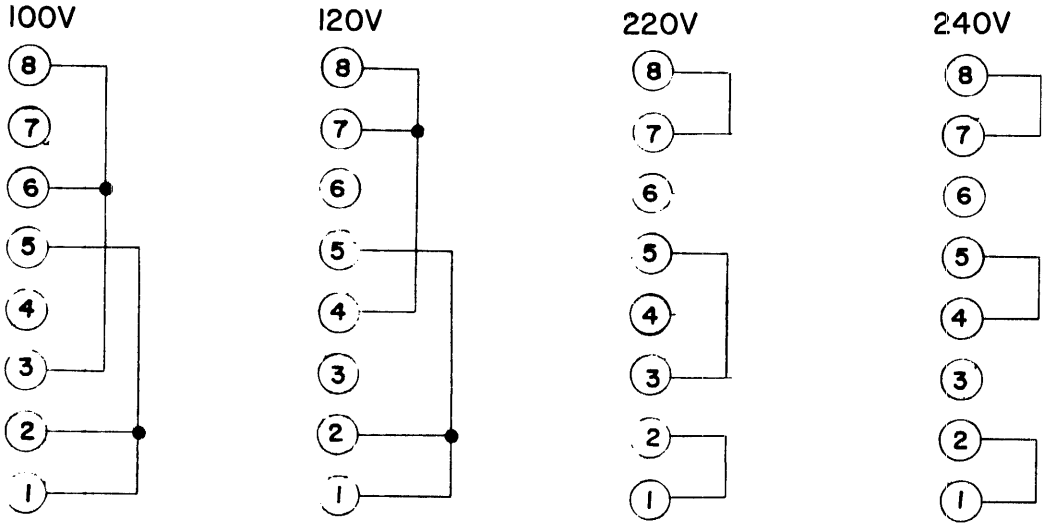


Figure 7-10. Block Diagram, Control Panel

SECTION 8
SCHEMATICS

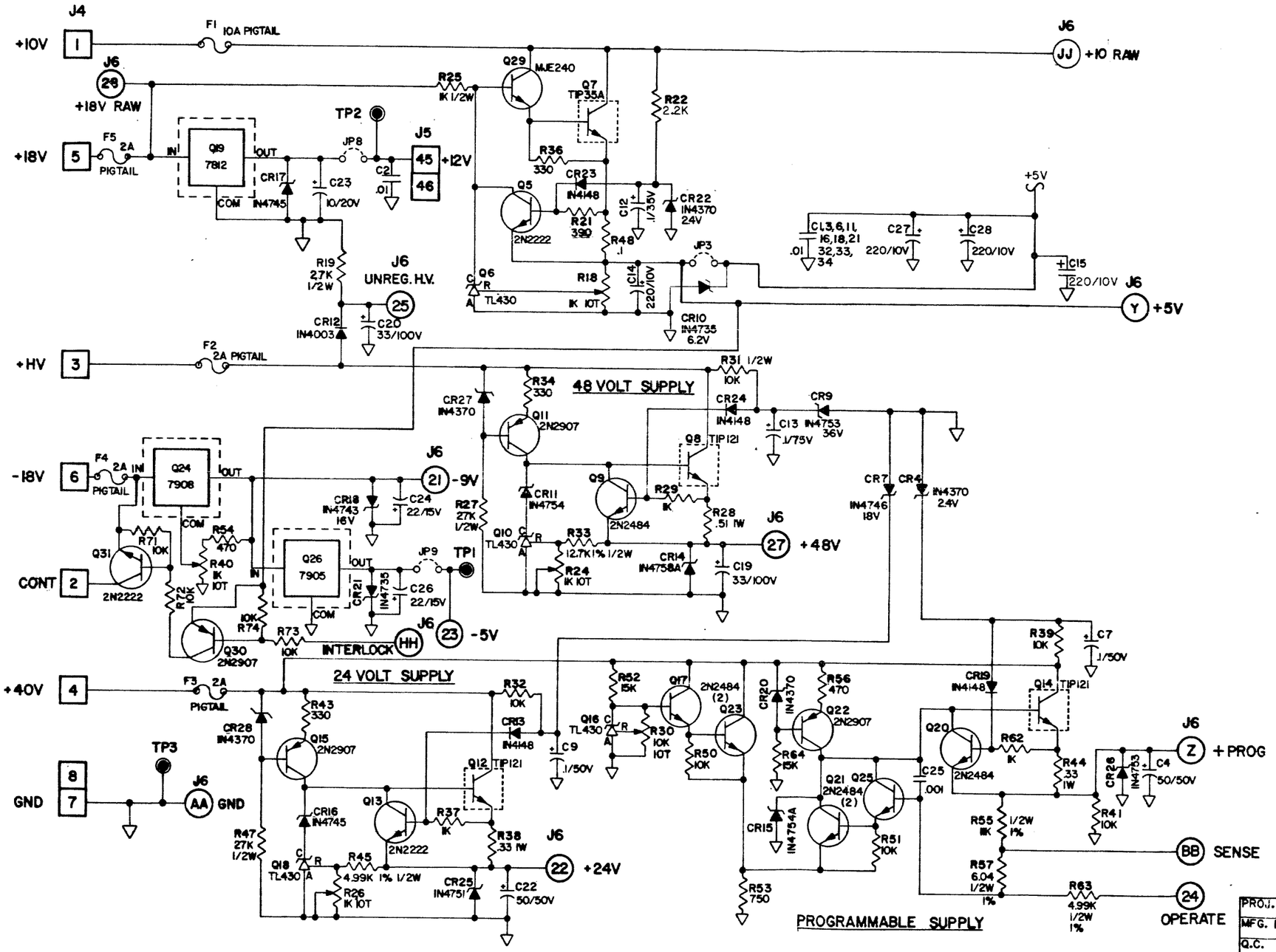
008-1519	Power Select Board
008-1520	Controller (Page 1 of 3)
008-1520	Controller (Page 2 of 3)
008-1520	Controller (Page 3 of 3)
008-1521	Keyboard and Display Card
008-1522	Filter Board
008-1523	Program Card Interface
008-1533	Extended Memory
008-1580	Expanded Program Memory

DATE	SYM	REVISION RECORD	DR.	CK
8/78	A	PRODUCTION REL.	TC	
11/78	B	ECN #2561		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ± —		SCALE —	DRAWN BY T. CONNERTON APPROVED BY
FRACTIONAL ± —	TITLE POWER SELECT BOARD SYSTEM 19		
ANGULAR ± —	DATE 8/16/78	DRAWING NUMBER 008-1519	

REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE	APP	DATE
	A	RELEASE				8-7-78
	B	CN 2461				9-28-78
	C	CN 2583				11-15-78
	D	CN 2534				11-28-78
	E	CN 2643				12-7-78
	F	ECN 2648				12-12-78
	–	ECR 2728				1-18-79
	G	ECN 2905				
	–	ECN 3016				
C5	–	ECN # 3062				7-79
	H	CN 3115				
	J	CN # 3145				8-11-79
	J	CN # 3443				3/80
	K	ECN # 3836				10/80
	L	ECN 3882				3/81
	M	ECN 4053				



PROJ. ENG.	DATA I/O REDMOND WASH
MFG. ENG.	
Q.C.	TITLE
ENG. MGR.	CONTROLLER SYSTEM 19
DATE 1-19-79	
VAL Z 6-27-78	SIZE D/B · CODE IDENT NO · DRAWING NO. 008-1520
	SCALE NONE · 8-16-78 · SHEET 1 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	F	SEE SHEET 1 OF 3 (ECN 2728)	1-10-79	
	H	SEE SHEET 1 OF 3 CN3115	8-4-79	
	J	CN#3145	8-11-79	
	K	ECN #3836	10-28-80	
	L	ECN 3881	3-17-81	
	M	ECN 4053	8-13-81	

REFERENCING NOTE

WHEN LINES ARE REFERENCED FROM ONE SHEET TO THE NEXT, THE PROCEDURE IS AS FOLLOWS

XXXX (NAME OF FUNCTION)
SHEET 3 ZONE 8D (3.8D)

PROJ. ENG.	DATA I/O ISSAQUAH WASH		
MFG. ENG.	CONTROLLER SYSTEM 19		
Q.C.			
ENG. MGR.			
DATE 1-19-79	7-12-78	SIZE D/B	CODE IDENT NO	DRAWING NO. 008-1520
	8-16-78	SCALE NONE		SHEET 2 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	F	SEE SHEET 1 OF 3 (ECN 2728)	1-18-79	
	G	SEE SHEET 1 OF 3 ECN 2905	4-13-79	
	H	SEE SHEET 1 OF 3 CN-3115	8-4-79	
	J	CN# 3145	8-11-79	
	J	CN# 3443	3-80	
	K	ECN # 3836	10-28-80	
	L	ECN 3882	3-17-81	
	M	ECN 4053	8-13-81	

RAM MEMORY

ADDRESS BUS 2.3C

DATA BUS 2.3C

U28 2114 2000-23FF

U27 2114 2400-27FF

U26 2114 2800-2BFF

U25 2114 2C00-2FFF

U19 2114

U18 2114

U17 2114

U16 2114

RAM DECODE

R/W

2.4C DIRECTION

2.6B PROM DECODE

74LS04

PROM MEMORY

U29 2708/16 +5=24 -5=21 +12=19 GND=12

U30 2708/16

U31 2708/16

U32 2708/16

LO ADDRESS GATE

U36 74LS245

HI ADDRESS GATE

U38 74LS245

LO ADDRESS REG

U37 74LS374 E201

HI ADDRESS REG

U39 74LS374 E200

A_0

J1 (16)

GATE ENABLE

J1 (14) J6 (CC)

2.3D I/O DECODE

2.3C CONTROL

EXTEND

IRQ (DD) (26) R/W (EE) EMUL STB (FF)

J6

R/W V.02

+5V R60 OMIT

R58 OMIT C29 OMIT

2.5C CI +5V 2.5C DREG

74LS08 U3

R 3.3K

74LS00 U1

BUS AVAILABLE JP1 2.7B

R59 OMIT Q27 OMIT

Q28 OMIT

DATA REG

U40 74LS374 E202

R61 3.3K +5V

TP4

74LS05 R66 OMIT +5V

DATA GATES

U41 74LS245 E202

RP6 RP8 RP7 RP9 RP7 RP9 3.3K(8)

2.8B TOA 74LS05 R70 2.2K +5V

STATUS GATES

2.5C SR

U42 74LS245 E203

RP9 RP7 RP9 RP9 RP9 RP7 RP7 RP7 3.3K(8)

+5V RP5 RP5 RP6 RP6 RP6 RP5 RP5 RP8 RP8 RP8 RP8 RP8 RP6 RP8 RP6 3.3K (16)

2.8A CLR

U43 74LS273 E203

CONTROL REG

R69 2.2K +5V CR29 IN4148

R75 56K +5V

R65 50K IOT CR30 IN4148

TONE CONT 2.5C

74LS05 R68 1K +5V

INTER-LOCK (HH)

(9) DI_1
(10) DI_2
(11) DI_3
(12) DI_4
(13) DI_5
(14) DI_6
(15) DI_7
(16) DI_8
(K) DO_1
(L) DO_2
(M) DO_3
(N) DO_4
(P) DO_5
(R) DO_6
(S) DO_7
(T) DO_8
(V) START
(20) 36
(W) W/L
(X) VOL/VOH
(U) A
(17) B
(19) 26
(18) CLOCK INH.
(LL) R

(29) PP
(30) RR
(31) READ
+10V (JJ) +10V
(32) FWD
(KK) WRITE

REFERENCING NOTE
WHEN LINES ARE REFERENCED FROM ONE SHEET TO THE NEXT, THE PROCEDURE IS AS FOLLOWS:
XXXX (NAME OF FUNCTION)
SHEET 3 ZONE 8D (3.8D)

(A) A_0 (B) A_1 (C) A_2 (D) A_3 (E) A_4 (I) A_5 (2) A_6 (3) A_7 (4) A_8 (5) A_9 (6) A_{10} (F) A_{11} (7) A_{12} (H) A_{13} (8) A_{14} (J) A_{15} J6

DATA I/O REDMOND WASH

CONTROLLER SYSTEM 19

DATE 1-19-79

PROJ ENG

SIZE D/B | CODE IDENT NO | DRAWING NO. 008-1520

SCALE NONE | 8-16-78 | SHEET 3 OF 3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE	6-9-78	
	B	CN 2450	9-16-78	
	C	CN# 2543	10-24-78	
	C	CN# 3540	4-4-80	
	C	ECN #4062	4-13-81	

J1

RL0 1 · RL1 2 · RL2 3 · RL3 4 · RL4 5 · RL5 6 · RL6 7 · RL7 8

RS0 11 · RS1 14 · RS2 15

B0 21 · B1 22 · B2 23 · B3 24

A0 17 · A1 18 · A2 19 · A3 20

+10V 12 · GND 13 26 · +5V 25

+5V

RP2 3.3K

BEGIN RAM S1 · EDIT S2 · SELECT S3 · DEVICE DATA S4 · KEYBOARD S5 · START S6

KEY PAD

S6 · S5 · S8 REVIEW · S9 PROG · S11 ENTER · S10 VERIFY · S7 OMIT · S12 LOAD

CR1 OMIT

CR2 60V

S9 · S10 · S12 · S1 · S2

RP2 3.3K (7)

U4 TRI-STATE PROM

U3 7445

1K (6 PLACES) R33 R32 R31 R30 R29 R28

R25 330 · R35 10K · Q18 MJE 251 · +10V

R26 330 · R34 10K · Q17 MJE 251 · DS7 IB · DS8 P · DS9 V · DS10 COMP

R11 39 1/2W. Q6 · R13 Q7 · R15 Q8 · R1 Q1 · R3 Q2 · R5 Q3 · R7 Q4 · R9 Q5

MJE 800 (8 PLACES)

R12 · R14 · R16 · R2 · R4 · R6 · R8 · R10 3.3K (8 PLACES)

RPI 2.2K +5V

7407 (2 PLACES)

C1 +/ 22/15V

MJE 700 (6 PLACES) Q9 · Q10 · Q11 · Q12 · Q13 · Q14

R17 10K · R18 10K · R19 10K · R20 10K · R21 10K · R22 10K

DS1 · DS2 · DS3 · DS4 · DS5 · DS6

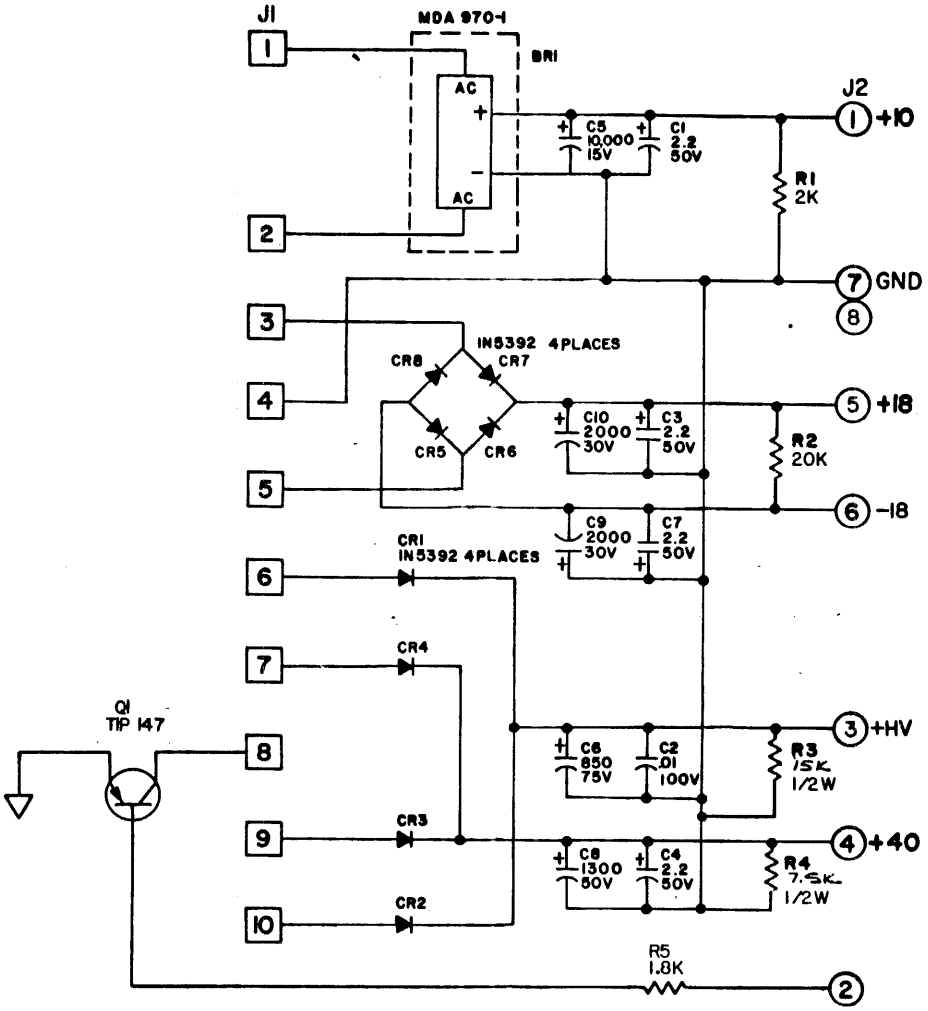
DISPLAY

DATA I/O

TITLE
KEYBOARD AND DISPLAY CARD
SYSTEM 19

DWN BY	K. LANZ	SIZE	CODE IDENT NO	DRAWING NO.
APRVD BY		D		008-1521
SCALE	NONE			SHEET 1 OF 1

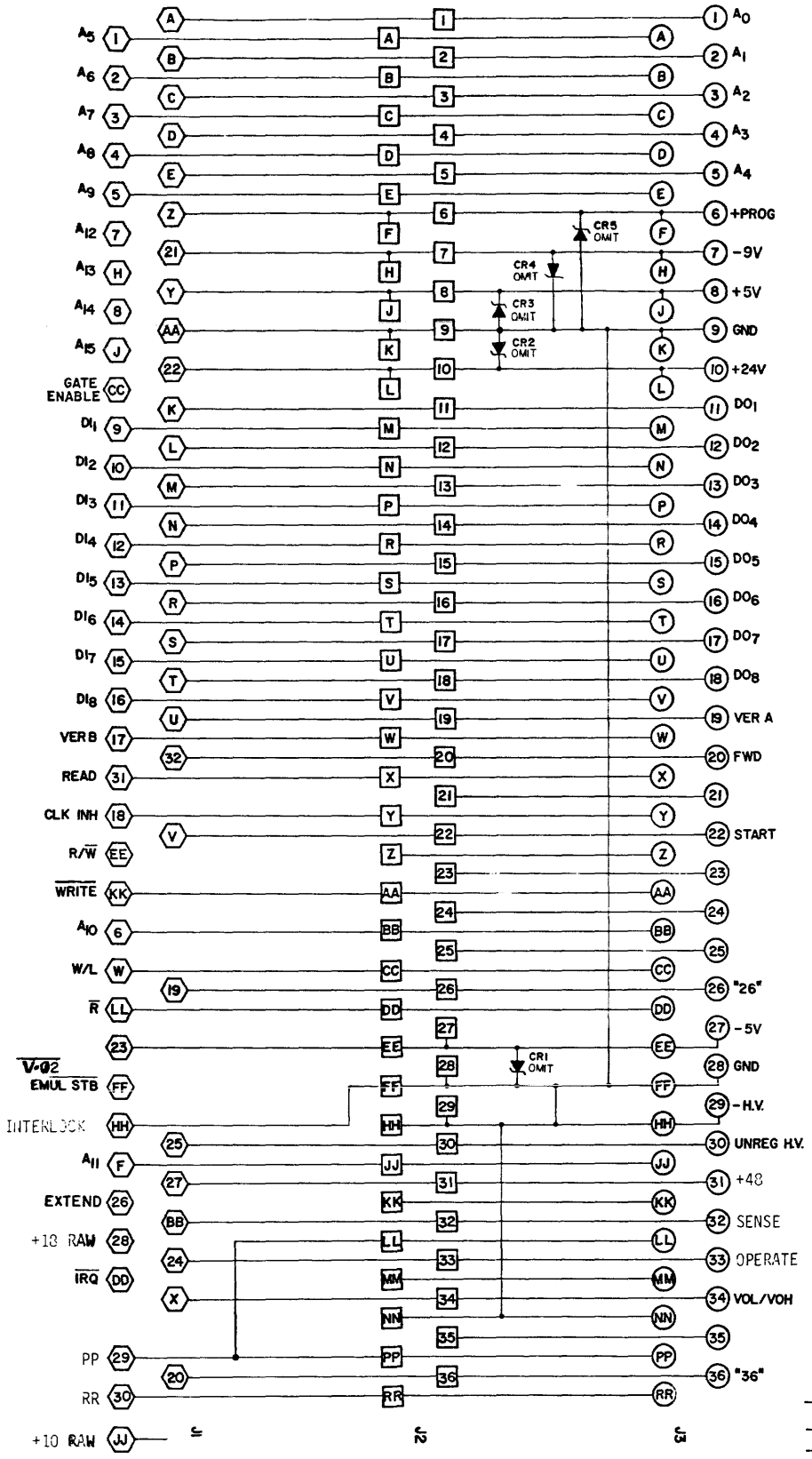
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASE	8-3-78	
	B	ECN 2490	9-29-78	
	C	ECN 2910 Ad.	4-12-79	



NOTES:

1. ALL RESISTORS 1/4 WATT. UNLESS OTHERWISE SPECIFIED.

TOLERANCES (EXCEPT AS NOTED)	DATA I/O REDMOND, WASH.		
DECIMAL ±	TITLE	FILTER BOARD, SYSTEM 19	
ANGULAR ±			
DRAWN BY: T. CONNERTON	SIZE C	CODE IDENT. NO.	DRAWING NO. 008-1522
APPROVED BY:	SCALE ~	8-16-78	SHEET 1 OF 1



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	CO 2495	8-27-79	
	B	CN 3434	10-6-79	
			2-4-80	

DATA I/O

PROGRAM CARD INTERFACE

P. WALTER	SIZE D	CODE IDENT NO	DRAWING NO 008-1523
SCALE NONE	8-16-78		SHEET 1 OF 1

REVISIONS						
ZONE	LTR	DESCRIPTION	CK	PE	APP	DATE
	A	PROD. RELEASE				10-31-78
	B	CN# 2755	KR			1-25-79

LOW ORDER

HIGH ORDER

P1

A0 3 · A1 4 · A2 5 · A3 6 · A4 7 · A5 8 · A6 9 · A7 10 · A8 11 · A9 12 · A10 13 · A11 14 · A12 15 · A13 16 · A14 17 · A15 18

D0 20 · D1 21 · D2 22 · D3 23 · D4 24 · D5 25 · D6 26 · D7 27

V-22 29

+5V 39 40 +5V

GND 49 50

R/W 30

U28 PROM 32 X 8 TS CS

U13 74LS138

U12 74LS138

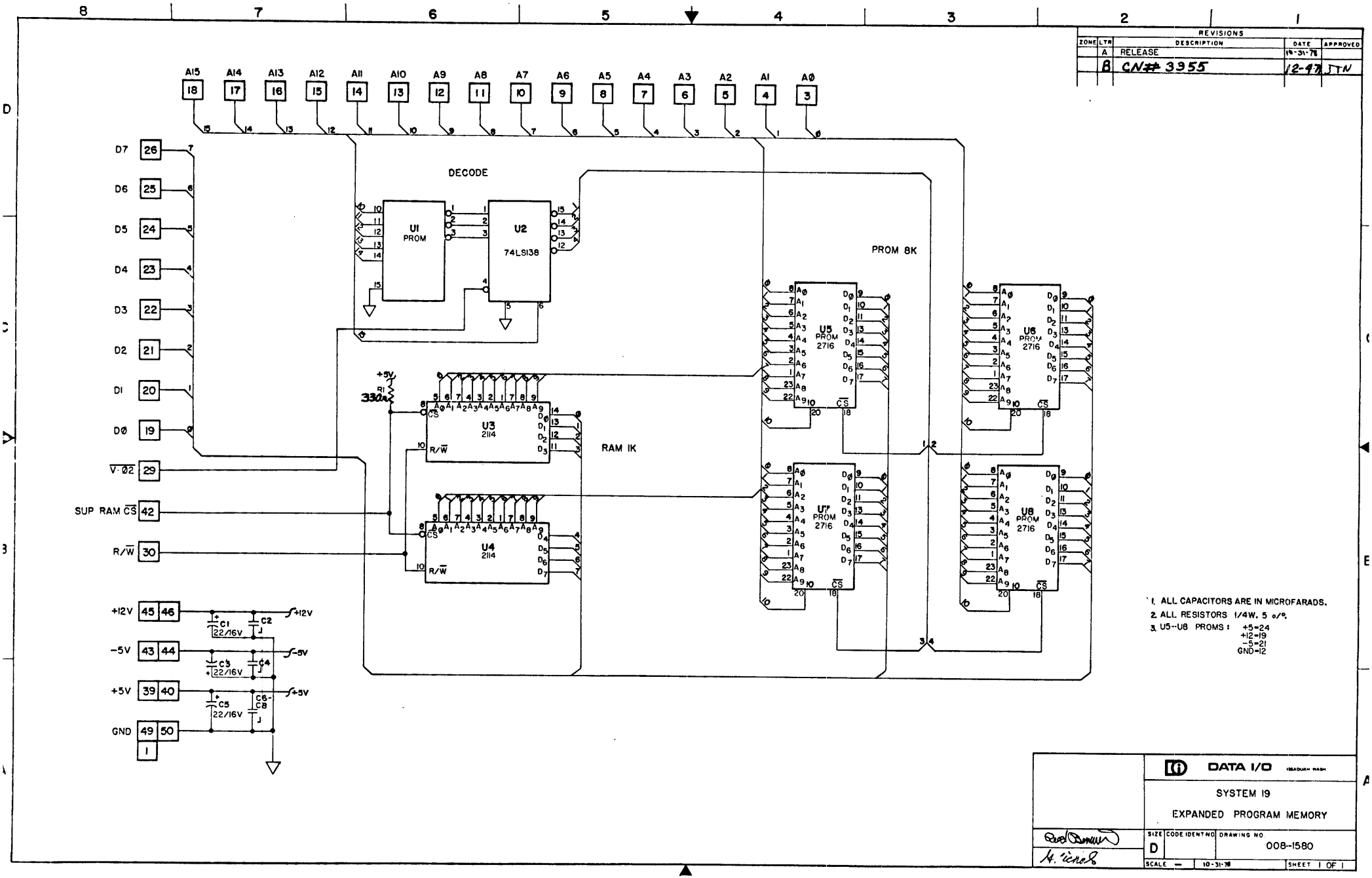
CS DECODE

C1-C2 .01 · C4-C15 · C3 22 15V.

U8	4000-43FF	U14	5000-53FF	U2	4000-43FF	U21	5000-53FF
U9	4400-47FF	U15	5C00-5FFF	U3	4400-47FF	U22	5C00-5FFF
U10	4800-4BFF	U16	5400-57FF	U4	4800-4BFF	U23	5400-57FF
U11	3000-33FF	U18	3800-3BFF	U5	3000-33FF	U25	3800-3BFF
U17	3400-37FF	U19	5800-5BFF	U24	3400-37FF	U26	5800-5BFF
U7	4C00-4FFF	U20	3C00-3FFF	U1	4C00-4FFF	U27	3C00-3FFF

All: 2114 · R/W · CS

APPROVALS		DATA I/O	
PROJ. ENG.		EXTENDED MEMORY	
MFG. ENG.			
Q.C.			
ENG. MGR.			
DATE 10-31-78	DWN Rod Bernard 10-31-78 · CHECKER: K Lane	SIZE D · CODE IDENT NO · DRAWING NO. 008-1533	
		SCALE	SHEET 1 OF 1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE 10-31-78
B CN# 3955 12-4-78 JTN
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
V·Ø2
SUP RAM CS
R/W
DECODE
U1 PROM
U2 74LS138
PROM 8K
U5 PROM 2716
U6 PROM 2716
U7 PROM 2716
U8 PROM 2716
+5V
R1 330Ω
U3 2114
U4 2114
RAM 1K
+12V
-5V
+5V
GND
C1 22/16V
C2
C3 22/16V
C4
C5 22/16V
C6-C8
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS 1/4W, 5 o/o.
3. U5--U8 PROMS : +5=24
+12=19
-5=21
GND=12
DATA I/O REDMOND WASH
SYSTEM 19
EXPANDED PROGRAM MEMORY
SIZE D
CODE IDENT NO
DRAWING NO. 008-1580
SCALE —
10-31-78
SHEET 1 OF 1

SECTION 9
GLOSSARY

This section contains definitions of terms as they are used in this manual. The definitions below are more restrictive than those in a dictionary for the same words; therefore, this section can be of value in readily understanding the discussions in this manual.

Address Field. Optional set of control characters in data translation format, which defines the address of the next data byte.

Address Offset. A parameter which may be specified in I/O commands with data formats that use addresses. The offset is subtracted from addresses on the way into the programmer and added to addresses on the way out.

Begin Device Address. The first device address at which data will be programmed or verified, or from which data will be loaded to the programmer RAM. Specified by BLOCK LIMIT L3.

Begin RAM Address. The first RAM address at which data will be loaded or verified, or from which data will be programmed into the device. Specified by BLOCK LIMIT L1.

Blank Check. An automatic test of the device to be programmed to see that it contains no programmed locations.

Block Move. A data transfer operation in which only a specified number of data bytes are moved. Such a block can be programmed, loaded, verified, input or output, or moved from one RAM location to another (RAM-to-RAM block move). Block moves require setting BLOCK LIMITS.

Block Size. The number of bytes to be programmed, loaded, verified, input, output, or moved within RAM. Specified by BLOCK LIMIT L2.

Calibration. A combination of tests and adjustments to maintain proper programming specifications.

Data Translation Format. Form in which the unit's translator software accepts input data. Also the form for data output by the unit.

Default Value. The value the programmer uses in the absence of operator specification.

Device. Programmable integrated circuit (PROM, EPROM, FPLA, etc.)

End Code. Character in data translation format which signals completion of data transfer.

EPROM. Erasable Programmable Read-Only Memory. PROM which can be cleared of data by exposure to ultra-violet light.

Function. Software routine that performs a machine task — either an operation with data, a data integrity test, or a series of electrical tests.

Gang Programming Pak. Optional hardware attached to the unit's front panel which provides the capability of programming up to 8 devices simultaneously.

Illegal Bit. A bit in the device under test which does not exist in the programmer RAM.

Input. Data transfer from the serial port to RAM.

Input Compare. Data comparison between the serial port and RAM.

Load. Data transfer of a master device to RAM.

Operation. The execution of a function or mode.

Output. Data transfer from RAM to the serial port.

Personality. Configuration of the unit for compatibility with a specific device type.

Program. Data transfer from RAM to the device.

Program Card Set (PCS). Two printed wiring boards connected with a cable and installed within the Programming Pak. This set usually consists of one analog and one digital card.

Program Electronics. Circuitry which generates waveforms required to program devices. See Program Card Set.

Programming Module. Generic term for Programming Pak, UniPak, Gang Module, FPLF Pak, etc. See Programming Electronics.

Programming Pak. Hardware containing a Program Card Set installed on the unit's front panel to establish the personality of the unit. It allows (with a socket adapter) the unit to program a specific device.

PROM. Programmable Read-Only Memory.

RAM. Random Access Memory. The unit's internal memory used for data storage.

RAM Destination Address. The first address in RAM where a block of RAM data will be stored in a RAM-to-RAM block move. Specified by BLOCK LIMIT L3.

RAM Source Address. The first address in RAM where a block of data will be taken from in a RAM-to-RAM block move. Specified by BLOCK LIMIT L1.

Select Code. Two-digit (hex) number used to specify data translation formats, serial interface operations or certain RAM data manipulations.

Socket Adapter. A TexTool socket mounted in data I/O frame; used as interface between device to be programmed and programming electronics.

Start Code. Character in data translation format which signals beginning of data transfer.

Sum-Check. The four digit hexadecimal total of data in RAM or data transferred in an operation. The sum-check ensures that RAM data equals data transferred from a device or peripheral.

UniPak. A Single Programming Pak which can program most bipolar and MOS PROMs.

Verify. Byte-by-byte comparison of RAM data with data in a device.

Waveforms. Timing and magnitude of program pulses that cause programming of data at selected address. If the waveforms are not kept within tolerance, programming yield is jeopardized.

APPENDIX 1

SYSTEM 19 ERROR CODES

CODE	NAME	DESCRIPTION
(None)	PROM Sum-check Error	The programmer's internal program memory contains incorrect values. If this error occurs, the programmer will display "ERR".
21	Illegal Bit Error	It is not possible to program the device due to the presence of already programmed locations of incorrect polarity.
22	Programming Error	The programming electronics were unable to program the device (reject).
23	First Pass Verify Error	The device data was incorrect on the first pass of the automatic verify sequence during a device programming operation.
24	Second Pass Verify Error	The device data was incorrect on the second pass of the automatic verify sequence during a device programming operation.
25	No Programming Electronics Installed	A device related operation was attempted without programming electronics being installed.
26	Programming Electronics Reset	The programming electronics will not start operation due to a reset condition. This could be due to overcurrent shutdown caused by an upside down device.
27	L1 + L2 Greater Than RAM; Invalid L2	The sum of the specified Begin RAM Address, L1, and the block size, L2, exceeds the capacity of RAM, or an attempt was made to enter 0 for L2.
28	Calibrate Mode Address Range Error	The operator attempted to program a device at an invalid address in Calibrate mode.
30-39	Programming-Electronics Error	The programming module's software detected an error. Refer to the specific programming electronics Manual.
41	Framing Error	The serial interface detected a start bit but the stop bit was incorrectly positioned. Can be caused by incorrect baud rate.
42	Overrun Error	The serial interface received characters when the programmer was unable to service them.
43	Framing And Overrun Combined	See 41 and 42.
46	I/O Timeout	No characters (or only nulls and rub-outs) were received on serial input for 25 seconds after depressing the START key. No characters could be transmitted for a period of 25 seconds due to the state of the handshake lines.
48	Serial Port Buffer Overflow	The serial port input buffer received too many characters after the programmer informed the sending device to stop. This will never occur with handshake connected.
50	No Data Input	Because of address errors or an invalid format, no data transferred during input.
52	Input Compare Error	The data from the serial port did not match the data in RAM.
54	Insufficient Data On Remote Input	The programmer expected more characters. Can occur when wrong characters are received in address or data fields or four bit data occurred when the machine expected eight bit data.
56	Address Range Error	The address field encountered on data input is outside the range of RAM addresses. The entry of the correct offset value when selecting input will allow for any value in the address field.

61	No RAM Installed	There is no data RAM.
62	Last RAM Not On 1K Boundary	The RAM in the machine is not an increment of 1K. Caused by hardware failure of RAM.
63	RAM Write Failure	The programmer was unable to write the intended data to RAM. This error indicates the failure of the associated RAM memory chip, and requires the replacement of the failing device.
64	RAM Data Failure	The programmer has detected a spurious change in RAM data.
65	Program Memory Failure	The sum-check of software residing in the installed programming electronics is in error.
66	Unidentified Interrupt	The IRQ line to the processor was held low for no apparent reason.
68	Data Locked	With data lock in effect, the programmer displays this message when a disallowed keystroke has been made, and also when Programming Paks are changed. RAM data remains intact.
70-79	Programming-Electronics Error	The programming module's software detected an error. Refer to the specific programming electronics Manual.
81	Parity Error	The incoming data was of incorrect parity.
82	Sum-Check Error	The sum-check field received by the programmer does not agree with its own calculated sum-check. For ASCII Binary formats, error message indicates missing F characters.
84	Invalid Data	Programmer received invalid characters or not enough data characters. These are: Non-data characters(Formats 01-03) Missing data characters(Formats 12, 13, 30-37 and 50-58) Non-hex characters(Formats 80-86)
83, 85, 86 and 87	Composite Error	A composite error occurs from any combination of errors 81, 82 and 84. These combinations are: Error 83 = errors 81 and 82 Error 85 = errors 81 and 84 Error 86 = errors 82 and 84 Error 87 = errors 81, 82 and 84
91	Address-Field Error	The programmer received an invalid character in the address field.
92	Address-Check Error	The address check was in error. Signetics Absolute Object and Tektronix Hexadecimal Formats only.
93	Record-Count Error	The number of input records did not equal the Record Count. MOS Technology Format only.
94	Record-Type Error	The record type was in error. Intel Intellec 8/MDS Format only.
95	Illegal Split or Shuffle	An attempt was made to perform 2 consecutive splits not preceeded by a shuffle or 2 consecutive shuffles not preceeded by a split.

96	Illegal Center Point	The center point specified for a split or shuffle is not a power of 2 or is greater than the midpoint of RAM.
97	Block-Move Parameters Out of Range	RAM is too small to achieve the desired RAM-RAM Block Move.
98	L2 + L3 Greater Than RAM	The sum of the specified Begin Device Address, L3, and the specified block size, L2, exceeds the capacity of RAM.

Programmer Configuration — System 17 / 19

A. MANUALS

The 026-1902 Rev. J manual consists of:

ITEM	QTY	PART NUMBER	DESCRIPTION	
1	1	035-1900	Operation and Maintenance Manual	E
2	1	055-1901	Translation Formats Package Manual	C
3	1	055-1902	Computer Remote Control Manual	C
4	1	990-1902	Programmer Configuration Sheet	J
5	1	004-1900	Operator's Synopsis	

B. HARDWARE

ITEM	QTY	PART NUMBER	DESCRIPTION	
1	1	901-1900	System 19	H
2	1	324-8002	FIRMWARE	
3	1	401-3064	Connector, Serial I/O	
4	1	401-3069	Hood, Serial I/O	
5	1	615-0019	Enclosure Assembly	D
6	1	750-0026	PCM Shield Assembly	A
7	1	415-2252	Label, Power and UL	A
8	1	950-1580	Expanded Program Memory	D
9	REF	001-1900	Test Procedure	

C. SOFTWARE

ON LABEL

ITEM	PROGRAM		DEVICE LOCATION	DEVICE TYPE	JUMPER NUMBER	JUMPER POS.	ASSEMBLY LISTING	REV	DESCRIPTION
1	324-8002-004		U29-1520	2716	JP4	AA	76-324-8002		1902 Option
2	324-8002-005		U30-1520	2716	JP5	AA			
3	324-8002-006		U31-1520	2716	JP6	AA			
4	324-8002-007		U32-1520	2716	JP7	AA			
5	324-8002-003		U8-1580	2716					
6	324-8002-002		U7-1580	2716					
7	324-8002-001		U6-1580	2716					

DATE	REV	REVISION RECORD	CK
9-20-82	J	ECN #4395	EF/

990 - 1902

SYSTEM 19 WITH COMPUTER REMOTE CONTROL

Serial No. _____

Software Configuration Check 41A4

DATA I/O

Programming systems for tomorrow...today

DATA I/O
SYSTEM 19 MANUAL
035-1900 REV. E OR LATER

CHANGE SHEET NOVEMBER 11, 1980

Make the following changes to this manual:

NO.	PAGE	
1	A-3	Error 98, L2 + L3 Greater Than RAM, should be changed to say "L2 + L3 Greater Than Device"; the error description should be changed to say "The sum of the specified Begin Device Address, L3, and the specified Block Size, L2, exceeds the word limit of the installed programming electronics (device size)."
2	2-4	To the NOTES in Figure 2-5, add the following: "4. Transmission faster than 600 baud is not possible when using the 20 mA current loop interface."
3	2-2	Section 2.4.1, 3rd paragraph: Change 2nd sentence from "Press gently on the module to ensure connector mating" to read "Press the module down and toward the rear of the programmer to ensure connector mating."
4	2-3	Figure 2-4(b). The baud rate selector switch may have the hexadecimal character set (0-9,A-F) instead of numerals (0-15). If so, add the following conversions to the table of Baud Rates: A = 2400; B = 3600; C = 4800; D = 7200; E = 9600; F = 19,200.