

501
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PERMISSION TECHNOLOGY
CORP.

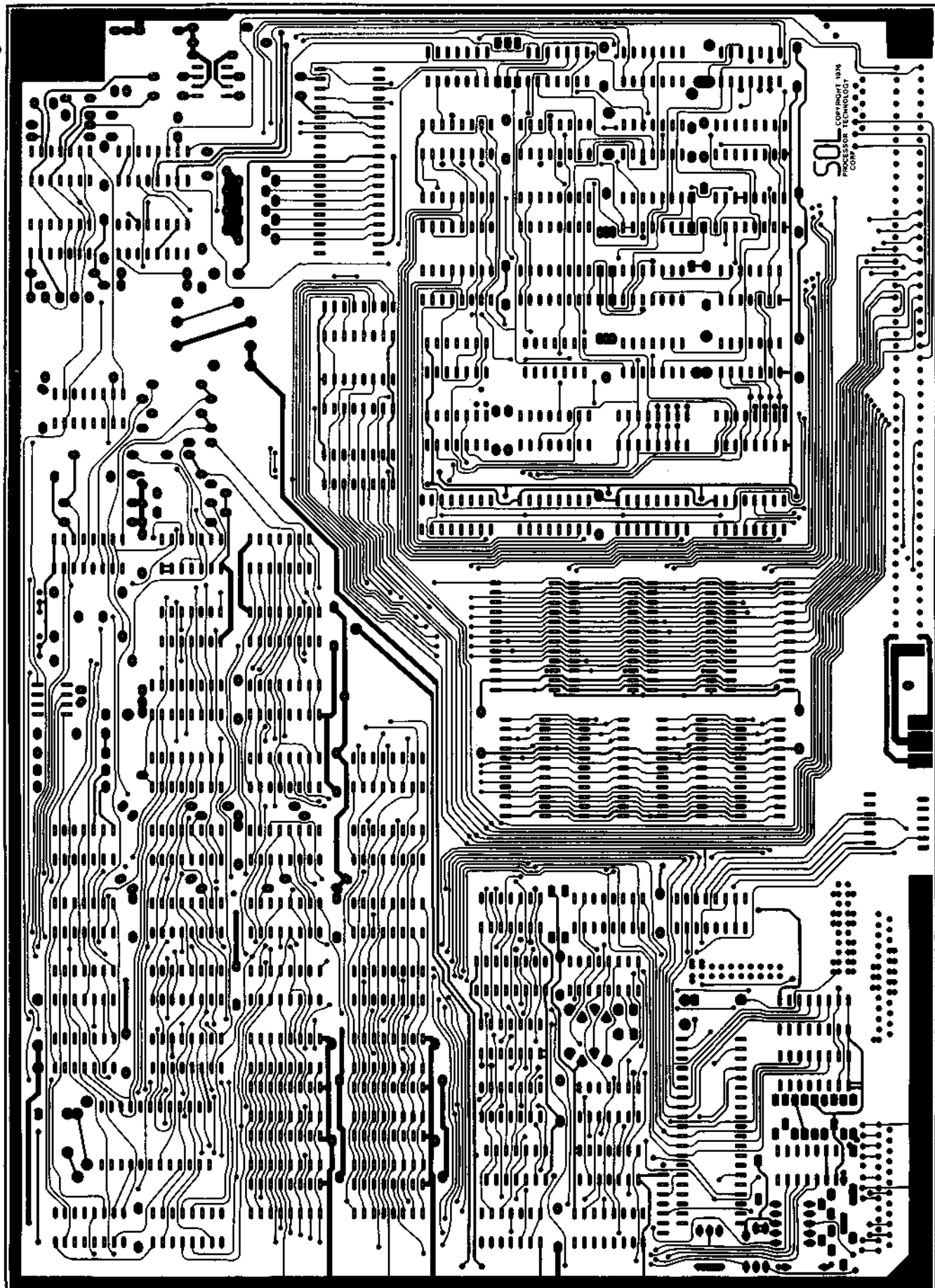
TOP



CC 2256

SOL
CORPORATION
PROCESSOR TECHNOLOGY

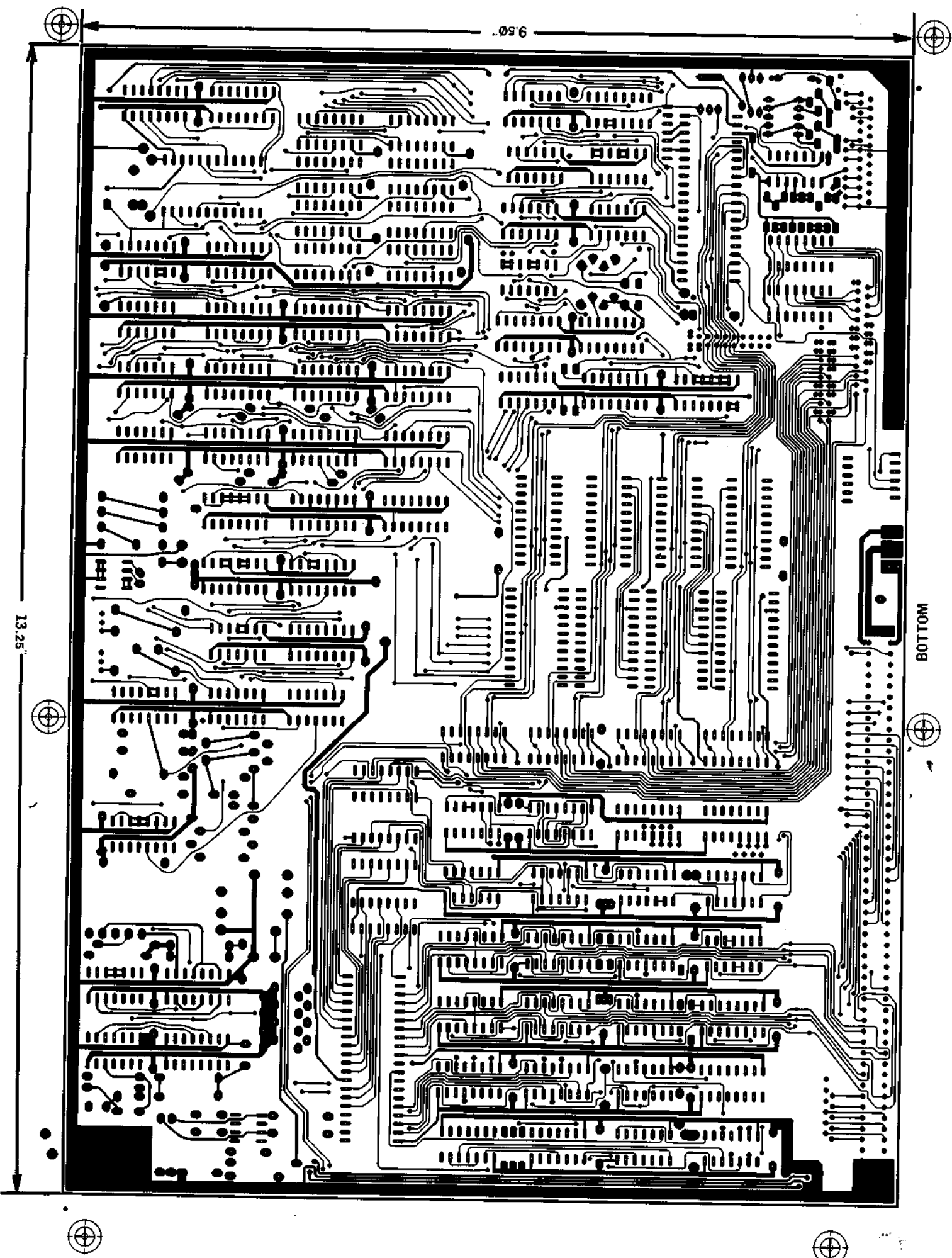
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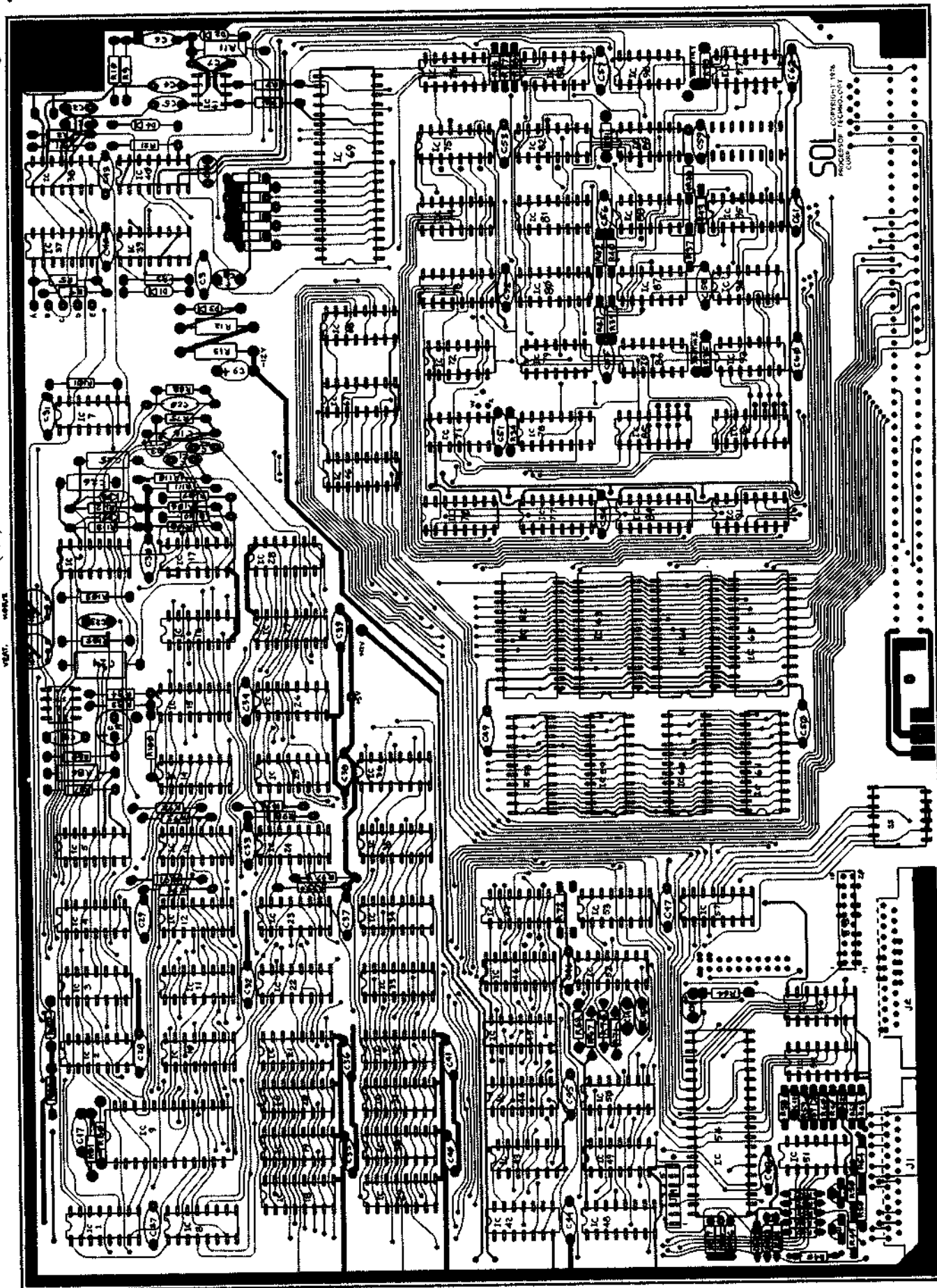


056

13.25

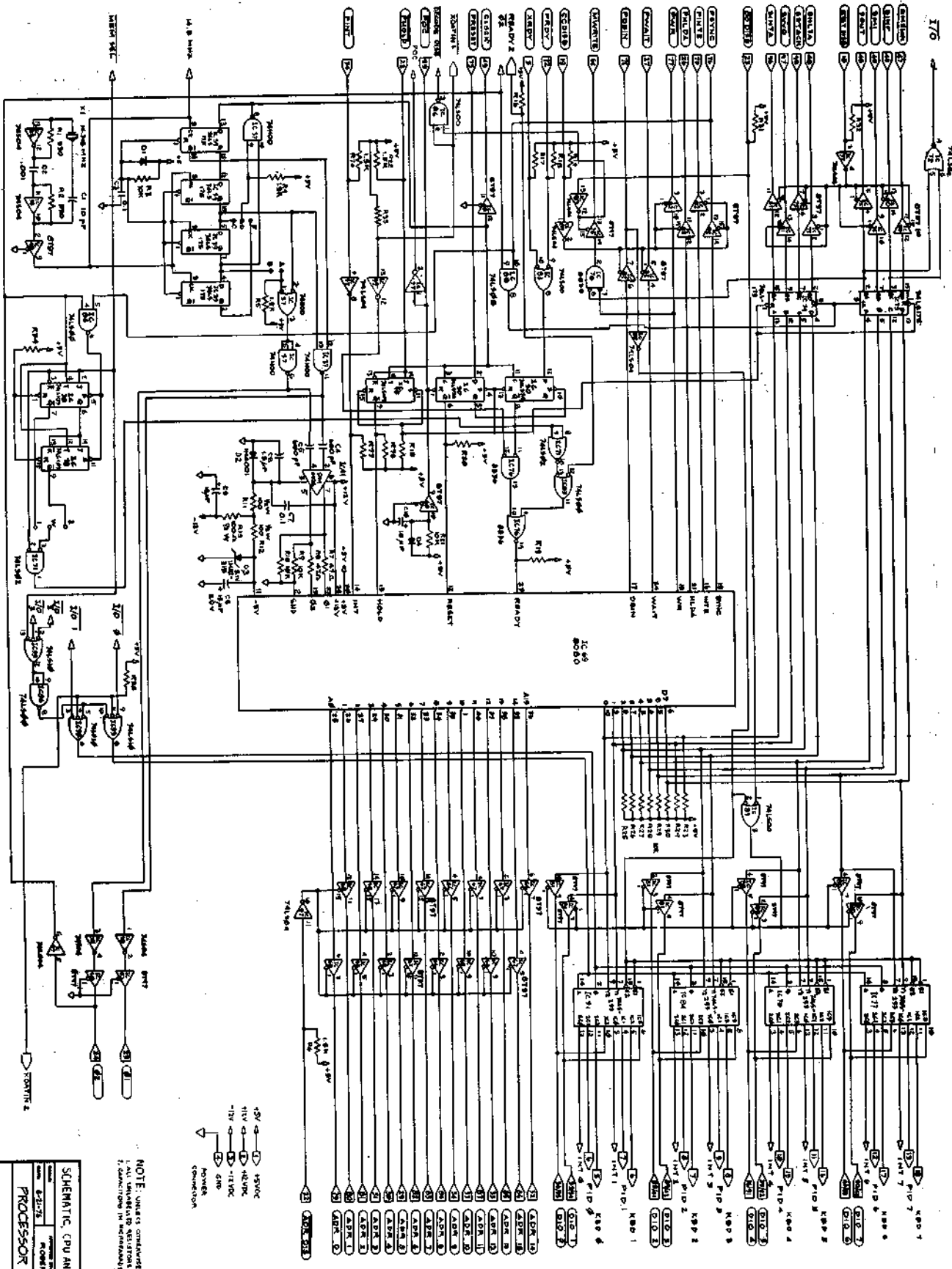
BOTTOM





COMPONENT LOCATION DIAGRAM Sol - I

TOP

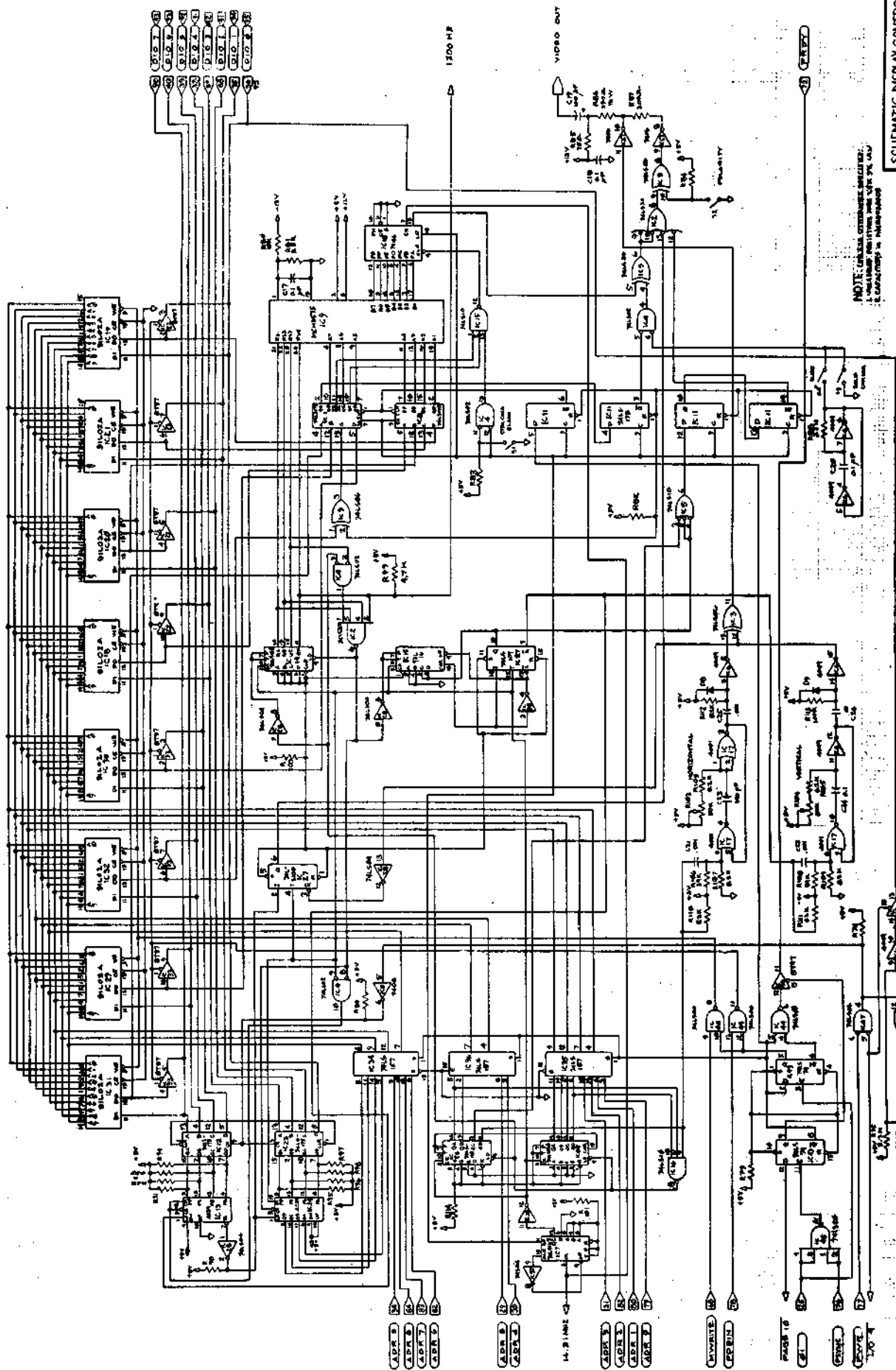


NOTE: UNLESS OTHERWISE SPECIFIED,
 ALL UNLABLED RESISTORS 1/4W 5%
 CAPACITORS IN MICROFARADS

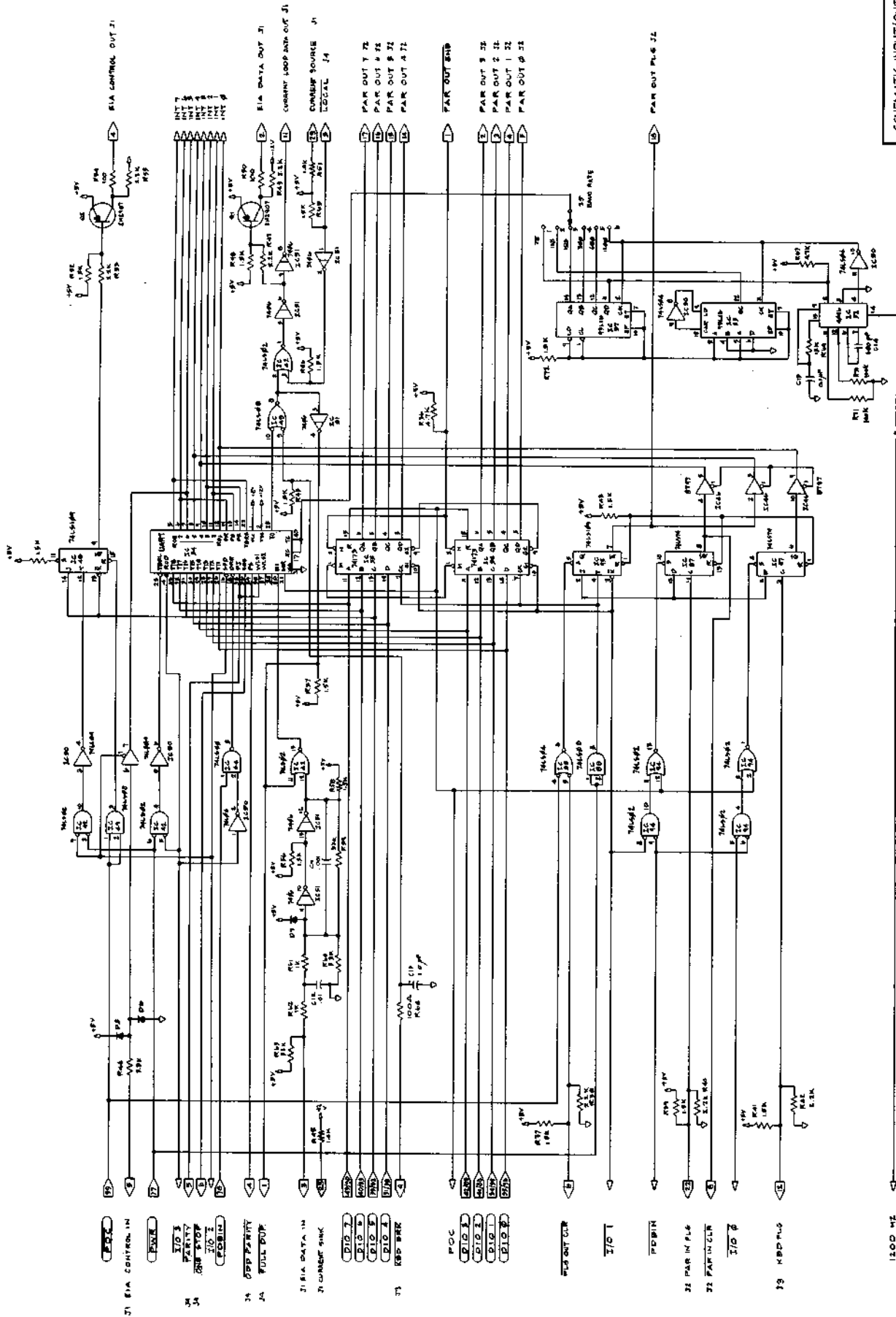
5V \rightarrow \square 5V05
 11V \rightarrow \square 11V05
 -12V \rightarrow \square 12V05
 \rightarrow \square 0V
 POWER CONNECTION

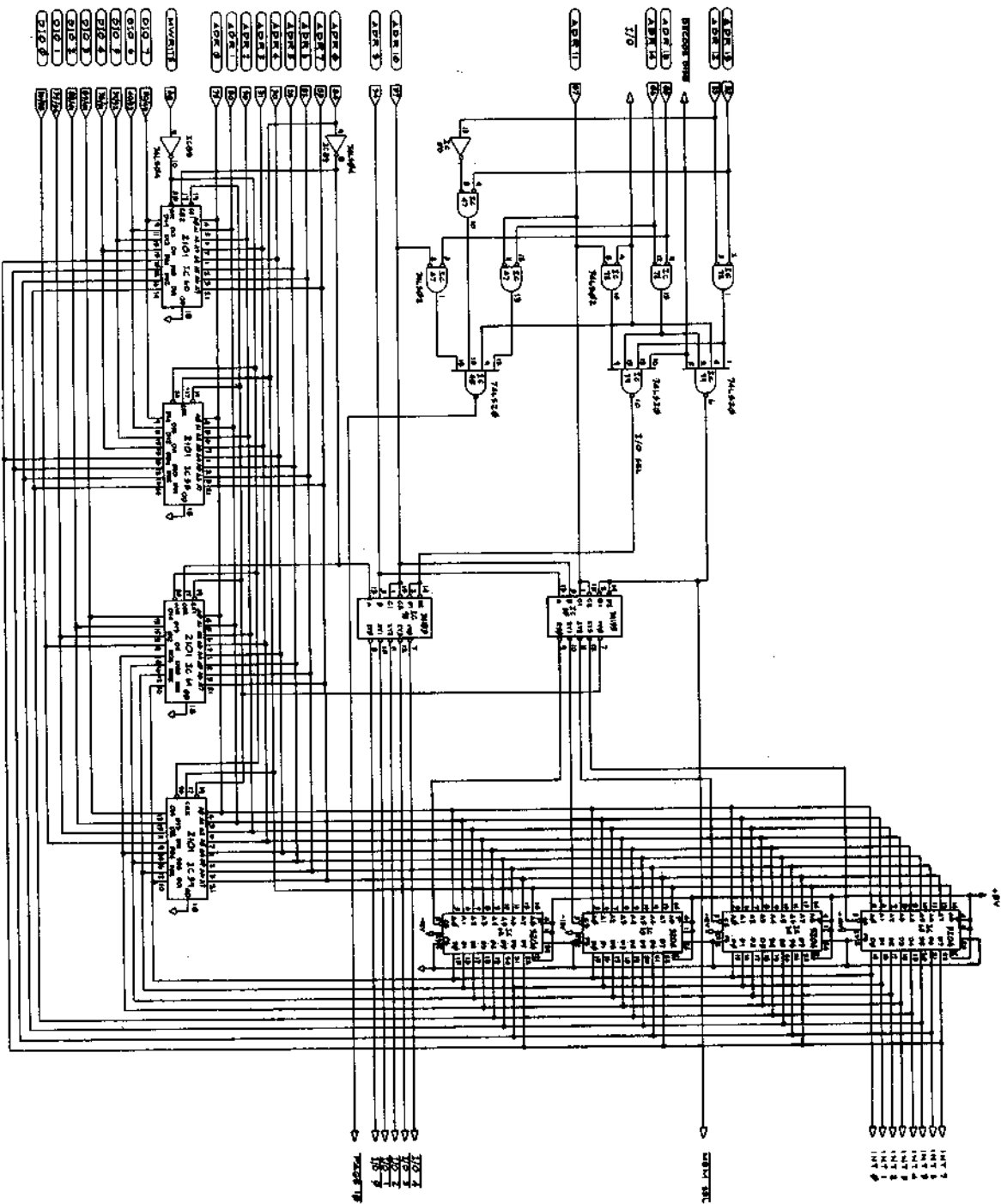
SCHEMATIC: CPU AND BUS, Sol-1

DATE: 8-21-78
 DESIGNER: ROBERT W. PHARSH
 CHECKER: JAMES L. LITTE
 PROJECT: PROCESSOR TECHNOLOGY



NOTE: CHECK ALL CONNECTIONS CAREFULLY.
 1. VERIFY ALL CONNECTIONS WITH DATA SHEET.
 2. CONFIRM ALL CONNECTIONS.





SCHEMATIC MEMORY, 501-I
 MODEL 5-327-76
 ROBERT N. MARSH
 PROCESSOR TECHNOLOGY
 1976