CZ80PIO
Peripheral Device Megafunction

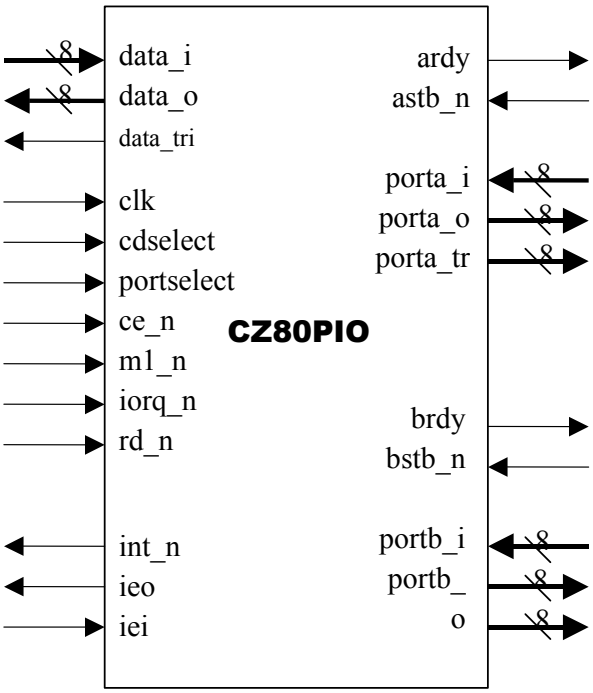
General Description

The CZ80PIO, hereinafter referred to as PIO, is a dual-port device which can be programmed by the system software to function as a broad range of peripheral devices that are compatible with the Z80CPU such as most keyboards, printers etc.

System design is simplified because the PIO connects directly to the Z80CPU with no additional logic. In larger systems, address decoders and buffers may be required.

The CZ80PIO is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous, with no internal tri-states and a synchronous reset.

Symbol



Features

- Provides a direct interface between Z80 microprocessor systems and peripheral devices
- Two ports with interrupt-driven handshake for fast response
- Four programmable operating modes:
  - Output Mode (both ports)
  - Input Mode (both ports)
  - Bi-directional (Port A only)
  - Bit Control Mode (both ports)
- Programmable interrupts on peripheral status conditions

Applications

- Programmable, dual - port device
- Interface for a wide range of peripheral devices such as:
  - Keyboards
  - Printers
  - Paper table readers
  - PROM programmers etc.

Pin Description

Name	Type	Description
Clock		
clk	In	System Clock
Interface to Processor		
data_tri	Out	Tristate controller for buffer for data bus
data_i	In	Data bus input
data_o	Out	Data bus output:
rd_n	In	Read Cycle Status
iorq_n	In	Input / Output Request
ce_n	In	Chip Enable
cdselect	In	Control / Data select
portselect	In	Port B / A select
m1_n	In	Machine Cycle One
Interrupt Service Routine		
int_n	In	Interrupt Request
iei	In	Interrupt Enable Input
ieo	Out	Interrupt Enable Output
Control		
porta_tri	In	Tristate controller for buffer for data bus
porta_i	In	Port B bus input
porta_o	Out	Port B bus output
portb_tri	In	Tristate controller for buffer for data bus
portb_i	In	Port B bus input
portb_o	Out	Port B bus output
ardy	Out	Register A ready
brdy	Out	Register B ready
astb_n	In	Port A strobe pulse from peripheral device
bstb_n	In	Port B strobe pulse from peripheral device

Functional Description

The CZ80PIO megafunction is partitioned into modules as shown in figure 1 and described below.

Port Logic

Each port contains separate input and output registers, handshake control logic and the control registers. All data transfers between the peripheral unit and the CPU use the data input and output registers. The handshake logic associated with each port controls the data transfers through the input and the output registers. The mode control register (two bits) selects one of the four programmable operating modes. The Bit Control mode (mode 3) uses the remaining registers. The input/output control register specifies which of the eight data bits in the port are to be outputs and enables these bits; the remaining bits are inputs. The mask register specifies which of the bits in the port are masked.

Control logic

The control logic consists of the CPU bus interface logic, interrupt control logic and internal control logic. The CPU bus interface logic interfaces the CZ80PIO directly to the CZ80CPU, so no external logic is necessary. For large systems, however, address decoders and/or buffers may be necessary. The interrupt control logic section handles all CPU interrupt protocol for nested-priority interrupt structures. Any device's physical location in a daisy-chain configuration determines its priority. Two lines (IEO and IEI) are provided in each PIO to form this daisy chain. The device closest to the CPU has the highest priority. Within a PIO, port A interrupts have higher priority then those of port B. In the byte input, byte output or bi-directional modes, an interrupt can be generated whenever the peripheral requests a new byte transfer. In the bit control mode, an interrupt can be generated when the peripheral status matches a programmed value.

Block Diagram

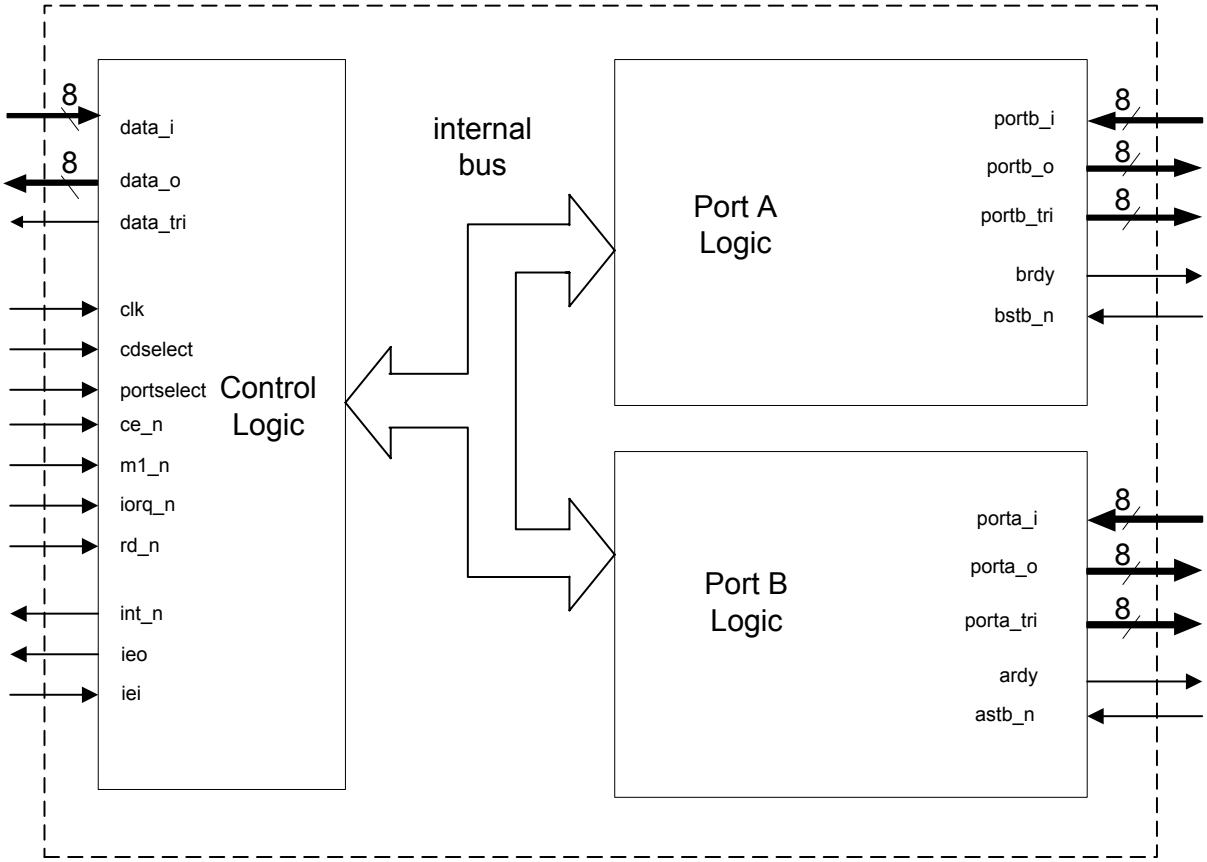


Figure 1. CZ80PIO Peripheral Device Block Diagram

Device Utilization & Performance

Supported Family	Device Tested	Utilization		Performance (MHz)
		LEs	Memory	
Flex	EPF10KE30-1	733	-	67 MHz
Acex	EP1K30-1	731	-	67 MHz
Apex	EP20KE30-1	748	-	70 MHz
Apex2	EP2A15-7	763	-	95 MHz
Cyclone	EP1C3-6	583	-	120 MHz
Stratix	EP1S10-5	583	-	132 MHz
Stratix-II	EP2S15-3	561	-	218 MHz

Notes:
1. Optimized for speed
2. Assumes all I/O is routed off-chip

Deliverables

Netlist License

- Post-synthesis EDIF netlist
- Testbench (self checking)
- Vectors for testing the functionality of the megafunction
- Place & Route Script
- Constraint file
- Simulation script
- Documentation

HDL Source License

- VHDL or Verilog RTL source code
- Testbench (self checking)
- Vectors for testing the functionality of the megafunction
- Simulation scripts
- Synthesis scripts
- Documentation

Verification Methods

The CZ80PIO megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Zilog Z80PIO chip, and the results compared with the megafunction's simulation outputs.

Megafunction Modifications

The CZ80PIO megafunction can be modified to include additional new ports. Please contact CAST, Inc. directly for any required modifications.

Contact Information

CAST, Inc.
11 Stonewall Court
Woodcliff Lake, New Jersey 07677 USA
Phone: +1 201-391-8300
Fax: +1 201-391-8694
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

This megafunction developed by peripheral controller experts at Evatronix SA