

<b>16K</b>	<b>Commercial Industrial</b>	<b>X2816B X2816BI</b>	<b>2048 x 8 Bit</b>
<b>Electrically Erasable PROM</b>			

### FEATURES

- **250 ns Access Time**
- **High Performance Advanced NMOS Technology**
- **Fast Write Cycle Times**
  - 16-Byte Page Write Operation
  - Byte or Page Write Cycle: 5 ms Typical
  - Complete Memory Rewrite: 640 ms Typical
  - Effective Byte Write Cycle Time of 300  $\mu$ s Typical
- **DATA Polling**
  - Allows User to Minimize Write Cycle Time
- **Simple Byte and Page Write**
  - Single TTL Level  $\overline{WE}$  Signal
  - Internally Latched Address and Data
  - Automatic Write Timing
- **JEDEC Approved Byte-Wide Pinout**

### DESCRIPTION

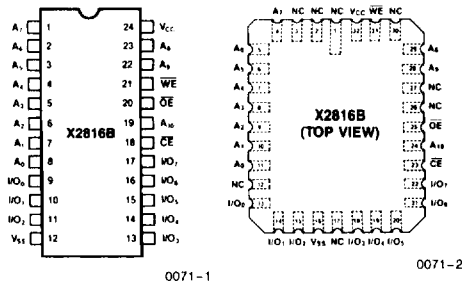
The Xicor X2816B is a 2K x 8 E<sup>2</sup>PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816B supports a 16-byte page write operation, typically providing a 300  $\mu$ s/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816B also features  $\overline{DATA}$  Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 100 years.

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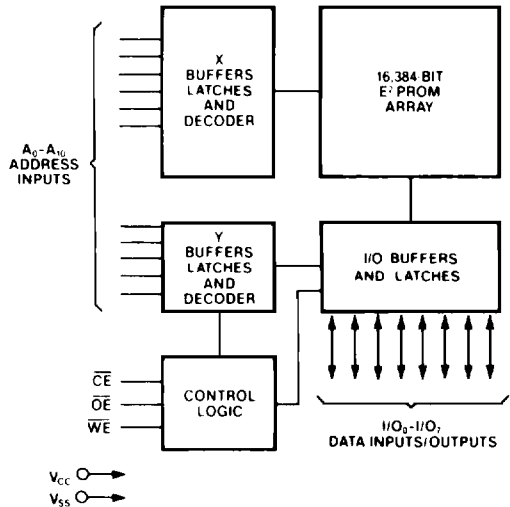
### PIN CONFIGURATIONS



### PIN NAMES

$A_0$ – $A_{10}$	Address Inputs
$I/O_0$ – $I/O_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$V_{CC}$	+5V
$V_{SS}$	Ground
NC	No Connect

### FUNCTIONAL DIAGRAM



0071-3

# X2816B, X2816BI

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X2816B	-10°C to +85°C
X2816BI	-65°C to +135°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground	-1.0V to +7V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

X2816B  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

X2816BI  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	X2816B/X2816B-25 Limits			X2816BI/X2816BI-25 Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.		
$I_{CC}$	$V_{CC}$ Current (Active)		80	120		80	140	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = $V_{CC}$
$I_{SB}$	$V_{CC}$ Current (Standby)		45	60		45	70	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = $V_{CC}$
$I_{LI}$	Input Leakage Current			10			10	$\mu\text{A}$	$V_{IN} = \text{GND to } V_{CC}$
$I_{LO}$	Output Leakage Current			10			10	$\mu\text{A}$	$V_{OUT} = \text{GND to } V_{CC}$ , $\overline{CE} = V_{IH}$
$V_{IL}$	Input Low Voltage	-1.0		0.8	-1.0		0.8	V	
$V_{IH}$	Input High Voltage	2.0		$V_{CC} + 1.0$	2.0		$V_{CC} + 1.0$	V	
$V_{OL}$	Output Low Voltage			0.4			0.4	V	$I_{OL} = 2.1 \text{ mA}$
$V_{OH}$	Output High Voltage	2.4			2.4			V	$I_{OH} = -400 \mu\text{A}$

## TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
$t_{PUR}^{(2)}$	Power-Up to Read Operation	1	ms
$t_{PUW}^{(2)}$	Power-Up to Write Operation	5	ms

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0 \text{ MHz}$ ,  $V_{CC} = 5\text{V}$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(2)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(2)}$	Input Capacitance	6	pF	$V_{IN} = 0\text{V}$

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100 \text{ pF}$

## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	$D_{OUT}$	Active
L	H	L	Write	$D_{IN}$	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

**Notes:** (1) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

(2) This parameter is periodically sampled and not 100% tested.

# X2816B, X2816BI

## A.C. CHARACTERISTICS

X2816B  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

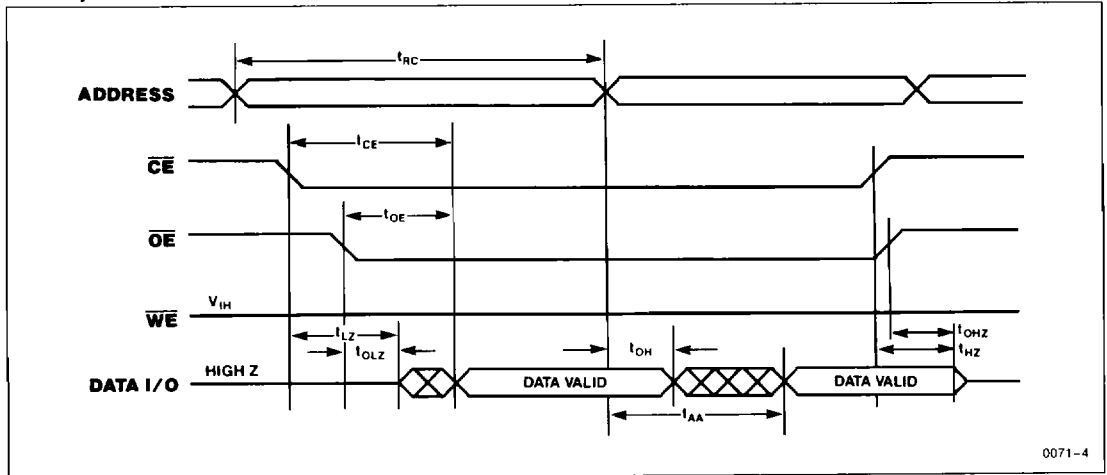
X2816BI  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

### Read Cycle Limits

Symbol	Parameter	X2816B-25 X2816BI-25		X2816B X2816BI		Units
		Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	250		300		ns
$t_{CE}$	Chip Enable Access Time		250		300	ns
$t_{AA}$	Address Access Time		250		300	ns
$t_{OE}$	Output Enable Access Time		100		100	ns
$t_{LZ}$	Chip Enable to Output in Low Z	10		10		ns
$t_{HZ}^{(3)}$	Chip Disable to Output in High Z	10	60	10	80	ns
$t_{OLZ}$	Output Enable to Output in Low Z	10		10		ns
$t_{OHZ}^{(3)}$	Output Disable to Output in High Z	10	60	10	80	ns
$t_{OH}$	Output Hold from Address Change	10		10		ns

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### Read Cycle



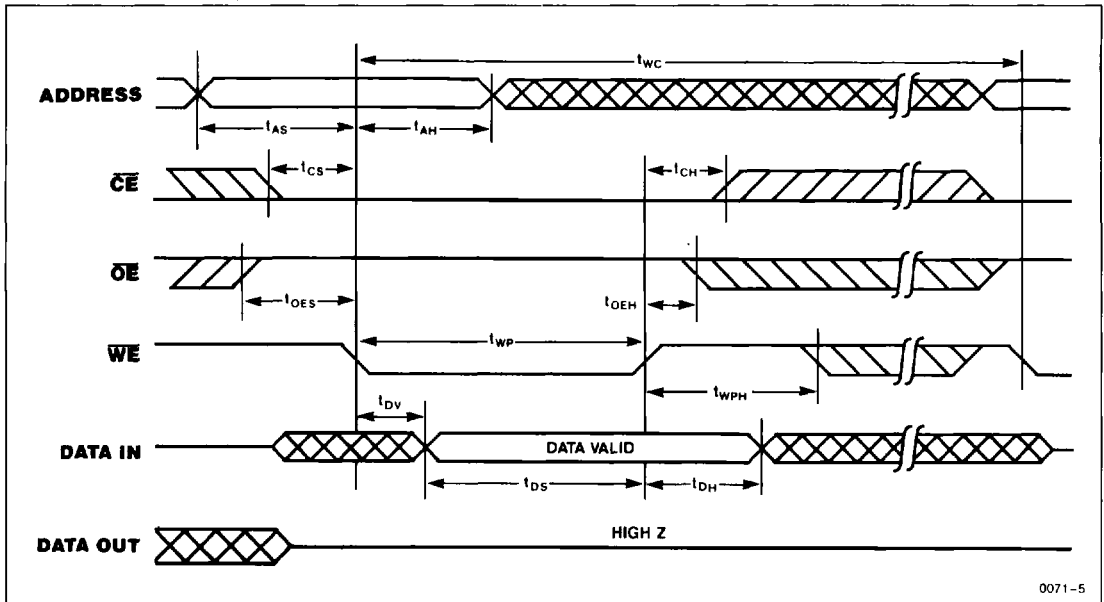
Note: (3)  $t_{HZ}$  and  $t_{OHZ}$  are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

# X2816B, X2816BI

## Write Cycle Limits

Symbol	Parameter	Min.	Typ.(4)	Max.	Units
$t_{WC}$	Write Cycle Time		5	10	ms
$t_{AS}$	Address Setup Time	10			ns
$t_{AH}$	Address Hold Time	150			ns
$t_{CS}$	Write Setup Time	0			ns
$t_{CH}$	Write Hold Time	0			ns
$t_{CW}$	$\overline{CE}$ Pulse Width	150			ns
$t_{OES}$	$\overline{OE}$ High Setup Time	10			ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	10			ns
$t_{WP}$	$\overline{WE}$ Pulse Width	150			ns
$t_{WPH}$	$\overline{WE}$ High Recovery	50			ns
$t_{DV}$	Data Valid			300	ns
$t_{DS}$	Data Setup	100			ns
$t_{DH}$	Data Hold	15			ns
$t_{DW}$	Delay to Next Write	500			$\mu$ s
$t_{BLC}$	Byte Load Cycle	3		20	$\mu$ s

## $\overline{WE}$ Controlled Write Cycle

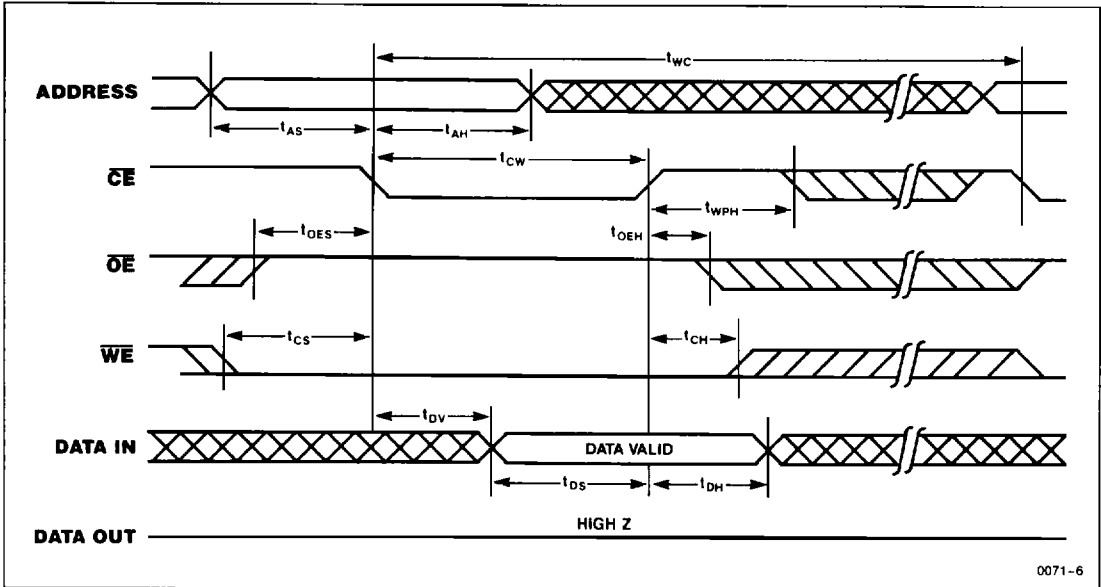


Note: (4) Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltage.

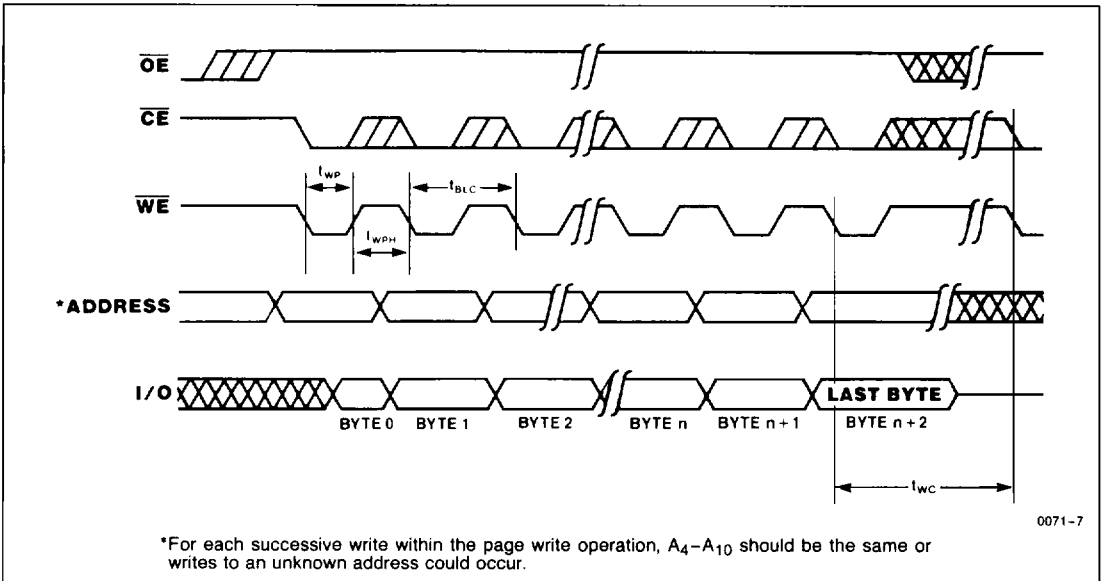
# X2816B, X2816BI

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## CE Controlled Write Cycle

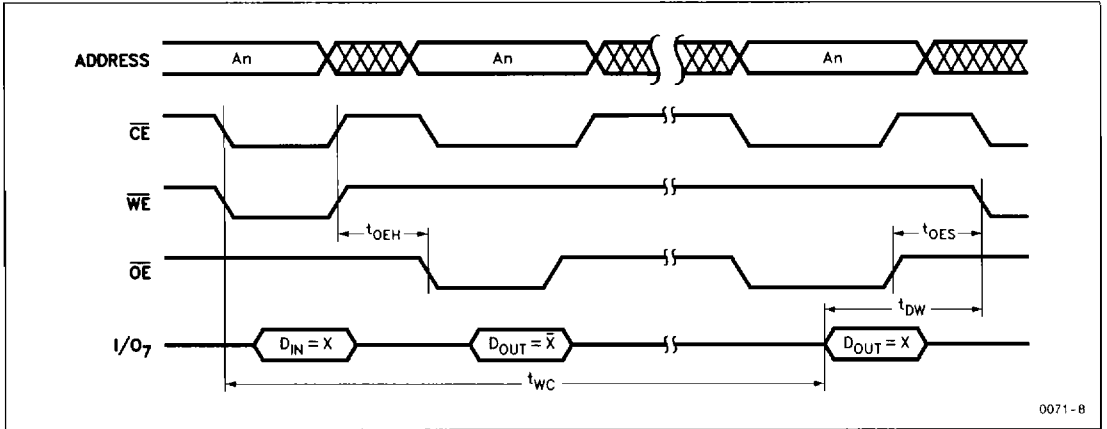


## Page Mode Write Cycle



# X2816B, X2816BI

## DATA Polling Timing Diagram



## X2816B, X2816BI

### PIN DESCRIPTIONS

#### Addresses ( $A_0$ – $A_{10}$ )

The Address inputs select an 8-bit memory location during a read or write operation.

#### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

#### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read operations.

#### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X2816B through the I/O pins.

#### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to the X2816B.

### DEVICE OPERATION

#### Read

Read operations are initiated by both  $\overline{OE}$  and  $\overline{CE}$  LOW. The read operation is terminated by either  $\overline{CE}$  or  $\overline{OE}$  returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH.

#### Write

Write operations are initiated when both  $\overline{CE}$  and  $\overline{WE}$  are LOW and  $\overline{OE}$  is HIGH. The X2816B supports both a  $\overline{CE}$  and  $\overline{WE}$  controlled write cycle. That is, the address is latched by the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs last. Similarly, the data is latched internally by the rising edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

#### Page Write Operation

The page write feature of the X2816B allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816B prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816B, the destination page address of the X2816B should be the same on each subsequent strobe of the  $\overline{WE}$  and  $\overline{CE}$  inputs. That is,  $A_4$

through  $A_{10}$  must be the same for each transfer of data to the X2816B during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the  $\overline{WE}$  HIGH to LOW transition, must begin within 20  $\mu$ s of the falling edge of the preceding  $\overline{WE}$ . If a subsequent  $\overline{WE}$  HIGH to LOW transition is not detected within 20  $\mu$ s, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20  $\mu$ s.

#### DATA Polling

The X2816B features  $\overline{DATA}$  Polling as a method to indicate to the host system that the byte write or page write cycle has completed.  $\overline{DATA}$  Polling allows a simple bit test operation to determine the status of the X2816B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on  $I/O_7$  (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete,  $I/O_7$  will reflect true data.

#### WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A  $\overline{WE}$  pulse of less than 20 ns will not initiate a write cycle.
- $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3V$ , typically.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH or  $\overline{CE}$  HIGH during power-on and power-off, will inhibit inadvertent writes.

#### ENDURANCE

Xicor E<sup>2</sup>PROMs are designed and tested for applications requiring extended endurance. The process average for endurance of Xicor E<sup>2</sup>PROMs is approximately 1/2 million cycles, as documented in RR504, the *Xicor Reliability Report on Endurance*. Included in that report is a method for determining the expected endurance of the device based upon the specific application environment. RR504 and additional reliability reports are available from Xicor.

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## X2816B, X2816BI

### SYSTEM CONSIDERATIONS

Because the X2816B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

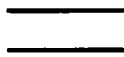



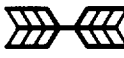
To gain the most benefit it is recommended that  $\overline{CE}$  be decoded from the address bus and be used as the primary device selection input. Both  $\overline{OE}$  and  $\overline{WE}$  would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2816B has two power modes, standby and active, proper decoupling of the memory array is of

prime concern. Enabling  $\overline{CE}$  will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1  $\mu\text{F}$  high frequency ceramic capacitor be used between  $V_{CC}$  and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7  $\mu\text{F}$  electrolytic bulk capacitor be placed between  $V_{CC}$  and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

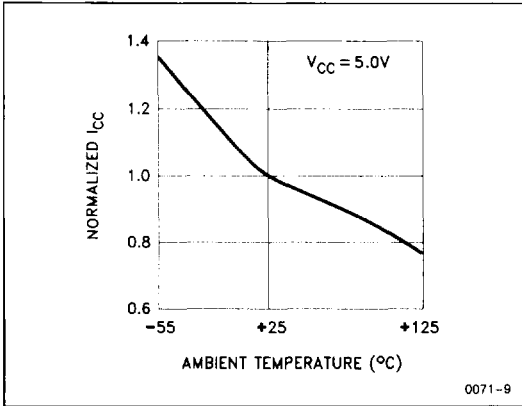
**SYMBOL TABLE**

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care : Changes Allowed	Changing : State Not Known
	N/A	Center Line is High Impedance

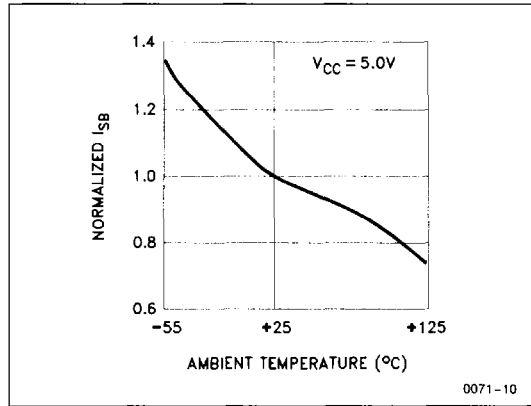


# X2816B, X2816BI

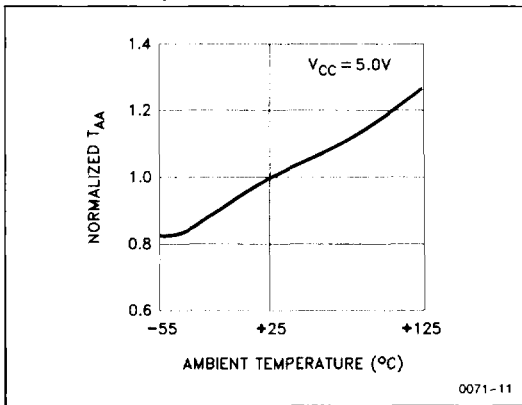
**Normalized Active Supply Current vs. Ambient Temperature**



**Normalized Standby Supply Current vs. Ambient Temperature**



**Normalized Access Time vs. Ambient Temperature**



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