HIGH SPEED 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 45 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
  — ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS27C256F is a 32K x 8 CMOS EPROM which has been speed-enhanced to 45 ns. It is based upon WaferScale's patented CMOS Split Gate EPROM technology.

The 45 ns access time of the WS27C256F is a key parameter. Traditionally, as memory densities increase, memory access times become slower. This forces microprocessors to insert Wait States which negatively impact system throughput. Real Time applications cannot afford Wait States regardless of memory density. WSI's unique memories can keep pace with the fastest microprocessors. The combination of speed and density available in the WS27C256F enables the use of more complex and comprehensive algorithms in real time applications.

WSI's patented CMOS Split-Gate EPROM technology not only enables the development of fast and dense memory products, it also provides a higher level of Quality and Reliability. Tests have proven that WSI EPROM products program very efficiently and quickly. Also, the WSI EPROM retains its data an order of magnitude better than traditional EPROM technologies. This combination of speed, density, quality and reliability make WSI the obvious choice when selecting a non-volatile memory supplier.

The WS27C256F is configured in the JEDEC standard EPROM pin configuration. It is also easily programmed on popular EPROM programmers as well as the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

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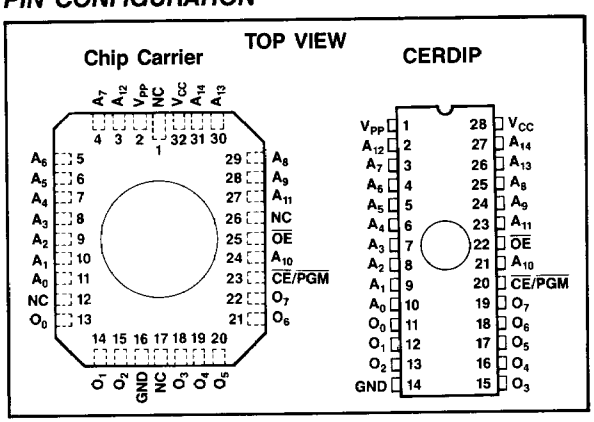
MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE E0H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-45	WS27C256F-55	WS27C256F-70	WS27C256F-90
Address Access Time (Max)	45 ns	55 ns	70 ns	90 ns
Chip Select Time (Max)	45 ns	55 ns	70 ns	90 ns
Output Enable Time (Max)	25 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65° to +150°C
Voltage on Any Pin with
Respect to GND ..... −0.6V to +7V
V_{PP} with respect to GND ..... −0.6V to +13V
ESD Protection ..... >2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0°C to +70°C	+5V ± 5%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

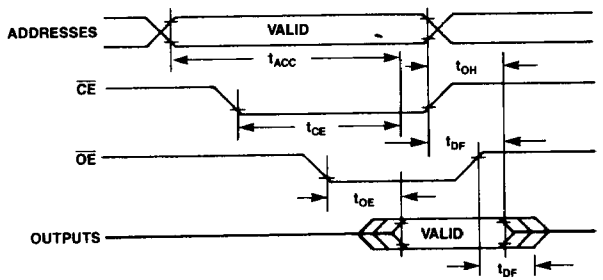
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} ± 0.3V (Note 1)		500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = V_{IH} (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current[3]	Commercial		30	mA
		Military		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	27C256F-45		27C256F-55		27C256F-70		27C256F-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		45		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		45		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		25		30		30	
Output Disable to Output Float	t_{DF}		25		25		30		30	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM



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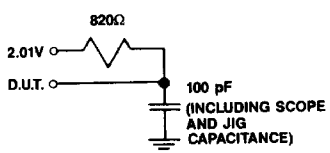
CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0.45 and 2.4V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

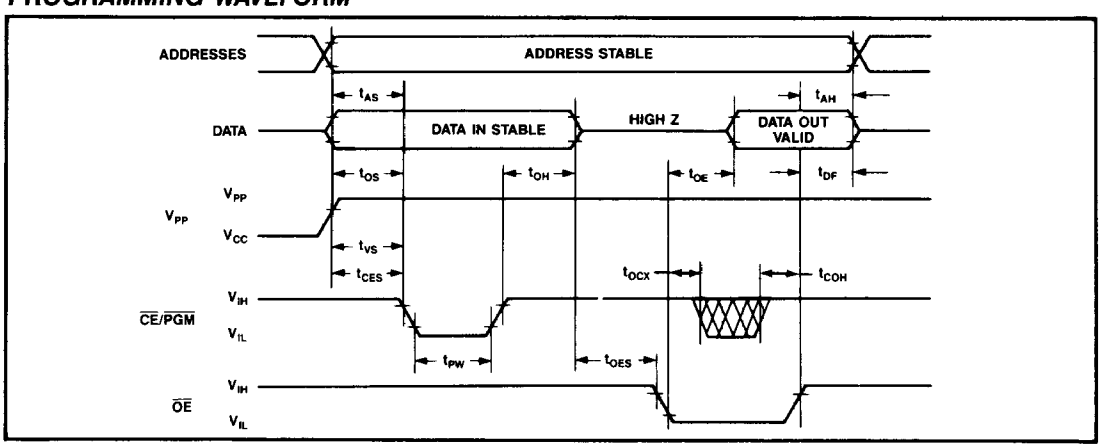
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

NOTE: These values are for standard programming — actual programming algorithm may use different limitations.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-45D*	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90LMB	90	32 Pin CLDCC	L3	Military	MIL-STD-883C

*This product is Advance Information.

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