HIGH SPEED 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 8510207**
- **EPI Processing**
  - — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Available in PLDCC**

GENERAL DESCRIPTION

The WS57C64F is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming very little power.

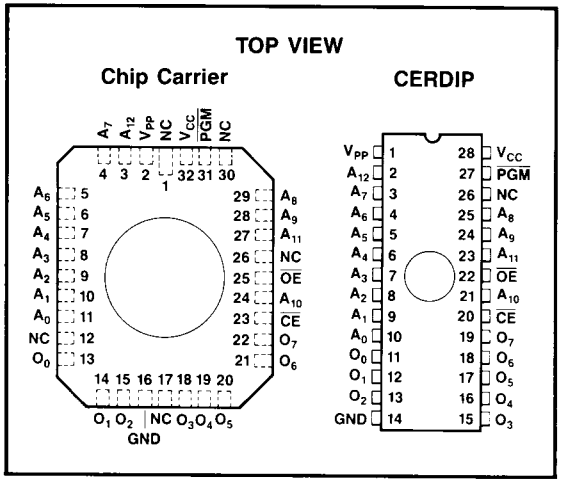
Two major features of the WS57C64F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include modems, secure telephones, servo controllers, and industrial controllers.

The WS57C64F is configured in the standard EPROM pinout which provides an easy upgrade path to higher density EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	X	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	V_{CC}	High Z

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C64F-55	WS57C64F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	20ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature.....−65° to + 150°C

Voltage on any Pin with
Respect to Ground .....−0.6V to +7V

V_{PP} with Respect to Ground.....−0.6V to + 14V

ESD Protection.....>2000V

***NOTICE:**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

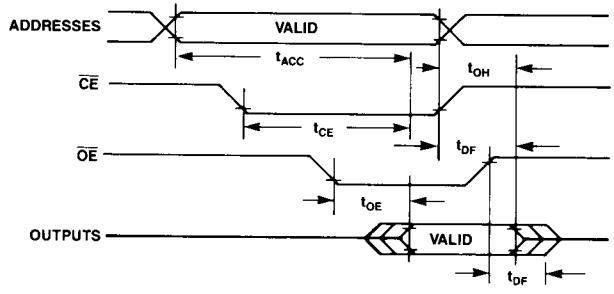
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 5)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3 V (Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH} (Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		20	mA
			Industrial		30	mA
			Military		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		25	mA
			Industrial		35	mA
			Military		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

PARAMETER	SYMBOL	WS57C64F-55		WS57C64F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM

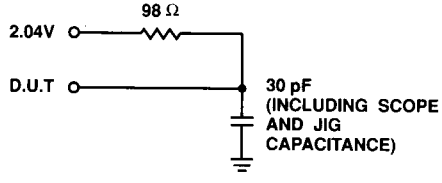


CAPACITANCE (6) T_A = 25°C, f = 1 MHz

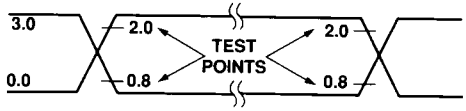
SYMBOL	PARAMETER	CONDITIONS	TYP (7)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

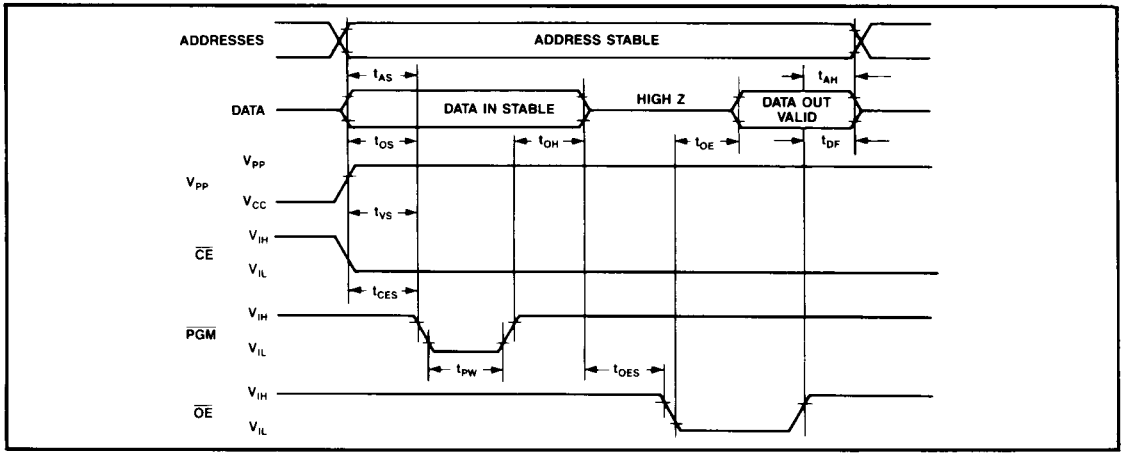
SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.6V ± 0.25V, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C64F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C64F-70CMB*	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C64F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C64F-70DMB*	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C64F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard

NOTES: 12. The actual part marking will not include the initials "WS."

*SMD product. See section 5 for DESC SMD number.

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

REFER TO PAGE 6-1

The WS57C64F is programmed using Algorithm A shown on page 6-3.