T-46-13-29

LH57191/LH57191J CMOS 16K (2K×8) OTPROM/EPROM T-46-13-25

Description

The LH57191 is an extremely high performance 16K UV erasable electrically programmable read only memory organized as 2,048×8 bits. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 75mA.

The LH57191J is packaged in 24-pin CERDIP which is pin-compatible to bipolar PROM.

The LH57191 is a one time PROM packaged in plastic DIP.

Features

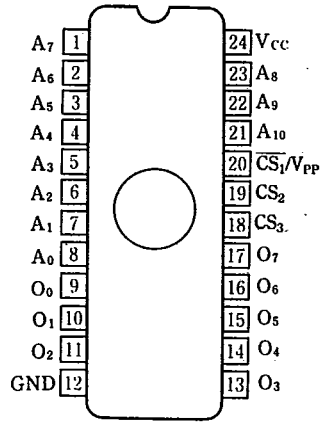
1. 2,048×8 bit organization
2. Low power consumption: 398mW (MAX.)
3. Access time
   LH57191J: 55/70ns (MAX.)
   LH57191: 70ns (MAX.)
4. Single +5V power supply
5. Fully static operation
6. All inputs and outputs TTL compatible
7. Pin compatible with Bipolar PROM
8. Three-state output
9. Output hold time (after address change) : 10ns
10. EPROM
    24-pin CERDIP (WDIP24-G-600)
    OTPROM
    24-pin DIP (DIP24-P-600)
    24-pin SK-DIP (DIP24-P-300)

Ordering Information

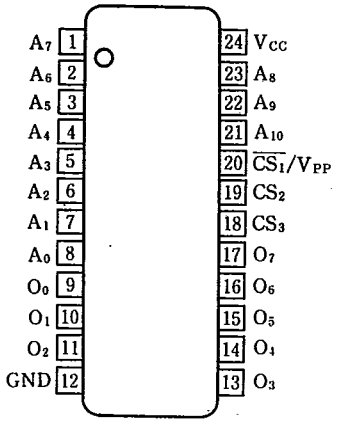
LH57191 X-XX
- Access time
  - 55: 55ns
  - 70: 70ns
- Package
  - [EPROM]
    - J: 24-pin CERDIP (WDIP24-G-600)
  - [OTPROM]
    - Blank: 24-pin DIP (DIP24-P-600)
    - D: 24-pin SK-DIP (DIP24-P-300)
- Model No.

Pin Connections

LH57191J



LH57191D



Top View

Pin Description

Signal	Pin name
A_0-A_{10}	Address input
O_0-O_7	Data output
$\overline{CS_1}/V_{PP}$	Chip select/Program power
CS_2, CS_3	Chip select input
V_{CC}	Power supply (+5V)
GND	Ground

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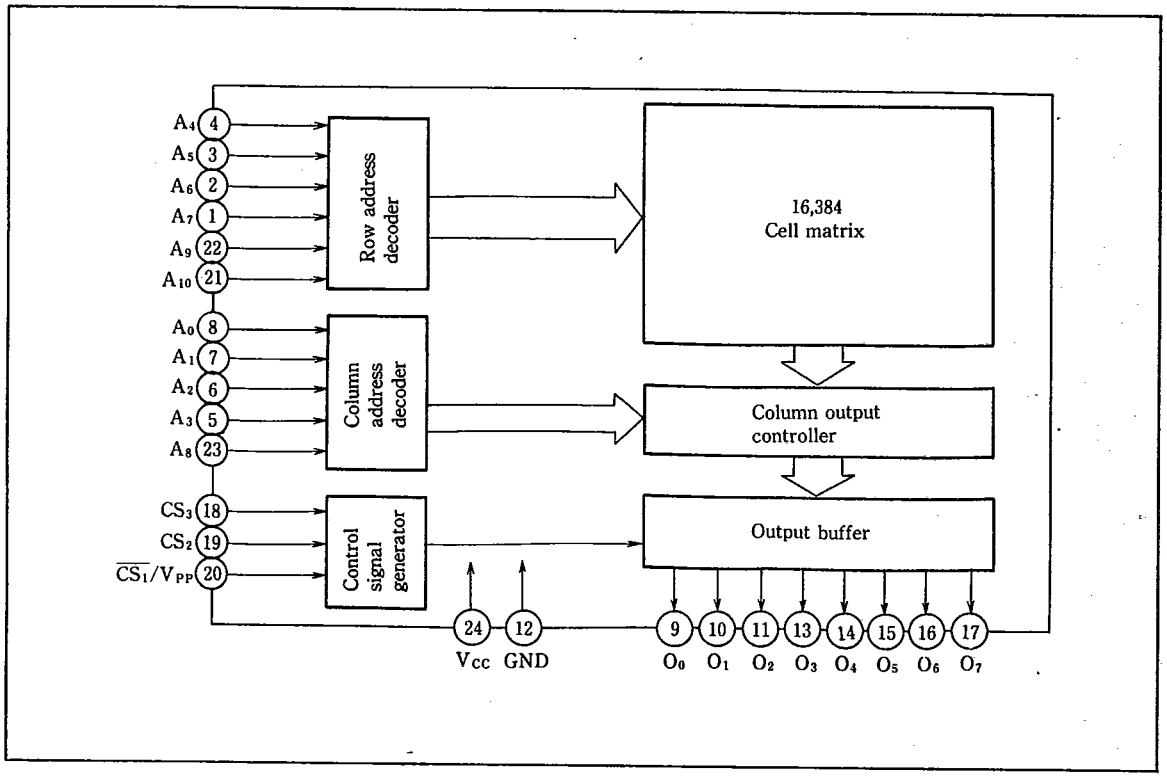
Block Diagram



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Truth Table

Mode		O_0-O_7	$\overline{CS_1}/V_{PP}$	CS_2	CS_3	V_{CC}	Note
Read	Read	D_{OUT}	L	H	H	+5V	1
	Output disable	High Z	H	X	X	+5V	
			X	L	X	+5V	
			X	X	L	+5V	
Program	Program	D_{IN}	V_{PP}	X	X	+6V	
	Program inhibit	High Z	H	X	X	+6V	
	Program verify	D_{OUT}	L	H	H	+6V	

Note 1: H=V_{IH}, L=V_{IL}, X=H or L

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	−0.6 to +7.0	V	1
	$\overline{CS}/V_{PP}$	−0.6 to +14.0		
	V_{IN}, V_{OUT}	−0.6 to +7.0		
Operating temperature	Topr	0 to+ 70	℃	
Storage temperature	Tstg	−65 to +150	℃	2
		−55 to +150		3

Note 1: The maximum applicable voltage on any pin with respect to GND. Maximum ratings are those values beyond which damage to the device may occur.
Note 2: Applied to ceramic package.
Note 3: Applied to plastic package.

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Recommended Operating Conditions (Read mode)

(Ta=0 to +70℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input "High" voltage	V_{IH}	−0.1		0.8	
Input "Low" voltage	V_{IL}	2.0		V_{CC}+0.3	

DC Characteristics (Read mode)

(V_{CC}=5V±5%, Ta=0 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	I_{LI}	V_{IN}=GND or V_{CC}	−10		10	μA	
Output leakage current	I_{LO}	V_{OUT}=GND or V_{CC}	−10		10	μA	
V_{CC} operating current	I_{CC1}	CMOS input			75	mA	1, 2
	I_{CC2}	TTL input			75	mA	1, 3
Input " Low" voltage	V_{IL}		−0.1		0.8	V	
Input " High " voltage	V_{IH}		2.0		V_{CC}+0.3	V	
Output "Low " voltage	V_{OL}	I_{OL}=16mA			0.45	V	
Output "High " voltage	V_{OH}	I_{OH}=−4mA	2.4			v	

Note 1: Minimum cycle time, I_{OUT}=0mA
Note 2: V_{IN}=GND±0.3V or V_{CC}±0.3V
Note 3: V_{IN}=V_{IL} or V_{IH}

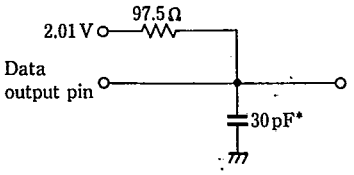
AC Characteristics (Read mode)

(V_{CC}=5V±5%, Ta=0 to +70℃)

Parameter	Symbol	LH57191J-55		LH57191J-70 LH57191/D-70		Unit
		MIN.	MAX.	MIN.	MAX.	
Address valid to output valid	t_{ACC}		55		70	ns
Chip select to output valid	t_{CS}		25		30	ns
Chip disable to output in High Z	t_{DF}	0	20	0	30	ns
Output hold from address	t_{OH}	10		10		ns

AC test conditions

- Input voltage amplitude ..... 0V to 3V
- Input rise/fall time ..... ≦10ns
- Input reference level 1V,2V
- Output reference level 0.8V,2V



*Includes scope and jig capacitance

Output load circuit

Capacitance

(Ta=25℃,f=1MHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN}=0V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT}=0V		8	12	pF

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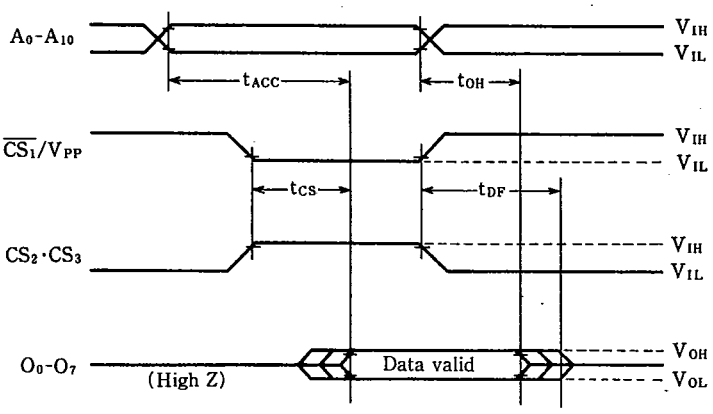
Timing Diagram (Read mode)



Recommended Operating Conditions (Program mode)

(Ta=25℃ ±5℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	5.75	6.0	6.25	V
Program voltage	$\overline{CS}/V_{PP}$	12.7	13.0	13.3	V
Input "Low" voltage	V_{IL}	−0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC}+0.3	V

DC Characteristics (Program mode)

(V_{CC}=6.0V±0.25V, $\overline{CS_1}/V_{PP}$ level=13.0V±0.3V, Ta=25℃ ±5℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	$V_{IN}=V_{CC}$ or 0.45V	−10		10	μA
$\overline{CS_1}/V_{PP}$ current	I_{PP}	Programming			75	mA
V_{CC} supply current	I_{CC}				75	mA
Input "Low" voltage	V_{IL}		−0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC}+0.3	V
Output "Low" voltage	V_{OL}	I_{OL}=16mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH}=−4mA	2.4			V

Note 1: The program pulse $\overline{CS_1}/V_{PP}$ must be applied after V_{CC} is stabled and cut before V_{CC} is turned off.
Note 2: $\overline{CS_1}/V_{PP}$ must not be greater than 14 volts including overshoot.

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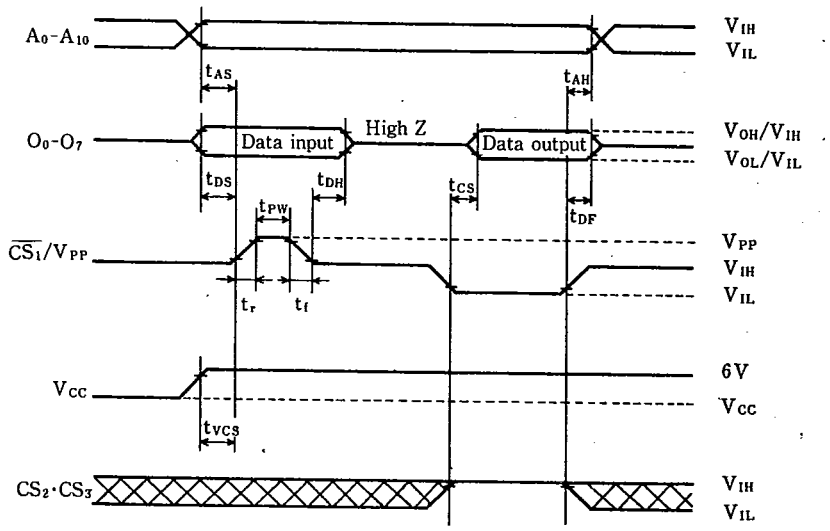
AC Characteristics (Program mode)

(V_{CC}=6.0V±0.25V, $\overline{CS_1}/V_{PP}$=13.0V±0.3V, Ta=25℃±5℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}	2			μs
$\overline{CS_1}/V_{PP}$ rise time	t_r	1		100	μs
$\overline{CS_1}/V_{PP}$ fall time	t_f	1		100	μs
Data setup time	t_{DS}	2			μs
Chip select delay time	t_{CS}			30	ns
Data hold time	t_{DH}	2			μs
Output disable time	t_{DF}			30	ns
V_{CC} setup time	t_{VCS}	2			μs
$\overline{PGM}$ pulse width	t_{PW}	0.95	1.0	1.05	ms
Add $\overline{PGM}$ pulse width*	t_{OPW}	2.85		78.75	ms
Program pulse count	N	1		25	TIMES

* The t_{OPW} is defined by the Program Flowchart.

Timing Diagram (Program mode)



Programming

Upon delivery from Sharp or after each erasure (See Erasure section), the LH57191J has all 2,048×8 bits in the "1", or high state. "0's" are loaded into the LH57191J through the procedure of programming.

The programming mode is entered when +12.5V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the LH57191J to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase an LH57191J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2537 Angstroms (Å)) with intensity of 12000 μW/cm^2 for 20 to 30 minutes. The LH57191J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57191J and similar devices, will erase with light sources, having wave-length shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57191J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Caution

The fluoresent-light and sunlight include UV ray which will erase written program of EPROM.

To prevent from deterioration of reliability of EPROM due to UV ray, it is recommended that EPROMs should not be left under direct sunlight of fluorescent light, or the package window should be covered with an opaque label.

Care must be taken not to cause the faulty operation due to friction between package window and plastics or the like.

Programming Flowchart