SMOS SYSTEMS

64K BIT CMOS UV EPROM/OT PROM

SPM27C64H15 • SPM27C64H20
SPM27C64C15 • SPM27C64C20

SPM27C64

04/1811

■DESCRIPTION

The CMOS EPROM SPM27C64H15/20 is an 8,192 words × 8 bits erasable and electrically programmable ROM. The peripheral CMOS circuit realizes High-speed and Low supply current. The SPM27C64H15/20 is packaged in a 28-pin CERDIP with a transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device. The SPM27C64C15/20* is a one time programmable ROM, packaged in a 28-pin plastic dual-in-line package. Its functions and characteristics are same as the SPM27C64H15/20 except that the SPM27C64C15/20* allows one time writing only.

■FEATURES

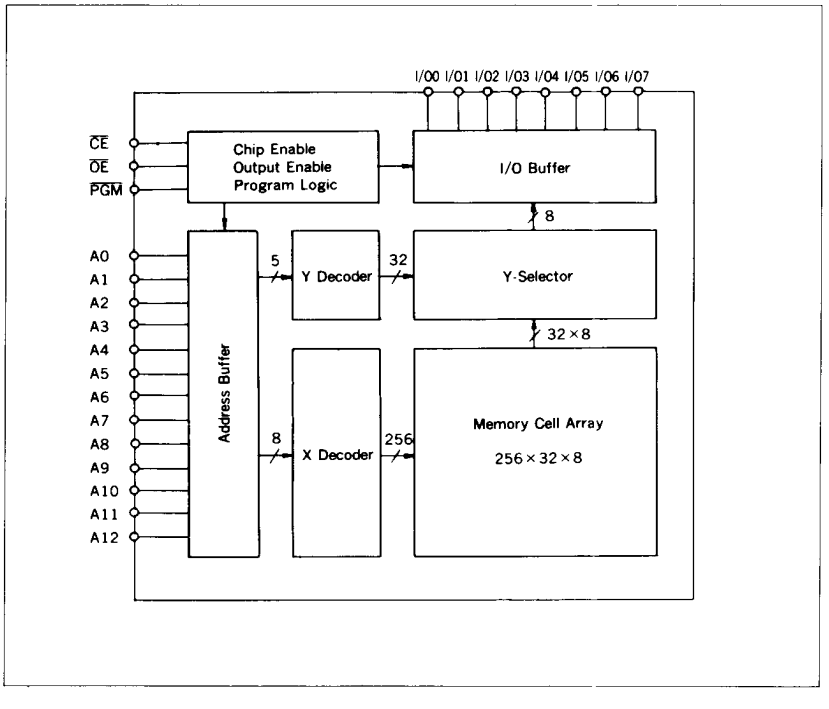
- ●Fast access time ·····SPM27C64H15 150ns (Max)
  SPM27C64H20 200ns (Max)
- ●Low supply current ·····Standby : 1μA (Typ)
  Operation : 30mA (Max)
- ●Simple programming ·····Program voltage +21V
  Program with one 50ms pulse
- ●Completely static ·····No clock required
- ●Single power supply ·····5V±10%
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Package·····SPM27C64H15/20 — 28-pin CERDIP with transparent lid
  SPM27C64C15/20* (OT PROM) — 28-pin DIP (plastic)

DIP

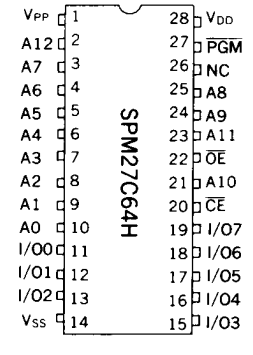
1544

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A12	Address Input
CE	Chip Enable
OE	Output Enable
PGM	Program Input
I/O0 to I/O7	Data I/O
VPP	Power Supply for Program
VDD	Power Supply (5V)
VSS	Power Supply (0V)
NC	No connection

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■SPM27C64H SERIES

Model	Access time	Function	Package
SPM27C64H$_{15}$	150ns	UV EPROM	28-pin CERDIP with transparent lid
SPM27C64H$_{20}$	200ns		
SPM27C64C$_{15}$	150ns	One Time PROM	28-pin DIP (plastic)
SPM27C64C$_{20}$	200ns		

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage*1	V_{DD}	−0.6 to 7.0	V
Supply voltage for programming*1	V_{PP}	−0.6 to 22	V
Input voltage*1	V_I	−0.6 to 7.0	V
Output voltage*1	V_O	−0.6 to 7.0	V
Output current	I_O	10	mA
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

*1 With respect to V_{SS}

■ELECTRICAL CHARACTERISTICS

Read Mode

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, V_{PP}=V_{DD}±0.6V, Ta= 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+1.0	V
Low level input voltage	V_{IL}		−0.6	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}$=V_{DD}±0.3V	—	1	100	μA
Operating supply current	I_{DDO}	Output open	—	—	30	mA
Programming supply current	I_{PP}		—	—	100	μA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	−10.0	—	10.0	μA
High level output voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V

●Terminal Capacitance

(f=1.0MHz, Ta=25°C)

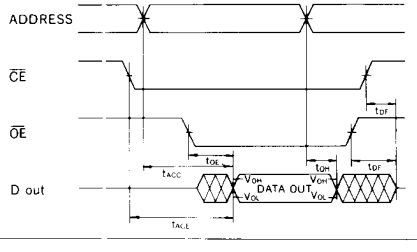
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	—	6	pF
Output Capacitance	C_O	V_O=0V	—	—	12	pF

●AC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, V_{PP}=V_{DD}±0.6V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SPM27C64H$_{15}$		SPM27C64H$_{20}$		Unit
			Min	Max	Min	Max	
Address access time	t_{ACC}	CL=1TTL+100pF V_{IH}=2.2V V_{IL}=0.8V V_{OH}=1.5V V_{OL}=1.5V t_r=t_f=20ns	—	150	—	200	ns
Chip enable access time	t_{ACE}		—	150	—	200	ns
Output enable access time	t_{OE}		—	60	—	70	ns
Output floating	t_{DF}		—	50	—	60	ns
Output hold time	t_{OH}		0	—	0	—	ns

●Timing Chart



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●Standby mode

When $\overline{CE}$ is "H" the SPM27C64H15/20 is in the standby mode. Then, Data I/O terminals are Hi-z, and all of address inputs are prohibited.

●Program

Initially, and after each erasure, all bits of the SPM27C64H15/20 are in the "H" state.

Data are programmed when a 50ms "L" pulse is applied to the $\overline{PGM}$ input while $\overline{CE}$ is kept "L" and the address and data are stable.

●Program verify

The verify on the programmed bits is performed with $\overline{CE}$ and $\overline{OE}$ at "L" level, $\overline{PGM}$ at "H" level and V_{PP} at 21V.

●Program inhibit

A "H" level $\overline{CE}$ input inhibits program while V_{PP} is 21V.

●High performance program

This SPM27C64H15/20 can be applied the High Performance Programming algorithm shown in the flowchart.

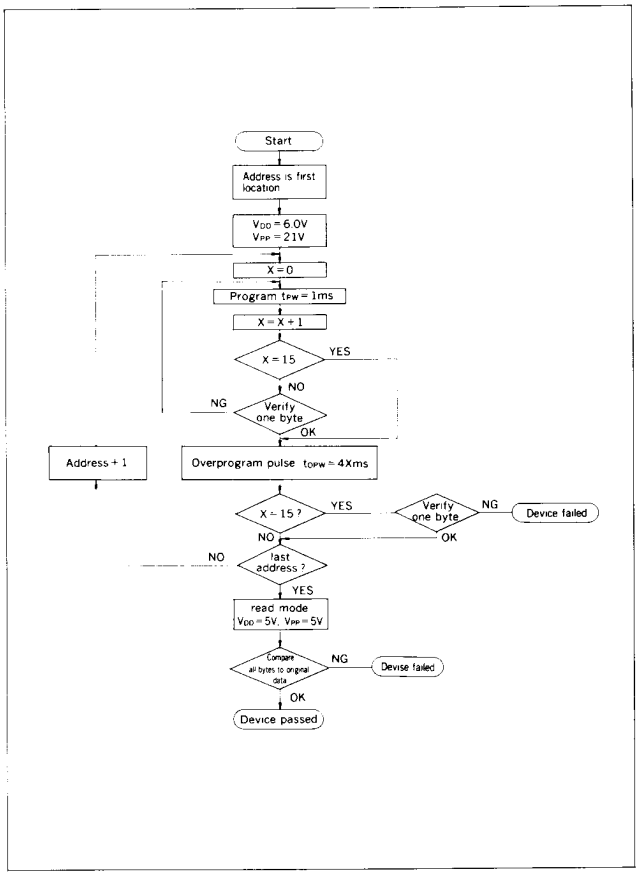
The 1 ms initial "L" pulse is applied to $\overline{PGM}$ for a first address with V_{DD} at 6V, and V_{PP} at 21V. After that, the data programmed should be verified. This procedure should be repeated X times ($X \leqq 15$) until the data of a word are correctly programmed.

After the data programmed are verified to be correct, the 4X ms overprogram pulse is applied. If the data are not programmed correctly with 15 times initial pulse, a 60 ms overprogram pulse should be applied.

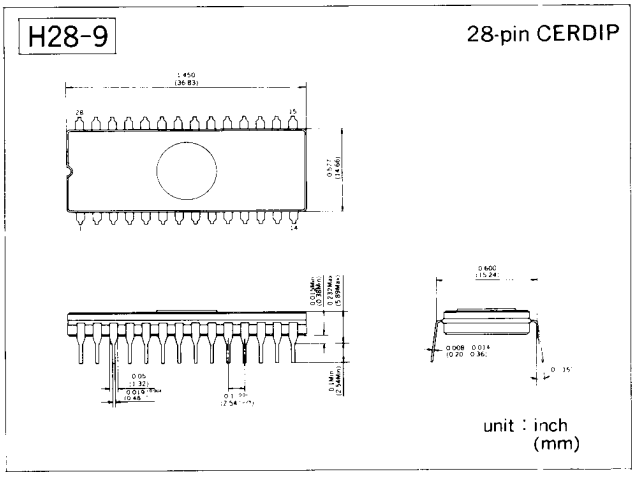
The same procedures for each address should be performed up to the last address.

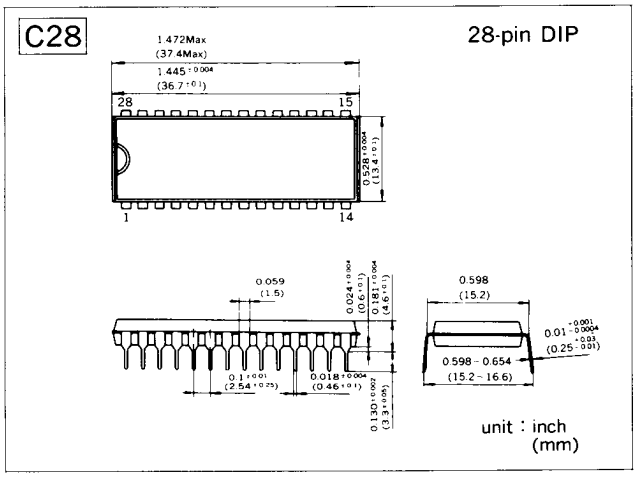
When the high performance programming cycle has been completed, all bytes should be compared to the original data with $V_{DD} = V_{PP} = 5V$.

●High Performance Program Flowchart



■PACKAGE DIMENSIONS





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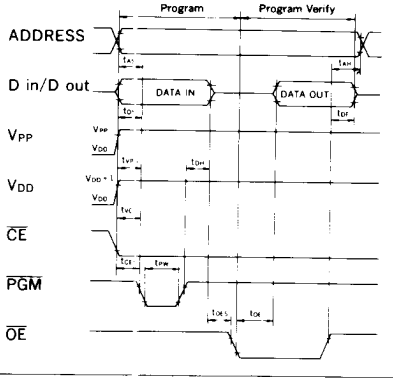
●AC Electrical Characteristics

(V_{DD} = 6 ±0.25V, V_{SS} = 0V, V_{PP} = 21 ±0.5V, Ta = 25 ±5°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address setup time	t_{AS}		2	—	—	μs
Chip enable setup time	t_{CES}		2	—	—	μs
Output enable setup time	t_{OES}		2	—	—	μs
Data setup time	t_{DS}		2	—	—	μs
Address hold time	t_{AH}		0	—	—	μs
Data hold time	t_{DH}		2	—	—	μs
Output floating	t_{DF}		0	—	130	ns
Output enable access time	t_{OE}		—	—	150	ns
V_{PP} setup time	t_{VPS}		2	—	—	μs
V_{DD} setup time	t_{VCS}		2	—	—	μs
$\overline{PGM}$ initial pulse width	t_{PW}		0.95	1.0	1.05	ms
$\overline{PGM}$ overprogram pulse width	t_{OPW}		3.8	—	63	ms

●Timing Chart



■ERASE

Erasure of SPM27C64H15/20 is performed by exposure to ultraviolet light of 2737 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2

■FUNCTIONS

●Truth Table

Mode \ Pin name	Address input A0 to A12	Data I/O I/O0 to I/O7	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{DD}	V_{PP}
Read	Stable	Output data	L	L	H	V_{DD}	V_{DD}
Output disable	Stable	Hi-Z	L	H	X	V_{DD}	V_{DD}
				X	L		
Standby	X	Hi-Z	H	X	X	V_{DD}	V_{DD}
Programming	Stable	Input data	L	X	L	V_{DD}	V_{PP}
Program verify	Stable	Output data	L	L	H	V_{DD}	V_{PP}
Program inhibit	X	Hi-Z	H	X	X	V_{DD}	V_{PP}

X : "H" or "L"

●Reading data

Data is able to be read by setting addresses during holding $\overline{CE}$ = "L", $\overline{OE}$ = "L" and $\overline{PGM}$ = "H".

●Output disable

Data I/O terminals are Hi-Z when $\overline{OE}$ = "H" or $\overline{PGM}$ = "L"

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Programming Mode

●DC Electrical Characteristics

(V_{DD}=5V±5%, V_{SS}=0V, V_{PP}=21±0.5V, Ta=25±5°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		−0.1	—	0.8	V
Input leakage current	I_{LI}	V_I=5.25V/0.45V	−2.0	—	2.0	μA
V_{DD} supply current	I_{DDO}		—	—	30	mA
V_{PP} supply current	I_{PP}	$\overline{CE}=\overline{PGM}=V_{IL}$	—	—	30	mA
High level output voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V

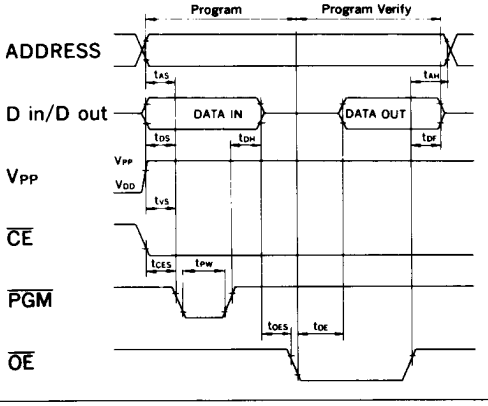
●AC Electrical Characteristics

(V_{DD}=5V±5%, V_{SS}=0V, V_{PP}=21±0.5V, Ta=25±5°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address setup time	t_{AS}		2	—	—	μs
Chip enable setup time	t_{CES}		2	—	—	μs
Output enable setup time	t_{OES}		2	—	—	μs
Data setup time	t_{DS}		2	—	—	μs
Address hold time	t_{AH}		0	—	—	μs
Data hold time	t_{DH}		2	—	—	μs
Output floating	t_{DF}		0	—	130	ns
Output enable access time	t_{OE}		—	—	150	ns
V_{PP} setup time	t_{VS}		2	—	—	μs
$\overline{PGM}$ pulse width during programming	t_{PW}		25	50	55	ms

*t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

●Timing Chart



High Performance Programming Mode

●DC Electrical Characteristics

(V_{DD}= 6 ±0.25V, V_{SS}=0V, V_{PP}=21±0.5V, Ta=25±5°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		−0.1	—	0.8	V
Input leakage	I_{LI}	V_I=5.25V/0.45V	−2.0	—	2.0	μA
Operating supply current	I_{DDO}		—	—	30	mA
Programming supply current	I_{PP}		—	—	30	mA
High level output voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.45	V

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