SMOS SYSTEMS

256K BIT CMOS UV EPROM

SPM27C256H$_{20}$ • SPM27C256H$_{25}$

Dup

SPM27C256

1543

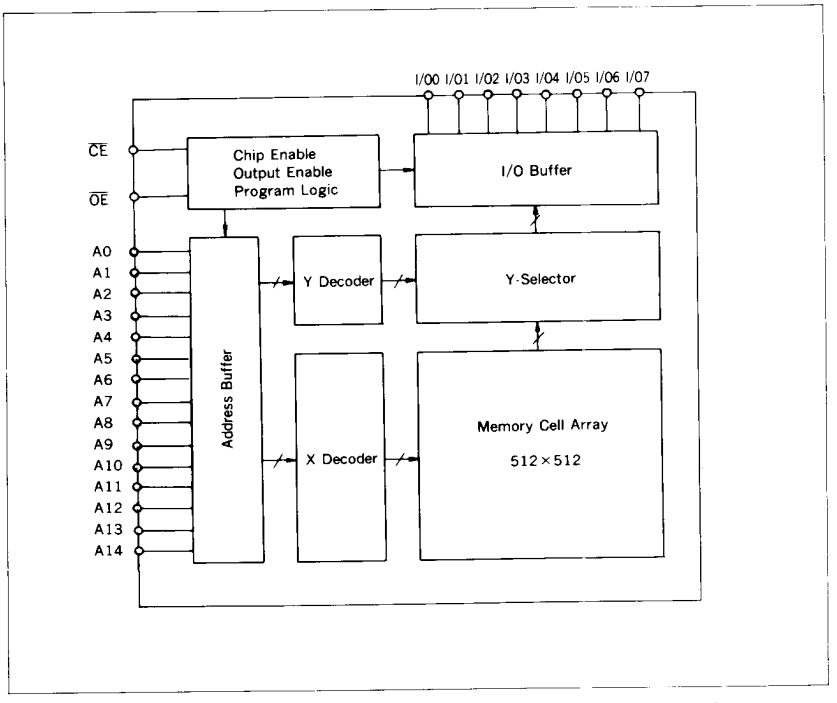
■DESCRIPTION

The CMOS EPROM SPM27C256H$_{20/25}$ is a 32,768 words×8 bits erasable and electrically programmable ROM. The peripheral CMOS circuit realizes High-speed and Low supply current. The SPM27C256H$_{20/25}$ is packaged in a 28-pin CERDIP with a transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device.

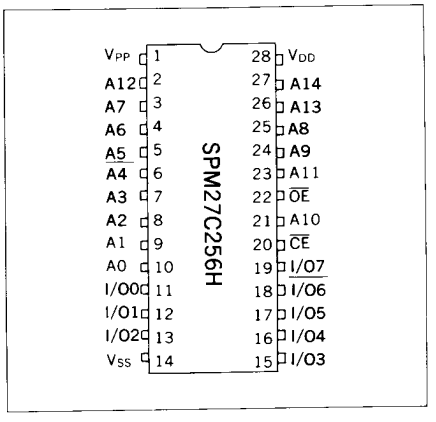
■FEATURES

- ●Fast access time ····· SPM27C256H$_{20}$ 200ns (Max)
  SPM27C256H$_{25}$ 250ns (Max)
- ●Low supply current ····· Standby : 1μA (Typ)
  Operation : 8mA/MHz (Max)
- ●Simple programming ····· Program voltage : 12.5V
- ●Completely static ····· No clock required
- ●Single power supply ····· 5V±5%
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Package ····· 28-pin CERDIP with transparent lid

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A14	Address Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
I/O0 to I/O7	Data I/O
V_{PP}	Power Supply for Program
V_{DD}	Power Supply (5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage *1	V_{DD}	−0.6 to 7.0	V
Supply voltage for programming *1	V_{PP}	−0.6 to 14	V
Input voltage *1	V_I	−1.0*2 to 7	V
Output voltage*1	V_O	−1.0*2 to 7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Temperature under bias	T_{bias}	−10 to 80	°C

*1 With respect to V_{SS}. *2 Pulse width : 50ns, DC : V_{IL} (Min) = −0.6V

■ELECTRICAL CHARACTERISTICS

Read Mode

●DC Electrical Characteristics

(V_{DD} = 5V ± 5%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD} + 1.0	V
Low level input voltage	V_{IL}		−1.0*1	—	0.8	V
Input leakage current	I_{LI}	V_I = 5.25V	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}$ = V_{IH}	—	—	1	mA
	I_{DDS1}	$\overline{CE}$ = V_{DD} ± 0.3V	—	1	20	μA
Operating supply current	I_{DDO1}	$\overline{CE}$ = V_{IL}, I_O = 0mA	—	—	30	mA
	I_{DDO2}	f = 5MHz, I_O = 0mA	—	—	30	
	I_{DDO3}	f = 1MHz, I_O = 0mA	—	—	8	
Programming supply current	I_{PP1}	V_{PP} = 5.5V	—	1	20	μA
Output leakage current	I_{LO}	V_O = 5.25V/0.4V	−2.0	—	2.0	μA
High level output voltage	V_{OH1}	I_{OH} = −400μA	2.4	—	—	V
	V_{OH2}	I_{OH} = −100μA	V_{DD} − 0.7	—	—	
Low level output voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V

*1 Pulse width : 50ns, DC : V_{IL} (Min) = −0.3V

●Terminal Capacitance*2

(f = 1.0MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I = 0V	—	4	6	pF
Output capacitance	C_O	V_O = 0V	—	8	12	pF

*2 This parameter is sampled and not 100% tested.

●AC Electrical Characteristics

(V_{DD} = 5V ± 5%, V_{SS} = 0V, V_{PP} = V_{DD}, Ta = 0 to 70°C)

Parameter	Symbol		Conditions	SPM27C256H$_{20}$		SPM27C256H$_{25}$		Unit
				Min	Max	Min	Max	
Address access time	t_{ACC}	*3	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	—	200	—	250	ns
Chip enable access time	t_{ACE}		$\overline{OE}$ = V_{IL}	—	200	—	250	ns
Output enable access time	t_{OE}		$\overline{CE}$ = V_{IL}	10	70	10	100	ns
Output floating	t_{DF}		$\overline{CE}$ = V_{IL}	0	50	0	60	ns
Output hold time	t_{OH}		$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	—	0	—	ns

*3 Input pulse level : 0.45V to 2.4V, Input rise and fall times ≦ 20ns, Output load : 1TTL + 100pF, Reference level for measuring timing : 0.8V and 2.0V

High Performance Programming Mode

●DC Electrical Characteristics ($V_{DD}=6\pm0.25V$, $V_{SS}=0V$, $V_{PP}=12.5\pm0.3V$, $Ta=25\pm5°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}	V
Low level input voltage	V_{IL}		−0.1	—	0.8	V
Input leakage current	I_{LI}	$V_I=6.25V/0.45V$	−2.0	—	2.0	μA
Operating supply current	I_{DDO2}		—	—	30	mA
Programming supply current	I_{PP2}	$\overline{CE}=V_{IL}$	—	—	40	mA
High level output voltage	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.1mA$	—	—	0.45	V

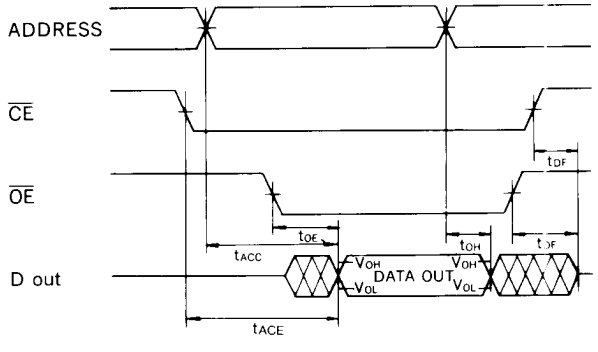
●AC Electrical Characteristics ($V_{DD}=6\pm0.25V$, $V_{SS}=0V$, $V_{PP}=12.5\pm0.3V$, $Ta=25\pm5°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address setup time	t_{AS}	Input pulse level: 0.45V to 2.4V Input rise and fall times: ≦20ns Reference level for measuring timing: 0.8V and 2V	2	—	—	μs
Chip enable setup time	t_{CES}		2	—	—	μs
Output enable setup time	t_{OES}		2	—	—	μs
Data setup time	t_{DS}		2	—	—	μs
Address hold time	t_{AH}		0	—	—	μs
Data hold time	t_{DH}		2	—	—	μs
Output floating*4	t_{DF}		—	—	130	ns
Output enable access time	t_{OE}		0	—	150	ns
V_{PP} setup time	t_{VPS}		2	—	—	μs
V_{DD} setup time	t_{VCS}		2	—	—	μs
Programming pulse width	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ overprogram pulse width*5	t_{OPW}		2.85	—	78.75	ms

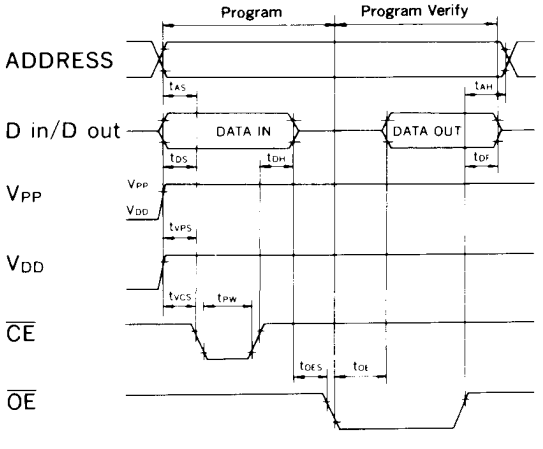
*4 t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.
*5 t_{OPW} is defined as mentioned in flow chart.

●Timing Chart

○Read Mode



○High Performance Programming Mode



■FUNCTIONS

●Truth Table

Mode \ Pin name	Address input A0 to A14	Data I/O I/O0 to I/O7	$\overline{CE}$	$\overline{OE}$	V_{DD}	V_{PP}
Read	Stable	Output data	L	L	V_{DD}	V_{DD}
Output disable	Stable	Hi—Z	L	H	V_{DD}	V_{DD}
Standby	X	Hi—Z	H	X	V_{DD}	V_{DD}
High performance program	Stable	Input data	L	H	V_{DD}	V_{PP}
Program verify	Stable	Output data	H	L	V_{DD}	V_{PP}
Optional verify	Stable	Output data	L	L	V_{DD}	V_{PP}
Program inhibit	X	Hi—Z	H	H	V_{DD}	V_{PP}

X : "H" or "L"

●Read

Data is able to be read by setting addresses during holding $\overline{CE}$ = "L" and $\overline{OE}$ = "L"

●Output Disable

Data I/O terminals are Hi-Z when $\overline{OE}$ = "H"

●Standby

When $\overline{CE}$ is "H" the SPM27C256H20/25 is in the standby mode. Then, Data I/O terminals are Hi-z, and all of address inputs are prohibited.

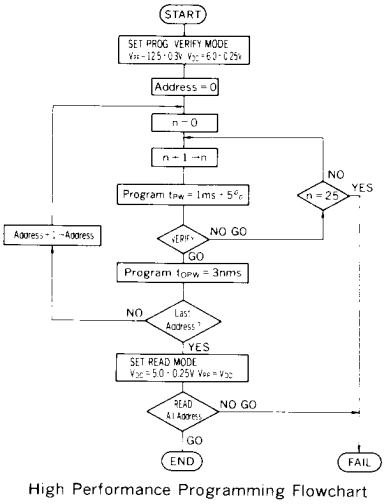
●High Performance Programming

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

●Erase

Erasure of SPM27C256H20/25 is performed by exposure to ultraviolet light of 2737 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm^2

■High Performance Program



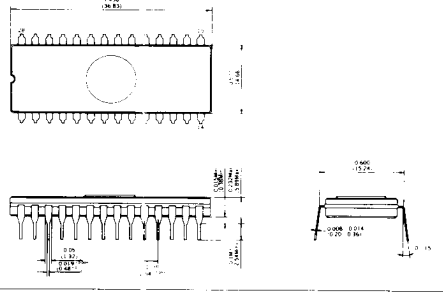
High Performance Programming Flowchart

*1 V_{DD} must be applied before V_{PP} and removed after V_{PP}.
*2 V_{PP} must not exceed 13V including overshoot.
*3 An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
*4 Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.

■PACKAGE DIMENSIONS

H28-9

28-pin CERDIP



unit : inch
(mm)

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