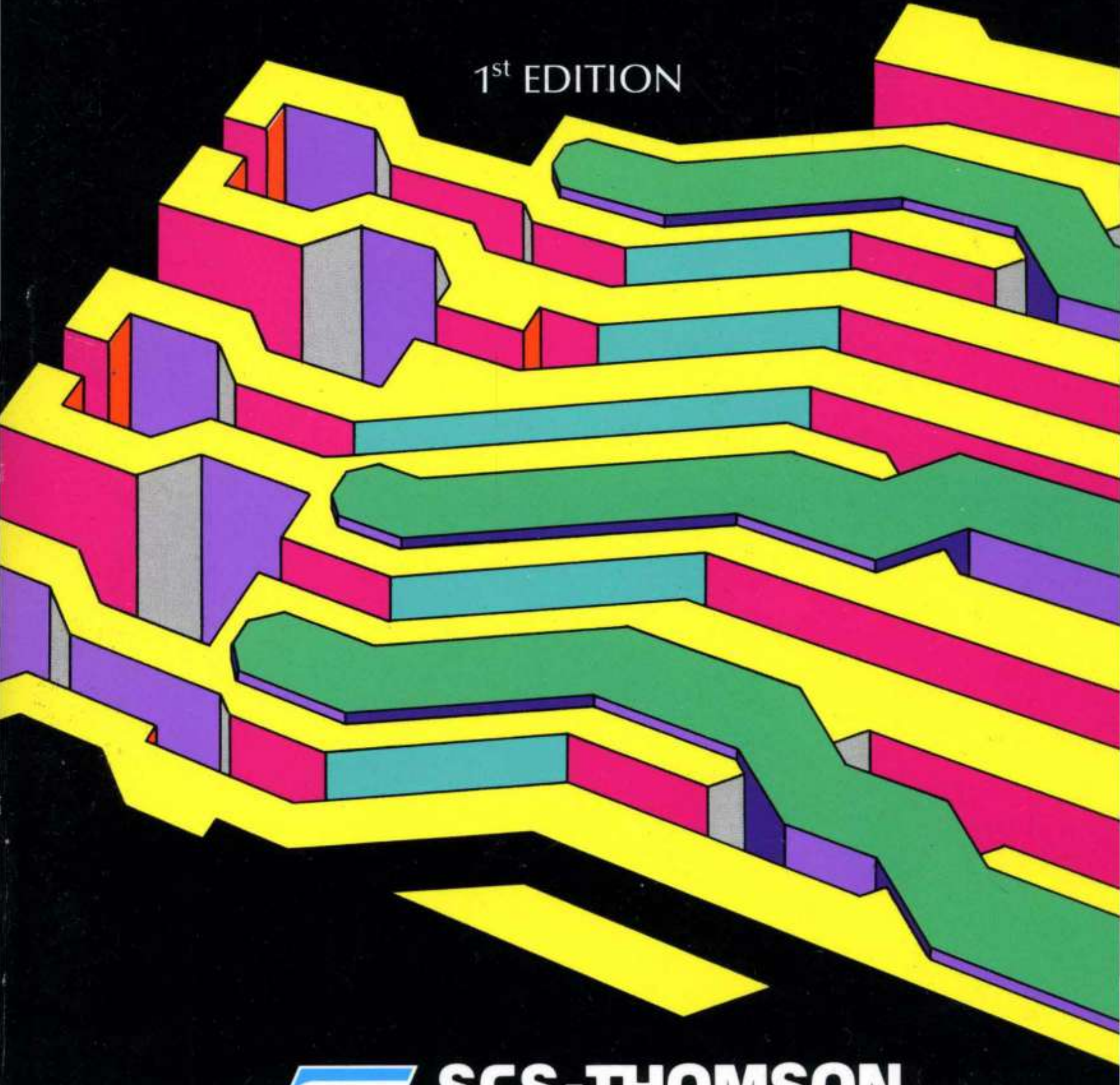
MEMORY PRODUCTS

DATABOOK

1st EDITION



SGS-THOMSON
MICROELECTRONICS

MEMORY PRODUCTS

DATABOOK

1st EDITION

JUNE 1988

USE IN LIFE SUPPORT MUST BE EXPRESSLY AUTHORIZED

SGS-THOMSON' PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEM WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF SGS-THOMSON Microelectronics. As used herein:

1. Life support devices or systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT GUIDE

The SGS-THOMSON Microelectronics Memories data book is a comprehensive collection of information on advanced, high density, high speed memory products for specific applications.

SGS-THOMSON offers 4 groups of memory products: EPROMs and OTP's, EEPROMs, ROMs and Static RAMs.

EPROMs (Electrically Programmable Read Only Memory) and OTP's (One Time Programmable Read Only Memory) are non volatile memory components for program storage.

SGS-THOMSON Microelectronics has one of the largest product range to meet your requirements:

- all densities from 16K to 1 Megabit.
- NMOS or CMOS technology.
- Jedec approved footprints for easy upgrades.
- UV EPROM in Cerdip package.
- One Time Programmable in windowless plastic package ideally suited for high volume production environment and surface mounting applications.
- very fast programming algorithm.

EEPROMS (Electrically Erasable Programmable Read Only Memories) embody the full range of EPROM functional advantages plus the added features of in-circuit erasability and programmability. SGS-THOMSON range comprehends serial access products, with densities ranging from 256 bit to 2K bit, including 2-wire bus compatible versions.

Static RAM products cover high speed memories, biport devices and Zeropower™ Timekeeper™ RAMS.

- High speed memories with a device density range of 4Kbits to 64Kbits and performance from 20ns to 55ns.
  Organizational flexibility (4K × 1, 16K × 1, 4K × 4, 64K × 1, 8K × 8) covers a vast range of applications, including large mainframes, high speed controllers, communications, graphics display and workstations.
- Biport devices consist of a family of FIFO (First-In-First-Out) buffers. These FIFO's provide an interface between digital information paths with widely varying speeds. Each information source can thus operate at its own intrinsic speed, while results are processed or distributed at speeds from 25ns to 200ns. The Biport family also includes a range of veritable Dual Port Rams enabling applications in systems with two or more processors, or with distributed processors, where separate computing units must exchange data at speeds approaching real time.
- The Zeropower and Timekeeper RAM family combines the operating simplicity of convention byte-wide SRAM's with the excellent data integrity of Zeropower technology. This integrity is achieved thanks to the use of advanced CMOS technology and long-life lithium cells. With densities from 2K × 8 to 8K × 8 and access/cycle times up to 120ns (150ns for 8K × 8), SGS-THOMSON Zeropower RAMs cover the full range of non-volatile needs for all microprocessor based systems. Thanks to the combined features of Zeropower technology with an on-chip real time clock, the 48T02 Timekeeper offers unparalleled non-volatile performance.

NMOS UV EPROM

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
ET2716Q	2K × 8	450ns	100mA	25mA	5V ± 5%	0 to +70°C	24
ET2716Q-1	2K × 8	350ns	100mA	25mA	5V ± 10%	0 to +70°C	24
M2716F1	2K × 8	450ns	100mA	25mA	5V ± 5%	0 to +70°C	24
M2716-1F1	2K × 8	350ns	100mA	25mA	5V ± 10%	0 to +70°C	24
M2716F6	2K × 8	450ns	100mA	25mA	5V ± 5%	−40 to +85°C	24
M2716-1F6	2K × 8	350ns	100mA	25mA	5V ± 10%	−40 to +85°C	24
M2732AF1	4K × 8	250ns	125mA	35mA	5V ± 5%	0 to +70°C	24
M2732A-2F1	4K × 8	200ns	125mA	35mA	5V ± 5%	0 to +70°C	24
M2732A-3F1	4K × 8	300ns	125mA	35mA	5V ± 5%	0 to +70°C	24
M2732A-4F1	4K × 8	450ns	125mA	35mA	5V ± 5%	0 to +70°C	24
M2732AF6	4K × 8	250ns	125mA	35mA	5V ± 5%	−40 to +85°C	24
M2732A-4F6	4K × 8	450ns	125mA	35mA	5V ± 5%	−40 to +85°C	24
M2764AF1	8K × 8	250ns	75mA	35mA	5V ± 5%	0 to +70°C	28
M2764A-1F1	8K × 8	180ns	75mA	35mA	5V ± 5%	0 to +70°C	28
M2764A-2F1	8K × 8	200ns	75mA	35mA	5V ± 5%	0 to +70°C	28
M2764A-3F1	8K × 8	300ns	75mA	35mA	5V ± 5%	0 to +70°C	28
M2764A-4F1	8K × 8	450ns	75mA	35mA	5V ± 5%	0 to +70°C	28
M2764A-18F1	8K × 8	180ns	75mA	35mA	5V ± 10%	0 to +70°C	28
M2764A-20F1	8K × 8	200ns	75mA	35mA	5V ± 10%	0 to +70°C	28
M2764A-25F1	8K × 8	250ns	75mA	35mA	5V ± 10%	0 to +70°C	28
M2764A-30F1	8K × 8	300ns	75mA	35mA	5V ± 10%	0 to +70°C	28
M2764A-45F1	8K × 8	450ns	75mA	35mA	5V ± 10%	0 to +70°C	28
M2764AF6	8K × 8	250ns	75mA	35mA	5V ± 5%	−40 to +85°C	28
M2764A-4F6	8K × 8	450ns	75mA	35mA	5V ± 5%	−40 to +85°C	28
M27128AF1	16K × 8	250ns	85mA	40mA	5V ± 5%	0 to +70°C	28
M27128A-1F1	16K × 8	150ns	85mA	40mA	5V ± 5%	0 to +70°C	28
M27128A-2F1	16K × 8	200ns	85mA	40mA	5V ± 5%	0 to +70°C	28
M27128A-3F1	16K × 8	300ns	85mA	40mA	5V ± 5%	0 to +70°C	28
M27128A-4F1	16K × 8	450ns	85mA	40mA	5V ± 5%	0 to +70°C	28
M27128A-20F1	16K × 8	200ns	85mA	40mA	5V ± 10%	0 to +70°C	28
M27128A-25F1	16K × 8	250ns	85mA	40mA	5V ± 10%	0 to +70°C	28
M27128A-30F1	16K × 8	300ns	85mA	40mA	5V ± 10%	0 to +70°C	28
M27128A-45F1	16K × 8	450ns	85mA	40mA	5V ± 10%	0 to +70°C	28
M27128AF6	16K × 8	250ns	85mA	40mA	5V ± 5%	−40 to +85°C	28
M27128A-4F6	16K × 8	450ns	85mA	40mA	5V ± 5%	−40 to +85°C	28
M27256F1	32K × 8	250ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-1F1	32K × 8	170ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-2F1	32K × 8	200ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-3F1	32K × 8	300ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-4F1	32K × 8	450ns	100mA	40mA	5V ± 5%	0 to +70°C	28
M27256-20F1	32K × 8	200ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-25F1	32K × 8	250ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-30F1	32K × 8	300ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256-45F1	32K × 8	450ns	100mA	40mA	5V ± 10%	0 to +70°C	28
M27256F6	32K × 8	250ns	100mA	40mA	5V ± 5%	−40 to +85°C	28
M27256-4F6	32K × 8	450ns	100mA	40mA	5V ± 5%	−40 to +85°C	28
M27512F1	64K × 8	250ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-2F1	64K × 8	200ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-3F1	64K × 8	300ns	125mA	40mA	5V ± 5%	0 to +70°C	28
M27512-25F1	64K × 8	250ns	125mA	40mA	5V ± 10%	0 to +70°C	28
M27512-30F1	64K × 8	300ns	125mA	40mA	5V ± 10%	0 to +70°C	28
M27512F6	64K × 8	250ns	125mA	40mA	5V ± 5%	−40 to +85°C	28

CMOS UV EPROM

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
ETC2716Q	2K × 8	450ns	10mA	1mA	5V ± 5%	0 to +70°C	24
ETC2716Q-1	2K × 8	350ns	10mA	1mA	5V ± 5%	0 to +70°C	24
ETC2716Q-V	2K × 8	450ns	10mA	1mA	5V ± 5%	−40 to +85°C	24
ETC2732Q	4K × 8	450ns	10mA	1mA	5V ± 5%	0 to +70°C	24
ETC2732Q-3	4K × 8	350ns	10mA	1mA	5V ± 5%	0 to +70°C	24
ETC2732Q-45-V	4K × 8	450ns	10mA	1mA	5V ± 5%	−40 to +85°C	24
TS27C64A-15XCQ	8K × 8	150ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C64A-20XCQ	8K × 8	200ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C64A-25XCQ	8K × 8	250ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C64A-30XCQ	8K × 8	300ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C64A-15CQ	8K × 8	150ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C64A-20CQ	8K × 8	200ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C64A-25CQ	8K × 8	250ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C64A-30CQ	8K × 8	300ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C64A-15VQ	8K × 8	150ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C64A-20VQ	8K × 8	200ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C64A-25VQ	8K × 8	250ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C64A-30VQ	8K × 8	300ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-15XCQ	32K × 8	150ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C256-17XCQ	32K × 8	170ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C256-20XCQ	32K × 8	200ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C256-25XCQ	32K × 8	250ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C256-30XCQ	32K × 8	300ns	30mA	1mA	5V ± 5%	0 to +70°C	28
TS27C256-17CQ	32K × 8	170ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C256-20CQ	32K × 8	200ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C256-25CQ	32K × 8	250ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C256-30CQ	32K × 8	300ns	30mA	1mA	5V ± 10%	0 to +70°C	28
TS27C256-15VQ	32K × 8	150ns	30mA	1mA	5V ± 5%	−40 to +85°C	28
TS27C256-17CQ	32K × 8	170ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-20VQ	32K × 8	200ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-25VQ	32K × 8	250ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
TS27C256-30VQ	32K × 8	300ns	30mA	1mA	5V ± 10%	−40 to +85°C	28
M27C1024-12XF1	64K × 16	120ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-15XF1	64K × 16	150ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-20XF1	64K × 16	200ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-25XF1	64K × 16	250ns	50mA	1mA	5V ± 5%	0 to +70°C	40
M27C1024-12F1	64K × 16	120ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-15F1	64K × 16	150ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-20F1	64K × 16	200ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-25F1	64K × 16	250ns	50mA	1mA	5V ± 10%	0 to +70°C	40
M27C1024-15XF6	64K × 16	150ns	50mA	1mA	5V ± 5%	−40 to +85°C	40
M27C1024-20XF6	64K × 16	200ns	50mA	1mA	5V ± 5%	−40 to +85°C	40
M27C1024-25XF6	64K × 16	250ns	50mA	1mA	5V ± 5%	−40 to +85°C	40

NMOS OTP ROM

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
ST2764A-18XCP	8K × 8	180ns	75mA	35mA	5V ± 5%	0 to +70°C	28
ST2764A-20XCP	8K × 8	200ns	75mA	35mA	5V ± 5%	0 to +70°C	28
ST2764A-18CP	8K × 8	180ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-20CP	8K × 8	200ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-25CP	8K × 8	250ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST2764A-30CP	8K × 8	300ns	75mA	35mA	5V ± 10%	0 to +70°C	28
ST27128A-15XCP	16K × 8	150ns	85mA	40mA	5V ± 5%	0 to +70°C	28
ST27128A-20XCP	16K × 8	200ns	85mA	40mA	5V ± 5%	0 to +70°C	28
ST27128A-20CP	16K × 8	200ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27128A-25CP	16K × 8	250ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27128A-30CP	16K × 8	300ns	85mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-17XCP	32K × 8	170ns	100mA	40mA	5V ± 5%	0 to +70°C	28
ST27256-20XCP	32K × 8	200ns	100mA	40mA	5V ± 5%	0 to +70°C	28
ST27256-20CP	32K × 8	200ns	100mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-25CP	32K × 8	250ns	100mA	40mA	5V ± 10%	0 to +70°C	28
ST27256-30CP	32K × 8	300ns	100mA	40mA	5V ± 10%	0 to +70°C	28

CMOS OTP ROM

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
TS27C64A-15CFN	8K × 8	150ns	30mA	1mA	5V ± 10%	0 to × 70°C	32
TS27C64A-20CFN	8K × 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-25CFN	8K × 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-30CFN	8K × 8	300ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
TS27C64A-15VFN	8K × 8	150ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
TS27C64A-20VFN	8K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
TS27C64A-25VFN	8K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
TS27C64A-30VFN	8K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
TS27C64A-15TFN	8K × 8	150ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
TS27C64A-20TFN	8K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
TS27C64A-25TFN	8K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
TS27C64A-30TFN	8K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
TS27C64A-15CP	8K × 8	150ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-20CP	8K × 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-25CP	8K × 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-30CP	8K × 8	300ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
TS27C64A-15VP	8K × 8	150ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
TS27C64A-20VP	8K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
TS27C64A-25VP	8K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
TS27C64A-30VP	8K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
TS27C64A-15TP	8K × 8	150ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
TS27C64A-20TP	8K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
TS27C64A-25TP	8K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
TS27C64A-30TP	8K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
ST27C256-17CFN	32K × 8	170ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-20CFN	32K × 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-25CFN	32K × 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-30CFN	32K × 8	300ns	30mA	1mA	5V ± 10%	0 to + 70°C	32
ST27C256-17VFN	32K × 8	170ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
ST27C256-20VFN	32K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
ST27C256-25VFN	32K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
ST27C256-30VFN	32K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	32
ST27C256-17TFN	32K × 8	170ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
ST27C256-20TFN	32K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
ST27C256-25TFN	32K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
ST27C256-30TFN	32K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	32
ST27C256-17CP	32K × 8	170ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-20CP	32K × 8	200ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-25CP	32K × 8	250ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-30CP	32K × 8	300ns	30mA	1mA	5V ± 10%	0 to + 70°C	28
ST27C256-17VP	32K × 8	170ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
ST27C256-20VP	32K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
ST27C256-25VP	32K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
ST27C256-30VP	32K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 85°C	28
ST27C256-17TP	32K × 8	170ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
ST27C256-20TP	32K × 8	200ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
ST27C256-25TP	32K × 8	250ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28
ST27C256-30TP	32K × 8	300ns	30mA	1mA	5V ± 10%	– 40 to + 105°C	28

NMOS EEPROM

Part Number	Orga.	Frequency	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
M8571B1	1K-bit	125KHz	20mA	—	5V ± 10%	0 to +70°C	8
M8571B6	1K-bit	125KHz	20mA	—	5V ± 10%	– 40 to +85°C	8
M9306B1	256-bit	250KHz	6mA	3mA	5V ± 10%	0 to +70°C	8
M9306B6	256-bit	250KHz	6mA	3mA	5V ± 10%	– 40 to +85°C	8
M9306M1	256-bit	250KHz	6mA	3mA	5V ± 10%	0 to +70°C	8
M9306M6	256-bit	250KHz	6mA	3mA	5V ± 10%	– 40 to +85°C	8
M9346B1	1-Kbit	250KHz	6mA	3mA	5V ± 10%	0 to +70°C	8
M9346B6	1-Kbit	250KHz	6mA	3mA	5V ± 10%	– 40 to +85°C	8
M9346M1	1-Kbit	250KHz	6mA	3mA	5V ± 10%	0 to +70°C	14
M9346M6	1-Kbit	250KHz	6mA	3mA	5V ± 10%	– 40 to +85°C	14

CMOS EEPROM

Part Number	Orga.	Frequency	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
ST24C02CP	2-KBIT	100KHz	3mA	0.1mA	5V ± 10%	0 to +70°C	8
ST24C02VP	2-KBIT	100KHz	3mA	0.1mA	5V ± 10%	– 40 to +85°C	8
TS59C11CP	1-KBIT	250KHz	3mA	0.1mA	5V ± 10%	0 to +70°C	8
TS59C11VP	1-KBIT	250KHz	3mA	0.1mA	5V ± 10%	– 40 to +85°C	8
TS93C46CP	1-KBIT	250KHz	3mA	0.1mA	5V ± 10%	0 to +70°C	8
TS93C46VP	1-KBIT	250KHz	3mA	0.1mA	5V ± 10%	– 40 to +85°C	8
ST93C56	2-KBIT	1MHz	3mA	0.1mA	5V ± 10%	0 to +70°C	8

NMOS ROM

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
M2316H	2Kx8	300ns	70mA	—	5V ± 10%	0 to +70°C	24
M2332/M2333	4Kx8	250ns	70mA	—	5V ± 10%	0 to +70°C	24
M2364	8Kx8	250ns	80mA	—	5V ± 10%	0 to +70°C	24
M2365	8Kx8	250ns	70mA	—	5V ± 10%	0 to +70°C	28

ZEROPOWER

Part Number	Orga.	Access Time	I_{CC} Max		V_{CC}		Temp. Range	Pin Count
			Act	St.by				
BATTERY BACK-UP								
MK48C02AN15	2K×8	150ns	80mA	3mA	5V	+10% −5%	0 to +70°C	24
MK48C02AN20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AN25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AK15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AK20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48C02AK25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
TIMEKEEPER								
MK48T02B12	2K×8	120ns	80mA	3mA	5V	+10% −5%	0 to +70°C	24
MK48T02B15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T02B20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T02B25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU12	2K×8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T02BU25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B12	2K×8	120ns	80mA	3mA	5V	+10% −10%	0 to +70°C	24
MK48T12B15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T12B25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU12	2K×8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48T12BU25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
ZEROPOWER								
MK48Z02B12	2K×8	120ns	80mA	3mA	5V	+10% −5%	0 to +70°C	24
MK48Z02B15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02B20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02B25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU12	2K×8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z02BU25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B12	2K×8	120ns	80mA	3mA	5V	+10% −10%	0 to +70°C	24
MK48Z12B15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12B25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU12	2K×8	120ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU15	2K×8	150ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU20	2K×8	200ns	80mA	3mA	5V		0 to +70°C	24
MK48Z12BU25	2K×8	250ns	80mA	3mA	5V		0 to +70°C	24
MKI48Z02B12	2K×8	120ns	80mA	3mA	5V	+10% −5%	−40 to +85°C	24
MKI48Z02B15	2K×8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02B20	2K×8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02B25	2K×8	250ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU12	2K×8	120ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU15	2K×8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU20	2K×8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z02BU25	2K×8	250ns	80mA	3mA	5V		−40 to +85°C	24

Note: 1. Letter "U" inserted in sales type indicates "Underwriters' Laboratories" branding.

ZEROPOWER

Part Number	Orga.	Access Time	I_{CC} Max		V_{CC}		Temp. Range	Pin Count
			Act	St.by				
MKI48Z12B12	2K × 8	120ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B15	2K × 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B20	2K × 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12B25	2K × 8	250ns	80mA	3mA	5V	+10%	−40 to +85°C	24
MKI48Z12BU12	2K × 8	120ns	80mA	3mA	5V	−10%	−40 to +85°C	24
MKI48Z12BU15	2K × 8	150ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12BU20	2K × 8	200ns	80mA	3mA	5V		−40 to +85°C	24
MKI48Z12BU25	2K × 8	250ns	80mA	3mA	5V		−40 to +85°C	24
MK48Z08B15	8K × 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08B20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08B25	8K × 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z08BU15	8K × 8	150ns	50mA	3mA	5V	−5%	0 to +70°C	28
MK48Z08BU20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z08BU25	8K × 8	250ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B15	8K × 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18B25	8K × 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z18BU15	8K × 8	150ns	50mA	3mA	5V	−10%	0 to +70°C	28
MK48Z18BU20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z18BU25	8K × 8	250ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09B15	8K × 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09B20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09B25	8K × 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z09BU15	8K × 8	150ns	50mA	3mA	5V	−5%	0 to +70°C	28
MK48Z09BU20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z09BU25	8K × 8	250ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B15	8K × 8	150ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19B25	8K × 8	250ns	50mA	3mA	5V	+10%	0 to +70°C	28
MK48Z19BU15	8K × 8	150ns	50mA	3mA	5V	−10%	0 to +70°C	28
MK48Z19BU20	8K × 8	200ns	50mA	3mA	5V		0 to +70°C	28
MK48Z19BU25	8K × 8	250ns	50mA	3mA	5V		0 to +70°C	28

Note: 1. Letter "U" inserted in sales type indicates "Underwriters' Laboratories" branding.

FAST STATIC RAM

Part Number	Orga.	Access Time	I_{CC} Max		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
MK41H66N20	16K × 1	20ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H66N25	16K × 1	25ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H66N35	16K × 1	35ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H67N20	16K × 1	20ns	120mA	10mA	5V ± 10%	0 to +70°C	20
MK41H67N25	16K × 1	25ns	120mA	10mA	5V ± 10%	0 to +70°C	20
MK41H67N35	16K × 1	35ns	120mA	10mA	5V ± 10%	0 to +70°C	20
MK41H68N20	4K × 4	20ns	120mA	8mA	5V ± 10%	0 to +70°C	20
MK41H68N25	4K × 4	25ns	120mA	8mA	5V ± 10%	0 to +70°C	20
MK41H68N35	4K × 4	35ns	120mA	8mA	5V ± 10%	0 to +70°C	20
MK41H69N20	4K × 4	20ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H69N25	4K × 4	25ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H69N35	4K × 4	35ns	120mA	—	5V ± 10%	0 to +70°C	20
MK41H79N20	4K × 4	20ns	120mA	16mA	5V ± 10%	0 to +70°C	22
MK41H79N25	4K × 4	25ns	120mA	16mA	5V ± 10%	0 to +70°C	22
MK41H79N35	4K × 4	35ns	120mA	16mA	5V ± 10%	0 to +70°C	22
TAGRAM							
MK41H80N20	4K × 4	20ns	120mA	—	5V ± 10%	0 to +70°C	22
MK41H80N25	4K × 4	25ns	120mA	—	5V ± 10%	0 to +70°C	22
MK41H80N35	4K × 4	35ns	120mA	—	5V ± 10%	0 to +70°C	22

Note: 1. Letter "U" inserted in sales type indicates "Underwiters' Laboratories" branding.

SELECTION GUIDE

BIPORT (DUAL PORT)

Part Number	Orga.	Access Time	I_{CC} MAX		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
MK4511N12	512 × 9	120ns	50mA	5mA	5V ± 10%	0 to +70°C	28
MK4511N15	512 × 9	150ns	50mA	5mA	5V ± 10%	0 to +70°C	28
MK4511N20	512 × 9	200ns	50mA	5mA	5V ± 10%	0 to +70°C	28

FIFO

Part Number	Orga.	Access Time	I_{CC} Max		V_{CC}	Temp. Range	Pin Count
			Act	St.by			
MK4501K10	512 × 9	100ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501K12	512 × 9	120ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501K15	512 × 9	150ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501K20	512 × 9	200ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501K65	512 × 9	65ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501K80	512 × 9	80ns	80mA	8mA	5V ± 10%	0 to +70°C	32
MK4501N10	512 × 9	100ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4501N12	512 × 9	120ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4501N15	512 × 9	150ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4501N20	512 × 9	200ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4501N65	512 × 9	65ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4501N80	512 × 9	80ns	80mA	8mA	5V ± 10%	0 to +70°C	28
MK4503N10	2048 × 9	100ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4503N12	2048 × 9	120ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4503N15	2048 × 9	150ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4503N20	2048 × 9	200ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4503N65	2048 × 9	65ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4503N80	2048 × 9	80ns	120mA	12mA	5V ± 10%	0 to +70°C	28
MK4505MN25	1024 × 5	15ns	100mA	—	5V ± 10%	0 to +70°C	24
MK4505MN33	1024 × 5	20ns	100mA	—	5V ± 10%	0 to +70°C	24
MK4505MN50	1024 × 5	25ns	100mA	—	5V ± 10%	0 to +70°C	24
MK4505SN25	1024 × 5	15ns	100mA	—	5V ± 10%	0 to +70°C	20
MK4505SN33	1024 × 5	20ns	100mA	—	5V ± 10%	0 to +70°C	20
MK4505SN50	1024 × 5	25ns	100mA	—	5V ± 10%	0 to +70°C	20

Note: 1. Letter "U" inserted in sales type indicates "Underwriters' Laboratories" branding.

UV EPROM

PRODUCT DESCRIPTION	SGS-THOMSON	AMD	FUJITSU	HITACHI	INTEL	MICROCHIP TECHNOL. (GI)	MITSUBISHI	NSC	NEC	OKI	SIGNETICS	TI	TOSHIBA
2K×8 NMOS	ET2716Q M2716F	AM2716										TMS2516	
2K×8 CMOS	ETC2716Q							NMC2716BQ					
4K×8 NMOS	M2732A	AM2732			2732A							TMS2732A	
4K×8 CMOS	ETC2732Q							NMC27C32BQ					
8K×8 NMOS	M2764AF	AM2764	MBM2764		2764A							TMS2764	TMM2764AD
8K×8 CMOS	TS27C64AQ		MBM27C64	HN27C64G	27C64	27C64		NMC27C64Q			27C64A		
16K×8 NMOS	M27128AF	AM27128A	MBM27128	HN27128AG	27128A				μPD27128D			TMS27128	TMM27128AD
16K×8 CMOS	–				27C128	27C128		NMC27C128Q				TMS27C128	
32K×8 NMOS	M27256F	AM27256	MBM27256	HN27256G	27256	27256	M5M27256K		μPD27256D	MSM27256		TMS27256	TMM27256AD
32K×8 CMOS	TS27C256Q	AM27C256	MBM27C256	HN27C256G	27C256	27C256	M5M27C256K	NMC27C256Q	μPD27C256		27C256FA	TMS27C256	
64K×8 NMOS	M27512F	AM27512	MBM27512	HN27512G	27512F		M5M27512K						TMM27512D
64K×8 CMOS		AM27C512				27C512	M5M27C512AK	NMC27C512Q	μPD27C512D			TMS27C512	
128K×8 NMOS					27010					MSM271000			
128K×8 CMOS	ST27C1001			HN27C101G			M5M27C101K	NMC27C1023Q	μPD27C1001D				TC571001D
64K16 NMOS					27210					MSM271024			
64K16 CMOS	M27C1024	AM27C1024	MBM27C1024	HN27C1024			M5M27C102K	NMC27C1024	μPD27C1024D			TMS27C1024	TC57C1024D

OTP ROM

PRODUCT DESCRIPTION	SGS-THOMSON	HITACHI	INTEL	MICROCHIP TECHNOL. (GI)	MITSUBISHI	NSC	NEC	OKI	SIGNETICS	TI	TOSHIBA
8K × 8 NMOS	ST2764AP		P2764A		M5M2764P		μPD2764C	MSM2764AZB		TMS27P64	TMM2764AP
8K × 8 CMOS	TS27C64AP/FN		P27C64	P27C64		NMC27C64N	μPD27C64C		27C64A-N		
16K × 8 NMOS	ST27128AP	HN27128AP	P27128A				μPD27128C	MSM27128AZB		TMS27P128	TMM27128AP
32K × 8 NMOS	ST27256P	HN27256P	P27256	P27256	M5M27256P			MSM27256AZB		TMS27P256	TMM27256AP
32K × 8 CMOS	ST27C256P/FN		P27C256	P27C256	M5M27C256		μPD27C256AC		27C256-N	TMS27PC256	TC54256AP

EEPROM

PRODUCT DESCRIPTION	SGS-THOMSON	CATALYST	GENERAL INSTRUM.	HYUNDAI	ICT	NATIONAL	OKI	SIEMENS	SIERRA	VALVO (PHILIPS)	XICOR
SERIAL NMOS 256 BIT	M9306					NMC9306					
1024 BIT	M9346					NMC9346					
1024 BIT 2-WIRE BUS	M8571		PCD8572					SDA2516		PCF8572	
SERIAL CMOS 1024 BIT	TS59C11	CAT59C11	ER5911 (NMOS)				MSM16911				
1024 BIT	TS93C46	CAT93C46		HY93C46	ICT93C46	NMC93CS46 NMC93CS06	MSM16811		SC22011		
2048 BIT 2-WIRE BUS	ST24C02		PCD8582					SDA2526		PCF8582	X24C02 X2402 (NMOS)
2048 BIT $V_{CC}=3V$	ST93C56					NMC93CS56					

VFSRAM

PRODUCT DESCRIPTION	SGS-THOMSON	CYPRESS	MATRA	INMOS	IDT	MOTOROLA	NEC	FUJITSU
(16KX1)	MK41H67	CY7C167	HM65767	IMS1403	IDT6167A	MCM6167	μPD4311	MB81C67
(4KX4)	MK41H68	CY7C168	HM65768	IMS1423	IDT6168A	MCM6168	μPD4314	MB81C68
(64KX1)	MK41H87	CY7C187	HM65787	IMS1600	IDT7187	MCM6187	μPD4361	MB81C71
(8KX8)	MK48H64	CYC185	HM65641	IMS1630	IDT7164	MCM6164	μPD4364	MB81C78

FIFO

PRODUCT DESCRIPTION	SGS-THOMSON	IDT	CYPRESS	DALLAS	AMD/MMI	VTI
(512 × 9)	MK4501	IDT7201	CY7C412	DS2009	67C201	—
(2KX9)	MK4503	IDT7202/3	CY7C424/9	DS2010/1	67C202/3	VT2F9

ZEROPOWER

PRODUCT DESCRIPTION	SGS-THOMSON	DALLAS	GREENWICH
(2KX8)	MK48Z02	DS1210	NCR2
(8KX8)	MK48Z08	DS1225	NVR8

PROCESSES CHARACTERISTICS

NMOS EPROM

Process Name	Channel Length	Max. Speed	V_{PP} (external)	Main Products
E1	4 µm	350 ns	25 V	M2716
E3	1.5 µm	200 ns	21 V	M2732A
E3	1.5 µm	150 ns	12.5 V	M2764A M27128A M27256 M27512

CMOS EPROM

P2	5 µm	350 ns	25 V	ETC2716 ETC2732
3E	1.4 µm	150 ns	12.5 V	TS27C64A TS27C256
E4	1.0 µm	120 ns	12.5 V	M27C1024

NMOS EEPROM

F1	3.5 µm	250 KHz	5V	M8571 M9306 M9346

CMOS EEPROM

2E2	2.0 µm	250 KHz	5V	TS59C11 TS93C46 ST24C02
F3	1.5 µm	1 MHz	5V	ST93C56

STATIC RAMS

Technology	Channel Length	Max. Speed	Metal Levels/ Memory Cell	Main products
CMOS	2.0 µm	65 ns	1/8T	FIFO MK4501 MK4503
CMOS	2.0 µm	20 ns	1/8T	DUAL PORT MK4511
CMOS	2.0 µm	120 ns	1/6T	ZEROPOWER/ TIMEKEEPER MK48Z02 MK48T02
CMOS	1.2 µm	20 ns	2/6T	VERY FAST MK41H67 MK41H68 MK41H80 MK48H64
CMOS	1.2 µm	150 ns	2/6T	ZEROPOWER MK48Z08
CMOS	1.2 µm	25 ns	2/8T	FIFO MK4505

EPROM DEVICES

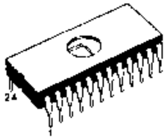
NMOS UV EPROM

SGS-THOMSON
MICROELECTRONICS

ET2716
M2716

16K (2K×8) NMOS UV ERASABLE PROM

- 2048 × 8 ORGANIZATION
- 525 MW MAX ACTIVE POWER, 132 MW MAX STANDBY POWER
- LOW POWER DURING PROGRAMMING
- ACCESS TIME M/ET2716-1, 350ns; M/ET2716, 450ns
- SINGLE 5V POWER SUPPLY
- STATIC-NO CLOCKS REQUIRED
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- EXTENDED TEMPERATURE RANGE (F6)



Q/F
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M/ET2716 is high speed 16K UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn around and pattern experimentation are important requirements.

The M/ET2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

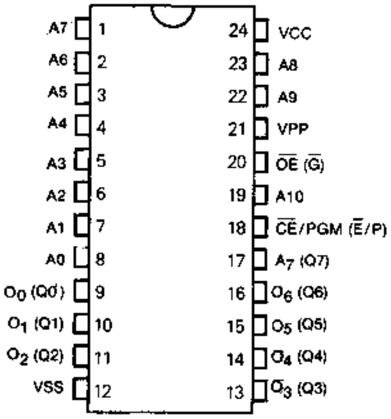
This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology X-MOS.

PIN NAMES

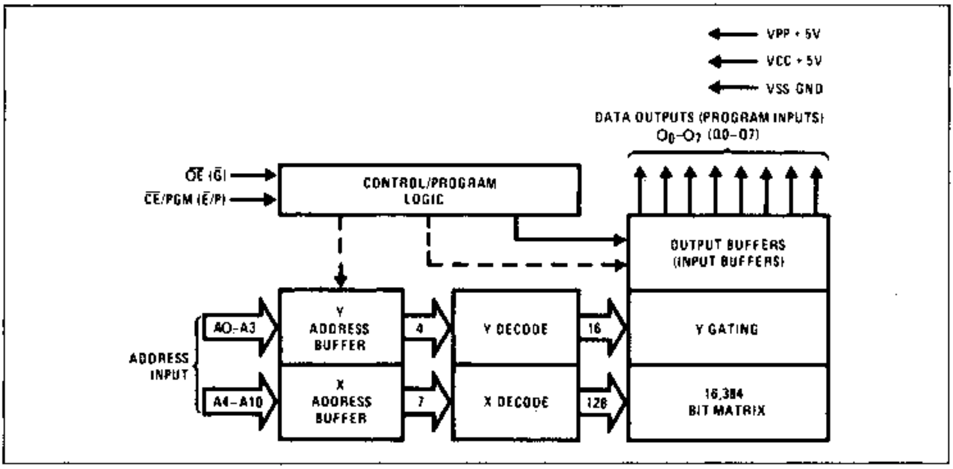
A0—A10	ADDRESS INPUTS
O_0—O_7 (Q0—Q7)	DATA OUTPUTS
$\overline{CE}$/PGM ($\overline{E}$/P)	CHIP ENABLE/PROGRAM
$\overline{OE}$ (G)	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	POWER (5V)
V_{SS}	GROUND

Note: Symbols in parentheses are proposed JEDEC standard

PIN CONNECTIONS



BLOCK DIAGRAM


VPP + 5V
VCC + 5V
VSS GND
DATA OUTPUTS (PROGRAM INPUTS)
O_0–O_7 (Q0–Q7)
$\overline{OE}$ ($\overline{G}$)
$\overline{CE}$/PGM ($\overline{E}$/P)
CONTROL/PROGRAM LOGIC
OUTPUT BUFFERS (INPUT BUFFERS)
ADDRESS INPUT
AO-A3
Y ADDRESS BUFFER
4
Y DECODE
16
Y GATING
A4–A10
X ADDRESS BUFFER
7
X DECODE
128
16,384 BIT MATRIX

PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	5	5	D_{OUT}
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

* Symbols in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias (Extended Temperature Range)	– 10 to + 80 (– 50 to + 95)	°C °C
T_{stg}	Storage Temperature	– 65 to + 125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to – 0.3	V
V_{in}	All Input or Output Voltages with Respect to V_{SS}	6V to – 0.3	V
P_D	Power Dissipation	1.5	W
	Lead Temperature (Soldering 10 seconds)	+ 300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS[1] $T_A = 0°C$ to $+ 70°C$[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current	$V_{IN} = 5.25V$ ORVIN $= V_{IL}$	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$, $\overline{CE}$/PGM $= 5V$	—	—	10	μA
I_{PP1}	V_{PP} Supply Current	$V_{PP} = 5.25V$	—	—	5	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{CE}$/PGM $= V_{IH}$, $\overline{OE} = V_{IL}$	—	10	25	mA
I_{CC2}	V_{CC} Supply Current (Active)	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$	—	57	100	mA
V_{IL}	Input Low Voltage		− 0.1	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{CC} + 1$	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V

AC CHARACTERISTICS $T_A = 0°C$ to $+70°C$ C[6], $V_{CC} = 5V \pm 5\%$ for M/ET2716, $V_{CC} = 5V \pm 10\%$ for M/ET2716-1 $V_{PP} = V_{CC}$[3], $V_{SS} = 0V$, (Unless otherwise specified).

Symbol		Parameter	Test Conditions	M/ET2716-1		M/ET2716		Unit
Standard	Jedec			Min.	Max.	Min.	Max.	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$	—	350	—	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM $= V_{IL}$	—	120	—	120	ns
t_{DF} (Note 5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}$/PGM $= V_{IL}$	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$	0	—	0	—	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE} = V_{IL}$	0	100	0	100	ns

CAPACITANCE[4] $T_A = 25°C$, $f = 1$ MHz

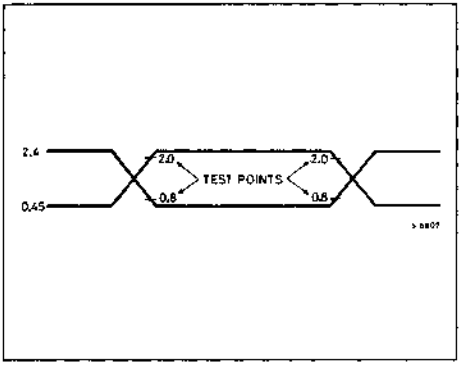
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. VCC must be applied at the same time or before VPP and removed after or at the same time as V_{PP}
2. Typical conditions are for operation at: $T_A = 25°C$, VCC = 5V, VPP = VCC, and VSS = 0V
3. VPP may be connected to VCC except during program.
4. Capacitance is guaranteed by periodic testing. $T_A = 25°C$, $f = 1$ MHz.
5. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ wich ever occurs first. This parameter as only sampled and not 100% tested.
6. $T_A = -40°C$ To $+85°C$ for the F6 version (extended To range).

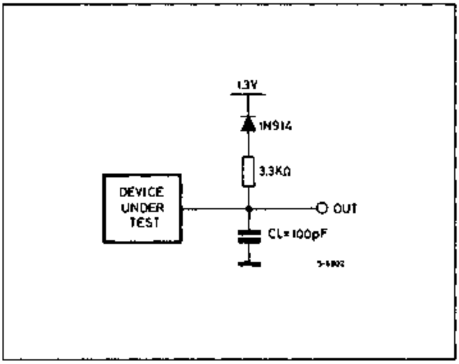
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level Inputs, Outputs	0.8V and 2V

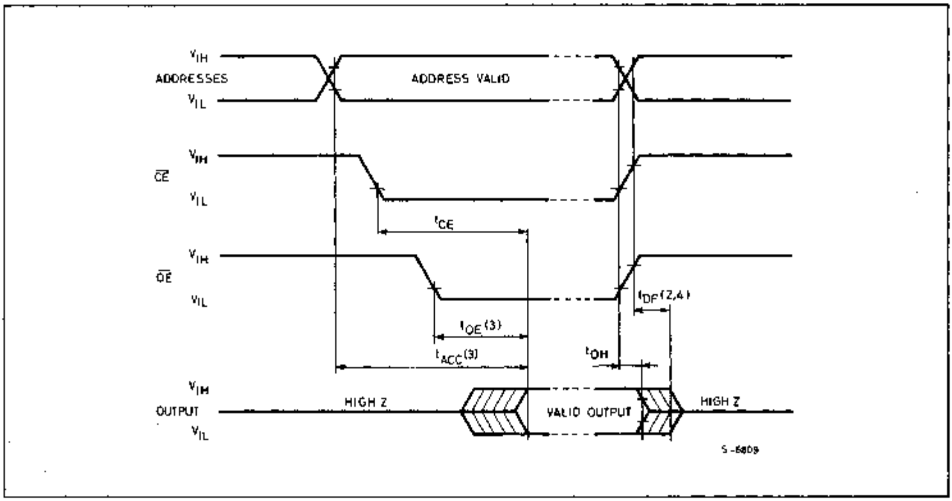
AC TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
5-6808

AC WAVEFORMS


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE
VIH
OE
VIL
tDF(2,4)
tOE(3)
tACC(3)
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
5-6809

Notes:

1. Typical values are for T_{amb} = 25°C and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The M/ET2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

TABLE I. OPERATING MODES ($V_{CC} = V_{PP} = 5V$)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	D_{OUT}
DESELECT	Don't Care	V_{IH}	Hi-Z
STANDBY	V_{IH}	Don't Care	Hi-Z

READ MODE

The M/ET2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PCM = VIL and that addresses A0 – A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Swithching Time Waveforms) depending on wich is limiting.

DESELECT MODE

The M/ET2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the adresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more M/ET2716's for memory expansion.

STANDBY MODE (Power Down)

The M/ET2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintened at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The M/ET2716 is shipped from SGS-THOMSON completely erased. All bits will be at "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The M/ET2716 is programmed by introducing "0" s into the desidered locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels including the program pulse on chip enable are TTL compatible. The programming sequence is:

With V_{PP} = 25V, VCC = 5V, $\overline{OE}$ = V_{IH} and $\overline{CE}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins. (V_{IL} = "0" and V_{IL} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) must not be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. M/ET2716's may be programmed in parallel with the same data in this mode.

PROGRAM VERIFY MODE

The programming of the M/ET2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with V_{PP} = 25V (or 5V) in either case. V_{PP} must be at 5V for all operating modes and can be maintained at 25V for all programming modes.

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several M/ET2716's simultaneously with different data for each one by controlling wich ones receive the program pulse. All similar inputs of the M/ET2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = V_{IH} will put its outputs in the Hi-Z state.

TABLE II. PROGRAMMING MODES ($V_{CC} = 5V$)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	V_{PP} 21	OUTPUTS 9—11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25(5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

ERASING

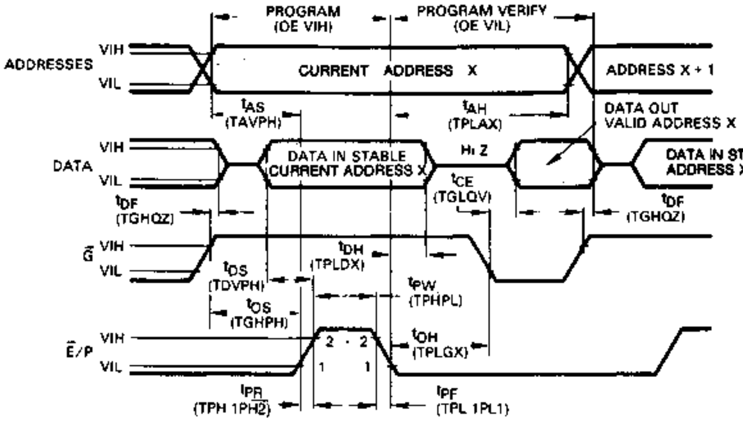
The M/ET2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the M/ET2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time.

An ultraviolet source of 2537 A yelding a total integrated dosage of 15 watt-seconds/cm² power rating is used. The M/ET2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

TIMING DIAGRAM

PROGRAM MODE



PROGRAM (OE VIH)
PROGRAM VERIFY (OE VIL)
ADDRESSES
VIH
VIL
CURRENT ADDRESS X
ADDRESS X + 1
t_{AS} (TAVPH)
t_{AH} (TPLAX)
DATA OUT VALID ADDRESS X
DATA
DATA IN STABLE CURRENT ADDRESS X
Hi Z
DATA IN STABLE ADDRESS X + 1
t_{CE} (TGLQV)
t_{DF} (TGHQZ)
t_{DF} (TGHQZ)
$\bar{G}$
t_{DH} (TPLDX)
t_{DS} (TDVPH)
t_{PW} (TPHPL)
t_{OS} (TGHPH)
$\bar{E}/P$
t_{OH} (TPLGX)
2 · 2
1 1
t_{PR} (TPH 1PH2)
t_{PF} (TPL 1PL1)

Note: Symbols in parentheses are proposed JEDEC standard

PROGRAMMING OPERATION

DC AND OPERATING CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)
Notes 1 and 2

Symbol	Parameter	Min.	Max.	Units
I_{LI}	Input Leakage Current (Note 3)	—	10	µA
V_{IL}	Input Low Level	– 0.1	0.8	V
V_{IH}	Input High Level	2.0	$V_{CC} + 1$	V
I_{CC}	V_{CC} Power Supply Current	–	100	mA
I_{PP1}	V_{PP} Supply Current	—	5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse (Note 5)	—	30	mA

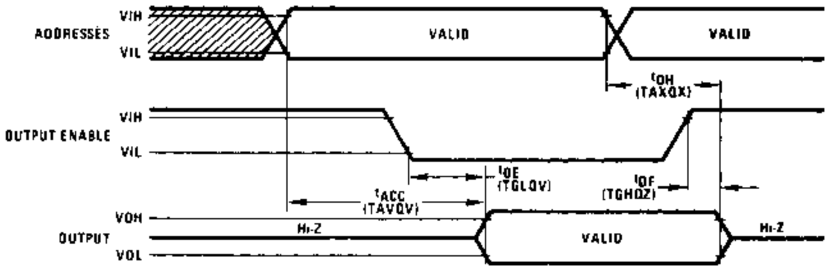
AC CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$) Notes 1, 2 and 6

Symbol		Parameter	Min.	Typ.	Max.	Units
Standard	Jedec					
t_{AS}	TAVPH	Address Setup Time	2	—	—	µs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2	—	—	µs
t_{DS}	TDVPH	Data Setup Time	2	—	—	µs
t_{AH}	TPLAX	Address Hold Time	2			µs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2	—	—	µs
t_{DH}	TPLDX	Data Hold Time	2	—	—	µs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0	—	100	ns
t_{OE}	TGLQV	Output Enable to Output Delay (Note 4)	—	—	120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5	—	—	ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5	—	—	ns

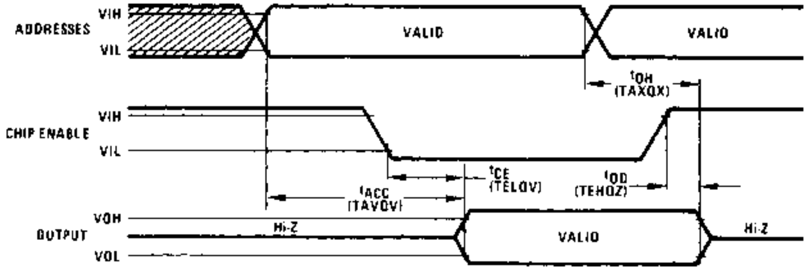
Notes 1. VCC must be applied at the same time of before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be insereted into a board with power applied.
2. Care must be taken to prevent overshoot of the VPP supply when switching + 25V
3. 0.45V ⩽ VIN < 5.25V
4. CE/PGM = VIL, VPP = VCC
5. VPP = 26 V
6. Transition times ⩽20 ns unless otherwise noted

SWITCHING TIME WAVEFORMS

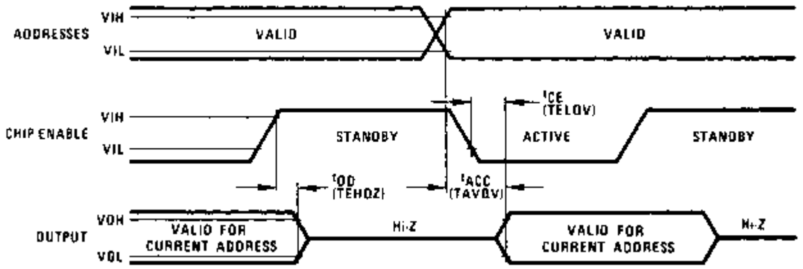
Read Cycle ($\overline{CE}$/PGM = VIL)


VIH
ADDRESSES
VIL
VALID
VALID
t_{OH} (TAXQX)
VIH
OUTPUT ENABLE
VIL
t_{OE} (TGLQV)
t_{DF} (TGHQZ)
t_{ACC} (TAVQV)
VOH
OUTPUT
VOL
Hi-Z
VALID
Hi-Z

Read Cycle ($\overline{OE}$ = VIL)


VIH
ADDRESSES
VIL
VALID
VALID
t_{OH} (TAXQX)
VIH
CHIP ENABLE
VIL
t_{CE} (TELQV)
t_{OD} (TEHQZ)
t_{ACC} (TAVQV)
VOH
OUTPUT
VOL
Hi-Z
VALID
Hi-Z

Standby Power Down Mode ($\overline{OE}$ = VIL)


VIH
ADDRESSES
VIL
VALID
VALID
t_{CE} (TELQV)
VIH
CHIP ENABLE
VIL
STANDBY
ACTIVE
STANDBY
t_{OD} (TEHQZ)
t_{ACC} (TAVQV)
VOH
OUTPUT
VOL
VALID FOR CURRENT ADDRESS
Hi-Z
VALID FOR CURRENT ADDRESS
Hi-Z

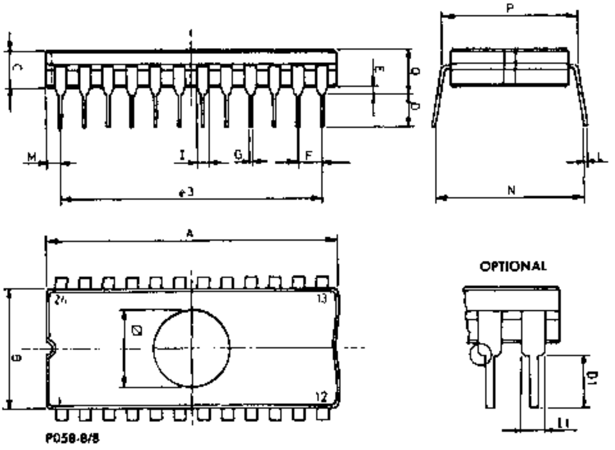
Symbols in parentheses are proposed JEDEC standard

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ET2716Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ET2716-Q1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F1	450 ns	5V ± 5%	0 to +70°C	DIP-24
M2716-1F1	350 ns	5V ± 10%	0 to +70°C	DIP-24
M2716F6	450 ns	5V ± 5%	−40 to +85°C	DIP-24
M2716-1F6	350 ns	5V ± 10%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1[1]	3.40			0.134		
E	0.50		1.78	0.020		0.070
e3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1[1]	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

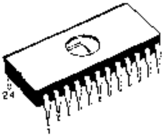
Note: 1. Optional see drawing

SGS-THOMSON
MICROELECTRONICS

M2732A

32K (4K × 8) NMOS UV ERASABLE PROM

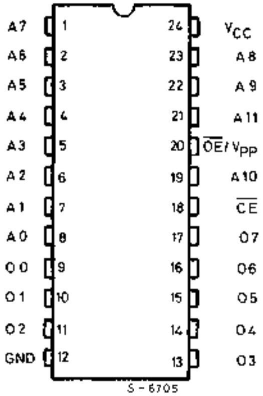
- FAST ACCESS TIME:
  200ns MAX M2732A-2F1
  250ns MAX M2732AF1/M2732AF6
  300ns MAX M2732A-3F1
  450ns MAX M2732A-4F1/M2732A-4F6
- 0 TO +70°C STANDARD TEMPERATURE RANGE
- −40 TO +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (35mA MAX)
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM
- COMPLETELY STATIC



F
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

The M2732A is a 32,768-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 4,096 words by 8 bits and manufactured using SGS-THOMSON' N-channel Si-Gate MOS process. The M2732A with its single +5V power supply and with an access time of 200ns, is ideal for use with the high performance +5V microprocessors such as the Z8*, Z80* and Z8000*.

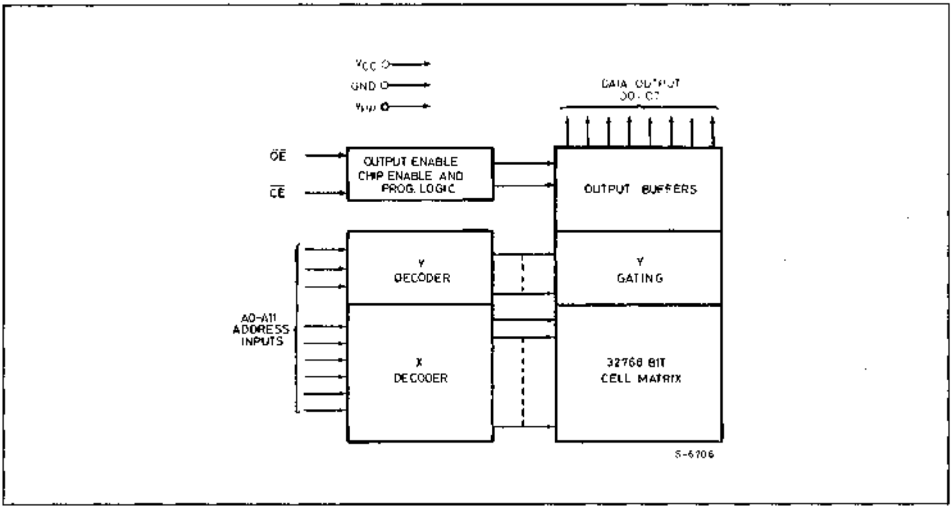
The M2732A has an important feature which is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control elimitates bus contention in multiple bus microprocessor systems.

The M2732A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 125 mA while the maximum standby current is only 35 mA a 70% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.
The M2732A is available in a 24-lead dual in-line ceramic package glass lens (frit-seal).

PIN NAMES

A0-A11	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
DATA OUTPUT
O0 - O7
$\overline{OE}$
$\overline{CE}$
OUTPUT ENABLE CHIP ENABLE AND PROG. LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A11 ADDRESS INPUTS
X DECODER
32768 BIT CELL MATRIX
S-6706

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
V_{PP}	Supply voltage with respect to ground during program	+ 22 to − 0.6	V
T_{amb}	Ambient temperature under bias F1/-2F1/-3F1/-4F1 F6/4F6	− 10 to + 80 − 50 to + 95	°C °C
T_{stg}	Storage temperature range	− 65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+5	D_{OUT}
STANDBY	V_{IH}	Don't Care	+5	High Z
PROGRAM	V_{IL}	V_{PP}	+5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	+5	High Z

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 2F1/ – 3F1/ – 4F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$			35	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$		70	125	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2732A-2		M2732A		M2732A-3		M2732A-4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		100		100		150		150	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	130	0	130	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE (4) ($T_{amb} = 25°C$, f = 1MHz)

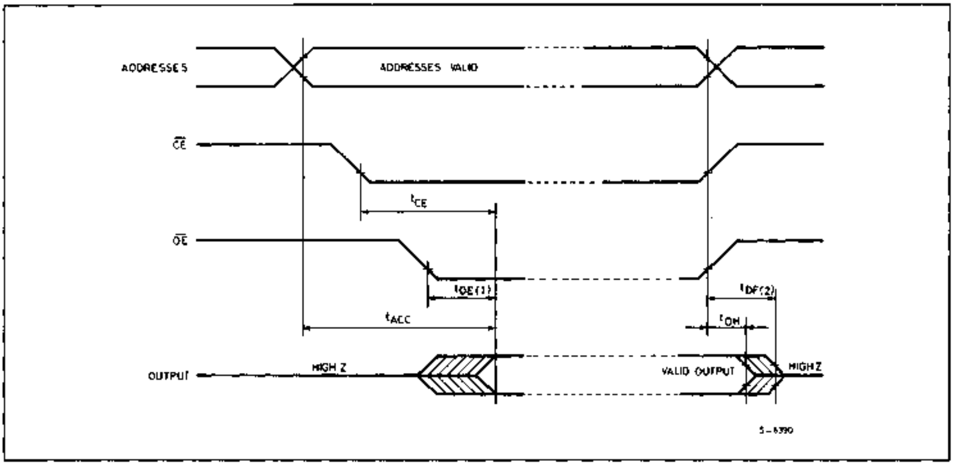
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	
C_{IN1}	Input Capacitance excepet $\overline{OE}/V_{PP}$	$V_{IN} = 0$		4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input capacitance	$V_{IN} = 0$			20	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested

READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC WAVEFORMS



Notes:
1. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2732A has a standby mode which reduces the active power current by 70%, from 125mA to 35mA. The M2732A is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because M2732A's are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING OPERATION(1) (T_{amb} = 25°C ±5°C, $V_{CC}^{(2)}$ = 5V ±5%, $V_{PP}^{(2,3)}$ = 21V ±0.5V)

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 μA	2.4			V
I_{CC2}	V_{CC} Supply Current (Active)			70	125	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}, \overline{OE} = V_{PP}$			30	mA

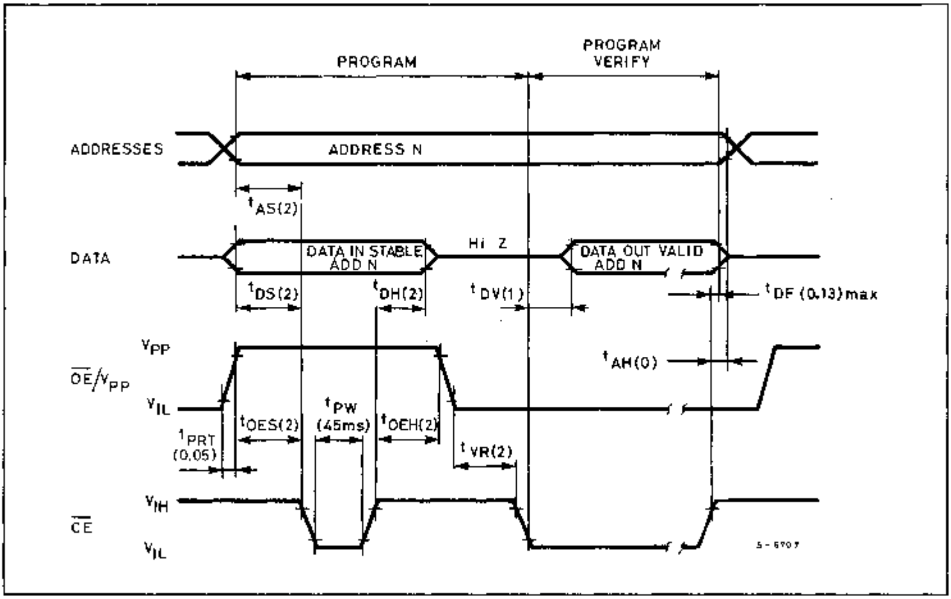
AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set Up Time		2			μs
t_{OES}	$\overline{OE}$ Set Up Time		2			μs
t_{DS}	Data Set Up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	ns
t_{DV}	Data valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1	μs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse rise time During Programming		50			ns
t_{VR}	V_{PP} recovery time		2			μs

Notes: 1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}. The M2732A must not be inserted into or removed from a board with V_{PP} at 21±0.5V or damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +22V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.

PROGRAMMING OPERATION (Continued)

PROGRAMMING WAVEFORMS



Notes: 1. All times shown in ( ) are minimum and in µsec unless otherwise specified.
2. The input timing reference level is 1V for V_{IL} and 2V for V_{IH}.
3. t_{OE} and t_{DF} are characteristics of the device but must be accomodated by the programmer.

PROGRAMMING

Caution: Exceeding 22V on pin (V_{PP}) will damage the M2732A.

When delivered, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 µF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple 2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled 2732As.

PROGRAM INHIBIT

Programming of multiple 2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel 2732As may be common. A TTL level program pulse applied to a 2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that 2732A. A high level $\overline{CE}$ input inhibits the other 2732As from being programmed.

PROGRAMMING OPERATION (Continued)

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}.

ERASURE OPERATION

The erasure characteristics of the M2732A are such that erasure begins when the cels are exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2732A window to prevent unintentional erasure.

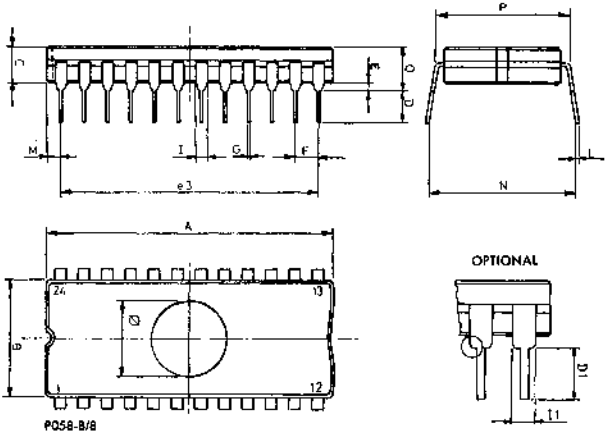
The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2732AF1	250 ns	5V ± 5%	0 to +70°C	DIP-24
M2732A2F1	200 ns	5V ± 5%	0 to +70°C	DIP-24
M2732A3F1	300 ns	5V ± 5%	0 to +70°C	DIP-24
M2732A4F1	450 ns	5V ± 5%	0 to +70°C	DIP-24
M2732AF6	250 ns	5V ± 5%	−40 to +85°C	DIP-24
M2732A-4F6	450 ns	5V ± 5%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1[1]	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1[1]	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

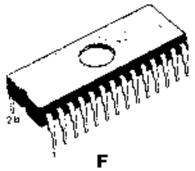
Note: 1. Optional see drawing

SGS-THOMSON
MICROELECTRONICS

M2764A

64K (8K × 8) NMOS UV ERASABLE PROM

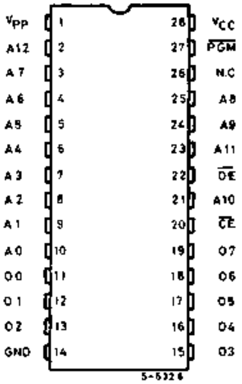
- FAST ACCESS TIME:
  180ns MAX M2764A-1F1/M2764A-18F1
  200ns MAX M2764A-2F1/M2764A-20F1
  250ns MAX M2764AF1/M2764AF6/M2764A-25F1
  300ns MAX M2764A-3F1/M2764A-30F1
  450ns MAX M2764A-4F1/M2764A-4F6/M2764A-45F1
- 0 to +70°C STANDARD TEMPERATURE RANGE
- −40 to +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (35mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

The M2764A is a 65,536-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 8,192 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

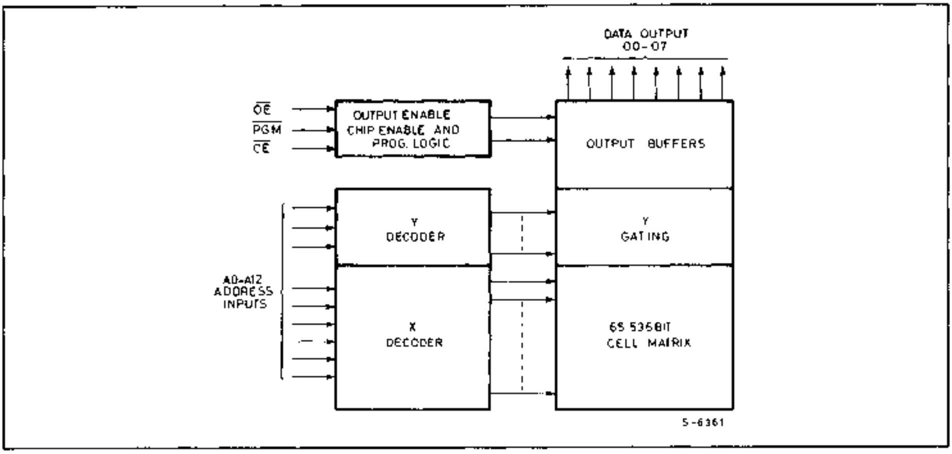
The M2764A with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The M2764A has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The M2764A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 75mA while the maximum standby current is only 35 mA, a 53% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M2764A has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M2764A is available in a 28-lead dual in-line ceramic package (frit-seal) glass lens.

PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


DATA OUTPUT
O0-O7
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE
CHIP ENABLE AND
PROG. LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A12
ADDRESS
INPUTS
X
DECODER
65 536BIT
CELL MATRIX
5-6361

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.5 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to +80 − 50 to +95	°C °C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 1F1/ – 2F1 – 3F1/ – 4F1	– 18F1/ – 20F1/ – 25F1 – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply $^{(1,2)}$	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Voltage $^{(2)}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.$^{(3)}$	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
$I_{PP1(2)}$	V_{PP} Current Read	$V_{PP} = 5.5V$			5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			35	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$			75	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V
$V_{PP(2)}$	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm$ 5%	2764A-1		2764A-2		2764A		2764A-3		2764A-4		Unit
		$V_{CC} \pm 10\%$	2764A-18		2764A-20		2764A-25		2764A-30		2764A-45		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		180		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		180		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		65		75		100		120		150	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		55	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		0		ns

CAPACITANCE$^{(5)}$ ($T_{amb} = 25$°C, f = 1 MHz)

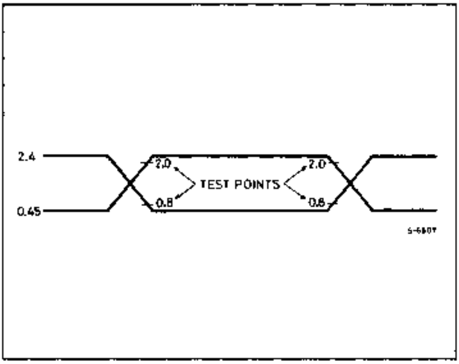
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25$°C and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and is not 100% tested.

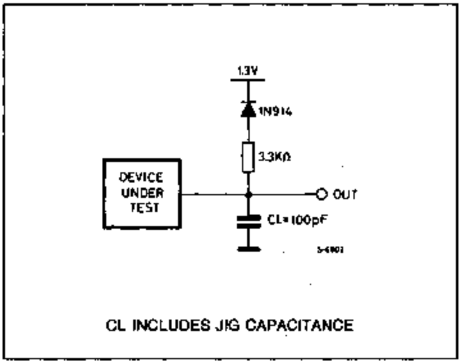
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

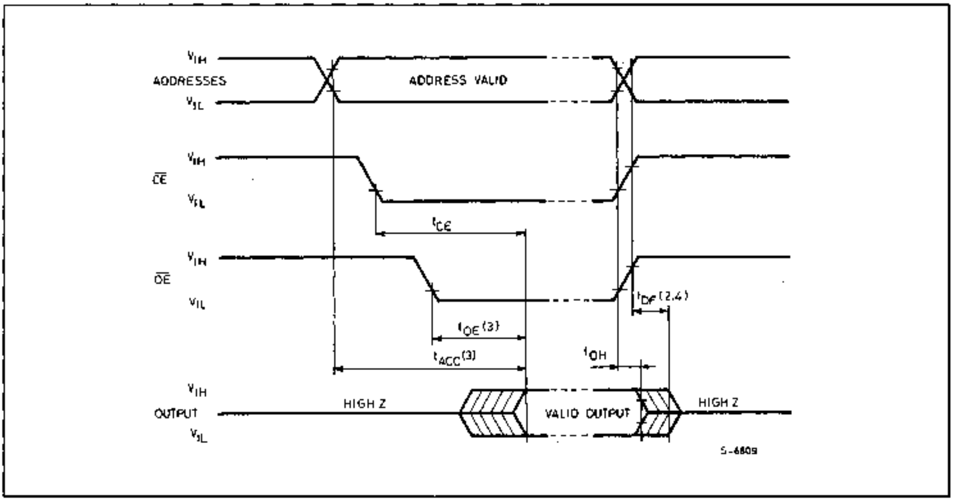

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6808

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE
V_IH
OE
V_IL
t_DF (2,4)
t_OE (3)
t_ACC (3)
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes:

1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the M2764A are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M2764A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2764A has a standby mode which reduces the maximum active power current from 75 mA to 35 mA. The M2764A is placed in the standby mode by applying a TTL high signal to the $\overline{\text{CE}}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{\text{CE}}$ should be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ should be made a common connection to all devices in the array and connected to the $\overline{\text{READ}}$ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{\text{CE}}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND.

This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 1 (V_{PP}) will damage the M2764A.

When delivered, and after each erasure, all bits of the M2764A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2764A is in the programming mode when V_{PP} input is at 12.5V and $\overline{\text{CE}}$ and $\overline{\text{PGM}}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M2764A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M2764A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{\text{PGM}}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M2764A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

DEVICE OPERATION (Continued)

The entire sequence of program pulses and byte verifications is performed at $V_{CC}=6V$ and $V_{PP}=12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}=V_{PP}=5V$.

PROGRAM INHIBIT

Programming of multiple M2764As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M2764A may be common. A TTL low pulse applied to a M2764A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M2764A. A high level $\overline{CE}$ input inhibits the other M2764A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M2764A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M2764A. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0=V_{IL}$) represents the manufacturer code and byte 1 ($A0=V_{IH}$) the device identifier code. For the SGS-THOMSON M2764A, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M2764A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2764A in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M2764A is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M2764A window to prevent unintentional erasure. The recommended erasure procedure for the M2764A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M2764A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	0	0	0	08

PROGRAMMING OPERATION (T_{amb} = 25°C ± 5°C, $V_{CC}^{(1)}$ = 6V ± 0.25V, $V_{PP}^{(1)}$ = 12.5V ± 0.3V)

DC AND OPERATING CHARACTERISTIC

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		– 0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = – 400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				75	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

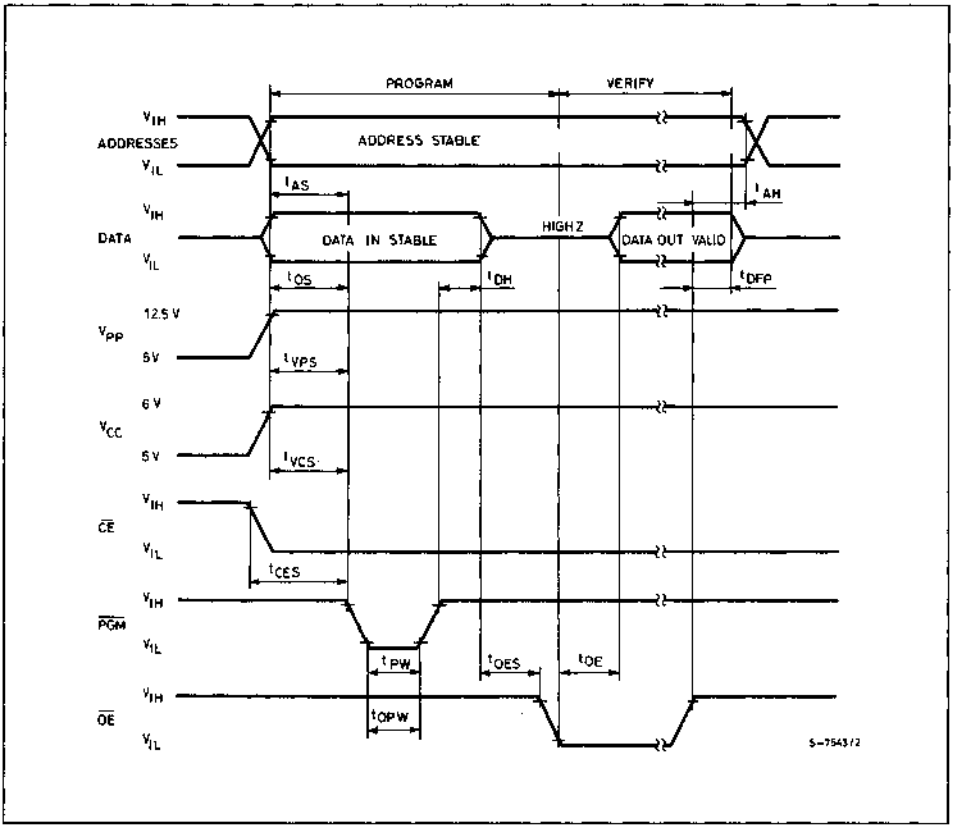
AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

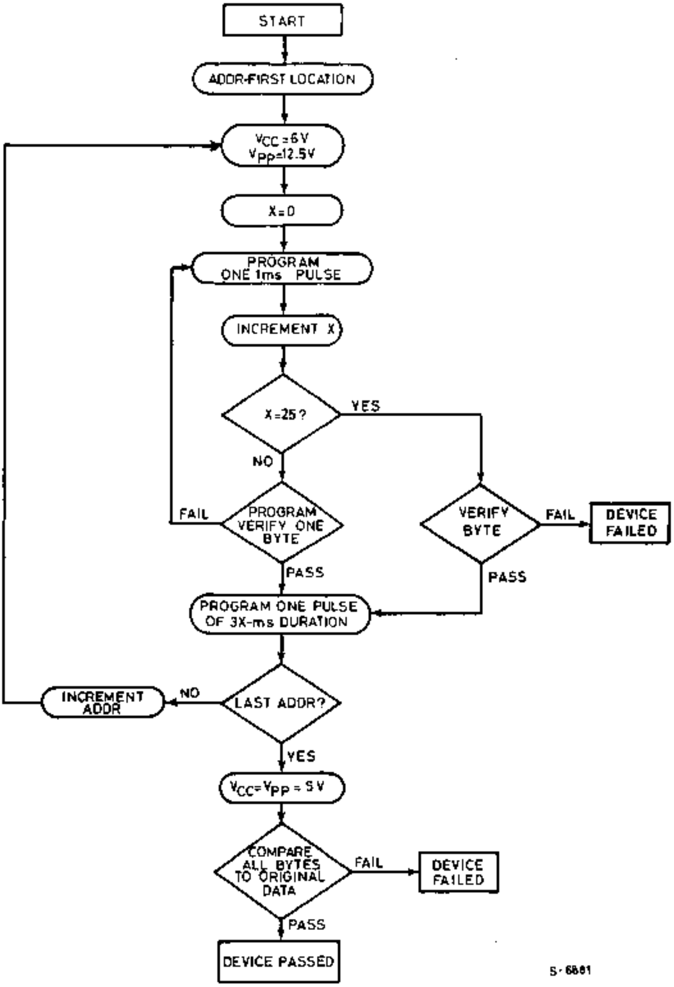
PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5 V
5 V
t_{VPS}
V_{CC}
6 V
5 V
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
t_{OPW}
S-7543/2

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M2764A a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

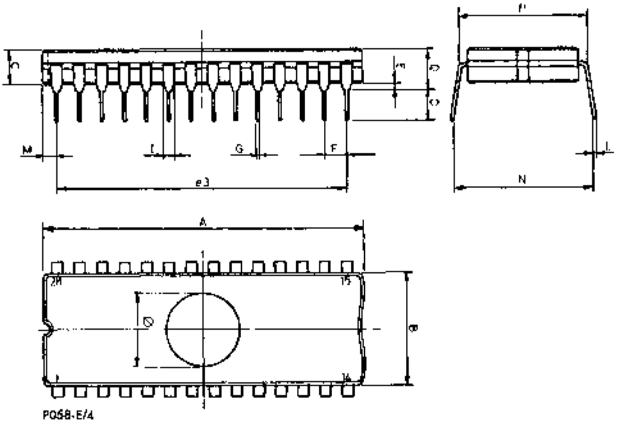

START
ADDR-FIRST LOCATION
VCC = 6V
VPP=12.5V
X=0
PROGRAM ONE 1ms PULSE
INCREMENT X
X=25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC=VPP = 5V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S-6881

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2764A-1F1	180 ns	5V ± 5%	0 to +70°C	DIP-28
M2764A-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M2764AF1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M2764A-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M2764A-4F1	450 ns	5V ± 5%	0 to +70°C	DIP-28
M2764A-18F1	180 ns	5V ± 10%	0 to +70°C	DIP-28
M2764A-20F1	200 ns	5V ± 10%	0 to +70°C	DIP-28
M2764A-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-28
M2764A-30F1	300 ns	5V ± 10%	0 to +70°C	DIP-28
M2764A-45F1	450 ns	5V ± 10%	0 to +70°C	DIP-28
M2764AF6	250 ns	5V ± 5%	−40 to +85°C	DIP-28
M2764A-4F6	450 ns	5V ± 5%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



PO58-E/4

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

SGS-THOMSON
MICROELECTRONICS

M27128A

128K (16K x 8) NMOS UV ERASABLE PROM

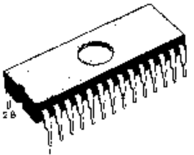
- FAST ACCESS TIME:
  150ns MAX M27128A-1F1
  200ns MAX M27128A-2F1/M27128A-20F1
  250ns MAX M27128AF1/M27128AF6/M27128A-25F1
  300ns MAX M27128A-3F1/M27128A-30F1
  450ns MAX M27128A-4F1/M27128A-4F6/M27128A-45F1
- 0 to +70°C STANDARD TEMPERATURE RANGE
- −40 to +85°C EXTENDED TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE

DESCRIPTION

The M27128A is a 131,072-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 16,384 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

The M27128A with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The M27128A has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

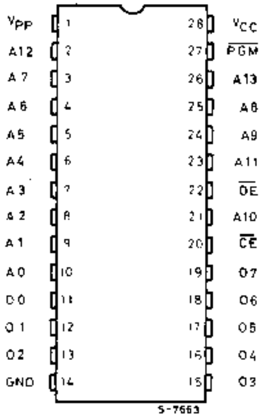
The M27128A also features a standby mode which reduces the power dissipation without increasing access time. The active current is 85mA while the maximum standby current is only 40 mA, a 53% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27128A has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M27128A is available in a 28-lead dual in-line ceramic package (frit-seal) glass lens.



F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

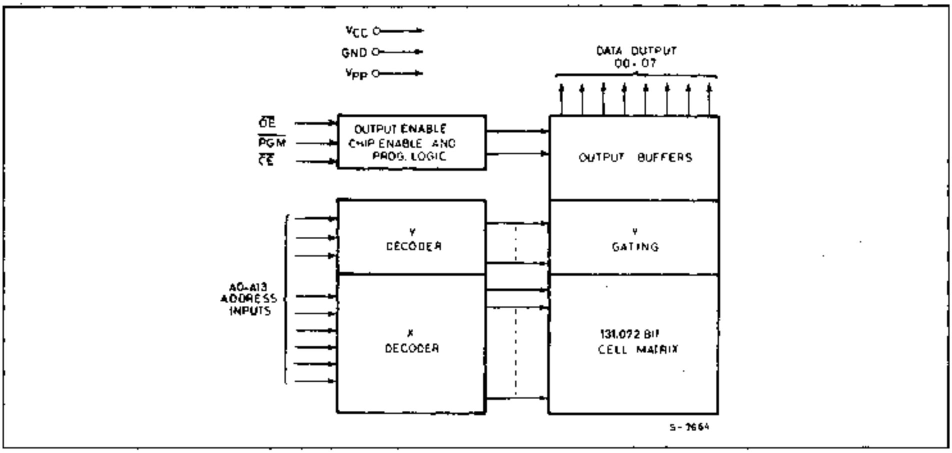
PIN CONNECTIONS



PIN NAMES

A0-A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


VCC
GND
VPP
DATA OUTPUT
O0 - O7
OE
PGM
CE
OUTPUT ENABLE
CHIP ENABLE AND
PROG. LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A13
ADDRESS
INPUTS
X
DECODER
131,072 BIT
CELL MATRIX
S - 7664

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.25 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0.6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to +80 − 50 to +95	°C °C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 1F1/ – 2F1/ – 3F1/ – 4F1	– 20F1/ – 25F1/ – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{PP1}(2)	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			40	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$			85	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
V_{PP}(2)	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm$ 5%	27128A-1		27128A-2		27128A		27128A-3		27128A-4		Unit
		$V_{CC} \pm 10\%$			27128A-20		27128A-25		27128A-30		27128A-45		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		65		75		100		120		150	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		55	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		0		ns

CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

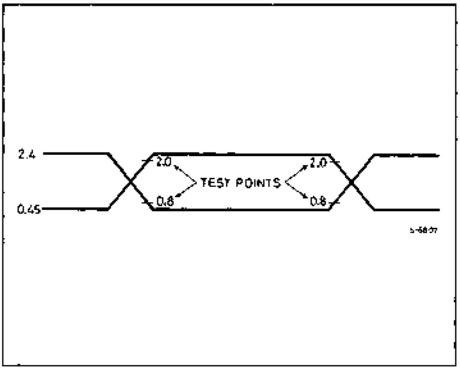
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}^{2}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven. (See timing diagram).
5. This parameter is only sampled and is not 100% tested.

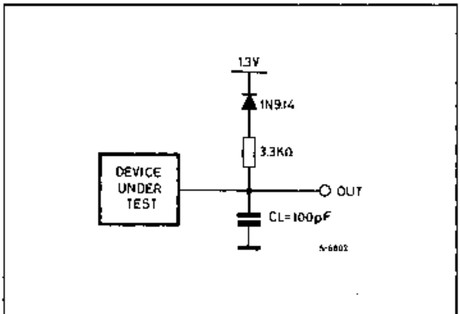
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

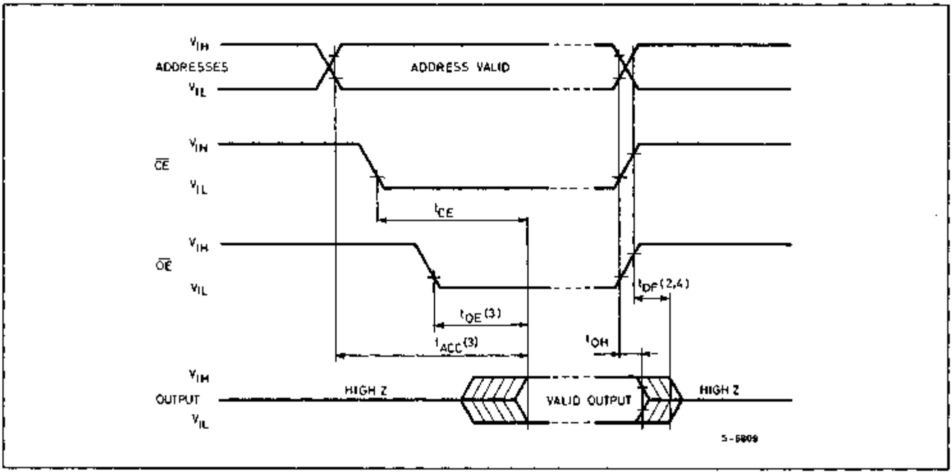

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
5-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE
VIH
OE
VIL
tDF (2,4)
tOE (3)
tACC (3)
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
5-6809

Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the M27128A are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27128A has a standby mode which reduces the maximum active power current from 85 mA to 40 mA. The M27128A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors.

It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the M27128A.

When delivered, and after each erasure, all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

DEVICE OPERATION (Continued)

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple M27128As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27128A. A high level $\overline{CE}$ input inhibits the other M27128A from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27128A. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27128A. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M27128A, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27128A should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	0	0	1	89

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, V_{CC}(1) = 6V ±0.25V, V_{PP}(1) = 12.5V ±0.3V)

DC AND OPERATING CHARACTERISTIC

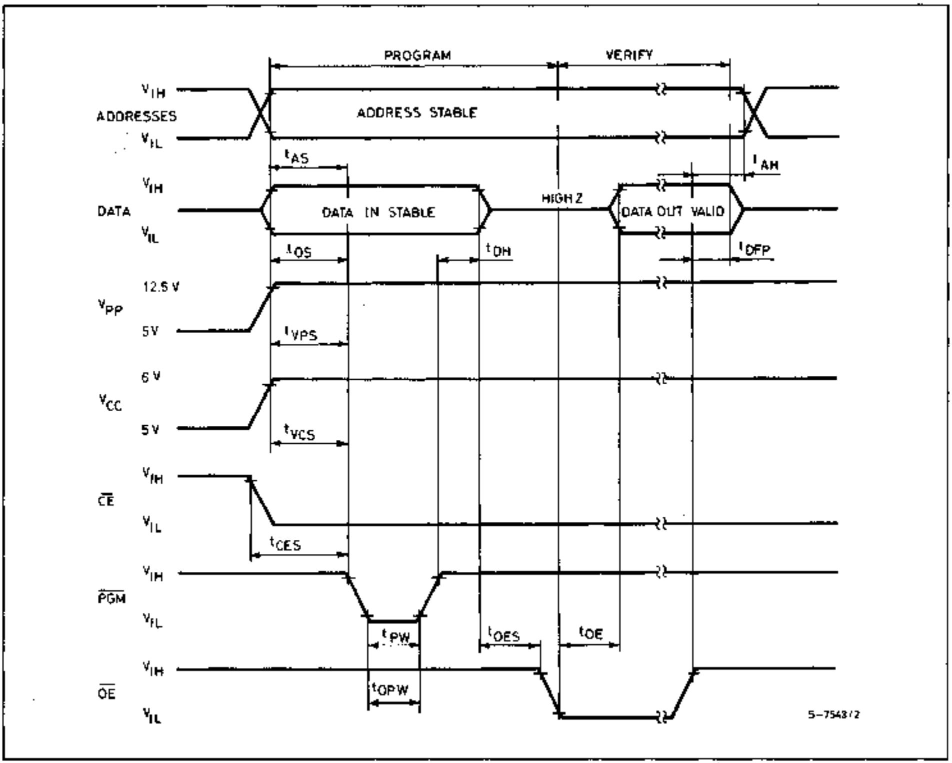
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

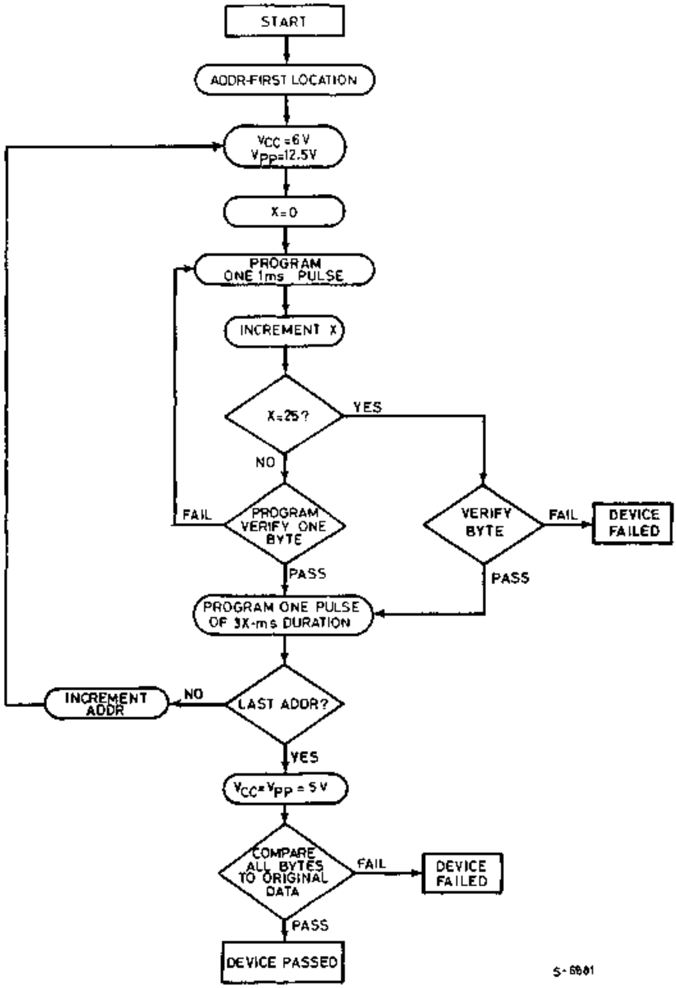
PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5 V
5V
t_{VPS}
V_{CC}
6 V
5 V
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OPW}
t_{OES}
t_{OE}
$\overline{OE}$
5–7543/2

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27128A a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

AST PROGRAMMING FLOWCHART


START
ADDR-FIRST LOCATION
$V_{CC}=6V$
$V_{PP}=12.5V$
X=0
PROGRAM ONE 1ms PULSE
INCREMENT X
X=25?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
$V_{CC}=V_{PP}=5V$
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

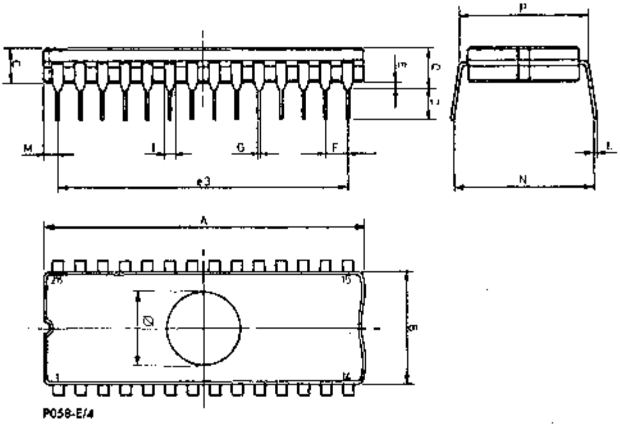
S-6881

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27128A-1F1	150 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M27128AF1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-4F1	450 ns	5V ± 5%	0 to +70°C	DIP-28
M27128A-20F1	200 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-30F1	300 ns	5V ± 10%	0 to +70°C	DIP-28
M27128A-45F1	450 ns	5V ± 10%	0 to +70°C	DIP-28
M27128AF6	250 ns	5V ± 5%	−40 to +85°C	DIP-28
M27128A-4F6	450 ns	5V ± 5%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			13.00	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
∅	6.86		7.36	0.270		0.290

SGS-THOMSON
MICROELECTRONICS

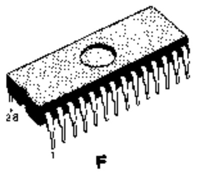
M27256

256K (32K×8) NMOS UV ERASABLE PROM

- FAST ACCESS TIME:
  170ns MAX M27256-1F1
  200ns MAX M27256-2F1/M27256-20F1
  250ns MAX M27256F1/M27256F6/M27256-25F1
  300ns MAX M27256-3F1/M27256-30F1
  450ns MAX M27256-4F1/M27256-4F6/M27256-45F1
- 0 to +70°C STANDARD TEMP. RANGE
- −40 to +85°C EXTENDED TEMP. RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE

DESCRIPTION

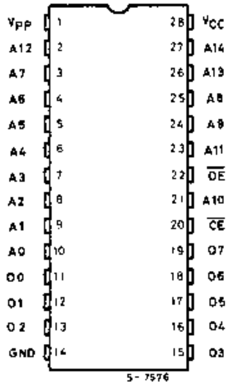
The M27256 is a 262,144-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 32.768 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process. The M27256 with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The M27256 has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. The M27256 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40 mA, a 60% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27256 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the M27256's high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27256 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27256 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27256 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.



F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

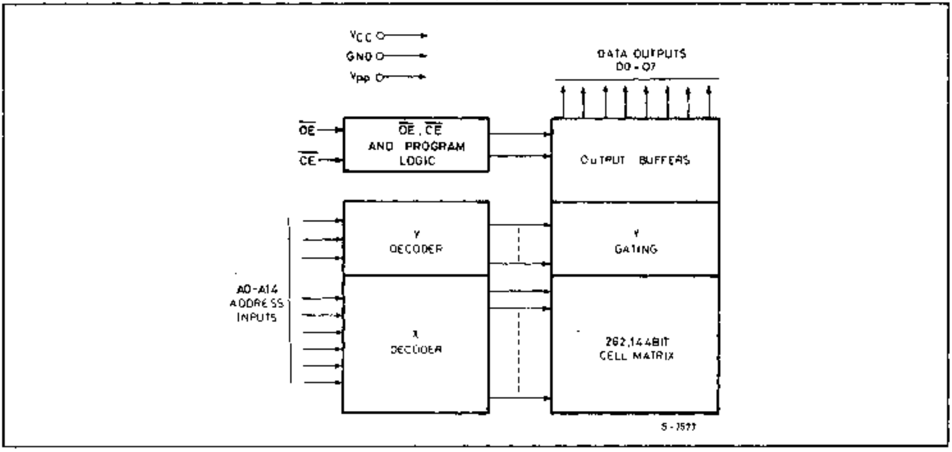
PIN CONNECTIONS



PIN NAMES

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


VCC
GND
VPP
DATA OUTPUTS
D0 - O7
$\overline{OE}$
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$
AND PROGRAM
LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A14
ADDRESS
INPUTS
X
DECODER
262,144BIT
CELL MATRIX
S - 7577

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+6.25 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to +80 −50 to +95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	A0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
OPTIONAL VERIFY	V_{IL}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 1F1/ – 2F1/ – 3F1/ – 4F1	– 20F1/ – 25F1/ – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply [1,2]	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Voltage [2]	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. [3]	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{PP1}[2]	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
I_{CC1}[2]	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
I_{CC2}[2]	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$		45	100	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA	2.4			V
V_{PP}[2]	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm$ 5%	27256-1		27256-2		27256		27256-3		27256-4		Unit
		$V_{CC} \pm 10\%$			27256-20		27256-25		27256-30		27256-45		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		70		75		100		120		150	ns
t_{DF}[4]	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		35	0	55	0	60	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		0		ns

CAPACITANCE[5] ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

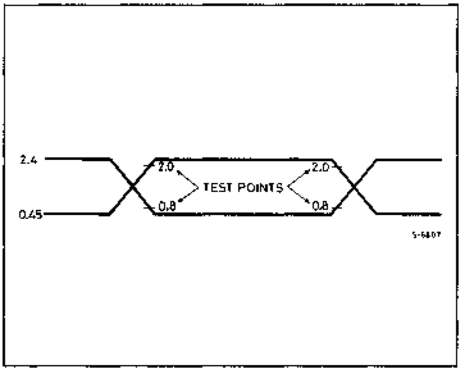
Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

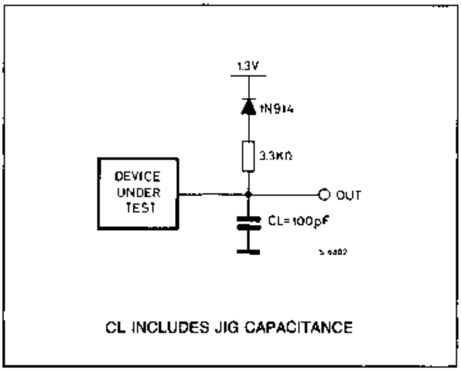
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

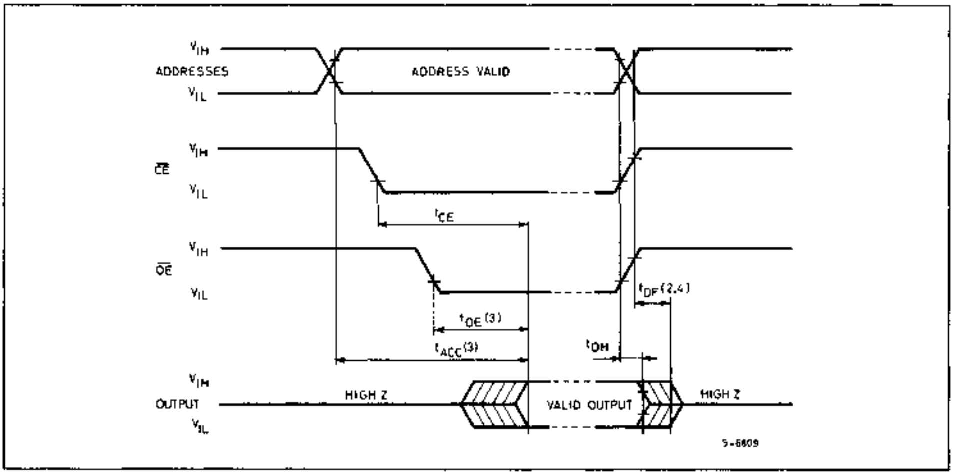
AC TESTING INPUT/OUTPUT WAVEFORM


2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6407

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6402
CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE
VIH
OE
VIL
tDF (2,4)
tOE (3)
tACC (3)
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
S-6609

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The eight modes of operations of the M27256 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The M27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27256 has a standby mode which reduces the maximum active power current from 100 mA to 40 mA. The M27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the M27256.

When delivered, and after each erasure, all bits of the M27256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27256 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27256 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the M27256 Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27256 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC}=6V$ and $V_{PP}=12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}=V_{PP}=5V$.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27256 may be common. A TTL low pulse applied to a M27256's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27256. A high level $\overline{CE}$ input inhibits the other M27256s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with $V_{PP} = 12.5V$ and $\overline{OE} = V_{IL}$ will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (= 6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27256. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M27256, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27256 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27256 window to prevent unintentional erasure. The recommended erasure procedure for the M27256 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M27256 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	1	0	0	04

PROGRAMMING OPERATION ($T_{amb} = 25°C \pm 5°C$, $V_{CC}^{(1)} = 6V \pm 0.25V$, $V_{PP}^{(1)} = 12.5V \pm 0.3V$

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ μA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

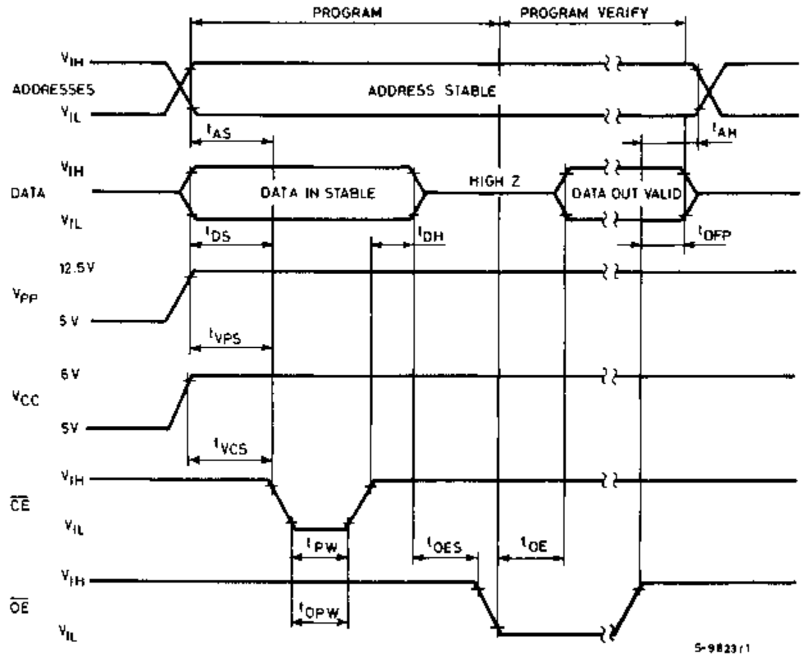
AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

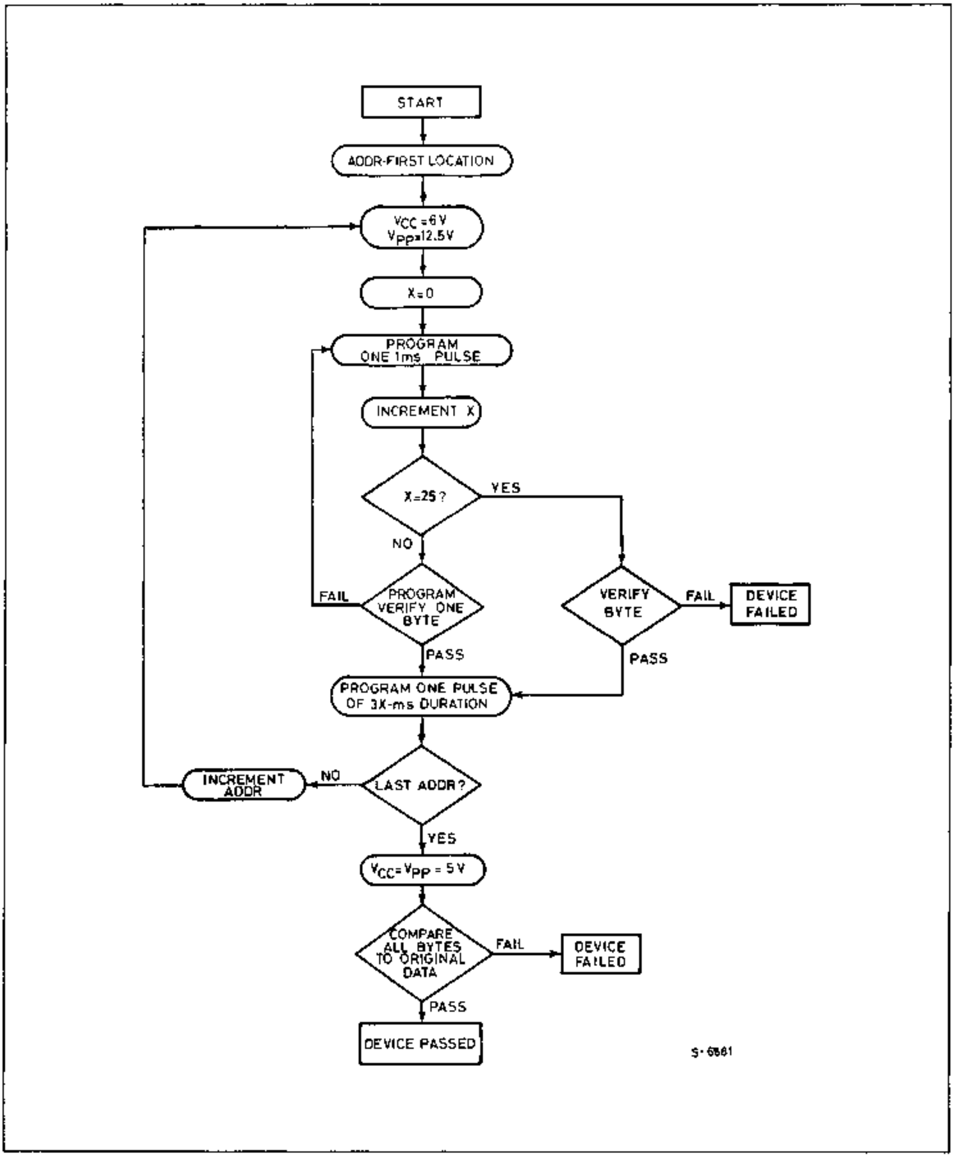
PROGRAMMING WAVEFORMS


PROGRAM
PROGRAM VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5V
5 V
t_{VPS}
V_{CC}
6 V
5V
t_{VCS}
$\overline{CE}$
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
t_{OPW}
5-9823/1

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27256 a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

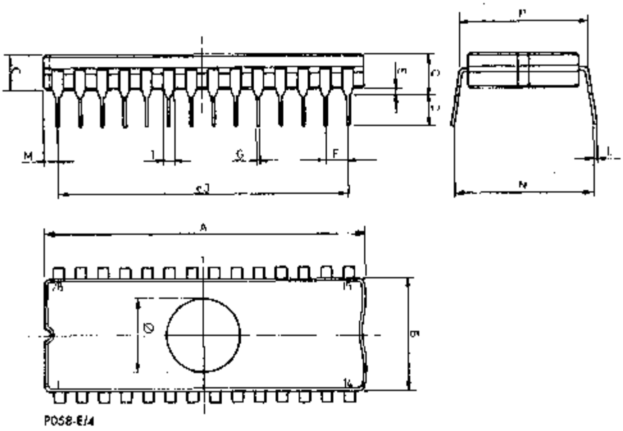

START
ADDR-FIRST LOCATION
VCC = 6V
VPP = 12.5V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR ?
YES
VCC = VPP = 5V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S - 6861

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27256-1F1	170 ns	5V ± 5%	0 to +70°C	DIP-28
M27256-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M27256F1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M27256-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M27256-4F1	450 ns	5V ± 5%	0 to +70°C	DIP-28
M27256-20F1	200 ns	5V ±10%	0 to +70°C	DIP-28
M27256-25F1	250 ns	5V ±10%	0 to +70°C	DIP-28
M27256-30F1	300 ns	5V ±10%	0 to +70°C	DIP-28
M27256-45F1	450 ns	5V ±10%	0 to +70°C	DIP-28
M27256F6	250 ns	5V ± 5%	−40 to +85°C	DIP-28
M27256-4F6	450 ns	5V ± 5%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE

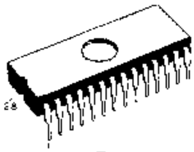


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.30		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.170		0.290

512K (64K × 8) NMOS UV ERASABLE PROM

PRELIMINARY DATA

- FAST ACCESS TIME: 200ns MAX M27512-2F1
- 0 TO +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE
- FAST PROGRAMMING
- ELECTRONIC SIGNATURE



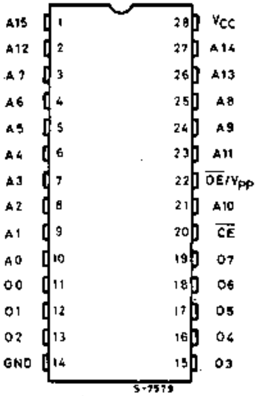
F
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M27512 is a 524,288-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process. The M27512 with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor allowing full speed operation without the addition of performance-degrading WAIT states. The M27512 has an important feature which is to separate the output control, Output Enable ($\overline{OE}/V_{PP}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}/V_{PP}$ control eliminates bus contention in multiple bus microproces sor systems. The M27512 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 125mA while the maximum standby current is only 40 mA, a 70% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the M27512s high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27512 large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27512 directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The M27512 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The M27512 is available in a 28-lead dual in-line ceramic package glass lens (frit seal).

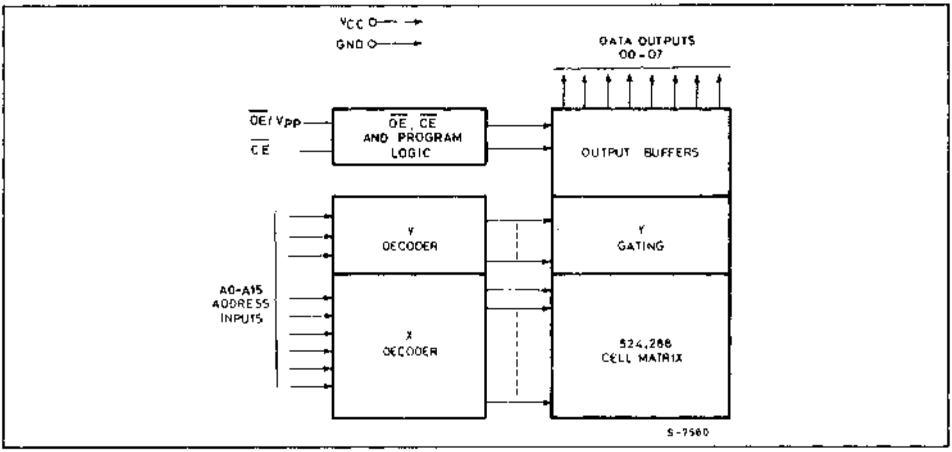
PIN CONNECTIONS



PIN NAMES

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}/V_{PP}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


V_{CC}
GND
DATA OUTPUTS
O0 - O7
$\overline{OE}$/ V_{PP}
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$
AND PROGRAM
LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A15
ADDRESS
INPUTS
X
DECODER
524,288
CELL MATRIX
S-7560

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.5 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to − 0.6	V
T_{amb}	Ambient temperature under bias /F1 /F6	−10 to + 80 −50 to + 95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	A0 (10)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{PP}	X	X	V_{CC}	D_{IN}
PROGRAM INHIBIT	V_{IH}	V_{PP}	X	X	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	MAN.CODE DEV.CODE

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	F1/ – 2F1/ – 3F1/	– 25F1/ – 30F1	F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ± 5%	5V ± 10%	5V ± 5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (2)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		90	125	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm 5\%$	27512-2		27512		27512-3		Unit
		$V_{CC} \pm 10\%$			27512-25		27512-30		
		Test Conditions	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120	ns
t_{DF}(3)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0		0		0		ns

CAPACITANCE(4) ($T_{amb} = 25°C$, f = 1 MHz)

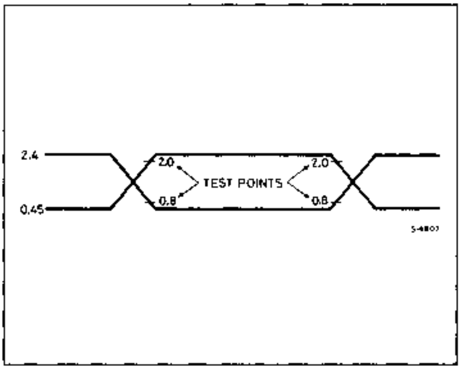
Symbol	Parameter	Test Conditions	Min.	Typ. (2)	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
4. This parameter is only sampled and not 100% tested.

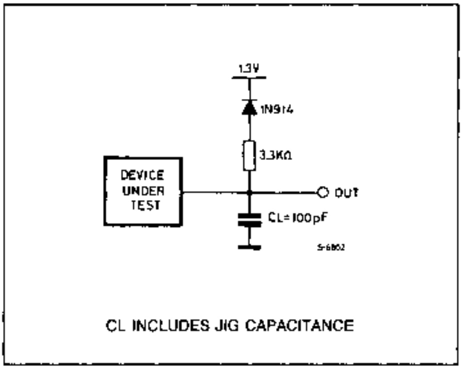
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

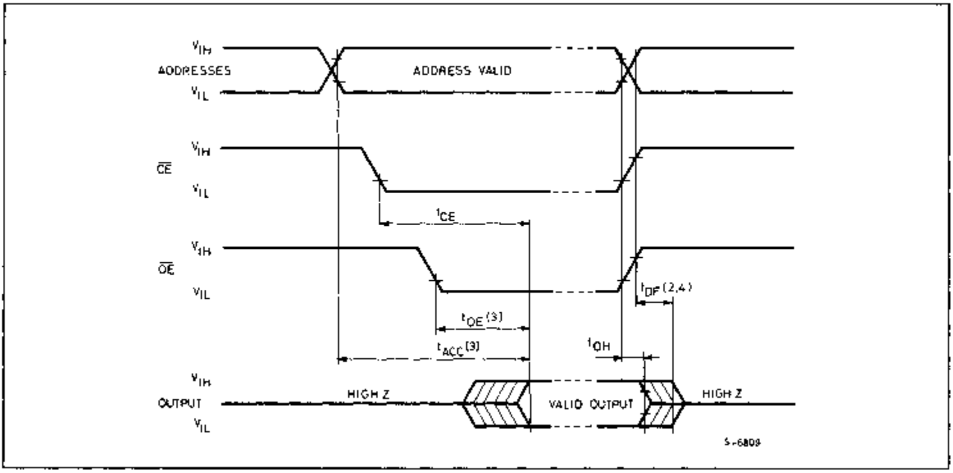

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6862

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE
V_IH
OE
V_IL
t_DF (2,4)
t_OE (3)
t_ACC (3)
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes: 1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}/V_{PP}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The six modes of operations of the M27512 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ and 12V on A9 for Electronic Signature.

READ MODE

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27512 has a standby mode which reduces the maximum active power current from 125 mA to 40 mA. The M27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will permanently damage the M27512.

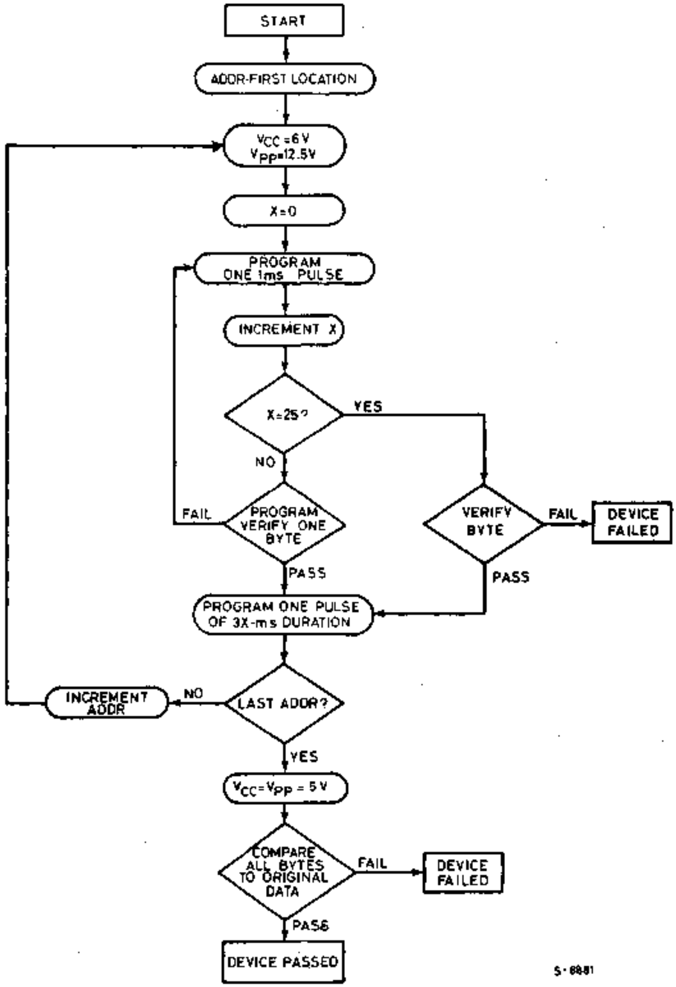
When delivered, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27512 is in the programming mode when $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. The M27512 can use PRESTO* Programming Algorithm that drasticaly reduces the programming time (typically less than 50 seconds) nevertheless to achieve compatibility with all programming equipments, standard FAST Programming Algorithm can be used as well.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M27512 EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 Fast Programming Algorithm is shown in the next page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3X msec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses is performed at $V_{CC}=6V$ and $\overline{OE}/V_{PP}=12.5V$ (byte verifications at $V_{CC}=6V$ and $\overline{OE}/V_{PP}=V_{IL}$). When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}=5V$.

DEVICE OPERATIONS (Continued)

FAST PROGRAMMING ALGORITHM FLOW CHART


START
ADDR-FIRST LOCATION
VCC=6V
VPP=12.5V
X=0
PROGRAM ONE 1ms PULSE
INCREMENT X
X=25?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
VCC=VPP = 5V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S-8881

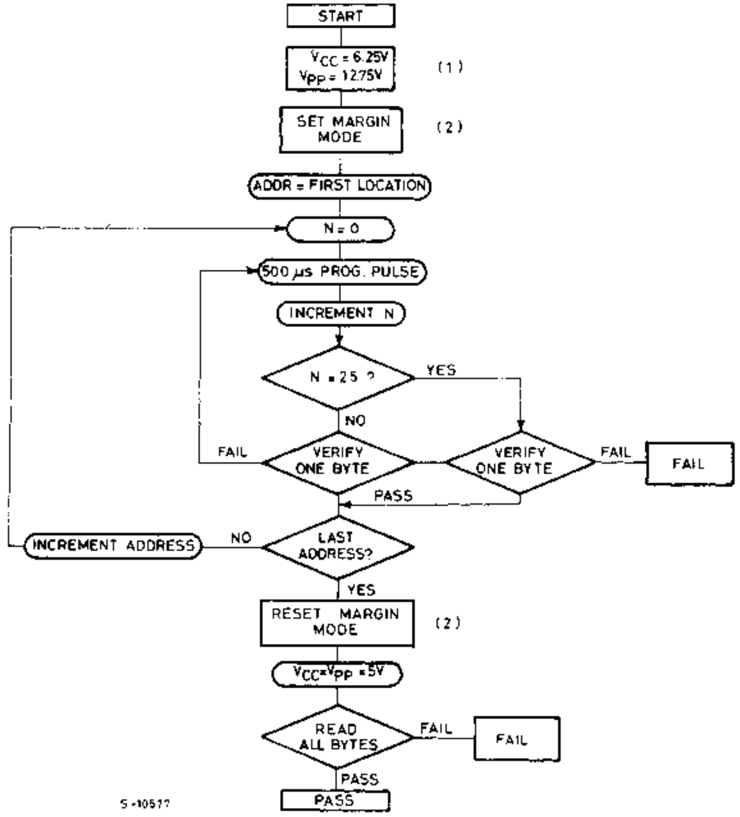
DEVICE OPERATION (Continued)

PRESTO PROGRAMMING ALGORITHM

PRESTO Programming Algorithm allows to programm the whole array with a guaranteed margin, in a typical time of less than 50 seconds (to be compared with 283 seconds for the Fast algorithm). This can be achieved with SGS-THOMSON M27512 due to several design innovations described in next paragraph to improve programming efficiency and to bring adequate margin for reliability. Before starting the programming the internal MARGIN MODE* circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 500 microseconds program pulses are applied to each byte until a correct verify occurs. No overprogram pulses are applied since the verify in MARGIN MODE provides the necessary margin to each programmed cell. PRESTO programming algorithm is supported on the full line of DATA I/O programmers,for the most popular production equipments the firmware revision are:

- Series 1000: revision V08.1
- Mode 120 A and 121A: revision V14.1

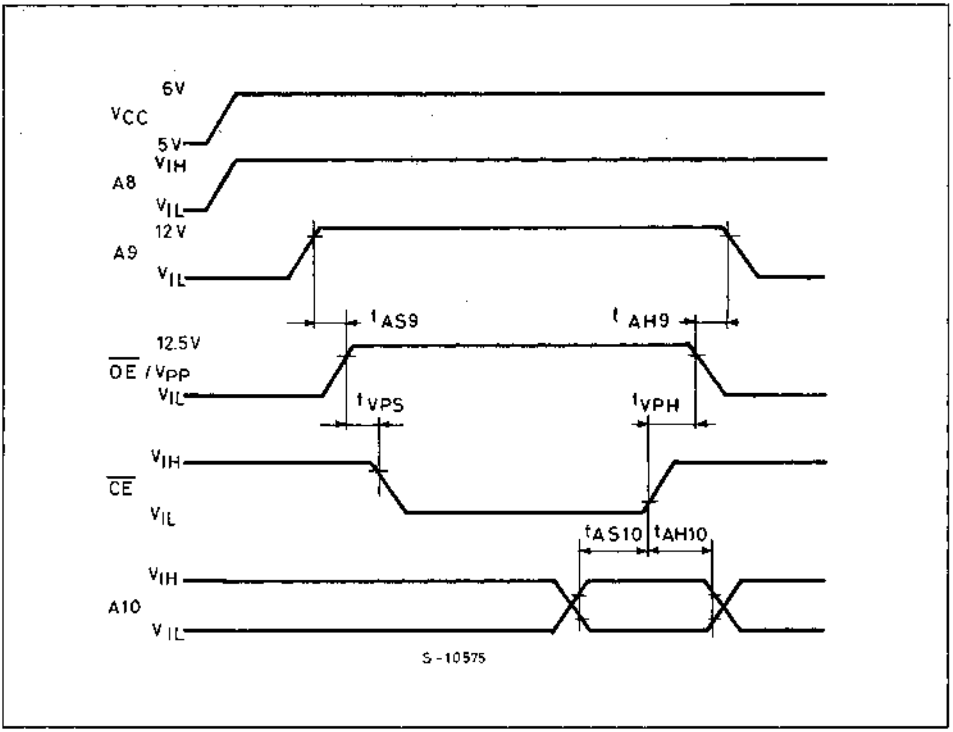
PRESTO PROGRAMMABLE ALGORITHM FLOW CHART


START
V_{CC} = 6.25V
V_{PP} = 12.75V
(1)
SET MARGIN MODE
(2)
ADDR = FIRST LOCATION
N = 0
500 µs PROG. PULSE
INCREMENT N
N = 25 ?
YES
NO
FAIL
VERIFY ONE BYTE
VERIFY ONE BYTE
FAIL
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
RESET MARGIN MODE
(2)
V_{CC}=V_{PP} =5V
READ ALL BYTES
FAIL
FAIL
PASS
PASS
S-10517

Notes: 1. V_{CC} must be mantained at 6V during the whole programming algorithm between set and reset MARGIN MODE operations. A drop of V_{CC} below 4V could reset the internal MARGIN MODE flip-flop giving place to insufficient programming margins.
2. See MARGIN MODE set and reset waveforms.

DEVICE OPERATION (Continued)

MARGIN MODE SET AND RESET WAVEFORMS


6V
VCC
5V
VIH
A8
VIL
12V
A9
VIL
tAS9
tAH9
12.5V
OE / VPP
VIL
tVPS
tVPH
VIH
CE
VIL
tAS10
tAH10
VIH
A10
VIL
S-10575

Notes: 1. Other addresses are don't care
2. Set MARGIN MODE A10 = V_{IH}, Reset MARGIN MODE A10 = V_{IL}

MARGIN MODE AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS10}	A10 Set Up Time		1			µs
t_{AH10}	A10 Hold Time		1			µs
t_{VPH}	V_{PP} Hold Time		2			µs
t_{VPS}	V_{PP} Set Up Time		2			µs
t_{AS9}	A9 Set up Time		2			µs
t_{AH9}	A9 Hold Time		2			µs

DEVICES OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple M27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{PP}$) of the parallel M27512 may be common. A TTL low level pulse applied to a M27512's $\overline{CE}$ input, with $\overline{OE}/V_{PP}$ at 12.5V, will program that M27512. A high level $\overline{CE}$ input inhibits the other M27512s from being programmed.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the M27512. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be held high. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS M27512, these two identifier bytes are given here below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ERASURE OPERATION

The erasure characteristic of the M27512 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27512 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27512 window to prevent unintentional erasure. The recommended erasure procedure for the M27512 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The M27512 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	1	0	1	0D

Note: A9 = 12V ±0.5V; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$; A14, A15 = V_{IH}

PROGRAMMING OPERATION (T_{amb} = 25°C ± 5°C, V_{CC}(1) = 6V ± 0.25V, OE/V_{PP}(1) = 12.5V ± 0.5V)

DC AND OPERATING CHARACTERISTIC:

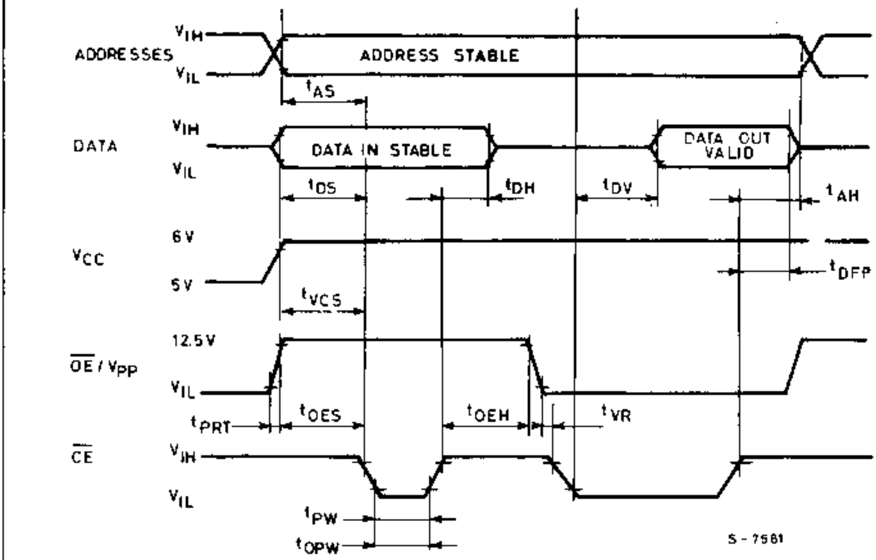
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		– 0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = – 400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current				150	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2			µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VCS}	V_{CC} Setup Time		0			µs
t_{PW}(3)	$\overline{CE}$ Initial Program Pulse Width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{CE}$ Overprogram Pulse Width		2.85		78.75	ms
t_{DV}	Data Valid from $\overline{CE}$				1	ns
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2			µs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50			ns

Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING WAVEFORMS


ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
DATA
DATA IN STABLE
DATA OUT VALID
t_{DS}
t_{DH}
t_{DV}
t_{AH}
V_{CC}
6 V
5 V
t_{VCS}
t_{DFP}
$\overline{OE}$ / V_{PP}
12.5 V
t_{PRT}
t_{OES}
t_{OEH}
t_{VR}
$\overline{CE}$
t_{PW}
t_{OPW}
S - 7581

Notes: 1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING PRESTO

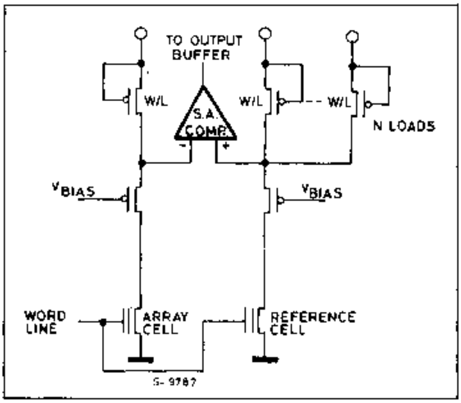
M27512 includes several design innovations to obtain a very efficient programming:

- during programming the word line voltage is bootstrapped over the V_{PP} voltage by about 2V
- the bit line voltage is regulated at the optimum value for fast write.

This allows a reduction of about one order of magnitude in the programming time. The programming is also independent of the V_{PP} voltage (from about 10V to 14V). The V_{CC} voltage (6V during the Algorithm) influences the programming speed since the cell drain voltage regulation uses V_{CC} as a reference.

The sensing scheme is also innovative in SGS-THOMSON M27512. The conventional sensing compares the addressed cell within the memory array with a reference cell (usually one reference cell for each word line) as shown in figure 1.

Figure 1. Conventional Sensing Schematic



If the addressed cell is erased its current is the same as the reference cell's current and the imbalance at the inputs of the comparator (higher voltage on right side = 1) is obtained by connecting lower impedence load on the right side than on the left.

If the addressed cell is written (no current) the left input to the comparator will have a higher voltage than the right side (0 state).

The above approach has proven to be efficient and reliable but still shows a drawback that is the dependance of the V_{CC} operating range (at high V_{CC}) on the threshold shift of the written cell. This can be easily understood by looking at the cell transcharacteristics diagram: together with the characteristics of the erased and the written cell in the memory array the "virtual" reference cell current can be drawn.

The "virtual" reference cell current is the current of the reference cell divided by the ratio between the impedence of the left side loads and the impedence of the right side loads (usually the ratio ranges from 2 to 5).

The figure 2 illustrates very well the dependance of V_{CC} (voltage on the addressed word line) on the threshold shift of the cell: the sensing of a written cell will not be correct where the "virtual" reference cell characteristic crosses and stays below the written cell characteristic (V_{CC} max).

The dependance of V_{CC} max on the threshold shift of a written cell can be illustrated as in figura 3, where the different lines are for different ratios between the impedance of the loads.

Figure 2 - Current relationship of reference and array cells (Conventional Technique)

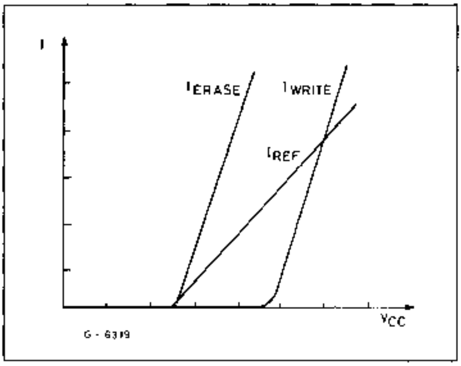
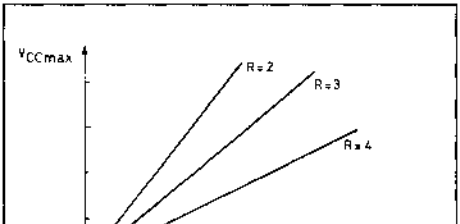


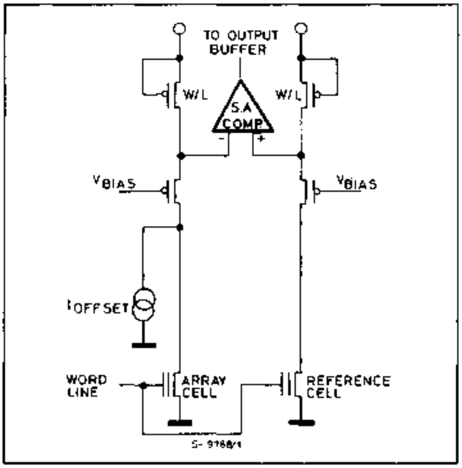
Figure 3 - Dependance of V_{CC} max on threshold shift (R = Loads impedance ratios) (conventional techniques)



M27512 DESIGN INNOVATIONS FOR AN EFFICIENT PROGRAMMING PRESTO (Continued)

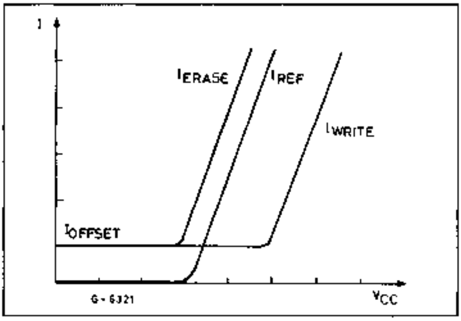
As a conclusion at least a minimum threshold shift of 2V to 3V must be required to the programmed cell to guarantee a wide V_{CC} operation range and reliability.
An innovative approach for the sensing was implemented into the M27512 to remove the above described drawback. The sensing scheme is illustrated in figure 4: the impedance of the loads is the same on both sides; on the left side an offset current is added to the addressed cell's current - (patent pending).

Figure 4 - M27512 sensing schematic



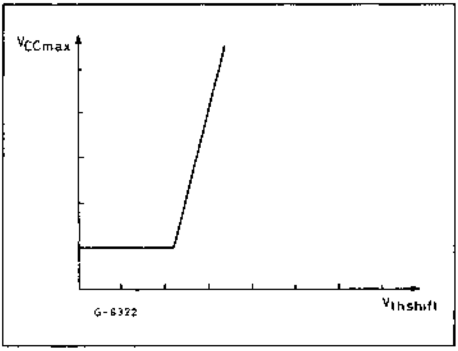
The improvement is easily pointed out in the diagram of the cell transcharacteristics (figure 5) the difference in slope between the written cell and the reference cell are drastically reduced.

Figure 5 - Current relemention ship of reference and array cells (New Technique)



The final result is that a threshold shift of about 1V for a written cell is enough to allow a proper sensing in a very wide V_{CC} operating range (figure 6).

Figure 6 - Dependance of V_{CC} max on threshold Shift (M27512)



For better process margin and producibility the offset current is not fixed but tracks the matrix cell current. The improvement of both the programming speed and the sensing efficiency will reduce the typical programming time per byte to below 200 μsec.
In order to take full advantage of this the original PRESTO programming algorithm was developped as illustrated in previous paragraph.

The similarity with the Fast Programming Algorithm is evident but several main differences exist:

- 500 μsec elementary pulses
- no overprogram pulses are applied after correct verification of a byte
- the existence of a sufficient margin for the written cells is guaranteed by making the program verify in a special test mode called MARGIN MODE*...

Reading a cell in MARGIN MODE requires to the written cell a threshold shift of about 2V: 1V margin above the threshold shift required for a correct operation with wide V_{CC} range in normal operating modes. The circuit arrangement that allows to guarantee the margin is illustrated in figure 7.
The result in the transcharacteristic plane helps to understand the MARGIN MODE feature (figure 8).
The threshold shift margin has been carefully tuned in order to guarantee that the V_{CC} operating range and the access time performance would not be reduced by a cell marginally written; taking into account the temperature range, noise conditions, and data retention (intrinsic charge loss).
The MARGIN MODE is set before starting the programming algorithm and reset after the completion.

Figure 7 - M27512 Sensing schematic with activated margin mode

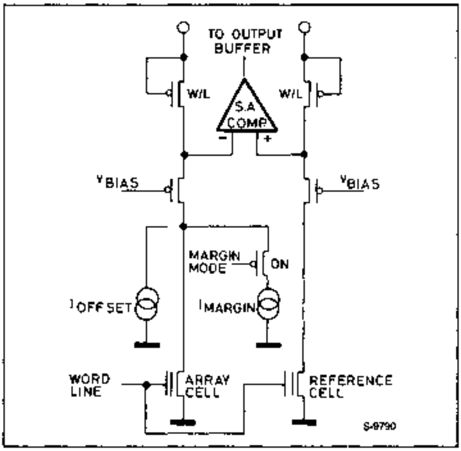
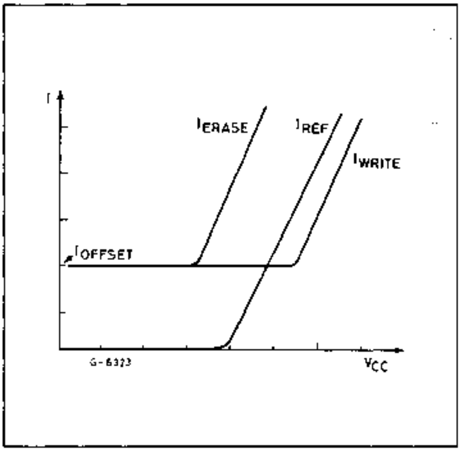

TO OUTPUT BUFFER
W/L
S.A COMP
W/L
-
+
VBIAS
VBIAS
MARGIN MODE
ON
IOFFSET
IMARGIN
WORD LINE
ARRAY CELL
REFERENCE CELL
S-9790

Figure 8 - Current relationship of reference and array cells with margin mode activated



CONCLUSION

M27512 has succesfully achieved the goal of drastically reducing the programming time by:

- improving the programming efficiency
- implementing an improved sensing scheme
- guaranteing by an innovative hardware approach an adequate margin for reliability

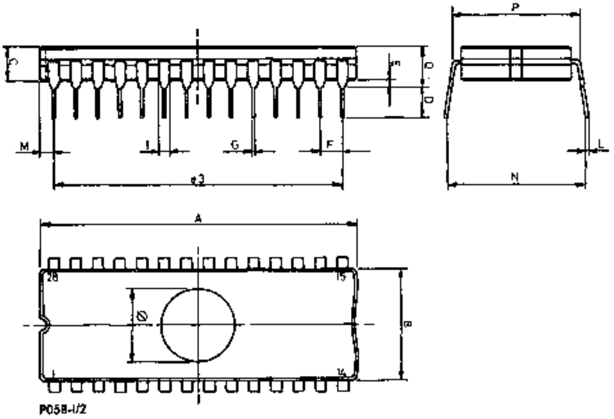
The goal has been achieved without requiring any additional scaling to the well proven NMOS-E3 technology: further improvements can be foreseen when combining the new scaled down technologies (CMOS-E4) with the above circuit techniques. Extensive characterization and life tests have demonstrated the efficiency and the reliability of the solutions adopted.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27512-2F1	200 ns	5V ± 5%	0 to +70°C	DIP-28
M27512F1	250 ns	5V ± 5%	0 to +70°C	DIP-28
M27512-3F1	300 ns	5V ± 5%	0 to +70°C	DIP-28
M27512-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-28
M27512-30F1	300 ns	5V ± 10%	0 to +70°C	DIP-28
M27512F6	250 ns	5V ± 5%	– 40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	8.64		9.14	0.340		0.360

EPROM DEVICES

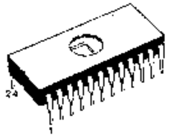
CMOS UV EPROM

SGS-THOMSON
MICROELECTRONICS

ETC2716

16K BIT (2K×8) CMOS UV ERASABLE PROM

- CMOS POWER CONSUMPTION
- PERFORMANCE COMPATIBLE TO MARKET STANDARD 8-BIT CMOS MICROP.
- 2048 × 8 ORGANIZZATION
- PIN COMPATIBLE TO 2716
- ACCESS TIME DOWN TO 350 ns
- SINGLE 5V POWER SUPPLY
- STATIC - NO CLOCKS REQUIRED
- TTL COMPATIBLE I/Os DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- OPER. TEMP. : 0 to + 70°C ; −40 to + 85°C (V suffix).



Q
DIP-24
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

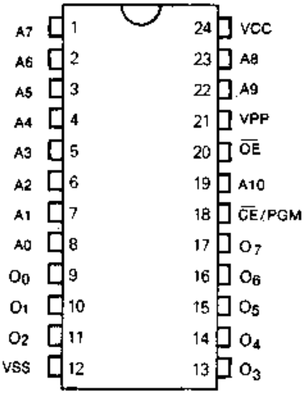
The ETC 2716 is a high speed 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The ETC 2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P² CMOS silicon gate technology.

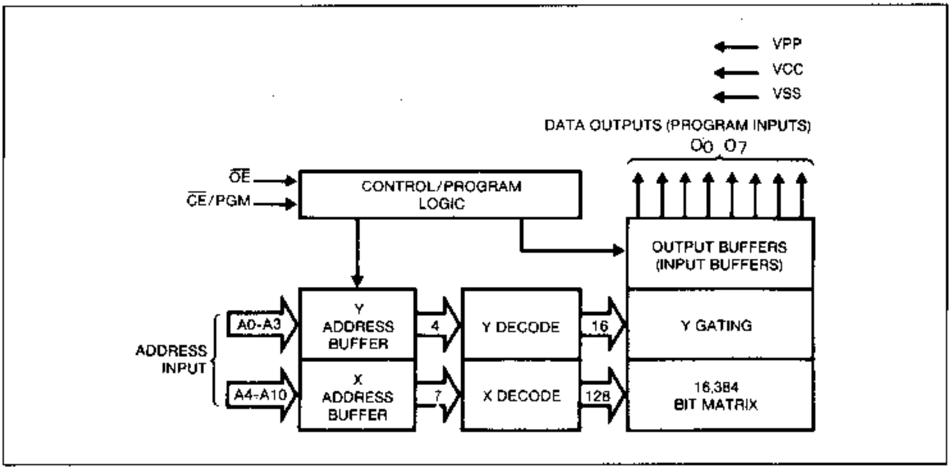
PIN NAMES

A0—A10	ADDRESS INPUTS
O_0—O_7	DATA OUTPUTS
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
V_{PP}	READ 5V, PROGRAM 25V
V_{CC}	5V
V_{SS}	GROUND

PIN CONNECTIONS



BLOCK DIAGRAM


VPP
VCC
VSS
DATA OUTPUTS (PROGRAM INPUTS)
O0 O7
OE
CE/PGM
CONTROL/PROGRAM LOGIC
OUTPUT BUFFERS (INPUT BUFFERS)
ADDRESS INPUT
A0-A3
Y ADDRESS BUFFER
4
Y DECODE
16
Y GATING
A4-A10
X ADDRESS BUFFER
7
X DECODE
128
16,384 BIT MATRIX

PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER				
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	V_{PP} 21	V_{CC} 24	OUTPUTS 9-11, 13-17
Read	V_{IL}	V_{IL}	5	5	D_{OUT}
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias "V" range	– 10 to + 80 – 50 to + 95	°C °C
T_{stg}	Storage Temperature	– 65 to + 125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to – 0.3	V
V_{in}	Input Voltages with Respect to V_{SS} except V_{PP}	6V to – 0.3	V
	Output Voltages with Respects to V_{SS}	V_{CC} + 0.3V to V_{SS} – 0.3V	
P_D	Power Dissipation	1.0	W
	Lead Temperature (Soldering 10 seconds)	+ 300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$ (2), $V_{SS} = 0V$, (Unless otherwise specified)(6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{LI}	Input Current	$V_{IN} = V_{CC}$ or GND	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$, $\overline{CE}$/PGM $= V_{IH}$	—	—	10	μA
V_{IL}	Input Low Voltage		-0.1	—	0.8	V
V_{IH}(4)	Input High Voltage		2.0	—	$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ μA	2.4	—	—	V
V_{OL2}	Output Low Voltage	$I_{OL} = 0$ μA	—	—	0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 0$ μA	$V_{CC} - 0.1$	—	—	V
I_{PP1}	V_{PP} Supply Current	$V_{PP} = 5.25V$	—	—	10	μA
I_{CC1}	V_{CC} Supply Current Active (TTL Levels)	$\overline{CE}$/PGM, $\overline{OE} = V_{IL}$ Address $= V_{IH}$ or V_{IL} Frequency 1MHz, I/O = 0mA	—	2	10	mA
I_{CC2}	V_{CC} Supply Current Active (CMOS Levels)	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$ (Note 5) Addresses = GND or V_{CC} Frequency 1MHz, I/O = 0mA	—	1	5	mA
I_{CCSB1}	V_{CC} Supply Current Standby	$\overline{CE}$/PGM $= V_{IH}$	—	0,1	1	mA
I_{CCSB2}	V_{CC} Supply Current Standby	$\overline{CE}$/PGM $= V_{CC}$	—	0,01	0,1	mA

AC CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, $V_{SS} = 0V$; Unless otherwise specified)(6).

Symbol		Parameter	Test Conditions	ETC2716-1		ETC2716 (-V)		Unit
Alternate	Standard			Min.	Max.	Min.	Max.	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$	—	350	—	450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM $= V_{IL}$	—	120	—	120	ns
t_{DF}(5)	TGHQZ	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}$/PGM $= V_{IL}$	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM $= \overline{OE} = V_{IL}$	0	—	0	—	ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE} = V_{IL}$	0	100	0	100	ns

CAPACITANCE(3) $T_A = 25°C$, f = 1 MHz

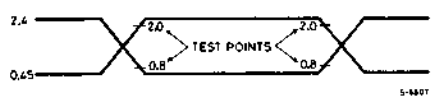
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_I	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_O	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes 1. Typical conditions are for operation at: $T_A = 25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$.
2. V_{PP} may be connected to V_{CC} except during program.
3. Capacitance is guaranteed by periodic testing. $T_A = 25°C$, f = 1 MHz. .
4. The inputs (Address, OE, CE) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V.
5. T_{DF} is specified for OE or CE which ever occurs first. This parameter is only sampled and not 100% tested.
6. $T_A = -40°C$ to $+85°C$ for "V" range

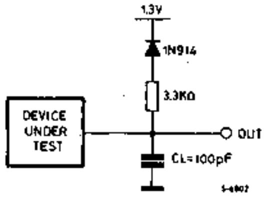
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

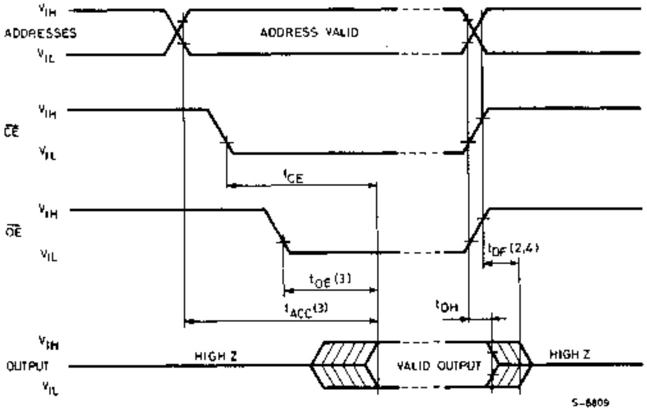

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE
V_IH
OE
V_IL
t_DF (2,4)
t_OE (3)
t_ACC (3)
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The ETC2716 has 3 modes of operation in the normal system environment. These are shown in Table 1.

TABLE I. OPERATING MODES (V_{CC} = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{\text{CE}}$/PGM 18	$\overline{\text{OE}}$ 20	Outputs 9-11, 13-17
Read	V_{IL}	V_{IL}	D_{OUT}
Deselect	Don't Care	V_{IH}	Hi-Z
Standby	V_{IH}	Don't Care	Hi-Z

READ MODE

The ETC2716 read operation requires that $\overline{\text{OE}}$ = V_{IL}, $\overline{\text{CE}}$/PGM = V_{IL} and that addresses A_0-A_{10} have been stabilized. Valid data will appear on the output pins after t_{ACC} t_{OE} or t_{CE} times (see Switching Time Wafeforms) depending on which is limiting.

DESELECT MODE

The ETC2716 is deselected by making $\overline{\text{OE}}$ = V_{IH}. This mode is independent of $\overline{\text{CE}}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{\text{OE}}$ = V_{IH}. This allows OR-tying 2 or more ETC2716 for memory expansion.

STANDBY MODE (POWER DOWN)

The ETC2716 may be powered down to the standby mode by making $\overline{\text{CE}}$/PGM = V_{IH}. This is independent of $\overline{\text{OE}}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 0.4% of the normal operating power. V_{CC} must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The ETC2716 is shipped from SGS-THOMSON completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

PROGRAM MODE

The ETC2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With V_{PP} = 25V, V_{CC} = 5V, $\overline{\text{OE}}$ = V_{IH} and $\overline{\text{CE}}$/PGM = V_{IL}, an address is selected and the desired data word is applied to the output pins. (V_{IL} = "0" and V_{IH} = "1" for both address and data). After the address and data signals are stable the program pin is pulsed from V_{IL} to V_{IH} with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (V_{IH} or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ETC2716 may be programmed in parallel with the same data in this mode.

PROGRAM VERIFY MODE

The programming of the ETC2716 is verified in the program verify mode which has V_{PP} at V_{CC} (see Table II). After programming an address, that same address cannot be immediately verified without an address change (dummy read).

PROGRAM INHIBIT MODE

The program inhibit mode allows programming several ETC2716 simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the ETC2716 may be paralleled. Pulsing the program pin (from V_{IL} to V_{IH}) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{\text{OE}}$ = V_{IH} will put its outputs in the HI-Z state.

TABLE II. PROGRAMMING MODES (V_{CC} = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{\text{CE}}$/PGM 18	$\overline{\text{OE}}$ 20	V_{PP} 21	OUTPUTS 9-11, 13-17
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	25	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	25(5)	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	25	Hi-Z

ERASING

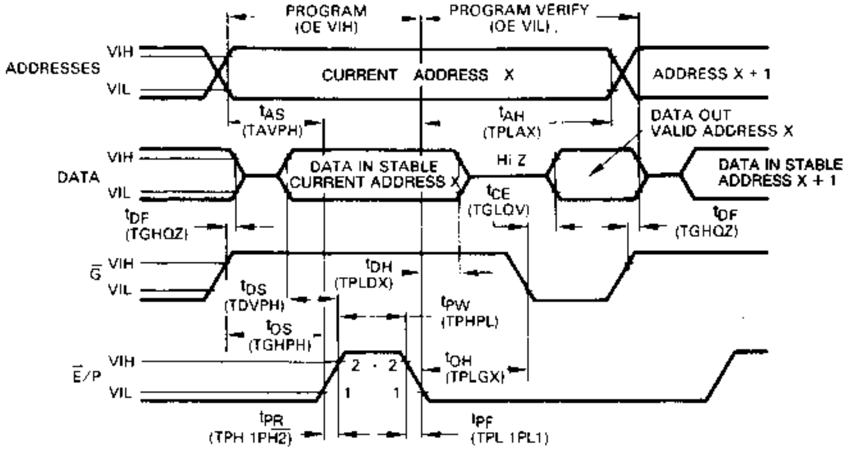
The ETC2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ETC2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 µW/cm² power rating is used. The ETC2716 to be erased should be place 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

TIMING DIAGRAM

PROGRAM MODE


PROGRAM (OE VIH)
PROGRAM VERIFY (OE VIL)
ADDRESSES
VIH
VIL
CURRENT ADDRESS X
ADDRESS X + 1
tAS (TAVPH)
tAH (TPLAX)
DATA OUT VALID ADDRESS X
DATA
DATA IN STABLE CURRENT ADDRESS X
Hi Z
DATA IN STABLE ADDRESS X + 1
tDF (TGHQZ)
tCE (TGLQV)
tDF (TGHQZ)
G̅
tDH (TPLDX)
tDS (TDVPH)
tPW (TPHPL)
tOS (TGHPH)
E̅/P
2 · 2
1 1
tOH (TPLGX)
tPR (TPH 1PH2)
tPF (TPL 1PL1)

Note: Symbols in parentheses are proposed JEDEC standard

PROGRAM OPERATIONS$^{(1,2)}$

DC AND OPERATIVE CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Values			Unit
		Min.	Typ.	Max.	
I_{LI}	Input Leakage Current (Note 3)	—	—	10	μA
V_{IL}	Input Low Level	−0.1	—	0.8	V
V_{IH}	Input High Level (Note 7)	2.2	—	$V_{CC}+1$	V
I_{CC}	V_{CC} Power Supply Current	—	—	10	mA
I_{PP1}	V_{PP} Supply Current (Note 4)	—	—	10	μA
I_{PP2}	V_{PP} Supply Current During Programming Pulse (Note 5)	—	—	30	mA

AC CHARACTERISTICS ($T_A = 25°C \pm 5°C$) ($V_{CC} = 5V \pm 5\%$, $V_{PP} = 5V \pm 1V$) (Note 6)

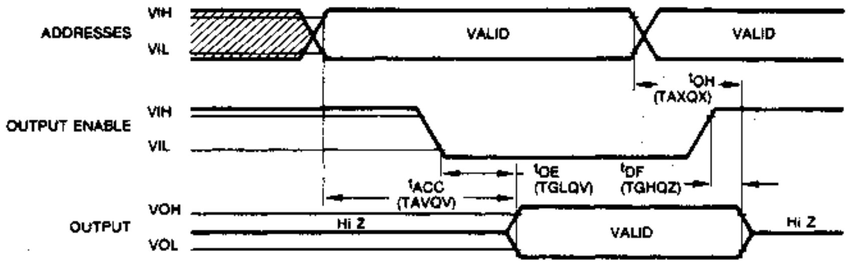
Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	2	—	—	μs
t_{OS}	$\overline{OE}$ Setup Time	2	—	—	μs
t_{DS}	Data Setup Time	2	—	—	μs
t_{AH}	Address Hold Time	2	—	—	μs
t_{OH}	$\overline{OE}$ Hold Time	2	—	—	μs
t_{DH}	Data Hold Time	2	—	—	μs
t_{DF}	Output Disable to Output Three state Delay	0	—	100	μs
t_{OE}	Output Enable to Output Delay	—	—	120	ns
t_{PW}	Program Pulse Width	45	50	55	ms
t_{PR}	Program Pulse Rise Time	5	—	—	ns
t_{PF}	Program Pulse Fall Time	5	—	—	ns

Notes 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. To prevent damage to the device it must not be inserted into a board with power applied.

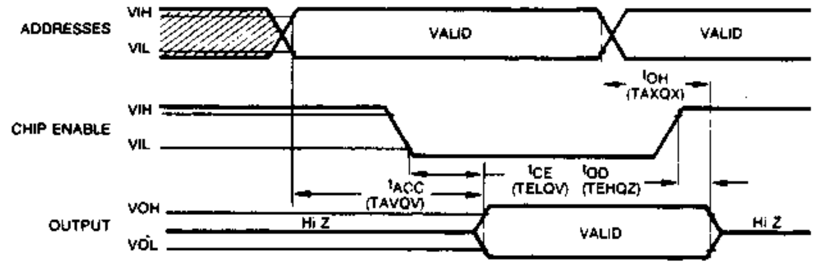
2. Care must be taken to prevent overshoot of the V_{PP} supply when switching to +26V max.
3. $0V \leqslant V_{IN} \leqslant 5.25V$.
4. $CE/PGM = V_{IL}$, $V_{PP} = V_{CC}$.
5. $V_{PP} = 26V$.
6. Transition times ⩽ 20 ns unless otherwise noted.
7. The inputs (Address, OE, CE) may go above V_{PP} by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to $V_{PP} + 0.3V$ to $V_{SS} - 0.3V$.

SWITCHING TIME WAVEFORMS

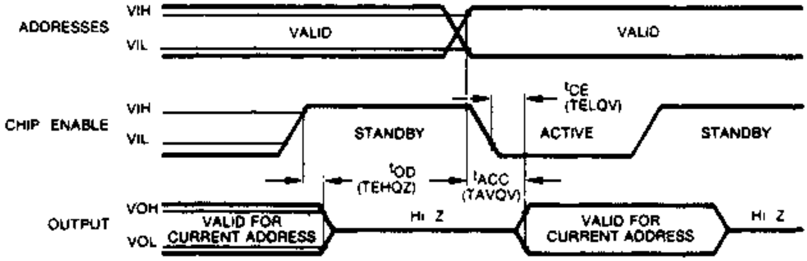
Read Cycle ($\overline{CE}$/PGM = VIL)


ADDRESSES
VIH
VIL
VALID
VALID
t_{OH}
(TAXQX)
OUTPUT ENABLE
VIH
VIL
t_{OE}
(TGLQV)
t_{DF}
(TGHQZ)
t_{ACC}
(TAVQV)
OUTPUT
VOH
VOL
Hi Z
VALID
Hi Z

Read Cycle ($\overline{OE}$ = VIL)


ADDRESSES
VIH
VIL
VALID
VALID
t_{OH}
(TAXQX)
CHIP ENABLE
VIH
VIL
t_{CE}
(TELQV)
t_{OD}
(TEHQZ)
t_{ACC}
(TAVQV)
OUTPUT
VOH
VOL
Hi Z
VALID
Hi Z

Standby Power-Down Mode ($\overline{OE}$ = VIL)


ADDRESSES
VIH
VIL
VALID
VALID
t_{CE}
(TELQV)
CHIP ENABLE
VIH
VIL
STANDBY
ACTIVE
STANDBY
t_{OD}
(TEHQZ)
t_{ACC}
(TAVQV)
OUTPUT
VOH
VOL
VALID FOR CURRENT ADDRESS
Hi Z
VALID FOR CURRENT ADDRESS
Hi Z

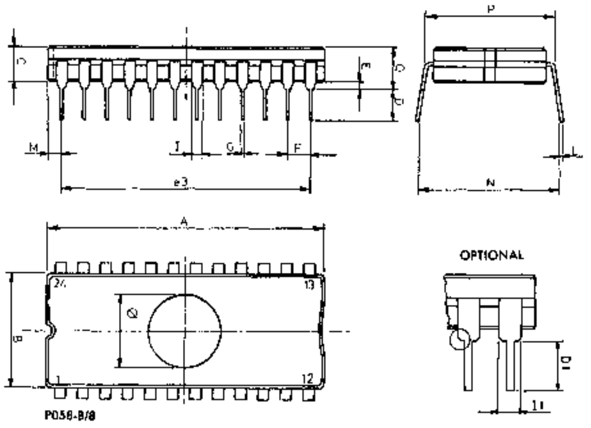
Symbols in parentheses are proposed JEDEC standard

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ETC2716Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2716Q-1	350 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2716Q-V	450 ns	5V ± 5%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1(1)	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1(1)	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

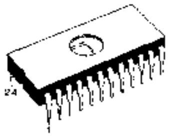
Note: 1. Optional see drawing

SGS-THOMSON
MICROELECTRONICS

ETC2732

32K BIT (4K × 8) CMOS UV ERASABLE PROM

- CMOS POWER CONSUMPTION: 26.25 mW MAX ACTIVE POWER, 0.53 mW MAX STANDBY POWER
- 4096 × 8 ORGANIZZATION
- PIN COMPATIBLE TO M/ET2716, ETC2716, M2732A,
- ACCESS TIME DOWN TO 350 ns
- SINGLE 5V POWER SUPPLY
- STATIC - NO CLOCKS REQUIRED
- TTL COMPATIBLE I/Os DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT WITH OR-TIE CAPABILITY
- OPER. TEMP. : 0 to +70°C ; −40 to +85°C (V suffix).



Q
DIP-24
(Ceramic Bull's Eye)

(Ordering information at the end of the datasheet)

DESCRIPTION

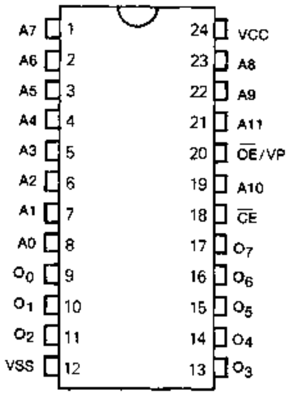
The ETC2732 is a high speed 32K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The ETC2732 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure. This EPROM is fabricated with the reliable, high volume, time proven, P² CMOS silicon gate technology.

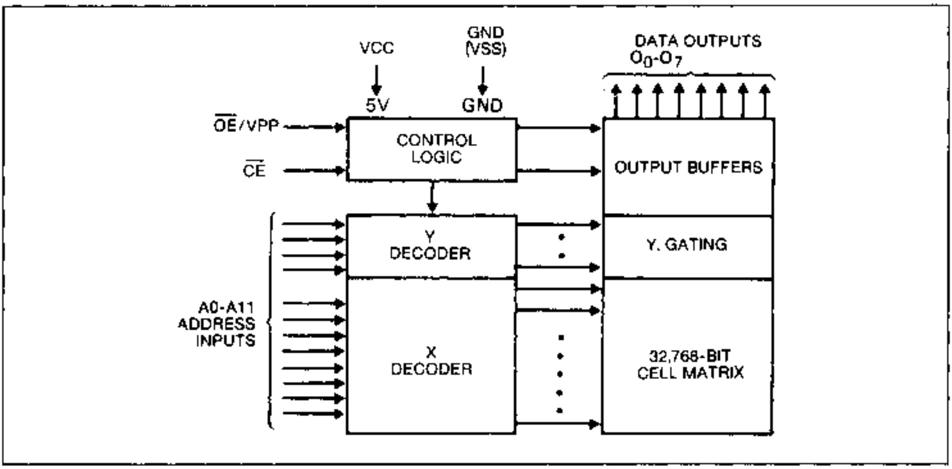
PIN NAMES

A0—A11	ADDRESS INPUTS
O_0—O_7	DATA OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{PP}	READ RV, PROGRAM 25V
V_{CC}	5V
V_{SS}	GROUND

PIN CONNECTIONS



BLOCK DIAGRAM


VCC
GND (VSS)
DATA OUTPUTS
O0-O7
5V
GND
OE/VPP
CE
CONTROL LOGIC
OUTPUT BUFFERS
Y DECODER
Y. GATING
A0-A11
ADDRESS
INPUTS
X DECODER
32,768-BIT CELL MATRIX

PIN CONNECTION DURING READ OR PROGRAM

MODE	PIN NAME/NUMBER			
	$\overline{\text{CE}}$ 18	$\overline{\text{OE}}/V_{PP}$ 20	V_{CC} 24	OUTPUTS 9—11, 13-17
READ	V_{IL}	V_{IL}	5V	D_{OUT}
STANDBY	V_{IH}	Don't Care	5V	Hi-Z
PROGRAM	V_{IL}	25V	5V	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	5V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	25V	5V	Hi-Z

* Symbol in parentheses are proposed JEDEC standard.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{amb}	Temperature Under Bias "V" range	– 10 to + 80 – 50 to + 95	°C °C
T_{stg}	Storage Temperature	– 65 to + 125	°C
V_{PP}	V_{PP} Supply Voltage with Respect to V_{SS}	26.5V to – 0.3	V
V_{in}	Input Voltages with Respect to V_{SS} except V_{PP}	6V to – 0.3	V
	Output Voltages with Respects to V_{SS}	V_{CC} + 0.3V to V_{SS} – 0.3V	
P_D	Power Dissipation	1.0	W
	Lead Temperature (Soldering 10 seconds)	300	°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are, not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

READ OPERATION

DC CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, (Unless otherwise specified)(6)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
I_{LI}	Input Current	$V_{IN} = V_{CC}$ or GND	—	—	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}, $\overline{CE} = V_{IH}$	—	—	10	μA
V_{IL}	Input Low Voltage		−0.1	—	0.8	V
V_{IH}(3)	Input High Voltage		2.0	—	$V_{CC}+1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ μA	2.4	—	—	V
V_{OL2}	Output Low Voltage	$I_{OL} = 0$μA	—	—	0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 0$μA	$V_{CC} - 0.1$	—	—	V
I_{CC1}	V_{CC} Supply Current Active (TTL Levels)	$\overline{CE} = \overline{OE} = V_{IL}$ Input $= V_{IH}$ or V_{IL} Frequency 1MHz, I/O = 0mA	—	2	10	mA
I_{CC2}	V_{CC} Supply Current Active (CMOS Levels)	$\overline{CE} = \overline{OE} = V_{IL}$ (Note 4) Inputs = GND or V_{CC} Frequency 1MHz, I/O = 0mA	—	1	5	mA
I_{CCSB1}	V_{CC} Supply Current Standby	$\overline{CE} = V_{IH}$	—	0.1	1	mA
I_{CCSB2}	V_{CC} Supply Current Standby	$\overline{CE} = V_{CC}$	—	0.01	0.1	mA

AC CHARACTERISTICS $T_A = 0°C$ to C, $V_{CC} = 5V \pm 5\%$ $V_{SS} = 0V$; Unless otherwise specified)(6).

Symbol	Parameter	Test Conditions	ETC2732-3		ETC2732 (-V)		Unit
			Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay	CE/PGM = OE = V_{IL}	—	350	—	450	ns
t_{CE}	CE to Output Delay	$\overline{OE} = V_{IL}$	—	350	—	450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = V_{IL}	—	150	—	150	ns
t_{DF}(4,5)	$\overline{OE}$ or $\overline{CE}$ High to Output Hi-Z	$\overline{CE}$/PGM = V_{IL}	0	130	0	130	ns
t_{OH}	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE} = V_{IL}$	0	—	0	—	ns

CAPACITANCE ($T_A = +25°C$, f = 1 MHz) (Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$		4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		—	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

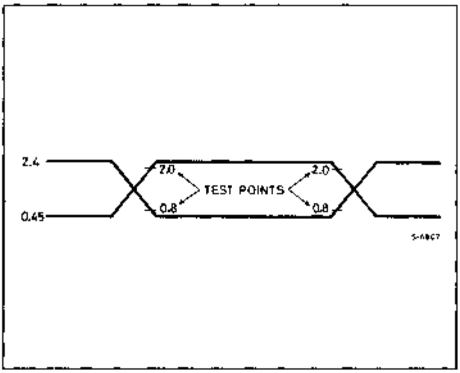
Notes 1. Typical conditions are for operation at: TA = 25°C, VCC = VPP = VCC, and VSS = OV.

2. Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.
3. The Inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3 V.
4. The t_{DF} compare level is determined as follows:
   High to Hi-Z, the measured V_{OH1} (DC) — 0.10V
   Low to Hi-Z, the measured V_{OH1} (DC) + 0.10V
5. T_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ which ever occurs first. This parameter is only sampled, not 100% tested.
6. $T_A = -40°C$ to $+85°C$ for "V" range

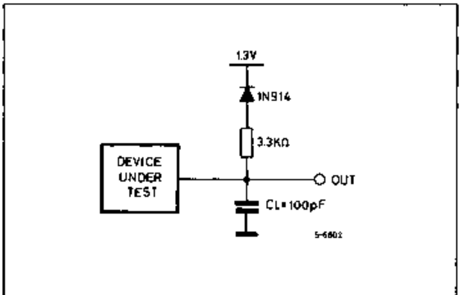
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

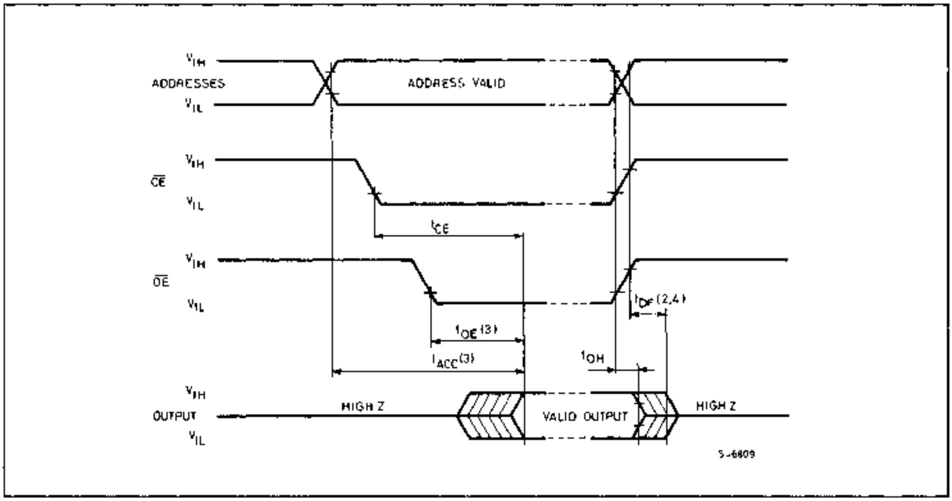

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
5-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} (2,4)
t_{OE} (3)
t_{ACC} (3)
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z
5-6809

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The five modes of operation of the ETC 2732 are listed in the Operating Modes table. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}$/Vpp during programming. In the program mode the $\overline{OE}$/Vpp input is pulsed from a TTL level to 25V.

READ MODE

The ETC2732 has two control functions, both of wich must be logically active in order to obtain data at the ouputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ETC2732 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53mW. The ETC 2732 is placed in the standby mode, by applying a TTL high signal to the $\overline{CE}$ input when in standby mode the outputs are in a high impedance state, independant of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because EPROMS are usually used in larger memory arrays, we have provided a 2-line control function that accomodates this use of multiple memory connection. The 2-line control function allows for.

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the ETC2732.

Initially, and after each erasure, all bits of the ETC 2732 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The ETC2732 is in the programming mode when the $\overline{OE}$/Vpp input is at 25V. It is required that a 0.1 µF capacitor be placed across $\overline{OE}$/Vpp, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms active low TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time-either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The ETC 2732 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple ETC 2732s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled ETC 2732s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled.

OPERATING MODES

PIN / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9—11, 13-17)
READ	V_{IL}	V_{IL}	5	D_{OUT}
STANDBY	V_{IH}	Don't Care	5	Hi-Z
PROGRAM	V_{IL}	V_{PP}	5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	5	Hi-Z

PROGRAM INHIBIT

Programming multiple ETC2732s in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$, all like inputs (including $\overline{\text{OE}}$) of the parallel ETC2732s may be common. A TTL level program pulse applied to an ETC2732s $\overline{\text{CE}}$ input with $\overline{\text{OE}}$/Vpp at 25 V will program that ETC2732. A high level $\overline{\text{CE}}$ input inhibits the other ETC2732s from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{\text{OE}}$/Vpp $\overline{\text{CE}}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{\text{CE}}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the ETC2732 are such that erasure begins to occur when exposed to light with wavelenghts shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelenghts in the 3000 A - 4000 A range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical ETC 2732 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the ETC2732 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the ETC2732 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the ETC 2732 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm². The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm² power rating. The ETC2732 should be place within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

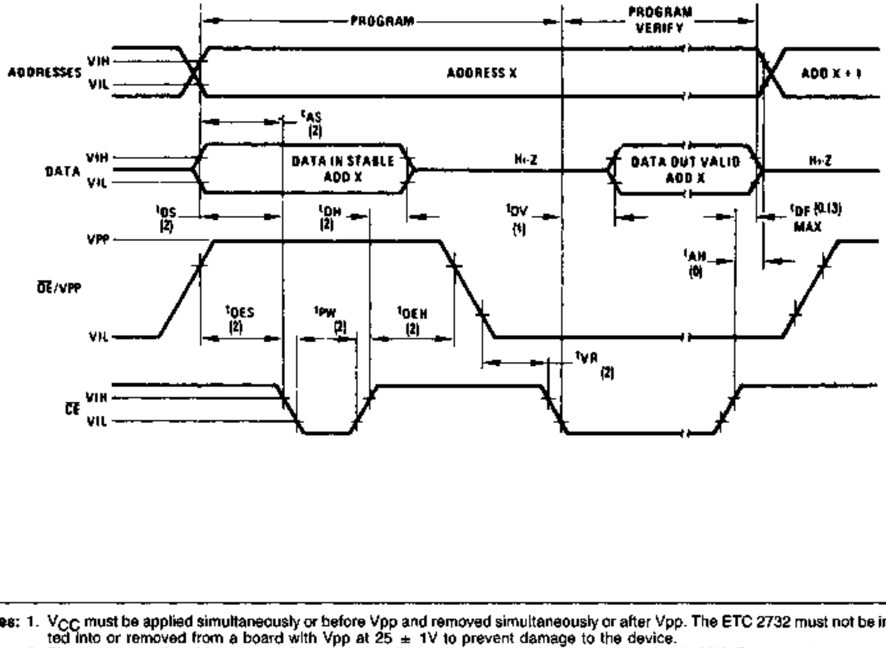
SYSTEM CONSIDERATION

The power swhitching characterics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer - the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltgage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1μF Ceramic capacitor be used an every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7μF bulk electolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

PROGRAMMING WAVEFORMS

Note: All times shown in parentheses are minimum and in μs unless otherwise specified.
The input timing reference is 0.8V for a V_{IL} and 2V for a V_{IH}.

TIMING DIAGRAM


PROGRAM
PROGRAM VERIFY
ADDRESSES
VIH
VIL
ADDRESS X
ADD X + 1
tAS (2)
DATA
VIH
VIL
DATA IN STABLE ADD X
Hi-Z
DATA OUT VALID ADD X
Hi-Z
tDS (2)
tDH (2)
tDV (1)
tDF (0.13) MAX
VPP
$\overline{OE}$/VPP
VIL
tAH (0)
tOES (2)
tPW (2)
tOEH (2)
tVR (2)
$\overline{CE}$
VIH
VIL

Notes: 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.
2. The maximum allowable voltage with may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

PROGRAMMING OPERATION (1,2)

DC OPERATING CHARACTERISTICS $T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All inputs)	$V_{IN} = V_{CC}$ or GND	—	—	10	µA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA	—	—	0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4	—	—	V
I_{CC}	V_{CC} Supply Current		—	2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1	—	0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0	—	$V_{CC}+1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$	—	—	30	mA

AC CHARACTERISTICS ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, V_{PP} $25V \pm 1V$).

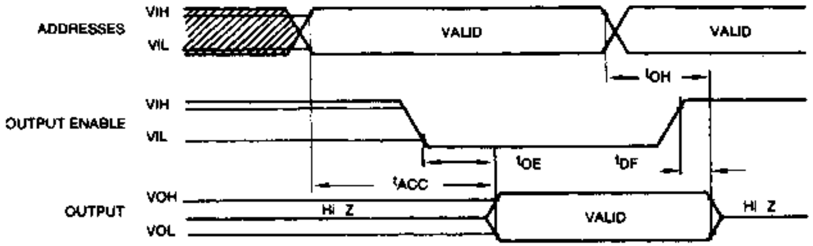
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{AS}	Address Set-Up Time		2	—	—	µs
t_{OES}	$\overline{OE}$ Set-Up Time		2	—	—	µs
t_{DS}	Data Set-Up Time		2	—	—	µs
t_{AH}	Address Hold Time		0	—	—	µs
t_{OEH}	$\overline{OE}$ Hold Time		2	—	—	µs
t_{DH}	Data Hold Time		2	—	—	µs
t_{DF}	Chip Enable to Output Float Delay		0	—	130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$; $\overline{OE} = V_{IL}$	—	—	1	µs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50	—	—	ns
t_{VR}	V_{PP} Recovery Time		2	—	—	µs

Notes 1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The ETC 2732 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.

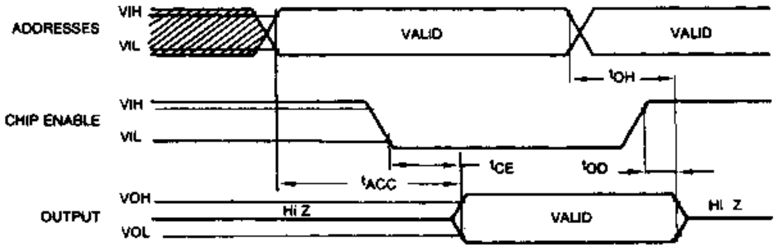
2. The maximum allowable voltage which may be applied to the Vpp pin during programming is 26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 µF capacitor is required across Vpp, Vcc to GND to suppress spurious voltage transients which may damage the device.

SWITCHING TIME WAVEFORMS

Read Cycle ($\overline{CE}$ = VIL)


ADDRESSES
VIH
VIL
VALID
VALID
tOH
OUTPUT ENABLE
VIH
VIL
tOE
tDF
tACC
OUTPUT
VOH
VOL
Hi Z
VALID
Hi Z

Read Cycle ($\overline{OE}$ = VIL)

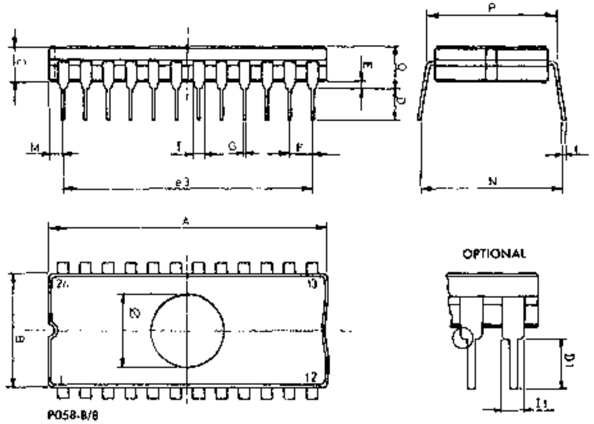

ADDRESSES
VIH
VIL
VALID
VALID
tOH
CHIP ENABLE
VIH
VIL
tCE
tOO
tACC
OUTPUT
VOH
VOL
Hi Z
VALID
Hi Z

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ETC2732Q-3	350 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2732Q	450 ns	5V ± 5%	0 to +70°C	DIP-24
ETC2732Q-45-V	450 ns	5V ± 5%	−40 to +85°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			32.30			1.272
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
D1[1]	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
I1[1]	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
∅	6.86		7.36	0.270		0.290

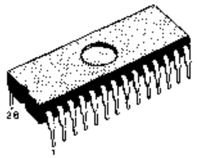
Note: 1. Optional see drawing

SGS-THOMSON
MICROELECTRONICS

TS27C64AQ

64K (8K × 8) CMOS UV ERASABLE PROM

- FAST ACCESS TIME - 150ns, 200ns, 250ns, 300ns
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE
- 28-PIN JEDEC APPROVED PIN-OUT
- LOW POWER CONSUMPTION:
  ACTIVE 30mA MAX.
  STANDBY 1MA MAX.
- PROGRAMMING VOLTAGE: 12.5 V
- HIGH SPEED PROGRAMMING (< 1 minute)
- ELECTRONIC SIGNATURE
- ALSO PROPOSED IN PLASTIC PACKAGES (OTP)



Q
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

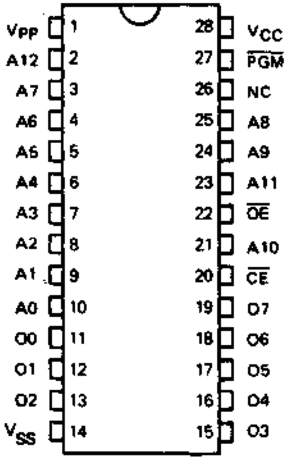
The TS27C64A is a high speed 65,536 bit UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

The TS27C64A is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

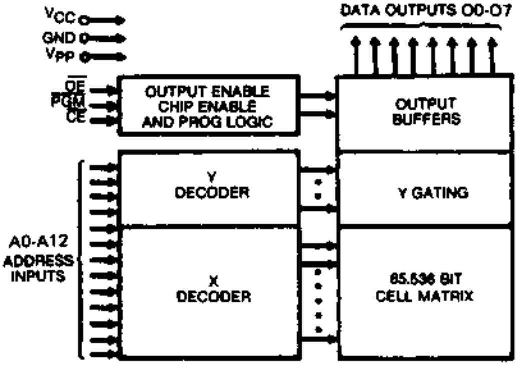
PIN NAMES

A0—A12	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NON CONNECTED

PIN CONNECTIONS


Vpp 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
Vss 14
28 Vcc
27 PGM
26 NC
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE CHIP ENABLE AND PROG LOGIC
DATA OUTPUTS O0-O7
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A12 ADDRESS INPUTS
X DECODER
65.536 BIT CELL MATRIX

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range TS27C64ACQ TS27C64AVQ	T_L to T_H 0 to + 70 – 40 to + 85	°C
T_{stg}	Storage temperature range	– 65 to + 125	°C
V_{PP}(2)	Supply voltage	– 0.6 to + 14	V
V_{in}(2)	Input voltages A9 Except V_{PP}, A9	– 0.6 to + 13.5 – 0.6 to + 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

Notes: 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND

OPERATING MODES

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	Hi-Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	CODE

Notes: 1. X can be either V_{IL} or V_{IH} — 2. $V_H = 12.0V \pm 0.5V$
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 08).

READ OPERATION

DC CHARACTERISTICS ($T_{amb} = T_L$ to T_H, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$; Unless otherwise specified)(5)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(1)	Max.	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}, $\overline{CE} = V_{IH}$			10	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC} - 0.7$		V_{CC}	V
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $I_{OL} = 0$ µA			0.45 0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA $I_{OH} = 0$ µA	2.4 $V_{CC} - 0.1$			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE} = \overline{OE} = V_{IL}$, Inputs $= V_{IH}$ or V_{IL}, f = 5 MHz, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE} = V_{IH}$		0.5	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE} = V_{CC}$		10	100	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{CC} = 5.5V$			100	µA

Note: 1. Typical conditions are for operation at: $T_{amb} = +25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$

AC CHARACTERISTICS(1)($T_{amb} = T_L$ to T_H)(5)

Symbol	Parameter	Test Conditions	27C64A -15		27C64A -20		27C64A -25		27C64A -30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		80		100		120	ns
$t_{DF}^{(2,4)}$	$\overline{OE}$ or $\overline{CE}$ High to output float		0	50	0	50	0	60	0	105	ns
t_{OH}	Output Hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE $T_{amb} = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{out}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}·V_{PP} may be connected to V_{CC} except during program.

2. The t_{DF} compare level is determined as follows:
High to THREE-STATE, the measured $V_{OH}(DC) - 0.1V$
Low to THREE-STATE the measured $V_{OL}(DC) + 0.1V$.

3. Capacitance is guaranteed By periodic testing. $T_{amb} = +25°C$, f = 1MHz.

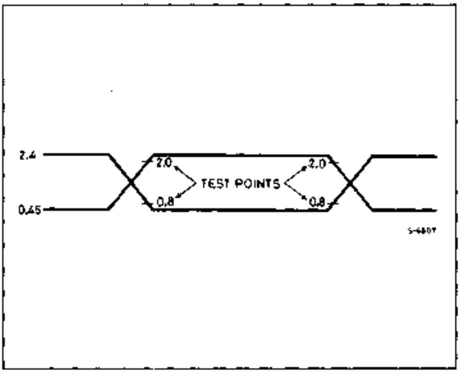
4. T_{DF}, is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100% tested.

5. All parameters are specified at $V_{CC} = 5V \pm 5\%$ for 27C64-15X, 27C64-20X, 27C64-25X and 27C64-30X.

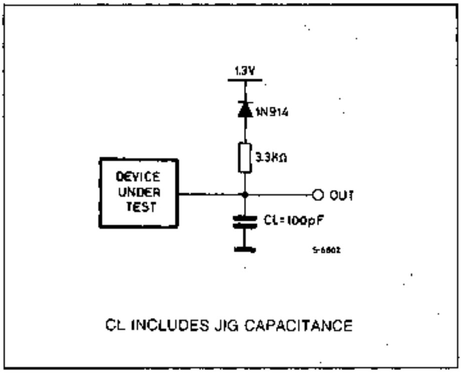
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

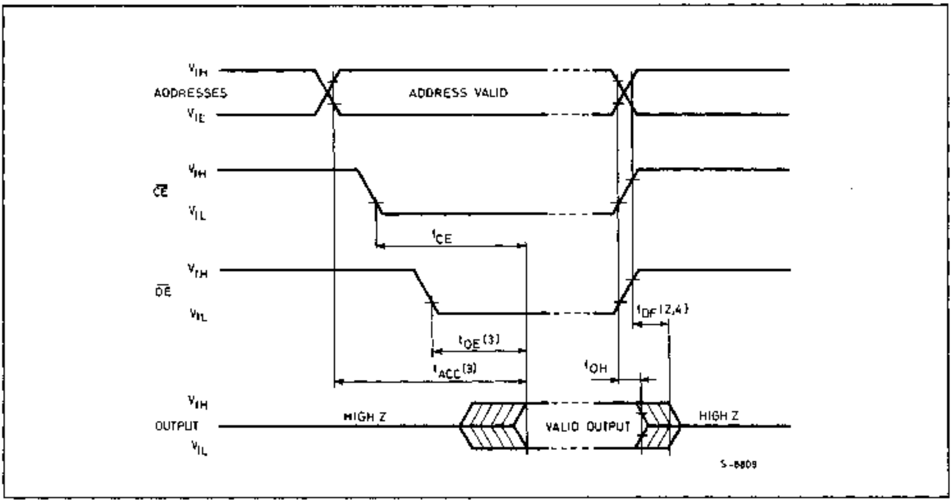

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE
V_IH
OE
V_IL
t_DF (2,4)
t_OE (3)
t_ACC (3)
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

READ MODE

The TS27C64A has two control functions, both of wich must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C64A has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these control lines most eficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING MODES

Caution: Exceeding 14V on pin 1 (V_{PP}) will damage the TS27C64A.

Initially, and after each erasure, all bits of the TS27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C64A is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. It is required that a 0.1 µF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64As.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flow chart rapidly programs TS27C64A using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

PROGRAM INHIBIT

Programming of multiple TS27C64As in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64As from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64As may be common. A TTL low-level pulse applied to a TS27C64A $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5V will program that TS27C64A.

PROGRAM VERIFY

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5 V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will indentify the EPROM manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64A. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the TS27C64A. Two bytes may then be sequenced from the device outputs by toggling address line AO (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electonic signature mode.

ERASING

The TS27C64A is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C64A be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Coverting the window also reduces ICC due to photodiode currents. An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The TS27C64A to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The disance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have ben erroneously suspected when incomplete erasure was the basic problem.

PROGRAMMING OPERATIONS[1]($T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (all inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -400$ μA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS

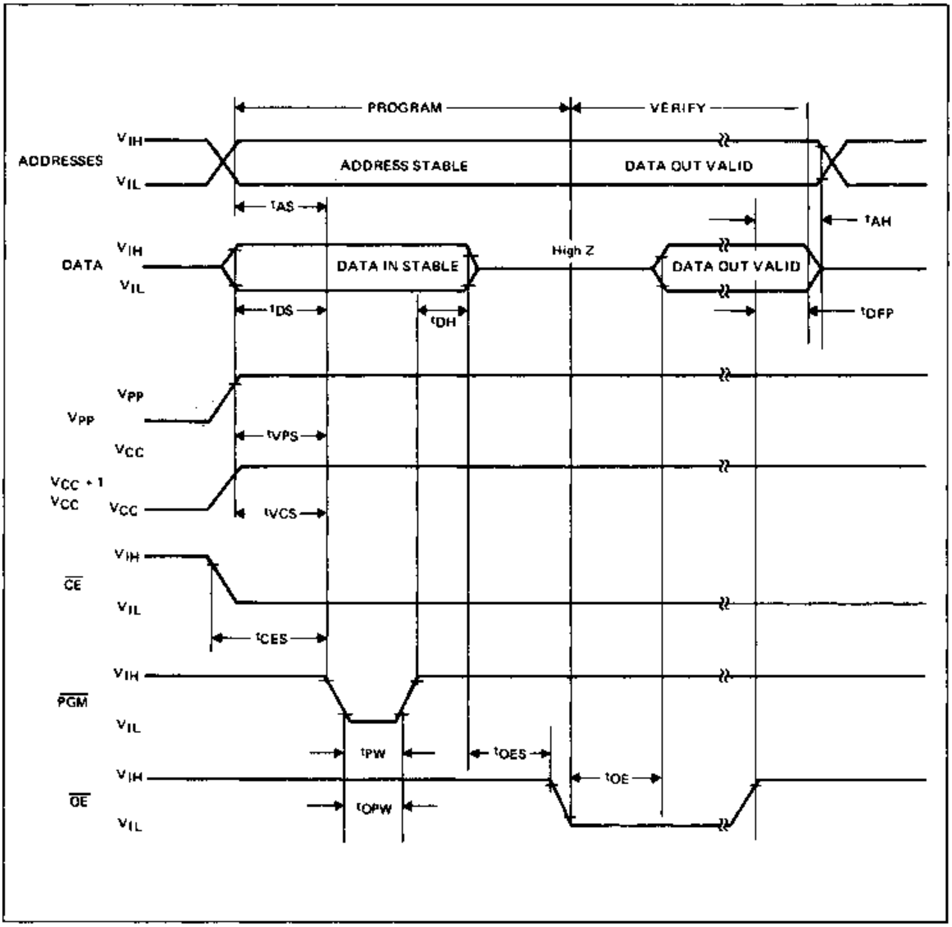
Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set-up Time		2			μs
t_{OES}	$\overline{OE}$ Set-up Time		2			μs
t_{DS}	Data Set-up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			μs
t_{VCS}	V_{CC} set-up time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{CES}	$\overline{CE}$ set-up time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

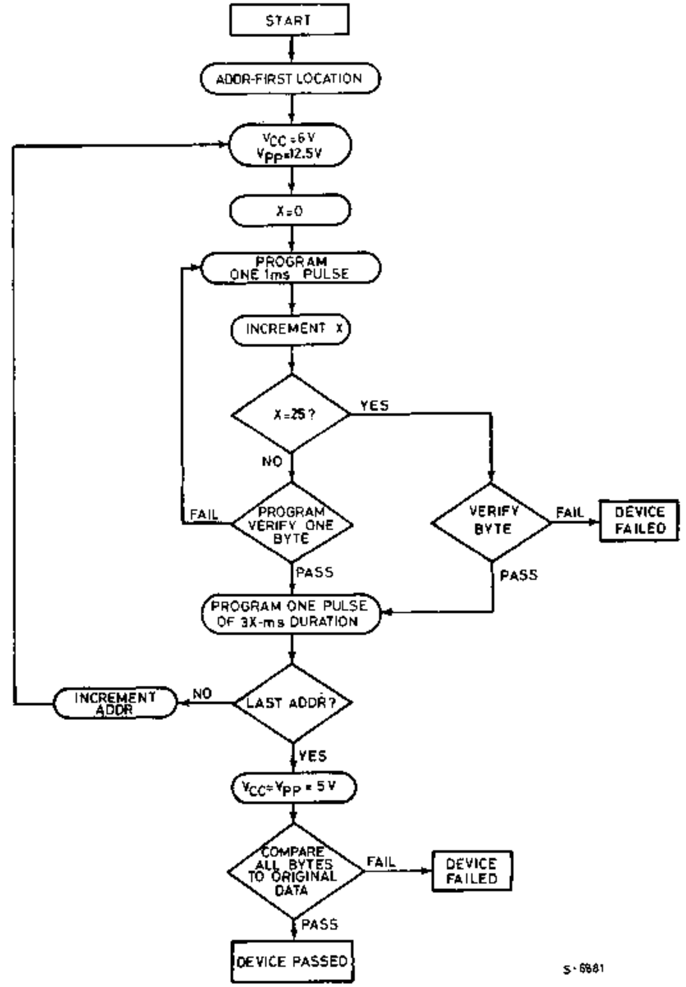
Input rise and fall times (10% to 90%)	≤ 20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Output timing reference level	0.8V and 2.0V

HIGH SPEED PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
DATA OUT VALID
t_{AS}
t_{AH}
DATA
High Z
DATA IN STABLE
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
V_{PP}
V_{CC}
t_{VPS}
$V_{CC}+1$
V_{CC}
V_{CC}
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OES}
$\overline{OE}$
t_{OE}
t_{OPW}

Notes: 1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be be accommodated by the programmer.
3. When programming the TS27C64A, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transiens which can damage the device.

HIGH SPEED PROGRAMMING FLOW CHART

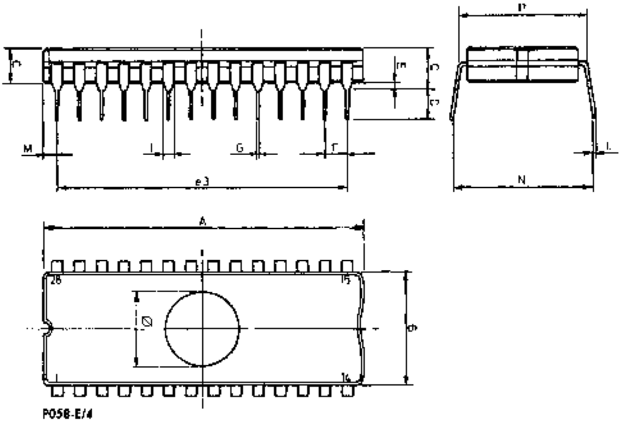

START
ADDR-FIRST LOCATION
VCC = 6V
VPP = 12.5V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
PROGRAM VERIFY ONE BYTE
FAIL
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
LAST ADDR ?
NO
INCREMENT ADDR
YES
VCC = VPP = 5V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S-6881

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-15XCQ	150ns	5V ± 5%	0 to +70°C	DIP-28
TS27C64A-20XCQ	200ns	5V ± 5%	0 to +70°C	DIP-28
TS27C64A-25XCQ	250ns	5V ± 5%	0 to +70°C	DIP-28
TS27C64A-30XCQ	300ns	5V ± 5%	0 to +70°C	DIP-28
TS27C64A-15CQ	150 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C64A-20CQ	200 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C64A-25CQ	250 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C64A-30CQ	300 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C64A-15VQ	150 ns	5V ± 10%	– 40 to +85°C	DIP-28
TS27C64A-20VQ	200 ns	5V ± 10%	– 40 to +85°C	DIP-28
TS27C64A-25VQ	250 ns	5V ± 10%	– 40 to +85°C	DIP-28
TS27C64A-30VQ	300 ns	5V ± 10%	– 40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



P058-E/4

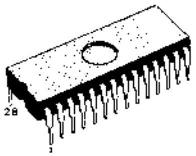
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e 3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

SGS-THOMSON
MICROELECTRONICS

TS27C256Q

256K (32K × 8) CMOS UV ERASABLE PROM

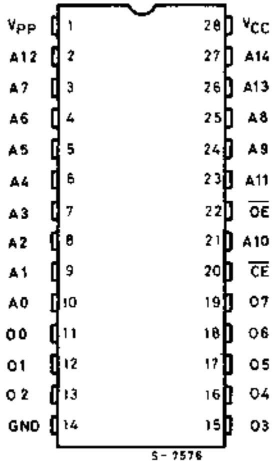
- FAST ACCESS TIME: 150ns, 170ns, 200ns, 250ns, 300ns.
- COMPATIBLE TO HIGH SPEED MICROPROCESSORS ZERO WAIT STATE
- 28-PIN JEDEC APPROVED PIN-OUT
- LOW POWER CONSUMPTION:
  ACTIVE 30mA MAX
  STANDBY 1mA MAX
- PROGRAMMING VOLTAGE 12.5V
- HIGH SPEED PROGRAMMING
- ELECTRONIC SIGNATURE
- WILL BE PROPOSED IN PLASTIC PACKAGE (OTP)



Q
DIP-28
(Ceramic Bull's Eye)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS


V_{PP} 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
28 V_{CC}
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3
S - 7576

DESCRIPTION

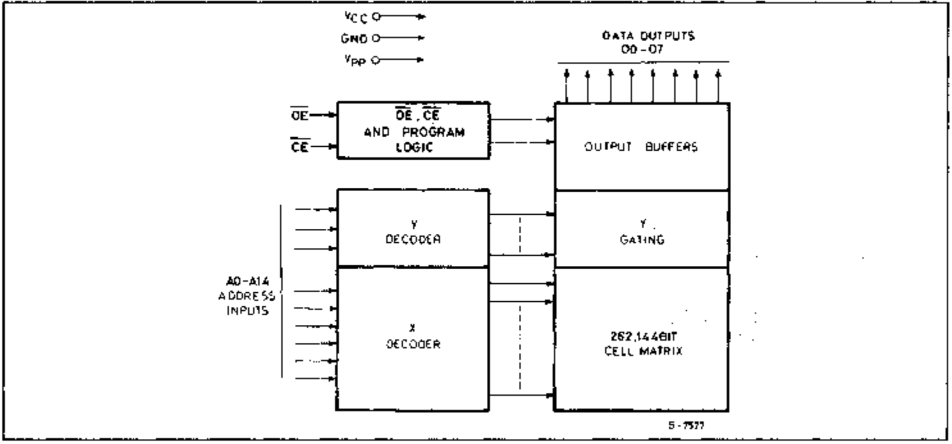
The TS27C256 is a high speed 262,144 bit UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

The TS27C256 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

PIN NAMES

A0—A14	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
DATA OUTPUTS
O0 - O7
$\overline{OE}$
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$
AND PROGRAM
LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0 - A14
ADDRESS
INPUTS
X
DECODER
262,144 BIT
CELL MATRIX
5 - 7577

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range TS27C256CQ TS27C256VQ	T_L to T_H 0 to + 70 – 40 to + 85	°C
T_{stg}	Storage temperature range	– 65 to + 125	°C
V_{PP}(2)	Supply voltage	– 0.6 to + 14	V
V_{IN}(2)	Input voltages A9 Except V_{PP}, A9	– 0.6 to + 13.5 – 0.6 to + 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

Notes: 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13 15-19)
READ	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Hi-Z
STANDBY	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{CC}	V_{CC}	CODE

Notes: 1 - X can be either V_{IL} or V_{IH} — 2 - $V_H = 12.0V \pm 0.5V$
3 - All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 04).

READ OPERATION

DC CHARACTERISTICS ($T_{amb} = T_L$ to T_H, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$; Unless otherwise specified)(5)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(1)	Max.	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}, $\overline{CE} = V_{IH}$			10	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC} - 0.7$		V_{CC}	V
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $I_{OL} = 0$ µA			0.45 0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA $I_{OH} = 0$ µA	2.4 $V_{CC} - 0.1$			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE} = \overline{OE} = V_{IL}$, Inputs $= V_{IH}$ or V_{IL}, f = 5 MHz, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	V_{IH} or V_{IL}		0.05	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$V_{CC} - 0.1V$ or $V_{SS} + 0.1V$		1	10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{CC} = 5.5V$			10	µA

Note: 1. Typical conditions are for operation at: $T_{amb} = +25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$

AC CHARACTERISTICS(1)($T_{amb} = T_L$ to T_H)(5)

Symbol	Parameter	Test Conditions	27C256 -15		27C256 -17		27C256 -20		27C256 -25		27C256 -30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		170		200		250	300	ns	
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		75		75		100		120	ns
t_{DF}(2,4)	$\overline{OE}$ or $\overline{CE}$ High to output float		0	50	0	50	0	55	0	60	0	75	ns
t_{OH}	Output Hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		0		ns

CAPACITANCE $T_{amb} = +25°C$, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{out}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

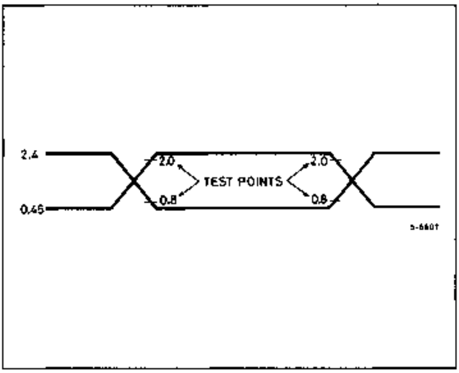
Notes: 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}. V_{PP} may be connected to V_{CC} except during program.

2. The t_{DF} compare level is determined as follows:
   High to THREE-STATE, the measured V_{OH}(DC) $-0.1V$
   Low to THREE-STATE the measured V_{OL}(DC) $+0.1V$.
3. Capacitance is guaranteed By periodic testing. $T_{amb} = +25°C$, f = 1MHz.
4. T_{DF}, is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first. This parameter is only sampled and not 100% tested.
5. All parameters are specified at $V_{CC} = 5V \pm 5\%$ for 27C256-15X, 27C256-17X, 27C256-20X, 27C256-25X and 27C256-30X.

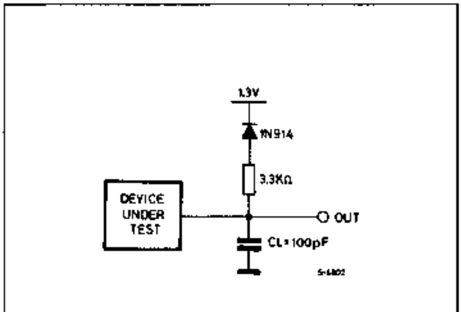
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

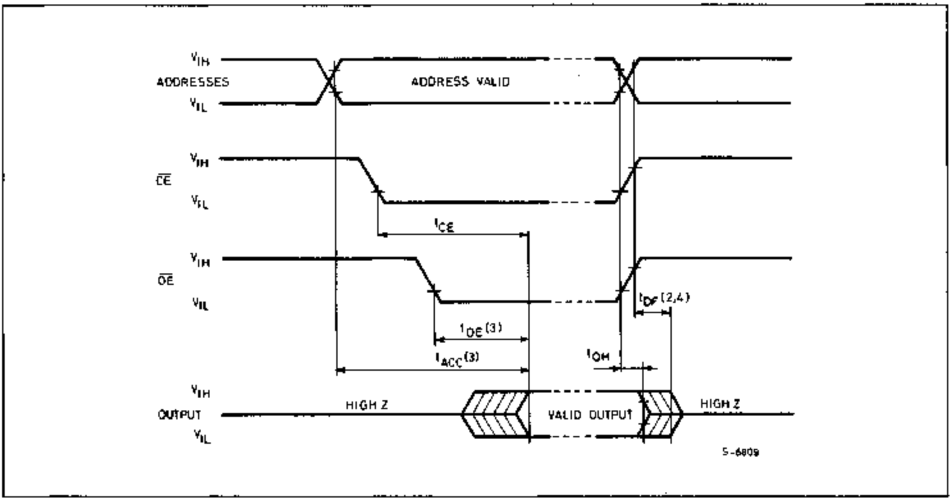

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6801

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL = 100pF
5-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{DF} (2,4)
t_{OE} (3)
t_{ACC} (3)
t_{OH}
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
5-6809

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C256 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

READ MODE

The TS27C256 has two control functions, both of wich must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to Output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C256 has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because EPROMs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ (pin 20) should be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING MODES

Caution: Exceeding 14V on pin 1 (V_{PP}) will damage the TS27C256.

Initially, and after each erasure, all bits of the TS27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The TS27C256 is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ is at TTL Low. It is required that a 0.1 µF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled TS27C256s.

HIGH SPEED PROGAMMING

The high speed programming algorithm described in the flow chart rapidly programs TS27C256 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 5 minutes.

PROGRAM INHIBIT

Programming of multiple TS27C256s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ input inhibits the other TS27C256s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C256s may be common. A TTL low-level pulse applied to a TS27C256 $\overline{CE}$ input with V_{PP} at 12.5 V will program that TS27C256.

PROGRAM VERIFY

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5 V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will indentify the EPROM manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C256. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the TS27C256. Two bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electonic signature mode.

ERASING

The TS27C256 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the TS27C256 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537A yielding a total integrated dosage of 15 watt-seconds/cm² is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm² power rating is used. The TS27C256 to be erased should be placed 1 inch from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occuring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

PROGRAMMING OPERATIONS(1) ($T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (all inputs)		– 0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -400$ μA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL}$			30	mA

AC CHARACTERISTICS

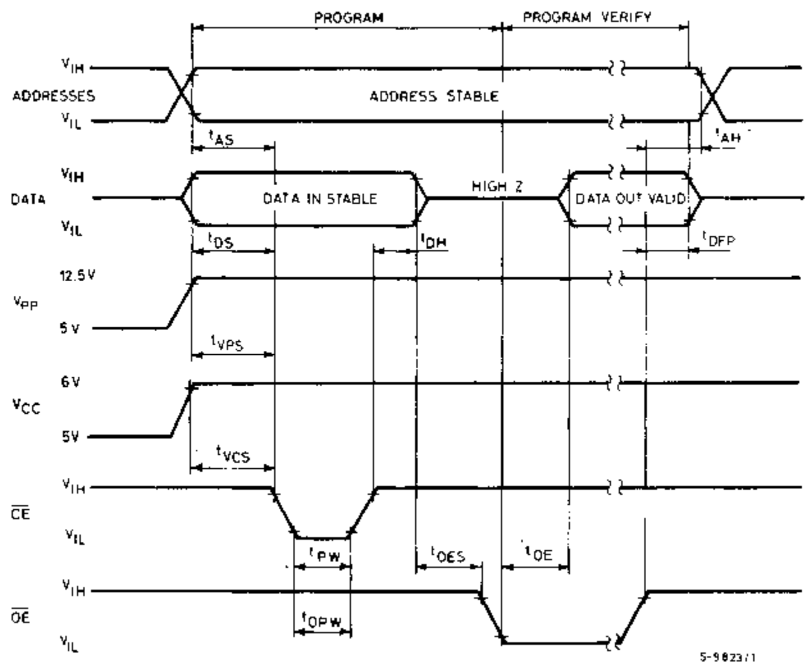
Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set-up Time		2			μs
t_{OES}	$\overline{OE}$ Set-up Time		2			μs
t_{DS}	Data Set-up Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			μs
t_{VCS}	V_{CC} set-up time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}(2)	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

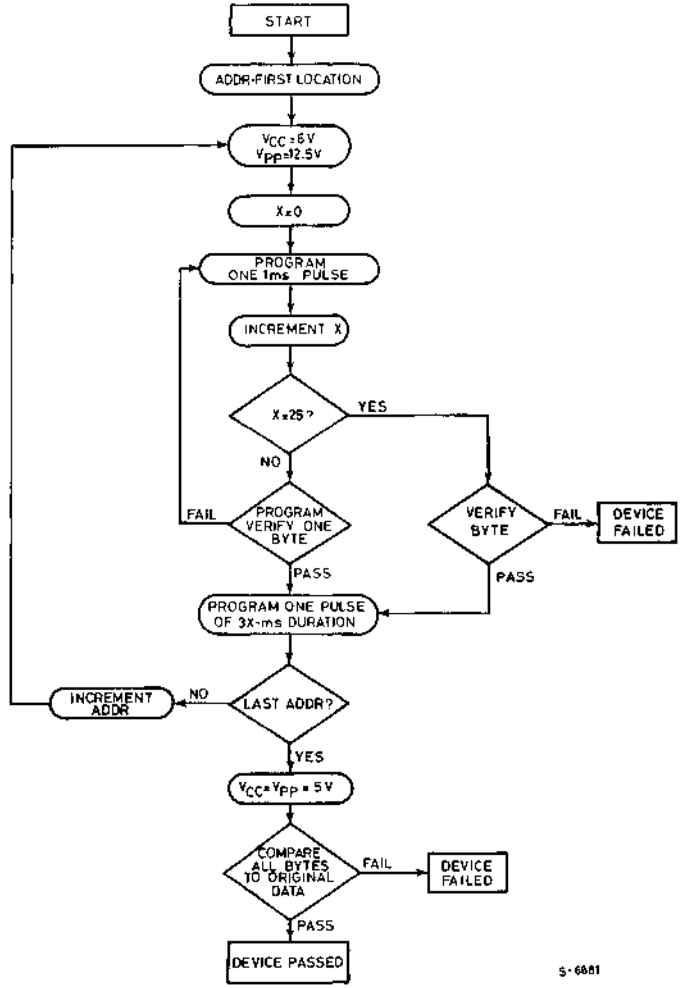
Input rise and fall times (10% to 90%)	≤20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Output timing reference level	0.8V and 2.0V

HIGH SPEED PROGRAMMING WAVEFORMS


PROGRAM
PROGRAM VERIFY
V_IH
ADDRESSES
V_IL
ADDRESS STABLE
t_AS
t_AH
V_IH
DATA
V_IL
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DFP
12.5 V
V_PP
5 V
t_VPS
6 V
V_CC
5V
t_VCS
V_IH
CE
V_IL
t_PW
t_OES
t_OE
V_IH
OE
V_IL
t_OPW
5-9823/1

1. The input timing reference level is 0.8 for V_{IL} and 2.0V for V_{IH}
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodate by the programmer.
3. When programming the TS27C256, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transiens which can damage the device.

HIGH SPEED PROGRAMMING FLOW CHART

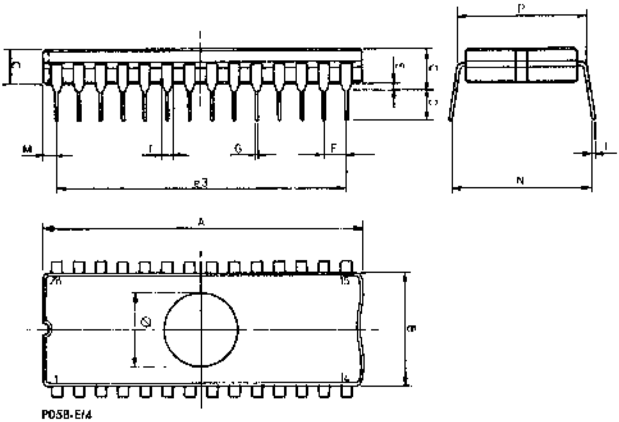

START
ADDR-FIRST LOCATION
VCC = 6V
VPP=12.5V
X=0
PROGRAM
ONE 1ms PULSE
INCREMENT X
X=25?
YES
NO
FAIL
PROGRAM
VERIFY ONE
BYTE
VERIFY
BYTE
FAIL
DEVICE
FAILED
PASS
PASS
PROGRAM ONE PULSE
OF 3X-ms DURATION
INCREMENT
ADDR
NO
LAST ADDR?
YES
VCC=VPP=5V
COMPARE
ALL BYTES
TO ORIGINAL
DATA
FAIL
DEVICE
FAILED
PASS
DEVICE PASSED
S-6881

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C256-15XCQ	150 ns	5V ± 5%	0 to +70°C	DIP-28
TS27C256-17XCQ	170 ns	5V ± 5%	0 to +70°C	DIP-28
TS27C256-20XCQ	200 ns	5V ± 5%	0 to +70°C	DIP-28
TS27C256-25XCQ	250 ns	5V ± 5%	0 to +70°C	DIP-28
TS27C256-30XCQ	300 ns	5V ± 5%	0 to +70°C	DIP-28
TS27C256-17CQ	170 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C256-20CQ	200 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C256-25CQ	250 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C256-30CQ	300 ns	5V ± 10%	0 to +70°C	DIP-28
TS27C256-15VQ	150 ns	5V ± 5%	−40 to +85°C	DIP-28
TS27C256-17VQ	170 ns	5V ± 10%	−40 to +85°C	DIP-28
TS27C256-20VQ	200 ns	5V ± 10%	−40 to +85°C	DIP-28
TS27C256-25VQ	250 ns	5V ± 10%	−40 to +85°C	DIP-28
TS27C256-30VQ	300 ns	5V ± 10%	−40 to +85°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A			38.10			1.500
B	13.05		13.36	0.514		0.526
C	3.90		5.08	0.154		0.200
D	3.00			0.118		
E	0.50		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.018		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	16.51		18.00	0.650		0.709
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
Ø	6.86		7.36	0.270		0.290

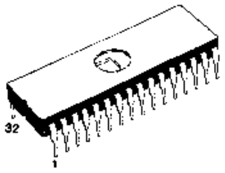
SGS-THOMSON
MICROELECTRONICS

ST27C1001

1024K (128K × 8) CMOS UV ERASABLE PROM

ADVANCED DATA

- 8 BITS OUTPUTS
- FAST ACCESS TIME 120ns.
- LOW "CMOS" CONSUMPTION 50mA (MAX.)
- PROGRAMMING VOLTAGE 12.5V
- ELECTRONIC SIGNATURE FOR AUTOMATED PROGRAMMING
- PROGRAMMING TIMES IN THE 20 SECONDS RANGE.



F
DIP-32
(Ceramic Bull's eye)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The ST27C1001 is a high speed 1 Mbit UV erasable and electrically programmable EPROM ideally suited for 8-bit microprocessors systems requiring large programs.

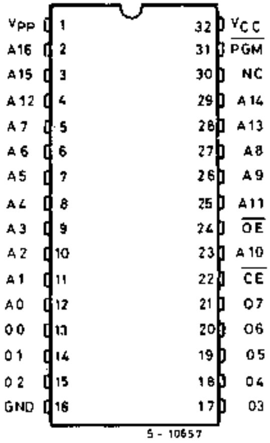
It is organized as 131072 words by 8 bits, and packaged in a 32 pins Ceramic DIP Bull's eye package. ST will also introduce the following versions based on the same architecture but with different configurations. They are:

- ST27C1011 is a page addressed 1024K (8 × 16K × 8) device, packaged in a 28 pin DIP for easy replacement of 64K and 128K standard EPROM versions.
- ST87C1011 is the same device as the ST27C1011 with latched addresses for design optimization in multiplexed bus environment.
- ST27C1000 is organized as 128K × 8 bits with a ROM compatible pinout.
- ST87C1000 is the same device as the ST27C1000 with latched addresses for design optimization in multiplexed bus environment.

PIN NAMES

A0—A16	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O_0-O_7	DATA INPUT/OUTPUT
NC	NON CONNECTED

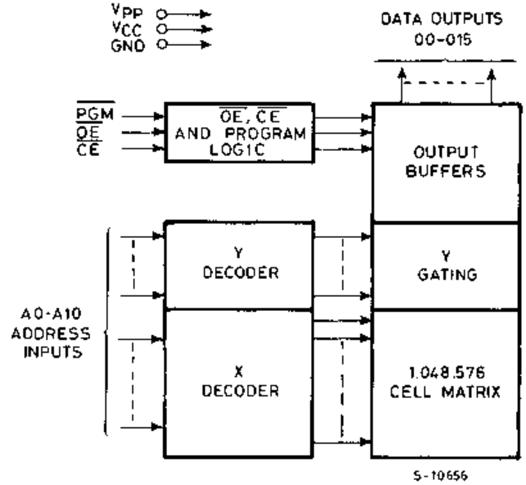
PIN CONNECTIONS



June 1988

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM


VPP
VCC
GND
DATA OUTPUTS
O0-O15
PGM
OE
CE
OE, CE
AND PROGRAM
LOGIC
OUTPUT
BUFFERS
Y
DECODER
Y
GATING
A0-A10
ADDRESS
INPUTS
X
DECODER
1.048.576
CELL MATRIX
S-10656

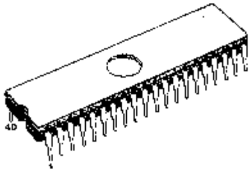
SGS-THOMSON
MICROELECTRONICS

M27C1024

1024K (64K x 16) CMOS UV ERASABLE PROM

PRELIMINARY DATA

- FAST ACCESS TIME:
  120ns MAX M27C1024-12XF1/M27C1024-12F1
  150ns MAX M27C1024-15XF1/M27C1024-15F1/ M27C1024-15XF6
  200ns MAX M27C1024-20XF1/M27C1024-20F1/ M27C1024-20XF6
  250ns MAX M27C1024-25XF1/M27C1024-25F1/ M27C1024-25XF6
- 0 TO +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT (1mA MAX)
- TTL PROGRAMMING
- VERY FAST AND RELIABLE PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



F
DIP-40
(Ceramic Bull's Eye)

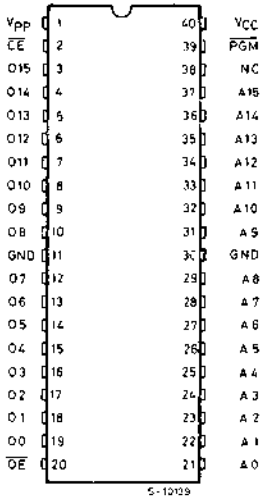
(Ordering Information at the end of the datasheet)

DESCRIPTION

The M27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable read only memory (EPROM). It is organized as 65,536 words by 16 bits and manufactured using SGS-THOMSON' CMOS-E4 process. The M27C1024 with its single +5V power supply and with an access time of 120ns, is ideal for use in 16 bit microprocessor system allowing full speed operation without WAIT states. In high performance CPU's (10MHz), the M27C1024 has an important feature which is to separate the output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. The M27C1024 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 50mA while the maximum standby current is only 1 mA. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The M27C1024 enables implementation of new, advanced systems with firmware intensive architectures.

The combination of the M27C1024s high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The M27C1024 large storage capability enables it to function as a high density software carrier. The M27C1024 has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

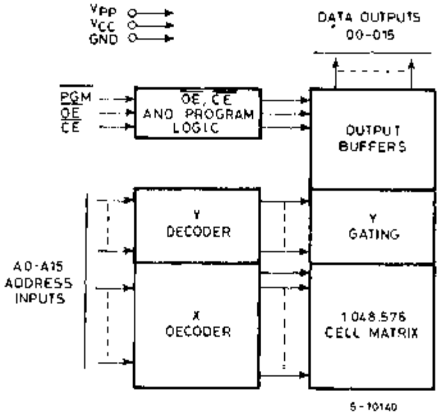
PIN CONNECTIONS



PIN NAMES

A0-A15	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
O0-O15	DATA INPUT/OUTPUT
NC	NON CONNECTED

BLOCK DIAGRAM


V_{PP}
V_{CC}
GND
DATA OUTPUTS
O0-O15
$\overline{PGM}$
$\overline{OE}$
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$ AND PROGRAM LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A15 ADDRESS INPUTS
X DECODER
1,048,576 CELL MATRIX
5-10140

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6.5 to − 0.6	V
V_{PP}	Supply voltage with respect to ground	+ 14 to − 0.6	V
T_{amb}	Ambient temperature under bias /F1 /F6	− 10 to + 80 − 50 to + 95	°C °C
T_{stg}	Storage temperature range	− 65 to + 125	°C
	Voltage on pin 31 with respect to ground	+ 13.5 to − 0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (2)	$\overline{OE}$ (20)	A9 (31)	$\overline{PGM}$ (39)	V_{PP} (1)	OUTPUTS
READ	L	L	X	H	V_{CC}	D_{OUT}
OUTPUT DISABLE	L	H	X	H	V_{CC}	HIGH Z
STANDBY	H	X	X	X	V_{CC}	HIGH Z
PROGRAM	L	X	X	L	V_{PP}	D_{IN}
PROGRAM VERIFY	L	L	X	H	V_{PP}	D_{OUT}
PROGRAM INHIBIT	H	X	X	X	V_{PP}	HIGH Z
ELECTRONIC SIGNATURE	L	L	V_H	H	V_{CC}	CODE

NOTE: X = DON'T CARE; V_H = 12V ±0.5V; H = HIGH; L = LOW

READ OPERATION

DC AND AC CONDITIONS

Selection Code	– 12XF1/ – 15XF1 – 20XF1/ – 25XF1	– 12F1/ – 15F1 – 20F1/ – 25F1	– 15XF6/ – 20XF6 – 25XF6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (2)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{CC1}	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			1	mA
I_{CC2}	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ @f = 8MHz		20	50	mA
V_{IL}	Input Low Voltage		–0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm 10\%$	27C1024-12/		27C1024-15/		27C1024-20/		27C1024-25/		Unit
		$V_{CC} \pm 5\%$	27C1024-12X		27C1024-15X		27C1024-20X		27C1024-25X		
		Test Condition	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60		75		75	ns
$t_{DF(3)}$	$\overline{OE}$High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	60	0	90	0	90	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE(4) ($T_{amb} = 25°C$, f = 1 MHz)

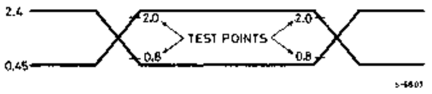
Symbol	Parameter	Test Conditions	Min.	Typ. (2)	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
3. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
4. This parameter is only sampled and not 100% tested.

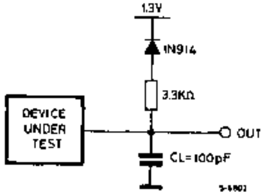
AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

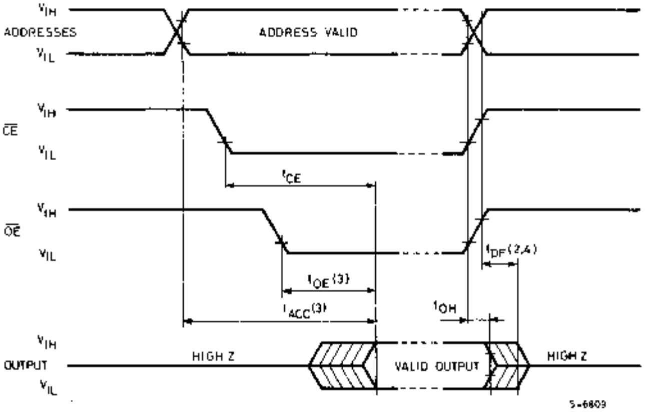

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6803

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
5-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} (2,4)
t_{OE} (3)
t_{ACC} (3)
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z
5-6809

Notes: 1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The modes of operations of the M27C1024 are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for 12V on A9 for Electronic Signature.

READ MODE

The M27C1024 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M27C1024 has a standby mode which reduces the maximum active power current from 50 mA to 1 mA. The M27C1024 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.
The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on V_{PP} pin will permanently damage the M27C1024.

When delivered, and after each erasure, all bits of the M27C1024 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M27C1024 is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL-low. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.
V_{CC} is specified to be 6.25V ± 0.25V.

VERY FAST AND RELIABLE PROGRAMMING ALGORITHM = PRESTO II

PRESTO II programming algorithm, available for the M27C1024 is an enhancement of the PRESTO algorithm used for the M27512.
During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 6 seconds.

PROGRAM INHIBIT

Programming of multiple M27C1024s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel M27C1024 may be common. A TTL low level pulse applied to a M27C1024's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that M27C1024. A high level $\overline{CE}$ input inhibits the other M27C1024s from being programmed. V_{CC} is specified to be 6.25V ± 0.25V.

PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, V_{PP} at 12.5V and V_{CC} at 6.25V ± 0.25V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27C1024. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 31) of the M27C1024. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 21) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode, except for A14 and A15 which should be held high. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON M27C1024, these two identifier bytes are given here below, and can be read-out on outputs O0 to O7 while outputs O_8 to O_{15} are don't care.

ERASURE OPERATION

The erasure characteristic of the M27C1024 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27C1024 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the M27C1024 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C1024 window to prevent unintentional erasure. The recommended erasure procedure for the M27C1024 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm^2 power rating. The M27C1024 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

ELECTRONIC SIGNATURE MODE

IDENTIFIER \ PINS	A0 (21)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	1	0	0	8C

Note: A9 = 12V ± 0.5V; A1-A8, A10-A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}; A14, A15 = V_{IH}

PROGRAMMING OPERATION (T_{amb} = 25°C ± 5°C, $V_{CC}^{(1)}$ = 6.25V ± 0.25V, $V_{PP}^{(1)}$ = 12.5V ± 0.5V)

DC AND OPERATING CHARACTERISTIC:

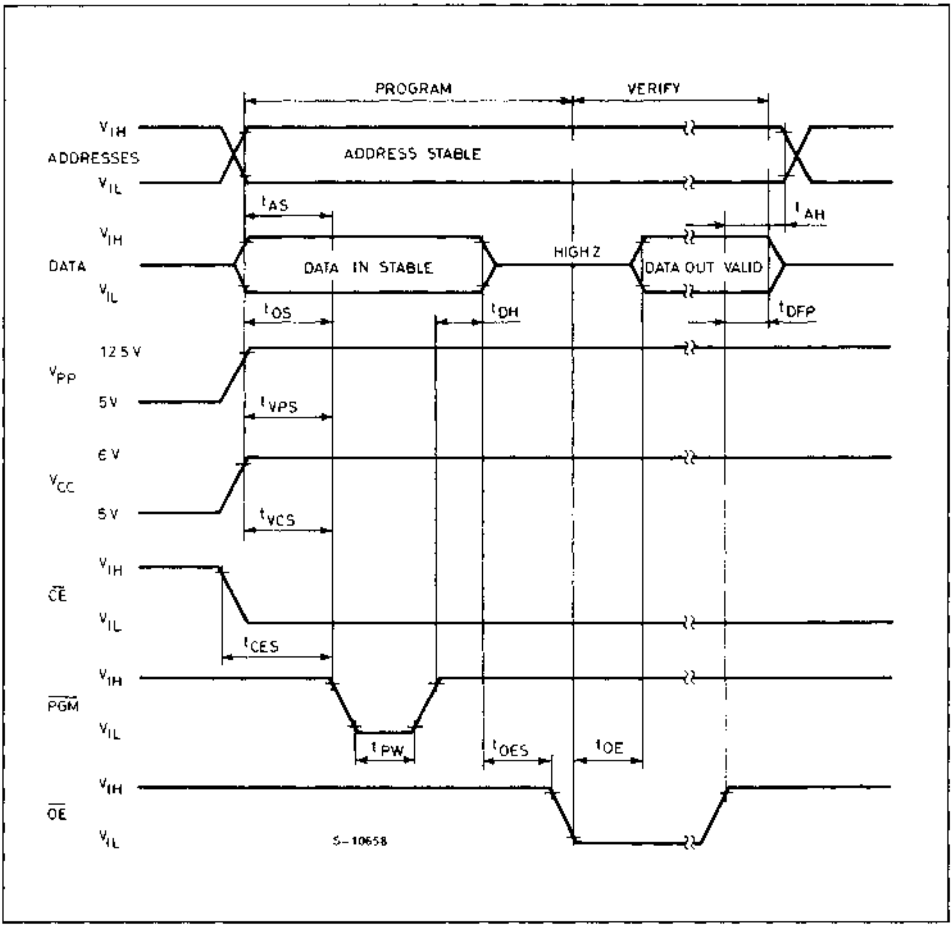
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		– 0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = – 400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current			20	50	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(2)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$				100	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

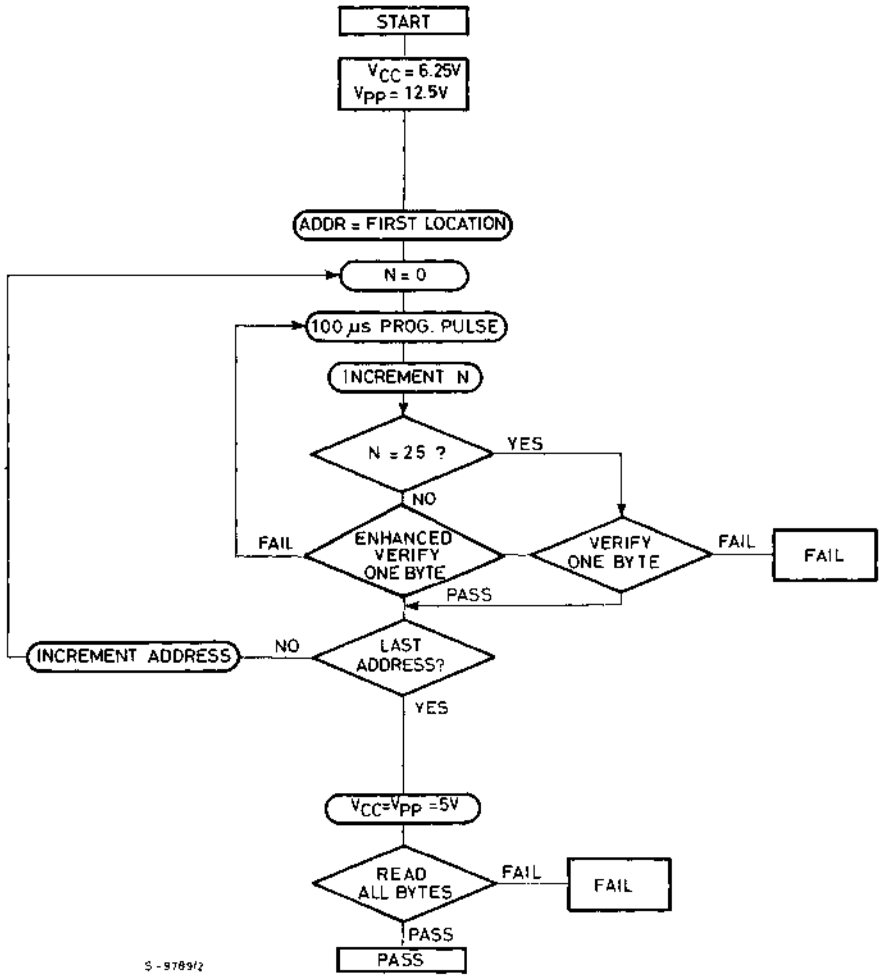
PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5 V
5V
t_{VPS}
V_{CC}
6 V
5 V
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OES}
t_{OE}
$\overline{OE}$
S-10658

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DPF} are characteristics of the device but must be accommodated by the programmer.
3. When programming the M27C1024 a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

PRESTO II PROGRAMMING ALGORITHM

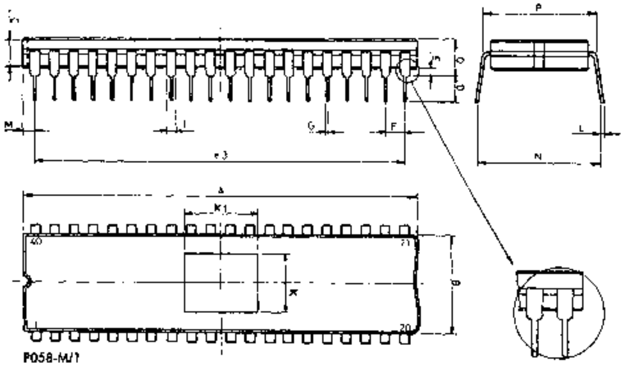

START
VCC = 6.25V
VPP = 12.5V
ADDR = FIRST LOCATION
N = 0
100 µs PROG. PULSE
INCREMENT N
N = 25 ?
YES
NO
FAIL
ENHANCED VERIFY ONE BYTE
VERIFY ONE BYTE
FAIL
FAIL
PASS
INCREMENT ADDRESS
NO
LAST ADDRESS?
YES
VCC=VPP =5V
READ ALL BYTES
FAIL
FAIL
PASS
PASS
S - 9789/2

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M27C1024-12F1	120 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-15F1	150 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-20F1	200 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-25F1	250 ns	5V ± 10%	0 to +70°C	DIP-40
M27C1024-12XF1	120 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-15XF1	150 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-20XF1	200 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-25XF1	250 ns	5V ± 5%	0 to +70°C	DIP-40
M27C1024-15XF6	150 ns	5V ± 5%	−40 to +85°C	DIP-40
M27C1024-20XF6	200 ns	5V ± 5%	−40 to +85°C	DIP-40
M27C1024-25XF6	250 ns	5V ± 5%	−40 to +85°C	DIP-40

PACKAGE MECHANICAL DATA

40-PIN CERAMIC DIP BULL'S EYE



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			53.40			2.102
B	14.50		14.90	0.571		0.587
C	3.90		5.08	0.154		0.200
D	3.40			0.134		
E	0.50		1.78	0.020		0.070
e 3		48.26			1.900	
F	2.29		2.79	0.090		0.110
G	0.40		0.55	0.016		0.022
I	1.27		1.52	0.050		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N	15.62		17.78	0.615		0.700
P	15.40		15.80	0.606		0.622
Q			5.71			0.225
K	7.90		8.38	0.311		0.330
K1	10.41		10.92	0.410		0.430

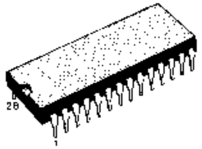
EPROM DEVICES

NMOS OTP ROM

ST2764AP

64K (8K × 8) NMOS ONE TIME PROGRAMMABLE ROM

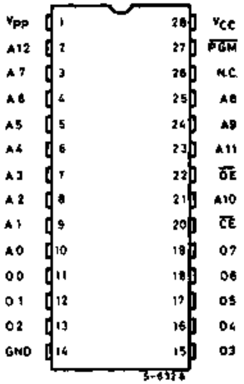
- FAST ACCESS TIME: 180ns
- 0 to +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (35mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



P
DIP-28
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

The ST2764AP is a 65,536-bit one time programmable read only memory (OTP ROM). It is organized as 8,192 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

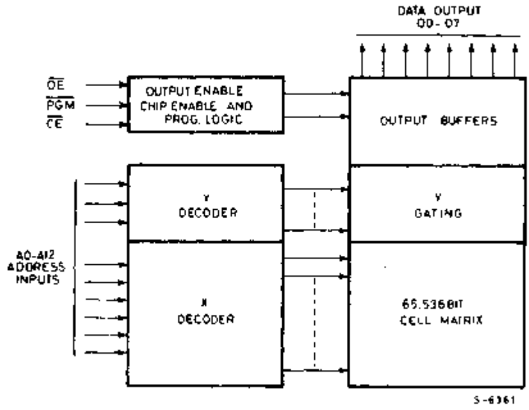
The ST2764AP with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The ST2764AP has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The ST2764AP also features a standby mode which reduces the power dissipation without increasing access time. The active current is 75mA while the maximum standby current is only 35 mA, a 53% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The ST2764AP has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.
The ST2764AP is available in a 28-lead dual in-line plastic package and therefore can not be rewritten.

PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


DATA OUTPUT
O0 - O7
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE
CHIP ENABLE AND
PROG. LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A12
ADDRESS
INPUTS
X
DECODER
65,536BIT
CELL MATRIX
S-6361

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.5 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias	−10 to +80	°C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION

DC AND AC CONDITIONS

Selection Code	– 18X/ – 20X	– 18/ – 20/ – 25/ – 30
Operating Temperature Range	0 to 70°C	0 to 70°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{PP1}(2)	V_{PP} Current Read	$V_{PP} = 5.5V$			5	mA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			35	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$			75	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
V_{PP}(2)	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm$ 5%	2764A-18X		2764A-20X						Unit
		$V_{CC} \pm 10\%$	2764A-18		2764A-20		2764A -25		2764A-30		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		180		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		180		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		65		75		100		120	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		55	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

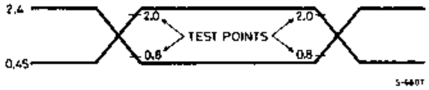
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and is not 100% tested.

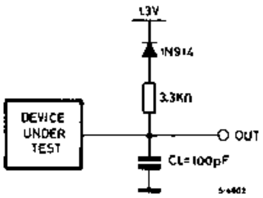
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

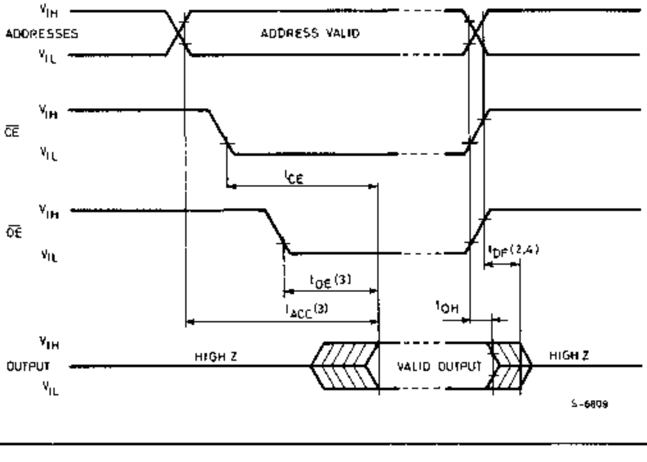

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6607

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6602

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_IH
ADDRESSES
V_IL
ADDRESS VALID
V_IH
CE
V_IL
t_CE
V_IH
OE
V_IL
t_DF (2,4)
t_OE (3)
t_ACC (3)
t_OH
V_IH
OUTPUT
V_IL
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the ST2764AP are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The ST2764AP has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ST2764AP has a standby mode which reduces the maximum active power current from 75 mA to 35 mA. The ST2764AP is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because OTPs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND.

This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 14V on pin 1 (V_{PP}) will damage the ST2764AP.

When delivered, all bits of the ST2764AP are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word.

The ST2764AP is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs ST2764AP EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the ST2764AP Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular ST2764AP location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

DEVICE OPERATION (Continued)

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple ST2764APs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ST2764AP may be common. A TTL low pulse applied to a ST2764AP's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that ST2764AP. A high level $\overline{CE}$ input inhibits the other ST2764AP from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the ST2764AP. To activate this mode,. the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the ST2764AP. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON ST2764AP, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ELECTRONIC SIGNATURE MODE

PINS IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	1	0	0	0	08

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, V_{CC}(1) = 6V ±0.25V, V_{PP}(1) = 12.5V ±0.3V)

DC AND OPERATING CHARACTERISTIC

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				75	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

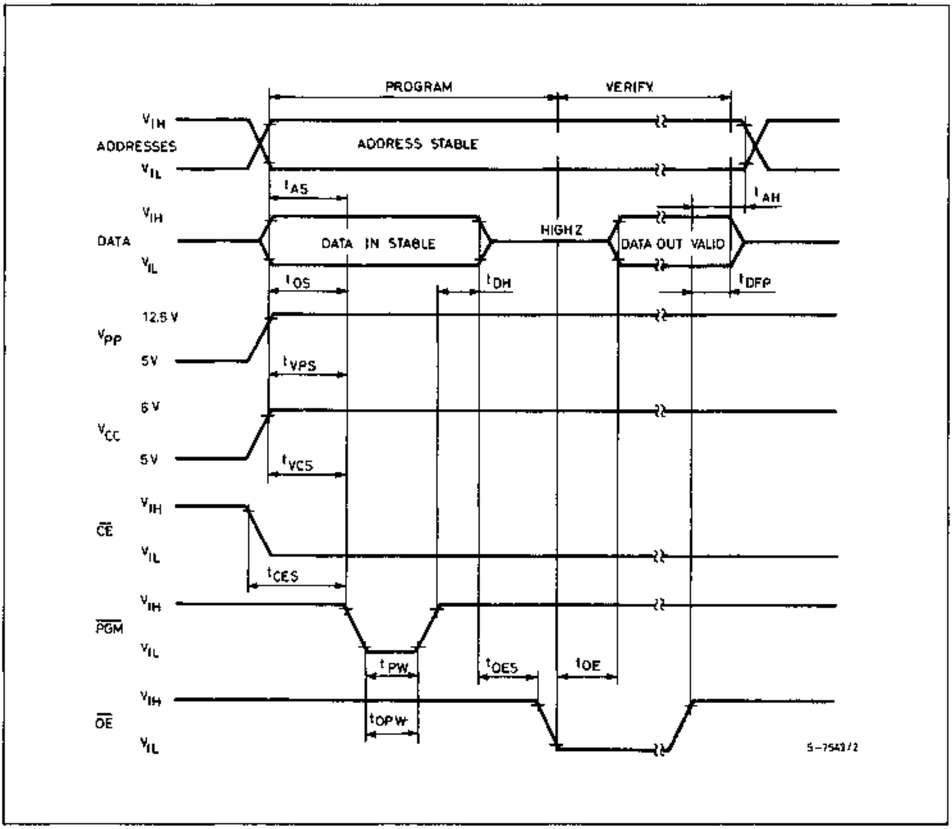
AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(4)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time				µs	2
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

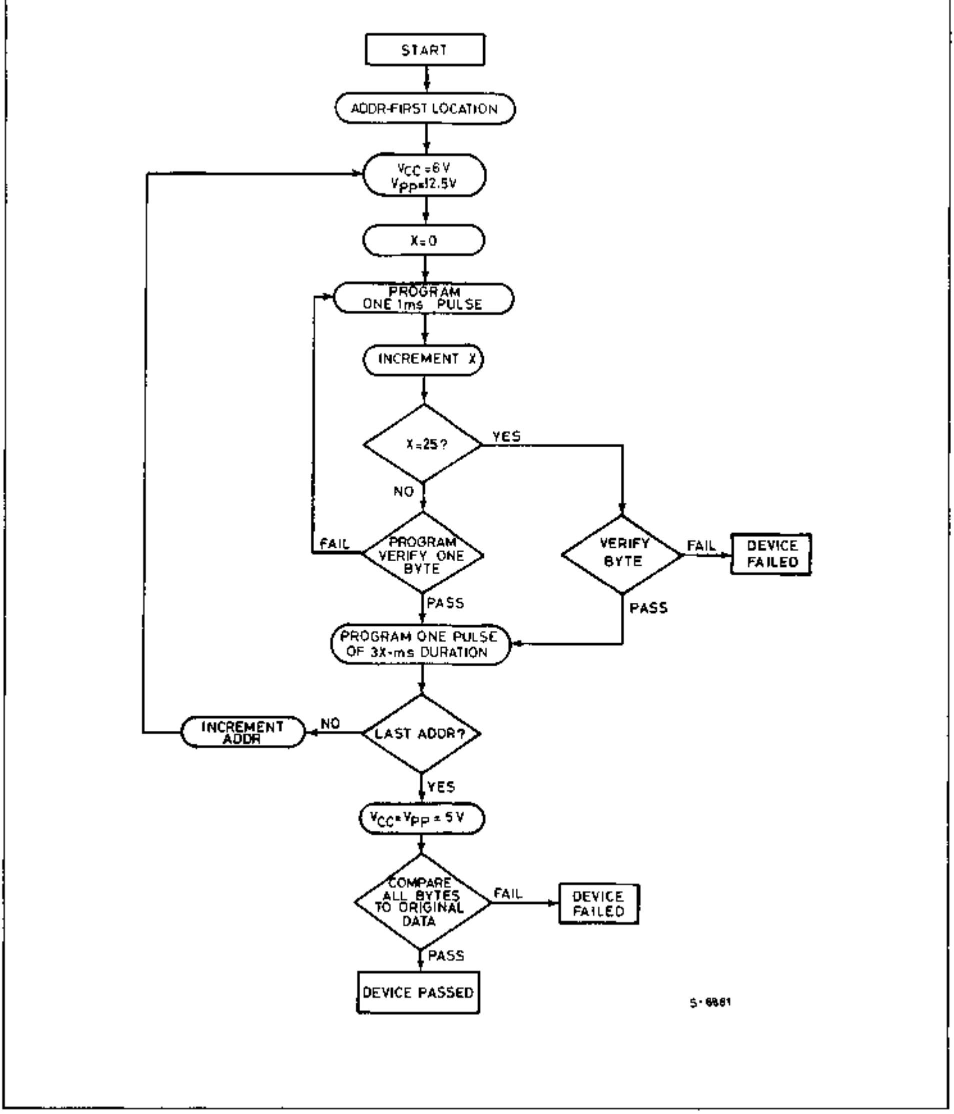
PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5 V
5V
t_{VPS}
V_{CC}
6 V
5 V
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OPW}
t_{OES}
t_{OE}
$\overline{OE}$
5-7543/2

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the ST2764AP a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

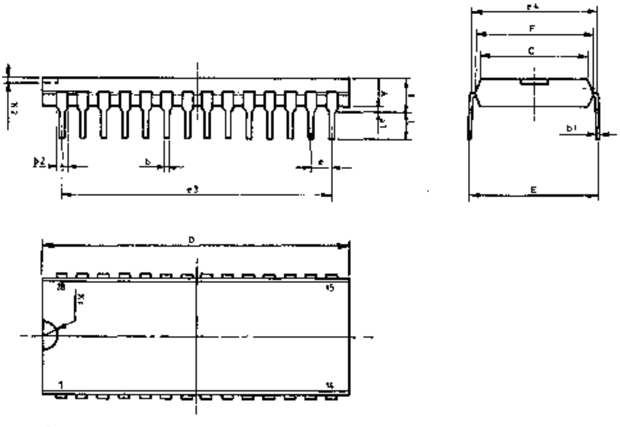

START
ADDR-FIRST LOCATION
V_{CC} = 6V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
V_{CC} = V_{PP} = 5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S - 6861

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST2764A-18XCP	180 ns	5V ± 5%	0 to +70°C	DIP-28
ST2764A-20XCP	200 ns	5V ± 5%	0 to +70°C	DIP-28
ST2764A-18CP	180 ns	5V ± 10%	0 to +70°C	DIP-28
ST2764A-20CP	200 ns	5V ± 10%	0 to +70°C	DIP-28
ST2764A-25CP	250 ns	5V ± 10%	0 to +70°C	DIP-28
ST2764A-30CP	300 ns	5V ± 10%	0 to +70°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

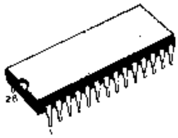
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

SGS-THOMSON
MICROELECTRONICS

ST27128AP

128K (16K × 8) NMOS ONE TIME PROGRAMMABLE ROM

- FAST ACCESS TIME: 150ns
- 0 to +70°C STANDARD TEMPERATURE RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



P
DIP-28
(Plastic Package)

(Ordering information at the end of the datasheet)

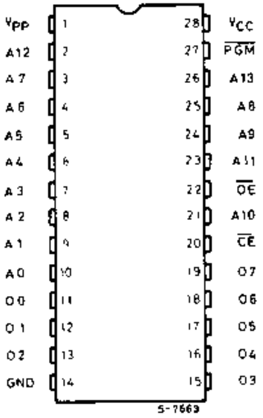
DESCRIPTION

The ST27128AP is a 131,072-bit one time programmable read only memory (OTP ROM). It is organized as 16,384 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process.

The ST27128AP with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The ST27128AP has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The ST27128AP also features a standby mode which reduces the power dissipation without increasing access time. The active current is 85mA while the maximum standby current is only 40mA, a 53% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The ST27128AP has an "Electronic Signature" that allows programmers to automatically identify device type and pinout. The ST27128AP is available in a 28-lead dual in-line plastic package and therefore cannot be rewritten.

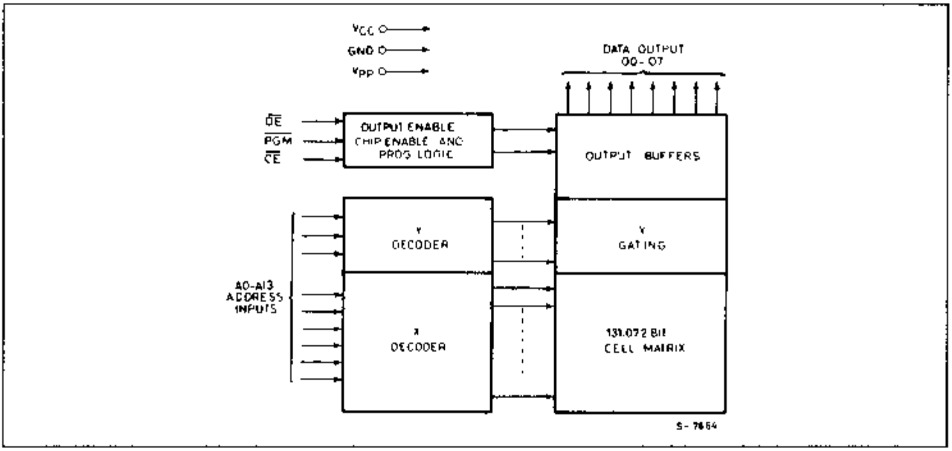
PIN CONNECTIONS



PIN NAMES

A0-A13	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
DATA OUTPUT
O0 - O7
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE
CHIP ENABLE AND
PROG LOGIC
OUTPUT BUFFERS
Y
DECODER
Y
GATING
A0-A13
ADDRESS
INPUTS
X
DECODER
131,072 BIT
CELL MATRIX
S - 7654

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	All Input or Output voltages with respect to ground	+6.25 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias	−10 to +80	°C
T_{stg}	Storage temperature range	− 65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
FAST PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL}	V_{IL}	V_H	V_{IH}	V_{CC}	V_{CC}	CODES

NOTE: X can be V_{IH} or V_{IL} $V_H = 12V \pm 0.5V$

READ OPERATION

DC AND AC CONDITIONS

Selection Code	– 15X/ – 20X	– 20/ – 25/ – 30
Operating Temperature Range	0 to 70°C	0 to 70°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{PP1}(2)	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IH}$			40	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$			85	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
V_{PP}(2)	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC} \pm 5\%$	27128A-15X		27128A-20X						Unit
		$V_{CC} \pm 10\%$			27128A-20		27128A-25		27128A-30		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		65		75		100		120	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		55	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

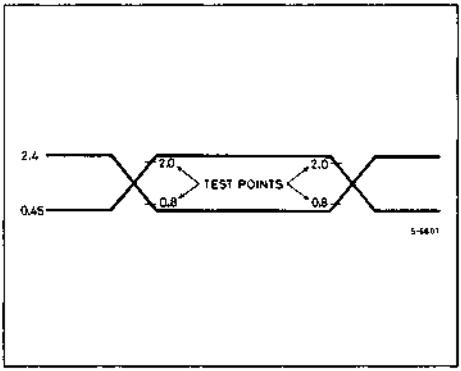
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}[2]	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven. (See timing diagram).
5. This parameter is only sampled and is not 100% tested.

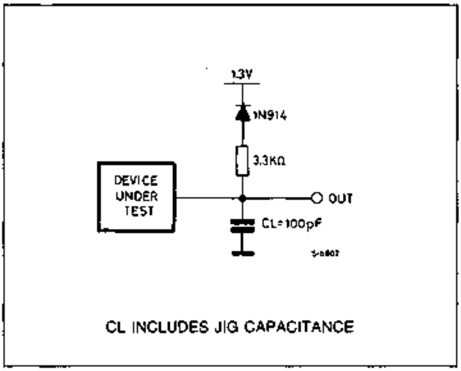
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

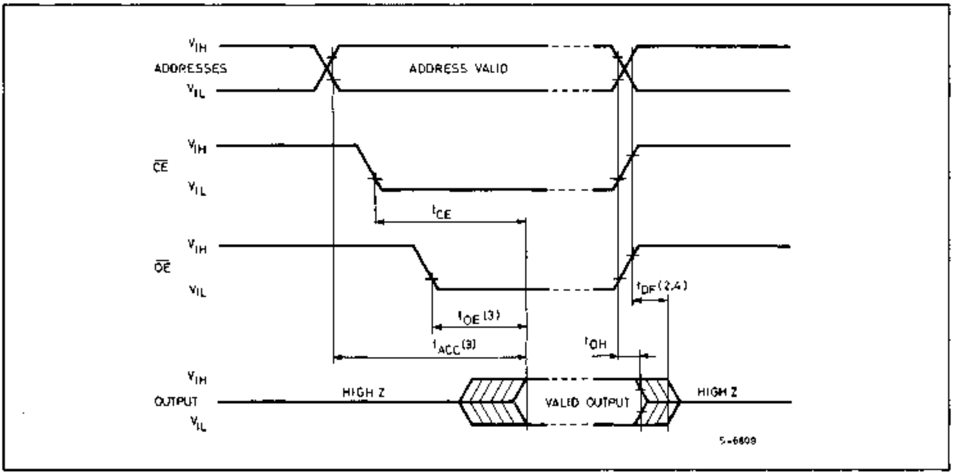

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6601

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
5-6602

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} (2,4)
t_{OE} (3)
t_{ACC} (3)
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z
5-6609

Notes:
1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operations of the ST27128AP are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

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The ST27128AP has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ST27128AP has a standby mode which reduces the maximum active power current from 85 mA to 40 mA. The ST27128AP is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because OTPs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors.

It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the ST27128AP.

When delivered, all bits of the ST27128AP are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word.

The ST27128AP is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and $\overline{PGM}$ are at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs ST27128AP EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the ST27128AP Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

The duration of the initial $\overline{PGM}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular ST27128AP location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

DEVICE OPERATION (Continued)

The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6V$ and $V_{PP} = 12.5V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5V$.

PROGRAM INHIBIT

Programming of multiple ST27128APs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M27128BA may be common. A TTL low pulse applied to a ST27128AP's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that ST27128AP. A high level $\overline{CE}$ input inhibits the other ST27128AP from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5V.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the ST27128AP. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the ST27128AP. Two identifier bytes may than be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON ST27128AP, these two identifier bytes are given below. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ELECTRONIC SIGNATURE MODE

PINS / IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	1	0	0	0	1	0	0	1	89

PROGRAMMING OPERATION (T_{amb} = 25°C ±5°C, $V_{CC}^{(1)}$ = 6V ±0.25V, $V_{PP}^{(1)}$ = 12.5V ±0.3V)

DC AND OPERATING CHARACTERISTIC

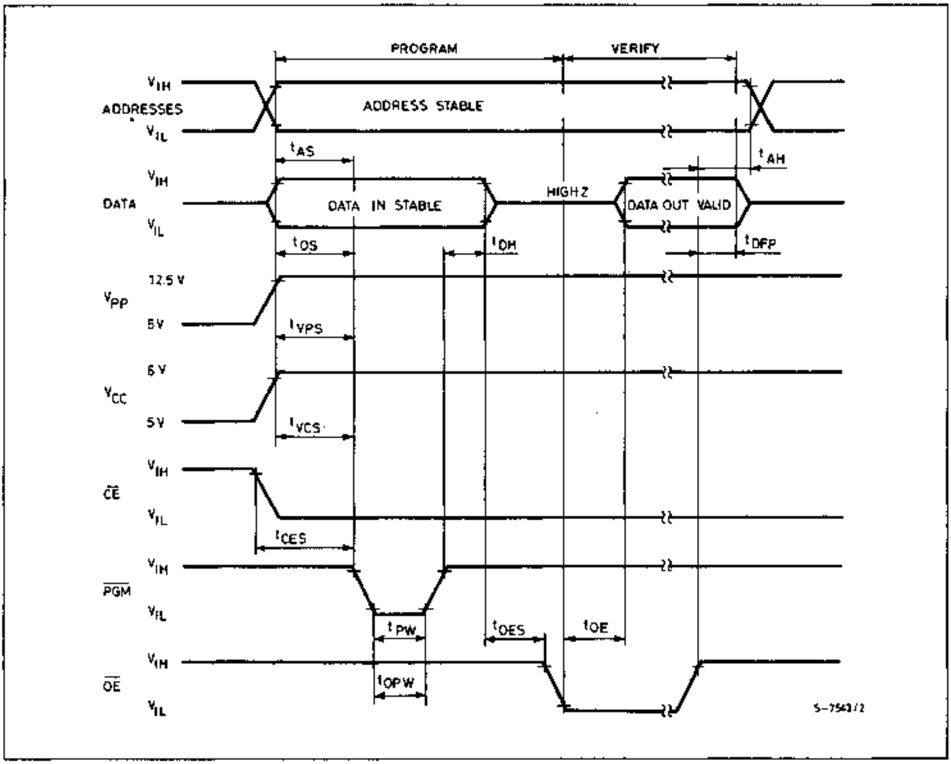
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 μA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
$t_{DFP}^{(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{CES}	CE Setup Time		2			μs
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

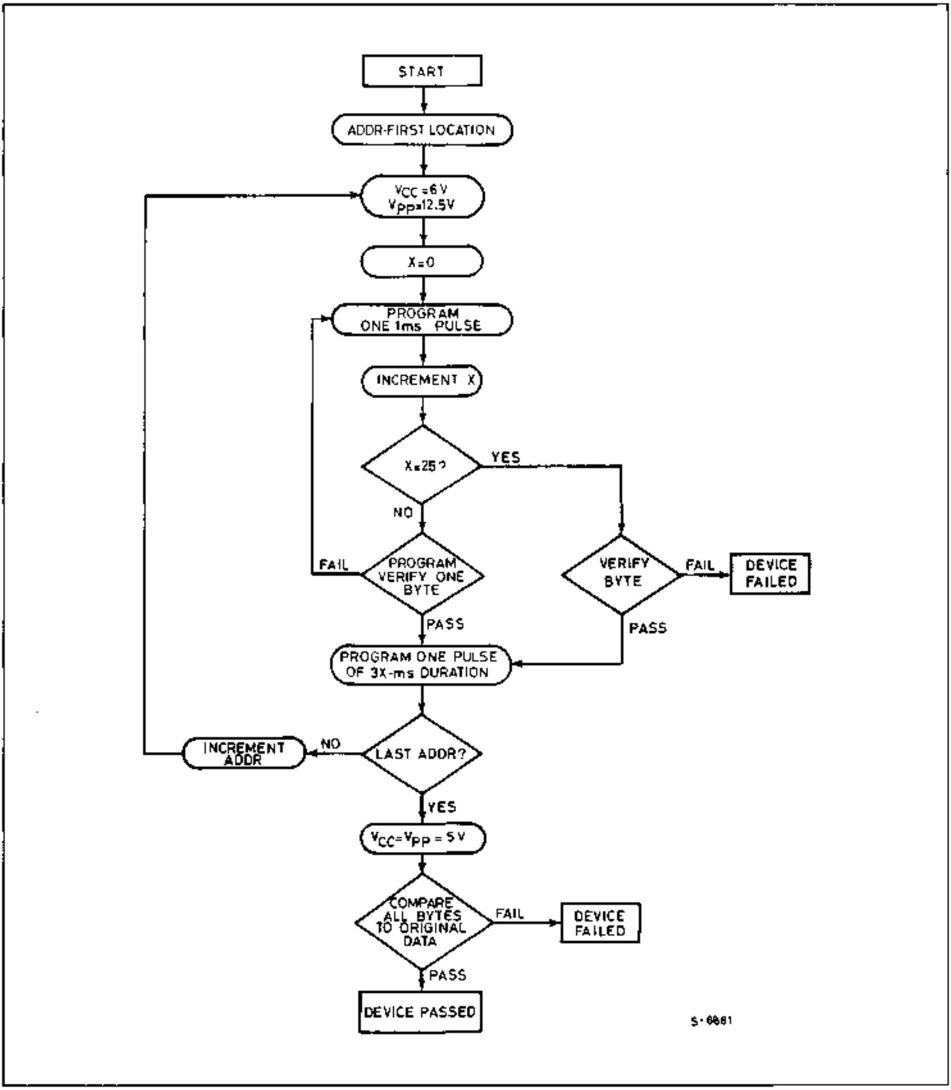
PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_IH
V_IL
ADDRESS STABLE
t_AS
t_AH
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_DS
t_DH
t_DFP
V_PP
12.5 V
5 V
t_VPS
V_CC
6 V
5 V
t_VCS
CE
t_CES
PGM
t_PW
t_OES
t_OE
OE
t_OPW
S-7543/2

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the ST27128AP a 0.1µF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

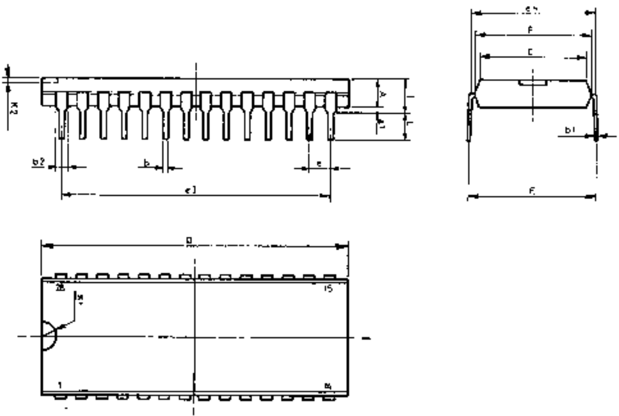

START
ADDR-FIRST LOCATION
V_{CC} = 6 V
V_{PP} = 12.5 V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
LAST ADDR?
NO
INCREMENT ADDR
YES
V_{CC} = V_{PP} = 5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S - 6881

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27128A-15XCP	150 ns	5V ± 5%	0 to +70°C	DIP-28
ST27128A-20XCP	200 ns	5V ± 5%	0 to +70°C	DIP-28
ST27128A-20CP	200 ns	5V ± 10%	0 to +70°C	DIP-28
ST27128A-25CP	250 ns	5V ± 10%	0 to +70°C	DIP-28
ST27128A-30CP	300 ns	5V ± 10%	0 to +70°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

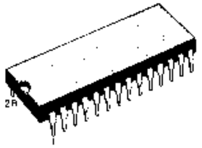
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

SGS-THOMSON
MICROELECTRONICS

ST27256P

256K (32K × 8) NMOS ONE TIME PROGRAMMABLE ROM

- FAST ACCESS TIME: 170ns
- 0 to +70°C STANDARD TEMP. RANGE
- SINGLE +5V POWER SUPPLY
- ±10% V_{CC} TOLERANCE AVAILABLE
- LOW STANDBY CURRENT (40mA MAX)
- TTL COMPATIBLE DURING READ AND PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE



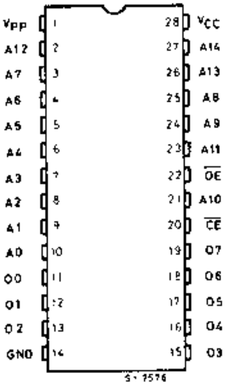
B
DIP-28
(Plastic Package)

(Ordering information at the end of the datasheet)

DESCRIPTION

The ST27256P is a 262,144-bit one time programmable read only memory (OTP ROM). It is organized as 32.768 words by 8 bits and manufactured using SGS-THOMSON' NMOS-E3 process. The ST27256P with its single +5V power supply and with an access time of 200ns, is ideal for use with high performance +5V microprocessor such as Z8, Z80 and Z8000. The ST27256P has an important feature which is to separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. The ST27256P also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40 mA, a 60% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input. The ST27256P enables implementation of new, advanced systems with firmware intensive architectures. The combination of the ST27256P's high density, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems. The ST27256P large storage capability enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a ST27256P directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads. The ST27256P has an "Electronic Signature" that allows programmers to automatically identify device type and pinout.

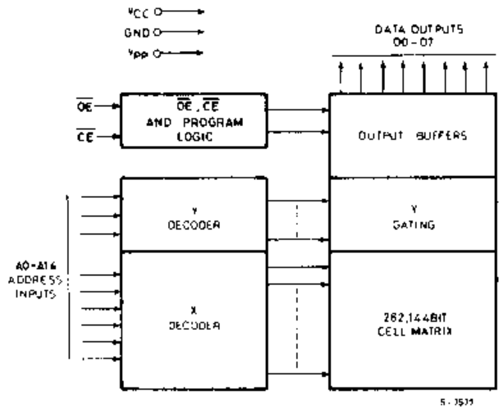
PIN CONNECTIONS



PIN NAMES

A0-A14	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
O0-O7	DATA INPUT/OUTPUT

BLOCK DIAGRAM


VCC
GND
VPP
DATA OUTPUTS
O0 - O7
$\overline{OE}$
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$ AND PROGRAM LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A14 ADDRESS INPUTS
X DECODER
262,144BIT CELL MATRIX
5-3535

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+6.25 to −0.6	V
V_{PP}	Supply voltage with respect to ground	+14 to −0,6	V
T_{amb}	Ambient temperature under bias	−10 to +80	°C
T_{stg}	Storage temperature range	−65 to +125	°C
	Voltage on pin 24 with respect to ground	+13.5 to −0.6	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	A0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
READ	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{IN}
VERIFY	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
OPTIONAL VERIFY	V_{IL}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z
ELECTRONIC SIGNATURE	V_{IL} V_{IL}	V_{IL} V_{IL}	V_H V_H	V_{IL} V_{IH}	V_{CC} V_{CC}	V_{CC} V_{CC}	MAN.CODES DEV.CODE

NOTE: X can be V_{IH} or V_{IL} V_H = 12V ±0.5V

READ OPERATION

DC AND AC CONDITIONS

Selection Code	−17X/−20X	−20/−25/−30
Operating Temperature Range	0 to 70°C	0 to 70°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ. (3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
$I_{PP1(2)}$	V_{PP} Current Read Standby	$V_{PP} = 5.5V$			5	mA
$I_{CC1(2)}$	V_{CC} Current Standby	$\overline{CE} = V_{IH}$		20	40	mA
$I_{CC2(2)}$	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$ $V_{PP} = V_{CC}$		45	100	mA
V_{IL}	Input Low Voltage		−0.1		+0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
$V_{PP(2)}$	V_{PP} Read Voltage	$V_{CC} = 5V \pm 0.25V$	3.8		V_{CC}	V

AC CHARACTERISTICS

Symbol	Parameter	$V_{CC}\pm$ 5%	27256-17X		27256-20X						Unit
		$V_{CC}\pm 10\%$			27256-20		27256-25		27256-30		
		Test Conditions	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		70		75		100		120	ns
$t_{DF(4)}$	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$		35	0	55	0	60	0	105	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

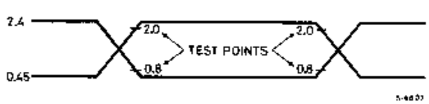
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

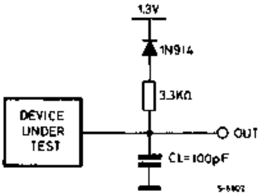
READ OPERATION (Continued)

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

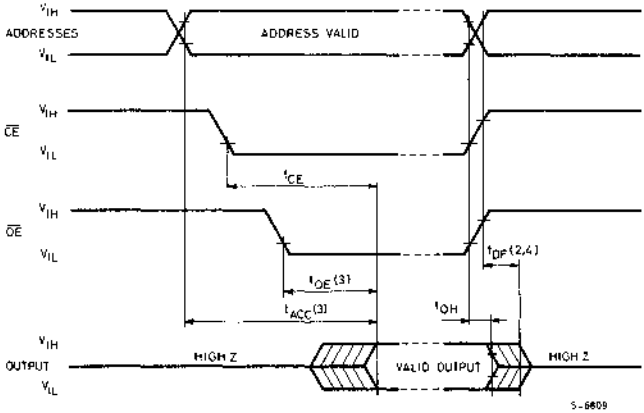

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6607

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6602

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


VIH
ADDRESSES
VIL
ADDRESS VALID
VIH
CE
VIL
tCE
VIH
OE
VIL
tDF (2,4)
tOE (3)
tACC (3)
tOH
VIH
OUTPUT
VIL
HIGH Z
VALID OUTPUT
HIGH Z
S-6609

Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The eight modes of operations of the ST27256P are listed in the Operating Modes. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

READ MODE

The ST27256P has two control function, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ST27256P has a standby mode which reduces the maximum active power current from 100 mA to 40 mA. The ST27256P is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

TWO LINE OUTPUT CONTROL

Because OTPs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of NMOS-E3 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

PROGRAMMING

Caution: exceeding 13V on pin 1 (V_{PP}) will damage the ST27256P.

When delivered, all bits of the ST27256P are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The ST27256P is in the programming mode when V_{PP} input is at 12.5V and $\overline{CE}$ and is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs ST27256P EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the ST27256P Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 3Xmsec. (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular ST27256P location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at V_{CC}=6V and V_{PP}=12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V_{CC}=V_{PP}=5V.

DEVICE OPERATION (Continued)

PROGRAM INHIBIT

Programming of multiple ST27256Ps in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ST27256P may be common. A TTL low pulse applied to a ST27256P's $\overline{CE}$ input, with V_{PP} at 12.5V, will program that ST27256P. A high level $\overline{CE}$ input inhibits the other ST27256Ps from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

OPTIONAL VERIFY

The optional verify may be performed instead of the verify mode. It is performed with $\overline{OE}$ at V_{IL}, $\overline{CE}$ at V_{IL} (as opposed to the standard verify which has $\overline{CE}$ at V_{IH}), and V_{PP} at 12.5V. The outputs will three-state according to the signal presented to $\overline{OE}$. Therefore, all devices with $V_{PP} = 12.5V$ and $\overline{OE} = V_{IL}$ will present data on the bus independent of the $\overline{CE}$ state. When parallel programming several devices which share the common bus, V_{PP} should be lowered to V_{CC} (=6V) and the normal read mode used to execute a program verify.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the ST27256P. To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the ST27256P.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the SGS-THOMSON ST27256P, these two identifier bytes are given below.

All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

ELECTRONIC SIGNATURE MODE

PINS IDENTIFIER	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE CODE	V_{IH}	0	0	0	0	0	1	0	0	04

PROGRAMMING OPERATION ($T_{amb} = 25°C \pm 5°C$, $V_{CC}^{(1)} = 6V \pm 0.25V$, $V_{PP}^{(1)} = 12.5V \pm 0.3V$

DC AND OPERATING CHARACTERISTIC:

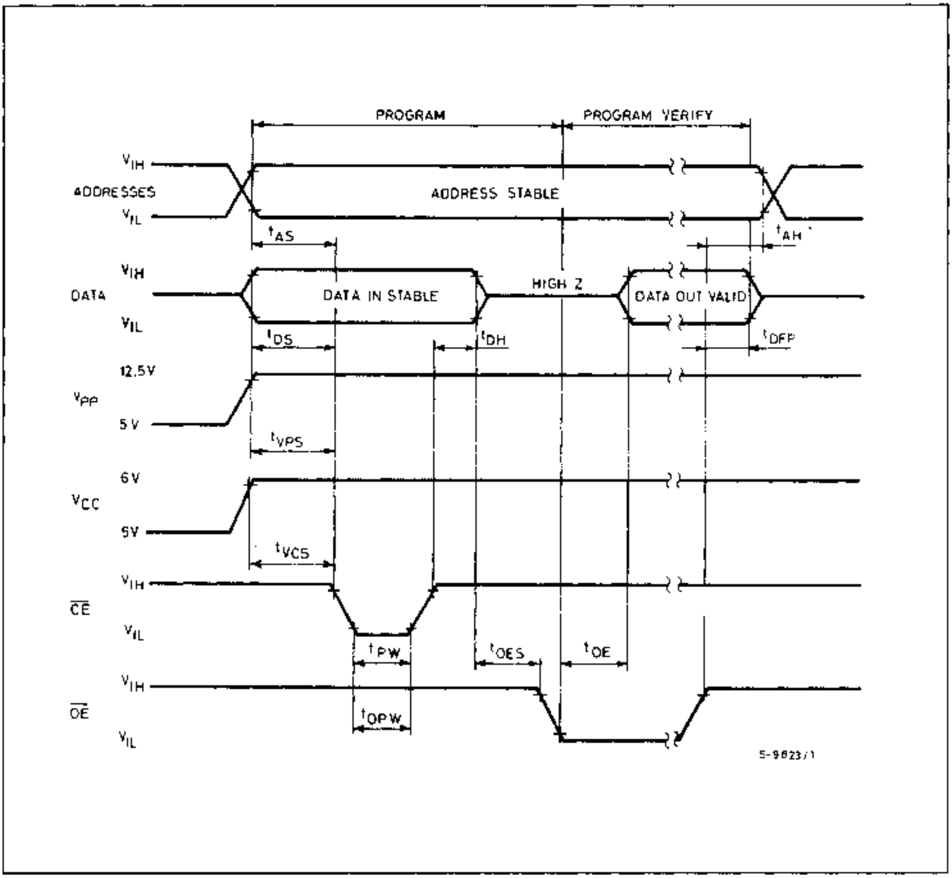
Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (All Inputs)		–0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Program & Verify)				100	mA
I_{PP2}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$			50	mA
V_{ID}	A9 Electronic Signature Voltage		11.5		12.5	V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 1)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
$t_{DFP(4)}$	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	(see Note 3)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see Note 2)	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
3. Initial Program Pulse width tolerance is 1msec ±5%.
4. This parameter is only sampled and not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

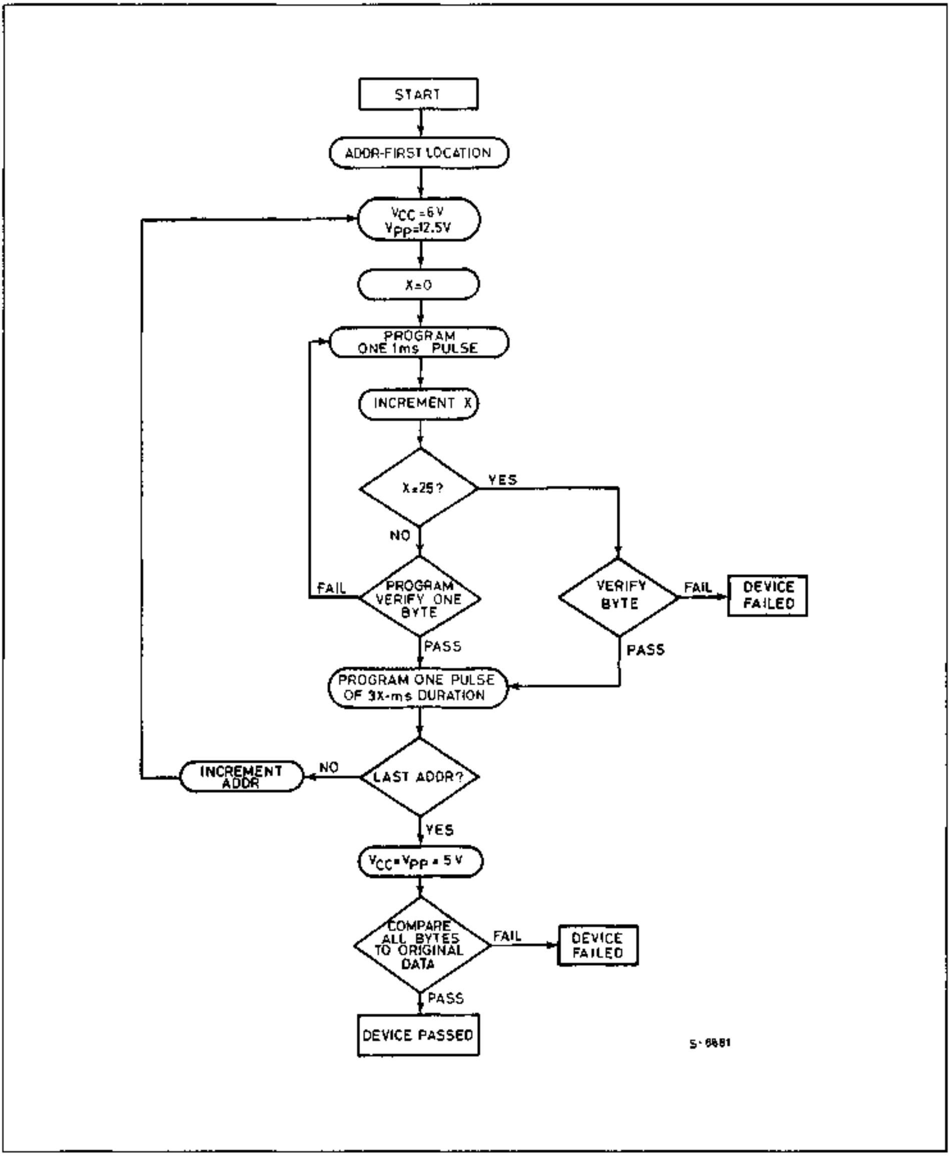
PROGRAMMING WAVEFORMS


PROGRAM
PROGRAM VERIFY
V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
V_{IH}
DATA
V_{IL}
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
12.5V
V_{PP}
5 V
t_{VPS}
6 V
V_{CC}
5V
t_{VCS}
V_{IH}
$\overline{CE}$
V_{IL}
t_{PW}
t_{OES}
t_{OE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{OPW}
5-9823/1

Notes:

1. The input timing reference level is 0.8V for a V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the ST27256P a 0.1μF capacitor is required across V_{PP} and GROUND to suppress spurious voltage transients which can damage the device.

FAST PROGRAMMING FLOWCHART

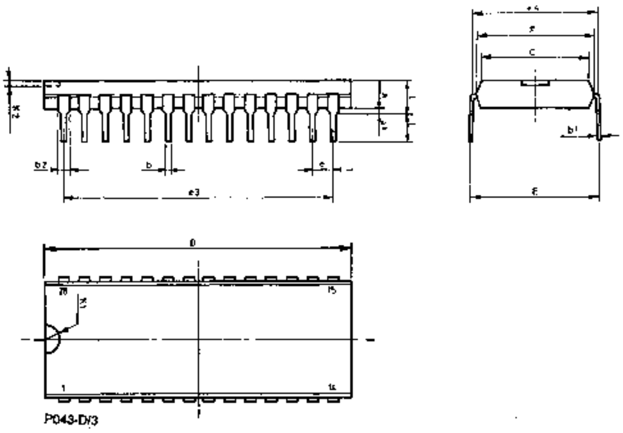

START
ADDR-FIRST LOCATION
V_{CC} = 6V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25?
YES
NO
PROGRAM VERIFY ONE BYTE
FAIL
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
LAST ADDR?
NO
INCREMENT ADDR
YES
V_{CC} = V_{PP} = 5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S-6681

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27256-17XCP	170 ns	5V ± 5%	0 to +70°C	DIP-28
ST27256-20XCP	200 ns	5V ± 5%	0 to +70°C	DIP-28
ST27256-20CP	200 ns	5V ± 10%	0 to +70°C	DIP-28
ST27256-25CP	250 ns	5V ± 10%	0 to +70°C	DIP-28
ST27256-30CP	300 ns	5V ± 10%	0 to +70°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

EPROM DEVICES

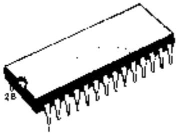
CMOS OTP ROM

SGS-THOMSON
MICROELECTRONICS

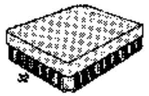
TS27C64AFN
TS27C64AP

64K (8K × 8) CMOS ONE TIME PROGRAMMABLE ROM

- COMPATIBLE TO TS27C64A EPROM (ELECTRICAL PARAMETERS, PROGRAMMING)
- PROGRAMMING VOLTAGE 12.5V
- HIGH SPEED PROGRAMMING
- 28-PIN JEDEC APPROVED PIN-OUT
- 32-PIN JEDEC APPROVED PIN-OUT (PLCC)
- IDEAL FOR AUTOMATIC INSERTION



P
DIP-28
(Plastic Package)



FN
PLCC32
(Plastic Chip Carrier)

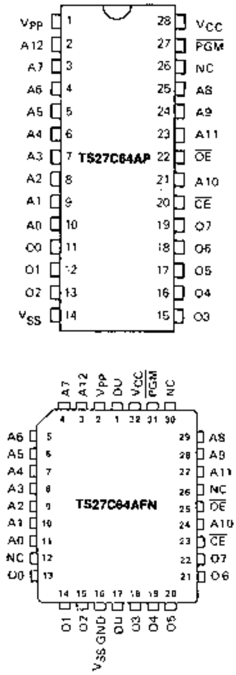
(Ordering Information at the end of the datasheet)

DESCRIPTION

The TS27C64AP and TS27C64AFN are high speed 65,536-bit One Time Programmable (OTP) CMOS ROM ideally suited for applications where fast turnaround is an important requirement.

The TS27C64AP is packaged in a 28-pin dual-in-line plastic package, the TS27C64AFN in a 32-pin PLCC plastic package and therefore can not be rewritten. Programming is performed according to standard SGS-THOMSON 64K EPROM procedure.

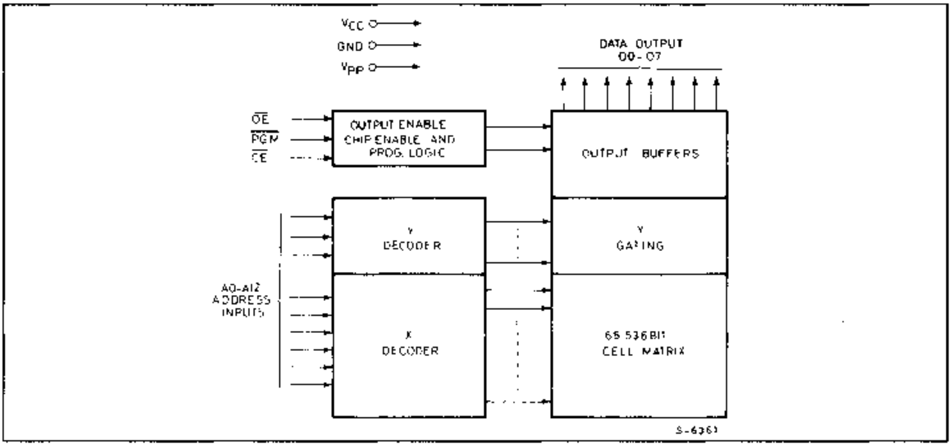
PIN CONNECTIONS


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
VSS 14
28 VCC
27 PGM
26 NC
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3
TS27C64AP
A7 4
A12 3
VPP 2
DU 1
VCC 32
PGM 31
NC 30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
O0 13
29 A8
28 A9
27 A11
26 NC
25 OE
24 A10
23 CE
22 O7
21 O6
TS27C64AFN
14 O1
15 O2
16 VSS GND
17 DU
18 O3
19 O4
20 O5

PIN NAMES

A0—A12	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
NC	NON CONNECTED
DU	DO NOT USE

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
DATA OUTPUT
O0 - O7
$\overline{OE}$
$\overline{PGM}$
$\overline{CE}$
OUTPUT ENABLE CHIP ENABLE AND PROG. LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A12 ADDRESS INPUTS
X DECODER
65 536 BIT CELL MATRIX
S-6361

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
T_{amb}	Operating temperature range TS27C64A-C TS27C64A-V TS27C64A-T	T_L to T_H 0 to + 70 − 40 to + 85 − 40 to + 105	°C
T_{stg}	Storage temperature range	− 65 to + 125	°C
V_{PP}(2)	Supply voltage	− 0.6 to + 14	V
V_{IN}(2)	Input voltages A9 Except V_{PP}, A9	− 0.6 to + 13.5 − 0.6 to + 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

Notes: 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to GND

OPERATING MODES

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	A9	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{IH}	V_{CC}	V_{CC}	Hi-Z
STANDBY	V_{IH}	X	X	X	V_{CC}	V_{CC}	Hi-Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	X	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	X	V_{PP}	V_{CC}	Hi-Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	CODE

Notes: 1. X can be either V_{IL} or V_{IH} — 2. $V_H = 12.0V \pm 0.5V$
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 08).

EAD OPERATION

C CHARACTERISTICS ($T_{amb} = T_L$ to T_H, $V_{CC} = 5V \pm 10\%$, GND = 0V; Unless otherwise specified)

ymbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.[1]	Max.	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC} - 0.7$		V_{CC}	V
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $I_{OL} = 0$ µA			0.45 0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA $I_{OH} = 0$ µA	2.4 $V_{CC} - 0.1$			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE} = \overline{OE} = V_{IL}$, Inputs = V_{IH} or V_{IL}, f = 5 MHz, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE} = V_{IH}$		0.5	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE} = V_{CC}$		10	100	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{CC} = 5.5V$			100	µA

Note: 1. Typical conditions are for operation at: $T_{amb} = +25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$

AC CHARACTERISTICS(1)($T_{amb} = T_L$ to T_H)

Symbol	Parameter	Test Conditions	27C64A -15		27C64A -20		27C64A -25		27C64A -30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250		300	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		80		100		120	ns
t_{DF}(2,4)	$\overline{OE}$ or $\overline{CE}$ High to	$\overline{CE} = V_{IL}$	0	50	0	50	0	60	0	105	ns
t_{OH}	Output Hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE $T_{amb} = +25°C$, f = 1 MHz (Note 3)

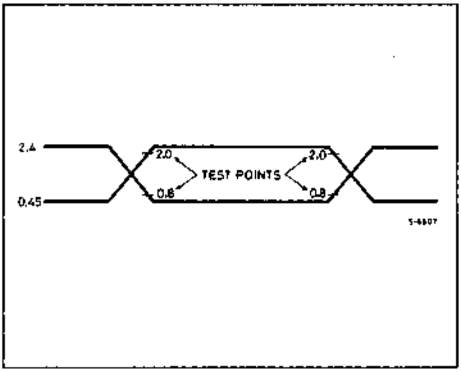
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{out}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied at the same time or before Vpp and removed after or at the same time as Vpp•Vpp may be connected to V_{CC} except during program.
2. The t_{DF} compare level is determined as follows:
High to THREE-STATE, the measured V_{OH}(DC) −0.1V
Low to THREE-STATE the measured V_{OL}(DC) +0.1V.
3. Capacitance is guaranteed By periodic testing. $T_{amb} = +25°C$, f = 1MHz.
4. T_{DF}, is specified from OE or CE whichever occurs first. This parameter is only sampled and not 100% tested.

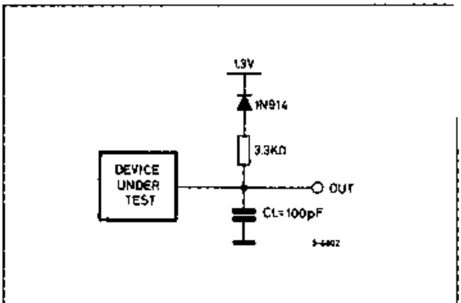
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

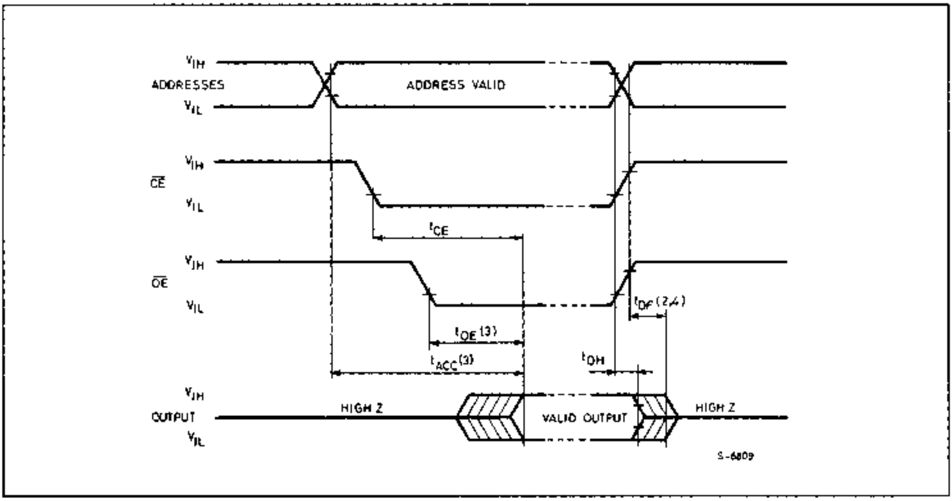

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
S-6807

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL=100pF
S-6802

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
$\overline{CE}$
$\overline{OE}$
t_{CE}
t_{OE} (3)
t_{ACC} (3)
t_{OH}
t_{DF} (2,4)
OUTPUT
HIGH Z
VALID OUTPUT
HIGH Z
S-6809

Notes:

1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the TS27C64A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

READ MODE

The TS27C64A has two control functions, both of wich must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to Output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The TS27C64A has a standby mode which reduces the maximum power dissipation to 5.5 mW. The TS27C64A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because OTPs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING

Caution: Exceeding 14V on V_{PP} pin will damage the TS27C64A.

Initially, all bits of the TS27C64A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word.

The TS27C64A is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. It is required that a 0.1 µF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple TS27C64As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel TS27C64As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled TS27C64As.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flow chart rapidly programs TS27C64A using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 1 minute.

PROGRAM INHIBIT

Programming of multiple TS27C64As in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ or $\overline{PGM}$ inputs inhibits the other TS27C64As from from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel TS27C64As may be common. A TTL low-level pulse applied to a TS27C64A $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at 12.5 V will program that TS27C64A.

PROGRAM VERIFY

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{CE}$ and $\overline{OE}$ at V_{IL}, $\overline{PGM}$ at V_{IH} and V_{PP} at 12.5 V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will indentify the EPROM manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the TS27C64A. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 of the TS27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electonic signature mode.

PROGRAMMING OPERATIONS[1] ($T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (all inputs)		– 0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -400$ µA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				30	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL} = \overline{PGM}$			30	mA

AC CHARACTERISTICS

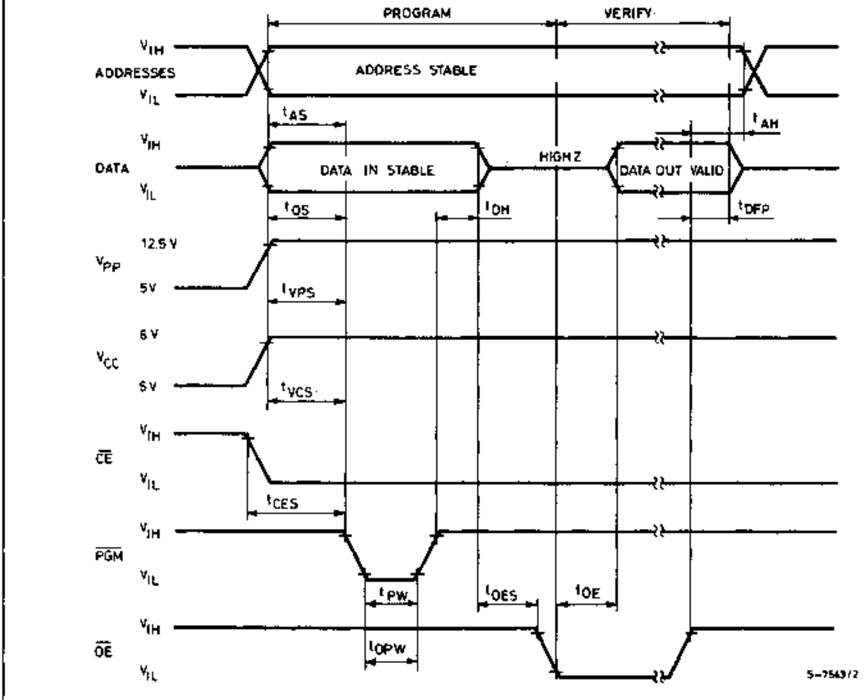
Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set-up Time		2			µs
t_{OES}	$\overline{OE}$ Set-up Time		2			µs
t_{DS}	Data Set-up Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			µs
t_{VCS}	V_{CC} set-up time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{PGM}$ overprogram pulse width		2.85		78.75	ms
t_{CES}	$\overline{CE}$ set-up time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

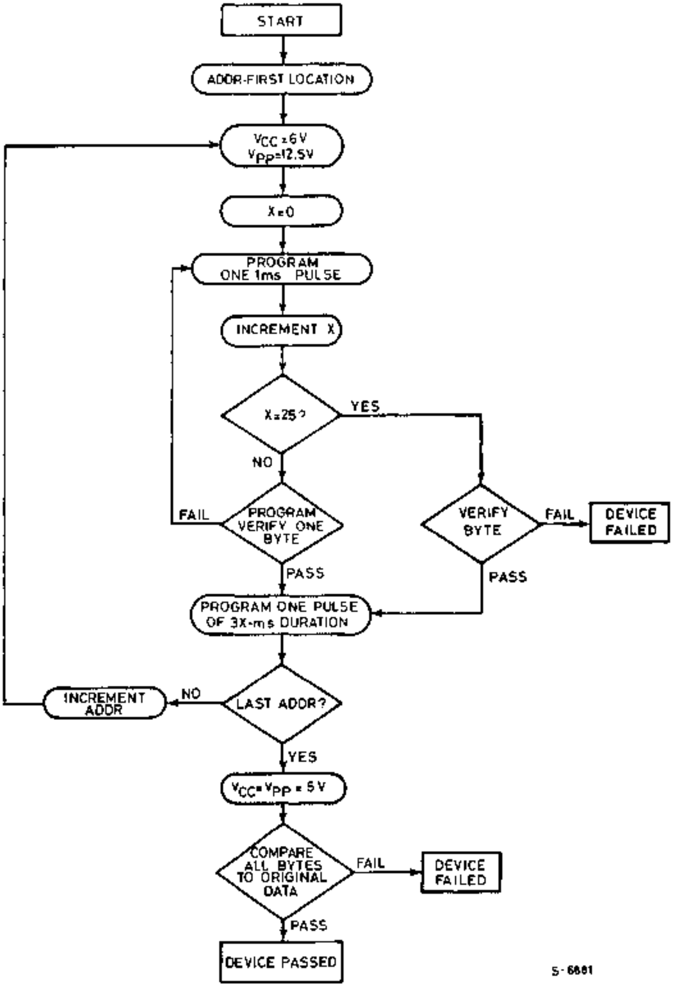
Input rise and fall times (10% to 90%)	20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Output timing reference level	0.8V and 2.0V

HIGH SPEED PROGRAMMING WAVEFORMS


PROGRAM
VERIFY
ADDRESSES
V_{IH}
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
DATA
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
V_{PP}
12.5 V
5V
t_{VPS}
V_{CC}
6 V
5 V
t_{VCS}
$\overline{CE}$
t_{CES}
$\overline{PGM}$
t_{PW}
t_{OPW}
t_{OES}
t_{OE}
$\overline{OE}$
5-7543/2

1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be be accommodated by the programmer.
3. When programming the TS27C64A, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transiens which can damage the device.

HIGH SPEED PROGRAMMING FLOW CHART

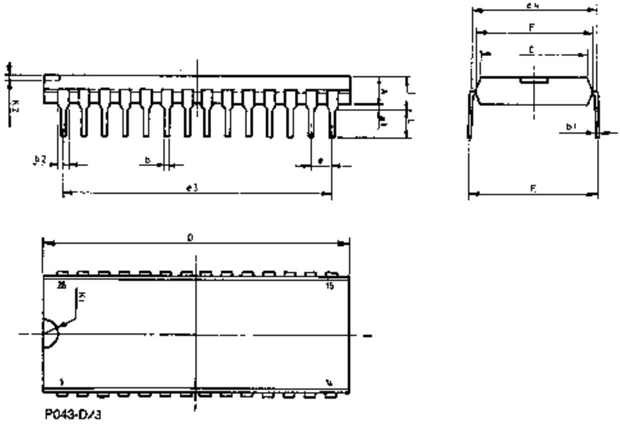

START
ADDR-FIRST LOCATION
V_{CC} = 6V
V_{PP} = 12.5V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR?
YES
V_{CC} = V_{PP} = 5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
5-6881

ORDERING INFORMATION (TS27C64AP)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-15CP	150 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-20CP	200 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-25CP	250 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-30CP	300 ns	5V ± 10%	0 to + 70°C	DIP-28
TS27C64A-15VP	150 ns	5V ± 10%	– 40 to + 85°C	DIP-28
TS27C64A-20VP	200 ns	5V ± 10%	– 40 to + 85°C	DIP-28
TS27C64A-25VP	250 ns	5V ± 10%	– 40 to + 85°C	DIP-28
TS27C64A-30VP	300 ns	5V ± 10%	– 40 to + 85°C	DIP-28
TS27C64A-15TP	150 ns	5V ± 10%	– 40 to + 105°C	DIP-28
TS27C64A-20TP	200 ns	5V ± 10%	– 40 to + 105°C	DIP-28
TS27C64A-25TP	250 ns	5V ± 10%	– 40 to + 105°C	DIP-28
TS27C64A-30TP	300 ns	5V ± 10%	– 40 to + 105°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

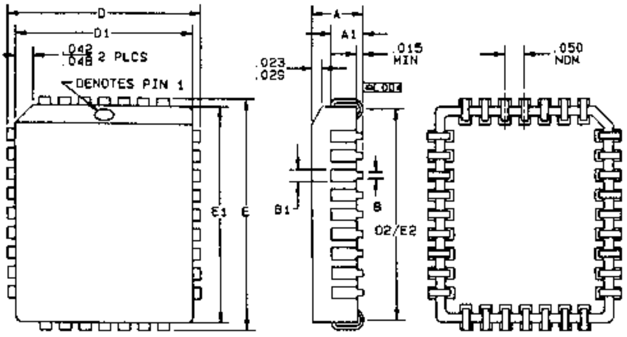
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

ORDERING INFORMATION (TS27C64AFN)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
TS27C64A-15CFN	150 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-20CFN	200 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-25CFN	250 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-30CFN	300 ns	5V ± 10%	0 to + 70°C	PLCC32
TS27C64A-15VFN	150 ns	5V ± 10%	− 40 to + 85°C	PLCC32
TS27C64A-20VFN	200 ns	5V ± 10%	− 40 to + 85°C	PLCC32
TS27C64A-25VFN	250 ns	5V ± 10%	− 40 to + 85°C	PLCC32
TS27C64A-30VFN	300 ns	5V ± 10%	− 40 to + 85°C	PLCC32
TS27C64A-15TFN	150 ns	5V ± 10%	− 40 to + 105°C	PLCC32
TS27C64A-20TFN	200 ns	5V ± 10%	− 40 to + 105°C	PLCC32
TS27C64A-25TFN	250 ns	5V ± 10%	− 40 to + 105°C	PLCC32
TS27C64A-30TFN	300 ns	5V ± 10%	− 40 to + 105°C	PLCC32

PACKAGE MECHANICAL DATA

PLCC32 32-LEAD PLASTIC LEADED CHIP CARRIER



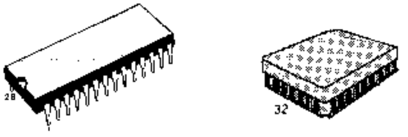
Dim.	mm		Inches	
	Min	Max	Min	Max
A	3.04	3.56	.120	.140
A 1	1.98	2.41	.078	.095
B	0.33	0.53	.013	.021
B 1	0.66	0.81	.026	.032
D	12.31	12.57	.485	.495
D1	11.35	11.50	.447	.453
D2	9.90	10.92	.390	.430
E	14.85	15.11	.585	.595
E1	13.89	14.04	.547	.553
E2	12.44	13.46	.490	.530

SGS-THOMSON
MICROELECTRONICS

ST27C256FN
ST27C256P

256K (32K × 8) CMOS ONE TIME PROGRAMMABLE ROM

- COMPATIBLE TO ST27C256 EPROM (ELECTRICAL PARAMETER, PROGRAMMING)
- PROGRAMMING VOLTAGE 12.5V.
- HIGH SPEED PROGRAMMING
- 28-PIN JEDEC APPROVED PIN-OUT
- 32-PIN JEDEC APPROVED PIN OUT
- IDEAL FOR AUTOMATIC INSERTION



P
DIP-28
(Plastic Package)

FN
PLCC32
(Plastic Chip Carrier)

(Ordering Information at the end of the datasheet)

DESCRIPTION

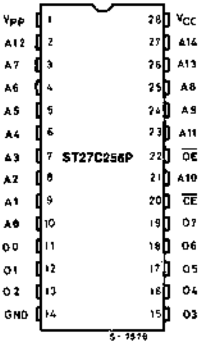
The ST27C256P and ST27C256FN are high speed 262,144K bit One Time Programmable (OTP) CMOS ROM ideally suited for applications where fast turn-around is an important requirement.

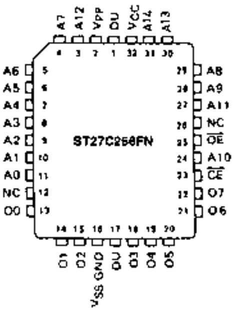
The ST27C256P is packaged in a 28-pin dual-in-line plastic package, the ST27C256FN in a 32-pin PLCC plastic package, and therefore can not be re-written. Programming is performed according to standard SGS-THOMSON 256K EPROM procedure.

PIN NAMES

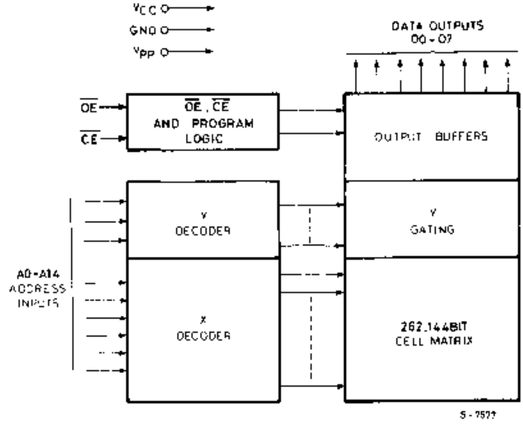
A0—A14	ADDRESS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
NC	NON CONNECTED
DU	DO NOT USE

PIN CONNECTIONS


VPP 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
ST27C256P
28 VCC
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3
S-7576


A7 4
A12 3
VPP 2
DU 1
VCC 32
A14 31
A13 30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
O0 13
ST27C256FN
29 A8
28 A9
27 A11
26 NC
25 OE
24 A10
23 CE
22 O7
21 O6
14 O1
15 O2
16 VSS GND
17 DU
18 O3
19 O4
20 O5

BLOCK DIAGRAM


V_{CC}
GND
V_{PP}
DATA OUTPUTS
O0 - O7
$\overline{OE}$
$\overline{CE}$
$\overline{OE}$, $\overline{CE}$ AND PROGRAM LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0-A14 ADDRESS INPUTS
X DECODER
262,144BIT CELL MATRIX
S - 7577

MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
T_{amb}	Operating temperature range ST27C256-C ST27C256-V ST27C256-T	T_L to T_H 0 to + 70 – 40 to + 85 – 40 to + 105	°C
T_{stg}	Storage temperature range	+ 65 to + 125	°C
V_{PP}(2)	Supply voltage	– 0.6 to + 14	V
V_{in}(2)	Input voltages A9 Except V_{PP}, A9	– 0.6 to + 13.5 – 0.6 to + 6.25	V
P_D	Max power dissipation	1.5	W
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

Notes: 1. "Maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating temperature range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical characteristics" provides conditions for actual device operation.
2. With respect to V_{SS}

OPERATING MODES

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	OUTPUTS
READ	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
OUTPUT DISABLE	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	Hi-Z
STANDBY	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
HIGH SPEED PROGRAMMING	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
ELECTRONIC SIGNATURE(3)	V_{IL}	V_{IL}	V_H (2)	V_{CC}	V_{CC}	CODE

Notes: 1. X can be either V_{IL} or V_{IH} — 2 - $V_H = 12.0V \pm 0.5V$
3. All address lines at V_{IL} except A9 and A0 that is toggled from V_{IL} (manufacturer code: 9B) to V_{IH} (type code: 04).

READ OPERATION

DC CHARACTERISTICS ($T_{amb} = T_L$ to T_H, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.[1]	Max.	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}, $\overline{CE} = V_{IH}$			10	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC} - 0.7$		V_{CC}	V
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $I_{OL} = 0$ µA			0.45 0.1	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ µA $I_{OH} = 0$ µA	2.4 $V_{CC} - 0.1$			V
I_{CC2}	V_{CC} Supply Active Current TTL Levels	$\overline{CE} = \overline{OE} = V_{IL}$, Inputs $= V_{IH}$ or V_{IL}, f = 5 MHz, I/O = 0 mA		10	30	mA
I_{CCSB1}	V_{CC} Supply Standby Current	$\overline{CE} = V_{IH}$ $\overline{OE}$ = Inputs		0.05	1	mA
I_{CCSB2}	V_{CC} Supply Standby Current	$\overline{CE} = V_{CC} - 0.1V$, $\overline{OE}$ = Inputs		1	10	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{CC} = 5.5V$			100	µA

Note: 1. Typical conditions are for operation at: $T_{amb} = +25°C$, $V_{CC} = 5V$, $V_{PP} = V_{CC}$, and $V_{SS} = 0V$

AC CHARACTERISTICS[1,2,3] ($T_{amb} = T_L$ to T_H)

Symbol	Parameter	Test Conditions	27C256 -17		27C256 -20		27C256 -25		27C256 -30		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		170		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		170		200		250		300	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		75		75		100		120	ns
t_{DF}[2][4]	$\overline{OE}$ or $\overline{CE}$ High to	$\overline{CE} = V_{IL}$	0	50	0	55	0	60	0	75	ns
t_{OH}	Output Hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occured first	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

CAPACITANCE $T_{amb} = +25°C$, f = 1 MHz

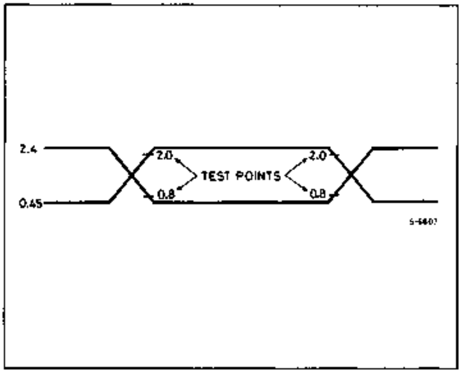
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{out}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

Notes: 1. V_{CC} must be applied at the same time or before V_{PP} and removed after or at the same time as V_{PP}·V_{PP} may be connected to V_{CC} except during program.
2. The t_{DF} compare level is determined as follows:
High to THREE-STATE, the measured V_{OH}(DC) $-0.1V$
Low to THREE-STATE the measured V_{OL}(DC) $+0.1V$.
3. Capacitance is guaranteed By periodic testing. $T_{amb} = +25°C$, f = 1MHz.
4. T_{DF}, is specified from OE or CE whichever occurs first. This parameter is only sampled and not 100% tested.

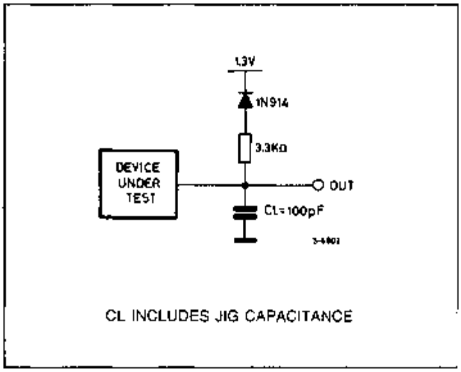
AC TEST CONDITIONS

Output Load:	1 TTL gate and CL = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input pulse levels:	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs, Outputs	0.8V and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

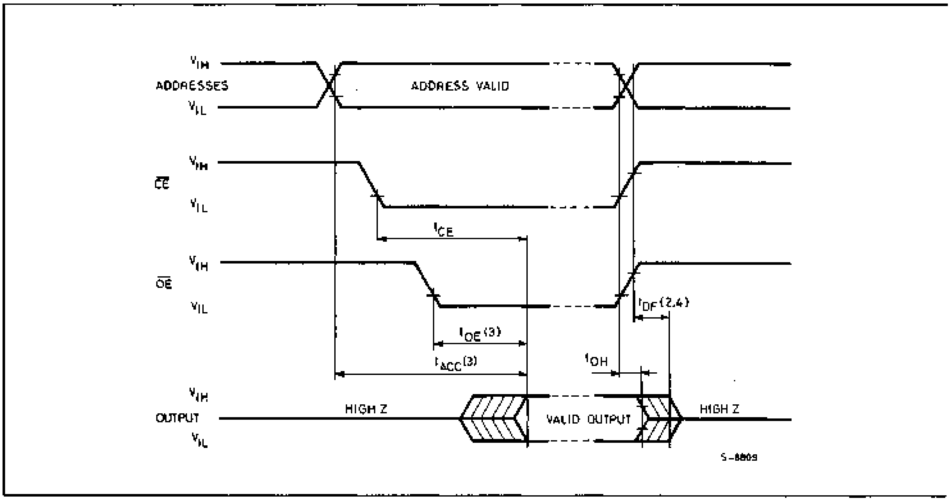

2.4
0.45
2.0
0.8
TEST POINTS
2.0
0.8
5-6607

AC TESTING LOAD CIRCUIT


1.3V
1N914
3.3KΩ
DEVICE UNDER TEST
OUT
CL = 100pF
5-6601

CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS


V_{IH}
ADDRESSES
V_{IL}
ADDRESS VALID
V_{IH}
$\overline{CE}$
V_{IL}
t_{CE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{DF} (2,4)
t_{OE} (3)
t_{ACC} (3)
t_{OH}
V_{IH}
OUTPUT
V_{IL}
HIGH Z
VALID OUTPUT
HIGH Z
5-6609

Notes:

1. Typical values are for $T_{amb} = 25°C$ and nominal supply voltage
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge $\overline{CE}$ without impact on t_{ACC}
4. $t_{DF}$is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

DEVICE OPERATION

The seven modes of operation of the ST27C256 are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

READ MODE

The ST27C256 has two control functions, both of wich must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to Output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The ST27C256 has a standby mode which reduces the maximum power dissipation to 5.25 mW. The ST27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TYING

Because OTPs are usually used in larger memory arrays, we have provided two control lines which accomodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To use these control lines most efficiently, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} pin will damage the ST27C256.

Initially, all bits of the ST27C256 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word.

The ST27C256 is in the programming mode when the V_{PP} input is at 12.5 V and $\overline{CE}$ and $\overline{PGM}$ are both at TTL Low. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Programming of multiple ST27C256s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled ST27C256s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled ST27C256s.

HIGH SPEED PROGRAMMING

The high speed programming algorithm described in the flow chart rapidly programs ST27C256 using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of 5 minute.

PROGRAM INHIBIT

Programming of multiple ST27C256s in parallel with different data is also easily accomplished by using the program inhibit mode. A high level on $\overline{CE}$ inputs inhibits the other ST27C256s from being programmed. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel ST27C256s may be common. A TTL low-level pulse applied to a ST27C256 $\overline{CE}$ input with V_{PP} at 12.5V will program that ST27C256.

PROGRAM VERIFY

A verify may be performed on the programmed bits to determine that they were correctly programmed. The verify is performed with $\overline{OE}$ at VIL, $\overline{CE}$ at V_{IH}, and V_{PP} at 12.5 V.

ELECTRONIC SIGNATURE MODE

Electronic signature mode allows the reading out of a binary code that will indentify the EPROMs manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the ST27C256. To activate this mode the programming equipment must force 11.5V to 12.5V on address line A9 of the ST27C256. Two bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during electonic signature mode.

PROGRAMMING CHARACTERISTICS ($T_{amb} = 25 \pm 5°C$, $V_{CC} = 6.0V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_I	Input Current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level (all inputs)		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -400$ µA	2.4			V
I_{CC3}	V_{CC} Supply current (Program & Verify)				40	mA
I_{PP2}	V_{PP} supply current (Program)	$\overline{CE} = V_{IL}$			30	mA

AC CHARACTERISTICS

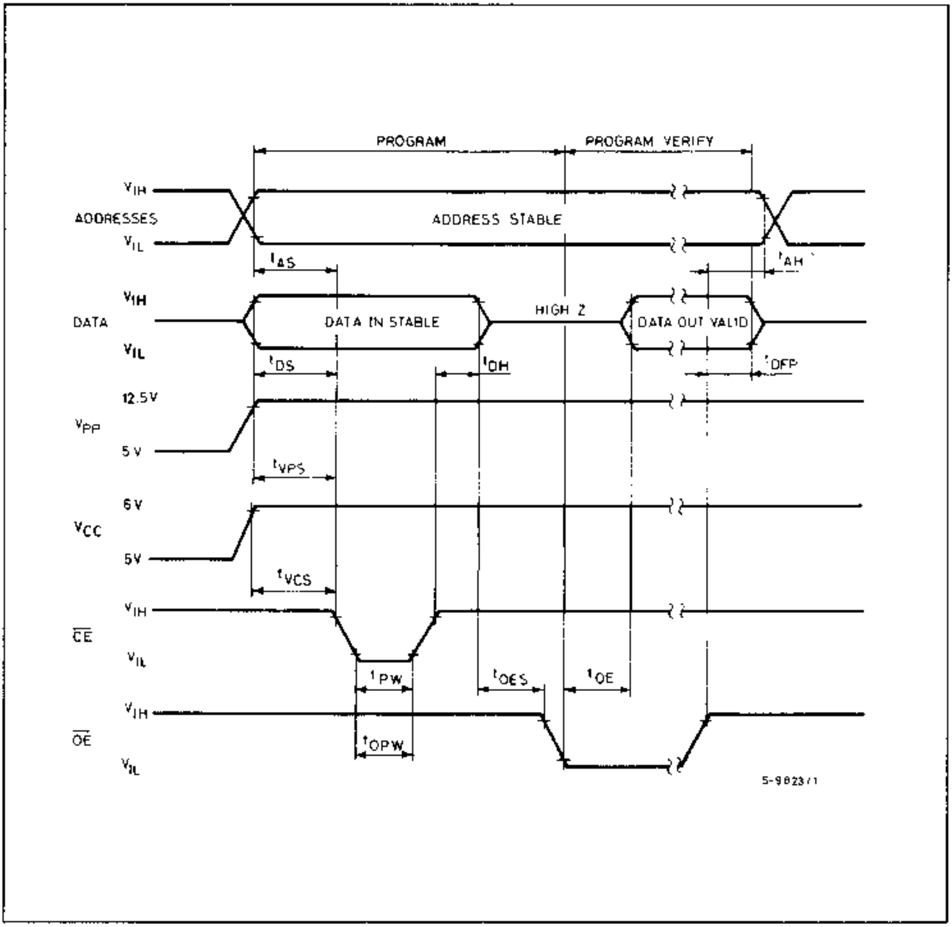
Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Set-up Time		2			µs
t_{OES}	$\overline{OE}$ Set-up Time		2			µs
t_{DS}	Data Set-up Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VPS}	V_{PP} set-up time		2			µs
t_{VCS}	V_{CC} set-up time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ overprogram pulse width		2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. t_{OPW} is defined in flow chart.

AC TEST CONDITIONS

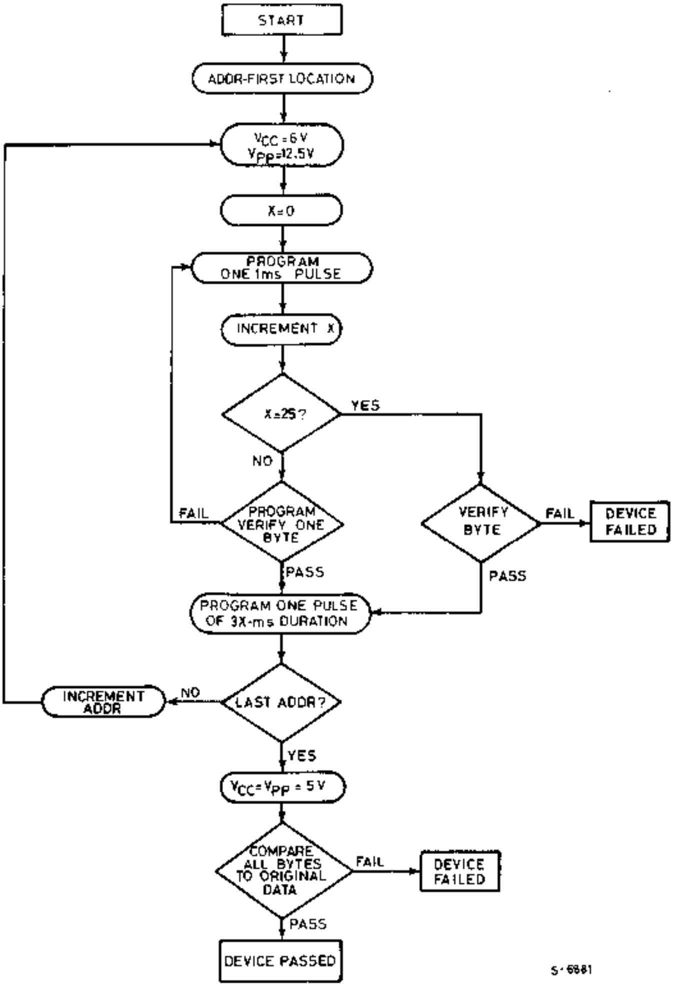
Input rise and fall times (10% to 90%)	≤20ns
Input pulse levels	0.45V to 2.4V
Input timing reference level	0.8V and 2.0V
Output timing reference level	0.8V and 2.0V

HIGH SPEED PROGRAMMING WAVEFORMS


PROGRAM
PROGRAM VERIFY
V_{IH}
ADDRESSES
V_{IL}
ADDRESS STABLE
t_{AS}
t_{AH}
V_{IH}
DATA
V_{IL}
DATA IN STABLE
HIGH Z
DATA OUT VALID
t_{DS}
t_{DH}
t_{DFP}
12.5V
V_{PP}
5 V
t_{VPS}
6 V
V_{CC}
5V
t_{VCS}
V_{IH}
$\overline{CE}$
V_{IL}
t_{PW}
t_{OES}
t_{OE}
V_{IH}
$\overline{OE}$
V_{IL}
t_{OPW}
5-9823/1

1. The input timing reference level is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be be accommodated by the programmer.
3. When programming the ST27C256, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transiens which can damage the device.

HIGH SPEED PROGRAMMING FLOW CHART

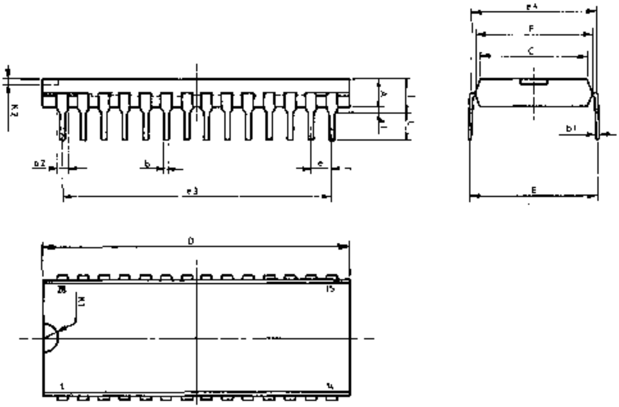

START
ADDR-FIRST LOCATION
VCC = 6 V
VPP = 12.5 V
X = 0
PROGRAM ONE 1ms PULSE
INCREMENT X
X = 25 ?
YES
NO
FAIL
PROGRAM VERIFY ONE BYTE
PASS
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PROGRAM ONE PULSE OF 3X-ms DURATION
INCREMENT ADDR
NO
LAST ADDR ?
YES
VCC = VPP = 5 V
COMPARE ALL BYTES TO ORIGINAL DATA
FAIL
DEVICE FAILED
PASS
DEVICE PASSED
S-6881

ORDERING INFORMATION (ST27C256P)

Part Number	Access Time	Supply Voltage	Temp. Range	Package
ST27C256-17CP	170 ns	5V ± 10%	0 to + 70°C	DIP-28
ST27C256-20CP	200 ns	5V ± 10%	0 to + 70°C	DIP-28
ST27C256-25CP	250 ns	5V ± 10%	0 to + 70°C	DIP-28
ST27C256-30CP	300 ns	5V ± 10%	0 to + 70°C	DIP-28
ST27C256-17VP	170 ns	5V ± 10%	− 40 to + 85°C	DIP-28
ST27C256-20VP	200 ns	5V ± 10%	− 40 to + 85°C	DIP-28
ST27C256-25VP	250 ns	5V ± 10%	− 40 to + 85°C	DIP-28
ST27C256-30VP	300 ns	5V ± 10%	− 40 to + 85°C	DIP-28
ST27C256-17TP	170 ns	5V ± 10%	− 40 to + 105°C	DIP-28
ST27C256-20TP	200 ns	5V ± 10%	− 40 to + 105°C	DIP-28
ST27C256-25TP	250 ns	5V ± 10%	− 40 to + 105°C	DIP-28
ST27C256-30TP	300 ns	5V ± 10%	− 40 to + 105°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



P043-D/3

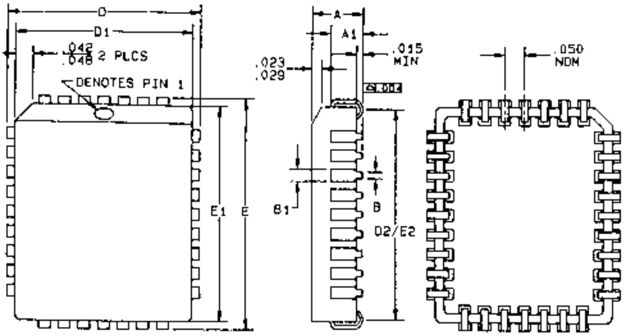
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

ORDERING INFORMATION (ST27C256FN)

Part Number	**Access Time**	**Supply Voltage**	**Temp. Range**	**Package**
ST27C256-17CFN	170 ns	5V ± 10%	0 to + 70°C	PLCC32
ST27C256-20CFN	200 ns	5V ± 10%	0 to + 70°C	PLCC32
ST27C256-25CFN	250 ns	5V ± 10%	0 to + 70°C	PLCC32
ST27C256-30CFN	300 ns	5V ± 10%	0 to + 70°C	PLCC32
ST27C256-17VFN	170 ns	5V ± 10%	− 40 to + 85°C	PLCC32
ST27C256-20VFN	200 ns	5V ± 10%	− 40 to + 85°C	PLCC32
ST27C256-25VFN	250 ns	5V ± 10%	− 40 to + 85°C	PLCC32
ST27C256-30VFN	300 ns	5V ± 10%	− 40 to + 85°C	PLCC32
ST27C256-17TFN	170 ns	5V ± 10%	− 40 to + 105°C	PLCC32
ST27C256-20TFN	200 ns	5V ± 10%	− 40 to + 105°C	PLCC32
ST27C256-25TFN	250 ns	5V ± 10%	− 40 to + 105°C	PLCC32
ST27C256-30TFN	300 ns	5V ± 10%	− 40 to + 105°C	PLCC32

PACKAGE MECHANICAL DATA

PLCC32-32-LEAD PLASTIC LEADED CHIP CARRIER



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.04	3.55	.120	.140
A 1	1.98	2.41	.078	.095
B	0.33	0.53	.013	.021
B 1	0.66	0.81	.026	.032
D	12.31	12.57	.485	.495
D1	11.35	11.50	.447	.453
D2	9.90	10.92	.390	.430
E	14.85	15.11	.585	.595
E1	13.89	14.04	.547	.553
E2	12.44	13.46	.490	.530

EEPROM DEVICES

NMOS EEPROM

M8571

1024 BIT SERIAL S-BUS/I²C BUS NMOS EEPROM

- 10 YEAR DATA RETENTION
- SINGLE +5V POWER SUPPLY
- AUTOMATIC POWER DOWN
- INTERNAL HIGH VOLTAGE AND SHAPING GENERATOR
- SELF TIMED E/W OPERATION
- AUTOMATIC ERASE BEFORE WRITE
- 3-WIRES S-BUS (I²C BUS COMPATIBLE)
- 2 CHIP SELECT FOR SIMPLE MEMORY EXTENSION
- SELF INCREMENTING ADDRESS REGISTER
- MULTI-MODE ADDRESSING (WHEN MS = V_{IH} ALLOWING:
  - PARTITIONING OF THE 1024 BITS INTO:
    - 128 x 8bit
    - 64 x 16bit
    - 32 x 32bit
  - OPCODE-LIKE ADDRESSES FOR:
    - halting of a modify operation
    - reading of the device "busy" status
    - "block erase" operation
    - reloading of the address register with the pre-increment value

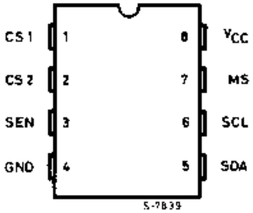
DESCRIPTION

The M8571 is a 1024-bit Electrically Erasable Programmable Read Only Memory (EEPROM). It allows partitioning of the 1024-bit into: 128 x 8-bit (bytes); 64 x 16-bit (words); 32 x 32-bit (pages).
The M8571 is manufactured with SGS-THOMSON's reliable floating gate technology. Addresses and data are transferred serially via a three-line bidirectional bus (S-BUS). When the MS pin is at V_{IL} the device works like the PCD 8571 CMOS RAM. The built-in address register is incremented automatically after writing or reading of each address partition.
The M8571 is designed and tested for applications requiring up to 10.000 erase/write cycles and data retention in excess than 100 years.
The M8571 is available in 8-pin dual in-line plastic and ceramic packages.

B
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



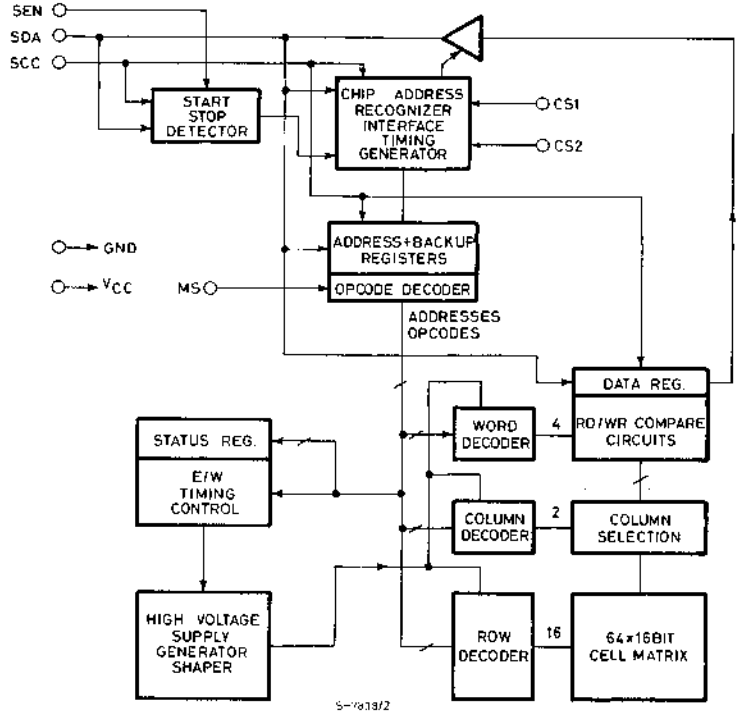
PIN NAMES

CS	CHIP SELECT INPUTS
SEN	START/STOP INPUT
SCL	CLOCK INPUT
SDA	DATA INPUT/OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
MS	MODE SELECT INPUT

PIN DESCRIPTION

- V_{CC}; GND: Power supplies.
- SCL: Clock line for the S-BUS system.
- SEN: Start/Stop line for the S-BUS system.
- SDA: Data line for the S-BUS system (open drain).
- CS1/CS2: Chip Select inputs. In order to select a device the 2 bits (7th and 6th) in the first byte of the interface protocol, must match the CS values.
- MS: Mode Select input to determine the operating mode of the M8571 (this pin can recognize a non standard level, $V_{IN} \geqslant$ 7.5V, to enable "Block Erase" operations).

BLOCK DIAGRAM


SEN
SDA
SCC
START STOP DETECTOR
CHIP ADDRESS RECOGNIZER INTERFACE TIMING GENERATOR
CS1
CS2
GND
VCC
MS
ADDRESS+BACKUP REGISTERS
OPCODE DECODER
ADDRESSES OPCODES
DATA REG.
RD/WR COMPARE CIRCUITS
WORD DECODER
4
STATUS REG.
E/W TIMING CONTROL
COLUMN DECODER
2
COLUMN SELECTION
HIGH VOLTAGE SUPPLY GENERATOR SHAPER
ROW DECODER
16
64×16BIT CELL MATRIX

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 6 to − 0.6	V
T_{amb}	Ambient temperature under bias /B1 /B6	−10 to + 80 −50 to + 95	°C °C
T_{stg}	Storage temperature range	−65 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (0° to +70°C, for standard Temperature/ −40° to +85°C for extended Temperature, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	µA
I_{CC2}	V_{CC} Current Active			10	20	mA
V_{IL}	Input Low Voltage		−0.1		1.5	V
V_{IH}	Input High Voltage		3.0		$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3$ mA			0.4	V

AC CHARACTERISTICS (refer to S-BUS Timing Diagram)

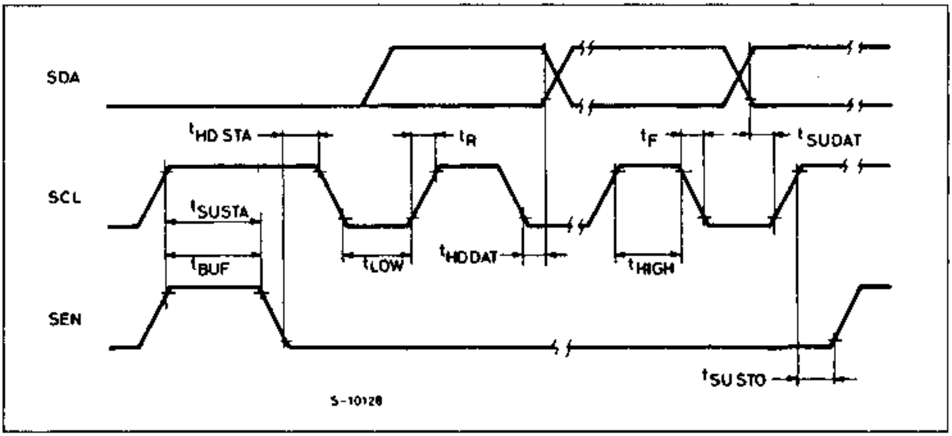
Symbol	Parameter	Test Conditions	Values		Unit
			Min.	Max.	
f_{SCL}	SCL clock frequency		0	125	KHz
T_I	Tolerable spike width on bus			100	ns
t_{AA}	SCL low to SDA data out valid			3.5	µs
t_{BUF}	Time the bus must be free before a new transmission can start		4		µs
t_{HDSTA}	Start condition hold time		4		µs
t_{LOW}	Clock low period		4		µs
t_{HIGH}	Clock high period		4		µs
$t_{SU\ STA}$	Start condition set-up time (for a repeated start condition)		4		µs
$t_{HD\ DAT}$	Data in hold time		0		µs
$t_{SU\ DAT}$	Data in set-up time		250		ns
t_R	SDA and SCL rise time			700	ns
t_F	SDA and SCL fall time			300	ns
$t_{SU\ STO}$	Stop condition set-up time		4		µs

ERASE/WRITE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
t_{EW}	Erase/Write cycle time	Note 1		6	10	ms
t_{BE}	Block erase time		5		10	ms

Note 1: The t_{EW} is the same for byte, word, and page configuration

S-BUS TIMING DIAGRAM



S-BUS DESCRIPTION

The S-BUS is a three-wire bidirectional data-bus with functional features similar to the I^{2}C bus. In fact the S-BUS includes decoding of START/STOP conditions and the arbitration procedure in case of multimaster system configuration. Both different transmission modes are shown in figures 2a and 2b. As it can be seen, the SDA line, in the I^{2}C bus, represents the AND combination of SDA and SEN lines in the S-BUS.

If the SDA and the SEN lines of the S-BUS are short-circuit connected, they appear as the SDA line of I^{2}C bus.

The START/STOP conditions (respectively points 1 and 6) are detected (by the peripherals designed to work with S-BUS) by a transition of the SEN line (1 - - > 0/0 - - > 1) while the SCL line is at the high level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the START information (point 1) the SEN line returns to the high level and remains unchanged for all the time the transmission is performed.

When the transmission is completed (point 5) the SDA line is set to high level and, at the same time, the SEN line returns to the low level in order to supply the STOP information with a low to high transition; while the SCL line is at high level.

On the S-BUS, as on the I^{2}C bus, each byte of eight bits is followed by one acknowledge bit which is a high level put on the SDA line by transmitter. A peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse as shown in Figure 3.

FIG. 1 - S-BUS CONFIGURATION

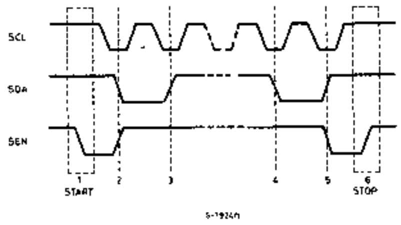


FIG. 2 - I^{2}C BUS CONFIGURATION

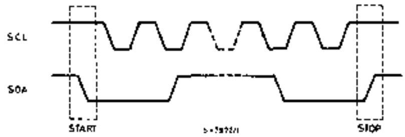
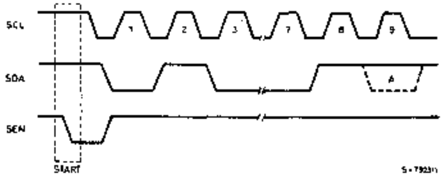


FIG. 3 - ACKNOWLEDGE



S-BUS DESCRIPTION (Continued)

An addressed receiver has to generate an aknowledge after the reception of each byte; otherwise the SDA line remains at the high level during the ninth clock pulse time.
In this case the master transmitter can generate the STOP information, via the SEN line, in order to abort the transfer.

COMPATIBILITY S-BUS/I²C BUS.

Using the S-BUS protocol it's possible to implement "mixed" system including S-BUS/I²C bus peripherals.
In order to have the compability with the I²C bus peripherals, the devices including the S-BUS interface must have their SDA and SEN pins connected together as shown in figures 5a and 5b.
It is also possible to use mixed S-BUS/I²C bus protocols as showed in figure 5c. S-BUS peripherals will only react to S-BUS protocol signals, while I²C bus peripheral will only react to I²C bus signals.

FIG. 4 - SYSTEM WITH S-BUS PERIPHERALS

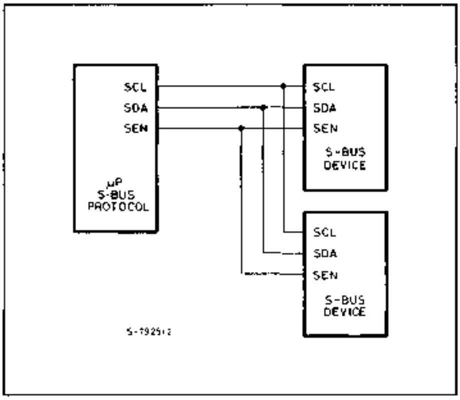
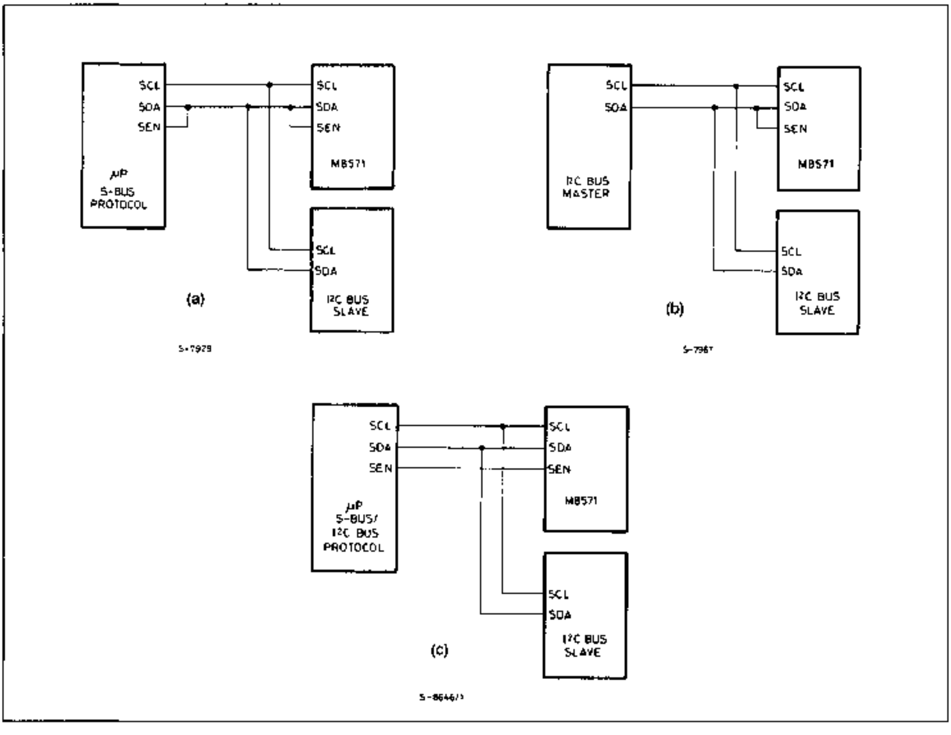

SCL
SDA
SEN
µP
S-BUS
PROTOCOL
SCL
SDA
SEN
S-BUS
DEVICE
SCL
SDA
SEN
S-BUS
DEVICE
S-7925/2

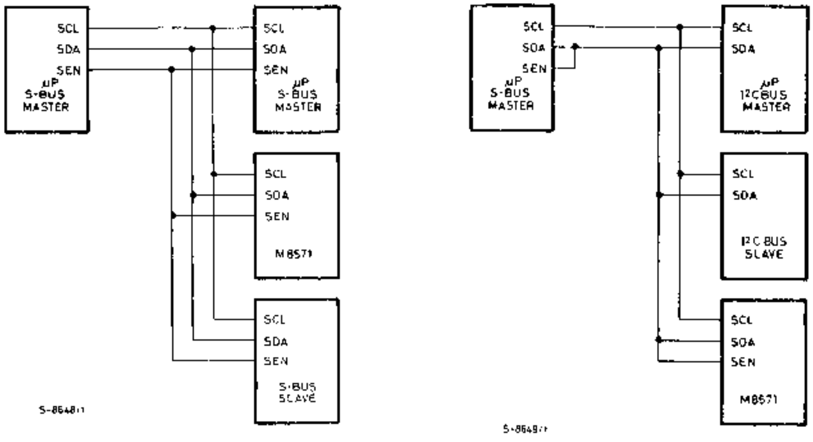
Fig. 5 - SYSTEM WITH "MIXED" S-BUS/I²C BUS PERIPHERAL


SCL
SDA
SEN
µP
S-BUS
PROTOCOL
SCL
SDA
SEN
M8571
SCL
SDA
I²C BUS
SLAVE
(a)
S-7929
SCL
SDA
I²C BUS
MASTER
SCL
SDA
SEN
M8571
SCL
SDA
I²C BUS
SLAVE
(b)
S-7967
SCL
SDA
SEN
µP
S-BUS/
I²C BUS
PROTOCOL
SCL
SDA
SEN
M8571
SCL
SDA
I²C BUS
SLAVE
(c)
S-8646/1

S-BUS DESCRIPTION (Continued)

MULTIMASTER SYSTEM.
The S-BUS allows the implementation of the multimaster configuration (two or more master stations and slave peripherals). In such a system if two or more transmitter, through the SEN line (SEN 1→0 while SCL = 1), require the bus at the same time, the arbitration procedure is performed as in the I²C bus.

FIG. 6 - MULTIMASTER SYSTEM


SCL
SDA
SEN
µP
S-BUS
MASTER
SCL
SDA
SEN
µP
S-BUS
MASTER
SCL
SDA
SEN
M8571
SCL
SDA
SEN
S-BUS
SLAVE
S-8648/1
SCL
SDA
SEN
µP
S-BUS
MASTER
SCL
SDA
µP
I²C BUS
MASTER
SCL
SDA
I²C BUS
SLAVE
SCL
SDA
SEN
M8571
S-8649/1

S-BUS INTERFACE

The serial, 3-wire, interface (SDA, SCL and SEN wires are open drain to allow "wired-and" operation) connects several devices which can be divided into "masters" and "slaves". A master is a device that can manage a data transfer; as such, it drives the Start and Stop (SEN), the clock (SCL) and the data (SDA) lines. The bus is "multimaster" in that more master devices can access it; arbitration procedures are provided in the bus management. Obviously, at least one master must be present on the bus. The M8571 is a hardware slave device. It can only answer the requests of the masters on the bus; therefore SDA is an I/O, while SCL and SEN are inputs. The S-BUS allows two operating speed: high (125KHz) and low (2KHz). The M8571 can work at both high and low speed.

START/STOP ACKNOWLEDGE

The timing specs of the S-BUS protocol require that data on the SDA and SEN lines be stable during the "high" time of SCL. Two exceptions to this rule are foreseen and they are used to signal the start and stop condition of a data transfer.
A "high to low" transition on the SEN line, with SCL "high", is a start (STA).
A "low to high" transition on the SEN line, with SCL "high", is a stop.
Data are transmitted in 8-bit groups; after each group, a ninth bit is interposed, with the purpose of acknowledging the transmitting sequence (the transmitter device place a "1" on the bus, the acknowledging receiver a "0").

INTERFACE PROTOCOL

The following description deals with 8-bits data transfers, so that it fully fits when the memory is "seen" as 128 × 8 array. Although the basic structure of the protocol remains the same the behaviour of the M8571 in 16 or 32 bit data transfers is somewhat different. The differencies are descibed later on.

The interface protocol comprises:
- A start condition (STA)
- A "chip address" byte, trasmitted by the master, containing two different informations.

  a) the code identifying the device the master wants to address (this information is present in the first seven bits); 4bits indicates the type of the device (i.e. memory, tuning, A/D, etc.; the code for memories is 1010); then there is a bit at low level and 2bits that are the Chip Select configuration that must match the hardware present on the 2 CS pins (this is the case of a device with 2 Chip Select like the M8571, for M8571 CS1 and CS2 must match respectively the 7th and the 6th bit of the byte).

  b) the direction of transmission on the bus (this information is given in the 8th bit of the byte); "0" means "Write", that is from the master to the slave, while "1" means "Read". The addressed slave must always acknowledge.

The sequence, from now on, is different according to the value of the R/W bit.

1) R/$\overline{W}$ = "0" (WRITE)

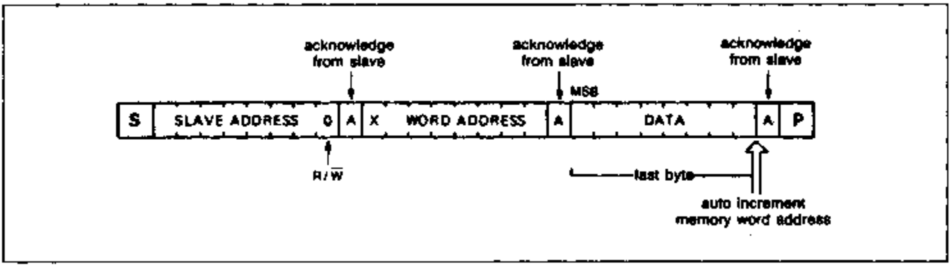
   In all the following bytes the master acts as transmitter; the sequence follows with:
   a) a "word address" byte containing the address of the selected memory word and/or opcode (see word address/opcode section).
   b) a "data" byte which will be written at the address given in the previous byte.
   c) further data bytes which, due to the self incrementing address register, will be written in the "next" memory locations. At the end of each byte the M8571 acknowledges.
   d) a stop condition (STO)

After receiving and acknowledging a data byte or a set of data bytes to be written, the M8571 automatically erases the addressed memory locations and rewrites them with the received data. Since the E/W time for an EEPROM is in the order of 10 ms, the next operation can take place only after $t_{E/W}$ (what the master can and must do is described in the E/W TIME SPECS section).
An example of a write sequence is given below:

0. STA
1. 10100ss0 A (M8571 acknowledges only if "ss" matches its CS code)
2. xyyyyyyy A
3. zzzzzzzz A (at this moment the M8571 starts writing zzzzzzzz at the address yyyyyyy)
4a. tttttttt H (the new data is not acknowledged while the M8571 is busy)
4b. tttttttt A (now the M8571 writes data tttttttt at address yyyyyyy + 1)

The write sequence can be composed by an unlimited number of data bytes.

MASTER TRANSMITS TO SLAVE RECEIVER (WRITE MODE)


acknowledge from slave
acknowledge from slave
acknowledge from slave
MSB
S
SLAVE ADDRESS
0
A
X
WORD ADDRESS
A
DATA
A
P
R/W̄
last byte
auto increment memory word address

2) R/W̄ = "1" (READ)

In this case the slave acts as transmitter and, therefore, the transmission changes direction. The second byte of the sequence will be sent by the M8571 and it will contain the data present in the memory present at the address pointed by the "current" value of the address register. Following bytes will be the data present at the "next" addresses. At the end of each byte, the M8571 places a "1" on the bus during acknowledge time and waits for the master to send a "0" (meaning "acknowledge"). When the master want to stop the transfer, it gives a "1" (not "acknowledged"): as a consequence, the M8571 leaves the bus high so that the master can give the stop condition. An example is given below:

0. STA
1. 10100ss1 A
2. xxxxxxxx H (xxxxxxxx is the data present in the currently addressed memory location; H is the high level placed on the bus by M8571)

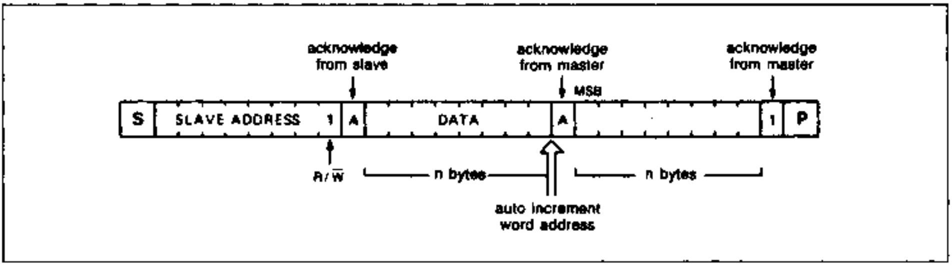
3) MIXED SEQUENCE

When the master wants to read a memory location different from the one currently addressed, a longer sequence is needed, which includes the writing of the address register. The sequence is as follows:

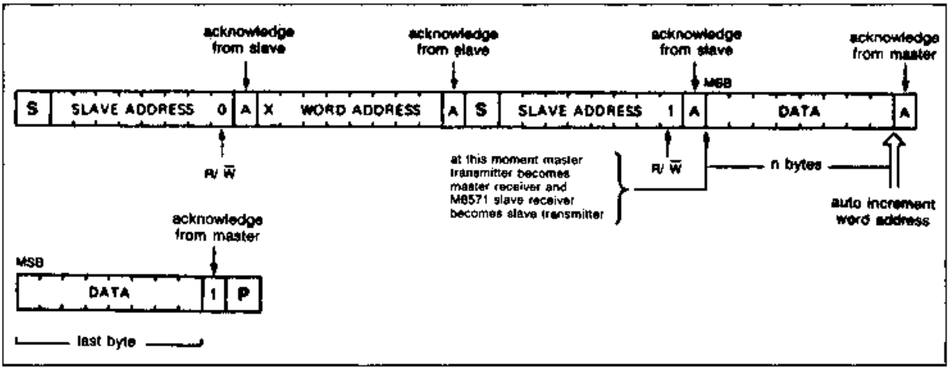
0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. STA
4. 10100ss1 A
5. xxxxxxxx H

Where xxxxxxxx is the data present in the yyyyyyy memory location
As appears from the example, a start condition can be given without a previous stop condition.

MASTER READS SLAVE IMMEDIATELY AFTER FIRST BYTE (READ MODE)


acknowledge from slave
acknowledge from master
acknowledge from master
MSB
S
SLAVE ADDRESS
1
A
DATA
A
1
P
R/W̄
n bytes
n bytes
auto increment word address

MASTER READS AFTER SETTING WORD ADDRESS (WRITE WORD ADDRESS; READ DATA)


acknowledge from slave
acknowledge from slave
acknowledge from slave
acknowledge from master
MSB
S
SLAVE ADDRESS
0
A
X
WORD ADDRESS
A
S
SLAVE ADDRESS
1
A
DATA
A
R/W̄
at this moment master transmitter becomes master receiver and M8571 slave receiver becomes slave transmitter
R/W̄
n bytes
auto increment word address
acknowledge from master
MSB
DATA
1
P
last byte

4) E/W TIME SPECS

After the beginning of an E/W operation at a certain location the M8571 is "busy" until the operation is finished. To show this busy state, the M8571 refuses acknowledge of the next data bytes to remove the M8571 from the "busy" state a data byte must be sent after the t_{EW} is over. This "dummy" byte will not be acknowledged and written. The data to be written in the next address must be sent again and will be acknowledged and written by the M8571.

The master device that wants to use the self increment feature must therefore keep sending the next data byte and monitoring the acknowledge bit until it becomes active.

The communication sequence on the bus becomes, therefore.

0. STA
1. 10100ss0 A
2. xyyyyyyy A
3. zzzzzzzz A
4a. tttttttt H (not acknowledged when $t < t_{E/W}$)

after t_{EW}:

4b. tttttttt H (not acknowledged, the M8571 is removed from the "busy" state)
4c. tttttttt A (acknowledged, the M8571 starts writing data ttttttt at address yyyyyyyy + 1)

Now the M8571 will write data ttttttt at address yyyyyyy + 1

This usage mode keeps the bus unavailable for other tasks during the $t_{E/W}$ time. It is possible to free the bus by giving a stop condition (this condition stops only the bus sequence, not the E/W operation). After a stop condition the access sequence must be started again from the beginning (start).

The E/W circuitry in the M8571 performs automatically the "Erase before Write" sequence required by the technology. Furthermore, both erase and write last all (and only) the time needed for the required modification to happen (this is accomplished by an intelligent "compare and retry" circuitry). This optimizes E/W time but may have the drawback of "locking" the circuitry in case a memory location "breaks down" and can not be modified (in which case $t_{E/W}$ becomes infinite).

To overcome this drawback, it has been made possible to force the circuit out of the E/W status, that is to halt a modify operation. Two different modes are provided, depending on the value of the MS control pin:

$$MS \leqslant V_{IL}$$

The E/W operation is unconditionally stopped by a following valid chip address byte.

$$MS \geqslant V_{IH}$$

An opcode is provided to halt the operation (see "EEPROM mode" section).

5) WORD ADDRESS/OPCODE

The second byte transmitted in a write sequence can assume several meaning according to the value of the MS pin. In any case, it carries all the informations the M8571 needs to perform the desired operation.
MS can assume three different values:

- V_{IL} ($V_{IN} \leq 1.5V$)
- V_{IH} ($3.0V \leq V_{IN} < V_{CC} + 1$)
- V_H ($9.0V \leq V_{IN} \leq 12V$)

With regards to the value of MS, the possible behaviours are:

a) $MS = V_{IL}$ ("RAM mode")
In this mode the M8571 is compatible with the PCD 8571 RAM (128 x 8bit). The second byte of the sequence gives the address of the word to be selected, both for write and for read:

1. xyyyyyyy A
yyyyyyy is the word address; the first bit is "don't care; the main feature of this mode are the following:
   - . the memory appears as an 128 x 8 array
   - . only "byte operations are allowed;
   - . E/W operations are stopped by the following accesses.

b) $MS = V_{IH}$ (EEPROM mode)

The word address-byte now must be regarded as mixed address-opcode byte; more precisely, the first three bits indicate the meaning to be attributed to the remainder of the byte. The possible combinations are:

0yyyyyyy	byte-mode (8 bits) RD or E/W at address yyyyyyy
10yyyyyy	word-mode (16 bits) RD or E/W at address yyyyyy
110yyyyy	page-mode (32 bits) RD or E/W at address yyyyy
11111111	E/W cycle stop
11100000	Read busy bit
11100100	Block Erase (needs V_H on MS pin, see also BLOCK mode)
11110001	Reload Address Register with pre-increment data

In this mode, as well as in RAM mode, the "busy" information is transmitted from the M8571 to the master using the "no acknowledge" format. Furthermore, "Read busy bit" instruction, which is always answered by the M8571 no matter what it is doing, allows the master to know wheter the "no acknowledge" condition comes from a "busy" status or from a malfunction; the "busy" status is signalled by the byte 11100101; the "no busy" by 00011010.
Also in this mode the self-incrementing address register is available, both for read and for write, for each word length.
The M8571 is provided with a double register for storing the address that is sent during the second byte of a write sequence.
When the self-incrementing is used, this address becomes the "starting address" of the modified string of bytes. The "reload" instruction allows the master to recover this address if it wants to read the modified string from the beginning, without the need for external storage of the "starting address".

c) $MS = V_H$ (BLOCK mode)

The only instruction that can be executed in this mode is "Block Erase", which is useful to erase the whole array in a single shot. This can occur either during testing or at the set-up of a new system, when the whole memory must be written. When this instruction is given, the self-timing circuitry is disabled, so that the operation must be stopped (after t_{BE}) by the master executing a START on the bus. The "enable" feature obtained with the non standard level on MS was added to avoid unintentional clearing of the whole memory, whenever the "Block Erase" code was erroneously sent.

6) 16-bit or 32-bit OPERATIONS

The obvious advantage of an operation on 16 bits (a word) or on 32 bits (a page) is that the E/W time is 10ms for the whole word or page. When a word or page mode operation is required, the device behaviour undergoes some slight modifications:

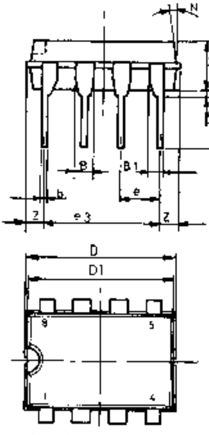
- The M8571 waits for receiving all the bytes that compose the word or the page before starting an E/W operation;
- The self-incrementing address register keeps into account the word or page lenght so that, at the end of a word or page mode operation, it points to the next word or page.

ORDERING INFORMATION

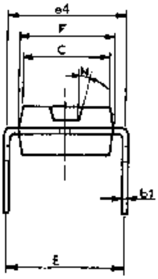
Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
M8571B1	125 KHz	5V ± 10%	0° to +70°C	DIP-8
M8571B6	125 KHz	5V ± 10%	−40° to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

SGS-THOMSON
MICROELECTRONICS

M9306

256 BIT (16 × 16) SERIAL NMOS EEPROM

- SINGLE SUPPLY READ/WRITE/ERASE OPERATIONS (5V ± 10%)
- TTL COMPATIBLE
- 16 × 16 READ/WRITE MEMORY
- LOW STANDBY CURRENT
- LOW COST SOLUTION FOR NON VOLATILE ERASE AND WRITE MEMORY
- RELIABLE FLOTOX PROCESS
- EXTENDED TEMPERATURE RANGE

B
DIP-8
(Plastic Package)

M
SO8
(Plastic Micropackage)

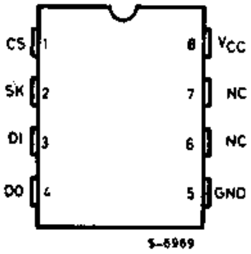
(Ordering information at the end of the datasheet)

DESCRIPTION

The M9306 is a 256 bit non-volatile sequential access memory manufactured using SGS-THOMSON FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface.

The device contains 256 bits organized as 16 x 16. The M9306 has been designed to meet application requiring up to 10000 E/W cycles per word. Written information has at least 10 years data retention. A power down mode allows consumption to be decreased.

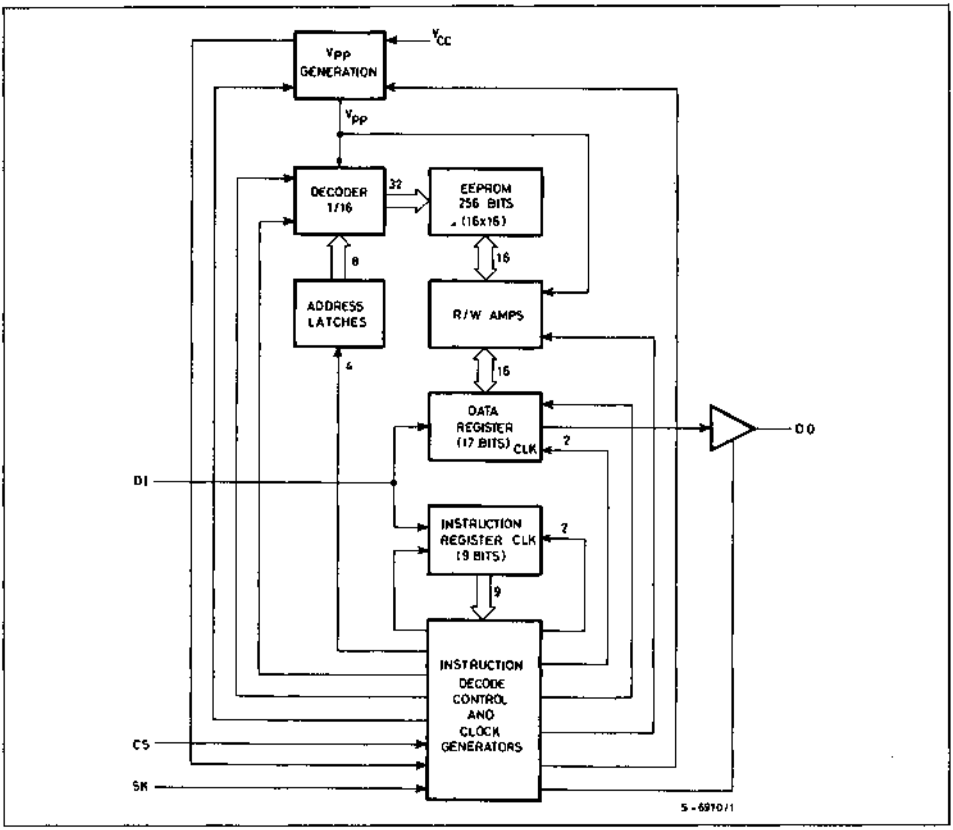
PIN CONNECTIONS



PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

BLOCK DIAGRAM


VPP GENERATION
VCC
VPP
DECODER 1/16
32
EEPROM 256 BITS (16x16)
8
16
ADDRESS LATCHES
R/W AMPS
4
16
DATA REGISTER (17 BITS) CLK
2
DO
DI
INSTRUCTION REGISTER CLK (9 BITS)
2
9
INSTRUCTION DECODE CONTROL AND CLOCK GENERATORS
CS
SK
S-6910/1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+6V to −0.3	V
T_{amb}	Ambient Operating Temperature: standard extended	0 to +70 −40 to +85	°C °C
T_{stg}	Ambient Storage Temperature	−65 to +125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (except for T_{amb})

ELECTRICAL CHARACTERISTICS (0°C to +70°C, for standard Temperature/−40°C to +85°C for extended Temperature, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1		1.5	5	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		1.2	3	mA
I_{CC3}	E/W Operating Current	$V_{CC} = 5.5V$		2.5	6	mA
V_{IL}	Input Voltage Levels		−0.1		0.8	V
V_{IH}			2.0		$V_{CC} + 1$	
V_{OL}	Output Voltage Levels	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4			
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	µA
	SK Frequency				250*	kHz
	SK Duty Cycle		25		75	%
	Input Set-Up and Hold Times:					
t_{CSS}	CS		0.2			µs
t_{CSH}			0			
t_{DIS}	DI		0.2			
t_{DIH}			0.2			
t_{PD1}	Output Delay	CL = 100 pF			0.5	µs
t_{PD0}	DO	$V_{OL} = 0.8V$,			0.5	
		$V_{OH} = 2.0V$				
$t_{E/W}$	Erase/Write Pulse Width		5		30	ms
t_{CS}	Min CS Low Time (Note 1)	$C_L = 100$ pF			1	µs

* The maximum SK Frequency is 500 KHz when SK Duty Cycle is as 50%

Note: 1. CS must be brought low for a minimum of 1µs (V_{CS}) between consecutive instruction cycles.

FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Seven 9-bit instruction can be executed. The instruction format as a logical "1" has a start bit, four bits as an op code, and four bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). The serial output (DO) pin is valid only during the read mode. During all other modes the DO pin is in high impedance state, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") precedes the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction in executed. The programming disable instruction is provided to protect against accidental data disturbance.
Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most EEPROMs, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low power standby state may be achieved by dropping CS low.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on chip high voltage section only generates high voltage during this programming mode, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycles ends. All programming mode should be ended with CS high for one SK period, or followed by another instruction.

CHIP WRITE

Entire chip can be written for ease of testing. Writing the chip means that all registers in the memory array have each bytes set as the byte sent with the instruction.

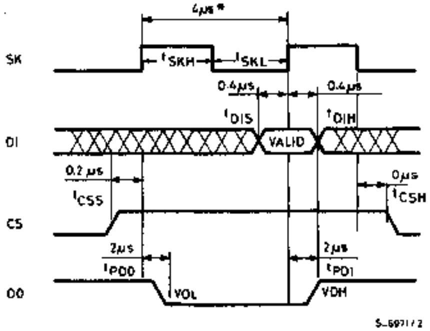
CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

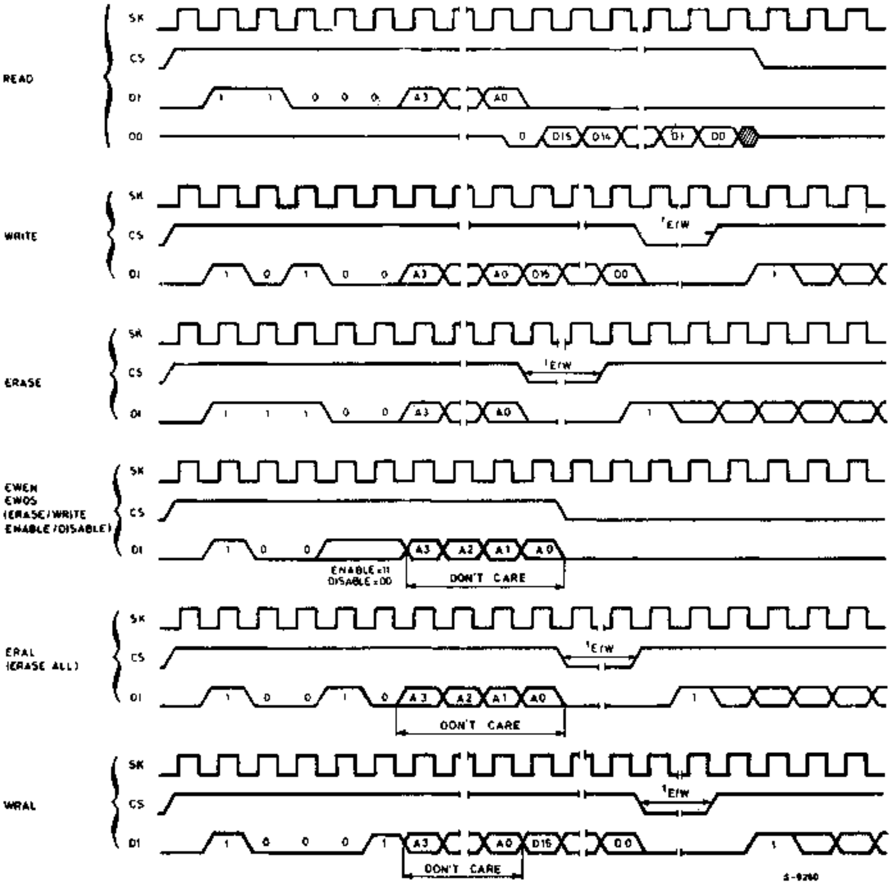
INSTRUCTION SET

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10XX	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01XX	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	11XX	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	X X X X		Erase/write enable
EWDS	1	0000	X X X X		Erase/write disable
ERAL	1	0010	X X X X		Erase all registers
WRAL	1	0001	X X X X	D15-D0	Write all registers

TIMING DIAGRAMS


4µs *
SK
t_{SKH}
t_{SKL}
0.4µs
0.4µs
t_{DIS}
t_{DIH}
DI
VALID
0.2 µs
t_{CSS}
0µs
t_{CSH}
CS
2µs
t_{PD0}
2µs
t_{PD1}
DO
VOL
VOH
S-6971/2

* THIS IS THE MAXIMUM SK FREQUENCY

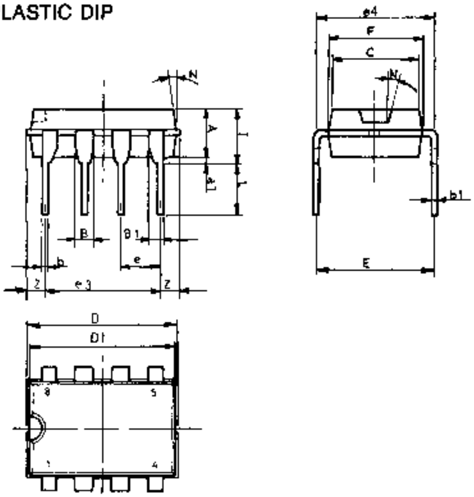

READ
SK
CS
DI
1
1
0
0
0
A3
A0
DO
0
D15
D14
D1
D0
WRITE
SK
CS
$t_{E/W}$
DI
1
0
1
0
0
A3
A0
D15
D0
1
ERASE
SK
CS
$t_{E/W}$
DI
1
1
1
0
0
A3
A0
1
EWEN
EWDS
(ERASE/WRITE
ENABLE/DISABLE)
SK
CS
DI
1
0
0
A3
A2
A1
A0
ENABLE =11
DISABLE =00
DON'T CARE
ERAL
(ERASE ALL)
SK
CS
$t_{E/W}$
DI
1
0
0
1
0
A3
A2
A1
A0
1
DON'T CARE
WRAL
SK
CS
$t_{E/W}$
DI
1
0
0
0
1
A3
A0
D15
D0
1
DON'T CARE
S-9260

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
M9306B1 M9306B6	250 KHz 250 KHz	5V ± 10% 5V ± 10%	0° to +70°C −40° to +85°C	DIP-8 DIP-8
M9306M1 M9306M6	250 KHz 250 KHz	5V ± 10% 5V ± 10%	0°to +70°C −40° to +85°C	SO8 SO8

PACKAGE MECHANICAL DATA

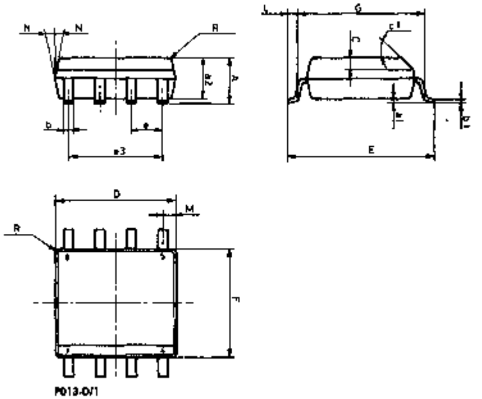
8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

8-LEAD PLASTIC MICROPACKAGE



P013-O/1

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			2.00			0.079
a1	0.10		0.20	0.004		0.008
a2			1.70			0.067
b		0.40			0.016	
b1		0.20			0.008	
C						
c1						
D			5.08			0.200
E			6.30			0.248
e		1.27			0.050	
e 3		3.81			0.150	
F	4.10		4.30	0.161		0.169
G	4.90			0.193		
L	0.25			0.010		
M			0.635			0.025
N						
R						

SGS-THOMSON
MICROELECTRONICS

M9346

1024 BIT (64 × 16) SERIAL NMOS EEPROM

- SINGLE SUPPLY READ/WRITE/ERASE OPERATIONS (5V ± 10%)
- TTL COMPATIBLE
- 64 × 16 READ/WRITE MEMORY
- LOW STANDBY CURRENT
- LOW COST SOLUTION FOR NON VOLATILE ERASE AND WRITE MEMORY
- RELIABLE FLOTOX PROCESS
- SELF-TIMED PROGRAMMING CYCLE
- DEVICE STATUS SIGNAL DURING PROGRAMMING
- POWER-ON/OFF DATA PROTECTION CIRCUITRY
- AUTOERASE
- BULK PROGRAMMING ENABLE OR DISABLE FOR ENHANCED DATA PROTECTION

DESCRIPTION

The M9346 is a 1024 bit non-volatile sequential access memory manufactured using SGS-THOMSON FLOATING GATE process. It is a peripheral memory designed for data storage and/or timing and is accessed via a simple serial interface. The device contains 1024 bits organized as 64x16. Written information is stored in a floating gate cell until updated by an erase and write cycle.

Bulk programming instructions (Chip Erase, Chip Write) can be enabled or disabled by the user for enhanced data protection. The M9346 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power down mode allows a consumption decrease by 75%.

PIN NAMES

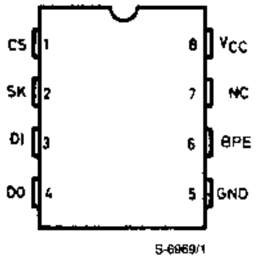
CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND
BPE	BULK PROGRAMMING ENABLE
NC	NO CONNECT

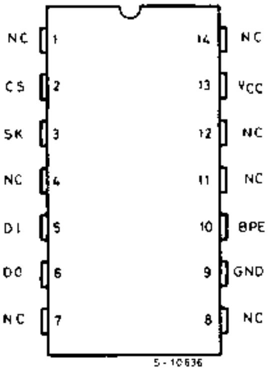
B
DIP-8
(Plastic Package)

M
SO14
(Plastic Micropackage)

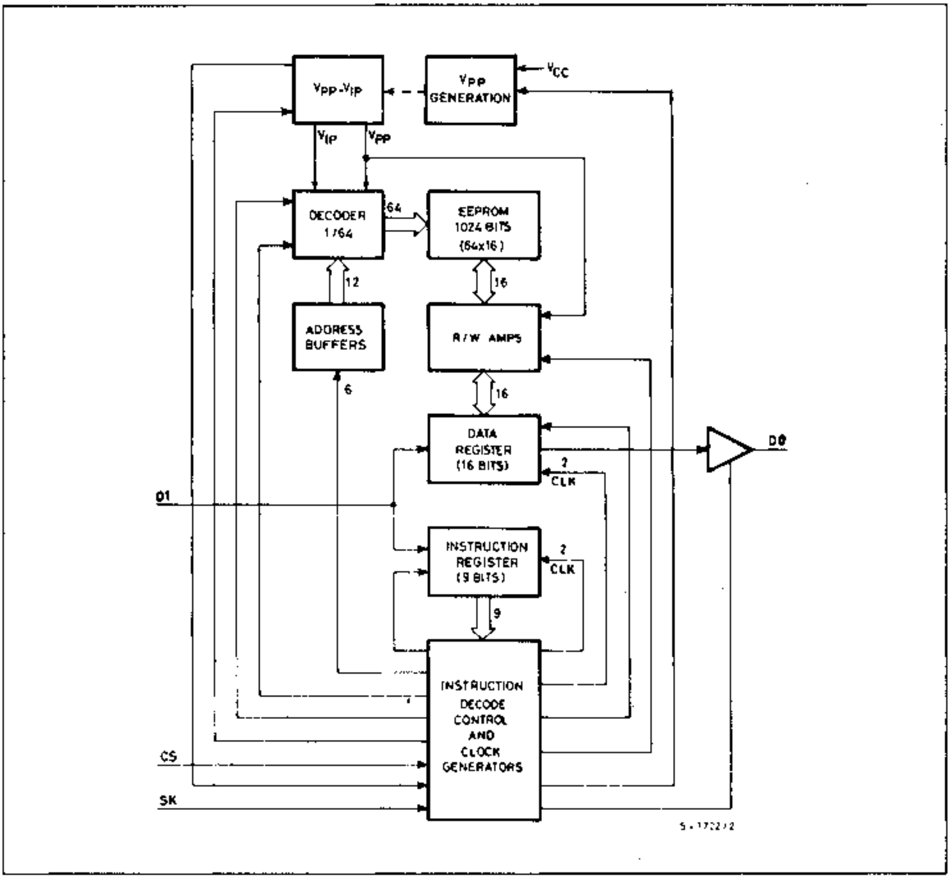
(Ordering Information at the end of the datasheet)

PIN CONNECTIONS





BLOCK DIAGRAM


VPP-VIP
VPP GENERATION
VCC
VIP
VPP
DECODER 1/64
64
EEPROM 1024 BITS (64x16)
12
16
ADDRESS BUFFERS
R/W AMPS
6
16
DATA REGISTER (16 BITS)
2 CLK
DO
DI
INSTRUCTION REGISTER (9 BITS)
2 CLK
9
INSTRUCTION DECODE CONTROL AND CLOCK GENERATORS
CS
SK
S-1722/2

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
V_I	Voltage Relative to GND	+ 6V to − 0.3	V
T_{amb}	Ambient Operating Temperature: standard extended	0 to + 70 − 40 to + 85	°C
T_{stg}	Ambient Storage temperature	− 65 to + 125	°C

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (except for T_{amb}).

ELECTRICAL CHARACTERISTICS (0° to +70°C, for standard Temperarure/ −40° to +85°C for extended Temperarure, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage		4.5		5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1		1.5	12	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		1.2	3	mA
I_{CC3}	E/W Operating Current	$V_{CC} = 5.5V$, SK = 1		2.5	12	mA
V_{IL} V_{IH}	Input Voltage Levels		−0.1 2.0		0.8 $V_{CC}+1$	V
V_{OL} V_{OH}	Output Voltage Levels	$I_{OL} = 2.1$ mA $I_{OH} = -400$ µA	 2.4		0.4 	V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0			10	µA
	SK Frequency		0		250	kHz
	SK Duty Cycle		25		75	%
	Input Set-Up and Hold Times:					
t_{CSAE}	CS (Note 2)		0.4			µs
t_{CSS}			0.2			
t_{CSH}			0			
t_{DIS}	DI		0.4			
t_{DIH}			0.4			
t_{PD1}	Output DO	CL = 100 pF $V_{OL} = 0.8V$, $V_{OH} = 2V$			2	µs
t_{PD0}		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$			2	
$t_{E/W}$	Self-Timed Program Cycle				10	ms
t_{CS}	Min CS Low Time (Note 1)		1			µs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF			1	µs
t_{0H}, t_{1H}	Falling Edge of CS to DO tri-state				0.4	µs

Note: 1. CS must be brought low for a minimum of 1µs (t_{CS}) between consecutive instruction cycles.
2. t_{CSAE} condition has to be fullfilled in "WRITE WITH AUTOERASE" mode.

FUNCTIONAL DESCRIPTION

The input and output pins are controlled by separate serial formats. Eight 9-bit instructions can be executed. The instruction format has a logical "1" as a start bit, two bits as an op code, and six bits of address. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip-erase, chip-write) to prevent spurious programming during other modes.

The programming cycle is self timed, with the data out (DO) pin indicating the ready/busy state of the chip. The serial output (DO) pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in high impedance state eliminating bus contention. The Bulk programming instructions (ERAL, WRAL) are enabled or disabled by the BPE pin. This pin connected to V_{IH} enables the executions of previous mentioned instructions. The BPE pin connected to V_{IL} causes the same instructions to be ignored. If the BPE pin is not connected, it is pulled-up to V_{CC} by an on-chip pull-up and the Bulk programming instructions are enabled. Execution of the EWEN, EWDS, WRITE and ERASE instructions are independent from the state of the BPE pin.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16 bit serial out shift register. A dummy bit (logical "0") precedes the 16 bit data output string. The output data changes during the high state of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 2)

Like most EEPROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an ERASE instruction is input, CS is dropped low.

This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE (Note 2)

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specifed in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

WRITE WITH AUTOERASE (Note 2)

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (DO) is put on the data in (DI) pin CS must be brought low before the next falling edge of the SK clock.

This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specifed in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

FUNCTIONAL DESCRIPTION (Continued)

CHIP ERASE (Note 2)

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a WRITE instruction. The chip erase cycle is identical to the erase cycle except for the different op code. The Chip Erase (ERAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

CHIP WRITE (Note 2)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction. The Chip Write (WRAL) instruction is ignored if the BPE pin is at V_{IL}, i.e. the array data is not changed.

DI/DO

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedance of Data Out and the signal source driving A_0. The higher current sourcing capability of A_0, the higher voltage at the Data Out pin. To solve this problem the DI pin must be in high impedance after the last rising edge of the SK clock.

POWER ON DATA PROTECTION CIRCUITRY

During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

Note 1: CS must be brought low for a minimum of 1 µs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e. start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

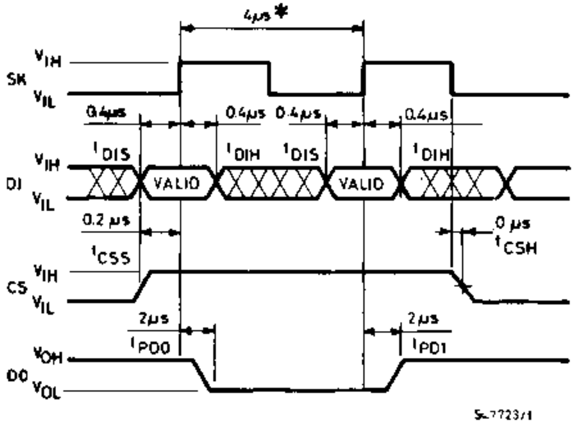
INSTRUCTION SET

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
WR. AUTOERASE	1	01	A5A4A3A2A1A0	D15-D0	Erase/write register A5A4A3A2A1A0
EWEN	1	00	11 x x x x		Erase/write enable
EWDS	1	00	00 x x x x		Erase/write disable
ERAL	1	00	10 x x x x		Erase all registers
WRAL	1	00	01 x x x x	D15-D0	Write all registers

M9346 has 8 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

TIMING DIAGRAMS

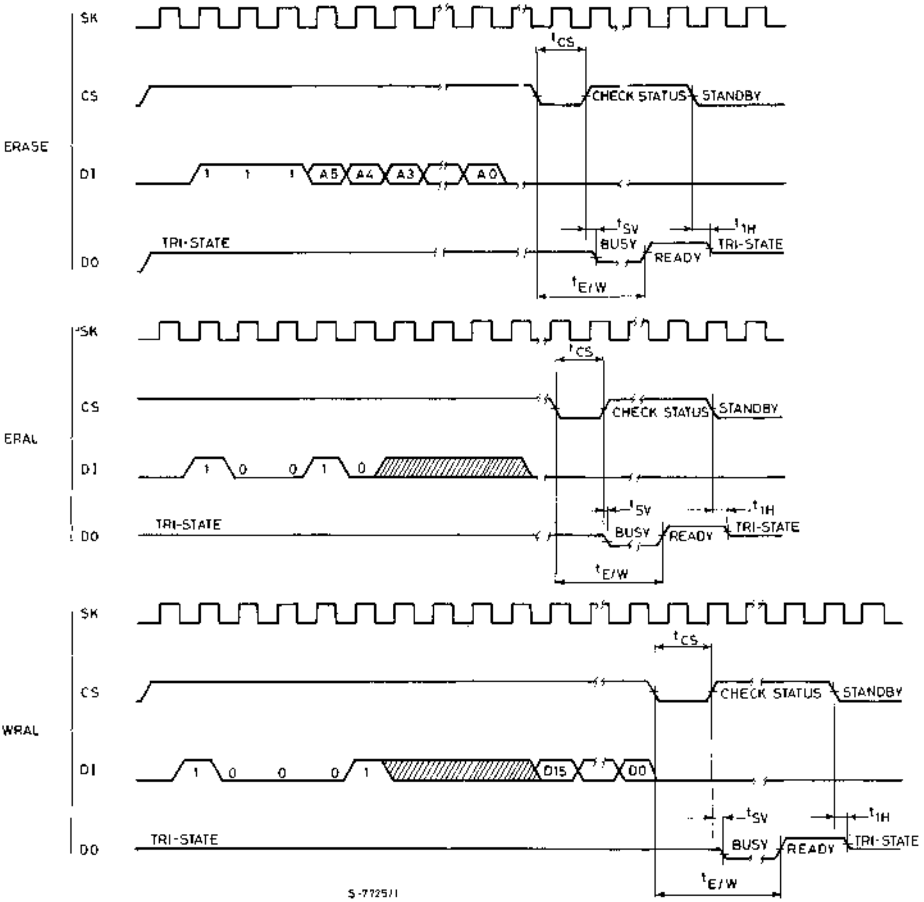
SYNCHRONOUS DATA TIMING


4µs *
SK
V_IH
V_IL
0.4µs
0.4µs
0.4µs
0.4µs
t_DIS
t_DIH
t_DIS
t_DIH
DI
V_IH
V_IL
VALID
VALID
0.2 µs
t_CSS
0 µs
t_CSH
CS
V_IH
V_IL
2µs
t_PD0
2µs
t_PD1
DO
V_OH
V_OL
5-7723/1

* THIS IS THE MINIMUM SK PERIOD

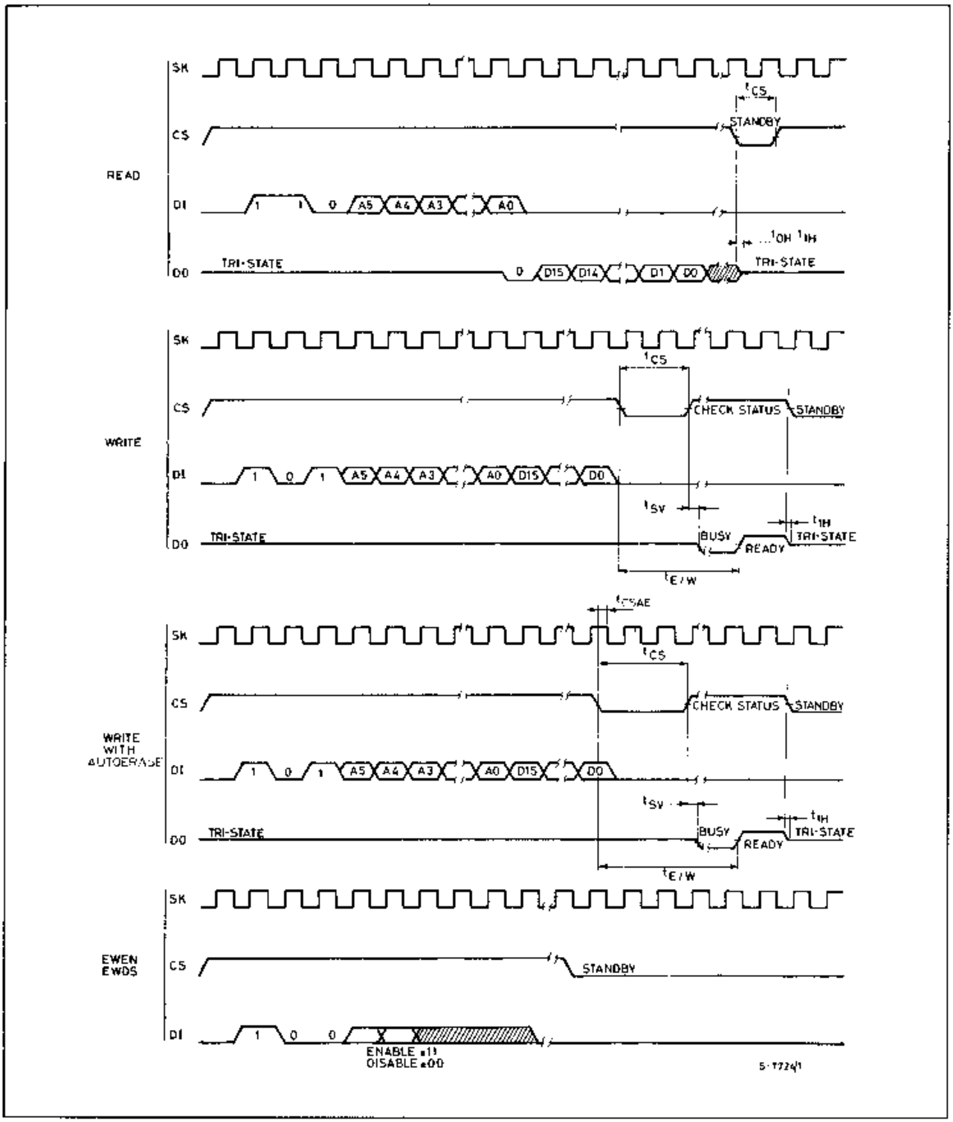
TIMING DIAGRAMS

INSTRUCTION TIMING


SK
CS
DI
DO
ERASE
tCS
CHECK STATUS
STANDBY
1 1 1 A5 A4 A3 A0
tSV
t1H
TRI-STATE
BUSY
READY
tE/W
ERAL
1 0 0 1 0
WRAL
1 0 0 0 1 D15 D0
S-7725/1

TIMING DIAGRAMS (Continued)

INSTRUCTION TIMING

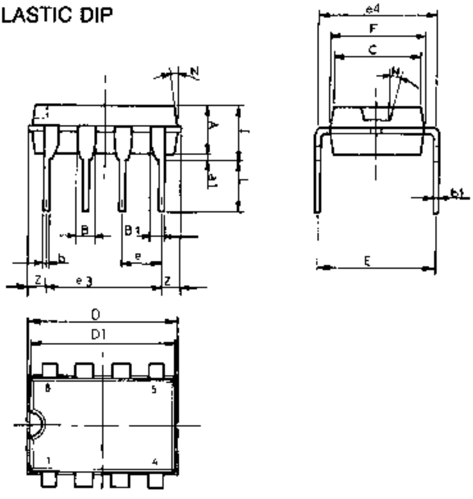

READ
SK
CS
DI
DO
t_{CS}
STANDBY
1
1
0
A5
A4
A3
A0
t_{OH} t_{IH}
TRI-STATE
0
D15
D14
D1
D0
TRI-STATE
WRITE
SK
t_{CS}
CS
CHECK STATUS
STANDBY
DI
1
0
1
A5
A4
A3
A0
D15
D0
t_{SV}
t_{IH}
DO
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$
WRITE WITH AUTOERASE
t_{CSAE}
SK
t_{CS}
CS
CHECK STATUS
STANDBY
DI
1
0
1
A5
A4
A3
A0
D15
D0
t_{SV}
t_{IH}
DO
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$
EWEN EWDS
SK
CS
STANDBY
DI
1
0
0
ENABLE =11
DISABLE =00
5-7724/1

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
M9346B1	250 KHz	5V ± 10%	0° to +70°C	DIP-8
M9346B6	250 KHz	5V ± 10%	−40° to +85°C	DIP-8
M9346M1	250 KHz	5V ± 10%	0° to +70°C	SO14
M9346M6	250 KHz	5V ± 10%	−40° to +85°C	SO14

PACKAGE MECHANICAL DATA

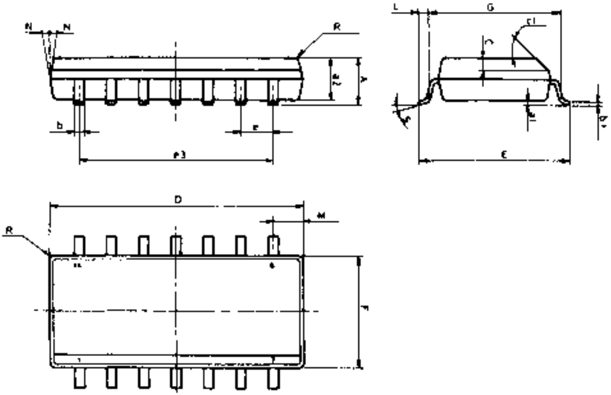
8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

14-LEAD PLASTIC MICROPACKAGE



P0/3-G/3

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
a1	0.10		0.20	0.004		0.008
a2			1.60			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.50			0.020	
c1		45°			45°	
D(1)	8.55		8.75	0.337		0.344
E	5.80		6.20	0.228		0.244
e		1.27			0.050	
e 3		7.62			0.300	
F(1)	3.80		4.00	0.150		0.157
G	4.60		5.30	0.181		0.209
L	0.50		1.27	0.020		0.050
M			0.68			0.027
N						
R						
S			8°			8°

Note: 1. D and F do not include mold flash or protusions. They should not exceed 0.15 mm/.006 inches.

EEPROM DEVICES

CMOS EEPROM

SGS-THOMSON
MICROELECTRONICS

ST24C02

2K BIT SERIAL 2 WIRE BUS CMOS EEPROM

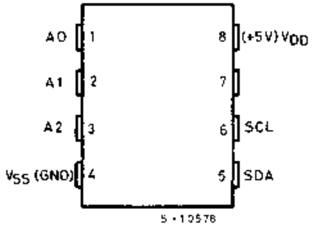
PRELIMINARY DATA

- 256 × 8 SERIAL EEPROM
- SINGLE +5V ONLY OPERATION
- COMPATIBLE WITH THE INTER-INTEGRATED-CIRCUIT BUS
- FULLY TTL COMPATIBLE INPUTS AND OUTPUTS
- UNLIMITED READ ACCESSES
- ESD PROTECTION: INPUTS ARE DESIGNED TO MEET 2.0 KV PER TEST METHOD 3015, MIL-STD 883
- HIGHLY RELIABLE N-WELL CMOS TECHNOLOGY
- DESIGNED FOR 10 YEAR DATA RETENTION AFTER 10000 ERASE/WRITE CYCLE PER WORD
- 0 TO +70°C OPERATING AMBIENT TEMPERATURE RANGE.
- −40 TO +85°C EXTENDED TEMPERATURE RANGE

P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



DESCRIPTION

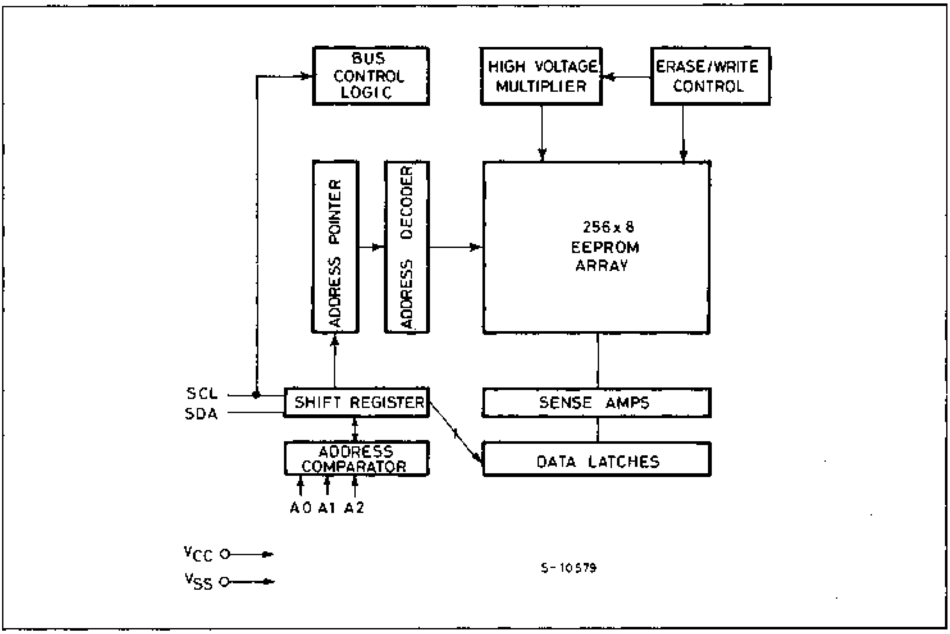
The ST24C02 is a 2K EEPROM manufactured in SGS-THOMSON highly reliable CMOS technology. The key features of this device are +5 volt only operation and inter—integrated circuit bus compatibility. This revolutionnary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of in the bus protocol. Up to eight ST24C02s may be capacitance).

Chip select is accomplished by means of the three address inputs A_0, A_1 and A_2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input the (SDA) at the appropriate time in the bus protocol. Up to eight TS24C02s may be connected to the serial bus.

PIN NAMES

A_0-A_1-A_2	CHIP ADDRESS INPUTS
V_{SS}	GROUND
S_{DA}	SERIAL DATA/ADDRESS, INPUT/OUTPUT
S_{CL}	SERIAL CLOCK INPUT, ERASE/WRITE
V_{CC}	+5V POWER SUPPLY

BLOCK DIAGRAM


BUS CONTROL LOGIC
HIGH VOLTAGE MULTIPLIER
ERASE/WRITE CONTROL
ADDRESS POINTER
ADDRESS DECODER
256 x 8 EEPROM ARRAY
SCL
SDA
SHIFT REGISTER
SENSE AMPS
DATA LATCHES
ADDRESS COMPARATOR
A0 A1 A2
V_{CC}
V_{SS}
S-10579

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristic	Min	Typ	Max	Units
V_{DD}	Power supply voltage	−0.3		7	V
V_I	Voltage on any input pin	$V_{SS}-0.8$		$V_{DD}+0.8$	V
T_A(1)	Ambient operating temperature	0		+70	°C
I_{SIG}	Storage temperature (unpowered and without data retention)	−65		+150	°C
I_I	Current into any input pin			100	μA
I_O	Output current			3	mA (SINK)
	Soldering temperature of leads (10 seconds)			300	°C

Note: 1. $T_A = -40°C$ to $+85°C$ for extended temperature range

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other condition outside those indicated in the operational sections of this specification, is not implied.

CHARACTERISTICS OF THE 2-WIRE BUS

This bus is intended for communication between different ICs. It consists of two bidirectional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:
- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpretated as control signals.

Accordingly, the following bus conditions have been defined:
Bus not busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to eight bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each receiver acknowledges with a ninth bit.

Whithin the bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The ST 24C02 works in both modes By definition a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clockpulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 1 attached shows the typical manner in which the ST24C02 is interfaced to the bus. For purposes of illustration chip address, A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight ST24C02s can be connected to the bus of a single system. The erase/write cycle time of this device T E/W is determinated internally.

FIG. 1 - TYPICAL INTERFACE

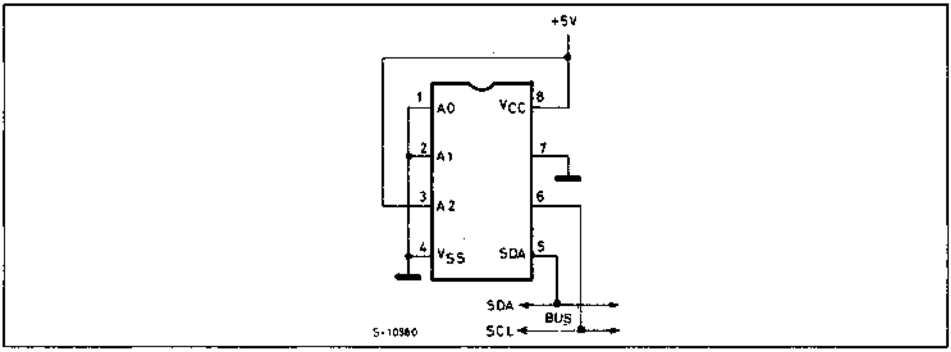


FIG. 2A - DATA TRANSFER SEQUENCE OF THE SERIAL BUS

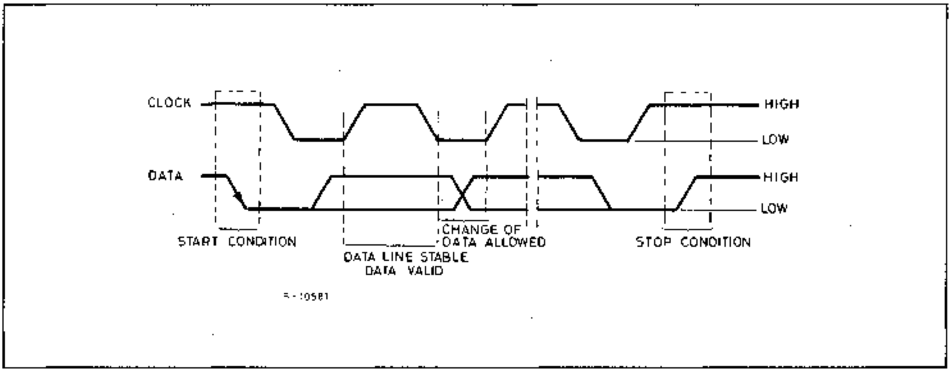

CLOCK
DATA
HIGH
LOW
HIGH
LOW
START CONDITION
DATA LINE STABLE
DATA VALID
CHANGE OF
DATA ALLOWED
STOP CONDITION
S-10581

FIG. 2B - ACKNOWLEDGEMENT

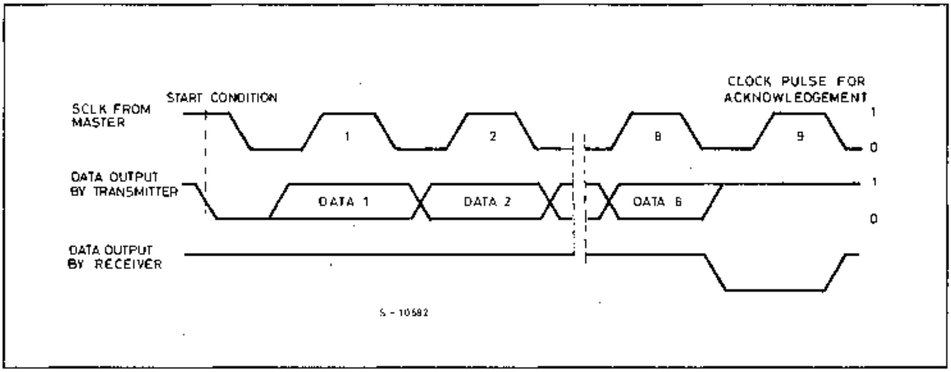
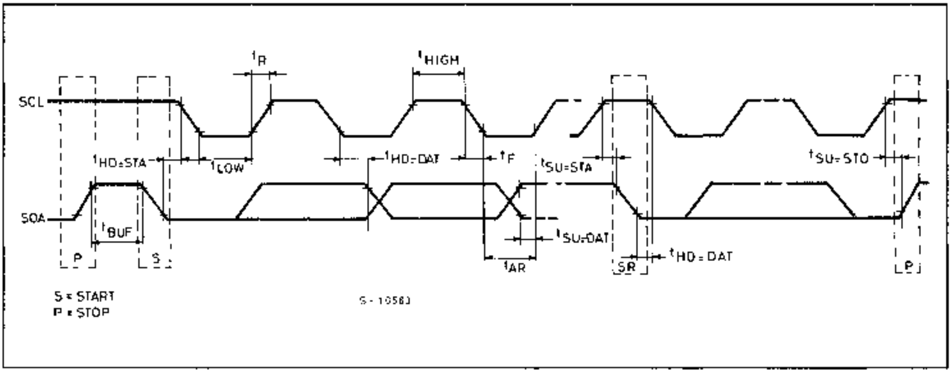

SCLK FROM
MASTER
START CONDITION
CLOCK PULSE FOR
ACKNOWLEDGEMENT
1
2
8
9
1
0
DATA OUTPUT
BY TRANSMITTER
DATA 1
DATA 2
DATA 8
1
0
DATA OUTPUT
BY RECEIVER
S-10582

FIG. 2C - BUS TIMING REQUIREMENTS


SCL
SDA
tR
tHIGH
tHD:STA
tLOW
tHD:DAT
tF
tSU:STA
tSU:STO
tBUF
tSU:DAT
tAR
tHD:DAT
P
S
SR
P
S = START
P = STOP
S-10583

ELECTRICAL CHARACTERISTICS

Standard conditions (unless otherwise moted)

V_{SS} = 0V (GND)
V_{CC} = +5 ±10% volts
Ambient Operating Temperature (T_A): 0°C to +70°C (commercial) −40°C to +85°C (industrial)

Data labeled "typical" is presented for design guidance only and is not guaranteed.

SGS-THOMSON makes no warranty, expressed or implied, as to the merchantability of fitness for a particular purpose of this device or its software supplied to the customer.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DDR}	Operating supply current READ MODE				1	mA
I_{DDW}	Operating supply current WRITE/ERASE Mode				3	mA
I_{DDO}	Operating supply current STANDBY mode (CMOS input)				0.1	mA
I_{IL}	Input leakage current (A_0, A_1, A_2, SCL pins)				10	μA
I_{OH}	Output leakage current HIGH				10	μA
V_{IH}	SCL input and SDA input/output pins: High level input voltage		3.0		$V_{DD}+0.8$	V
V_{IL}	Low level input voltage		−0.3		1.5	V
V_{OL}	Low level output voltage	I_{OL} = 3mA V_{DD} = 4.5V			0.4	V
V_{IH}	High level input voltage	(A_0, A_1, A_2 pins)	$V_{DD}-0.5$		$V_{DD}+0.5$	V
V_{IL}	Low level input voltage	(A_0, A_1, A_2 pins)	−0.3		0.5	V

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
f_{SCL}	SCL clock frequency		0		100	KHz
t_{LOW}	The LOW period of the clock		4.7			μs
t_{HIGH}	The HIGH period of the clock		4.0			μs
t_R	SDA and SCL rise time				1	μs
t_F	SDA and SCL fall time				300	μs
t_{AA}	SCL low to SDA data out		0.3	1.5	3.5	μs
$t_{HD:STA}$	START condition hold time. After this period the first clock pulse is generated		4.0			μs
$t_{SU:STA}$	Setup time for start condition (only relevant for a repeated start condition)		4.7			μs
$t_{SU:DAT}$	Data set-up time		250			ns
$t_{HD:DAT}$	Data hold time		0			μs
$T_{SU:STO}$	STOP condition set-up		4.7			μs
t_{BUF}	Time the bus must be free before a new transmission can start		4.7			μs
$T_{E/W}$	Erase/Write cycle time (per word)				10	ms
$N_{E/W}$	Endurance (number of erase/write cycles)				10000	E/W cycles
t_s	Data retention time		10			Years
C_I	Input capacitance on SCL, SDA				7	pf
T_I	Noise suppresion time constant at SCL and SDA input		0.25	0.5	1.0	μs

Notes: 1. All values referred to V_{IH} and V_{IL} levels
2. Note that a transmitter must internally provide at least time to bridge the undefined region (max. 300 ns) of the edge of SCL.

INTER INTEGRATED CIRCUIT BUS PROTOCOL

The following is a condensed description of each mode of operation.

Chip address (slave address) allocation: The three chip address inputs of each ST24C02 (A_2, A_1, A_0) must be externally connected to either +5V (V_{CC}) or ground (V_{SS}) thereby assigning to each ST24C02 a unique three-bit chip address. Up to eight ST24C02s may be connected to the serial bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected ST24C02. The correct bus protocol is shown in figure 3.

Erase/Write Mode:
In this mode the master transmitter transmits to the ST24C02 slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address, a logic 0 (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the data register. Another 7 data bytes may be strobed in following this in the data register. In the erase/write mode no more than 8 successive data bytes may be strobed into the ST24C02 (Fig. 4a). The ST24C02 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.
After the STOP condition the Erase/Write cycle starts. Its duration is at most 10 ms per data byte. After the receipt of each word, the three low order address bits are internally incremented by one. The high order five bits of the word address remain constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Read mode:

In this mode the master reads the ST24C02 slave after setting the slave address. See figure 5. Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/W = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The ST24C02 slave transmitter will now place the data byte at address An + 1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.
This cycle of reading consecutive addresses will continue until the master receiver send a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the ST24C02 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIG. 3 - SLAVE ADDRESS ALLOCATION

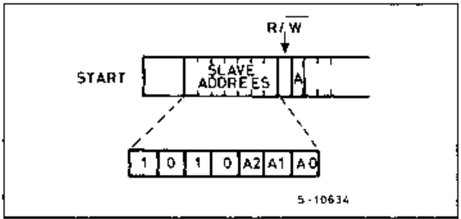


FIG. 4 - BYTE WRITE

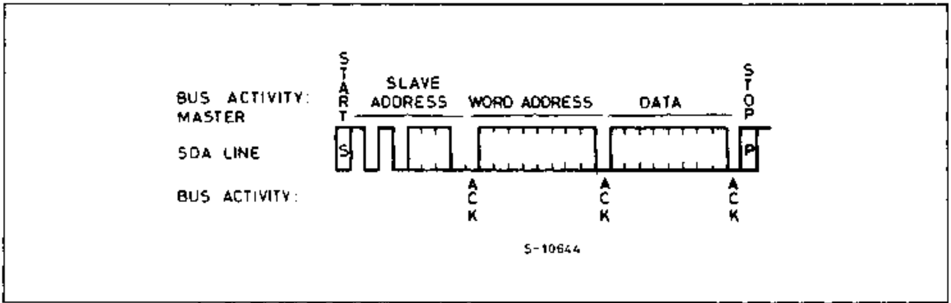


FIG. 4A - PAGE WRITE

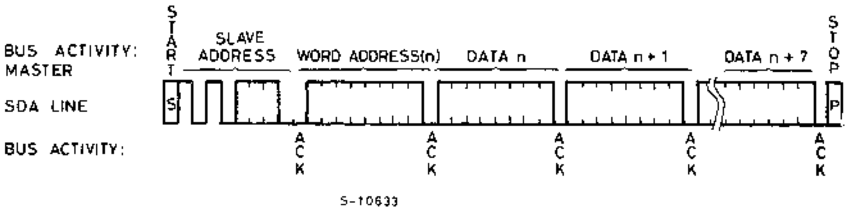

BUS ACTIVITY: MASTER
SDA LINE
BUS ACTIVITY:
START
SLAVE ADDRESS
WORD ADDRESS(n)
DATA n
DATA n + 1
DATA n + 7
STOP
S
P
ACK
ACK
ACK
ACK
ACK
S-10633

FIG. 5 - READ MODE

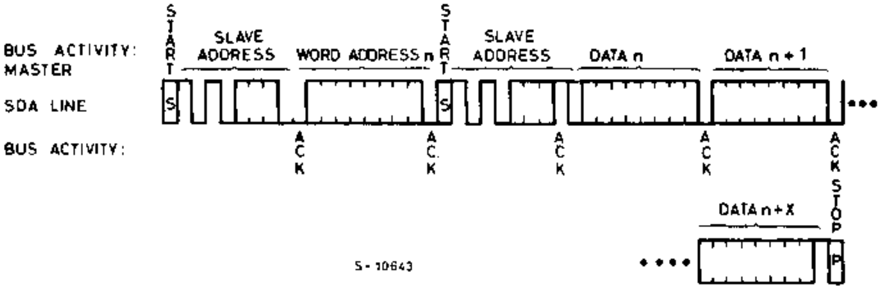
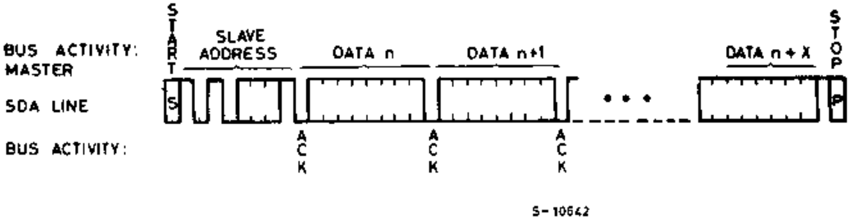

BUS ACTIVITY: MASTER
SDA LINE
BUS ACTIVITY:
START
SLAVE ADDRESS
WORD ADDRESS n
START
SLAVE ADDRESS
DATA n
DATA n + 1
S
S
ACK
ACK
ACK
ACK
ACK
STOP
DATA n + X
P
S-10643

FIG. 6 - ALTERNATE READ MODE

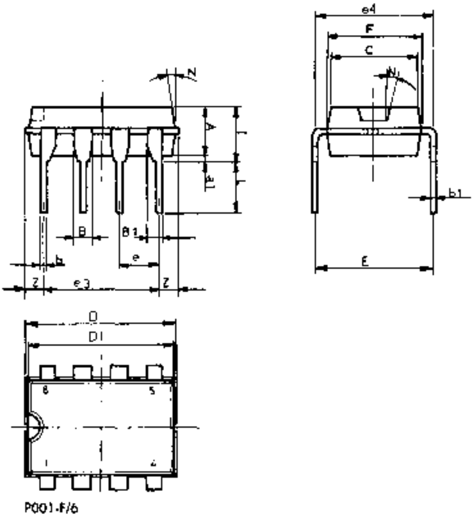

BUS ACTIVITY: MASTER
SDA LINE
BUS ACTIVITY:
START
SLAVE ADDRESS
DATA n
DATA n+1
DATA n + X
STOP
S
P
ACK
ACK
ACK
S-10642

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
ST24C02CP	100 KHz	5V ± 10%	0 to +70°C	DIP-8
ST24C02VP	100 KHz	5V ± 10%	− 40 to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

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TS59C11

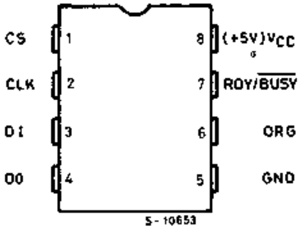
1K BIT SERIAL CMOS EEPROM

- HIGHLY RELIABLE CMOS FLOATING GATE TECHNOLOGY.
- SINGLE 5-VOLT SUPPLY
- EIGHT PIN PACKAGE.
- 64 × 16 OR 128 × 8 USER SELECTABLE SERIAL MEMORY
- COMPATIBLE WITH GENERAL INSTRUMENT GI 5911
- SELF TIMED PROGRAMMING CYCLE
- WORD AND CHIP ERASABLE
- 10,000 ERASE/WRITE CYCLES.
- TEN YEARS DATA RETENTION
- POWER-ON DATA PROTECTION

P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



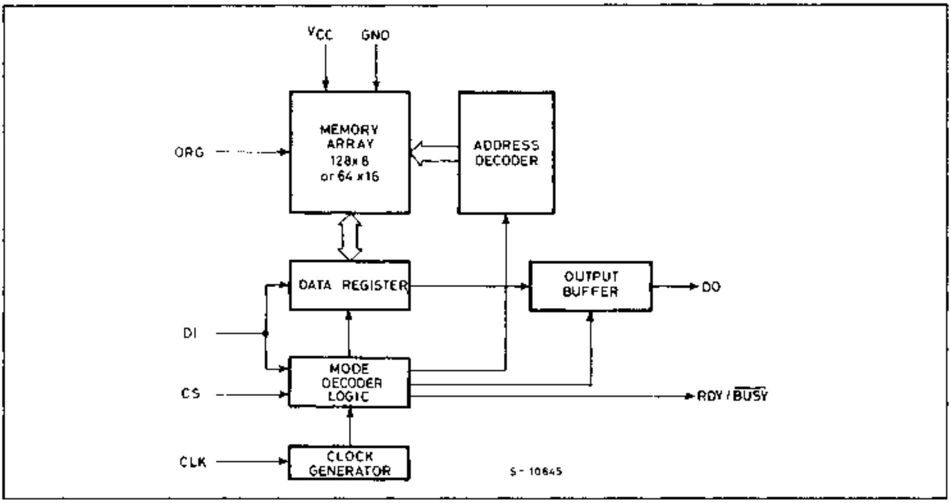
PIN NAMES

CS	CHIP SELECT
CLK	CLOCK INPUT
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
ORG	ORGANIZATION INPUT
R/$\overline{\text{B}}$	READY/$\overline{\text{BUSY}}$ OUTPUT
V_{CC}	+5V POWER SUPPLY
GND	GROUND

PIN DESCRIPTION

Name	No	Description
CS	1	Chip Select
CLK	2	Clock Input
DI	3	Serial Data Input
DO	4	Serial Data Output
GND	5	Ground
ORG	6	Memory Array Organization Selection Input. When the ORG pin is connected to +5, the 64 × 16 organization is selected. When it is connected to ground, the 128 × 8 organization is selected. If the ORG pin is left unconnected, then an internal pull up device will select the 64 × 16 organization.
RDY/$\overline{\text{BUSY}}$	7	Status Output
V_{CC}	8	+5V Power Supply

BLOCK DIAGRAM



INSTRUCTION SET

Instruction	Start bit	Opcode	Address		Data		Comments
			128 × 8	64 × 16	128 × 8	64 × 16	
READ	1	1000	A_6-A_0	A_5-A_0			Read Address A_N-A_O
PROGRAM	1	× 100	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Program Address A_N-A_0
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses
WRAL	1	0001	0000000	000000	D_7-D_0	D15-D_0	Program All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it si possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

POWER-ON DATA PROTECTION CIRCUITRY: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+ 7	V
	Voltage on any input pin	GND − 0.3 to + 7	V
	Voltage or any output pin	V_{CC} + 0.3 GND − 0.3	V
T_{STG}	Storage temperature range	− 65 to + 150	°C
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

READ OPERATION

DC CHARACTERISTICS

$T_{amb} = 0°C$ to $70°C$ for CP, $T_{amb} = -40$ to $+85°C$ for VP, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating voltage		4.5		5.5	V
I_{CC1}	Operating current	$V_{CC} = 5.5V$, $CS = V_{IH}$ CP range VP range			4 4	mA
I_{CC2}	Standby current	$V_{CC} = 5.5V$, $CS = DI = SK = GND + 0.1V)$			100	µA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		$V_{CC} + 1$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1mA$			0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
I_{LI}	Input leakage current	$V_{in} = 5.5V$			10	µA
I_{LO}	Output leakage current	$V_{out} = 5.5V$, $CS = 0$			10	µA

AC CHARACTERISTICS

($T_{amb} = 0°$ to $70°C$ for CP, $T_{amb} = -40$ to $+85°C$ for VP, $V_{CC} = 5V \pm 10\%$ (Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
	SK max (Maximum frequency)				250	KHz
	SK duty cycle		25	50	75	%
T_{CSS}	CS setup time		0.2			µs
T_{CSH}	CS hold time		0			µs
T_{DIS}	DI Setup time		0.4			µs
T_{DIH}	Data input hold time		0.4			µs
T_{CPW}	CLK pulse width		2.0			µs
T_{PD1} T_{PD0}	Data output delay	$CL = 100pF$, $V_{OL} = 0.8V$, $V_{OH} = 2.0V$ and $V_{IH} = 2.4V$, $V_{IL} = 0.45V$			2.0 2.0	µs
t_{PR}	Status low time (programming time)				10	ms

FIG. 1 - SYNCHRONOUS DATA TIMINGS

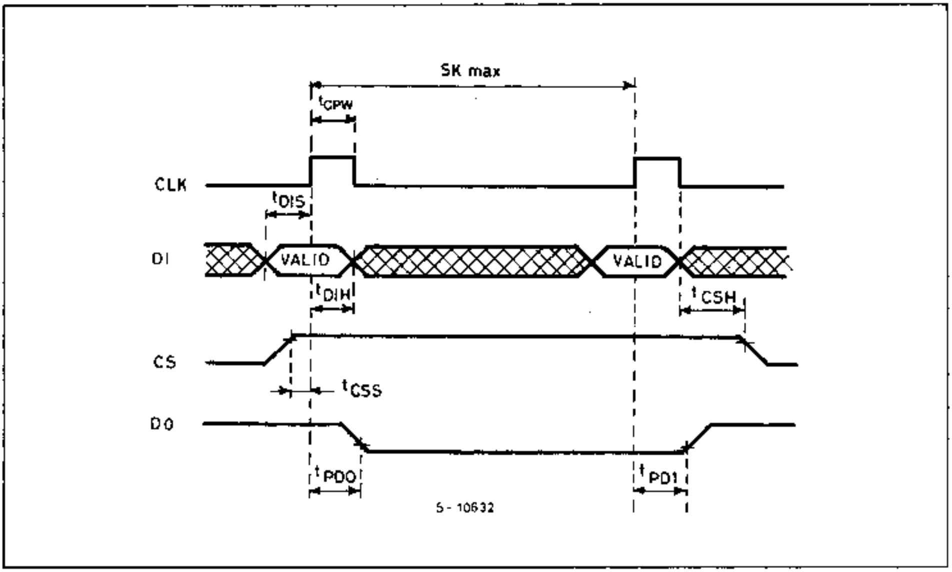
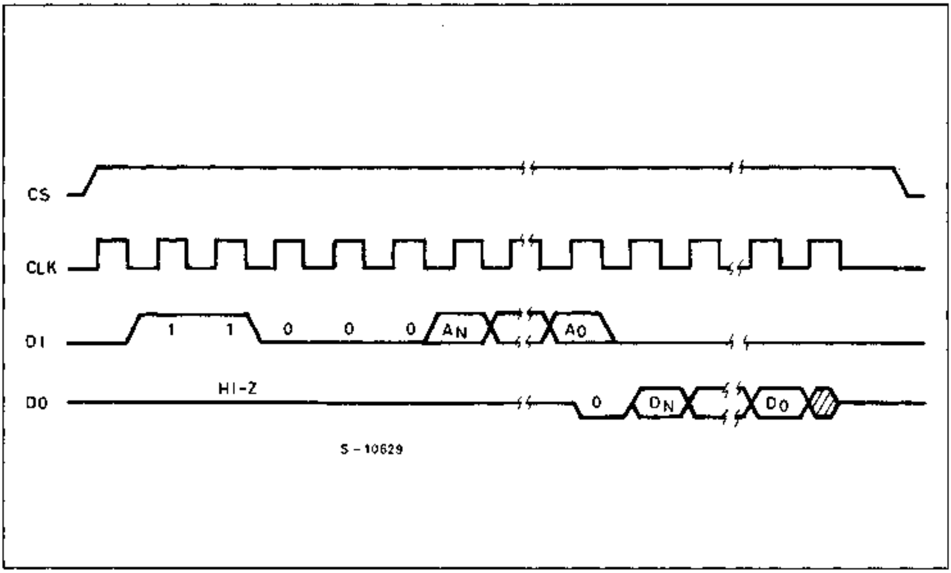

SK max
tCPW
CLK
tDIS
DI
VALID
VALID
tDIH
tCSH
CS
tCSS
DO
tPD0
tPD1
S - 10632

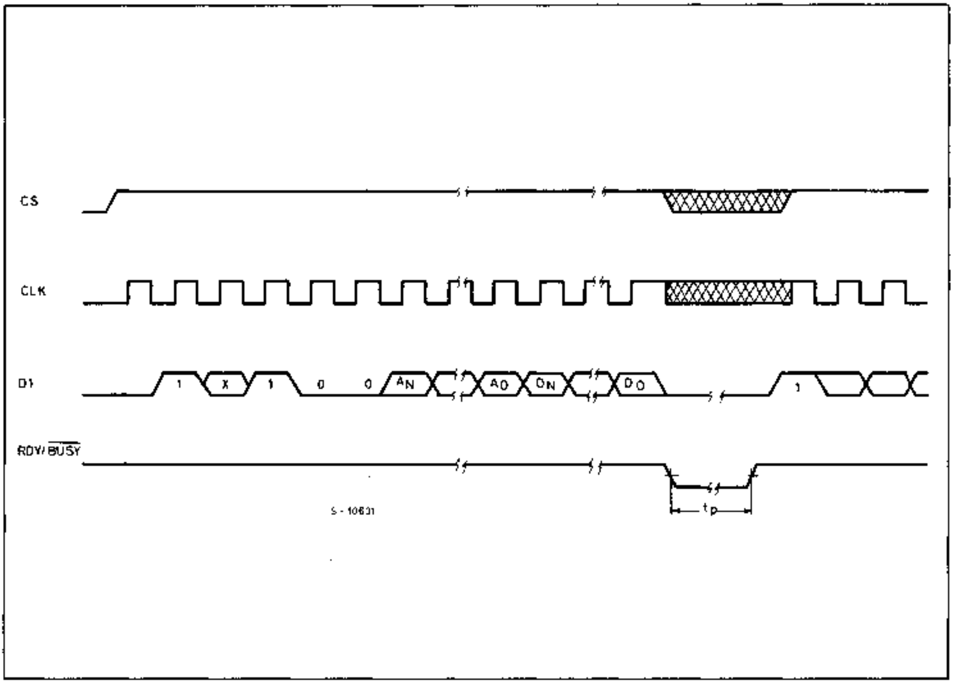
FIG. 2 - READ MODE


CS
CLK
DI
1
1
0
0
0
AN
A0
DO
HI-Z
0
DN
D0
S - 10629

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ isntruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") precedes the data output string. The output data changes during the high states of the system clock.

Organization	A_N	D_N
128 × 8	A_6	D_7
64 × 16	A_5	D_{15}

FIG. 3 - PROGRAM MODE



The PROGRAM instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

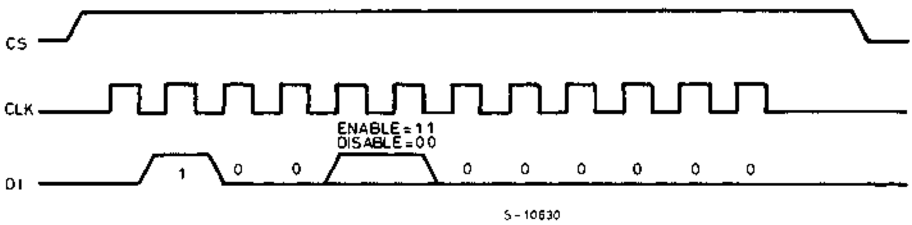
After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/$\overline{BUSY}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

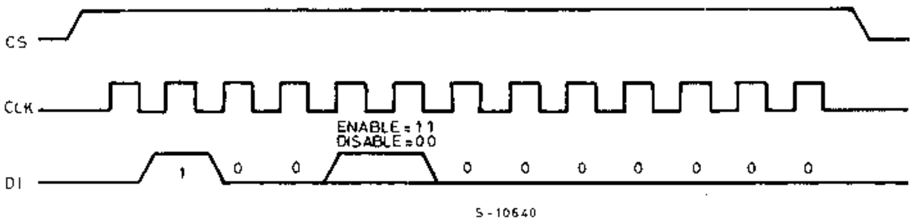
During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Organization	A_N	D_N
128 × 8	A_6	D_7
64 × 16	A_5	D_{15}

FIG. 4 - PEN (Program enable) AND PDS (Program Disable)


CS
CLK
ENABLE = 11
DISABLE = 00
DI
1
0
0
0
0
0
0
0
0
S - 10630

PEN and PDS for 128 × 8 organization


CS
CLK
ENABLE = 11
DISABLE = 00
DI
1
0
0
0
0
0
0
0
0
0
S - 10640

PEN and PDS for 64x16 organization

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

FIG. 5a - ERAL (Erase all) MODE for 128 × 8 Organization

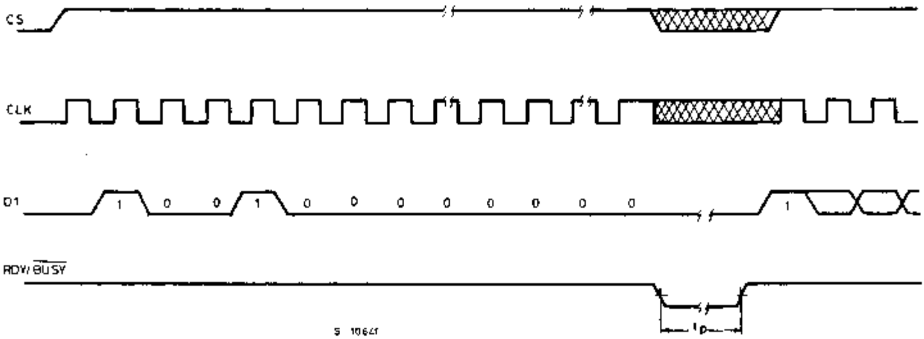
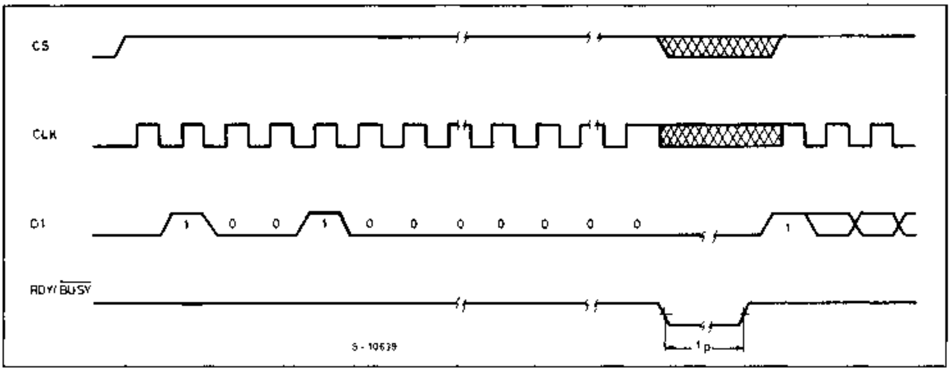

CS
CLK
D1
1
0
0
1
0
0
0
0
0
0
0
0
1
RDY/$\overline{\text{BUSY}}$
S 10641
tp

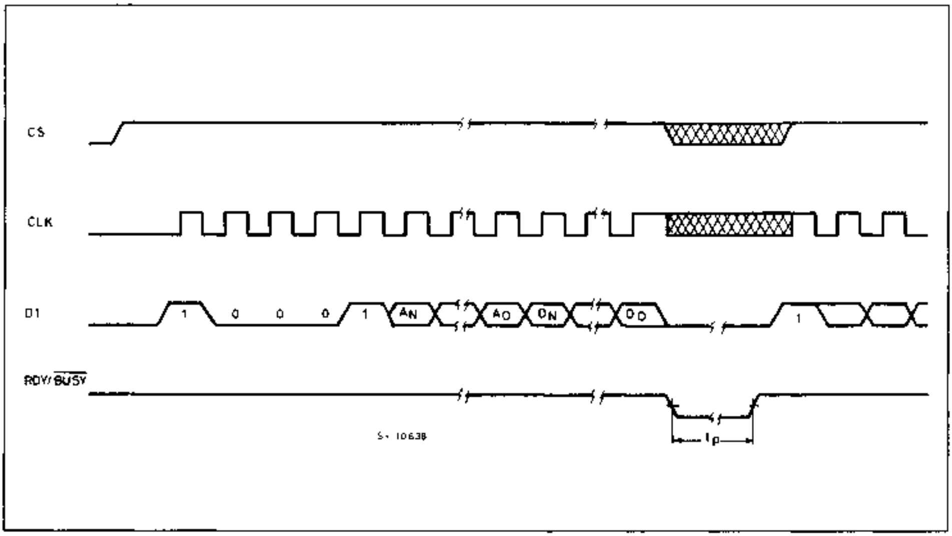
FIG. 5b - ERAL (Erase all) MODE for 64 × 16 Organization


CS
CLK
D1
1
0
0
1
0
0
0
0
0
0
0
1
RDY/$\overline{BUSY}$
S - 10639
tp

Entire chip erasing is provided for ease of clearing the whole memory and is implemented with the ERAL (erase all registers) instruction.

Erasing the chip means that all registers in the memory array have each bit set to a 1.

FIG. 6 - WRAL MODE


CS
CLK
D1
1
0
0
0
1
AN
A0
DN
D0
1
RDY/$\overline{BUSY}$
S - 10638
tp

The WRAL instruction is followed by either eight or sixteen bits of data. After the last data bit (D_0) has been shifted into the data register the contents of all adresses will be erased an the new data written to all adresses. The pre-erasing and writing of new data occur automatically and are self-timed on-chip.

During the automatic erase/write sequence the RDY/$\overline{DUSY}$ output will low for the duration of the automatic programming cycle as indicated by tp.

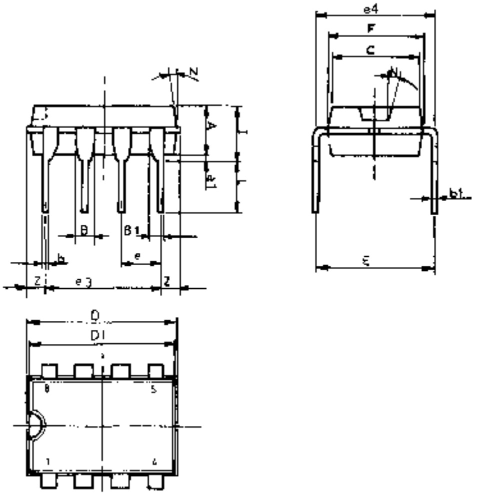
Organization	A_N-A_0	D_N
128 × 8	0000000	D_7
64 × 16	000000	D_{15}

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
TS59C11CP	250 KHz	5V ± 10%	0 to +70°C	DIP-8
TS59C11VP	250 KHz	5V ± 10%	−40 to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

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TS93C46

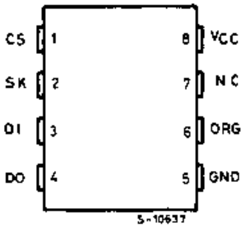
1K BIT SERIAL CMOS EEPROM

- HIGHLY RELIABLE CMOS FLOATING GATE TECHNOLOGY.
- SINGLE 5-VOLT SUPPLY
- EIGHT PIN PACKAGE.
- 64 × 16 OR 128 × 8 USER SELECTABLE SERIAL MEMORY
- COMPATIBLE WITH NATIONAL SEMICONDUCTOR NMC 9346 and NMC 9306
- SELF TIMED PROGRAMMING CYCLE.
- WORD AND CHIP ERASABLE
- 10,000 ERASE/WRITE CYCLES.
- TEN YEARS DATA RETENTION
- POWER-ON DATA PROTECTION

P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS



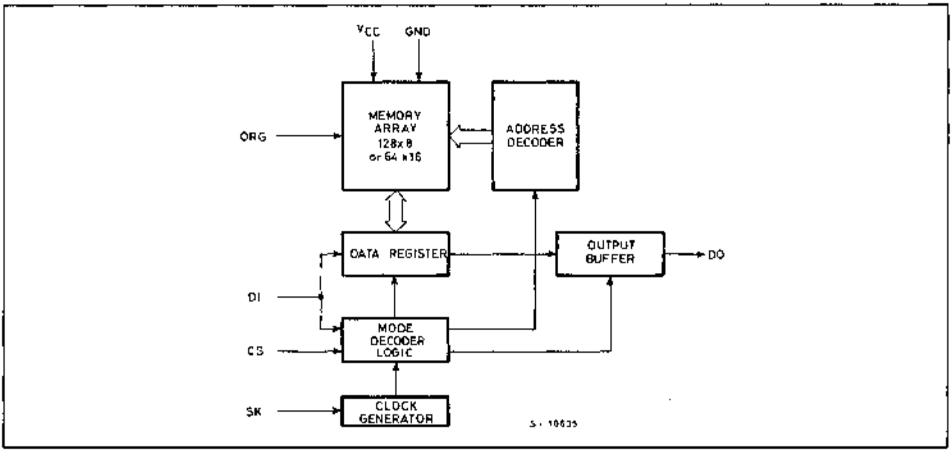
PIN NAMES

CS	CHIP SELECT
SK	CLOCK INPUT
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
ORG	ORGANIZATION INPUT
V_{CC}	+5V POWER SUPPLY
GND	GROUND
NC	NO CONNECT

PIN DESCRIPTION

Name	No	Description
CS	1	Chip Select
SK	2	Clock Input
DI	3	Serial Data Input
DO	4	Serial Data Output
GND	5	Ground
ORG	6	Memory Array Organization Selection Input. When the ORG pin is connected to +5, the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull up device will select the 64 x 16 organization.
V_{CC}	8	+5V Power Supply

BLOCK DIAGRAM



INSTRUCTION SET

Instruction	Start bit	Opcode	Address		Data		Comments
			128 × 8	64 × 16	128 × 8	64 × 16	
READ	1	10	A_6-A_0	A_5-A_0			Read Address A_N-A_O
ERASE	1	11	A_6-A_0	A_5-A_0			Erase Address A_N-A_0
WRITE*	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{16}-D_0	Write Address A_N-A_0
EWEN	1	00	11xxxxx	11xxxx			Program Enable
EWDS	1	00	00xxxxx	00xxxx			Program Disable
ERAL	1	00	10xxxxx	10xxxx			Erase All Addresses
WRAL	1	00	01xxxxx	01xxxx	D_7-D_0	D15-D_0	Program All Addresses

* Write instruction is a self timed program instruction. The selected byte (word) gets erased before being written.

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it si possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

POWER-ON DATA PROTECTION CIRCUITRY: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	+ 7	V
	Voltage on any input pin	GND − 0.3 to + 7	V
	Voltage or any output pin	V_{CC} + 0.3 GND − 0.3	V
T_{STG}	Storage temperature range	− 65 to + 150	°C
	Lead temperature (Soldering: 10 seconds)	+ 300	°C

READ OPERATION

DC CHARACTERISTICS

(T_{amb} = 0° to 70°C for CP, T_{amb} = − 40 to + 85°C for VP, V_{CC} = 5V ± 10%; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Operating voltage		4.5		5.5	V
I_{CC1}	Operating current	V_{CC} = 5.5V, CS = V_{IH} CP range VP range			 4 4	mA
I_{CC2}	Standby current	V_{CC} = 5.5V, CS = DI = SK = GND + 0.1V)			100	μA
V_{IL}	Input low voltage		− 0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC} + 1	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.4			V
I_{LI}	Input leakage current	V_{in} = 5.5V			10	μA
I_{LO}	Output leakage current	V_{out} = 5.5V, CS = 0			10	μA

AC ELECTRICAL CHARACTERISTICS

(T_{amb} = 0° to 70°C for CP T_{amb} = − 40 to + 85°C for VP, V_{CC} = 5V ± 10%; Unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
	SK max (Maximum frequency)				250	KHz
	SK duty cycle		25	50	75	%
T_{CSS}	CS setup time		0.2			μs
T_{CSH}	CS hold time		0			μs
T_{DIS}	DI Setup time		0.4			μs
T_{DIH}	Data input hold time		0.4			μs
T_{PD1} T_{PD0}	Data output delay	CL = 100pF, V_{OL} = 0.8V, V_{OH} = 2.0V and V_{IH} = 2.4V, V_{IL} = 0.45V			2.0 2.0	μs
T_{HZ}	Output delay to Hi Z				0.4	μs
$T_{E/W}$	Erase/write pulse width				10	ms
T_{CS}	Min. CS low time		1			μs
T_{SKHI}	SK high time		1			μs
T_{SKLOW}	SK low time		1			μs
T_{SV}	Output delay to status valid				1	μs

DEVICE OPERATION

The TS93C46 is a serial Eeprom memory featuring a software programmable organization: 128 × 8 bit or 64 × 16 bit. It has 7 instructions that allow it to read, erase or write.

Each instruction consists of a start bit (logical "1"), an opcode field (2 bits), an address field (6 or 7 bits) and optionaly a data field (8 or 16 bits) — Address and data fields length depending on organization × 8 or × 16.

The DO pin is a multiplexed pin. It is used as data out during the read mode. It can also be used as a ready/busy indicator in programming mode. In all other modes, DO is tri-stated.

During power-up, all modes of operation are disabled, and the device comes up in a program-disabled state. An EWEN instruction has to be issued before starting programming.

READ

The READ instruction reads the content of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

ERASE/WRITE ENABLE AND DISABLE

After power-up and before starting any programming instruction, the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The read instruction is independent from the EWEN and EWDS instructions.

ERASE

After an ERASE instruction has been shifted in, CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing TCS spec), the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to al logical "1".

WRITE

After a WRITE instruction has been shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming cycle. The addressed register will first be automatically erased and then the previously shifted data will be written in the register. If CS is brought high during the programming time (after observing the TCS spec), the DO pin will act as a status indicator-it will remain low a long as the chip is programming. It will go high after all the bits of the addressed register have been set to the proper value.

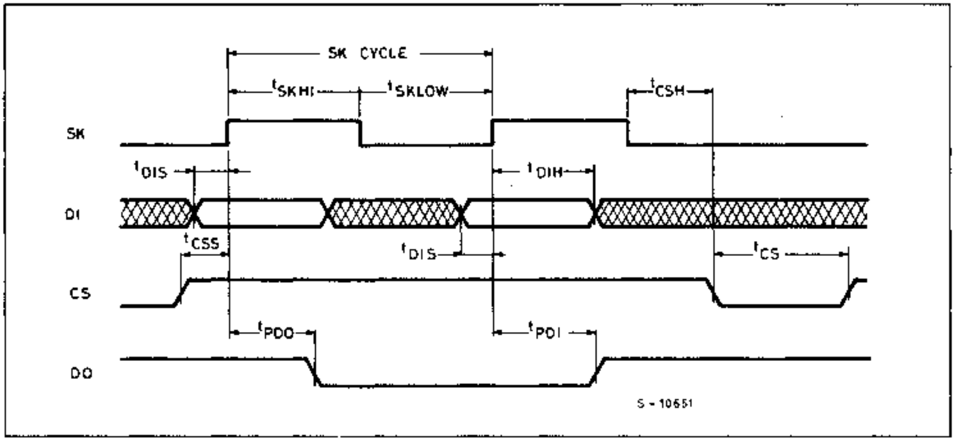
ERASE ALL

This instruction is provided to erase the whole chip. It works the same way as the erase instruction does.

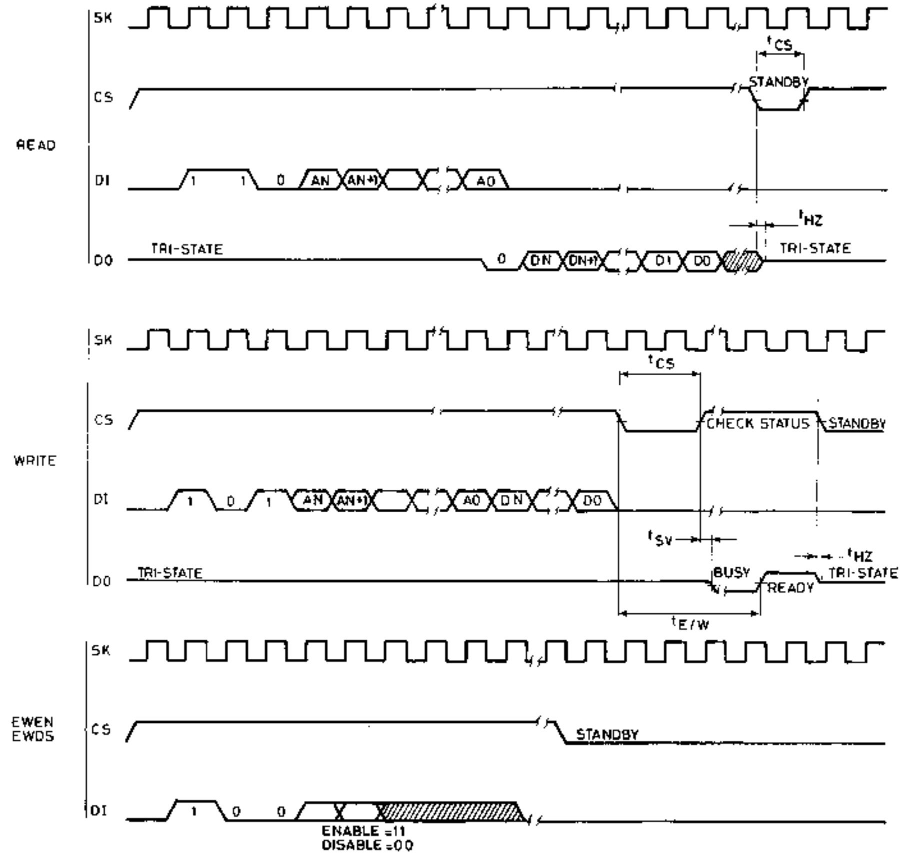
WRITE ALL

This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. The WRAL instruction works the same way as the write instruction does.

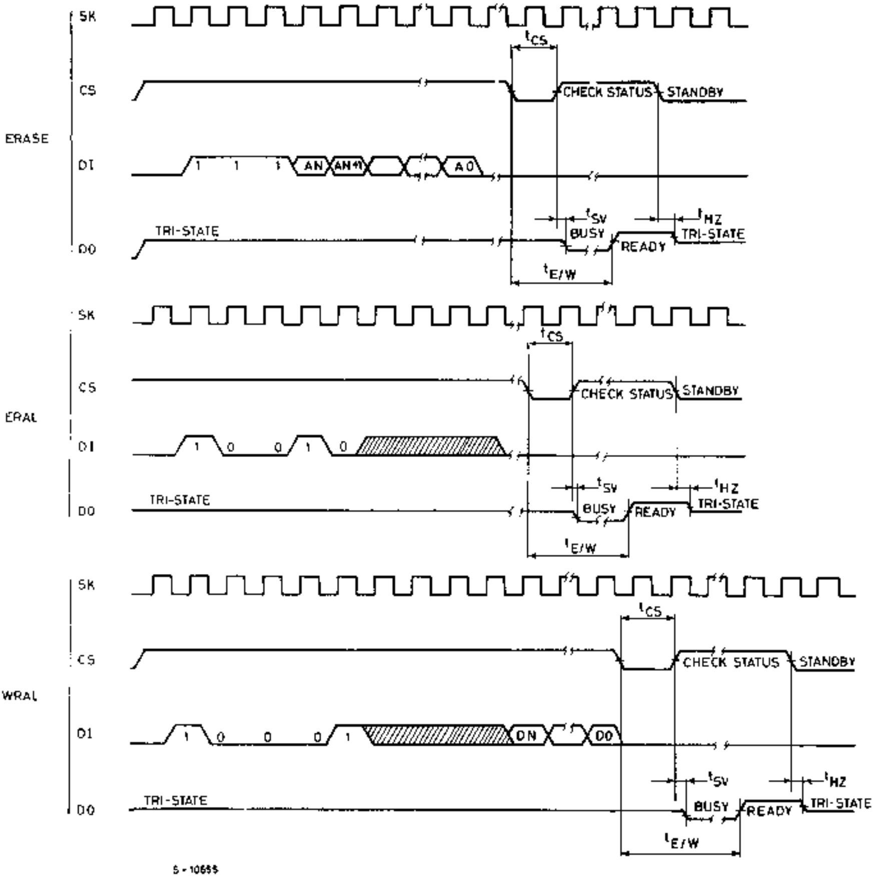
SYNCHRONOUS TIMINGS



INSTRUCTION TIMINGS


READ
SK
CS
DI
DO
tCS
STANDBY
1
1
0
AN
AN+1
A0
tHZ
TRI-STATE
0
DN
DN+1
D1
D0
TRI-STATE
WRITE
SK
CS
DI
DO
tCS
CHECK STATUS
STANDBY
1
0
1
AN
AN+1
A0
DN
D0
tSV
tHZ
TRI-STATE
BUSY
READY
TRI-STATE
tE/W
EWEN
EWDS
SK
CS
DI
STANDBY
1
0
0
ENABLE =11
DISABLE =00
S -10654

INSTRUCTION TIMINGS (Continued)

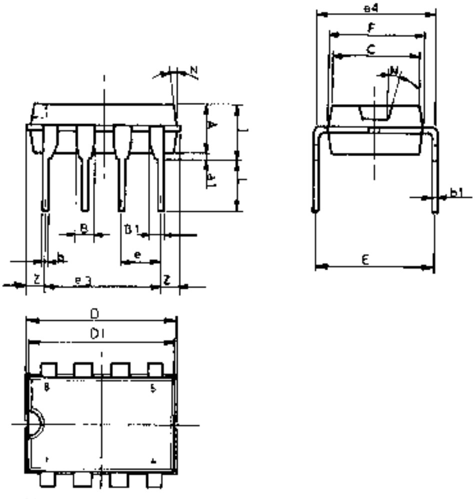

SK
CS
ERASE
DI
DO
1
1
1
AN
AN-1
A0
t_{CS}
CHECK STATUS
STANDBY
t_{SV}
t_{HZ}
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$
SK
CS
ERAL
DI
DO
1
0
0
1
0
t_{CS}
CHECK STATUS
STANDBY
t_{SV}
t_{HZ}
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$
SK
CS
WRAL
DI
DO
1
0
0
0
1
DN
D0
t_{CS}
CHECK STATUS
STANDBY
t_{SV}
t_{HZ}
TRI-STATE
BUSY
READY
TRI-STATE
$t_{E/W}$
S-10655

ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
TS93C46CP	250 KHz	5V ± 10%	0 to +70°C	DIP-8
TS93C46VP	250 KHz	5V ± 10%	– 40 to +85°C	DIP-8

PACKAGE MECHANICAL DATA

8-PIN PLASTIC DIP



P001-F/6

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.169
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

SGS-THOMSON
MICROELECTRONICS

ST93C56

2K BIT (128 × 16) SERIAL CMOS EEPROM

ADVANCE DATA

- 128 × 16 SERIAL EEPROM
- SINGLE POWER SUPPLY = FROM 2.7 TO 5.5. VOLTS
- 10 YEAR DATA RETENTION AFTER 100.000 ERASE/WRITE CYCLES PER WORD
- CMOS LOW POWER CONSUMPTION = 3 MA MAX ACTIVE CURRENT AND 0.1 MA MAX STANDBY CURRENT
- 4 BYTE WRITE MODE
- SELF TIMED PROGRAMMING CYCLE (WITH AUTOERASE)
- WRITE PROTECTION IN USER DEFINED SECTION OF MEMORY
- SEQUENTIAL REGISTER READ

P
DIP-8
(Plastic)

M
SO14
(Plastic Micropackage)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The ST93C56 is a 2048 bit non-volatile sequential access memory manufactured using SGS-THOMSON Single Floating Gate process.

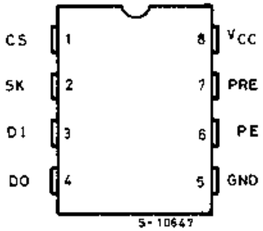
It is designed to operate from 3 to 5 Volts in order to match telecommunications requirements.

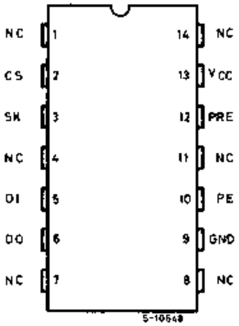
Moreover, a double cell per bit architecture will allow to guarantee 100K erase/write cycles.

PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
GND	GROUND
PE	PROGRAM ENABLE
PRE	PROTECT REGISTER ENABLE
V_{CC}	POWER SUPPLY
NC	NO CONNECT

PIN CONNECTIONS

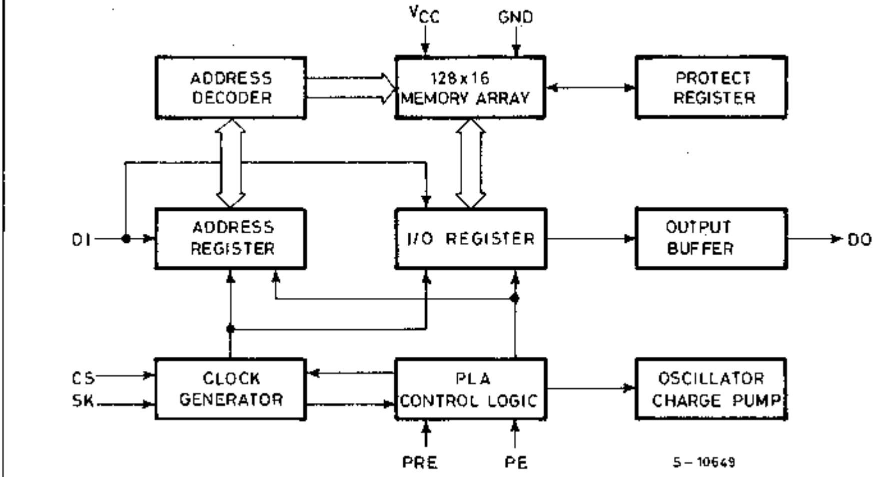




June 1988

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM


VCC
GND
ADDRESS DECODER
128 x 16 MEMORY ARRAY
PROTECT REGISTER
DI
ADDRESS REGISTER
I/O REGISTER
OUTPUT BUFFER
DO
CS
SK
CLOCK GENERATOR
PLA CONTROL LOGIC
OSCILLATOR CHARGE PUMP
PRE
PE
5 – 10649

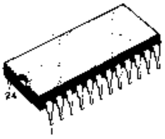
ROM DEVICES

SGS-THOMSON
MICROELECTRONICS

M2316H

16K-BIT READ ONLY MEMORY

- SINGLE + 5V ± 10% POWER SUPPLY
- ACCESS TIME 300 ns (MAX)
- COMPLETELY STATIC OPERATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- THREE PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- THREE STATE OUTPUTS FOR DIRECT BUS INTERFACE
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS



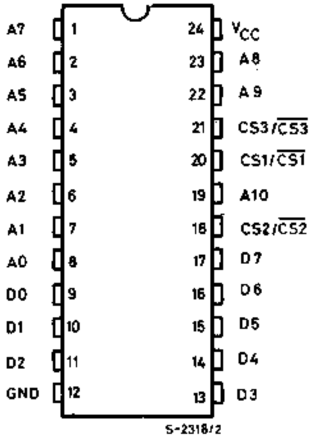
B
DIP-24
(Plastic Package)

(Ordering Information at the end of the datasheet)

DESCRIPTION

The M2316H is a 16,384-bit static Read Only Memory organized as 2,048 by 8 bits.
It is manufactured using SGS-THOMSON' high density N-channel Si-Gate MOS process and is ideal for non volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.
The M2316H is available in 24-lead dual in line plastic or ceramic packages.

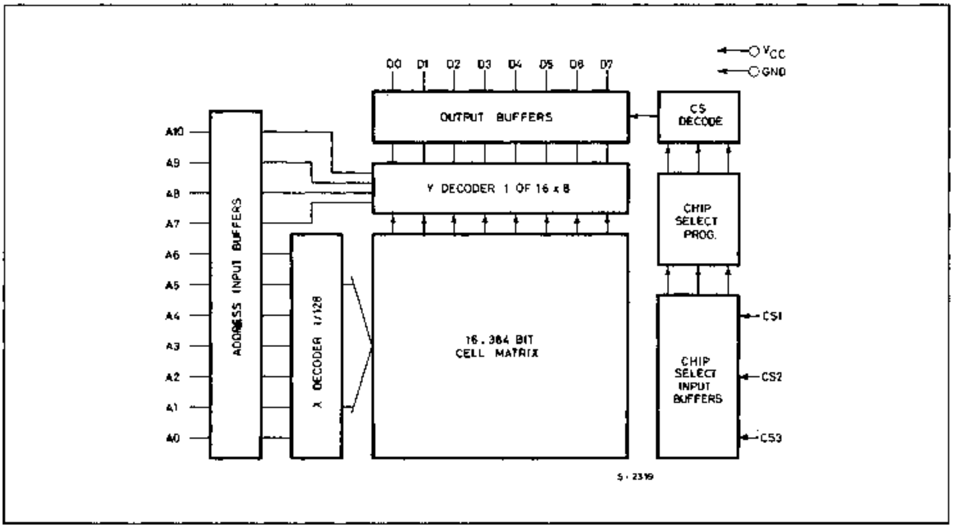
PIN CONNECTIONS


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
D0 9
D1 10
D2 11
GND 12
24 V_{CC}
23 A8
22 A9
21 CS3/$\overline{CS3}$
20 CS1/$\overline{CS1}$
19 A10
18 CS2/$\overline{CS2}$
17 D7
16 D6
15 D5
14 D4
13 D3
S-2318/2

PIN NAMES

A0-A10	ADDRESS INPUTS
D0-D7	DATA OUTPUTS
CS1-CS3	CHIP SELECT INPUTS

BLOCK DIAGRAM

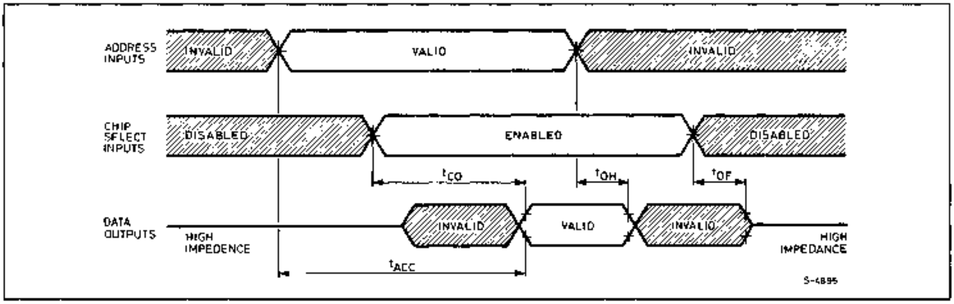

O0
O1
O2
O3
O4
O5
O6
O7
V_{CC}
GND
OUTPUT BUFFERS
CS DECODE
Y DECODER 1 OF 16 x 8
CHIP SELECT PROG.
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
ADDRESS INPUT BUFFERS
X DECODER 1/128
16,384 BIT CELL MATRIX
CHIP SELECT INPUT BUFFERS
CS1
CS2
CS3
S-2319

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any pin with respect to ground	– 0.5 to + 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package plastic package	– 65 to + 150 – 55 to + 125	°C °C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS


ADDRESS INPUTS
INVALID
VALID
INVALID
CHIP SELECT INPUTS
DISABLED
ENABLED
DISABLED
t_{CO}
t_{OH}
t_{OF}
DATA OUTPUTS
HIGH IMPEDENCE
INVALID
VALID
INVALID
HIGH IMPEDANCE
t_{ACC}
S-4895

STATIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$, $I_{OH} = -400\ \mu A$	2.4		V_{CC}	V
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	μA
V_{IL}	Input Low Voltage	See Note 1	– 0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	V
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		40	70	mA

Note 1: Input levels that swing more negative than – 0.5V will be clamped and may cause damage to the device.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min	Typ.	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pf			300	ns
t_{CO}	Chip Select Delay				100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns			100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	10			ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

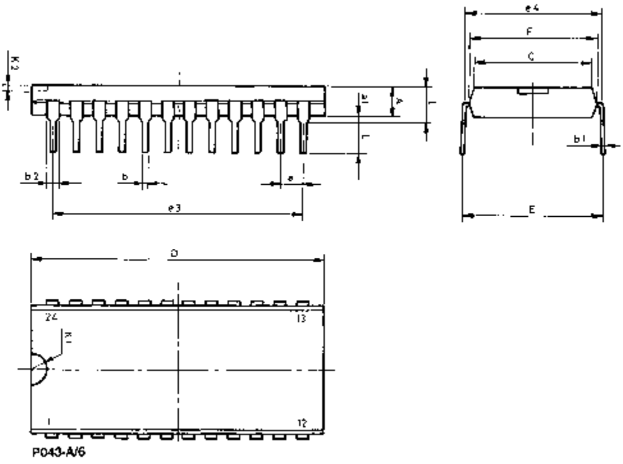
Note 2: This parameter is sampled periodically and is not 100% tested.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2316HB1	300ns	5V ± 10%	0° to +70°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN PLASTIC DIP


e4
F
C
b1
E
K2
a1
A
I
L
b2
b
e
e3
D
24
13
K1
1
12
P043-A/6

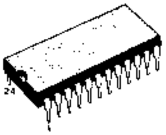
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.024	
B		0.45			0.017	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			32.20			1.267
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		27.94			1.100	
e4						
F			14.10			0.555
I	4.45		0.175			
L	3.30		0.129			
K1						
K2						

SGS-THOMSON
MICROELECTRONICS

M2332
M2333

32K-BIT READ ONLY MEMORY

- M2332-2532 EPROM PIN COMPATIBLE
- M2333-2732 EPROM PIN COMPATIBLE
- SINGLE +5V ± 10% POWER SUPPLY
- ACCESS TIME 250ns (MAX)
- COMPLETELY STATIC OPERATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- TWO PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- 2716/2532/2732 EPROMs ACCEPTED AS PROGRAM DATA INPUTS.
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE



B
DIP-24
(Plastic Package)

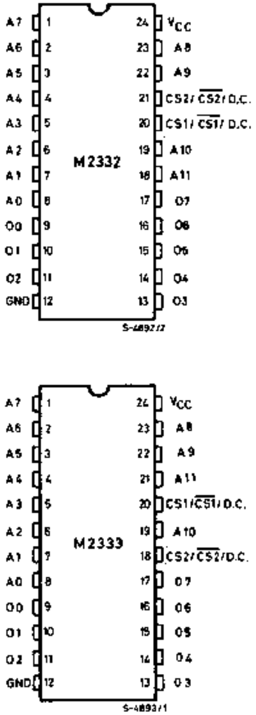
(Ordering Information at the end of the datasheet)

DESCRIPTION

The M2332 and M2333 are 32,768-bit static Read Only Memories organized as 4,096 by 8 bits. They are manufactured using our high density N-channel Si-Gate MOS process and are ideal for large, non-volatile data storage applications such as program storage.

The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.
The M2332 and M2333 are available in 24-lead dual-in-line plastic or ceramic packages.

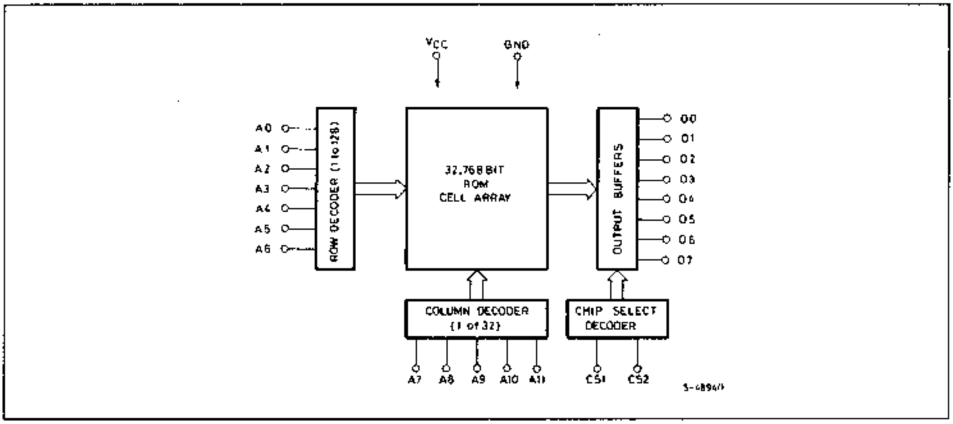
PIN CONNECTIONS


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 CS2/$\overline{CS2}$/D.C.
20 CS1/$\overline{CS1}$/D.C.
19 A10
18 A11
17 O7
16 O6
15 O5
14 O4
13 O3
M2332
S-4892/2
A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 A11
20 CS1/$\overline{CS1}$/D.C.
19 A10
18 CS2/$\overline{CS2}$/D.C.
17 O7
16 O6
15 O5
14 O4
13 O3
M2333
S-4893/1

PIN NAMES

A0-A11	ADDRESS INPUT
O0-O7	DATA OUTPUT
CS1-CS2	CHIP SELECT INPUTS
V_{CC}	POWER SUPPLY
GND	GROUND

BLOCK DIAGRAM

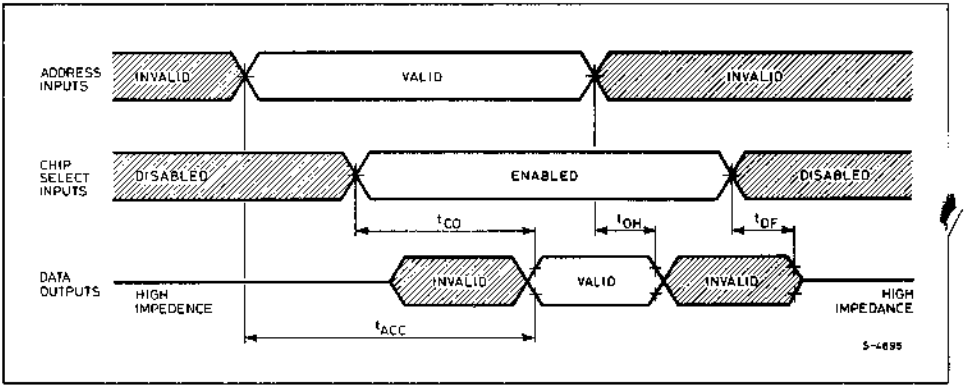

VCC
GND
A0
A1
A2
A3
A4
A5
A6
ROW DECODER (1 to 128)
32,768 BIT ROM CELL ARRAY
OUTPUT BUFFERS
O0
O1
O2
O3
O4
O5
O6
O7
COLUMN DECODER (1 of 32)
CHIP SELECT DECODER
A7
A8
A9
A10
A11
CS1
CS2
S-4894/1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to ground	− 0.5 to + 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: for ceramic package for plastic package	−65 to +150 −55 to +125	°C °C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS


ADDRESS INPUTS
INVALID
VALID
INVALID
CHIP SELECT INPUTS
DISABLED
ENABLED
DISABLED
t_{CO}
t_{OH}
t_{DF}
DATA OUTPUTS
HIGH IMPEDENCE
INVALID
VALID
INVALID
HIGH IMPEDANCE
t_{ACC}
S-4695

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leq V_{IN} \leq 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = +0.4V$ to V_{CC}			10	μA
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			70	mA
V_{IL}	Input Low Voltage	See Note 1	−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$ $I_{OH} = -400$ μA	2.4		V_{CC}	V

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2332-33/D1		Unit
			Min	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL Load and 100 pF		250	ns
t_{CO}	Chip Selected Delay			100	ns
t_{DF}	Chip Deselected Delay	Input transition time: 20 ns		100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	20		ns

CAPACITANCE ($T_{amb} = 25°C$, f = 1 MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

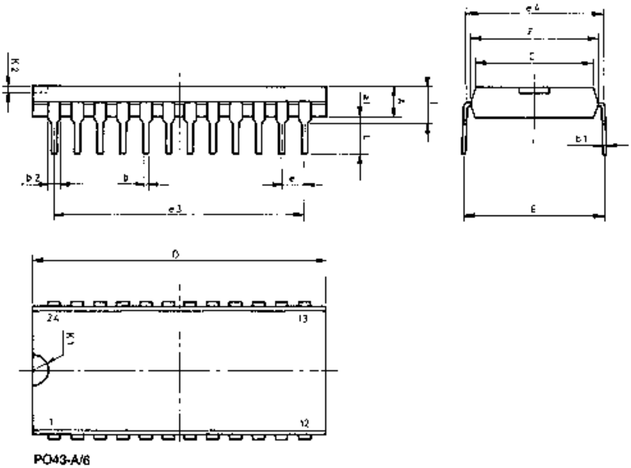
Note 2: This parameter is sampled periodically and is not 100% tested.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2332B1	250	5V ± 10%	0° to + 70°C	DIP-24
M2333B1	250	5V ± 10%	0° to + 70°C	DIP-24

PACKAGE MECHANICAL DATA

24-PIN PLASTIC DIP



PO43-A/6

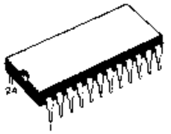
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.024	
B		0.45			0.017	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			32.20			1.267
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		27.94			1.100	
e4						
F			14.10			0.555
I	4.45		0.175			
L	3.30		0.129			
K1						
K2						

SGS-THOMSON
MICROELECTRONICS

M2364

64K-BIT READ ONLY MEMORY

- ACCESS TIME 250 ns (MAX)
- COMPLETELY STATIC OPERATION
- SINGLE +5V ±10% POWER SUPPLY
- 8192 × 8 BIT ORGANISATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- PROGRAMMABLE CHIP SELECT
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS



B
DIP-24
(Plastic Package)

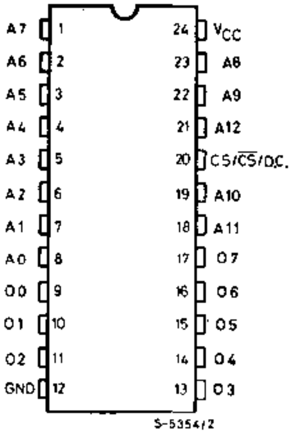
(Ordering Information at the end of the datasheet)

DESCRIPTION

The M2364 is a 65,536-bit static Read Only Memory organized as 8,192 by 8 bits.

It is manufactured using our high density N-channel Si-gate MOS process and is ideal for non-volatile data storage applications where high performance, large bit storage and simple interfacing are important design considerations.
The M2364 is available in 24-lead dual in-line plastic or ceramic package.

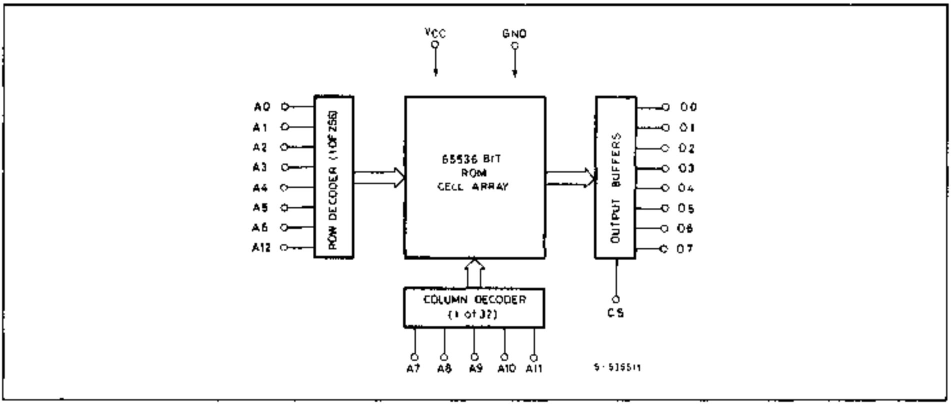
PIN CONNECTIONS


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 V_{CC}
23 A8
22 A9
21 A12
20 CS/$\overline{CS}$/D.C.
19 A10
18 A11
17 O7
16 O6
15 O5
14 O4
13 O3
S-5354/2

PIN NAMES

A0-A12	ADDRESS INPUTS
O0-O7	DATA OUTPUTS
CS/$\overline{CS}$-DC	CHIP SELECT INPUT
VCC	POWER SUPPLY
GND	GROUND

BLOCK DIAGRAM

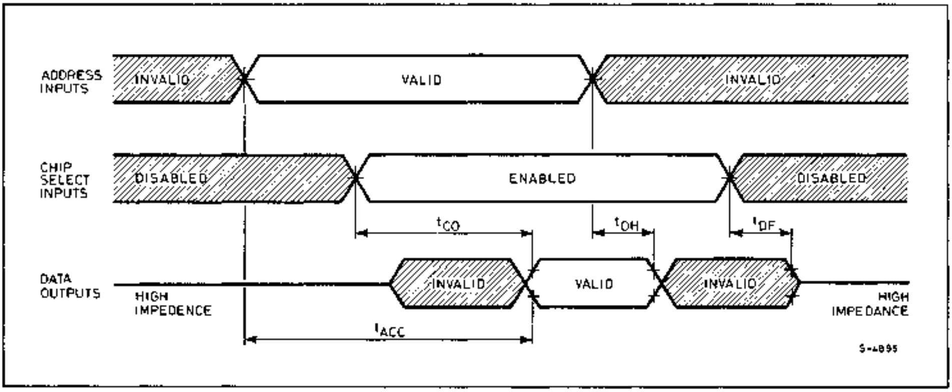

VCC
GND
A0
A1
A2
A3
A4
A5
A6
A12
ROW DECODER (1 OF 256)
65536 BIT ROM CELL ARRAY
OUTPUT BUFFERS
O0
O1
O2
O3
O4
O5
O6
O7
COLUMN DECODER (1 of 32)
CS
A7
A8
A9
A10
A11
S-535511

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to Ground	+0.5 to − 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package plastic package	−65 to +150 −55 to +125	°C °C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAFEFORMS


ADDRESS INPUTS
INVALID
VALID
INVALID
CHIP SELECT INPUTS
DISABLED
ENABLED
DISABLED
t_{CO}
t_{OH}
t_{DF}
DATA OUTPUTS
HIGH IMPEDENCE
INVALID
VALID
INVALID
HIGH IMPEDANCE
t_{ACC}
S-4895

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leq V_{IN} \leq 5.5V$			10	μA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	μA
V_{IL}	Input Low Voltage	See note 1	−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $V_{CC} = 4.5V$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA $V_{CC} = 4.5V$	2.4		V_{CC}	V
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			80	mA

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2364		Unit
			Min	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pF		250	ns
t_{CO}	Chip Select Delay			100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns		100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5 V Output: 0.8V and 2.0V	10		ns

CAPACITANCE ($T_{amb} = 25°C$, $f = 1$ MHz, see Note 2))

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

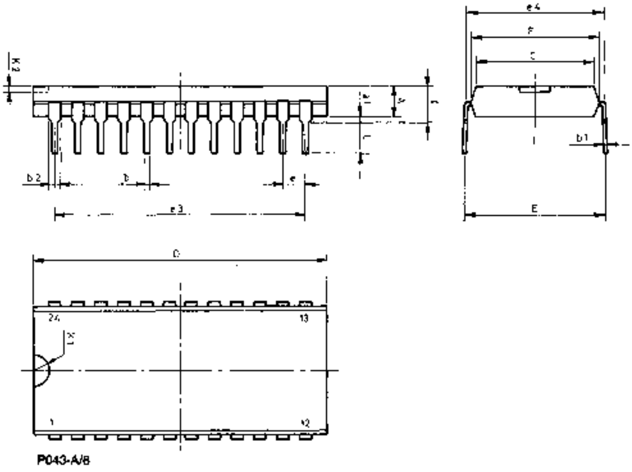
Note 2: This parameter is sampled periodically and is not 100%, tested.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2364B1	250ns	5V ± 10%	0° to +70°C	DIP-24

PACKAGE MECHANICAL DATA

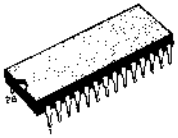
24-PIN PLASTIC DIP


K2
b2
b
e
e3
D
24
13
1
12
K1
e4
F
C
I
b1
E
L
a1
P043-A/8

Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.024	
B		0.45			0.017	
b 1	0.23		0.31	0.009		0.012
e 2		1.27			0.050	
C						
D			32.20			1.267
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		27.94			1.100	
e4						
F			14.10			0.555
I	4.45		0.175			
L	3.30		0.129			
K1						
K2						

64K-BIT READ ONLY MEMORY

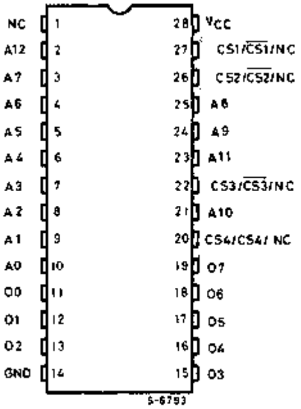
- PIN COMPATIBLE WITH M2764
- ACCESS TIME 250 ns (MAX)
- COMPLETELY STATIC OPERATION
- SINGLE +5V ± 10% POWER SUPPLY
- 8192 × 8 BIT ORGANISATION
- INPUTS AND OUTPUTS TTL COMPATIBLE
- PROGRAMMABLE CHIP SELECT
- THREE-STATE OUTPUTS FOR DIRECT BUS INTERFACE
- EPROMs ACCEPTED AS PROGRAM DATA INPUTS



B
DIP-28
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS


NC 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
28 Vcc
27 CS1/$\overline{CS1}$/NC
26 CS2/$\overline{CS2}$/NC
25 A8
24 A9
23 A11
22 CS3/$\overline{CS3}$/NC
21 A10
20 CS4/CS4/ NC
19 O7
18 O6
17 O5
16 O4
15 O3
S-6793

DESCRIPTION

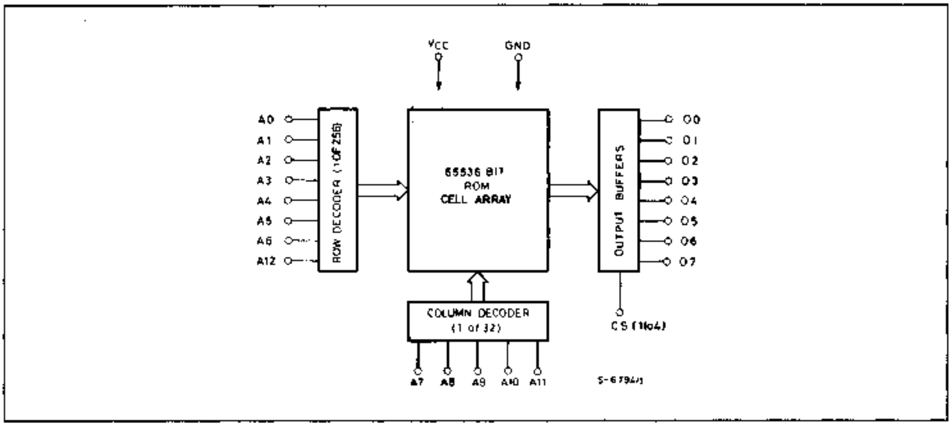
The M2365 is a 65,536-bit static Read Only Memory organized as 8,192 by 8 bits. It is manufactured using our high density N-channel Si-gate MOS process and is ideal for non-volatile data storage applications where high performance, large bit storage and simple interfacing are important design considerations.

The M2365 available in 28-lead dual in-line plastic or ceramic package.

PIN NAMES

A0-A12	ADDRESS INPUT
CS1-CS4	CHIP SELECT INPUTS
NC	NO CONNECTION
O0-O7	DATA OUTPUT
V_{CC}	POWER SUPPLY
GND	GROUND

BLOCK DIAGRAM

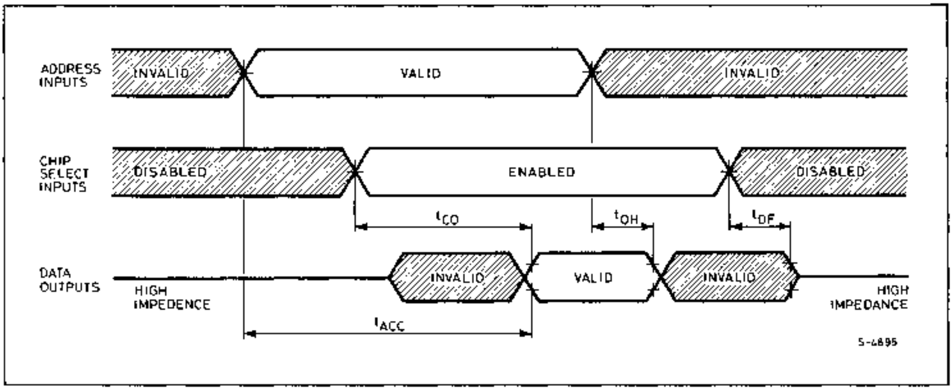

VCC
GND
A0
A1
A2
A3
A4
A5
A6
A12
ROW DECODER (1 OF 256)
65536 BIT
ROM
CELL ARRAY
OUTPUT BUFFERS
O0
O1
O2
O3
O4
O5
O6
O7
COLUMN DECODER
(1 of 32)
A7
A8
A9
A10
A11
CS (1to4)
S-6794/1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltages on any pin with respect to ground	– 0.5 to + 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: ceramic package plastic package	– 65 to + 150 – 55 to + 125	°C °C
T_{op}	Operating temperature	0 to + 70	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

WAVEFORMS


ADDRESS INPUTS
INVALID
VALID
INVALID
CHIP SELECT INPUTS
DISABLED
ENABLED
DISABLED
t_{CO}
t_{OH}
t_{DF}
DATA OUTPUTS
HIGH IMPEDENCE
INVALID
VALID
INVALID
HIGH IMPEDANCE
t_{ACC}
S-4895

DC AND OPERATING CHARACTERISTICS ($T_{amb} = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Load Current	$V_{CC} = 5.5V$, $0V \leqslant V_{IN} \leqslant 5.5V$			10	µA
I_{LO}	Output Leakage Current	Chip deselected $V_{OUT} = 0V$ to V_{CC}			10	µA
I_{CC}	Power Supply Current	Output unloaded, Chip enabled $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$			70	mA
V_{IL}	Input Low Voltage	See Note 1	−0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage	$V_{CC} = 4.5V$ $I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 4.5V$ $I_{OH} = -400$ µA	2.4		V_{CC}	V

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	M2365			Unit
			Min	Typ.	Max	
t_{ACC}	Address Access Time	Output load: 1 TTL load and 100 pf			250	ns
t_{CO}	Chip Select Delay				100	ns
t_{DF}	Chip Deselect Delay	Input transition time: 20 ns			100	ns
t_{OH}	Previous Data Valid After Address Change Delay	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V	10			ns

CAPACITANCE ($T_{amb} = 25°C$, f = 1 MHz, see Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	All pins except pin under test tied to AC ground			7	pF
C_{OUT}	Output Capacitance				10	pF

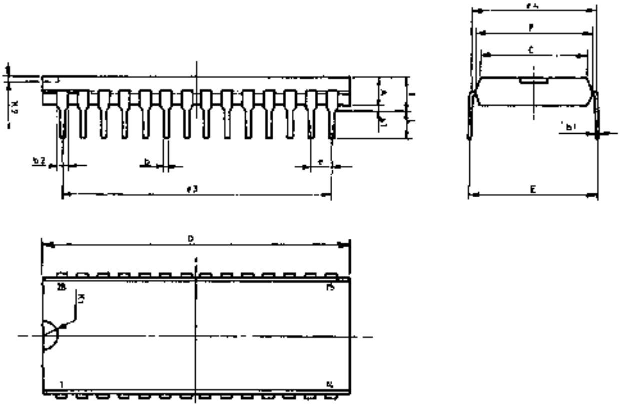
Note 2: This parameter is sampled periodically and is not 100% tested.

ORDERING INFORMATION

Part Number	Access Time	Supply Voltage	Temp. Range	Package
M2365B1	250ns	5V ± 10%	0° to +70°C	DIP-28

PACKAGE MECHANICAL DATA

28-PIN PLASTIC DIP



PO43-D/3

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a 1		0.63			0.025	
B		0.45			0.018	
b 1	0.23		0.31	0.009		0.012
b 2		1.27			0.050	
C						
D			37.34			1.470
E	15.20		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
e4						
F			14.10			0.555
I		4.45			0.175	
L		3.30			0.130	
K1						
K2						

STATIC RAM DEVICES

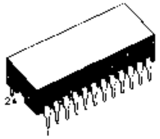
ZEROPOWER

SGS-THOMSON
MICROELECTRONICS

MK48Z02/12(B) -12/15/20/25

2K × 8 ZEROPOWER™ RAM

- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- FULL CMOS-440 mW ACTIVE; 5.5 mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC PINOUTS
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48Z02 4.75V $\geq V_{PFD} \geq$ 4.50V
  MK48Z12 4.50V $\geq V_{PFD} \geq$ 4.20V



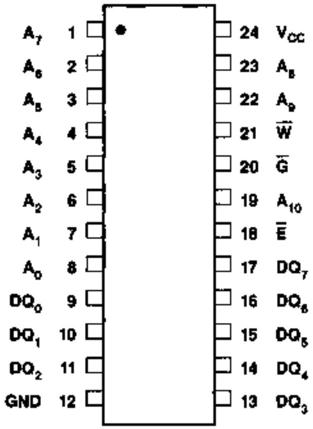
B
DIP-24
(Plastic with Battery Top Hat)

Part Number	Access Time	R/W Cycle Time
MK48ZX2-12	120 ns	120 ns
MK48ZX2-15	150 ns	150 ns
MK48ZX2-20	200 ns	200 ns
MK48ZX2-25	250 ns	250 ns

TRUTH TABLE (MK48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$< V_{CC}$ (Max) $> V_{CC}$ (Min)	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$< V_{PFD}$ (Min) $> V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

FIGURE 1. PIN CONNECTIONS



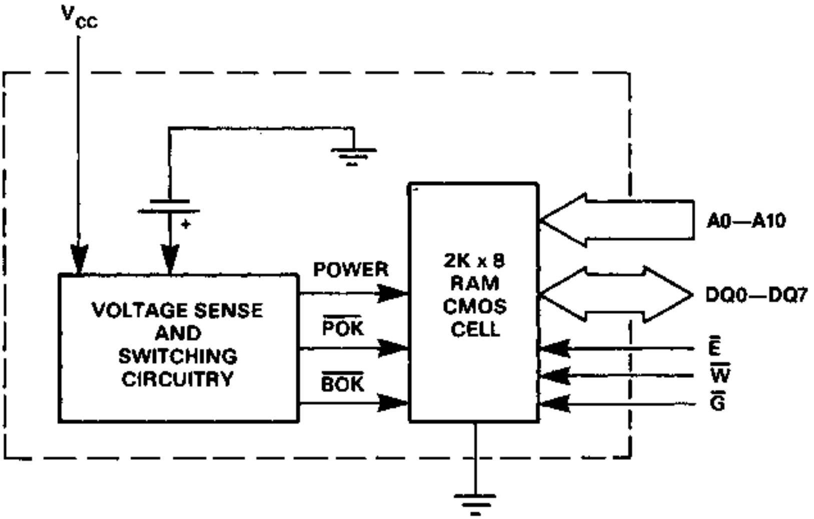
PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7	Data In/Data Out		

DESCRIPTION

The MK48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

FIGURE 2. BLOCK DIAGRAM



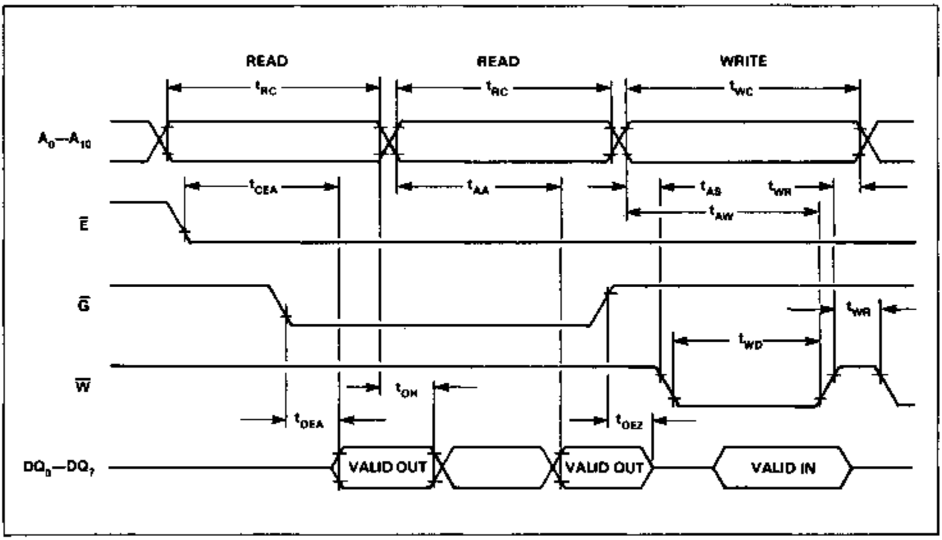
OPERATION

Read Mode

The MK48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 8.

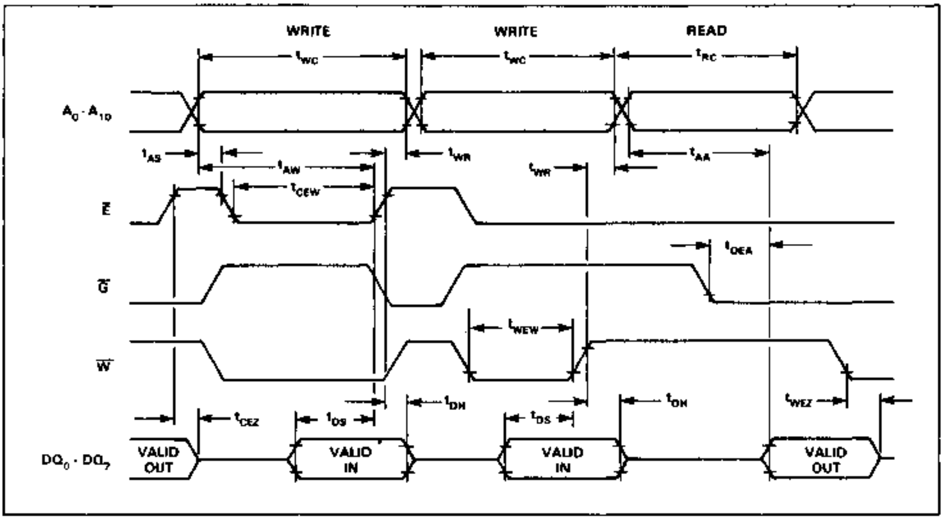
WRITE MODE

The MK48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

($0°C \leq T_A \leq 70°C$) (V_{CC} (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

		MK48ZX2-12		MK48ZX2-15		MK48ZX2-20		MK48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48Z02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48Z02 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48Z12 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS

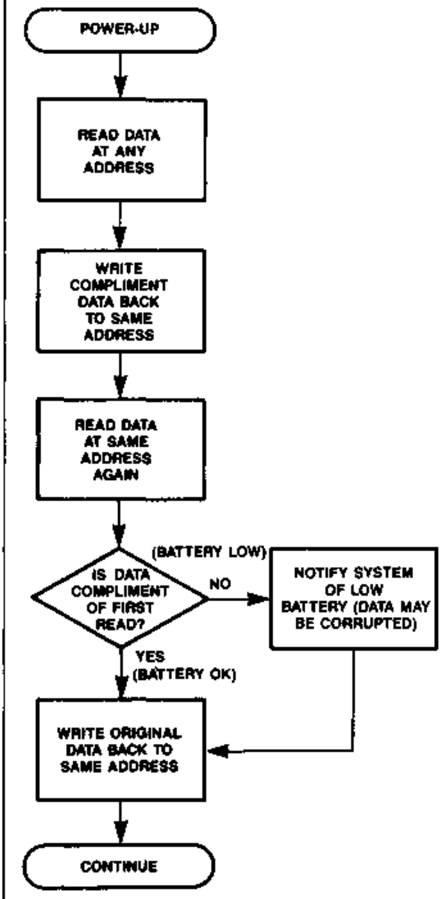
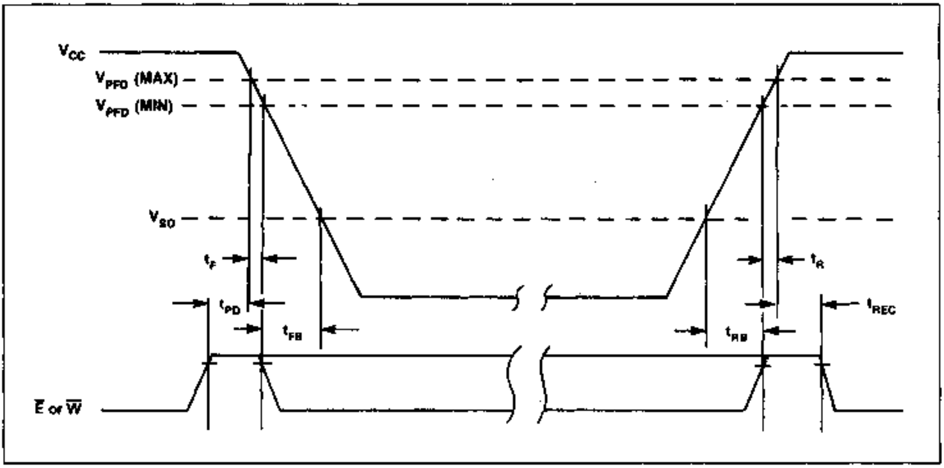

POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES
(BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE

FIGURE 6. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

($0°C \le T_A \le +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

($0°C \le T_A \le +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MK48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

> A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 7 indicates that a particular MK48Z02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MK48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MK48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. if the MK48Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z02/12 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

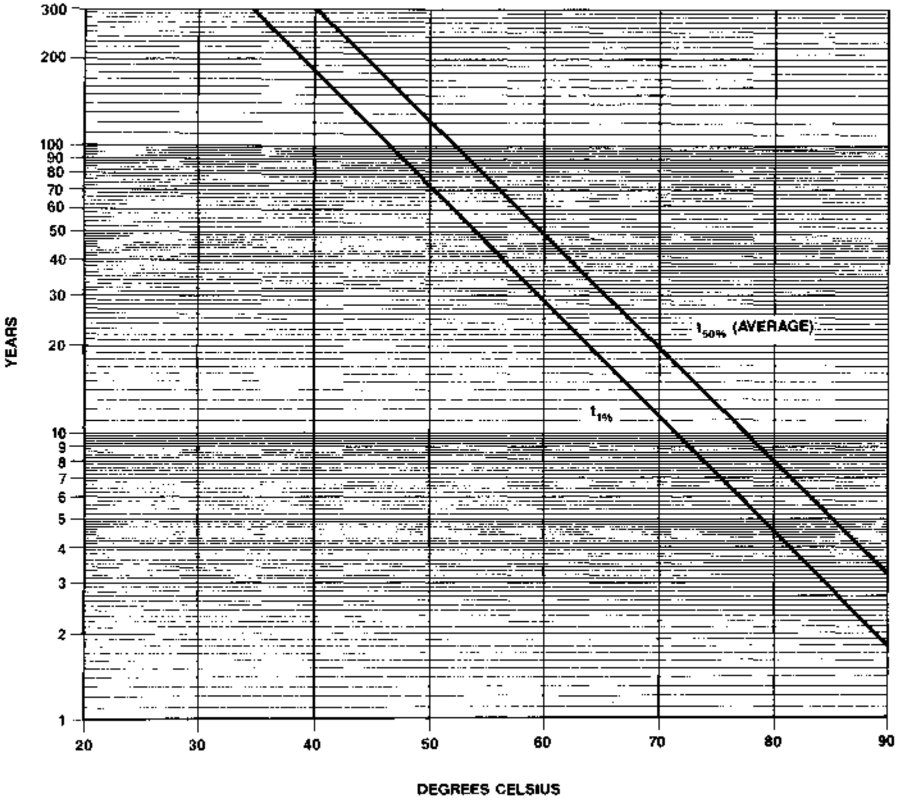
Reading predicted typical life values from Figure 7; BL_1 = 456 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 = 5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/456]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 116.5 \text{ yrs.}$$

FIGURE 7. MK48Z02/12 PREDICTED BATTERY STORAGE LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND . . . . −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature . . . . −40°C to +85°C
Total Device Power Dissipation . . . . 1 Watt
Output Current Per Pin . . . . 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated n the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since t will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, .e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} (max) ≥ V_{CC} ≥ V_{CC} (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{OL}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

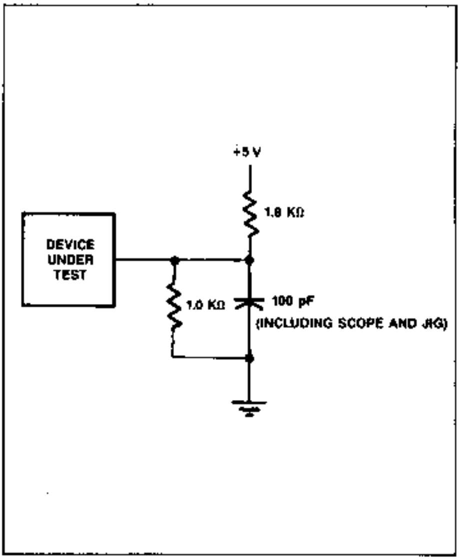
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48Z02)	4.75 V to 5.5 V
V_{CC} (MK48Z12)	4.5 V to 5.5 V

FIGURE 8. OUTPUT LOAD DIAGRAM


+5 V
1.8 KΩ
DEVICE UNDER TEST
1.0 KΩ
100 pF
(INCLUDING SCOPE AND JIG)

ORDERING INFORMATION

MK48Z	X	2	B	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

SPEED:

-12	120 NS ACCESS TIME
-15	150 NS ACCESS TIME
-20	200 NS ACCESS TIME
-25	250 NS ACCESS TIME

PACKAGE:

B	PLASTIC WITH BATTERY TOP HAT

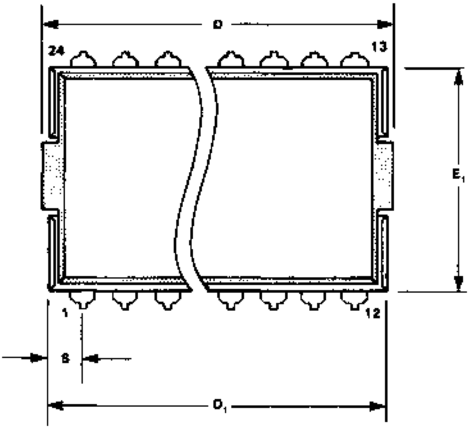
V_{CC} RANGE:

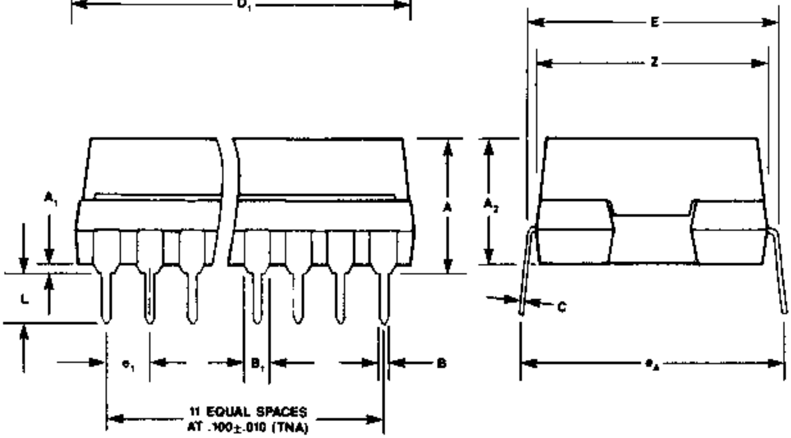
0	+10%/−5%
1	+10%/−10%

PACKAGE DESCRIPTION

B PACKAGE 24 PIN

	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
24 PIN PLASTIC D.I.P. ONLY	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D_1	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	





NOTES:

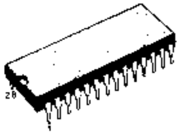
1. Overall length includes .010 in. flash on either end of the package.
2. Package standoff to be measured per JEDEC requirements.
3. Measured from centerline to centerline at lead tips.
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

SGS-THOMSON
MICROELECTRONICS

MK48C02A/12A(K,N) -15/20/25

2K × 8 ZEROPOWER™ RAM

- LOW CURRENT (1 μA @ 70°C) BATTERY INPUT FOR DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER 440 mW ACTIVE; 5.5 mW STANDBY
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- LOW-BATTERY WARNING
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48C02A 4.75V $\geq V_{PFD} \geq$ 4.50V
  MK48C12A 4.50V $\geq V_{PFD} \geq$ 4.20V
- POWER FAIL INTERRUPT OUTPUT

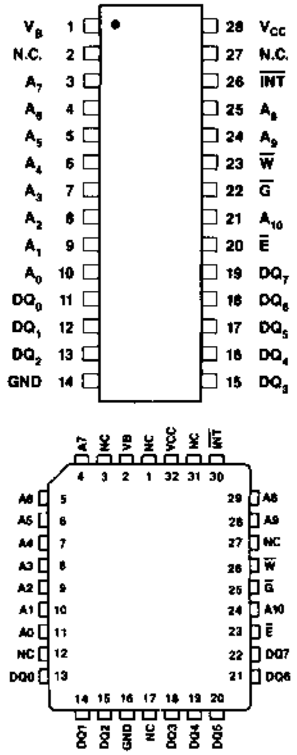


N
DIP-28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

Part Number	Access Time	R/W Cycle Time
MK48CX2A-15	150 ns	150 ns
MK48CX2A-20	200 ns	200 ns
MK48CX2A-25	250 ns	250 ns

FIGURE 1. PIN CONNECTIONS


V_B 1
N.C. 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
DQ_0 11
DQ_1 12
DQ_2 13
GND 14
28 V_{CC}
27 N.C.
26 $\overline{INT}$
25 A_8
24 A_9
23 $\overline{W}$
22 $\overline{G}$
21 A_{10}
20 $\overline{E}$
19 DQ_7
18 DQ_6
17 DQ_5
16 DQ_4
15 DQ_3
A7 4
NC 3
VB 2
NC 1
VCC 32
NC 31
$\overline{INT}$ 30
A6 5
A5 6
A4 7
A3 8
A2 9
A1 10
A0 11
NC 12
DQ0 13
29 A8
28 A9
27 NC
26 $\overline{W}$
25 $\overline{G}$
24 A10
23 $\overline{E}$
22 DQ7
21 DQ6
14 DQ1
15 DQ2
16 GND
17 NC
18 DQ3
19 DQ4
20 DQ5

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0-DQ_7	Data In/Data Out	V_B	Battery Input
$\overline{INT}$	Power Fail Interrupt (Open Drain Type)		
NC	No Connection		

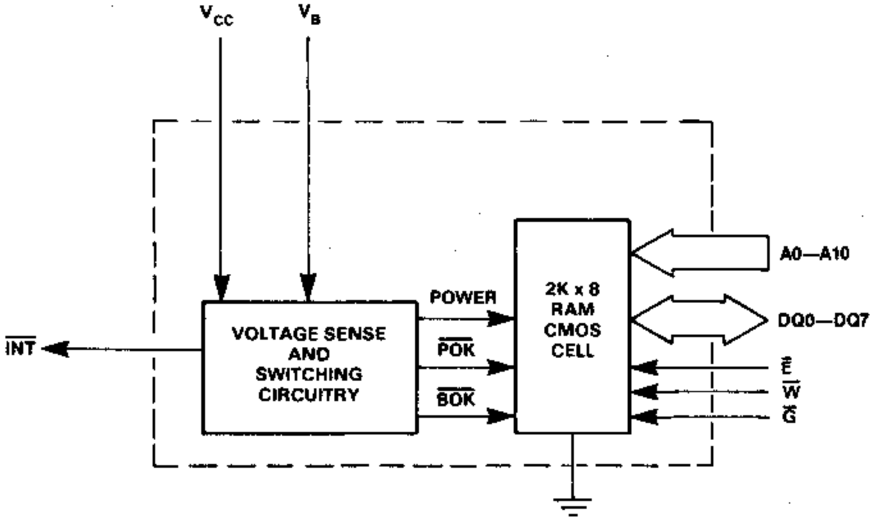
TRUTH TABLE (MK48C02A/12A)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$< V_{CC}$ (Max) $> V_{CC}$ (Min)	V_{IH}	X	X	Deselect	High-Z
	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$< V_{PFD}$ (Min) $> V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

DESCRIPTION

The MK48C02A/12A is a CMOS RAM with internal power fail support circuitry for battery backup applications. The fully static RAM uses an HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. A precision voltage detector write-protects the RAM to prevent inadvertent loss of data when V_{CC} falls out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75V (MK48C02A) and 4.5V (MK48C12A). Data protection is provided for V_{CC} below 4.5V (MK48C02A) and 4.2V (MK48C12A), and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5na) because all power-consuming circuitry is turned off. The low battery drain allows use of a long life Lithium primary cell.

FIGURE 2. BLOCK DIAGRAM


V_{CC}
V_B
VOLTAGE SENSE AND SWITCHING CIRCUITRY
$\overline{INT}$
POWER
$\overline{POK}$
$\overline{BOK}$
2K x 8 RAM CMOS CELL
A0—A10
DQ0—DQ7
$\overline{E}$
$\overline{W}$
$\overline{G}$

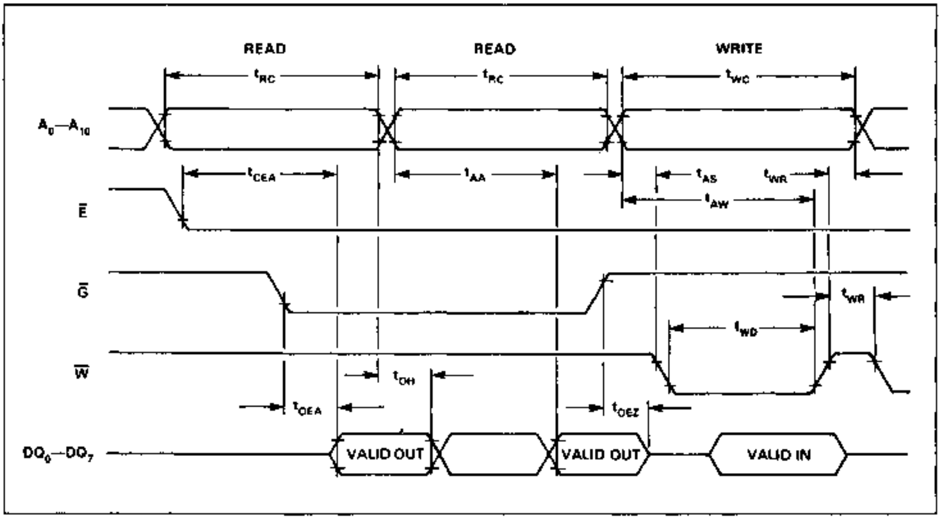
OPERATION

Read Mode

The MK48C02A/12A is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

($0°C \le T_A \le 70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 7.

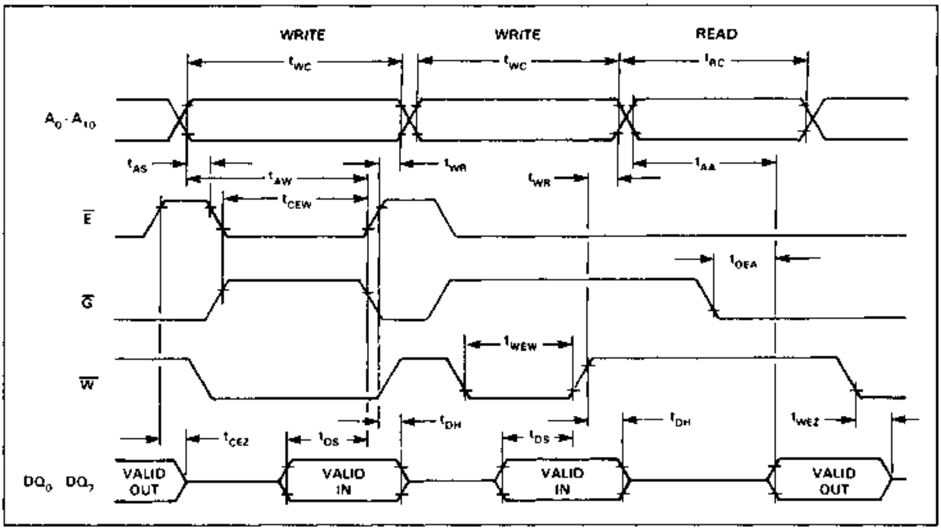
WRITE MODE

The MK48C02A/12A is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high, for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48C02A/12A $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)
(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

		MK48CX2A-15		MK48CX2A-20		MK48CX2A-25			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MK48C02A/12A operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48C02A has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48C12A has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48C02A/12A may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

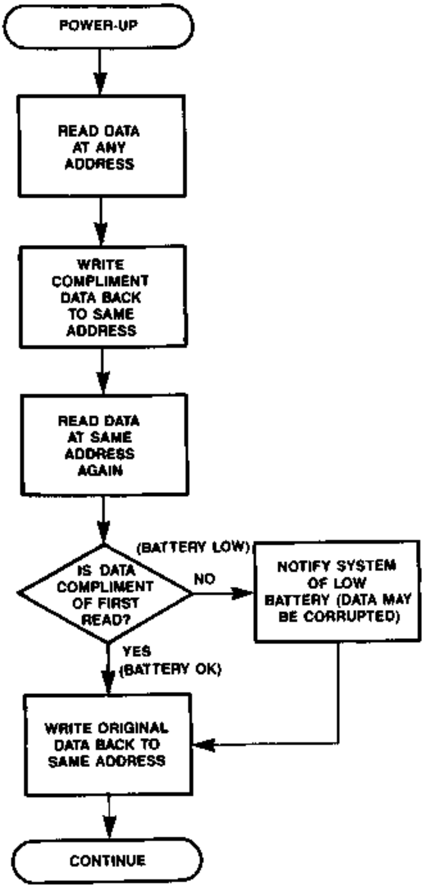
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{BOK}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48C02A/12A provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shut down of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10 µs to 40 µs advanced warning of an impending power-fail write protect.

FIGURE 5. CHECKING THE $\overline{BOK}$ FLAG STATUS


POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES
(BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		μs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after V_{PFD} (max)	120		μs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	μs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	μs	4
t_{FB}	V_{PFD} (Min) to V_{SO}	10		μs	

DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
($0°C \leq T_A \leq +70°C$)

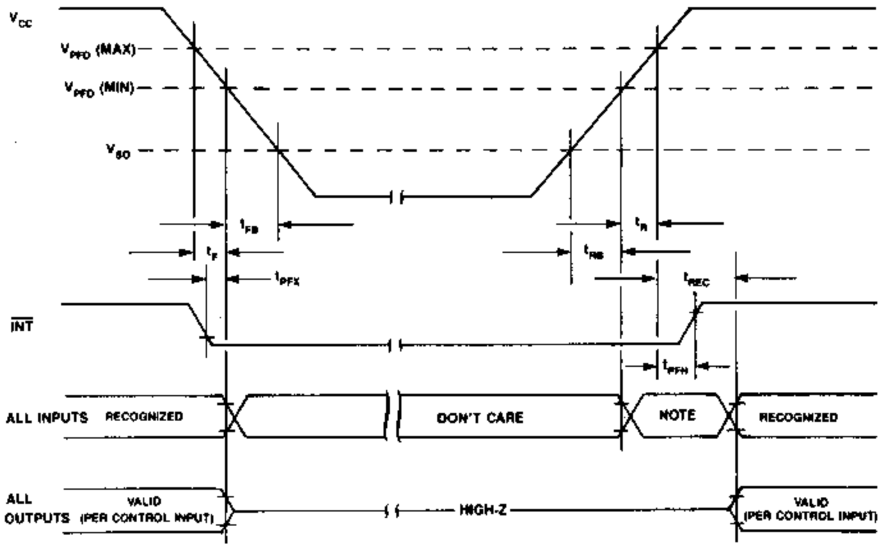
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48C02A)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48C12A)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40 μs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 μs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. INT may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION
Negative Undershoots Below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

FIGURE 6. POWER DOWN/POWER-UP TIMING


V_{CC}
V_{PFD} (MAX)
V_{PFD} (MIN)
V_{SO}
t_{FB}
t_F
t_{PFX}
t_R
t_{RB}
t_{REC}
$\overline{INT}$
t_{PFH}
ALL INPUTS
RECOGNIZED
DON'T CARE
NOTE
RECOGNIZED
ALL OUTPUTS
VALID (PER CONTROL INPUT)
HIGH-Z
VALID (PER CONTROL INPUT)

NOTE:

Inputs may or may not be recognized at this time.
Caution should be taken to keep $\overline{E}$ or $\overline{W}$ in the high state V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND . . . . −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature . . . . −55°C to +125°C
Total Device Power Dissipation . . . . 1 Watt
Output Current Per Pin . . . . 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48C02A)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48C12A)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2
V_B	Battery Voltage	1.8	4.0	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} (max) $\geq V_{CC} \geq V_{CC}$ (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC} - 0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	4
I_{OL}	Output Leakage Current	−5	+5	μA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	
V_{PFL}	INT Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	
I_{BATT}	Battery Backup Current V_B = 4.0 V		1	μA	
I_{CHG}	Battery Charging Current V_{CC} = 5.5 V	−5	+5	nA	
V_{LB}	Battery OK Flag	1.8	2.6	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins and $\overline{INT}$	10 pF	4,5

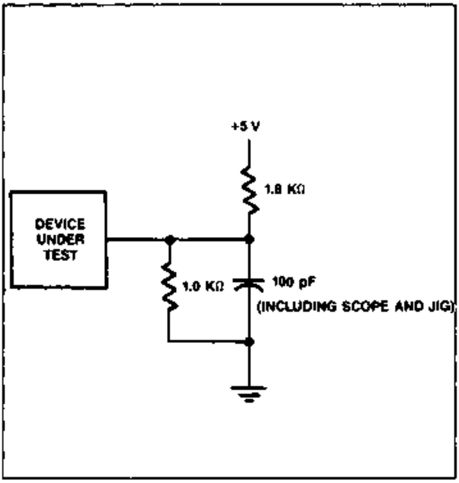
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $GND \leq V_I \leq V_{CC}$ and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} (MK48C02A)	4.75 V to 5.5 V
V_{CC} (MK48C12A)	4.5 V to 5.5 V

FIGURE 7. OUTPUT LOAD DIAGRAM


+5 V
1.8 KΩ
DEVICE UNDER TEST
1.0 KΩ
100 pF
(INCLUDING SCOPE AND JIG)

ORDERING INFORMATION

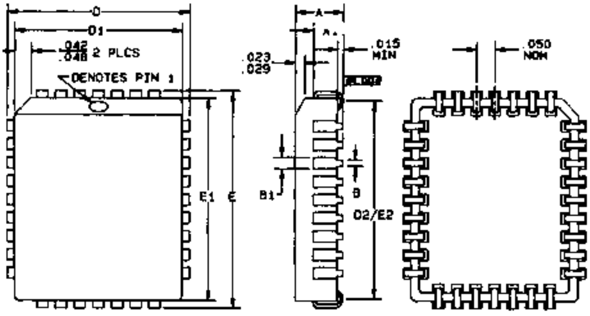
MK48C	X	2A	X	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

-15	150 NS ACCESS TIME
-20	200 NS ACCESS TIME
-25	250 NS ACCESS TIME

K	32 PIN PLCC
N	28 PIN DIP

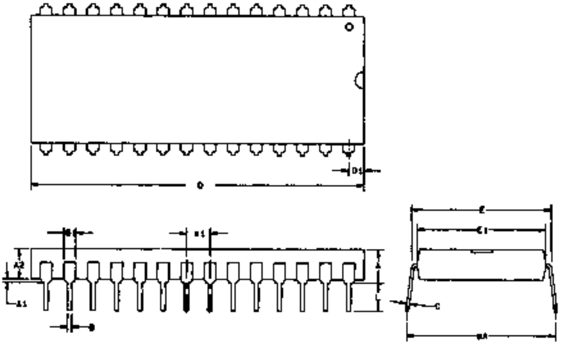
0	+10%/−5%
1	+10%/−10%

FIGURE 8. MK48C02A/12A PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14 046	.547	.553
E2	12.446	13.462	.490	.530

FIGURE 9. MK48C02A/12A PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	–	5.334	–	.210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2 286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	–	120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

MK48T02/12(B)
-12/15/20/25

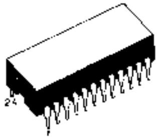
2K × 8 ZEROPOWER™/TIMEKEEPER™ RAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRYSTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES AND SECONDS
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 2K × 8 SRAMS
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48T02 $4.75V \geq V_{PFD} \geq 4.50V$
  MK48T12 $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MK48TX2-12	120 ns	120 ns
MK48TX2-15	150 ns	150 ns
MK48TX2-20	200 ns	200 ns
MK48TX2-25	250 ns	250 ns

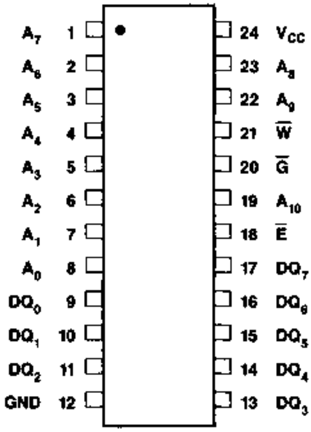
TRUTH TABLE (MK48T02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$< V_{CC}$ (Max) $> V_{CC}$ (Min)	V_{IH}	X	X	Deselect	High-Z
	V_{IL}	X	V_{IL}	Write	D_{IN}
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z
$< V_{PFD}$ (Min) $> V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z



B
DIP-24
(Plastic with Battery Top Alt)

FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	+5 V
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

June 1988

DESCRIPTION

The MK48T02/12 combines a 2K × 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon mono-fluoride battery, all in a single plastic DIP package. The MK48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K × 8 SRAM, such as the 6116 or 5517. It also easily fits into many EPROM AND EEPROM sockets, providing the non-volatility of the PROMs without any requirement for special write timing, or limitations on the number of writes that can be performed.

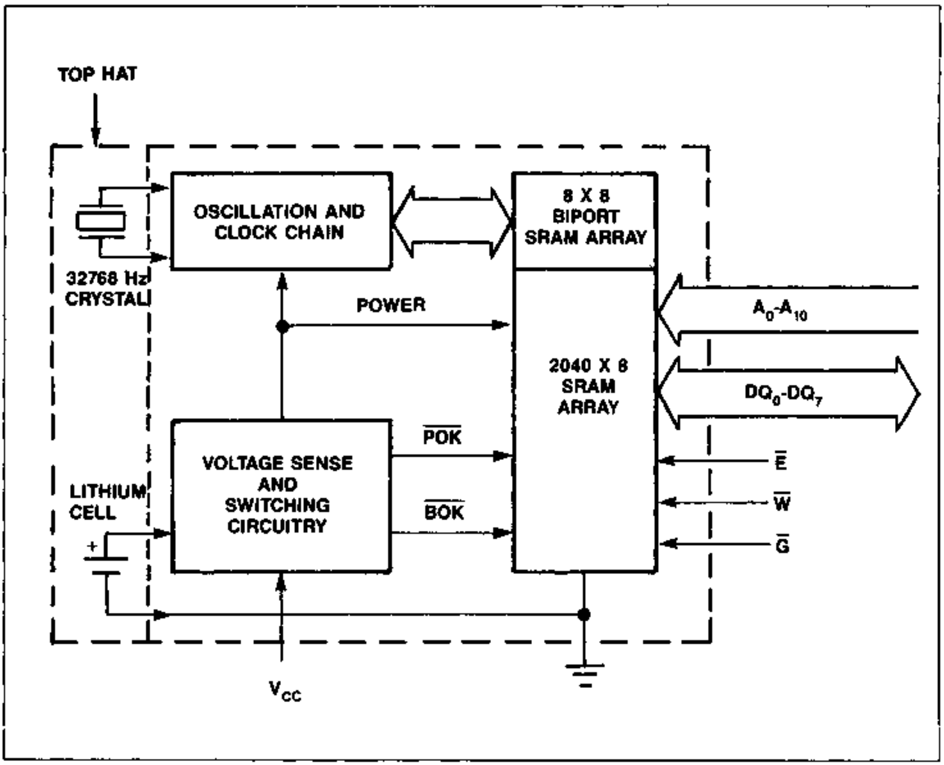
Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the Clock are combined on the same die. As Figure 2 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 Hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T02/12 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed.

The MK48T02/12 also has its own Power-fail Detect circuit. The circuit deselects the device whenever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

BiPORT, BYTEWIDE, TIMEKEEPER and ZEROPOWER are trademarks of SGS-THOMSON Microelectronics, Inc..

FIGURE 2. BLOCK DIAGRAM


TOP HAT
OSCILLATION AND CLOCK CHAIN
8 X 8 BIPORT SRAM ARRAY
32768 Hz CRYSTAL
POWER
A_0-A_{10}
2040 X 8 SRAM ARRAY
DQ_0-DQ_7
$\overline{POK}$
VOLTAGE SENSE AND SWITCHING CIRCUITRY
LITHIUM CELL
$\overline{BOK}$
$\overline{E}$
$\overline{W}$
$\overline{G}$
V_{CC}

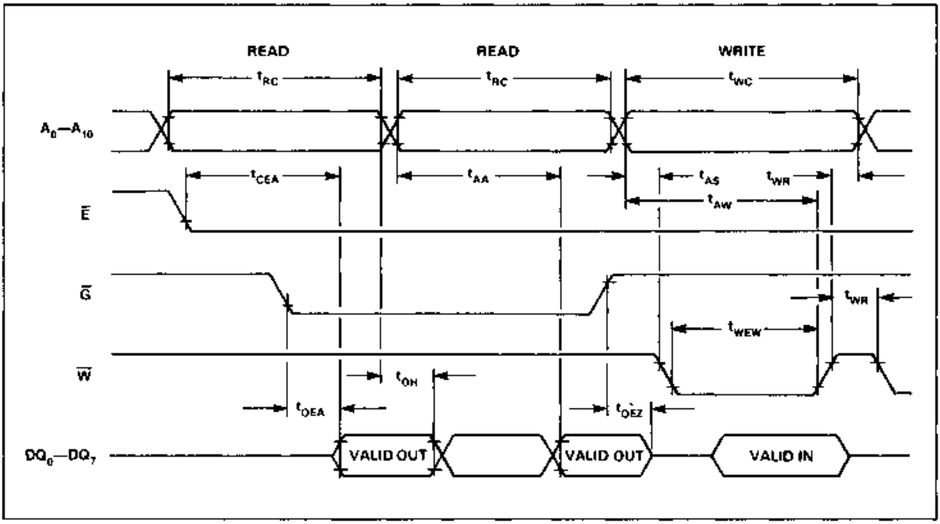
OPERATION

READ MODE

The MK48T02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access (changing Addresses without removing Chip Enable) to any of the 2048 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminant until the next t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)
($0°C \leq T_A \leq 70°C$) (V_{CC} (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

		MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		120		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		30		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		30		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 13.

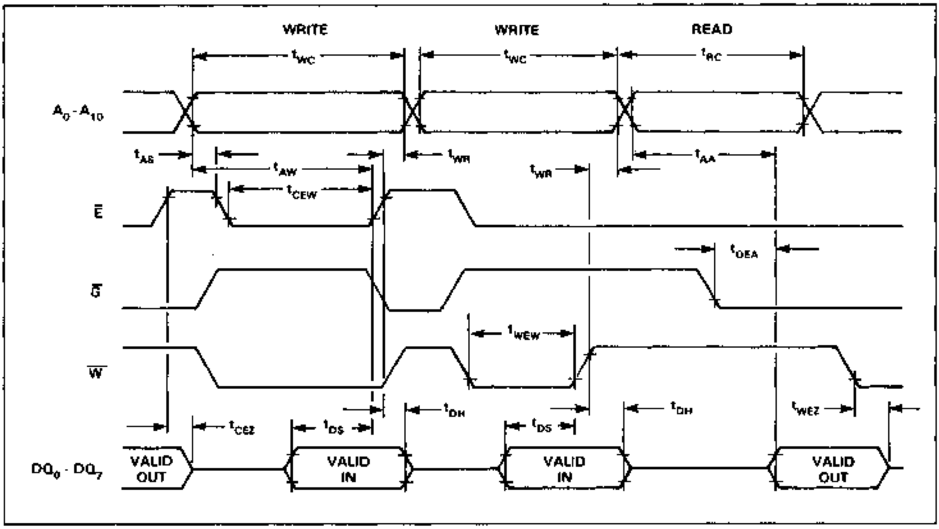
WRITE MODE

The MK48T02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MK48T02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

(0°C ≤ T_A ≤ 70°C) (V_{CC} (Max) ≥ V_{CC} ≥ V_{CC} (Min))

SYM	PARAMETER	MK48TX2-12		MK48TX2-15		MK48TX2-20		MK48TX2-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	
t_{AW}	Address Valid to End of Write	90		120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	75		90		120		160		ns	
t_{WEW}	Write Enable to End of Write	75		90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		10		ns	
t_{DS}	Data Setup Time	35		40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		40		50		60		80	ns	

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be Halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control register. As long as a "1" remains in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued. All of the TIMEKEEPER registers are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset to a "0".

Setting the Clock

The eighth bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values the actual TIMEKEEPER counters and allows normal operation to resume. The KS bit, FT bit and the bits marked with zeroes in Figure 5 must be written with zeroes to allow normal TIMEKEEPER and RAM operation.

FIGURE 5. THE MK48T02/12 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
7FF	—	—	—	—	—	—	—	—	YEAR	00-99
7FE	0	0	0	—	—	—	—	—	MONTH	01-12
7FD	0	0	—	—	—	—	—	—	DATE	01-31
7FC	0	FT	0	0	0	—	—	—	DAY	01-07
7FB	KS	0	—	—	—	—	—	—	HOUR	00-23
7FA	0	—	—	—	—	—	—	—	MINUTES	00-59
7F9	ST	—	—	—	—	—	—	—	SECONDS	00-59
7F8	W	R	S	—	—	—	—	—	CONTROL	

KEY: ST = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT S = SIGN BIT KS = KICK START

Calibrating the Clock

The MK48T02/12 is driven by a quartz crystal controlled oscillator with a nominal frequency of 32768 Hz.The crystal is mounted in the tophat along with the battery. A typical MK48T02/12 is accurate within ±1 minute per month at 25°C without calibration. The devices are tested not to exceed ± 35 ppm (Parts Per Million) oscillator frequency error at 25°C, which comes to about ±1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6 shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T02/12 design, however, employs periodic counter correction. The calibration circuit adds or subtracts count from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control register. Adding count speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits in the Control register. The byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 128 oscillator cycles, that is one tick of the divide by 256 stage. If a binary 1 is loaded into the register, only the first two minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

FIGURE 6. THE MK48T02/12 OSCILLATOR FREQUENCY VS. TEMPERATURE

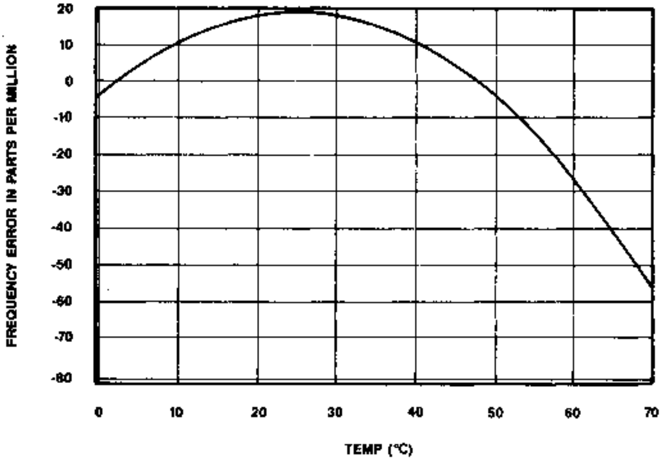
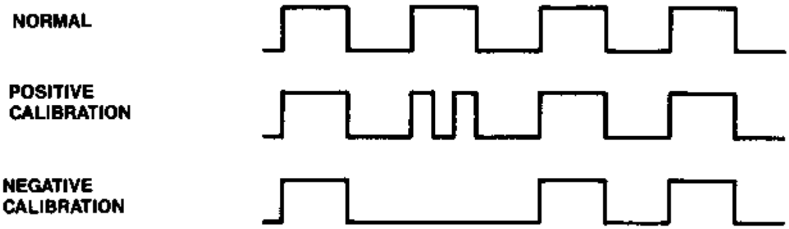


FIGURE 7. ADJUSTING THE DIVIDE BY 256 PULSE TRAIN



Therefore, each calibration step has the effect of adding or subtracting 256 oscillator cycles for every 125,829,120 (32768 x 60 x 64) actual oscillator cycles, that is 2.034 ppm of adjustment per calibration step; giving the user a ± 63.07 ppm calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 5.35 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T02/12 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accesses the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Day register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ_0) of the Seconds register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.00512 Hz would indicate a +10 ppm (1−(512/512.00512)) oscillator frequency error, requiring a -5 (000101_2) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must be stable at Address 7F9 when reading the 512 Hz on DQ_0.

The FT bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds register is monitored by holding the MK48T02/12 in an extended read of the Second register, without having the Read bit set. The FT bit MUST be reset to a "0" for normal clock operations to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB of the Seconds register. Setting it to a "1" stops the oscillator. In order to make the oscillator as stingy with current as possible, the oscillator is designed to require an extra "kick" to begin oscillation again. The extra kick is provided by the Kick Start (KS) bit, the MSB of the Hours register. To start the oscillator, implement the following procedure.

1. Set the Write Bit to "1".
2. Reset the Stop Bit to "0".
3. Set the Kick Start Bit to "1".
4. Reset the Write Bit to "0".
5. Wait 2 seconds.
6. Set the Write Bit to "1".
7. Reset the Kick Start Bit to "0".
8. Set the Correct time and date.
9. Reset the Write Bit to "0".

Note: Leaving the KS bit set will cause the Clock to draw excessive current and will shorten battery life.

DATA RETENTION MODE

With V_{CC} applied, the MK48T02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MK48T02 has a V_{PFD} (max) -V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MK48T12 has a V_{PFD} (max) -V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 8 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{\text{E}}$ or $\overline{\text{W}}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 8. CHECKING THE $\overline{\text{BOK}}$ FLAG STATUS

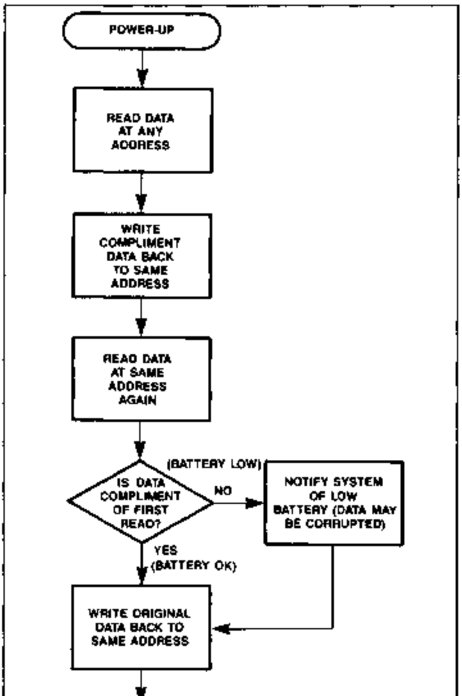
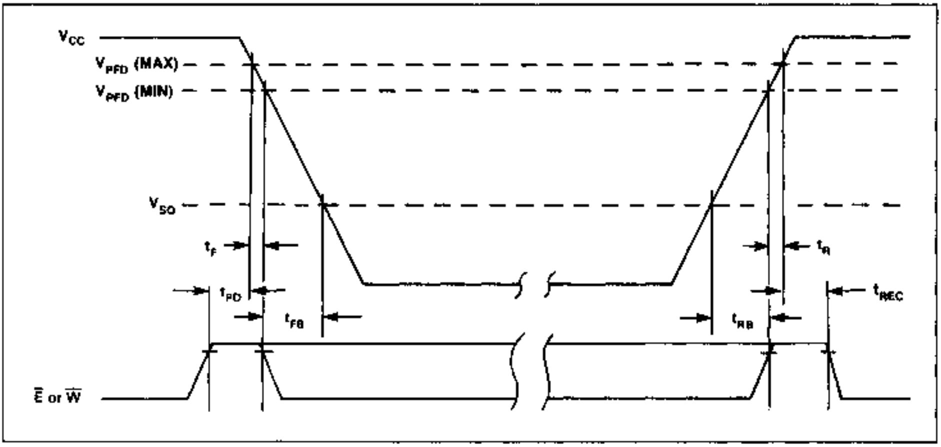

POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES
(BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE

FIGURE 9. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48T02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48T12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data or stop the clock.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data or stop the clock.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T02/12 is expected to ultimately come to an end for one of two reasons; either because it has been discharged while providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T02/12 are so low, they can be neglected in practical Storage Life calculations. Therefore, application of V_{CC} or turning off the oscillator can extend the effective Back-up System life.

Predicting Storage Life

Figure 10 illustrates how temperature affects Storage Life of the MK48T02/12 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T02/12.

Storage Life predictions presented in Figure 10 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

A Special Note: The summary presented in Figure 10 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 10. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 10 indicates that a particular MK48T02/12 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 20 years.

The $t_{1\%}$ figure represents the practical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48T02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8625 = 1986, week 25).

Calculating Predicted Storage Life of the Battery

As Figure 10 indicates, the predicted Storage Life of the battery in the MK48T02/12 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 10. If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = \frac{1}{[(TA_1/TT)/SL_1]+[(TA_2/TT)/SL_2]+\ldots+[(TA_n/TT)/SL_n]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

SL_1, SL_2, SL_n = Predicted Storage Life at Temp 1, Temp 2, etc. (See Figure 10).

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T02/12 is exposed to temperatures of 30°C (86°F) or less for 4672 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

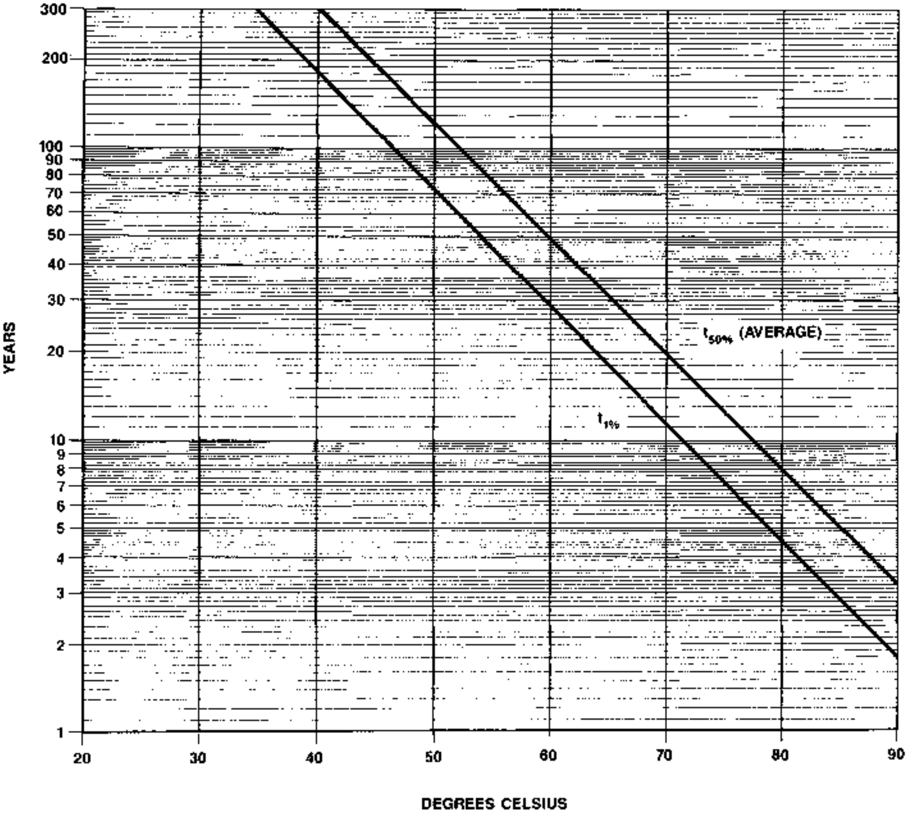
Reading predicted $t_{1\%}$ values from Figure 10; SL_1 = 456 yrs., SL_2 = 175 yrs., SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 =3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage Life} \geq \frac{1}{[(4672/8760)/456]+[(3650/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 126 \text{ yrs.}$$

FIGURE 10. MK48T02/12 PREDICTED BATTERY STORAGE LIFE VS. TEMPERATURE



Predicting Capacity Consumption Life

The MK48T02/12 internal cell has a minimum rated capacity of 35 mAh. The device places a nominal combined RAM and TIMEKEEPER load of 1.2 μA on a typical internal 37 mAh lithium battery when the clock is running and the device is in Battery Back-up mode. At that rate, the MK48T02/12 will consume the cell's capacity in 29,166 hours, or about 3.3 years. But, as Figure 11 shows, Capacity Consumption can be spread over a much longer period of time.

Naturally, Back-up current varies with temperature. As Figure 12 indicates, the rate of Current Consumption by the MK48T02/12 with the clock running in Battery Back-up mode is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variables, only the user can estimate consumption rates in a given design. As long as ambient temperature is held reasonably constant, expected Capacity Consumption life can be estimated by reading 0% V_{CC} Duty Cycle Capacity Consumption life directly from Figure 12, and dividing by the expected V_{CC} Duty Cycle (i.e. at 25°C with a 66% Duty Cycle, Capacity Consumption Life = 3.3/(1-.66) = 9.5 years).

If the MK48T02/12 spends an appreciable amount of time at a variety of temperatures, the same equation provided in the previous Storage Life section should be used to estimate Capacity Consumption life.

Example Consumption Life Calculation

Taking the same cash register/terminal used earlier, let's assume that the high and low temperature periods are the non-operating, Battery Back-up mode periods, and that the register is turned on 10 hours a day seven days per week. The two points of interest on the curves in Figure 12 will be the 25°C and the 70°C points.

Reading Capacity Life values from Figure 12; CL_1 = 3.3 yrs., CL_2 = 3.55 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 438 hrs./yr.

$$\text{Capacity Life} \geq \frac{1}{[(4672/8760)/3.3]+[(438/8760)/3.55]}$$

$$\geq 5.69 \text{ yrs.}$$

Estimating Back-up System Life

The procedure for estimating Back-up System Life is simple. Pick the lower of the two numbers. In the case calculated in the examples, that would be 5.69 years.

The fact is, since either mechanism, Storage Life or Capacity Consumption, can end the system's life, the end is marked by whichever occurs first.

FIGURE 11. TYPICAL CAPACITY CONSUMPTION LIFE AT 25°C VS. V_{CC} DUTY CYCLE

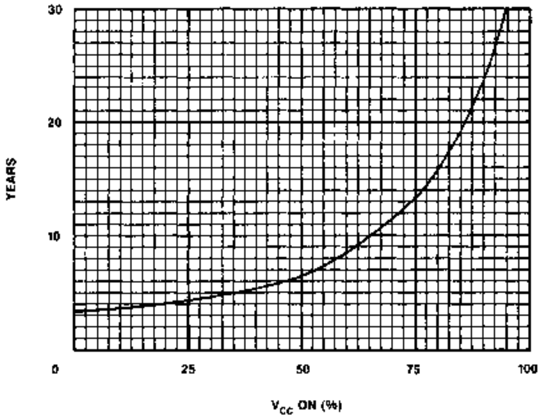
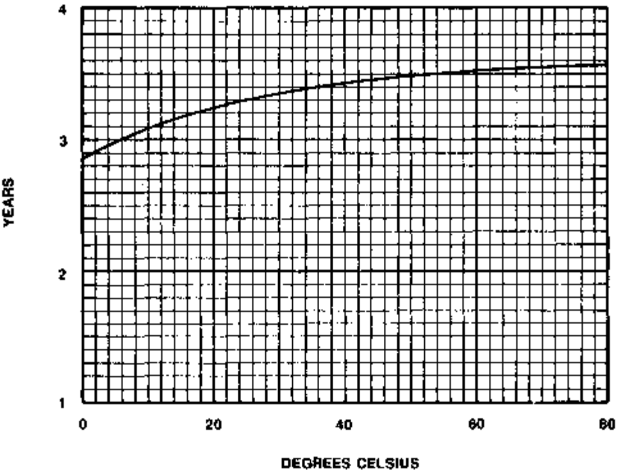


FIGURE 12. CURRENT CONSUMPTION LIFE OVER TEMPERATURE WITH 0% V_{CC} DUTY CYCLE



APPLICATION NOTE:

BINARY TO BCD, AND BCD TO BINARY CONVERSION

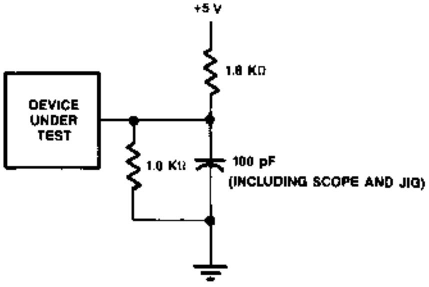
The MK48T02/12 presents and accepts TIMEKEEPER data in BCD format. Conversion to or from other formats can be executed in a single line of code, as the following example BASIC program demonstrates.

```
10 REM  BINARY TO BCD
20 DEF  FNA (X)=INT (X/10)*16+X-INT
        (X/10)*10
30 REM  BCD TO BINARY
40 DEF  FNB (X)=INT (X/16)*10+(XAND15)
```

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V

FIGURE 13. EQUIVALENT OUTPUT LOAD DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND	−0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A)	0°C to +70°C
Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	−20°C to +70°C
Total Device Power Dissipation	1 Watt
Output Current Per Pin	20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48T02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48T12)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le +70°C$) (V_{CC} (Max) $\ge V_{CC} \ge V_{CC}$ (Min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		5	mA	4
I_{CC3}	CMOS Standby Current ($\overline{E} = V_{CC} - 0.2$ V)		3	mA	4
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	5
I_{OL}	Output Leakage Current	−5	+5	μA	5
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0$ mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 2.1$ mA)		0.4	V	

CAPACITANCE ($T_A = 25°C$)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	6
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	6,7

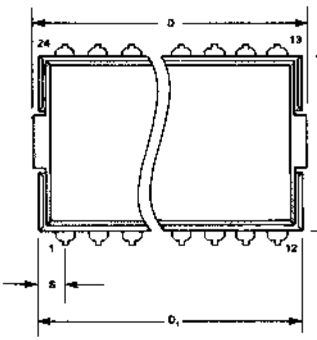
NOTES

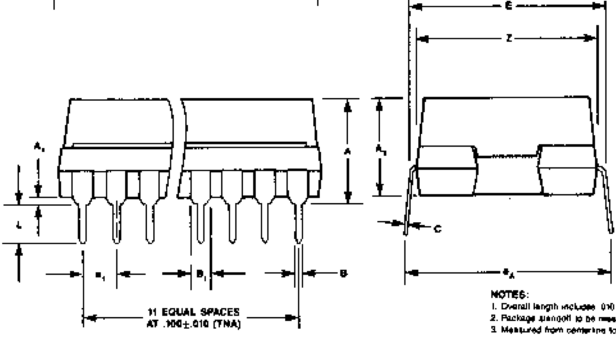
1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with Control Bits set as follows: R = 1; W, ST, KS, FT = 0.
5. Measured with $GND \le V_I \le V_{CC}$ and outputs deselected.
6. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{V\Delta}$ with $\Delta V = 3$ volts and power supply at 5.0 V.
7. Measured with outputs deselected.

PACKAGE DESCRIPTION

B PACKAGE 24 PIN

	Dim.	mm		Inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	–	32.893	–	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
24 PIN PLASTIC D.I.P. ONLY	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D_1	–	32.258	–	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	





NOTES:
1. Overall length includes .010 in. flash on either end of the package
2. Package standoff to be measured per JEDEC requirements
3. Measured from centerline to centerline at lead tips
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

ORDERING INFORMATION

MK48T	X	2	B	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

SPEED:

-12	120 NS ACCESS TIME
-15	150 NS ACCESS TIME
-20	200 NS ACCESS TIME
-25	250 NS ACCESS TIME

PACKAGE:

B	PLASTIC WITH BATTERY TOP HAT

V_{CC} RANGE:

0	+10%/−5%
1	+10%/−10%

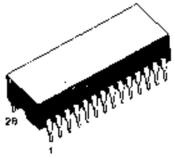
SGS-THOMSON
MICROELECTRONICS

MK48Z08/18/09/19(B) -15/20/25

8K × 8 ZEROPOWER™ RAM

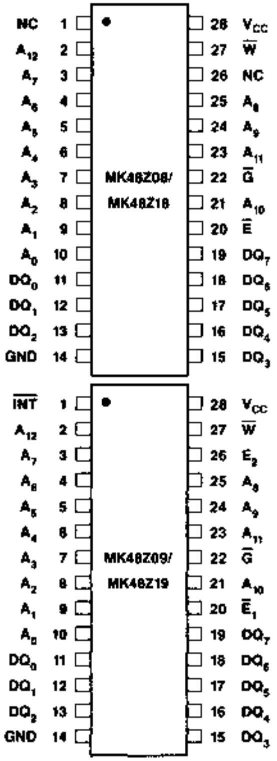
- PREDICTED WORST CASE BATTERY LIFE OF 11 YEARS @ 70°C
- DATA RETENTION IN THE ABSENCE OF POWER
- POWER FAIL INTERRUPT OUTPUT (MK48Z09/19) OPEN DRAIN
- EXTRA DATA SECURITY PROVIDED BY EARLY WRITE PROTECTION DURING POWER FAILURE (MK48Z08/09)
- DIRECT REPLACEMENT FOR VOLATILE 8K x 8 BYTE WIDE STATIC RAM
- +5 VOLT ONLY READ/WRITE
- UNLIMITED WRITE CYCLES
- JEDEC STANDARD 28 PIN MEMORY PINOUT
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MK48Z08/09: $4.75V \geq V_{PFD} \geq 4.50V$
  MK48Z18/19: $4.50V \geq V_{PFD} \geq 4.20V$

Part Number	Access Time	R/W Cycle Time
MK48Z08B-25	250 ns	250 ns
MK48Z08B-20	200 ns	200 ns
MK48Z08B-15	150 ns	150 ns
MK48Z18B-25	250 ns	250 ns
MK48Z18B-20	200 ns	200 ns
MK48Z18B-15	150 ns	150 ns
MK48Z09B-25	250 ns	250 ns
MK48Z09B-20	200 ns	200 ns
MK48Z09B-15	150 ns	150 ns
MK48Z19B-25	250 ns	250 ns
MK48Z19B-20	200 ns	200 ns
MK48Z19B-15	150 ns	150 ns



B
DIP-28
(Plastic with Battery Top Hat)

FIGURE 1. PIN CONNECTIONS


NC 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
DQ_0 11
DQ_1 12
DQ_2 13
GND 14
28 V_{CC}
27 $\overline{W}$
26 NC
25 A_8
24 A_9
23 A_{11}
22 $\overline{G}$
21 A_{10}
20 $\overline{E}$
19 DQ_7
18 DQ_6
17 DQ_5
16 DQ_4
15 DQ_3
MK48Z08/
MK48Z18
$\overline{INT}$ 1
A_{12} 2
A_7 3
A_6 4
A_5 5
A_4 6
A_3 7
A_2 8
A_1 9
A_0 10
DQ_0 11
DQ_1 12
DQ_2 13
GND 14
28 V_{CC}
27 $\overline{W}$
26 E_2
25 A_8
24 A_9
23 A_{11}
22 $\overline{G}$
21 A_{10}
20 $\overline{E}_1$
19 DQ_7
18 DQ_6
17 DQ_5
16 DQ_4
15 DQ_3
MK48Z09/
MK48Z19

PIN NAMES

A_0 - A_{12}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E_1}$, E_2	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0 - DQ_7	Data In/ Data Out	$\overline{INT}$	Power Fail Interrupt Output
NC	No Connect		

DESCRIPTION

The MK48Z08/MK48Z18/MK48Z09/MK48Z19 is a 65,536-bit, Non-Volatile Static RAM, organized 8K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 8K x 8 static RAM, directly conforming to the popular Byte Wide 28-pin DIP package (JEDEC). MK48Z08/18/09/19 also matches the pinning of 2764 EPROM and 8K x 8 EEPROMs. Like other static RAM, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

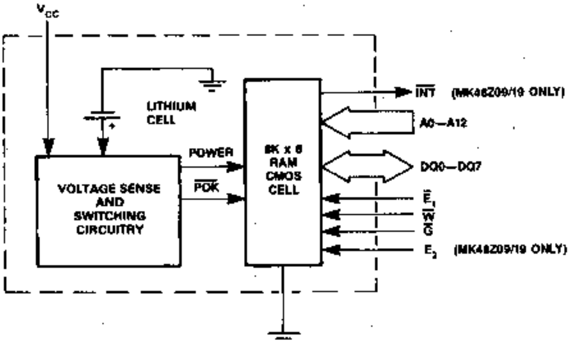
TRUTH TABLE MK48Z08/18

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max) $>V_{CC}$ (min)	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	Deselect	High Z	CMOS Standby
$\leq V_{SO}$	X	X	X	Deselect	High Z	Battery Back-up Mode

TRUTH TABLE MK48Z09/19

V_{CC}	$\overline{E_1}$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max) $>V_{CC}$ (min)	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	X	Deselect	High Z	CMOS Standby
$\leq V_{SO}$	X	X	X	X	Deselect	High Z	Battery Back-up Mode

FIGURE 2. BLOCK DIAGRAM



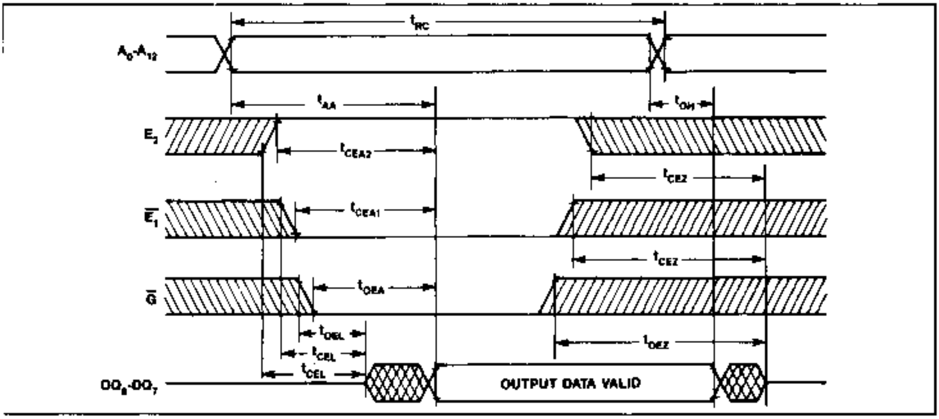
OPERATION

Read Mode

The MK48Z08/18/09/19 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high, $\overline{E_1}$ (Chip Enable) is low, and E_2 is high (MK48Z09/19), providing a ripple-through access of data from eight of 65,536 locations in the static storage array. Thus, the unique address specified by the 13 Address Inputs (A_n) defines which one of 8,192 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the Chip Enable and $\overline{G}$ access times are satisfied. If Chip Enable or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{OEA} or t_{CEA1} or t_{CEA2}), rather than the address. The state of the eight Data I/O signals is controlled by the Chip Enable and $\overline{G}$ control signals. The data linesmay be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ CYCLE



READ CYCLE
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} (min) $\leq V_{CC} \leq V_{CC}$ (max))

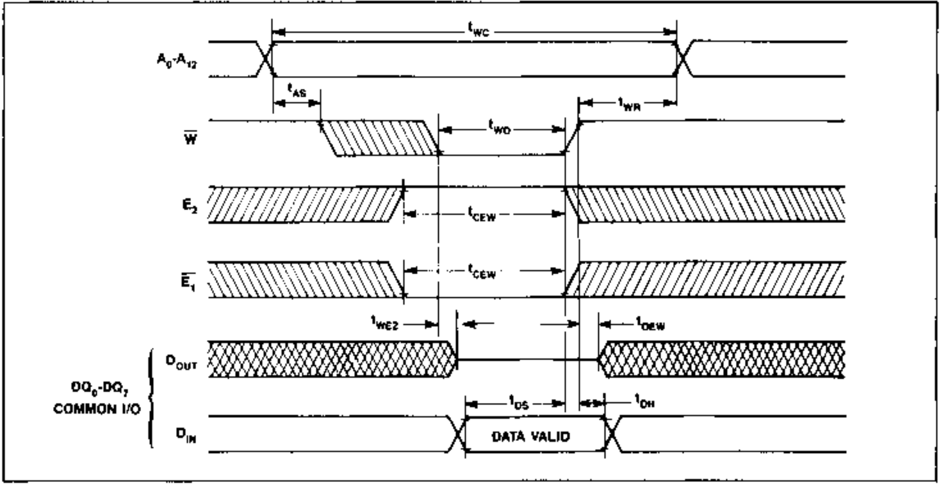
		MK48ZXX-15		MK48ZXX-20		MK48ZXX-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150	—	200	—	250	—	ns	
t_{AA}	Address Access Time	—	150	—	200	—	250	ns	
t_{CEA1}	$\overline{E_1}$ Access Time	—	150	—	200	—	250	ns	
t_{CEA2}	E_2 Access Time	—	150	—	200	—	250	ns	
t_{OEA}	Output Enable to Output Valid	—	75	—	100	—	125	ns	
t_{CEL}	Chip Enable ($\overline{E_1}$, E_2) to Output In Low-Z	10	—	10	—	15	—	ns	
t_{OEL}	Output Enable to Output Low-Z	5	—	5	—	10	—	ns	
t_{CEZ}	Chip Enable ($\overline{E_1}$, E_2) Output In High-Z	—	75	—	100	—	125	ns	
t_{OEZ}	Output Enable to Output High-Z	—	60	—	80	—	100	ns	
t_{OH}	Output Data Hold Time	20	—	20	—	25	—	ns	

Write Mode

The MK48Z08/18/09/19 is in the Write Mode whenever the $\overline{W}$ and $\overline{E_1}$ are low and E_2 (MK48Z09/19) is high. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E_1}$, or the rising edge of E_2 (MK48Z09/19). A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E_1}$ or the falling edge of E_2 (MK48Z09/19). The addresses must be held valid throughout the cycle. $\overline{E_1}$ or $\overline{W}$ must return high or E_2 (MK48Z09/19) must return low for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DS} prior to the end of write and must remain valid for t_{DH} afterward.

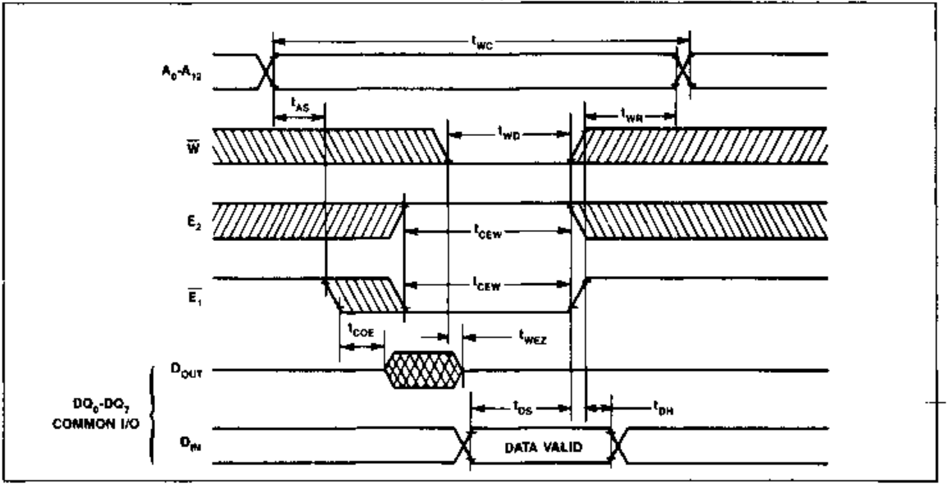
Because $\overline{G}$ is a Don't Care in Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE CYCLE 1 ($\overline{W}$ CONTROLLED WRITE)



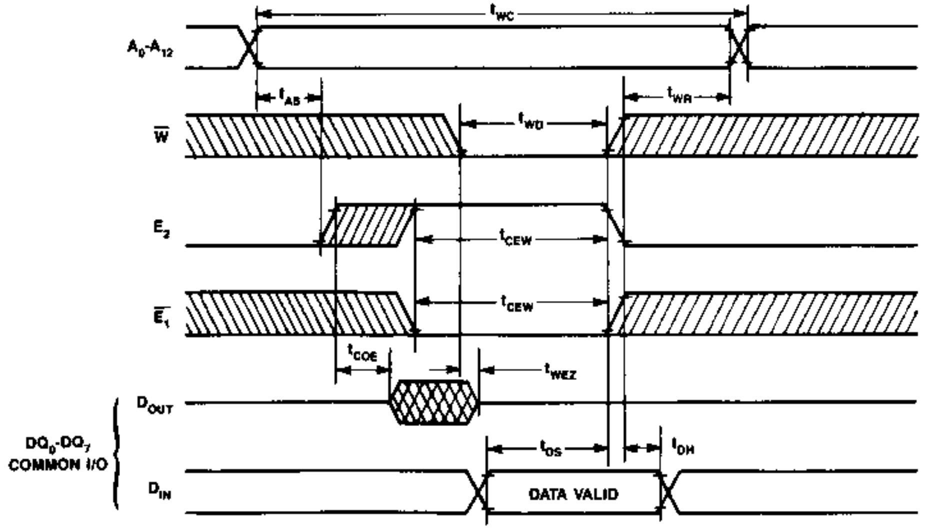
t_{WC}
A_0-A_{12}
t_{AS}
t_{WR}
$\overline{W}$
t_{WD}
E_2
t_{CEW}
$\overline{E_1}$
t_{CEW}
t_{WEZ}
t_{OEW}
D_{OUT}
DQ_0-DQ_7
COMMON I/O
t_{DS}
t_{DH}
D_{IN}
DATA VALID

FIGURE 5. WRITE CYCLE 2 ($\overline{E_1}$ CONTROLLED WRITE)



t_{WC}
A_0-A_{12}
t_{AS}
t_{WR}
$\overline{W}$
t_{WD}
E_2
t_{CEW}
$\overline{E_1}$
t_{CEW}
t_{COE}
t_{WEZ}
D_{OUT}
DQ_0-DQ_7
COMMON I/O
t_{DS}
t_{DH}
D_{IN}
DATA VALID

FIGURE 6. WRITE CYCLE 3 (E_2 CONTROLLED WRITE)



t_{WC}
A_0-A_{12}
t_{AS}
t_{WR}
$\overline{W}$
t_{WD}
E_2
t_{CEW}
$\overline{E_1}$
t_{CEW}
t_{COE}
t_{WEZ}
D_{OUT}
DQ_0-DQ_7
COMMON I/O
t_{DS}
t_{DH}
D_{IN}
DATA VALID

WRITE CYCLE
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq +70°C$) (V_{CC} (min) $\leq V_{CC} \leq V_{CC}$ (max))

SYM	PARAMETER	MK48ZXX-15 MIN	MK48ZXX-15 MAX	MK48ZXX-20 MIN	MK48ZXX-20 MAX	MK48ZXX-25 MIN	MK48ZXX-25 MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	150	—	200	—	250	—	ns	
t_{WD}	Write Pulse Width	100	—	150	—	200	—	ns	
t_{CEW}	Chip Enable to End of Write	130	—	180	—	230	—	ns	
t_{AS}	Address Set up Time	0	—	0	—	0	--	ns	
t_{WR}	Write Recovery Time	10	—	10	—	10	—	ns	
t_{WEZ}	$\overline{W}$ to Output High-Z	—	75	—	100	—	125	ns	
t_{DS}	Data Setup Time	70	—	80	—	90	—	ns	
t_{DH}	Data Hold Time	5	—	5	—	5	—	ns	
t_{OEW}	$\overline{W}$ High to Output Low Z	10	—	10	—	10	—	ns	

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E_1}$ or $\overline{W}$ at V_{IH} or E_2 at V_{IL} after Power-Up	120		µs	
t_{PFX}	$\overline{INT}$ Low to Auto Deselect	10	40	µs	
t_{PFH}	V_{PFD} (Max) to $\overline{INT}$ High		120	µs	4
t_{FB}	V_{PFD} (Min) to V_{SO}	10		µs	

DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MK48Z08/09)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MK48Z18/19)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

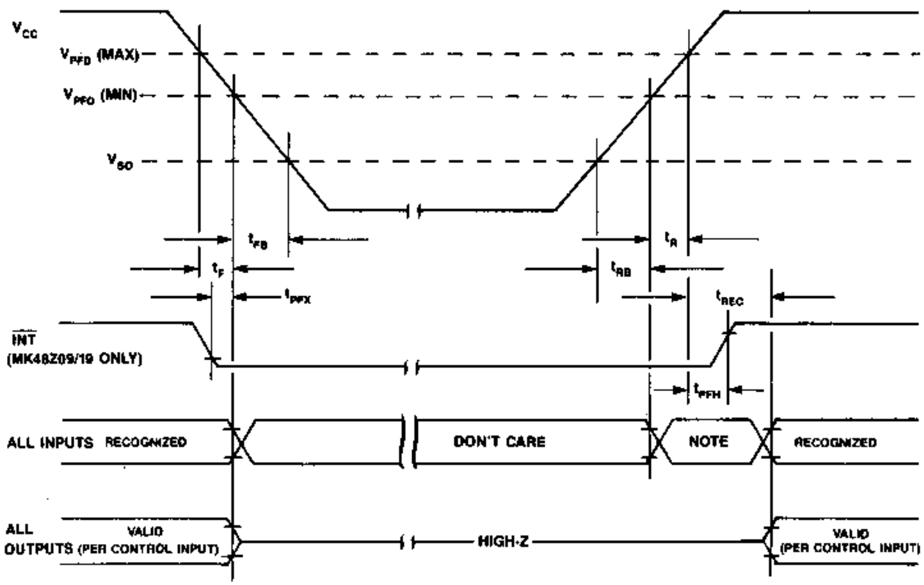
NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 40 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.
4. $\overline{INT}$ may go high anytime after V_{CC} exceeds V_{PFD} (min) and is guaranteed to go high t_{PFH} after V_{CC} exceeds V_{PFD} (max).

CAUTION

Negative Undershoots Below −0.3 volts are not allowed
on any pin while in Battery Back-up mode.

FIGURE 7. POWER DOWN/POWER-UP TIMING



NOTE:
Inputs may or may not be recognized at this time. Caution should be taken to keep E_1 or W in the high state or E_2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Power Fail and Data Retention

With V_{CC} applied, the MK48Z08/18/09/19 operates as a static RAM. The Power-Fail Detect Circuit of the MK48Z08/18/09/19 constantly monitors V_{CC}. Because the reference voltage applied to the detector/comparator is stabilized over temperature, the Power-Fail Detect trip point remains within the V_{PFD} min/max window under all rated conditions. Once deselection has occurred, all inputs and outputs are "Don't Cares" and may have anywhere from −0.3 to 5.5 volts applied to them with absolutely no effect upon the RAM.

As V_{CC} falls below approximately V_{SO} volts, the power switching circuit connects the lithium battery to supply power to the RAM.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above approximately V_{SO} volts. Normal RAM operation can resume t_{REC} after V_{CC} reaches V_{PFD} (max). Caution should be taken to keep $\overline{E_1}$, or $\overline{W}$ in the high state or E_2 low as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertant write cycles after V_{CC} rises but before normal system operation begins.

INTERRUPT FUNCTION

The MK48Z09/19 provides a power-fail interrupt output labeled $\overline{INT}$. The $\overline{INT}$ pin eliminates the need for external power sensing components in applications where an orderly shutdown of the system is necessary. The $\overline{INT}$ pin is open drain for "wire or" applications and provides the user with 10 µs to 40 µs advanced warning of an impending power-fail write protect.

DATA RETENTION TIME

About Figure 8

Figure 8 illustrates how expected MK48Z08/18/09/19 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MK48Z08/18/09/19 spends in battery back-up mode.

Battery life predictions presented in Figure 8 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.4 volt closed-circuit voltage across a 250K ohm load resistance.

> A Special Note: The summary presented in Figure 8 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 8. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure 8 indicates that a particular MK48Z08/18/09/19 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 19 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected to fail within 19 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MK48Z08/18/09/19 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 8 indicates, the predicted life of the battery in the MK48Z08/18/09/19 is a function of temperature. The back-up current required by the memory matrix in the MK48Z08/18/09/19 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 8. If the MK48Z08/18/09/19 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)]+[(TA_2/TT)/BL_2]+\ldots+[(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see **Figure 8**).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A cash register/terminal operates in an environment where the MK48Z08/18/09/19 is exposed to temperatures of 30°C (86°F) or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 40°C (104°F), for 5256 hrs/yr; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs/yr.

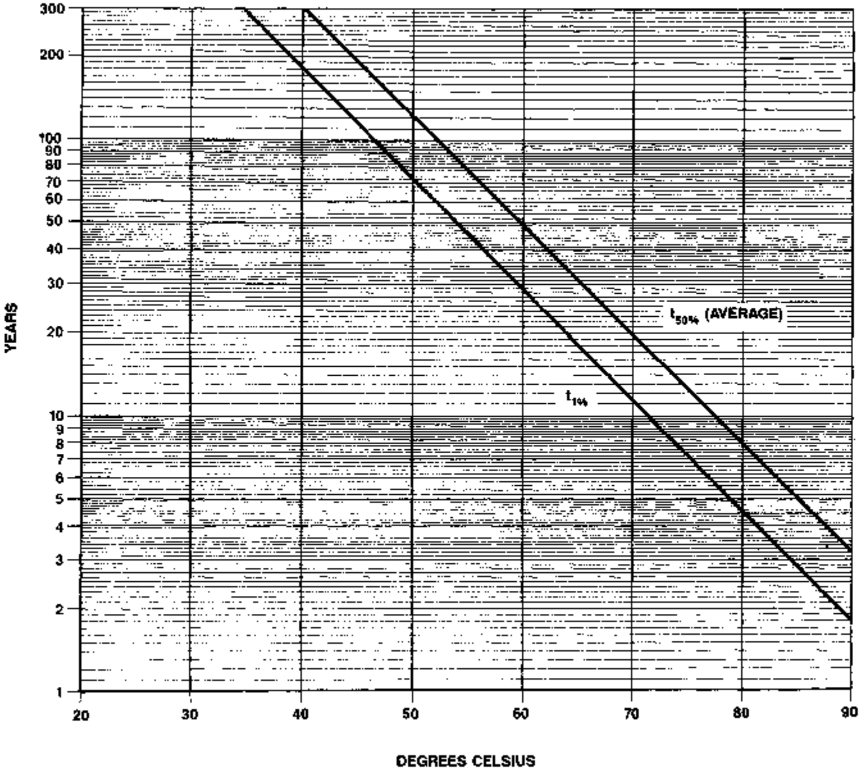
Reading predicted t1% life values from Figure 8; BL_1 = 300 yrs., BL_2 = 175 yrs., BL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 3066 hrs./yr. TA_2 =5256 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Battery Life} \geq \frac{1}{[(3066/8760)/300]+[(5256/8760)/175]+[(438/8760)/11.4]}$$

$$\geq 111.3 \text{ yrs.}$$

FIGURE 8. MK48Z08/18/09/19 PREDICTED BATTERY LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Total Power Dissipation . . . . 1.0 watt
Output Current Per Pin . . . . 10 mA
Voltage On Any Pin Relative To GND . . . . −0.3 V to +7.0 V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . 0°C to +70°C
Ambient Storage (V_{CC} Off) Temperature . . . . −40°C to +85°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below −0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MK48Z08/09)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MK48Z18/19)	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} (min) $\leq V_{CC} \leq V_{CC}$ (max))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		50	mA	3
I_{CC2}	TTL Standby Current ($\overline{E_1} = V_{IH}$ or $E_2 = V_{IL}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E_1} \geq V_{CC} - 0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	µA	4
I_{LO}	Output Leakage Current	−5	+5	µA	4
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	
$V_{\overline{INT}}$	$\overline{INT}$ Logic "0" Voltage (I_{OUT} = 0.5 mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	CONDITIONS	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

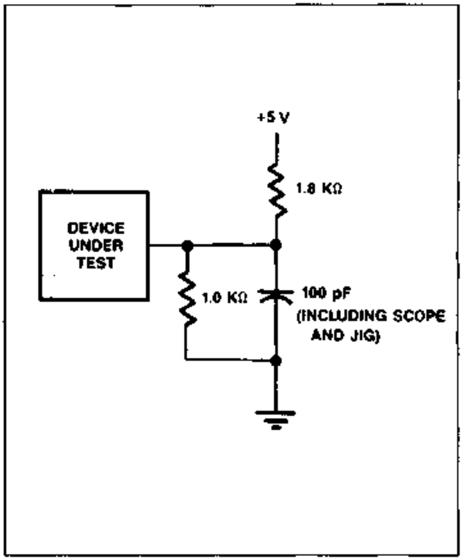
NOTES

1. All voltages referenced to GND.
2. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with GND $\leq V_I \leq V_{CC}$ and outputs deselected.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC} MK48Z08/09	4.75 V to 5.5 V
V_{CC} MK48Z18/19	4.5 V to 5.5 V

FIGURE 9. OUTPUT LOAD DIAGRAM



ORDERING INFORMATION

MK48Z	X	X	B	-XX
DEVICE FAMILY	V_{CC} RANGE	SPECIAL FUNCTIONS	PACKAGE	SPEED

-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME
-25 250 NS ACCESS TIME

B PLASTIC WITH BATTERY TOP HAT

8 SINGLE CHIP SELECT
9 TWO CHIP SELECTS AND INTERRUPT OUT

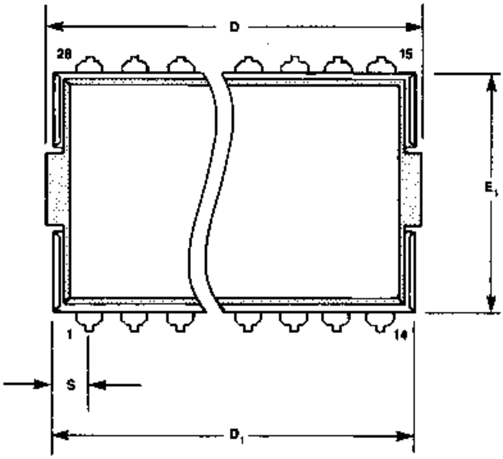
0 V_{CC} = +10%/−5%
1 V_{CC} = +10%/−10%

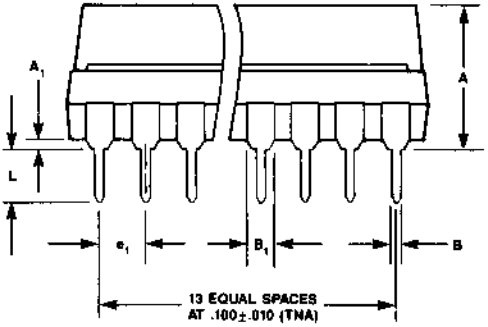
MK Commerical Temp Range 0°C +70°C

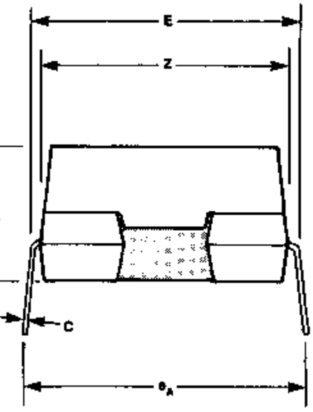
PACKAGE DESCRIPTION

B PACKAGE 28 PIN

	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	37.973	—	1.495	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
DIP-28 PLASTIC D.I.P. ONLY	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D_1	—	37.338	—	1.470	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	







NOTES:

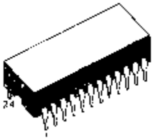
1. Lead finish is to be specified on the detail specifications.
2. Overall length includes .010 in. flash on either end of the package.
3. Package standoff to be measured per JEDEC requirements.
4. Measured from centerline to centerline at lead tips.
5. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

SGS-THOMSON
MICROELECTRONICS

MKI48Z02/12(B) -15/20/25

2K × 8 ZEROPOWER™ RAM

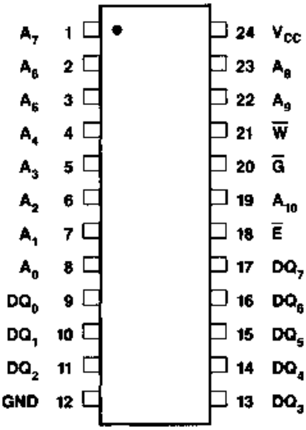
- INDUSTRIAL TEMPERATURE RANGE −40°C to +85°C
- PREDICTED WORST CASE BATTERY LIFE OF 6 YEARS @ 85°C
- DATA RETENTION IN THE ABSENCE OF POWER
- DATA SECURITY PROVIDED BY AUTOMATIC WRITE PROTECTION DURING POWER FAILURE
- +5 VOLT ONLY READ/WRITE
- CONVENTIONAL SRAM WRITE CYCLES
- LOW POWER-440 mW ACTIVE; 5.5 mW STANDBY
- 24-PIN DUAL IN LINE PACKAGE, JEDEC 24 PIN MEMORY PINOUT
- READ-CYCLE TIME EQUALS WRITE-CYCLE TIME
- ON BOARD LOW-BATTERY WARNING CIRCUITRY
- TWO POWER-FAIL DESELECT TRIP POINTS AVAILABLE
  MKI48Z02 4.75V $\geq V_{PFD} \geq$ 4.50V
  MKI48Z12 4.50V $\geq V_{PFD} \geq$ 4.20V



B
DIP-24
(Plastic with Battery Top Alt)

Part Number	Access Time	R/W Cycle Time
MKI48ZX2-15	150 ns	150 ns
MKI48ZX2-20	200 ns	200 ns
MKI48ZX2-25	250 ns	250 ns

FIGURE 1. PIN CONNECTIONS



TRUTH TABLE (MKI48Z02/12)

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ
$< V_{CC}$ (Max) $> V_{CC}$ (Min)	V_{IH} V_{IL} V_{IL} V_{IL}	X X V_{IL} V_{IH}	X V_{IL} V_{IH} V_{IH}	Deselect Write Read Read	High-Z D_{IN} D_{OUT} High-Z
$< V_{PFD}$ (Min) $> V_{SO}$	X	X	X	Power-Fail Deselect	High-Z
$\leq V_{SO}$	X	X	X	Battery Back-up	High-Z

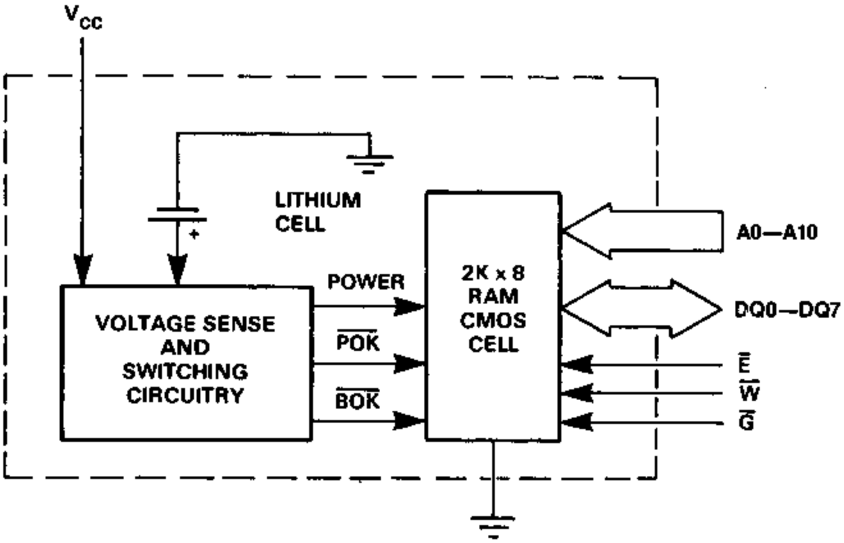
PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0—DQ_7 Data In/Data Out			

DESCRIPTION

The MKI48Z02/12 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using CMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards against inadvertent data loss have been incorporated to maintain data integrity in the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MKI48Z02/12 also matches the pinning of 2716 EPROM and 2K x 8 EEPROM. Like other static RAMs, there is no limit to the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require only +5 volts, no additional support circuitry is needed for interface to a microprocessor.

FIGURE 2. BLOCK DIAGRAM


V_{CC}
LITHIUM CELL
+
POWER
$\overline{POK}$
$\overline{BOK}$
VOLTAGE SENSE AND SWITCHING CIRCUITRY
2K x 8 RAM CMOS CELL
A0—A10
DQ0—DQ7
$\overline{E}$
$\overline{W}$
$\overline{G}$

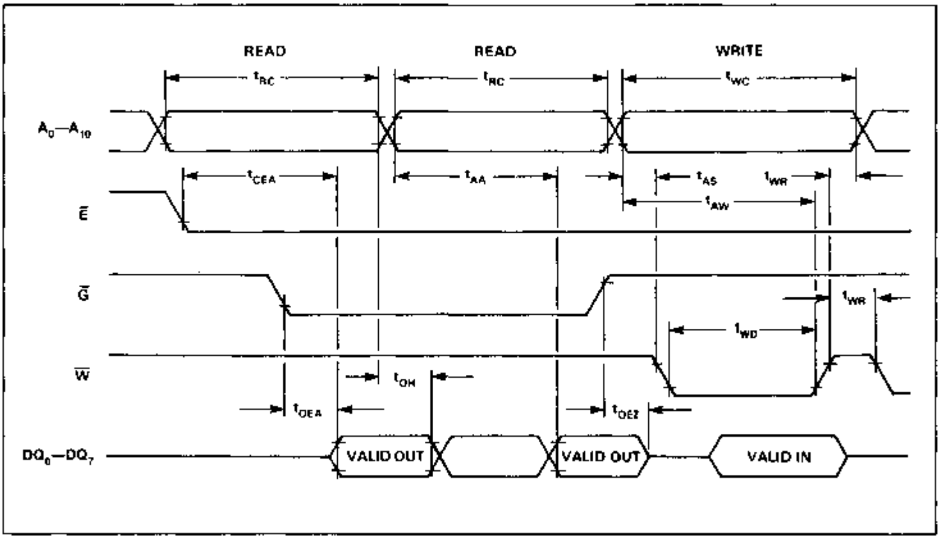
OPERATION

Read Mode

The MKI48Z02/12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2,048 bytes of data is to be accessed.

Valid data will be available to the eight data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}), rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

FIGURE 3. READ-READ-WRITE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE TIMING)

($-40°C \leq T_A \leq +85°C$) ($V_{CC}$ (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

		MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	1
t_{CEA}	Chip Enable Access Time		150		200		250	ns	1
t_{OEA}	Output Enable Access Time		75		80		90	ns	1
t_{CEZ}	Chip Enable Hi to High-Z		35		40		50	ns	
t_{OEZ}	Output Enable Hi to High-Z		35		40		50	ns	
t_{OH}	Valid Data Out Hold Time	15		15		15		ns	1

NOTE

1. Measured using the Output Load Diagram shown in Figure 8.

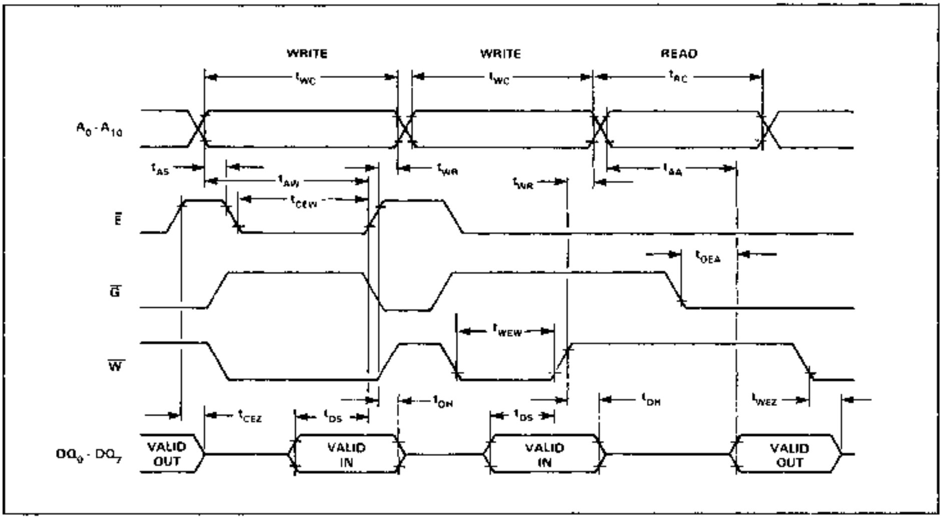
WRITE MODE

The MKI48Z02/12 is in Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are held low. The start of a Write is referenced to the latter occurring falling edge of either $\overline{W}$ or $\overline{E}$. A Write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ or $\overline{E}$ must return high for a minimum of t_{WR} prior to the initiation of another Read or Write Cycle. Data-in must be valid for t_{DS} prior to the End of Write and remain valid for t_{DH} afterward.

Some processors thrash producing spurious Write Cycles during power-up, despite application of a power-on reset. Users should force $\overline{W}$ or $\overline{E}$ high during power-up to protect memory after V_{CC} reaches V_{CC} (min) but before the processor stablizes.

The MKI48Z02/12 $\overline{G}$ input is a DON'T CARE in the write mode. $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after $\overline{W}$ falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 4. WRITE-WRITE-READ TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE TIMING)

($-40°C \leq T_A \leq +85°C$) ($V_{CC}$ (Max) $\geq V_{CC} \geq V_{CC}$ (Min))

SYM	PARAMETER	MKI48ZX2-15		MKI48ZX2-20		MKI48ZX2-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{WEW}	Write Enable to End of Write	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEZ}	Write Enable Low to High-Z		50		60		80	ns	

DATA RETENTION MODE

With V_{CC} applied, the MKI48Z02/12 operates as a conventional BYTEWIDE static ram. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. The MKI48Z02 has a V_{PFD} (max) to V_{PFD} (min) window of 4.75 volts to 4.5 volts, providing very high data security, particularly when all of the other system components are specified to 5.0 volts plus and minus 10%. The MKI48Z12 has a V_{PFD} (max) to V_{PFD} (min) window of 4.5 volts to 4.2 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the current address location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MKI48Z02/12 may respond to transient noise spikes that reach into the deselect window if they should occur during the time the device is sampling V_{CC}. Therefore decoupling of power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after first write, and normal RAM operation resumes. Figure 5 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD} (Max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD} (Min) as some systems may perform inadvertent write cycles after V_{CC} rises but before normal system operation begins.

FIGURE 5. CHECKING THE $\overline{\text{BOK}}$ FLAG STATUS

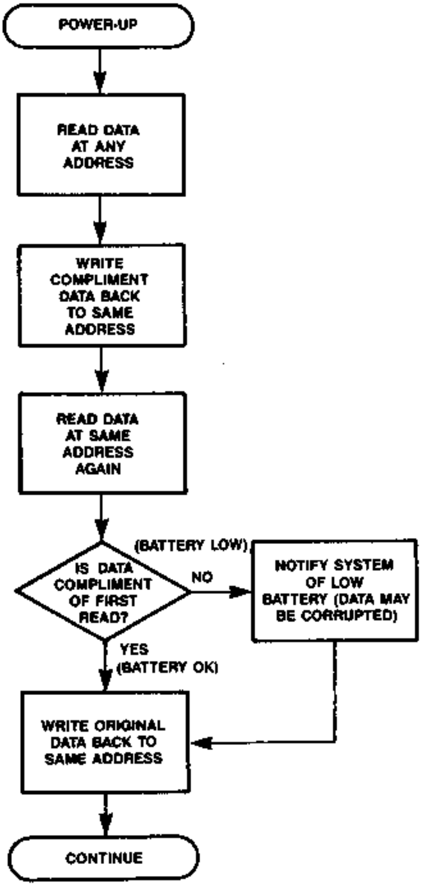
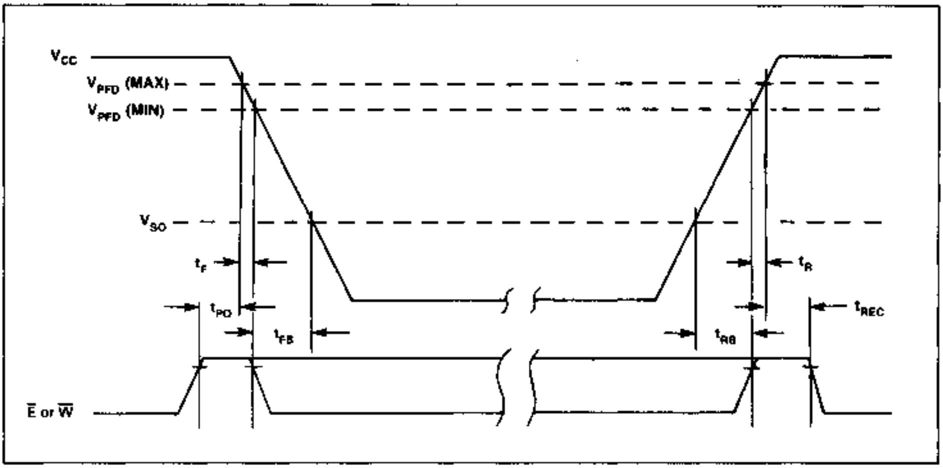

POWER-UP
READ DATA AT ANY ADDRESS
WRITE COMPLIMENT DATA BACK TO SAME ADDRESS
READ DATA AT SAME ADDRESS AGAIN
IS DATA COMPLIMENT OF FIRST READ?
(BATTERY LOW)
NO
NOTIFY SYSTEM OF LOW BATTERY (DATA MAY BE CORRUPTED)
YES
(BATTERY OK)
WRITE ORIGINAL DATA BACK TO SAME ADDRESS
CONTINUE

FIGURE 6. POWER-DOWN/POWER-UP TIMING



DC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TRIP POINT VOLTAGES)

($-40°C \leq T_A \leq +85°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage (MKI48Z02)	4.50	4.6	4.75	V	1
V_{PFD}	Power-fail Deselect Voltage (MKI48Z12)	4.20	4.3	4.50	V	1
V_{SO}	Battery Back-up Switchover Voltage		3		V	1

AC ELECTRICAL CHARACTERISTICS (POWER-DOWN/POWER-UP TIMING)

($-40°C \leq T_A \leq +85°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		ns	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		µs	2
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		µs	3
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		µs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} Rise Time	0		µs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

NOTES:

1. All voltages referenced to GND.
2. V_{PFD} (Max) to V_{PFD} (Min) fall times of less t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (Min). V_{PFD} (Max) to (Min) fall times of less than 10 µs may cause corruption of RAM data.
3. V_{PFD} (Min) to V_{SO} fall times of less than t_{FB} may cause corruption of RAM data.

CAUTION

Negative undershoots below −0.3 volts are not allowed on any pin while in Battery Back-up mode.

DATA RETENTION TIME

About Figure 7

Figure 7 illustrates how expected MKI48Z02/12 battery life is influenced by temperature. The life of the battery is controlled by temperature and is virtually independent of the percentage of time the MKI48Z02/12 spends in battery back-up mode.

Battery life predictions presented in Figure 7 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failure mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's ongoing battery testing since it began in 1982, we believe the likelihood of such failure mechanisms surfacing is extremely poor. For the purpose of this testing, a cell failure is defined as the inability of a cell stabilized at 25°C to produce a 2.0 volt closed-circuit voltage across a 250K ohm load resistance.

> A Special Note: The summary presented in Figure 7 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read-points of life tests presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 7. They are labeled "Average ($t_{50\%}$)" and "($t_{1\%}$)". These terms relate to the probability that a given number of failures will have accumulated by a particular point in time. If, for example, expected life at 80°C is at issue, Figure 7 indicates that a particular MKI48Z02/12 has a 1% chance of having a battery failure 10 years into its life and a 50% chance of failure at the 17 year mark. Conversely, given a sample of devices, 1% of them can be expected to experience battery failure within 10 years; 50% of them can be expected to fail within 17 years.

The $t_{1\%}$ figure represents the practical onset of wear-out, and is therefore suitable for use in what would normally be though of as a worst-case analysis. The $t_{50\%}$ figure represents "normal" or "average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning on the date of manufacture. Each MKI48Z02/12 is marked with a four digit manufacturing date code in the form YYWW (Example: 8502 = 1985, week 2).

Calculating Predicted Battery Life

As Figure 7 indicates, the predicted life of the battery in the MKI48Z02/12 is a function of temperature. The back-up current required by the memory matrix in the MKI48Z02/12 is so low that it has negligible influence on battery life.

Because predicted battery life is dependent upon application controlled variables, only the user can estimate predicted battery life in a given design. As long as ambient temperature is held reasonably constant, expected life can be read directly from Figure 7. If the MK148Z02/12 spends an appreciable amount of time at a variety of temperatures, the following equations should be used to estimate battery life.

$$\text{Predicted Battery Life} = \frac{1}{[(TA_1/TT)/BL_1)] + [(TA_2/TT)/BL_2] + \ldots + [(TA_n/TT)/BL_n)]}$$

Where TA_1, TA_2, TA_n = Time at Ambient Temperature 1, 2, etc.

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_n$

BL_1, BL_2, BL_n = Predicted Battery Lifetime at Temp 1, Temp 2, etc. (see Figure 7).

EXAMPLE PREDICTED BATTERY LIFE CALCULATION

A process control computer operates in an environment where the MKI48Z02/12 is exposed to temperatures of 50°C or less for 3066 hrs/yr; temperatures greater than 25°C, but less than 60°C, for 5256 hrs/yr; and temperatures greater than 40°C, but less than 85°C, for the remaining 438 hrs/yr.

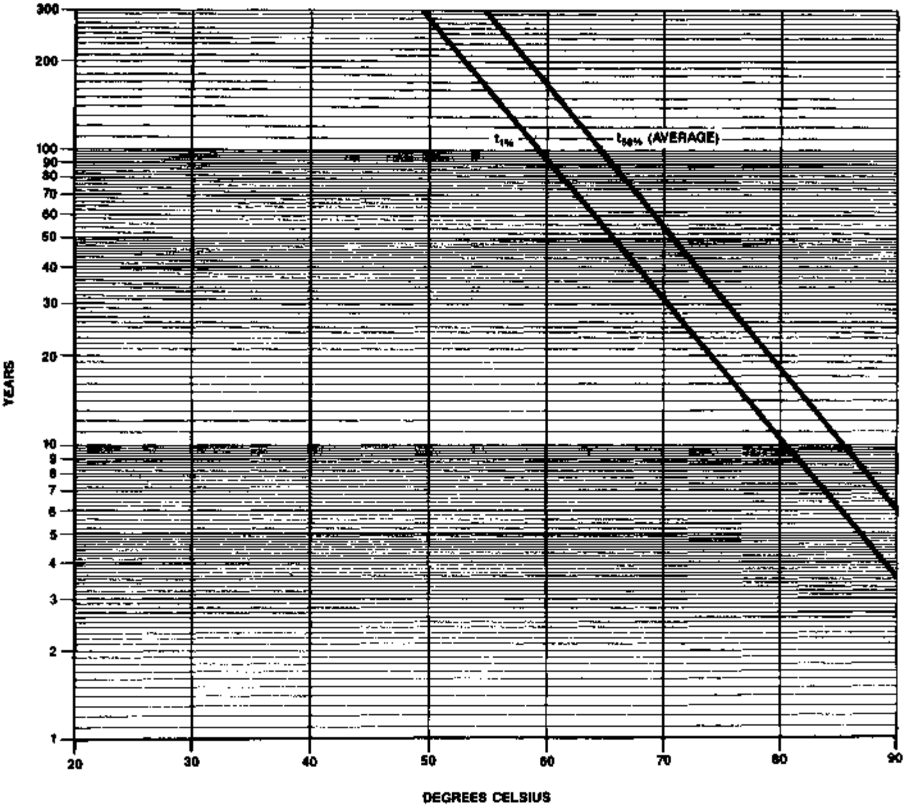
Reading predicted typical life values from Figure 7; $BL_1 = 275$ yrs., $BL_2 = 95$ yrs., $BL_3 = 32$ yrs.

Total Time (TT) = 8760 hrs./yr. $TA_1 = 3066$ hrs./yr. $TA_2 = 5256$ hrs./yr. $TA_3 = 438$ hrs./yr.

$$\text{Predicted Typical Battery Life} \geq \frac{1}{[(3066/8760)/275] + [(5256/8760)/95] + [(438/8760)/32]}$$

$$\geq 109.2 \text{ yrs.}$$

FIGURE 7. MKI48Z02/12 PREDICTED BATTERY STORAGE LIFE VS TEMPERATURE



ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative To GND . . . . -0.3 V to $+7.0$ V
Ambient Operating (V_{CC} On) Temperature (T_A) . . . . -40°C to $+85$°C
Ambient Storage (V_{CC} Off) Temperature . . . . -40°C to $+85$°C
Total Device Power Dissipation . . . . 1 Watt
Output Current Per Pin . . . . 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e do not force these pins below -0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($-40°C \leq T_A \leq +85°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (MKI48Z02)	4.75	5.50	V	1
V_{CC}	Supply Voltage (MKI48Z12)	4.50	5.5	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,2

DC ELECTRICAL CHARACTERISTICS

($-40°C \leq T_A \leq +85°C$) ($V_{CC}$ (max) $\geq V_{CC} \geq V_{CC}$ (min))

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC} - 0.2$ V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	-1	$+1$	μA	4
I_{OL}	Output Leakage Current	-5	$+5$	μA	4
V_{OH}	Output Logic "1" Voltage ($I_{OUT} = -1.0$ mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT} = 2.1$ mA)		0.4	V	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	5
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,5

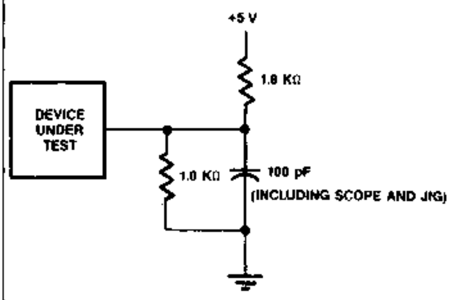
NOTES

1. All voltages referenced to GND.
2. Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.
3. I_{CC1} measured with outputs open.
4. Measured with $GND \leq V_I \leq V_{CC}$ and outputs deselected.
5. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels	0.8 V or 2.2 V
Ambient Temperature	−40°C to +85°C
V_{CC} (MKI48Z02)	4.75 V to 5.50 V
V_{CC} (MKI48Z12)	4.5 V to 5.50 V

FIGURE 8. OUTPUT LOAD DIAGRAM


+5 V
1.8 KΩ
DEVICE UNDER TEST
1.0 KΩ
100 pF
(INCLUDING SCOPE AND JIG)

ORDERING INFORMATION

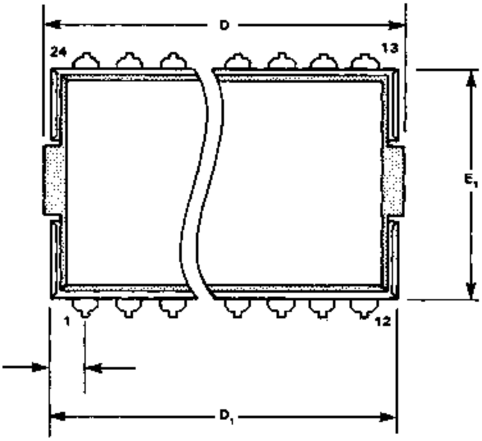
MKI48Z	X	2	B	-XX
DEVICE FAMILY	V_{CC} RANGE		PACKAGE	SPEED

-15	150 NS ACCESS TIME
-20	200 NS ACCESS TIME
-25	250 NS ACCESS TIME
B	PLASTIC WITH BATTERY TOP HAT
0	+10%/−5%
1	+10%/−10%

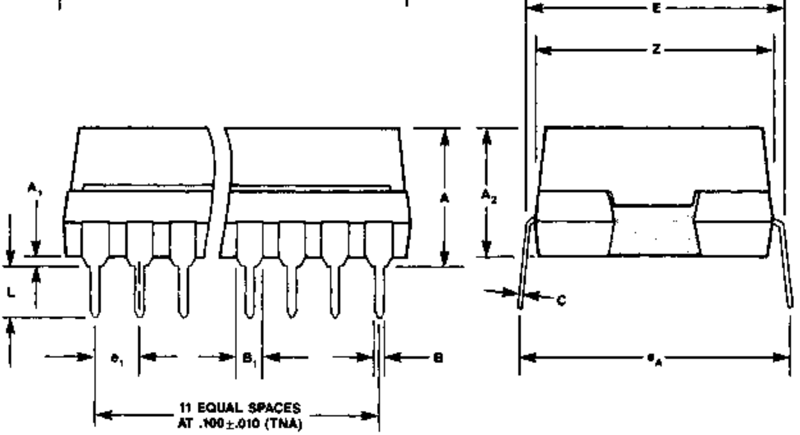
MKI Industrial Temp. Range
−40°C to +85°C

PACKAGE DESCRIPTION

B PACKAGE 24 PIN



	Dim.	mm		inches		Notes
		Min	Max	Min	Max	
BATTERY ONLY	D	—	32.893	—	1.295	
	Z	13.97	14.478	.550	.570	
	A	8.128	9.652	.320	.380	
	A_2	7.62	9.144	.300	.360	
24 PIN PLASTIC D.I.P. ONLY	E_1	13.462	13.97	.530	.550	
	B	0.381	0.533	.015	.021	4
	B_1	1.143	1.778	.045	.070	
	C	0.203	0.355	.008	.014	4
	D_1	—	32.258	—	1.270	1
	E	13.462	16.256	.530	.640	
	e_A	15.24	17.78	.600	.700	3
	e_1	2.286	2.794	.090	.110	
	L	3.048	3.81	.120	.150	
	A_1	0.381	0.762	.015	.030	2
	S	1.524	2.286	.060	.090	



NOTES:

1. Overall length includes .010 in. flash on either end of the package
2. Package standoff to be measured per JEDEC requirements.
3. Measured from centerline to centerline at lead tips
4. When the solder lead finish is specified, the maximum limit shall be increased by .003 in.

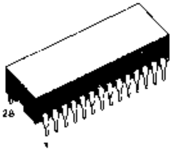
SGS-THOMSON
MICROELECTRONICS

MK48T08 (B)-10/12/15/20

8K X 8 ZEROPOWER TIMEKEEPER RAM

ADVANCED DATA

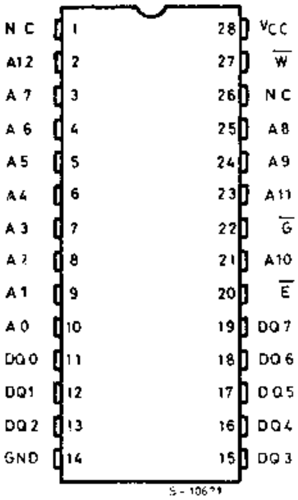
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, CRISTAL, POWER-FAIL CONTROL CIRCUIT AND BATTERY
- BYTEWIDE™ RAM-LIKE CLOCK ACCESS
- BCD CODED YEAR, MONTH, DAY DATE, HOURS, MINUTES AND SECONDS
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- PREDICTED WORST CASE BATTERY STORAGE LIFE OF 11 YEARS @ 70°C
- PIN AND FUNCTION COMPATIBLE WITH JEDEC STANDARD 8K X8 SRAMs
- AUTOMATIC POWER-FAIL CHIP DESELECT/WRITE PROTECTION



B
DIP-28
(Plastic with Battery Top Hat)

Part Number	Access Time	R/W Cycle Time
MK48T08-10	100 ηs	100 ηs
MK48T08-12	120 ηs	120 ηs
MK48T08-15	150 ηs	150 ηs
MK48T08-20	200 ηs	200 ηs

PIN CONNECTIONS


N C 1
A12 2
A 7 3
A 6 4
A 5 5
A 4 6
A 3 7
A 2 8
A 1 9
A 0 10
DQ 0 11
DQ1 12
DQ 2 13
GND 14
28 V_CC
27 W̄
26 N C
25 A 8
24 A 9
23 A 11
22 Ḡ
21 A10
20 Ē
19 DQ 7
18 DQ 6
17 DQ 5
16 DQ 4
15 DQ 3
S - 10671

PIN NAMES

A0-A12	ADDRESS INPUTS
$\overline{E}$	CHIP ENABLE
GND	Ground
NC	NO CONNECTION
V_{CC}	+5 VOLTS
$\overline{W}$	WRITE ENABLE
G	OUTPUT ENABLE
DQ0-DQ7	DATA IN/DATA OUT

June 1988

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

TRUTH TABLE MK48T08

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
< V_{CC} (max) V_{CC} (min)	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
< V_{PFD} (min) > V_{SO}	X	X	X	Deselect	High-Z	CMOS Standby
≤ V_{SO}	X	X	X	Deselect	High-Z	Battery Back-up

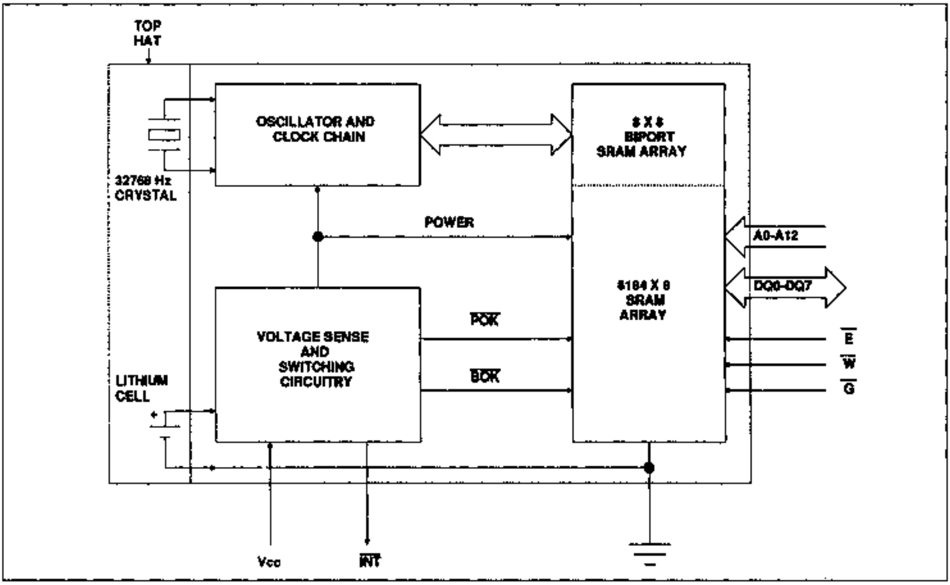
DESCRIPTION

The MK48T08 combines an 8K × 8 full CMOS SRAM, a BYTEWIDE accessible real time clock, a crystal and a long life lithium carbon monofluoride battery, all in a single plastic DIP package. The MK48T08 is a non-volatile pin and function equivalent to any JEDEC standard 8K × 8 SRAM. It also easily fits into many EPROM and EEPROM sockets, providing the non-volatility of the PROMs without any requiremnt for special write timing, or limitations on the number of writes that can be performed.

Access to the clock is as simple as conventional BYTEWIDE RAM access because the RAM and the clock are combined on the same die. As figure 1 indicates, the TIMEKEEPER registers are located in the upper eight locations of the RAM. The registers contain, beginning at the top; year, month, date, day, hour, minutes, and seconds data in 24 hour BCD format. Corrections for 28, 29 (Leap Year), 30 and 31 day months are made automatically. The eighth location is a Control register. These registers are not the actual clock counters; they are BiPORT read/write Static RAM memory locations. The MK48T08 includes a clock control circuit that, once every second, dumps the counters into the BiPORT RAM.

Because the Clock Registers are constructed using BiPORT memory cells, access to the rest of the RAM proceeds unhindered by updates to the TIMEKEEPER registers, even if the TIMEKEEPER registers are being updated at the very moment another location in the memory array is accessed. The MK48T08 also has its own Power-fail Detect circuit. The circuit deselects the device when ever V_{CC} is out of range, providing a high degree of data security in the midst of unpredictable system operations brought on by low V_{CC}.

FIGURE 1. BLOCK DIAGRAM

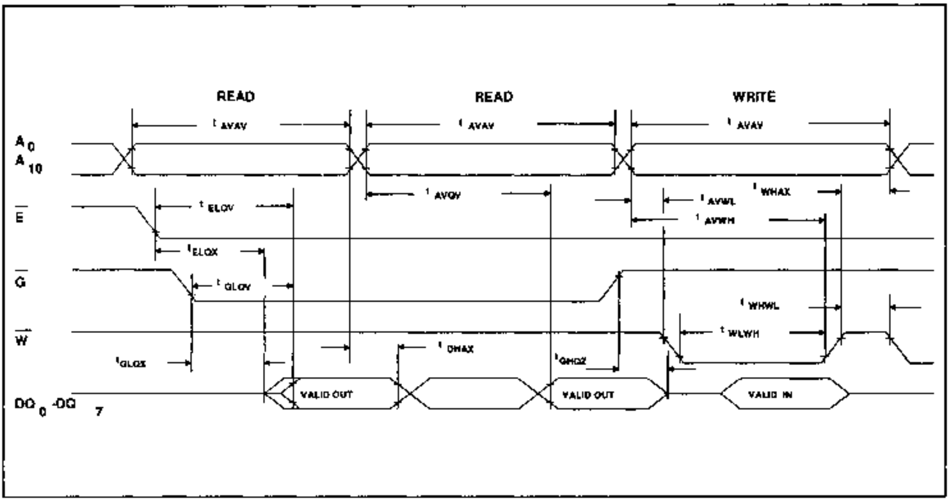

TOP HAT
OSCILLATOR AND CLOCK CHAIN
8 X 8 BIPORT SRAM ARRAY
32768 Hz CRYSTAL
POWER
A0-A12
8184 X 8 SRAM ARRAY
DQ0-DQ7
VOLTAGE SENSE AND SWITCHING CIRCUITRY
$\overline{POK}$
$\overline{BOK}$
$\overline{E}$
$\overline{W}$
$\overline{G}$
LITHIUM CELL
+
Vcc
$\overline{INT}$

READ MODE

The MK48T08 is the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access to any of the 8192 address locations in the static storage array. Valid data will be available at the Data I/O pins within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are satisfied.

If $\overline{E}$ or $\overline{G}$ access times are not yet met, valid data will be available at the latter of Chip Enable Access Time (t_{CEA}) or at Output Enable Access Time (t_{OEA}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the Outputs are activated before t_{AA}, the data lines will be driven to an indeterminate state until t_{AA}. If the Address inputs are changed while $\overline{E}$ and $\overline{G}$ remain low, output data will remain valid for Output Data Hold Time (t_{OH}) but will go indeterminate until the next Address Access.

FIGURE 2. READ CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

($0°C \le TA \le +70°C$, $V_{CC} = 5.0\ V + 10\%/-5\%$)

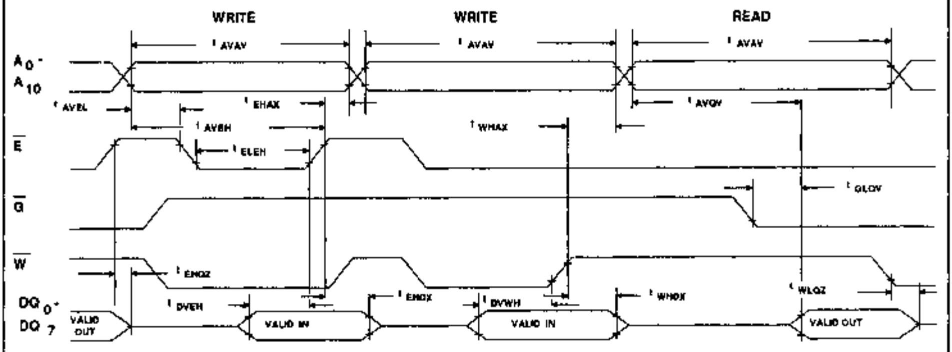
ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	t_{AVAV}	Read Cycle Time	100		120		150		200		ηs	
t_{AA}	t_{AVQV}	Address Access Time		100		120		150		200	ηs	3
t_{CEA}	t_{ELQV}	Chip Enable Access Time		100		120		150		200	ηs	3
t_{CEZ}	t_{EHQZ}	Chip Enable Data Off Time		50		60		75		100	ηs	
t_{OEA}	t_{GLQV}	Output Enable Access Time		50		60		75		100	ηs	3
t_{OEZ}	t_{GHQZ}	Output Enable Data Off Time		40		50		60		80	ηs	
t_{OEL}	t_{GLQX}	Output Enable to Q Low-Z	5		5		5		5		ηs	
t_{CEL}	t_{ELQX}	Chip Enable to Q Low-Z	10		10		10		10		ηs	
t_{OH}	t_{QHAX}	Output Hold from Address	5		5		5		5		ηs	

WRITE MODE

The MK48T08 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ control lines are low. The start of a write is referenced to the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{WR} prior to the initiation of another read or write cycle. Data-in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward.

Because $\overline{G}$ is a Don't Care in the Write Mode and a low on $\overline{W}$ will return the outputs to High-Z, $\overline{G}$ can be tied low and two-wire RAM control can be implemented. A low on $\overline{W}$ will disable the outputs t_{WEZ} after W falls. Take care to avoid bus contention when operating with two-wire control.

FIGURE 3. WRITE CYCLE TIMING



AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

(0°C ≤ TA ≤ +70°C, V_{CC} = 5.0 V + 10%/-5%)

ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	t_{AVAV}	Write Cycle Time	100		120		150		200		ηs	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0		0		ηs	
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0		0		ηs	
t_{CEW}	t_{ELEH}	Chip Enable to End of Write	80		100		130		180		ηs	
t_{AW}	t_{AVWH}	Add. Valid to End of Write	80		100		130		180		ηs	
t_{AW}	t_{AVEH}	Add. Valid to End Write	80		100		130		180		ηs	
t_{WEW}	t_{WLWH}	Write Pulse Width	50		70		100		150		ηs	
t_{ICEZ}	t_{EHQZ}	$\overline{E}$ Data Off Time		50		60		75		100	ηs	
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data Off Time		50		60		57		100	ηs	

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE) (Continued)

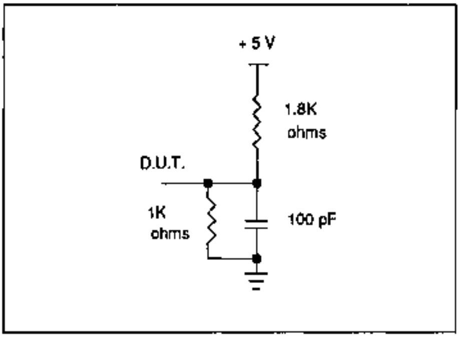
($0°C \leq T_A \leq +70°C$, $V_{CC} = 5.0$ V + 10%/-5%)

ALT. SYM.	STD. SYM.	PARAMETER	MK48T08-10		MK48T08-12		MK48T08-15		MK48T08-20		UNITS	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{WR}	t_{WHAX}	$\overline{W}$ High to Address Change	10		10		10		10		ηs	
t_{WR}	t_{EHAX}	$\overline{E}$ High to Address Change	10		10		10		10		ηs	
t_{WR}	t_{WHWL}	$\overline{W}$ High to $\overline{W}$ Low next Cycle	10		10		10		10		ηs	
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ High	50		60		70		80		ηs	
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ High	50		60		70		80		ηs	
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	5		5		5		5		ηs	
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	5		5		5		5		ηs	

AC TEST CONDITIONS

Input Levels:	0.6V to 2.4V
Transition Times:	5 ns
Input and Output Timing Reference Levels:	0.8V or 2.2V

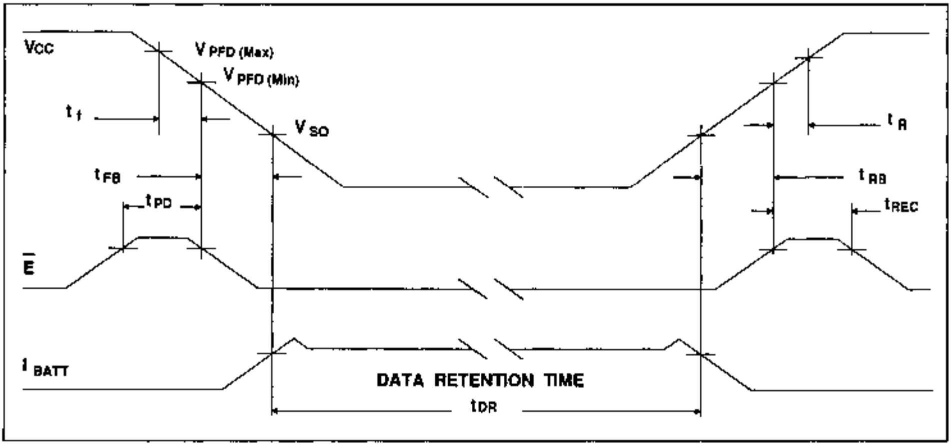
FIGURE 4. OUTPUT LOAD DIAGRAM



CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on all pins (except DQ)	7.0	pF	
C_{DQ}	Capacitance on DQ pins	10.0	pF	

FIGURE 5. POWER-UP / POWER-DOWN CONDITIONS



AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING)
(0°C ≤ TA ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		μs	
t_F	V_{PFD} (Max) to V_{PFD} (Min) V_{CC} Fall Time	300		μs	
t_{FB}	V_{PFD} (Min) to V_{SO} V_{CC} Fall Time	10		μs	
t_{RB}	V_{SO} to V_{PFD} (Min) V_{CC} Rise Time	1		μs	
t_R	V_{PFD} (Min) to V_{PFD} (Max) V_{CC} rise Time	0		μs	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS)
(0°C ≤ TA ≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage	4.5	4.6	4.75	V	
V_{SO}	Battery Back-up Switchover Voltage		3.0		V	
t_{DR}	Expected Data Retention Time (Oscillator On)	5			YEARS	

CAUTION
Negative undershoots below −0.3 volts are not allowed on any pin while in the Battery Back-up mode.

CLOCK OPERATIONS

Reading the Clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading of data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual counter, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written into the "Read" bit, the seventh most significant bit in the Control Register. As long as a "1" reamins in that position, updating is halted. After a Halt is issued, the registers reflect the count, that is day, date, and time that were current at the moment the Halt command was issued.

All of the TIMEKEEPER register are updated simultaneously. A Halt will not interrupt an update in progress. Updating is within a second after the bit is reset a "0".

Setting the Clock

The eight bit of the Control register is the "Write" bit. Setting the Write bit to a "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date and time data in 24 Hour BCD format. Resetting the Write bit to a "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain from the battery. The "Stop" bit is the MSB for the Seconds Register. Setting it to a "1" stops the oscillator.

FIGURE 6. THE MK48T08 REGISTER MAP

ADDRESS	DATA								FUNCTION	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1FFF	—	—	—	—	—	—	—	—	YEAR	00-99
1FFE	X	X	X	—	—	—	—	—	MONTH	01-12
1FFD	X	X	—	—	—	—	—	—	DATE	01-31
1FFC	X	FT	X	X	X	—	—	—	DAY	01-07
1FFB	X	X	—	—	—	—	—	—	HOUR	00-23
1FFA	X	—	—	—	—	—	—	—	MINUTES	00-59
1FF9	ST	—	—	—	—	—	—	—	SECONDS	00-59
1FF8	W	R	S	—	—	—	—	—	CONTROL	

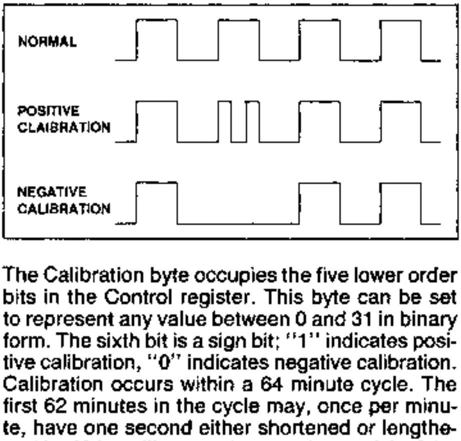
ST = STOP BIT
W = WRITE BIT
R = READ BIT
S = SIGNBIT
FT = FREQUENCY TEST
X = UNUSED

Calibrating the Clock

The MK48T08 is driven by a quartz controlled oscillator with a nominal frequency of 32768 Hz. The crystal is mounted in the tophat along with the battery. A typical MK48T08 is accurate within ± 1 minute per month at 25°C without calibration. The devices are tested not to exceed 35 PPM (parts per million) oscillator frequency error at 25°C, which comes to about ± 1.53 minutes per month. Of course the oscillation rate of any crystal changes with temperature. Figure 6. shows the frequency error that can be expected at various temperatures.

Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The MK48T08 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 128 stage, as shown in figure 7. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

FIGURE 7. ADJUSTING THE DIVIDE BY 128



The Calibration byte occupies the five lower order bits in the Control register. This byte can be set to represent any value between 0 and 31 in binary form. The sixth bit is a sign bit; "1" indicates positive calibration, "0" indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened or lengthened by 256 oscillator cycles, that is one tick of the divide by 128 stage of the clock chain. If a binary "1" is loaded into the register, only the first 4 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 24 will be affected and so on.

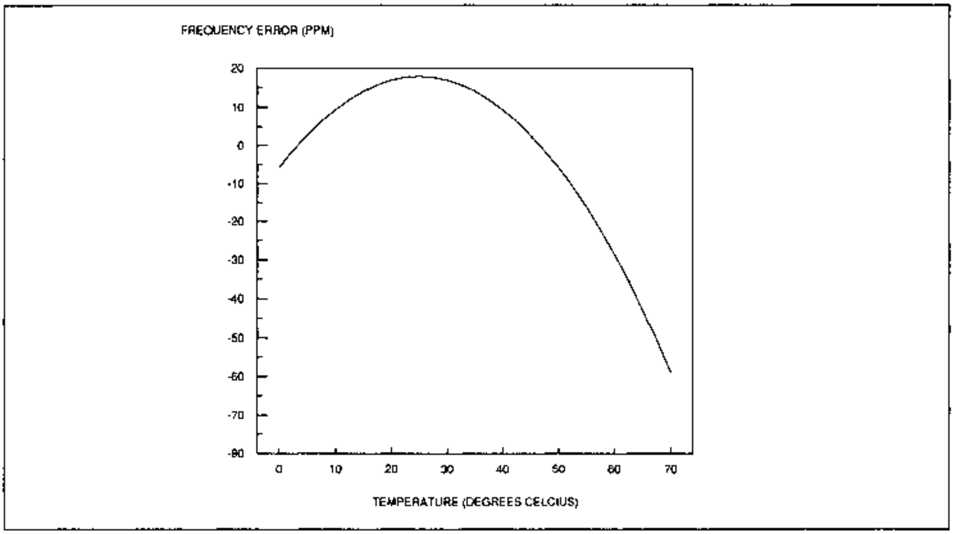
Therefore, each calibration step has the effect of adding or subtracting 512 oscillator cycles for every 125,829, 120 actual oscillator cycles, that is 4.068 PPM of adjustment per calibration step gin the user 126.14 PPM calibration range. Assuming that the oscillator is in fact running at exactly 32768 Hz, each of the 31 increments in the Calibration byte would represent 10.7 seconds per month.

Two methods are available for ascertaining how much calibration a given MK48T08 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte. The utility could even be menu driven and made foolproof.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT.) bit, the seventh-most significant bit in the day Register, is set to a "1", and the oscillator is running at 32768 Hz, the LSB (DQ0) of the Seconds Register will toggle at a 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz would indicate a + 20 PPM oscillator frequency error, requiring a -5 (000101) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency Test output frequency. The device must be selected and addresses must stable at Address 1FF9 when reading the 512 Hz on DQ0.

The FT. bit must be set using the same method used to set the clock, using the Write bit. The LSB of the Seconds Register is monitored by holding the MK48T08 in an extended read of the Seconds Register, without having the Read bit set. The FT. bit MUST be reset to a "0" for normal clock operations to resume.

FIGURE 8. FREQUENCY ERROR WITHOUT CALIBRATION



DATA RETENTION MODE

With V_{CC} applied, the MK48T08 operates as a conventional BYTEWIDE static RAM. Should the supply voltage decay, the RAM will automatically power-fall deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. The MK48T08 has a V_{PFD}(max)-V_{PFD}(min) window of 4.75 volts to 4.5 volts, allowing users constrained to a 10% power supply specification to use the device.

Note: A mid-write cycle power failure may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time does not exceed t_F. The MK48T08 may respond to transient noise spikes that reach into the deselect window if this should occur during the time the device is sampling V_{CC}. Therefore decoupling of the power supply lines is recommended.

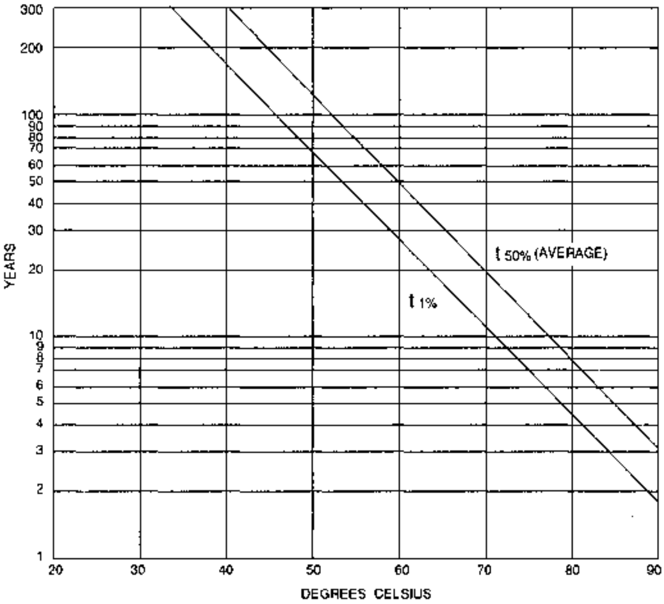
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. Normal RAM operation can resume t_{REC} after V_{CC} exceeds V_{PFD}(max). Caution should be taken to keep $\overline{E}$ or $\overline{W}$ high as V_{CC} rises past V_{PFD}(min) as some systems may perfom inadvertent write cycles after V_{CC} rises but before normal system operation begins.

PREDICTING BACK-UP SYSTEM LIFE

The useful life of the battery in the MK48T08 is expected to ultimately come to an end for one of two reasons; either because it has been discharged wile providing current to an external load; or because the effects of aging render the cell useless before it can actually be discharged. Fortunately, these two effects are virtually unrelated, allowing discharge, or Capacity Consumption and the effects of aging, or Storage Life to be treated as two independent but simultaneous mechanisms, the earlier of which defines Back-up System life.

The current drain that is responsible for Capacity Consumption can be reduced either by applying V_{CC} or turning off the oscillator. With the oscillator off, only the leakage currents required to maintain data in the RAM are flowing. With V_{CC} on, the battery is disconnected from the RAM. Because the leakage currents of the MK48T08 are so low, then can be neglected in practical Storage Life calculations.
Therefore, to extent the life of components that are just sitting on the shelf (not in system use) the oscillator should be turned off.

FIGURE 9. MK48T08 PREDICTED BATTERY STORAGE LIFE VS. TEMP.



Predicting Storage Life

Figure 9 illustrates how temperature affects Storage Life of the MK48T08 battery. As long as V_{CC} is applied or the oscillator is turned off, the life of the battery is controlled by temperature and is virtually unaffected by leakage currents drawn by the MK48T08.

Storage Life predictions presented in Figure 9 are extrapolated from temperature accelerated life-test data collected in over 100 million device hours of continuing bare cell and encapsulated cell battery testing by SGS-THOMSON. Obviously, temperature accelerated testing cannot identify non-temperature dependent failur mechanisms. However, in view of the fact that no random cell failures have been recorded in any of SGS-THOMSON's on going battery testing since it began in 1982, we believe the chance of such failure mechanisms surfacing is extremely small.

For the purpose of the testing, a cell failure is defined as the inability af a cell stabilized a 25°C to produce a 2.0 volt closed-circuit voltage across a 250K load resistance.

A Special Note: The summary presented in Figura 9 represents a conservative analysis of the data presently available. While SGS-THOMSON is most likely in possession of the largest collection of battery life data of this kind in the world, the results presented should not be considered absolute or final; they can be expected to change as yet more data becomes available. We believe that future read points of life test presently under way and improvements in the battery technology itself will result in a continuing improvement of these figures.

Two end of life curves are presented in Figure 9. They are labeled "Average" ($t_{50\%}$) and ($t_{1\%}$). These terms relate to the probability that a given number of failure will have accumulated by a particular point in time. If, for example, expected life at 70°C is at issue, Figure indicates that a particular MK48T08 has a 1% chance of having a battery failure 11 years into its life and a 50% chance of failure at the 20 year mark. Conversely, given a sample of device, 1% of them can be expected to experience battery failure within 11 years; 50% of them can be expected fail within 20 years.

The $t_{1\%}$ figure represents the práctical onset of wear out, and is therefore suitable for use in what would normally be thought of as a worst-case anaysis. The $t_{50\%}$ figure represents "normal" or 'average" life. It is, therefore, accurate to say that the average device will last "$t_{50\%}$".

Battery life is defined as beginning at the date of manufacture. Each MK48T08 is marked with a four digit manufacturing date code in the form YYWW (example: 8625 = 1986, week 25).

Calculating Predicted "Storage Life of the Battery

As Figure 9 indicates, the predicted Storage Life on the battery in the MK48T08 is a function of temperature.

Because the ambient temperature profile is dependent upon application controlled variable, only the user can estimate predicted Storage Life in a given design. As long as ambient temperature is held reasonably constant, expected Storage Life can be read directly from Figure 9. If the MK48T08 spends an appreciable amount of time at a variety of temperatures, the following equation should be used to estimate Storage Life.

$$\text{Predicted Storage Life} = 1 + \{[(TA_1 \div TT) \div SL_1] + [TA_2 \div TT) \div SL_2] + \ldots + [(TA_N \div TT) \div SL_N]\}$$

Where TA_1, TA_2, TA_N, = Time at Ambient Temperature 1, 2, ect

TT = Total Time = $TA_1 + TA_2 + \ldots + TA_N$

SL_1, SL_2, SL_N = Predicted Storage Life at Temp. 1, Temp. 2, ect. (See Figure 9)

Example Predicted Storage Life Calculation

A cash register/terminal operates in an environment where the MK48T08 is exposed to temperatures of 30°C (86°F) or less 4672 hrs./yr.: temperatures greater than 25°C, but less than 40°C (104°F), for 3650 hrs./yr.; and temperatures greater than 40°C, but less than 70°C (158°F), for the remaining 438 hrs./yr.

Reading Predicted $t_{1\%}$ values from Figure 10; SL_1 = 456 yrs., SL_2 = 175 yrs. SL_3 = 11.4 yrs.

Total Time (TT) = 8760 hrs./yr. TA_1 = 4672 hrs./yr. TA_2 = 3650 hrs./yr. TA_3 = 438 hrs./yr.

$$\text{Predicted Typical Storage Life} \geq 1 \div \{[(4672 \div 8760) \div 465] + [3650 + 8760) \div 175] + [(438 \div 8760) \div 11.4]\}$$

$$\text{Predicted Typical Storage Life} \geq 126 \text{ years}$$

ABSOLUTE MAXIMUM RATINGS*

Voltage On Any Pin Relative to GND	−0.3 V to +7.0V
Ambient Operating (V_{CC} On) Temperature (T_A)	0°C to +70°C
Ambient Storage (V_{CC} Off, Oscillator Off) Temperature	−20°C to +70°C
Total Device Power Dissipation	1 Watt
Output Current Per Pin	20 mA

* Stresses grater than those under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the opertional section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq TA \leq +70°C$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply voltage	4.75	5.5	V	
GND	Supply Voltage	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.2	$V_{CC}+0.3$	V	
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	

DC ELECTRICAL CHARACTERISTICS

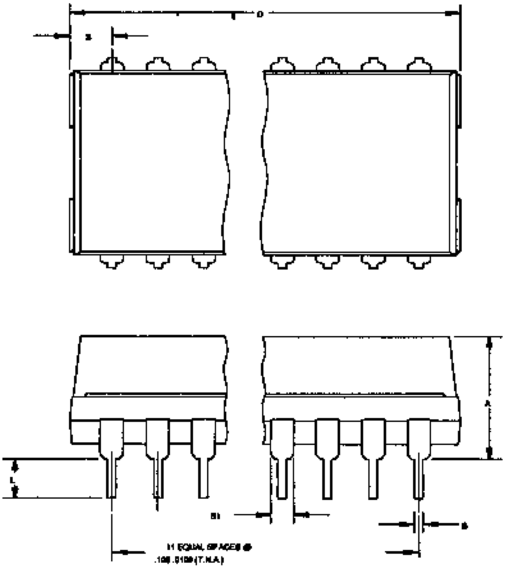
($0°C \leq TA \leq +70°C$) (V_{CC} (Max) $\leq V_{CC} \leq V_{CC}$(Min))

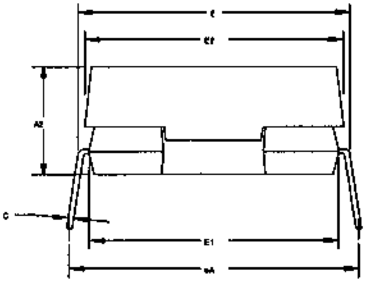
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	
I_{CC2}	TTL Standby Current ($\overline{E}=V_{IH}$)		5	mA	
I_{CC3}	CMOS Standby Current ($\overline{E}=V_{CC}-0.2V$)		3	mA	
I_{IL}	Input Leakage Current (Any Input)	−1	+1	μA	
I_{OL}	Output Leakage Current	−5	+5	μA	
V_{OH}	Output Logic "1" Voltage ($I_{OUT}=-1.0$ mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage ($I_{OUT}=2.1$ mA)		0.4	V	

PACKAGE DESCRIPTION

B PACKAGE 28 PIN

Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	8.128	9.652	.320	.380	2
A1	0.381	0.762	.015	.030	2
A2	7.62	9.144	.300	.360	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	—	37.973	—	1.495	1
E	13.462	16.256	.530	.640	
E1	13.462	13.97	.530	.550	
E1	13.97	14.478	.550	.570	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	3.81	.120	.150	
S	1.524	2.54	.060	.100	





NOTES

1. OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

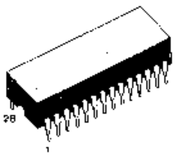
SGS-THOMSON
MICROELECTRONICS

MK48Z30 (B)-10/12/15

32K X 8 ZEROPOWER RAM

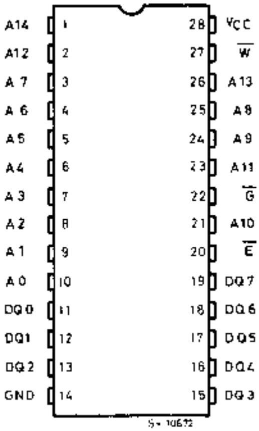
ADVANCED DATA

- DATA RETENTION IN THE ABSENCE OF V_{CC}
- DATA IS AUTOMATICALLY PROTECTED DURING POWER LOSS
- DIRECTLY REPLACES 32K×8 VOLATILE STATIC RAM OR EEPROM
- UNLIMITED WRITE CYCLES
- CMOS - LOW POWER OPERATION
- STANDARD 28-PIN JEDEC PINOUT
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- FULL 10% OPERATING RANGE
- LITHIUM ENERGY SOURCE IS ELECTRICALLY DISCONNECTED TO RETAIN FRESHNESS UNTIL POWER IS APPLIED THE FIRST TIME



B
DIP-28
(Plastic with Battery Top Hat)

PIN CONNECTIONS



TRUTH TABLE MK48Z30

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
$<V_{CC}$ (max) V_{CC} (min)	V_{IH}	X	X	Deselect	High-Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High-Z	Active
$<V_{PFD}$ (min) $>V_{SO}$	X	X	X	Deselect	High-Z	CMOS Standby
$\leq V_{SO}$	X	X	X	Deselect	High-Z	Battery -Back-up

DESCRIPTION

The MK48Z30 is a 262,144-bit, fully static, nonvolatile static RAM organized as 32,768 words by 8 bits. The nonvolatile memory has a self-contained lithium energy source and control circuitry which constantly monitors V_{CC} for an out of tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. The nonvolatile static RAM can be used in place of 32K X 8 static RAM directly conforming to the popular BYTEWIDE 28 pin DIP standard. There is no limit on the number of write cycles which can be executed and no additional support circuitry is required for microprocessor interface.

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

STATIC RAM DEVICES

CACHE TAG RAM

MK41H80(N,P)-20/25/35

4K × 4 CMOS TAGRAM™

- 4K × 4 SRAM WITH ONBOARD 4 BIT COMPARATOR
- 20, 25, AND 35ns ADDRESS TO COMPARE ACCESS TIME
- 12, 15, AND 20ns TAG DATA TO COMPARE ACCESS TIME
- EQUAL ACCESS, READ AND WRITE CYCLE TIMES
- FLASH CLEAR FUNCTION
- 22-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- WORD WIDTH EXPANDABLE

TRUTH TABLE

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	MODE
H	H	H	Valid	Compare Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Flash Clear Cycle

X = Don't Care

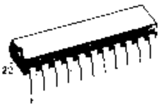
DESCRIPTION

The MK41H80 is a member of SGS-THOMSON's 4K × 4 CMOS Static RAM family featuring fully static operation requiring no external clocks or timing strobes. Cycle Time and Compare Access Time are equal. The MK41H80 is powered by a single +5V ±10% power supply and the inputs and outputs are fully TTL compatible.

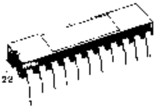
The MK41H80 features an onboard 4 bit comparator that compares RAM contents and current input data. The result is an active high match on the MATCH pin or an active low miss on the MATCH pin. The MATCH pins of several MK41H80's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

Tag data can be read from the data pins by bringing Output Enable ($\overline{OE}$) low. This will allow data stored in the memory array to be displayed at the Outputs (DQ_0-DQ_3).

Flash Clear operation is provided on the MK41H80 via the ($\overline{CLR}$) pin. A low applied to the $\overline{CLR}$ pin clears all RAM bits to a logic zero.

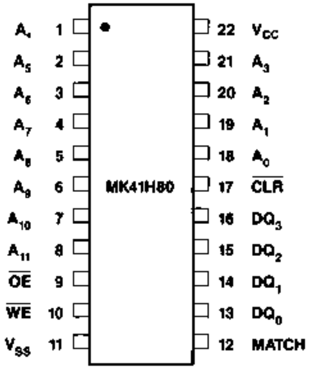


N
DIP-22
(Plastic Package)



P
DIP-22
(Ceramic Package)

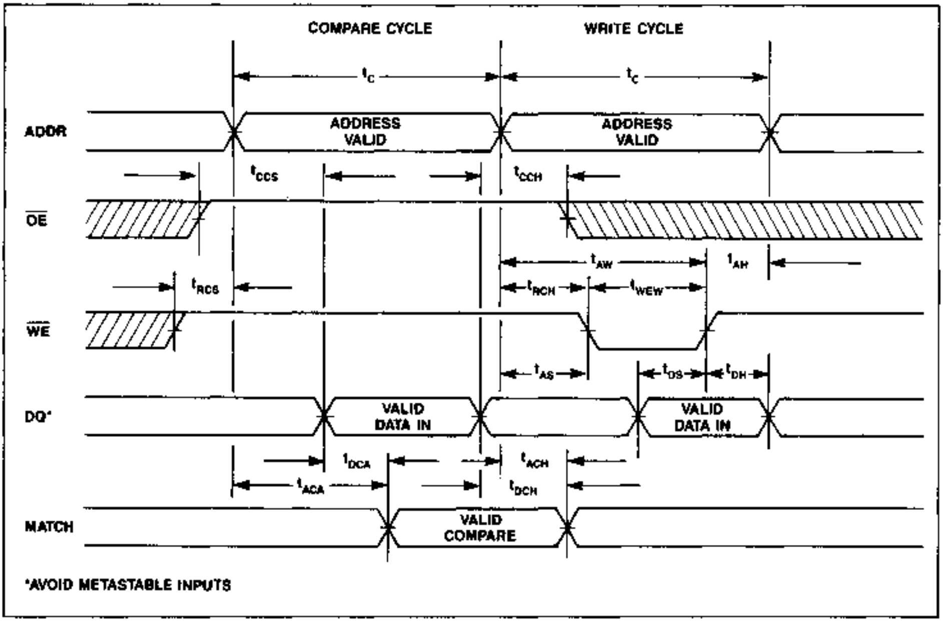
FIGURE 1. PIN CONNECTIONS



PIN NAMES

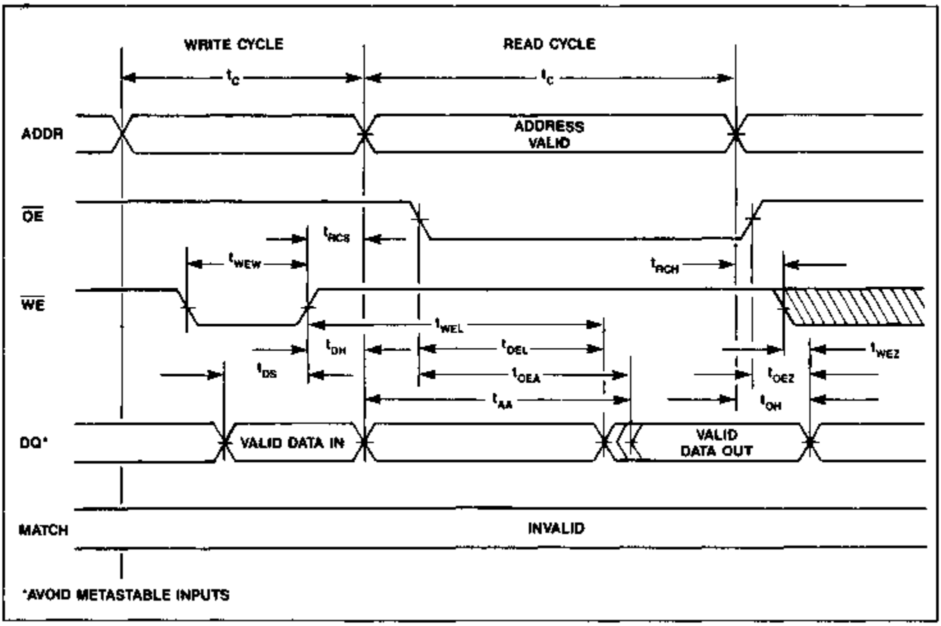
A_0 - A_{11}	- Address Inputs
DQ_0 - DQ_3	- Data Input/Output
MATCH	- Comparator Output
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
$\overline{CLR}$	- Flash Clear
V_{CC}	- Power (+5V)
V_{SS}	- Ground

FIGURE 2. COMPARE AND WRITE CYCLE


COMPARE CYCLE
WRITE CYCLE
t_C
t_C
ADDR
ADDRESS VALID
ADDRESS VALID
t_{CCS}
t_{CCH}
$\overline{OE}$
t_{AW}
t_{AH}
t_{RCS}
t_{RCH}
t_{WEW}
$\overline{WE}$
t_{AS}
t_{DS}
t_{DH}
DQ*
VALID DATA IN
VALID DATA IN
t_{DCA}
t_{ACH}
t_{ACA}
t_{DCH}
MATCH
VALID COMPARE

*AVOID METASTABLE INPUTS

FIGURE 3. WRITE AND READ CYCLE


WRITE CYCLE
READ CYCLE
t_C
t_C
ADDR
ADDRESS VALID
$\overline{OE}$
t_{RCS}
t_{WEW}
t_{RCH}
$\overline{WE}$
t_{WEL}
t_{DH}
t_{OEL}
t_{WEZ}
t_{DS}
t_{OEA}
t_{OEZ}
t_{AA}
t_{OH}
DQ*
VALID DATA IN
VALID DATA OUT
MATCH
INVALID

*AVOID METASTABLE INPUTS

COMPARE, WRITE AND READ TIMING

The MK41H80 employs three signals for device control. The Write Enable ($\overline{\text{WE}}$) pin enables a Write Cycle if low and either a Compare Cycle or a Read Cycle when high. The $\overline{\text{OE}}$ pin enables a Read Cycle if low or a Compare Cycle if high. The $\overline{\text{CLR}}$ pin enables a Flash Clear Cycle when brought low.

The MK41H80 begins a Compare Cycle with the application of a valid address (see Figure 2). A valid MATCH is enabled when $\overline{\text{OE}}$ and $\overline{\text{WE}}$ go high in conjunction with their respective Set Up and Hold times. MATCH will occur t_{ACA} after a valid address, and t_{DCA} after valid Data In. MATCH will then go invalid t_{ACH} after the address changes.

The MK41H80 starts a Write Cycle with stable addresses (see Figure 2). $\overline{\text{OE}}$ may be in either logic state. $\overline{\text{WE}}$ may fall with stable addresses, and must remain low until t_{AW} with a duration of t_{WEW}. Data in must be held valid t_{DS} before and t_{DH} after $\overline{\text{WE}}$ goes high. MATCH will be invalid during this cycle.

The MK41H80 begins a Read Cycle with stable addresses and $\overline{\text{WE}}$ high (see Figure 3). DQ becomes valid t_{AA} after a valid address, and t_{OEA} after the fall of $\overline{\text{OE}}$. DQ outputs become invalid t_{OH} after the address becomes invalid or t_{OEZ} after OE is brought high. Ripple through data access may be accomplished by holding $\overline{\text{OE}}$ active low while strobing addresses A_0-A_{11}, and holding $\overline{\text{CLR}}$ and $\overline{\text{WE}}$ high. The MATCH output will be invalid during the Read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_C	Cycle Time	20		25		35		ns	
t_{CCS}	Compare Command Set Up Time	7		8		10		ns	
t_{CCH}	Compare Command Hold Time	0		0		0		ns	
t_{RCS}	Read Command ($\overline{\text{WE}}$) Set Up Time	0		0		0		ns	
t_{RCH}	Read Command ($\overline{\text{WE}}$) Hold Time	0		0		0		ns	
t_{AS}	Address Set-up Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write Command ($\overline{\text{WE}}$)	16		20		30		ns	
t_{AH}	Address Hold Time after End of Write	0		0		0		ns	
t_{WEW}	Write Command ($\overline{\text{WE}}$) to End of Write	16		20		30		ns	
t_{DS}	Data Set Up Time	12		13		14		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{DCA}	Data Compare Access Time		12		15		20	ns	3
t_{ACA}	Address Compare Access Time		20		25		35	ns	3
t_{ACH}	Address Compare Hold Time	5		5		5		ns	3
t_{DCH}	Data Compare Hold Time	3		3		3		ns	3
t_{OEA}	Output Enable ($\overline{\text{OE}}$) Access Time		10		12		15	ns	3
t_{OH}	Valid Data Out ($\overline{\text{DQ}}$) Hold Time	5		5		5		ns	3
t_{AA}	Address Access Time		20		25		35	ns	3
t_{OEZ}	Output Enable ($\overline{\text{OE}}$) to High-Z		7		8		10	ns	4
t_{OEL}	Output Enable ($\overline{\text{OE}}$) to Low-Z	2		2		2		ns	4
t_{WEZ}	Write Enable ($\overline{\text{WE}}$) to High-Z		8		10		13	ns	4
t_{WEL}	Write Enable ($\overline{\text{WE}}$) to Low-Z	5		5		5		ns	4

APPLICATION

The MK41H80 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK41H80 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

The MK41H80 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input data generating a miss.

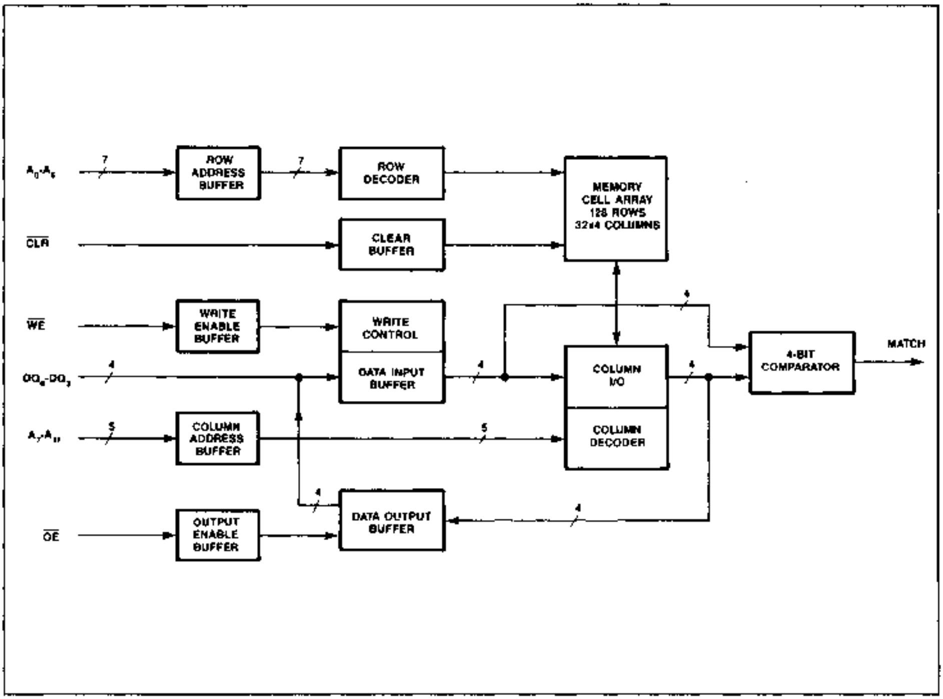
The MATCH output is always at either an active high or low logic level, and does not exhibit a three-state or high impedance characteristic. Since the comparator circuitry is always enabled, metastable data input levels can result in excessive MATCH output activity. Therefore, the use of pull-up or pull-down resistors is recommended on the data bus.

A pull-up resistor is also recommended for the $\overline{CLR}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{CLR}$ below V_{IH} minimum specifications.

Because high frequency current transients will be associated with the operation of the MK41H80, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 4. BLOCK DIAGRAM


A_0-A_6
7
ROW ADDRESS BUFFER
7
ROW DECODER
MEMORY CELL ARRAY 128 ROWS 32x4 COLUMNS
$\overline{CLR}$
CLEAR BUFFER
$\overline{WE}$
WRITE ENABLE BUFFER
WRITE CONTROL
4
4-BIT COMPARATOR
MATCH
DQ_0-DQ_3
4
DATA INPUT BUFFER
4
COLUMN I/O
4
A_7-A_{11}
5
COLUMN ADDRESS BUFFER
5
COLUMN DECODER
4
DATA OUTPUT BUFFER
4
$\overline{OE}$
OUTPUT ENABLE BUFFER

FLASH CLEAR CYCLE

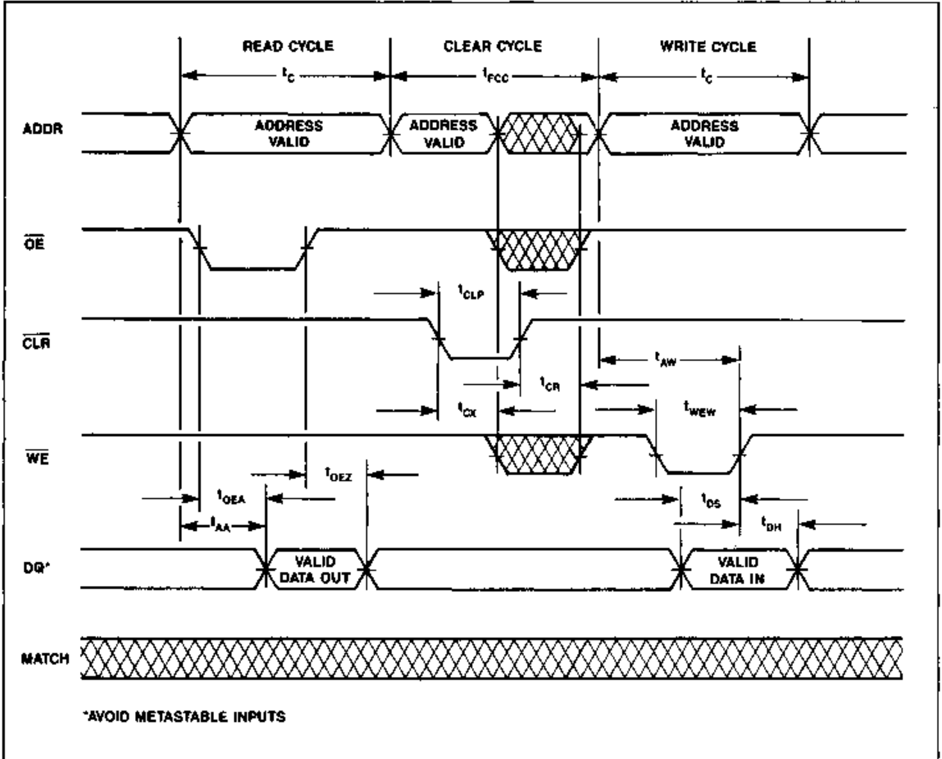
A Flash Clear Cycle begins as $\overline{CLR}$ is brought low (see Figure 5). A Flash Clear sets all 16,384 bits in the RAM to logic zero. Control Inputs will not be recognized from t_{CX} after $\overline{CLR}$ falls to t_{CR} after $\overline{CLR}$ is brought high. $\overline{OE}$ and $\overline{WE}$ are Don't Cares and DQ is High-Z. MATCH will be invalid while $\overline{CLR}$ is low.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	-20 MIN	-20 MAX	-25 MIN	-25 MAX	-35 MIN	-35 MAX	UNITS	NOTES
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CX}	Clear ($\overline{CLR}$) to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear ($\overline{CLR}$) to Inputs Recognized	0		0		0		ns	
t_{CLP}	Flash Clear ($\overline{CLR}$) Pulse Width	36		44		60		ns	

Figure 5. Read-Flash Clear-Write Cycle


READ CYCLE
CLEAR CYCLE
WRITE CYCLE
t_C
t_FCC
t_C
ADDR
ADDRESS VALID
ADDRESS VALID
ADDRESS VALID
OE
t_CLP
CLR
t_AW
t_CR
t_CX
t_WEW
WE
t_OEZ
t_OEA
t_DS
t_AA
t_DH
DQ*
VALID DATA OUT
VALID DATA IN
MATCH

*AVOID METASTABLE INPUTS

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS}	−1.0V to +7.0V
Operating Temperature T_A (Ambient)	0°C to +70°C
Storage Temperature (Ceramic)	−65°C to +150°C
Storage Temperature (Plastic)	−55°C to +125°C
Power Dissipation	1 Watt
Output Current per Pin	50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage (Referenced to V_{SS})	4.5	5.0	5.5	V	
V_{SS}	Ground	0.0	0.0	0.0	V	
V_{IH}	Input High (Logic 1) voltage, All Inputs (Referenced to V_{SS})	2.2		V_{CC}+0.3	V	
V_{IL}	Input Low (Logic 0) voltage, All Inputs (Referenced to V_{SS})	−0.3		0.8	V	

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Operating Current - Average Power Supply Operating Current		120	mA	1
I_{IL}	Input Leakage Current, Any input	−1	1	µA	5
I_{OL}	Output Leakage Current	−10	10	µA	6
V_{OH}	Output High (Logic 1) voltage Referenced to V_{SS}; I_{OH} = −4mA	2.4		V	
V_{OL}	Output Low (Logic 0) voltage Referenced to V_{SS}; I_{OL} = +8mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS

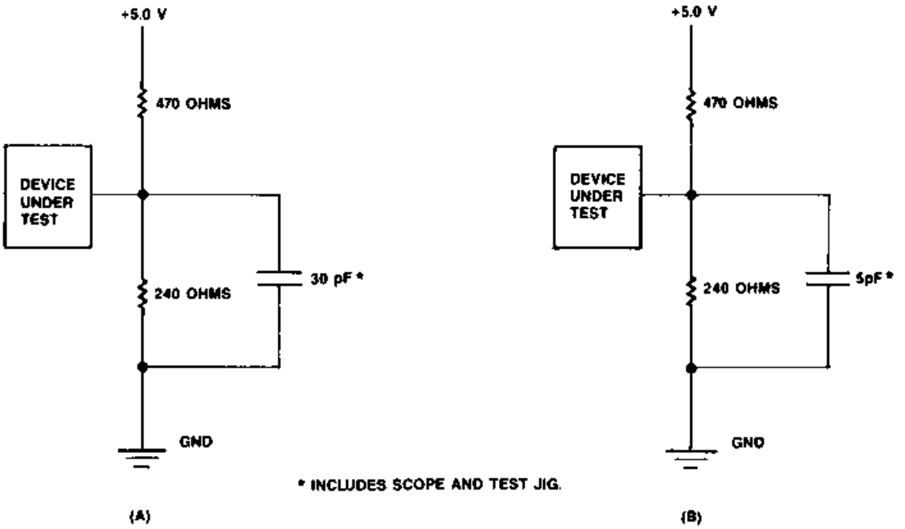
(T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on any Input Pin	4	5	pF	2
C_2	Capacitance on any Output Pin	8	10	pF	2

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS

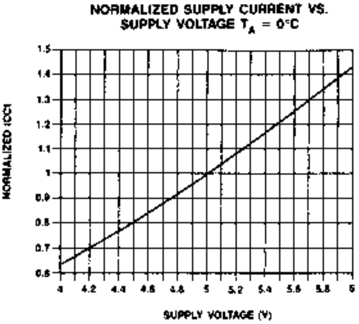

+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
30 pF *
GND
(A)
+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
5pF *
GND
(B)

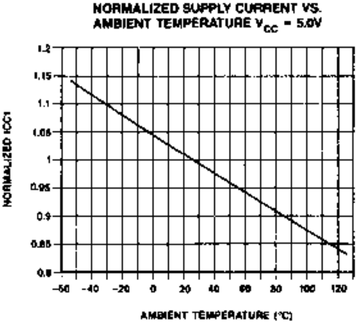
* INCLUDES SCOPE AND TEST JIG.

NOTES

1. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. t cycle = min duty cycle 100%.
2. Capacitances are sampled and not 100% tested.
3. Measured with load shown in Figure 6(A).
4. Measured with load shown in Figure 6(B).
5. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
6. Output leakage current specifications are valid for all DQs such that $0V < V_{OUT} < V_{CC}$. With exception to MATCH which is always enabled.

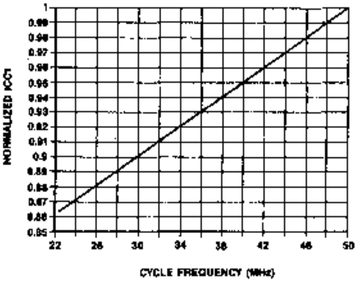
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



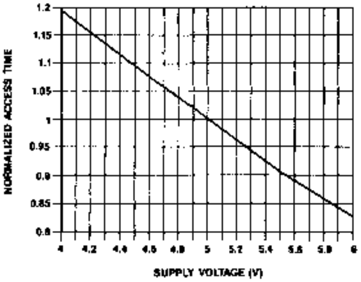


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

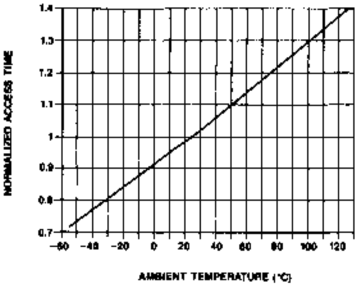
NORMALIZED SUPPLY CURRENT VS. CYCLE TIME V_{CC} = 5.0V T_A = 25°C



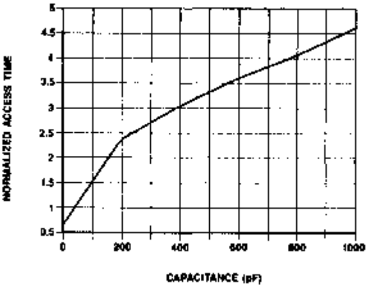
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE T_A = 25°C



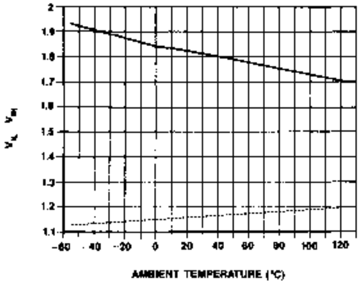
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE V_{CC} = 5.0V



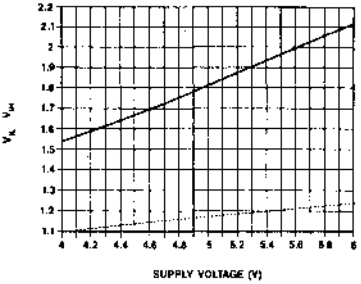
NORMALIZED ACCESS TIME VS. OUTPUT LOADING V_{CC} = 5.0V T_A = 25°C



LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC} = 5.0V

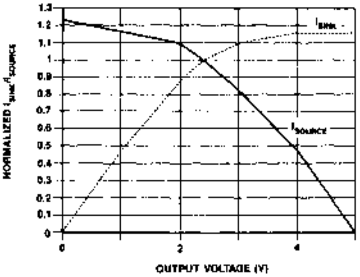


LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A = 25°C

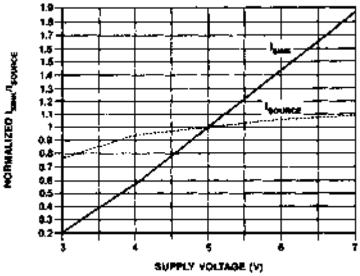


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

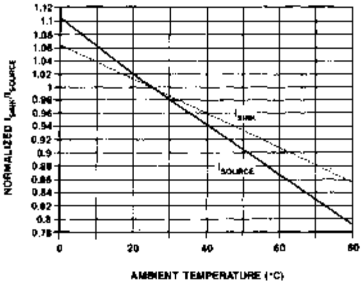
NORMALIZED SOURCE AND SINK CURRENTS VS. OUTPUT VOLTAGE V_{CC} = 5.0V, T_A = 25°C



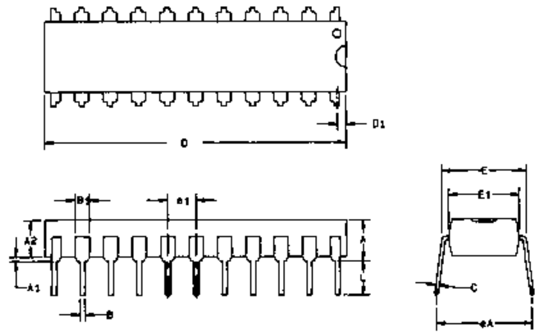
NORMALIZED SOURCE AND SINK CURRENTS VS. SUPPLY VOLTAGE T_A = 25°C



NORMALIZED SOURCE AND SINK CURRENTS VS. AMBIENT TEMPERATURE V_{CC} = 5.0V



22 PIN "N" PACKAGE, PLASTIC DIP

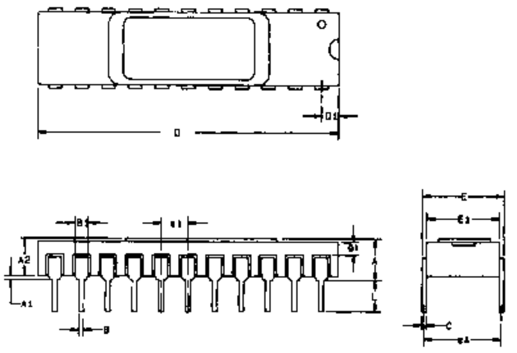


Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	110	
eA	7.62	10.16	.300	.400	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

22 PIN "P" PACKAGE, SIDE BRAZED CERAMIC DIP


D1
D
B1
e1
Q1
A2
A
L
A1
B
E
E1
C
eA

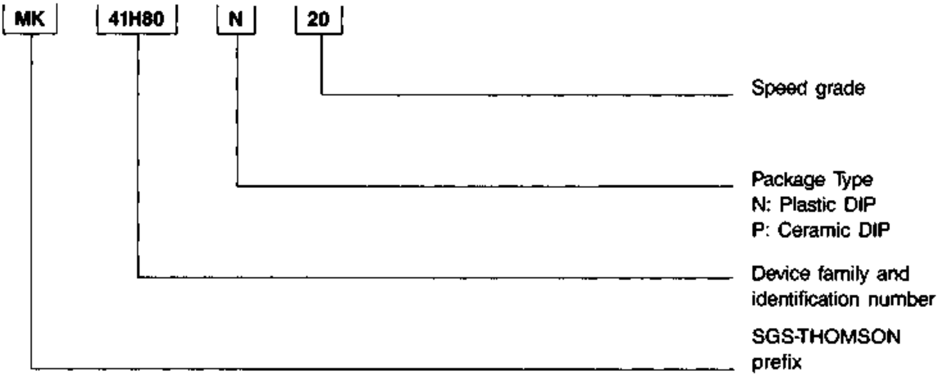
NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	.015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	27.559	28.321	1.085	1.125	
D1	0.889	1.651	.035	.065	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.048	—	.120	—	
Q1	0.127	—	.005	—	

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H80N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H80P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H80P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C


MK
41H80
N
20
Speed grade
Package Type
N: Plastic DIP
P: Ceramic DIP
Device family and
identification number
SGS-THOMSON
prefix

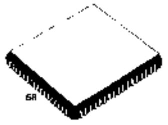
SGS-THOMSON
MICROELECTRONICS

MK4202(Q)-20

2048 × 20 CMOS TAGRAM™

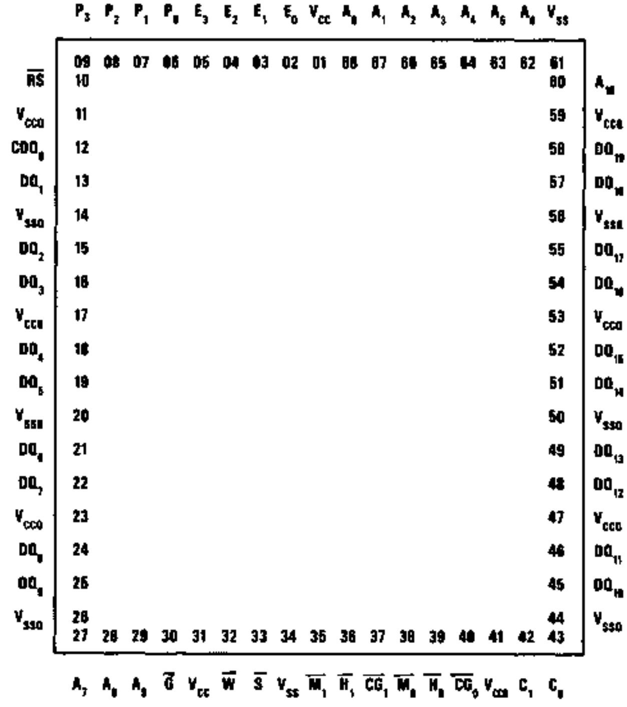
ADVANCED DATA

- 2048 x 20 CMOS SRAM WITH ONBOARD COMPARATOR
- MATCH ACCESS TIME = 20ns (MAX)
- READ ACCESS TIME = 25ns (MAX)
- RESET CYCLE = 25ns (MAX)
- I_{CC} (OUTPUTS DESELECTED) = 225mA (MAX)
- STANDBY = 70mA (MAX)
- FLASH CLEAR VALID BIT FUNCTION
- TARGET APPLICATION:
  68020-25, 68030-33 AND 80386 CACHE



Q
PLCC68
(Plastic Chip Carrier)

FIGURE 1. PINOUT FOR 68 PIN PLCC PACKAGE (PRELIMINARY)


P_3
P_2
P_1
P_0
E_3
E_2
E_1
E_0
V_{CC}
A_0
A_1
A_2
A_3
A_4
A_5
A_6
V_{SS}
09
08
07
06
05
04
03
02
01
68
67
66
65
64
63
62
61
$\overline{RS}$ 10
V_{CCQ} 11
CDQ_0 12
DQ_1 13
V_{SSQ} 14
DQ_2 15
DQ_3 16
V_{CCQ} 17
DQ_4 18
DQ_5 19
V_{SSQ} 20
DQ_6 21
DQ_7 22
V_{CCQ} 23
DQ_8 24
DQ_9 25
V_{SSQ} 26
60 A_{10}
59 V_{CCQ}
58 DQ_{19}
57 DQ_{18}
56 V_{SSQ}
55 DQ_{17}
54 DQ_{16}
53 V_{CCQ}
52 DQ_{15}
51 DQ_{14}
50 V_{SSQ}
49 DQ_{13}
48 DQ_{12}
47 V_{CCQ}
46 DQ_{11}
45 DQ_{10}
44 V_{SSQ}
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
A_7
A_8
A_9
$\overline{G}$
V_{CC}
$\overline{W}$
$\overline{S}$
V_{SS}
$\overline{M_1}$
$\overline{H_1}$
$\overline{CG_1}$
$\overline{M_0}$
$\overline{H_0}$
$\overline{CG_0}$
V_{CCQ}
C_1
C_0

PIN NAMES

V_{CC}, V_{SS}	+5 Volt Supply, Ground
V_{CCQ}, V_{SSQ}	+5 Volt Output Supply, Output Ground
A_0-A_{10}	Index Address Input
CDQ_0	Clearable Tag Data I/O
DQ_1-DQ_{19}	Tag Data I/O
E_0-E_3	Chip Enable (Programmable Active Low or High)
P_0-P_3	Chip Enable Program Inputs
$\overline{RS}$	Reset Input (Active Low)
$\overline{S}$	Chip Select Input (Active Low)
$\overline{W}$	Write Enable (Active Low)
$\overline{G}$	Data Output Enable (Active Low)
C_0	Compare 0 Output (3-State) Hit = High, Miss = Low
C_1	Compare 1 Output (3-State) Hit = High, Miss = Low
$\overline{H_0}$	Force Hit 0 Input (Active Low)
$\overline{H_1}$	Force Hit 1 Input (Active Low)
$\overline{M_0}$	Force Miss 0 Input (Active Low)
$\overline{M_1}$	Force Miss 1 Input (Active Low)
$\overline{CG_0}$	Compare 0 Output Enable (Active Low)
$\overline{CG_1}$	Compare 1 Output Enable (Active Low)

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

TRUTH TABLE

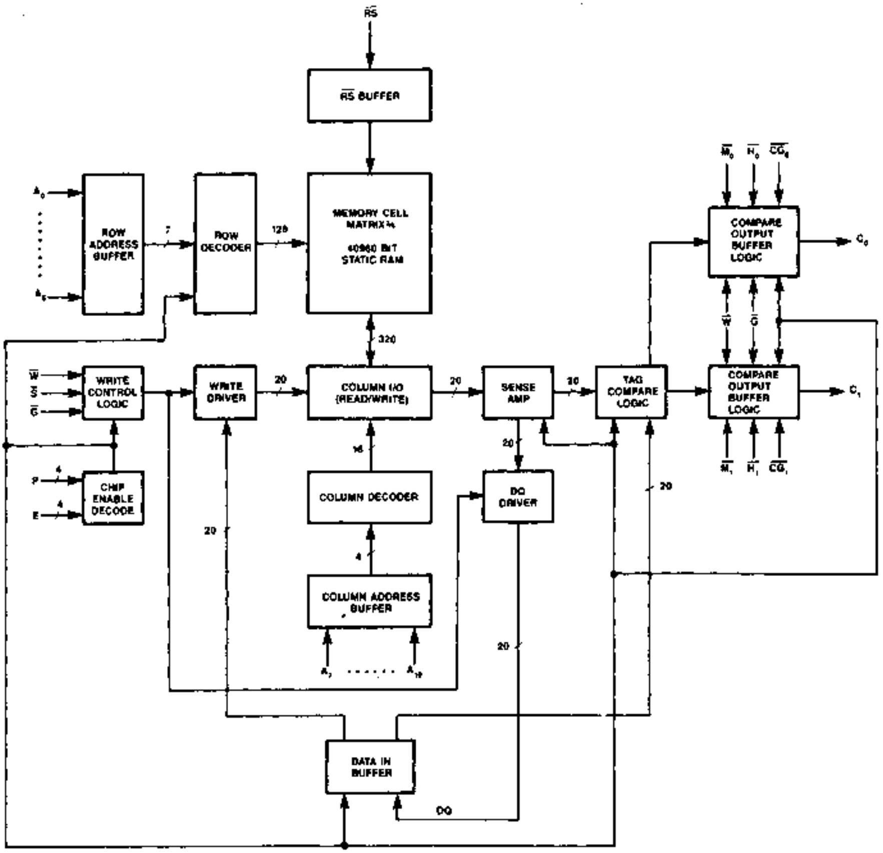
$\overline{RS}$	$\overline{S}$	E	$\overline{W}$	$\overline{G}$	$\overline{M_X}$	$\overline{H_X}$	$\overline{CG_X}$	MODE	C_X	DQ	NOTES
Hi	—	X	—	—	Lo	X	X	Force Miss	Low	—	1
Hi	—	X	—	—	Hi	Lo	X	Force Hit	High	—	1
Hi	—	X	—	—	Hi	Hi	Hi	Comp Disable	Hi-Z	—	1
Hi	X	F	X	X	Hi	Hi	X	Standby	Hi-Z	Hi-Z	
Hi	X	T	Hi	Hi	Hi	Hi	Hi	Compare	Hi-Z	D in	
Hi	X	T	Hi	Hi	Hi	Hi	Lo	Compare	Hi or Lo	D in	
Hi	Hi	T	Lo	X	Hi	Hi	Lo	Hit	High	Hi-Z	
Hi	Hi	T	X	Lo	Hi	Hi	Lo	Hit	High	Hi-Z	
Hi	Lo	T	Lo	X	Hi	Hi	Lo	Write	High	D in	
Hi	Lo	T	Hi	Lo	Hi	Hi	Lo	Read	High	D Out	
Lo	Hi	X	X	X	—	—	—	Reset	—	Hi-Z	
Lo	X	F	X	X	—	—	—	Reset	—	Hi-Z	
Lo	X	X	Hi	Hi	—	—	—	Reset	—	Hi-Z	
Lo	X	X	Hi	Lo	—	—	—	Reset	—	Lo-Z	
Lo	Lo	T	Lo	X	—	—	—	Not Allowed	—	Hi-Z	2
Lo	X	T	Hi	Hi	Hi	Hi	Lo	Reset	Lo	D in	3

Key:
X = Don't Care
$\overline{H_X}$ = $\overline{H_0}$ or $\overline{H_1}$
$\overline{M_X}$ = $\overline{M_0}$ or $\overline{M_1}$
$\overline{CG_X}$ = $\overline{CG_0}$ or $\overline{CG_1}$
F = (False) E_0-E_3 pattern DOES NOT match P_0-P_3 pattern.
T = (True) E_0-E_3 pattern DOES match P_0-P_3 pattern.
— = Not related to identified mode of operation.

NOTES

1. Force hit/miss operations independent of other RAM operations.
2. May disrupt Reset, will not damage device.
3. Reset will force C_X low during a valid compare when CDQ_0 is D in = Hi.

FIGURE 2. MK4202 BLOCK DIAGRAM


$\overline{RS}$
$\overline{RS}$ BUFFER
A_0
A_6
ROW ADDRESS BUFFER
7
ROW DECODER
128
MEMORY CELL MATRIX ¼
40960 BIT STATIC RAM
320
$\overline{W}$
$\overline{S}$
$\overline{G}$
WRITE CONTROL LOGIC
WRITE DRIVER
20
COLUMN I/O (READ/WRITE)
20
SENSE AMP
20
TAG COMPARE LOGIC
P
4
E
4
CHIP ENABLE DECODE
16
COLUMN DECODER
4
COLUMN ADDRESS BUFFER
A_7
A_{10}
20
20
DQ DRIVER
20
20
DATA IN BUFFER
DQ
$\overline{M_0}$
$\overline{H_0}$
$\overline{CG_0}$
COMPARE OUTPUT BUFFER LOGIC
C_0
$\overline{W}$
$\overline{G}$
COMPARE OUTPUT BUFFER LOGIC
C_1
$\overline{M_1}$
$\overline{H_1}$
$\overline{CG_1}$

DEVICE DESCRIPTION AND FEATURES

The MK4202 is designed to be connected DIRECTLY to a high performance 32 bit microprocessor, allowing the elimination of the logic delays associated with collecting HIT or Miss outputs into a subsequent gate or the RC delays associated with wired-OR open collector match outputs.

The MK4202 TAGRAM has four major features that allow direct connection:

1. Wide enough for almost any TAGRAM application without requiring multiple chip width expansion and the delays that would result.

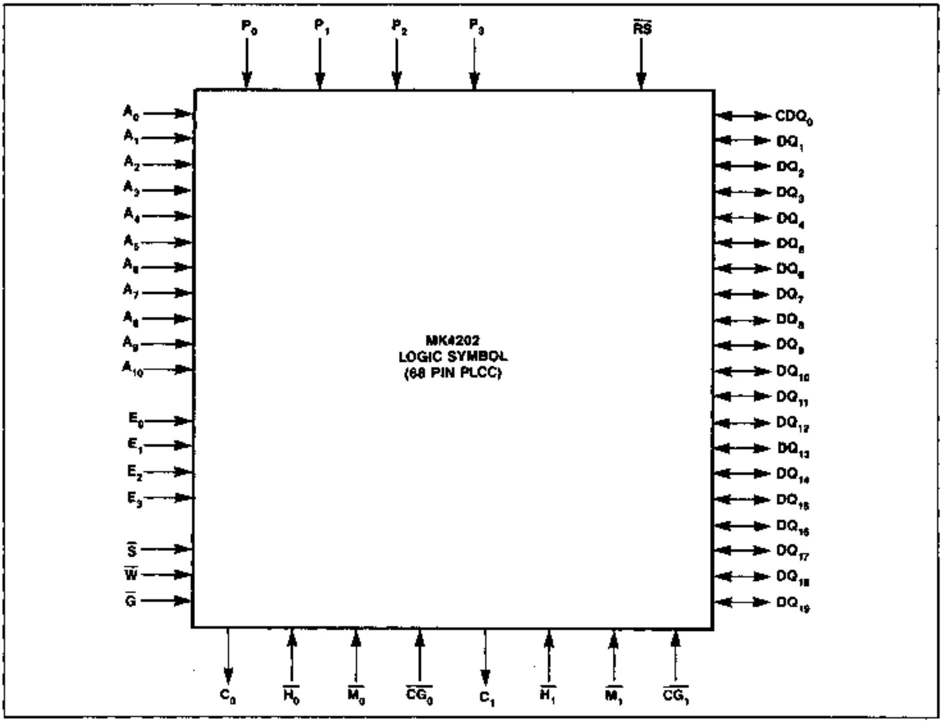
2. Four (4) programmable CHIP ENABLE inputs, allowing DEPTH EXPANSION without any of the attendant chip enable decode delays that would otherwise be required.

   P_0-P_3 should be tied directly to V_{CC} or V_{SS}, or through pull-up or pull-down resistors. The MK4202 is selected when E_0-E_3 equals P_0-P_3 in a binary match.
   (Example: E_0-E_1 = 0110, P_0-P_3 = 0110.)

3. 3-STATE COMPARE OUTPUTS, allowing all Compare outputs to be bused together so the Address-to-Compare access time for a depth expanded application is identical to that of a single device. The Programmable Chip Enables prevent bus contention by assuring that only one TAGRAM at a time drives each Compare bus when in Compare mode.

4. DUAL COMPARE OUTPUTS (C_0 and C_1) and FORCED HIT ($\overline{H_0}$ and $\overline{H_1}$) and FORCED MISS ($\overline{M_0}$ and $\overline{M_1}$) inputs for each. The arrangement allows direct connection of the TAGRAM to two separate processor inputs (such as BERR and HALT on the 68030), and connection of all signals that would otherwise have been connected to those processor inputs to be passed THROUGH the TAGRAM; eliminating the need for a subsequent gate to collect the COMPARE output and other BERR or HALT signal sources to the processor.

FIGURE 3. DEVICE LOGIC SYMBOL



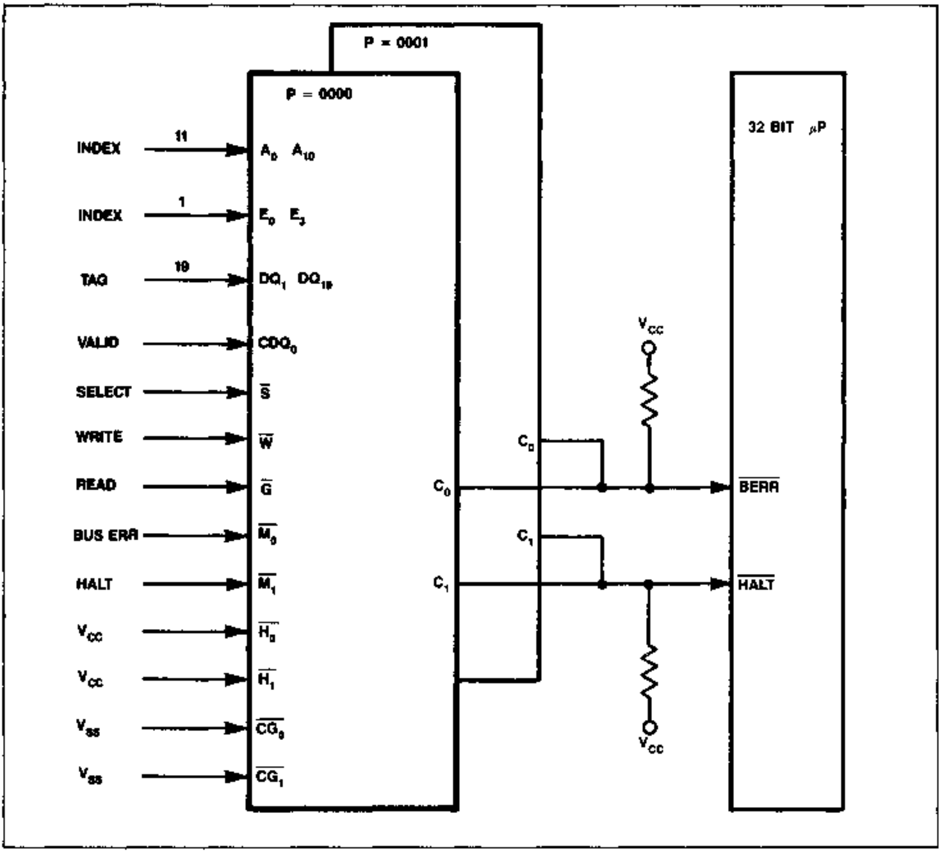
The net effect is that the Address-to-Compare access time demonstrated by the MK4202 is all of the delay the user must consider. The alternative approach, using narrow TAGRAMs with open collector outputs or narrow TAGRAMs with 2-state outputs and a 10ns programmable logic device, requires that the narrow TAGRAMs demonstrate a 10ns Address-to-Compare access time to yield the same performance in a user's system that the MK4202 provides.

POWER DISTRIBUTION

The MK4202, being a 20 output device, obviously requires the use of good power bussing techniques. MK4202 has been designed in such a way as to allow the user to minimize the effects of switching transients on overall circuit operation. Of particular interest is the separate bussing of the V_{CC} and V_{SS} lines to the output drivers. The advantage provided by these separate power pins,, designated V_{CCQ} and V_{SSQ}, is that voltage sags and ground bumps seen on these pins are not reflected into the other portions of the chip, particularly the input structures. As a result, switching noise in the supply has much less effect on input levels, providing the user with more noise margin than would otherwise be available.

Of course V_{SS} and V_{SSQ} must always be at the same DC potential. V_{CC} and V_{CCQ} must match as well. Differences between them due to AC effects are expected, but must be minimized through the use of adequate bussing and bypassing. All specifications and testing are done with $V_{SS} = V_{SSQ} \pm$ 10mV RMS, $V_{CC} = V_{CCQ} \pm$ 10mV RMS with instantaneous peak differences not exceeding 50mV.

FIGURE 4. APPLICATION BLOCK SCHEMATIC



READ MODE

The MK4202 is in the Read mode whenever $\overline{W}$ is HIGH, and $\overline{G}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied. The 11 address inputs (A_0-A_{10}) define a unique index address giving access to 20 of 40,960 bits of data in the static memory array. Valid data will be present at the 20 output pins within t_{AVQV} of the last stable address provided Chip Enable, Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) access times have been met. If Chip Enable, $\overline{S}$, or $\overline{G}$ access times are not met, data access will be measured from the latter falling edge or limiting parameter (t_{EVQV}, t_{SLQV}, or t_{GLQV}). The state of the tag data I/O pins is controlled by the (E_0-E_3), $\overline{S}$, $\overline{G}$, and $\overline{W}$ input pins. The data lines may be indeterminate at t_{EVQX}, t_{SLQX}, or t_{GLQX}, but will always have valid data at t_{AVQV}.

READ CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVAV}	t_C	Cycle Time	25		ns	
t_{AVQV}	t_{AA}	Address Access Time		25	ns	
t_{AXQX}	t_{AOH}	Address Output Hold Time	5		ns	
t_{EVQV}	t_{EA}	Chip Enable Access Time		25	ns	
t_{EXQX}	t_{EOH}	Chip Enable Output Hold Time	4		ns	
t_{EVQX}	t_{ELZ}	Chip Enable TRUE to Low-Z	4		ns	
t_{EXQZ}	t_{EHZ}	Chip Enable FALSE to High-Z		8	ns	
t_{SLQV}	t_{SA}	Chip Select Access Time		10	ns	
t_{SHQX}	t_{SOH}	Chip Select Output Hold Time	2		ns	
t_{SLQX}	t_{SLZ}	Chip Select to Low-Z	3		ns	
t_{SHQZ}	t_{SHZ}	Chip Select to High-Z		4	ns	
t_{GLQV}	t_{GA}	Output Enable Access Time		10	ns	
t_{GHQX}	t_{GOH}	Output Enable Output Hold Time	2		ns	
t_{GLQX}	t_{GLZ}	Output Enable to Low-Z	2		ns	
t_{GHQZ}	t_{GHZ}	Output Enable to High-Z		5	ns	

WRITE MODE

TheMK4202 is in the Write mode whenever $\overline{W}$ is LOW provided Chip Select ($\overline{S}$) is LOW and a true Chip Enable pattern (E_0-E_3) is applied ($\overline{G}$ may be in either logic state). Addresses must be held valid throughout a write cycle, with either $\overline{W}$ or $\overline{S}$ inactive HIGH during address transitions. $\overline{W}$ may fall with stable address, but must remain valid for t_{WLWH}. Since the write begins with the concurrence of $\overline{W}$ and $\overline{S}$, should $\overline{W}$ become active first, then t_{SLSH} must be satisfied. Either $\overline{W}$ or $\overline{S}$ can terminate the write cycle, therefore t_{DVWH} or t_{DVSH} must be satisfied before the earlier rising edge, and t_{WHDX} or t_{SHDX} after the earlier rising edge. If the outputs are active with $\overline{G}$ and $\overline{S}$ asserted LOW and with true Chip Enable, then $\overline{W}$ will return the outputs to high impedance within t_{WLHZ} of its falling edge.

WRITE CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVAV}	t_C	Cycle Time	25		ns	
t_{AVWL}	t_{AS}	Address Set-up Time to $\overline{W}$ LOW	0		ns	
t_{WHAX}	t_{AH}	Address Hold Time from $\overline{W}$ HIGH	0		ns	
t_{AVSL}	t_{AS}	Address Set-up Time to $\overline{S}$ LOW	0		ns	
t_{SHAX}	t_{AH}	Address Hold Time from $\overline{S}$ HIGH	0		ns	
t_{EVWL}	t_{ES}	Chip Enable Set-up Time to $\overline{W}$ LOW	5		ns	
t_{WHEX}	t_{EH}	Chip Enable Hold Time from $\overline{W}$ HIGH	0		ns	
t_{EVSL}	t_{ES}	Chip Enable Set-up Time to $\overline{S}$ LOW	5		ns	
t_{SHEX}	t_{EH}	Chip Enable Hold Time to $\overline{S}$ HIGH	0		ns	
t_{WLWH}	t_{WW}	Write Pulse Width	15		ns	
t_{SLSH}	t_{SW}	Chip Select Pulse Width	16		ns	
t_{DVWH}	t_{DS}	Data Set-up Time to $\overline{W}$ HIGH	10		ns	
t_{WHDX}	t_{DH}	Data Hold Time from $\overline{W}$ HIGH	0		ns	
t_{DVSH}	t_{DS}	Data Set-up Time to $\overline{S}$ HIGH	10		ns	
t_{SHDX}	t_{DH}	Data Hold Time from $\overline{S}$ HIGH	0		ns	
t_{WLQZ}	t_{WZ}	Outputs Hi-Z from $\overline{W}$ LOW		8	ns	
t_{WHQX}	t_{WL}	Outputs Low-Z from $\overline{W}$ HIGH	5		ns	

COMPARE MODE

The MK4202 is in the Compare mode whenever $\overline{W}$ and $\overline{G}$ are HIGH provided a true Chip Enable pattern (E_0-E_3) is applied. Chip Select ($\overline{S}$) is regarded as a don't care since the user is not concerned with the data outputs, but only with the Compare (C_X) outputs. $\overline{M_X}$ and $\overline{H_X}$ must be HIGH, and CG_X active LOW to enable the Compare outputs for a valid compare hit or miss.

The 11 index address inputs (A_0-A_{10}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_1-DQ_{19} and CDQ_0) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (C_X = HIGH). If at least one bit is not equal, then a miss occurs (C_X = LOW).

The Compare output will be valid t_{AVCV} from stable address, or t_{DVCV} from valid tag data provided Chip Enable is true, and $\overline{CG_X}$ is active LOW. Should the address be stable with valid tag data, and Chip Enable false, then compare access will be within t_{EVCV} from true Chip Enable. When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), C_X will be valid t_{WHCV} or t_{GHCV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively. Finally, when gating the C_X output in the compare mode with $\overline{CG_X}$, the compare output will be valid $t_{CGL\text{-}CV}$ from the falling edge of $\overline{CG_X}$.

COMPARE CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{AVCV}	t_{ACA}	Address Compare Access Time		20	ns	
t_{AXCX}	t_{ACOH}	Address Compare Output Hold Time	5		ns	
t_{DVCV}	t_{DCA}	Tag Data Compare Access Time		16	ns	
t_{DXCX}	t_{DCH}	Tag Data Compare Hold Time	2		ns	
t_{WLCH}	t_{WCH}	$\overline{W}$ LOW to Compare HIGH		10	ns	
t_{WHCX}	t_{WCOH}	$\overline{W}$ Compare Output Hold Time	3		ns	
t_{WLCX}	t_{WCLZ}	$\overline{W}$ to Compare Low-Z	3		ns	
t_{WHCV}	t_{WCV}	$\overline{W}$ to Compare Valid		8	ns	
t_{GLCH}	t_{GCH}	$\overline{G}$ LOW to Compare HIGH		10	ns	
t_{GHCX}	t_{CGOH}	$\overline{G}$ Compare Output Hold Time	3		ns	
t_{GLCX}	t_{GCLZ}	$\overline{G}$ to Compare Low-Z	3		ns	
t_{GHCV}	t_{GCV}	$\overline{G}$ to Compare Valid		8	ns	
t_{EVCV}	t_{ECA}	E True to Compare Access Time		20	ns	
t_{EXCX}	t_{ECOH}	E False Compare Hold Time	4		ns	
t_{EVCX}	t_{ECLZ}	E True to Compare Low-Z	4		ns	
t_{EXCZ}	t_{ECHZ}	E False to Compare High-Z		8	ns	
$t_{CGL\text{-}CV}$	t_{CGA}	$\overline{CG_X}$ to Compare Access Time		8	ns	
$t_{CGH\text{-}CX}$	t_{CGOH}	$\overline{CG_X}$ Compare Hold Time	2		ns	
$t_{CGL\text{-}CX}$	t_{CGLZ}	$\overline{CG_X}$ LOW to Compare Low-Z	2		ns	
$t_{CGH\text{-}CZ}$	t_{CGHZ}	$\overline{CG_X}$ HIGH to Compare High-Z		8	ns	

NOTE: E = Enable Inputs (E_0-E_3).

RESET MODE

The MK4202 allows an asynchronous reset whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits in CDQ_0 (2048 bits) to a logic zero. This output can be used as a valid tag bit to ensure a valid compare miss or hit condition. It should be noted that a valid write cycle is not allowed during a reset cycle ($\overline{W}$ = LOW, $\overline{S}$ = LOW, $\overline{RS}$ = LOW, and Chip Enable is true). The state of the data outputs is determined by the input control logic pins: Chip Enable, $\overline{S}$, $\overline{G}$, and $\overline{W}$ (see truth table). Should a reset occur during a valid compare cycle, and the CDQ_0 valid tag bit is set to a logic (1), then C_X will go LOW at $t_{RSL\text{-}CL}$ from the falling edge of $\overline{RS}$.

RESET CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
$t_{RLSL\text{-}AV}$	t_{RSC}	Reset Cycle Time	25		ns	
$t_{RSL\text{-}RSH}$	t_{RSW}	Reset Pulse Width	25		ns	
$t_{RSL\text{-}CL}$	t_{RSCL}	$\overline{RS}$ LOW to Compare Output LOW		25	ns	
$t_{RSH\text{-}AV}$	t_{RSR}	Address Recovery Time	0		ns	
$t_{RSH\text{-}EV}$	t_{RSR}	Chip Enable Recovery Time	0		ns	

FORCE HIT AND FORCE MISS

The MK4202 can force either a miss or hit condition on the C_X output by asserting $\overline{M_X}$ or $\overline{H_X}$ LOW. A Force Miss overrides a Force Hit condition and is not dependent upon Compare Output Enable ($\overline{CG_X}$) (see truth table). The C_X output will go HIGH within t_{HLCH} from the falling edge of $\overline{H_X}$, or C_X will go LOW within t_{MLCL} from the falling edge of $\overline{M_X}$. All $\overline{M_X}$ and $\overline{H_X}$ inputs must be HIGH during a valid compare cycle.

FORCE HIT OR MISS CYCLE TIMING

Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ± 10%)

STD SYM	ALT SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{HLCH}	t_{HA}	$\overline{H_X}$ to Force Hit Access Time		8	ns	
t_{HHCZ}	t_{HHZ}	$\overline{H_X}$ to Compare High-Z		5	ns	
$t_{HL\text{-}CGX}$	t_{HS}	Force Hit to $\overline{CG_X}$ Don't Care	2		ns	
$t_{HH\text{-}CGH}$	t_{HR}	Force Hit to $\overline{CG_X}$ Recognized	2		ns	
t_{MLCL}	t_{MA}	$\overline{M_X}$ to Force Miss Access Time		8	ns	
t_{MHCZ}	t_{MHZ}	$\overline{M_X}$ to Compare to High-Z		5	ns	
$t_{ML\text{-}CGX}$	t_{MS}	Force Miss to $\overline{CG_X}$ Don't Care		2	ns	
$t_{MH\text{-}CGH}$	t_{MR}	Force Miss to $\overline{CG_X}$ Recognized	2		ns	
t_{MLHX}	t_{MHS}	Force Miss to $\overline{H_X}$ Don't Care	2		ns	
t_{MHHH}	t_{MHR}	Force Miss To $\overline{H_X}$ Recognized	2		ns	

FIGURE 5. $\overline{W}$ WRITE CYCLE

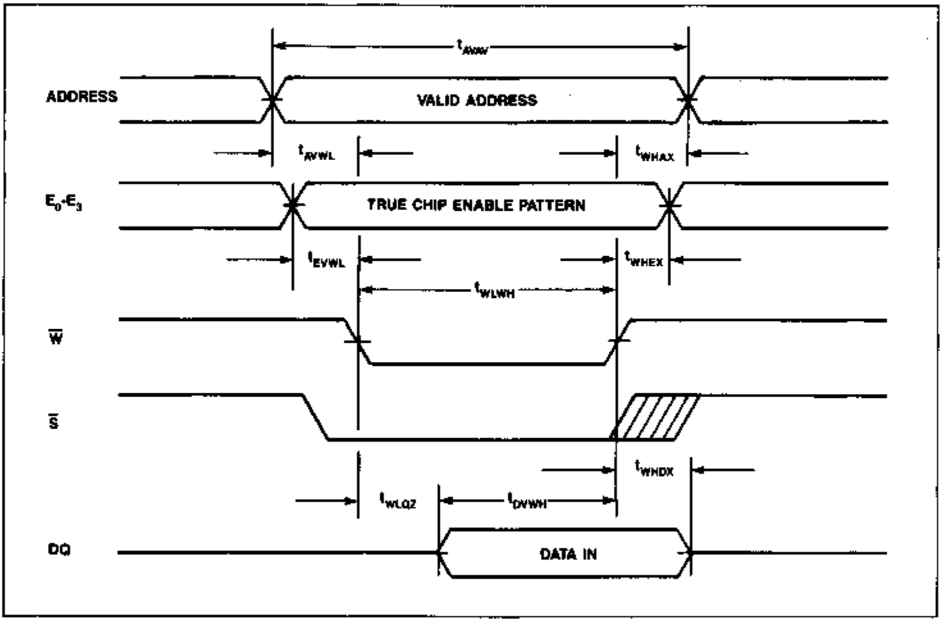

t_{AVAV}
ADDRESS
VALID ADDRESS
t_{AVWL}
t_{WHAX}
E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVWL}
t_{WHEX}
t_{WLWH}
$\overline{W}$
$\overline{S}$
t_{WHDX}
t_{WLQZ}
t_{DVWH}
DQ
DATA IN

FIGURE 6. $\overline{S}$ WRITE CYCLE

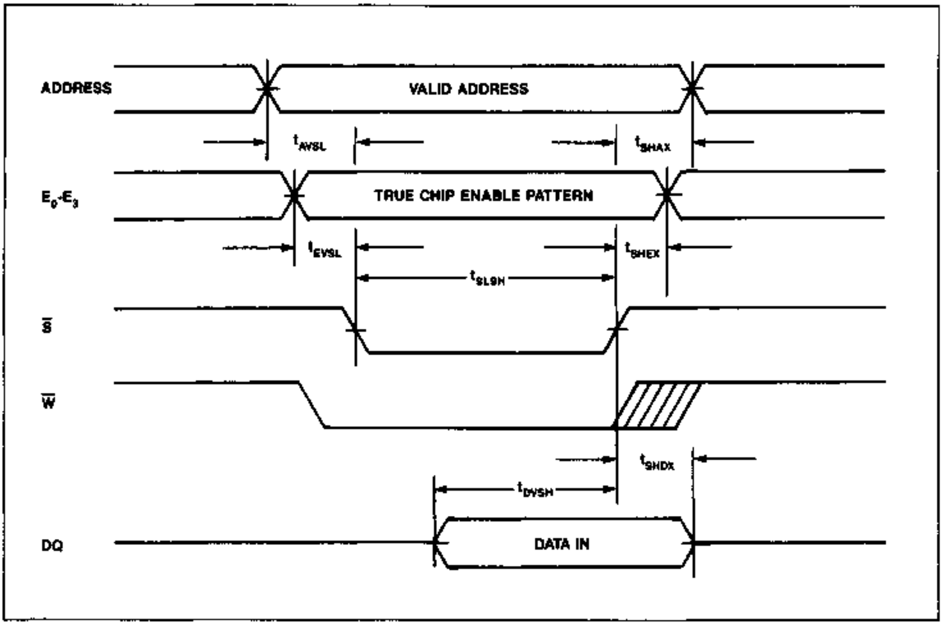

ADDRESS
VALID ADDRESS
t_{AVSL}
t_{SHAX}
E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVSL}
t_{SHEX}
t_{SLSH}
$\overline{S}$
$\overline{W}$
t_{SHDX}
t_{DVSH}
DQ
DATA IN

FIGURE 7. READ CYCLE

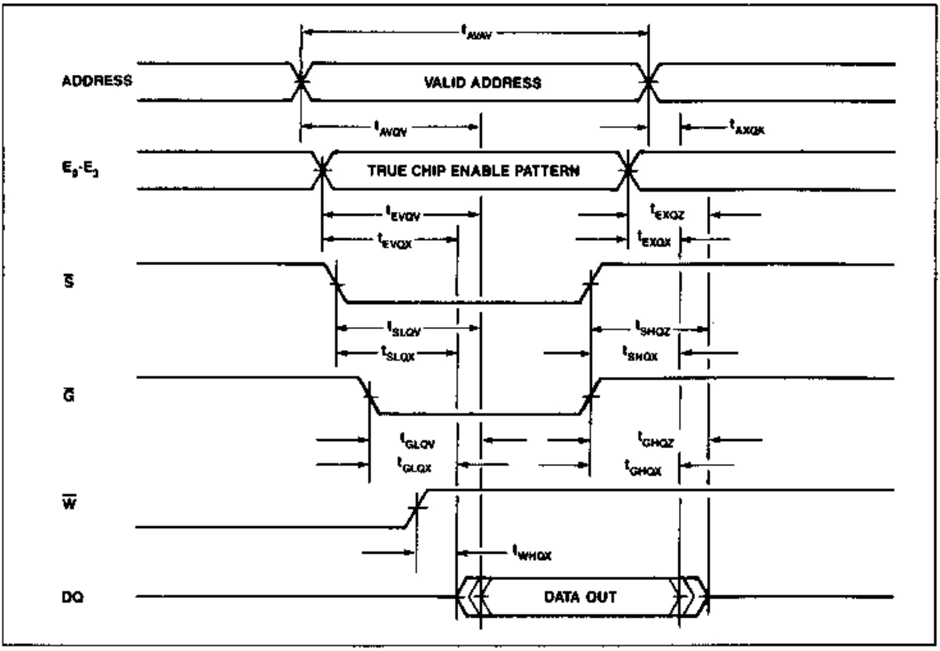

t_{AVAV}
ADDRESS
VALID ADDRESS
t_{AVQV}
t_{AXQX}
E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVQV}
t_{EVQX}
t_{EXQZ}
t_{EXQX}
$\overline{S}$
t_{SLQV}
t_{SLQX}
t_{SHQZ}
t_{SHQX}
$\overline{G}$
t_{GLQV}
t_{GLQX}
t_{GHQZ}
t_{GHQX}
$\overline{W}$
t_{WHQX}
DQ
DATA OUT

FIGURE 8. ADDRESS READ CYCLE

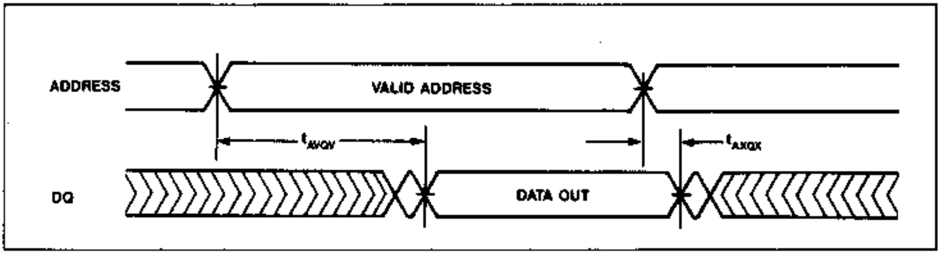

ADDRESS
VALID ADDRESS
t_{AVQV}
t_{AXQX}
DQ
DATA OUT

FIGURE 9. CHIP ENABLE READ CYCLE

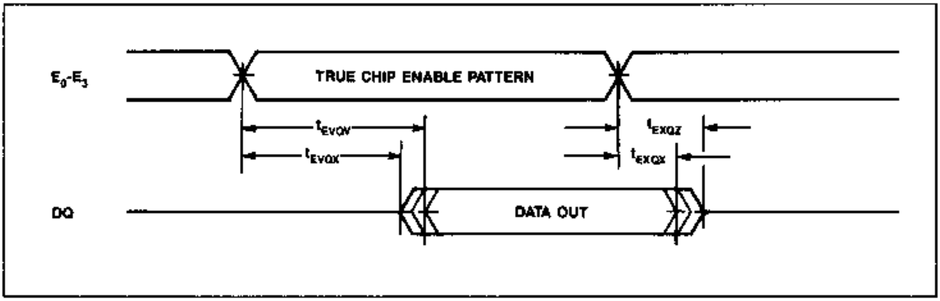

E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVQV}
t_{EVQX}
t_{EXQZ}
t_{EXQX}
DQ
DATA OUT

FIGURE 10. CHIP SELECT READ CYCLE

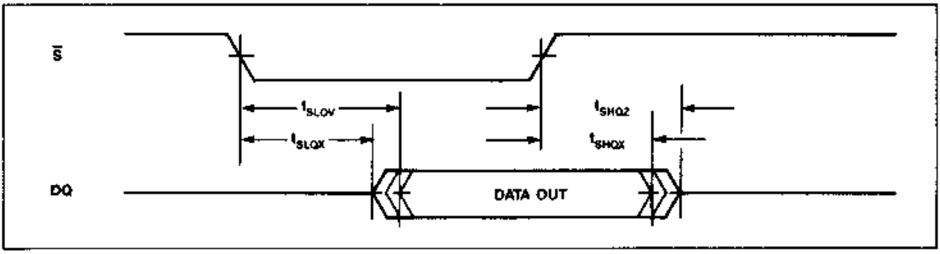

S̄
t_{SLQV}
t_{SLQX}
t_{SHQZ}
t_{SHQX}
DQ
DATA OUT

FIGURE 11. OUTPUT ENABLE READ CYCLE

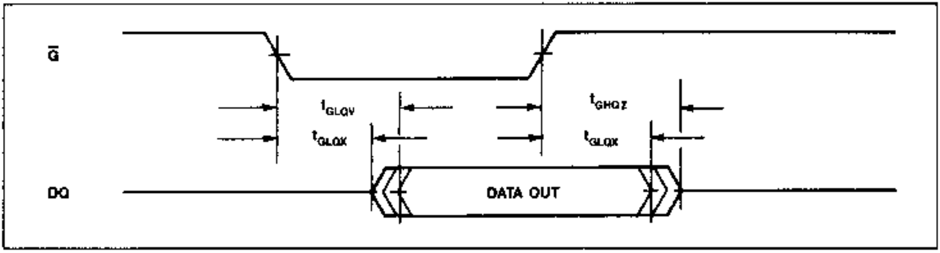

Ḡ
t_{GLQV}
t_{GLQX}
t_{GHQZ}
t_{GLQX}
DQ
DATA OUT

FIGURE 12. FORCE HIT AND FORCE MISS

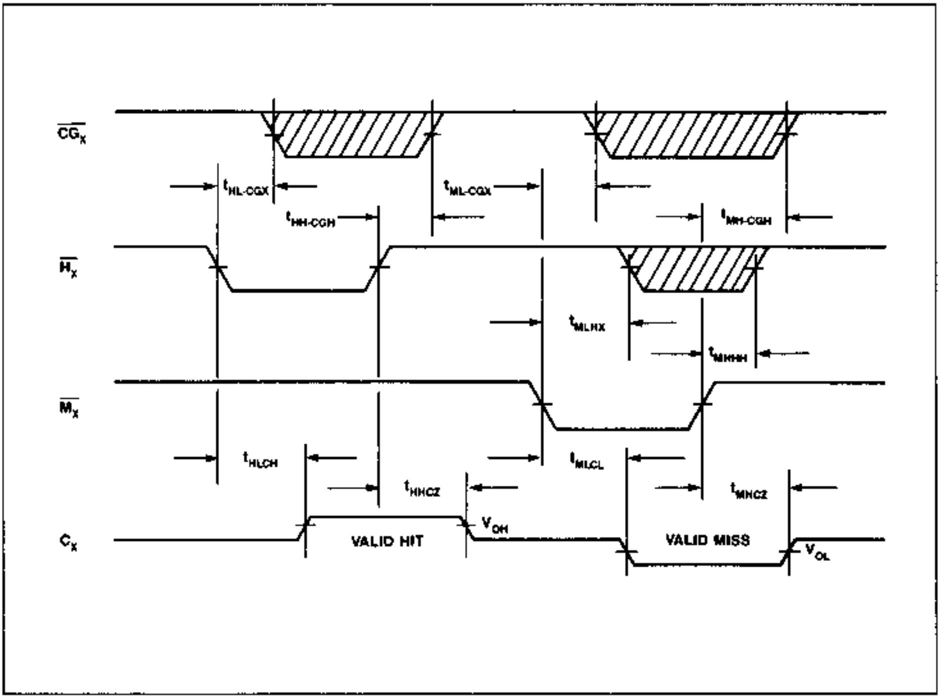
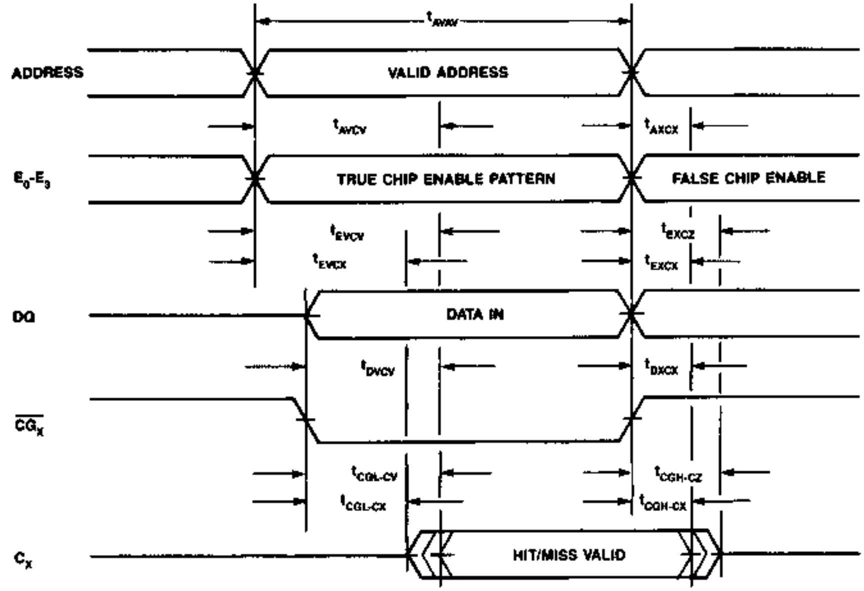
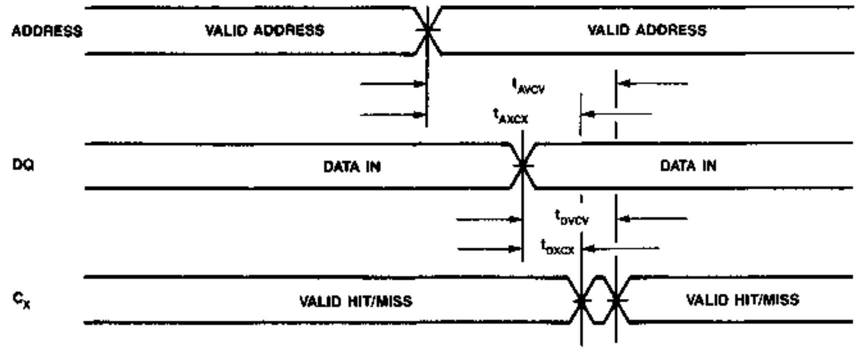

$\overline{CG_X}$
t_{HL-CGX}
t_{ML-CGX}
t_{HH-CGH}
t_{MH-CGH}
$\overline{H_X}$
t_{MLHX}
t_{MHHH}
$\overline{M_X}$
t_{HLCH}
t_{MLCL}
t_{HHCZ}
t_{MHCZ}
C_X
VALID HIT
V_{OH}
VALID MISS
V_{OL}

FIGURE 13. SUMMARY COMPARE CYCLE


t_{AVAV}
ADDRESS
VALID ADDRESS
t_{AVCV}
t_{AXCX}
E_0-E_3
TRUE CHIP ENABLE PATTERN
FALSE CHIP ENABLE
t_{EVCV}
t_{EVCX}
t_{EXCZ}
t_{EXCX}
DQ
DATA IN
t_{DVCV}
t_{DXCX}
$\overline{CG_X}$
t_{CGL-CV}
t_{CGL-CX}
t_{CGH-CZ}
t_{CGH-CX}
C_X
HIT/MISS VALID

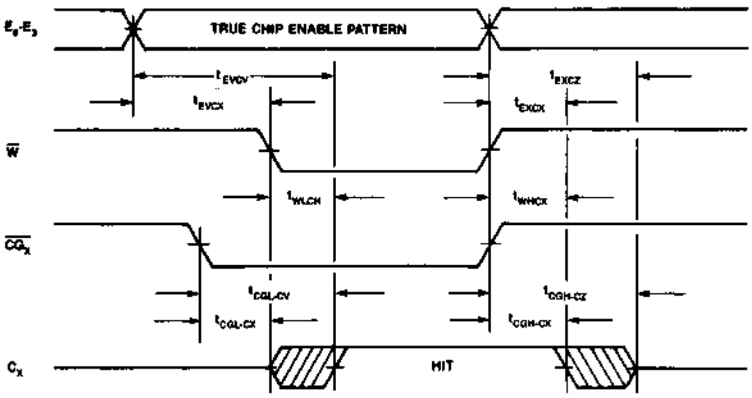
NOTE:
$\overline{W}$ and $\overline{G}$ are both assumed to be HIGH.
$\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 14. COMPARE CYCLE


ADDRESS
VALID ADDRESS
VALID ADDRESS
t_{AVCV}
t_{AXCX}
DQ
DATA IN
DATA IN
t_{DVCV}
t_{DXCX}
C_X
VALID HIT/MISS
VALID HIT/MISS

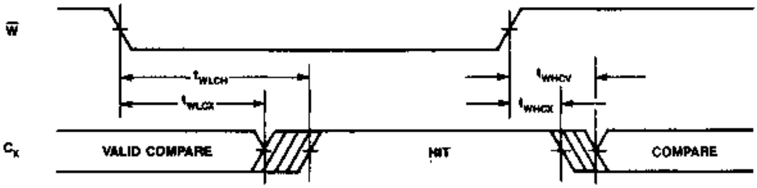
NOTE:
$\overline{W}$ and $\overline{G}$ are both HIGH, $\overline{CG_X}$ is LOW, and a true Chip Enable pattern is present. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH.

FIGURE 15. LATE WRITE - HIT CYCLE


E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVCV}
t_{EVCX}
t_{EXCZ}
t_{EXCX}
$\overline{W}$
t_{WLCH}
t_{WHCX}
$\overline{CG}_X$
$t_{CGL\text{-}CV}$
$t_{CGL\text{-}CX}$
$t_{CGH\text{-}CZ}$
$t_{CGH\text{-}CX}$
C_X
HIT

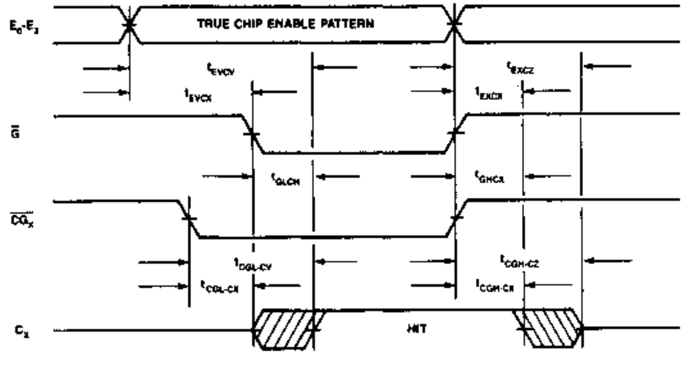
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present. $\overline{H}_X$ and $\overline{M}_X$ are both assumed to be HIGH.

FIGURE 16. COMPARE - WRITE HIT - COMPARE CYCLE


$\overline{W}$
t_{WLCH}
t_{WLCX}
t_{WHCV}
t_{WHCX}
C_X
VALID COMPARE
HIT
COMPARE

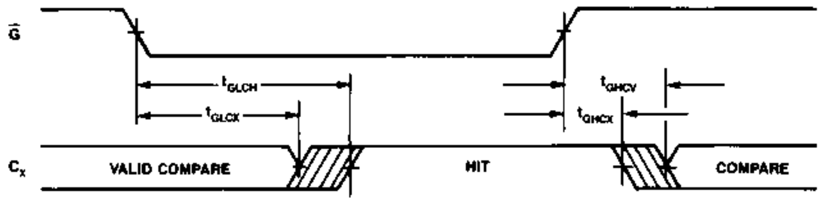
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present. $\overline{H}_X$ and $\overline{M}_X$ are both assumed to be HIGH, with $\overline{CG}_X$ LOW.

FIGURE 17. LATE READ - HIT CYCLE


E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVCV}
t_{EVCX}
t_{EXCZ}
t_{EXCX}
$\overline{G}$
t_{GLCH}
t_{GHCX}
$\overline{CG}_X$
$t_{CGL\text{-}CV}$
$t_{CGL\text{-}CX}$
$t_{CGH\text{-}CZ}$
$t_{CGH\text{-}CX}$
C_X
HIT

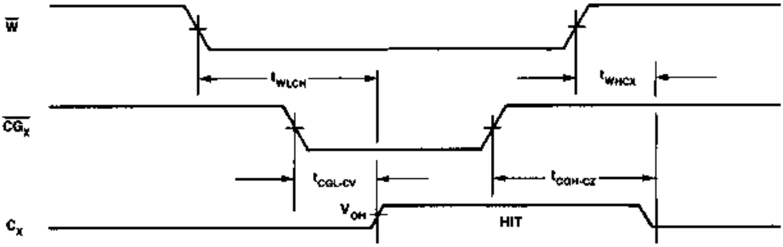
NOTE:
$\overline{W}$ is HIGH and a Valid Address is present. $\overline{H}_X$ and $\overline{M}_X$ are both assumed to be HIGH

FIGURE 18. COMPARE - READ HIT - COMPARE CYCLE


$\overline{G}$
t_{GLCH}
t_{GLCX}
t_{GHCV}
t_{GHCX}
C_X
VALID COMPARE
HIT
COMPARE

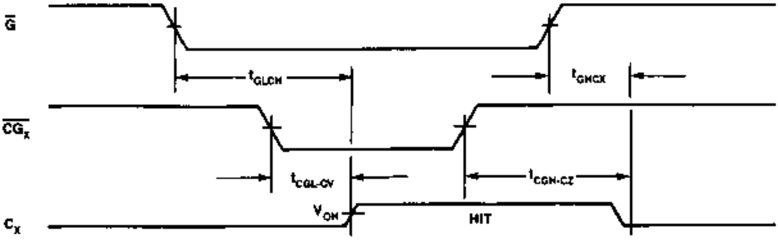
NOTE:
$\overline{W}$ is HIGH and a Valid Address is present. $\overline{H_X}$ and M_X are both assumed to be HIGH with $\overline{CG_X}$ LOW

FIGURE 19. EARLY WRITE - HIT CYCLE


$\overline{W}$
t_{WLCH}
t_{WHCX}
$\overline{CG_X}$
$t_{CGL\text{-}CV}$
$t_{CGH\text{-}CZ}$
V_{OH}
C_X
HIT

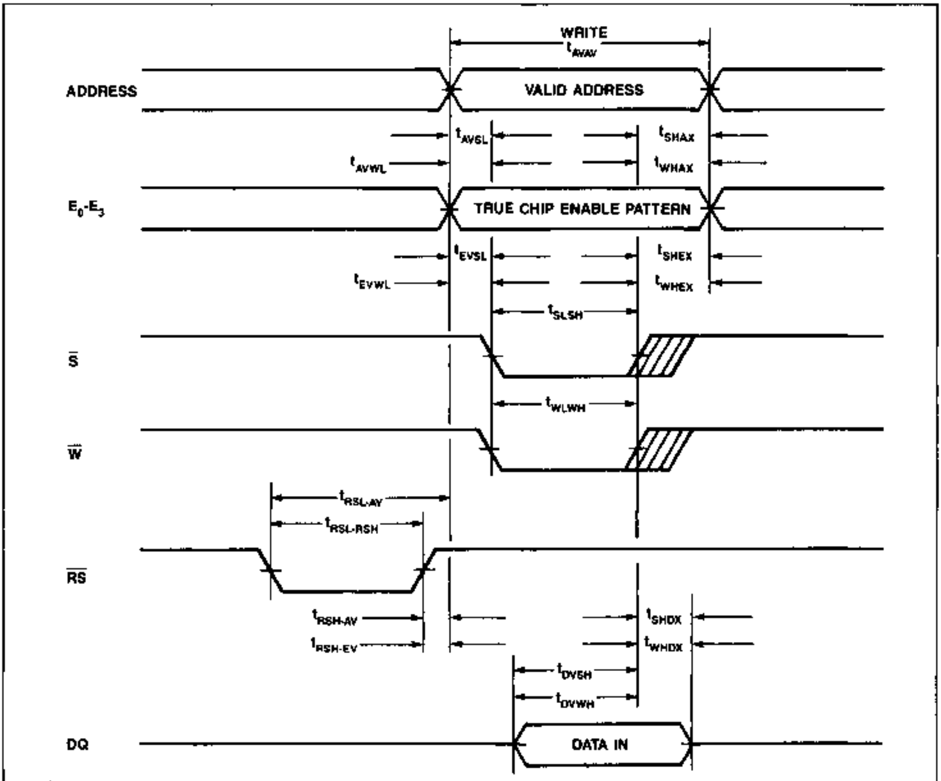
NOTE:
$\overline{G}$ is HIGH and a Valid Address is present, with (E_0-E_3) - True. $\overline{H_X}$ and M_X are both assumed to be HIGH

FIGURE 20. EARLY READ - HIT CYCLE


$\overline{G}$
t_{GLCH}
t_{GHCX}
$\overline{CG_X}$
$t_{CGL\text{-}CV}$
$t_{CGH\text{-}CZ}$
V_{OH}
C_X
HIT

NOTE:
$\overline{W}$ is HIGH and a Valid Address is present, with (E_0-E_3) - True. $\overline{H_X}$ and $\overline{M_X}$ are both assumed to be HIGH

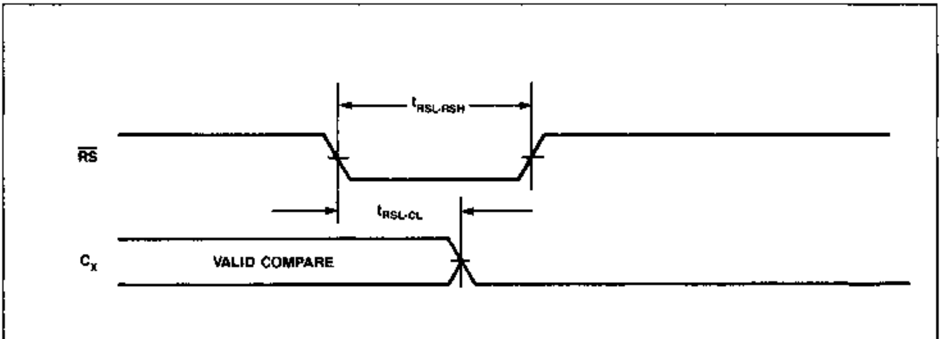
FIGURE 21. RESET CYCLE


WRITE
t_{AVAV}
ADDRESS
VALID ADDRESS
t_{AVSL}
t_{SHAX}
t_{AVWL}
t_{WHAX}
E_0-E_3
TRUE CHIP ENABLE PATTERN
t_{EVSL}
t_{SHEX}
t_{EVWL}
t_{WHEX}
t_{SLSH}
$\overline{S}$
t_{WLWH}
$\overline{W}$
t_{RSL-AV}
$t_{RSL-RSH}$
$\overline{RS}$
t_{RSH-AV}
t_{RSH-EV}
t_{SHDX}
t_{WHDX}
t_{DVSH}
t_{DVWH}
DQ
DATA IN

NOTE:

Reset during an active write cycle is not allowed. A write cycle may disrupt Reset, but will not damage device.

FIGURE 22. VALID COMPARE - RESET


$t_{RSL-RSH}$
$\overline{RS}$
t_{RSL-CL}
C_X
VALID COMPARE

NOTE: CDQ_0 is presumed to be HIGH.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} .... −1.5 to 7.0 volts
Ambient Operating Temperature (T_A) .... 0 to 70°C
Ambient Temperature under Bias .... −55°C to 125°C
Ambient Storage Temperature (Plastic) .... −55°C to 125°C
Total Device Power Dissipation .... 2.5 Watts
RMS Output Current per Pin 25mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Input	2.2		$V_{CC}+0.3$	V	5
V_{IL}	Logic 0 Input	−0.3		0.8	V	5

NOTE: All voltages referenced to V_{SS}.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0 to 70°C, V_{CC} = ± 10%)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
I_{CC}	Average Power Supply Current			225	mA	1
I_{CCA}	Active Power Supply Current (f = 0)			150	mA	1
I_{CCD}	Dynamic Power Supply Current per MHz			1.2	mA/MHz	1
I_{SB1}	TTL Standby Current			70	mA	1
I_{IL}	Input Leakage Current	−1		+1	μA	2
I_{OL}	Output Leakage Current	−10		+10	μA	3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = −4mA)	2.4			V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)			0.4	V	4

NOTES

1. Measured with outputs open. V_{CC} max.
2. Measured with V_{IN} = 0.0V to V_{CC}.
3. Measured at CDQ_0, DQ_1-DQ_{19}, C_0 and C_1.
4. All voltages referenced to V_{SSQ}.
5. Inputs (P_0-P_3) require V_{IH} min. = 4.5 volts and V_{IL} max. = 0.5 volts.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	LIMITS		UNITS	NOTE
		TYP	MAX		
C_I	Input Capacitance	4	4	pf	1
C_O	Output Capacitance	8	10	pf	1,2

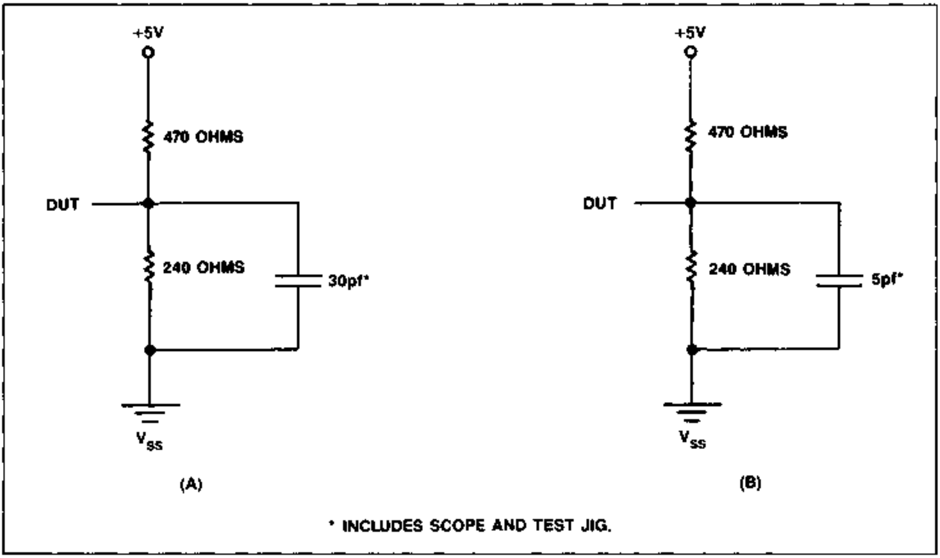
NOTES

1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data I/O's, C0 and C1.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0° to 70°C
V_{CC}	5.0 Volts ± 10%

FIGURE 23. EQUIVALENT OUTPUT LOAD CIRCUIT


+5V
470 OHMS
DUT
240 OHMS
30pf*
V_{SS}
(A)
+5V
470 OHMS
DUT
240 OHMS
5pf*
V_{SS}
(B)
* INCLUDES SCOPE AND TEST JIG.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	CYCLE TIME	PACKAGE TYPE	TEMPERATURE
MK4202(Q)-20	20ns	25ns	68 pin PLCC	0°C to 70°C

TAGRAM is a trademark of SGS-THOMSON Microelectronics, Inc.

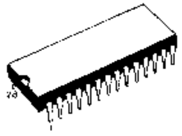
SGS-THOMSON
MICROELECTRONICS

MK48H74(N,P,E)-35/45/55

64K (8K × 8-BIT) CMOS TAGRAM™

ADVANCED DATA

- 8K × 8 CMOS SRAM WITH ONBOARD 8-BIT COMPARATOR
- ADDRESS TO COMPARE ACCESS 35/45/55ns
- FAST CHIP SELECT TO COMPARE ACCESS 20/25/30ns
- MATCH OUTPUT (OPEN DRAIN) WITH FAST TAG DATA TO COMPARE ACCESS OF 25/30/35ns (MAX.)
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- ALL INPUTS AND OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS FOR LOW POWER OPERATION
- FLASH CLEAR FUNCTION
- THREE-STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL DIP AND 32-PIN LCC
- HIGH SPEED ASYNCHRONOUS RAM CLEAR (CYCLE TIME = 2 × t_{AVAV})

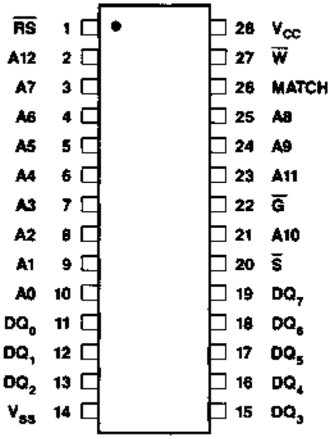


N
DIP-28
(Plastic Package)

PIN NAMES

A_0 - A_{12}	- Address Inputs
DQ_0 - DQ_7	- Data Input/Output
$\overline{S}$	- Chip Select
$\overline{W}$	- Write Enable
$\overline{G}$	- Output Enable
V_{CC}	- +5V
V_{SS}	- Ground
$\overline{RS}$	Reset Flash Clear
MATCH	Match Output

FIGURE 1. PIN CONNECTIONS



$\overline{RS}$ 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
DQ_0 11
DQ_1 12
DQ_2 13
V_{SS} 14
28 V_{CC}
27 $\overline{W}$
26 MATCH
25 A8
24 A9
23 A11
22 $\overline{G}$
21 A10
20 $\overline{S}$
19 DQ_7
18 DQ_6
17 DQ_5
16 DQ_4
15 DQ_3

MK48H74 TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	MODE	DQ	MATCH
X	X	X	L	Reset Clear	—	High
X	H	X	H	Deselect	High-Z	High
H	L	H	H	Miss-NOmatch	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High
H	L	L	H	Read	Q_{OUT}	High
L	L	X	H	Write	D_{IN}	High

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

DESCRIPTION

The MK48H74 is a 65,636-bit fast static cache TAGRAM organized as 8K × 8 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The MK48H74 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The device requires a single +5V ±10 percent supply, and is fully TTL compatible.

The MK48H74 has a fast Chip Select control for high speed operation to Match Compare valid, and device select/deselect operations. Additionally, the MK48H74 provides a Reset Clear, and Match compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open-drain for wired OR operation. During a match compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A_0-A_{12}) to the internal RAM data. If a match exists, the MATCH output issues a HIGH match valid signal. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

READ MODE

The MK48H74 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW, and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

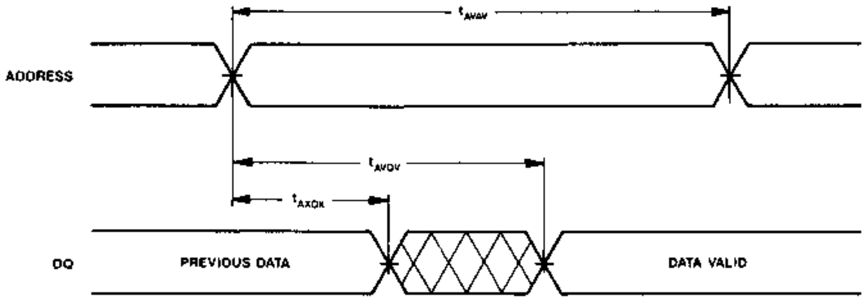
Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW, and $\overline{S}$ is LOW. If Chip Select or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{SLQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0 ±10%)

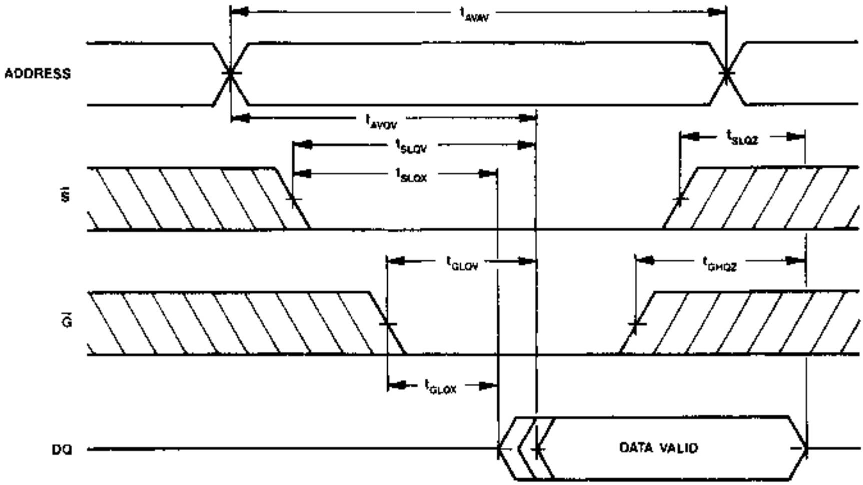
SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	35		45		55		ns	
t_{AA}	t_{AVQV}	Address Access Time		35		45		55	ns	1
t_{CSA}	t_{SLQV}	Chip Select Access Time		20		25		30	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		20		25		30	ns	1
t_{CSL}	t_{SLQX}	Chip Select to Output Low-Z	5		5		5		ns	
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		0		ns	
t_{CSZ}	t_{SHQZ}	Chip Select to High-Z		15		20		25	ns	
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		15		20		25	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	3		3		3		ns	1

FIGURE 2. READ TIMING NO. 1 (ADDRESS ACCESS)


t_{AVAV}
ADDRESS
t_{AVQV}
t_{AXQX}
DQ
PREVIOUS DATA
DATA VALID

NOTE: Chip Select and Output Enable are presumed valid, $\overline{W}$ = V_{IH}.

FIGURE 3. READ TIMING NO. 2 ($\overline{W}$ = V_{IH})


t_{AVAV}
ADDRESS
t_{AVQV}
t_{SLQV}
t_{SLQX}
t_{SLQZ}
$\overline{S}$
t_{GLQV}
t_{GHQZ}
$\overline{G}$
t_{GLQX}
DQ
DATA VALID

WRITE MODE

The MK48H74 is in the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL}, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$.

If the Output is enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ±10%)

SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	35		45		55		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		0		ns	
t_{AS}	t_{AVSL}	Address Set-up Time to Chip Select	0		0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	25		35		45		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	25		35		45		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		0		ns	
t_{CSW}	t_{SLSH}	Chip Select to End of Write	25		35		45		ns	
t_{WR}	t_{SHAX}	Write Recovery Time to Chip Deselect	0		0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	25		30		30		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (Active)	0		0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		15		20		25	ns	2

FIGURE 4. WRITING TIMING NO. 1 ($\overline{W}$ CONTROL)

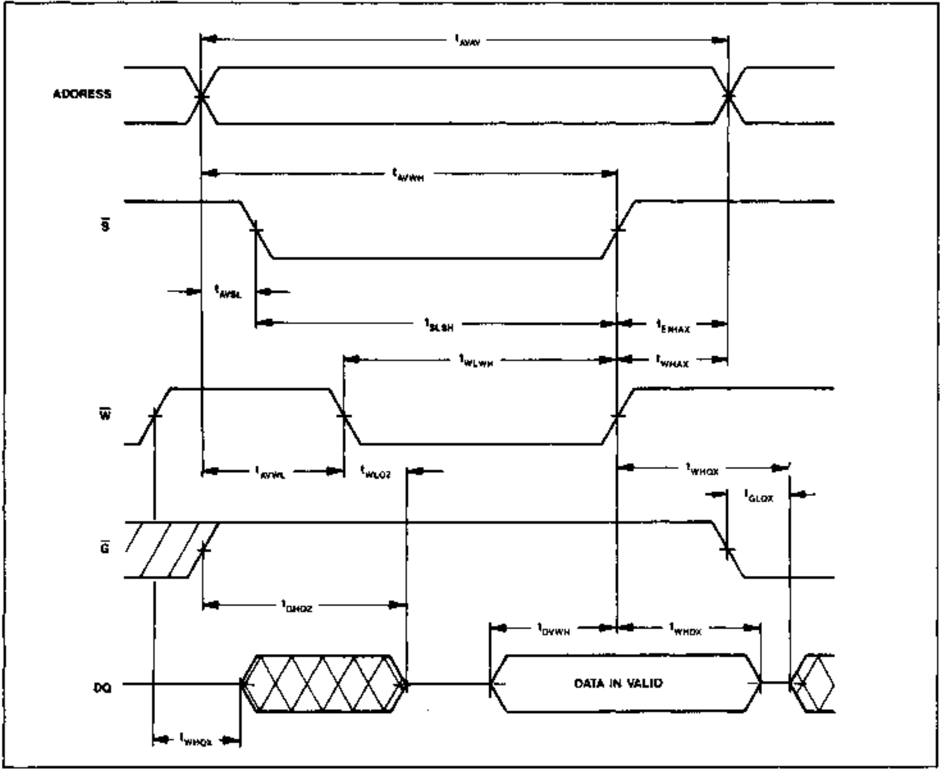
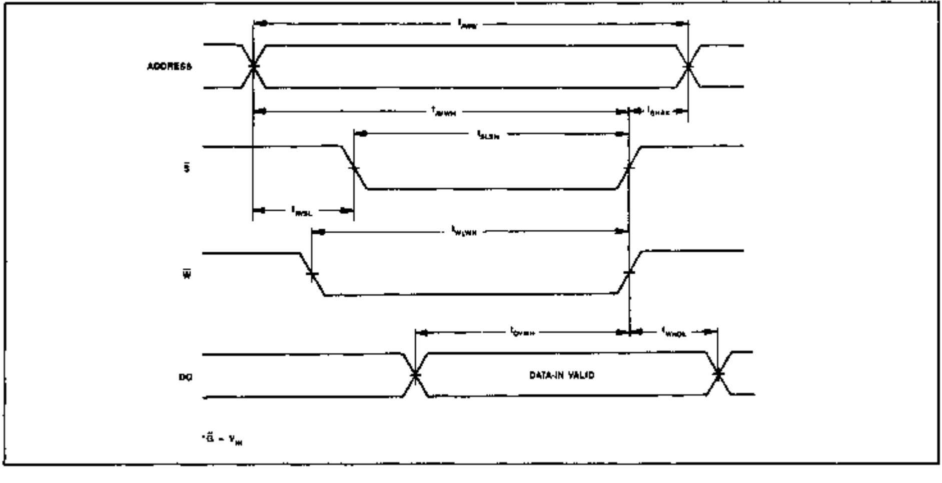

t_{AVAV}
ADDRESS
t_{AVWH}
$\overline{S}$
t_{AVSL}
t_{SLSH}
t_{EHAX}
t_{WLWH}
t_{WHAX}
$\overline{W}$
t_{AVWL}
t_{WLQZ}
t_{WHQX}
t_{GLQX}
$\overline{G}$
t_{GHQZ}
t_{DVWH}
t_{WHDX}
DQ
DATA IN VALID
t_{WHQX}

FIGURE 5. WRITING TIMING NO. 2 ($\overline{S}$ CONTROL)


t_{AVAV}
ADDRESS
t_{AVWH}
t_{SHAX}
t_{SLSH}
$\overline{S}$
t_{AVSL}
t_{WLWH}
$\overline{W}$
t_{DVWH}
t_{WHDX}
DQ
DATA-IN VALID
$^{*}\overline{G} = V_{IH}$

COMPARE MODE

The MK48H74 is in the Compare mode whenever W and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A_0-A_{12}) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ_0-DQ_7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal (match) then a hit condition occurs (MATCH = HIGH). When at least one bit is not equal, then MATCH will go LOW signifying a miss condition.

The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when $\overline{S}$ is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, and $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

MATCH COMPARE CYCLE TIMING AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 ±10%)

SYMBOLS			48H74-35		48H74-45		48H74-55			
ALT	STD	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{AMA}	t_{AVMV}	Address to MATCH Valid	—	35	—	45	—	55	ns	2,3
t_{CSM}	t_{SLMV}	Chip Select to MATCH Valid	—	20	—	25	—	30	ns	2,3
t_{CSMH}	t_{SHMH}	Chip Deselect to MATCH High	—	20	—	25	—	30	ns	2,3
t_{DMA}	t_{TVMV}	Tag Data to MATCH Valid	—	25	—	30	—	35	ns	2,3
t_{OEM}	t_{GHMV}	$\overline{G}$ High to MATCH Valid	—	25	—	35	—	45	ns	3
t_{OEMH}	t_{GLMH}	$\overline{G}$ Low to MATCH High	—	25	—	35	—	45	ns	3
t_{WEM}	t_{WHMV}	$\overline{W}$ High to MATCH Valid	—	25	—	35	—	45	ns	3
t_{WEMH}	t_{WLMH}	$\overline{W}$ Low to MATCH High	—	25	—	35	—	45	ns	3
t_{MHA}	t_{AHMV}	MATCH Hold From Address	5	—	5	—	5	—	ns	3
t_{MHD}	t_{DHMV}	MATCH Hold From Tag Data	5	—	5	—	5	—	ns	3

RESET MODE

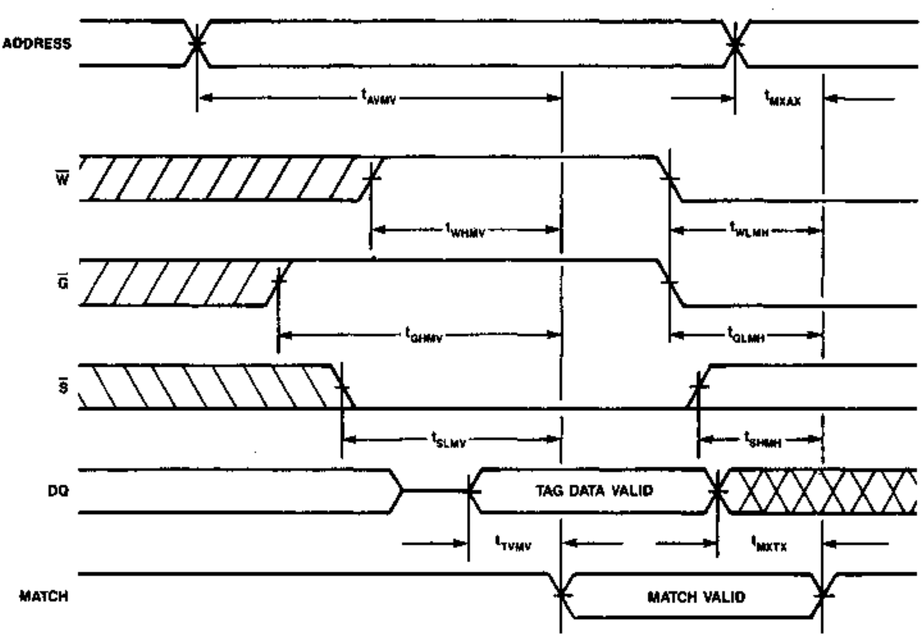
The MK48H74 allows an asynchronous reset clear whenever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65536 bits) to a logic zero as long as $t_{RSL\text{-}RSH}$ is satisfied. The state of the outputs is determined by the control logic input pins $\overline{S}$, $\overline{W}$, and $\overline{G}$ during reset (see truth table). The MATCH output will go HIGH $t_{RSL\text{-}MH}$ from the falling edge of $\overline{RS}$, and all inputs will not be recognized until $t_{RSH\text{-}AV}$ from the rising edge of reset ($\overline{RS}$).

RESET CLEAR CYCLE TIMING AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

SYMBOLS			-35		-45		-55			
ALT	STD	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{RSC}	Flash Clear Cycle Time	70		90		110		ns	
t_{RSX}	$t_{RSL\text{-}AX}$	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSV}	$t_{RSH\text{-}AV}$	$\overline{RS}$ to Inputs Valid	5		10		10		ns	
t_{RSP}	$t_{RSL\text{-}RSH}$	Reset ($\overline{RS}$) Pulse Width	65		85		100		ns	
t_{RSM}	$t_{RSL\text{-}MH}$	Reset ($\overline{RS}$) to MATCH High		25		35		45	ns	

FIGURE 6. MATCH COMPARE TIMING


ADDRESS
tAVMV
tMXAX
W̄
tWHMV
tWLMH
Ḡ
tGHMV
tGLMH
S̄
tSLMV
tSHMH
DQ
TAG DATA VALID
tTVMV
tMXTX
MATCH
MATCH VALID

APPLICATION

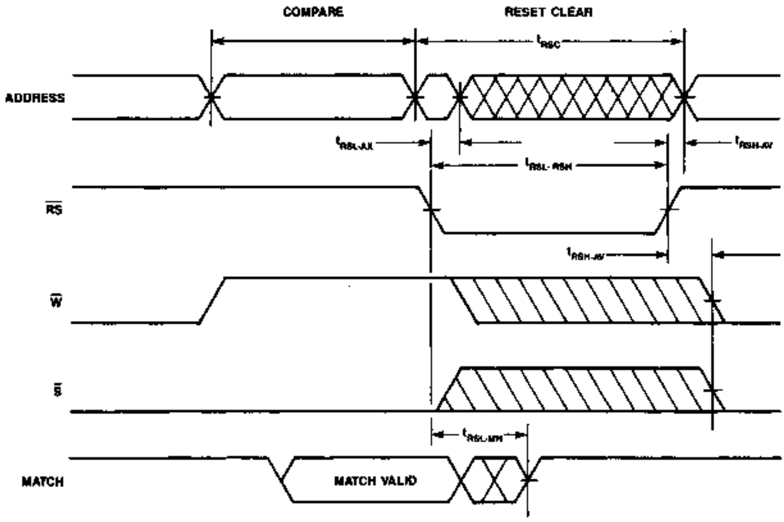
The MK48H74 operates from a 5.0 volt supply. It is compatible with all standard **TTL** families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input, does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK48H74 can also interface to 5 volt CMOS on all inputs and outputs.

The MK48H74 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWYDE™ on-board comparator — all in one chip. The MK48H74 compares contents of addressed RAM locations to the current data inputs. A logic one (1) output on the MATCH pin indicates that the input data and the RAM contents match. Conversely, a logic zero (0) on the MATCH pin indicates at least one bit difference between the RAM contents and input TAG data generating a miss. The MATCH output is constructed with an open drain arrangement. This provides easy wired-OR implementation when generating a composite MATCH signal.

In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of a portion of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48H74, and providing good hit or match ratio designs will enhance overall system performance.

Because high frequency current transients will be associated with the operation of the MK48H74, power lines inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 7. RESET TIMING



NOTE: $\overline{G}$ = HIGH FOR THIS EXAMPLE

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND .... −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) .... 0°C to +70°C
Ambient Storage Temperature (Plastic) .... −55°C to +125°C
Ambient Storage Temperature (Ceramic) .... −65°C to +150°C
Total Device Power Dissipation .... 1 Watt
Output Current per Pin .... 50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	4
V_{SS}	Supply Voltage	0	0	0	V	4
V_{IH}	Logic 1 Voltage, All Inputs	2.2		$V_{CC}+0.3$	V	4
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current f = min cycle		125	mA	5
I_{CC2}	Average Power Supply Current f = 0		60	mA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Q Output Pin)	−10	+10	μA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	4
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	4
V_{OL}	Match Output Logic 0 Voltage (I_{OUT} = 18 mA)		0.4	V	4

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	9

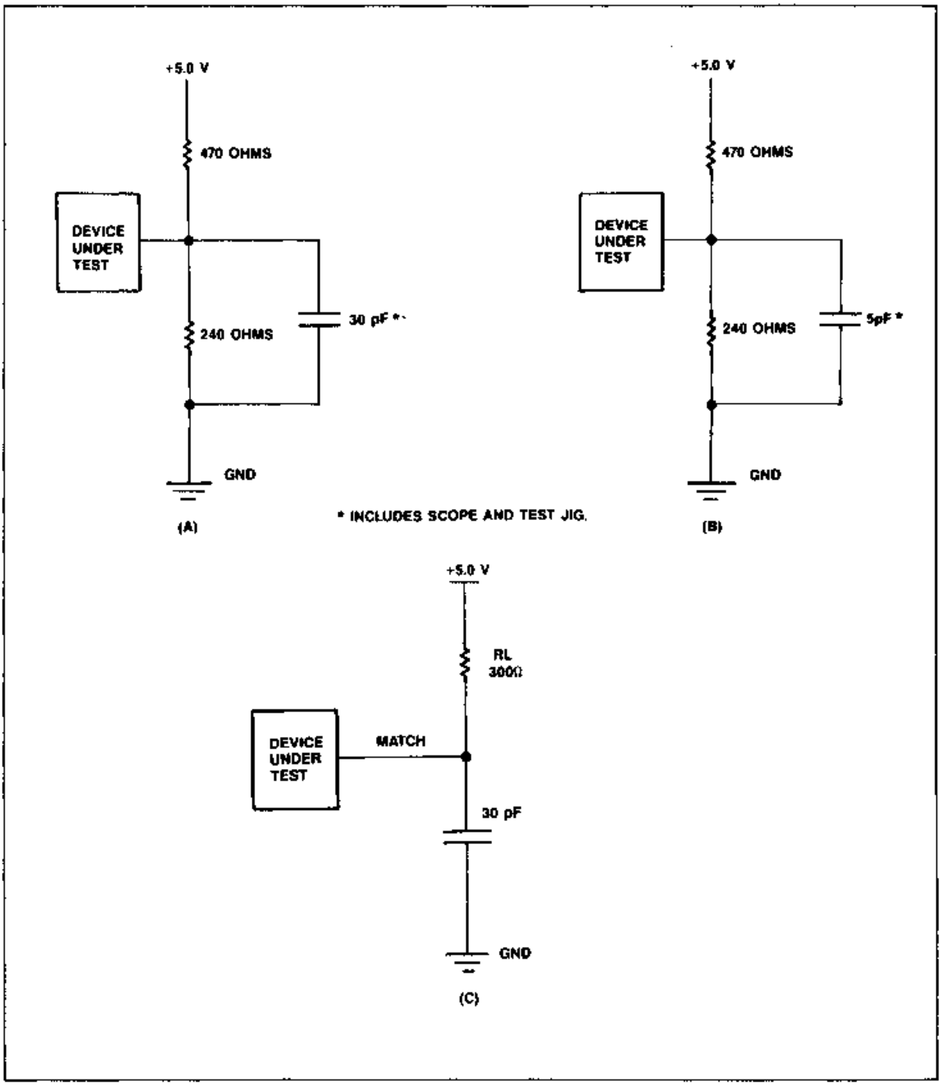
NOTES

1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. Measured with load shown in Figure 8(C).
4. All voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
6. I_{CC2} is measured with outputs open circuit.
7. Input leakage current specifications are valid for all V_{IN} such that $0\text{ V} < V_{IN} < V_{CC}$. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that $0\text{ V} < V_{OUT} < V_{CC}$, $\overline{S} = V_{IH}$, and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

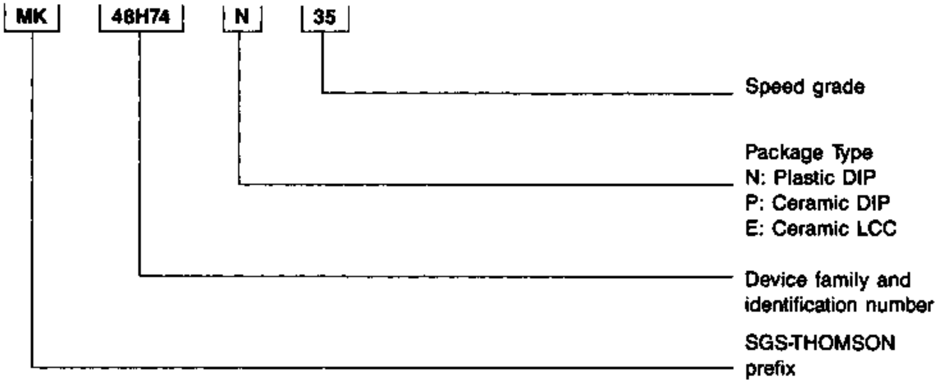
Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 8. OUTPUT LOAD CIRCUITS


+5.0 V
470 OHMS
DEVICE UNDER TEST
30 pF *
240 OHMS
GND
(A)
* INCLUDES SCOPE AND TEST JIG.
+5.0 V
470 OHMS
DEVICE UNDER TEST
5pF *
240 OHMS
GND
(B)
+5.0 V
RL
300Ω
DEVICE UNDER TEST
MATCH
30 pF
GND
(C)

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48H74N-35	35 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74N-45	45 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74N-55	55 ns	28 pin Plastic DIP	0°C to 70°C
MK48H74P-35	35 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74P-45	45 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74P-55	55 ns	28 pin Ceramic DIP	0°C to 70°C
MK48H74E-35	35 ns	32 pin LCC	0°C to 70°C
MK48H74E-45	45 ns	32 pin LCC	0°C to 70°C
MK48H74E-55	55 ns	32 pin LCC	0°C to 70°C


MK
48H74
N
35
Speed grade
Package Type
N: Plastic DIP
P: Ceramic DIP
E: Ceramic LCC
Device family and identification number
SGS-THOMSON prefix

TAGRAM is a trademark of SGS-THOMSON Microelectronics, Inc.
BYTEWYDE is a trademark of SGS-THOMSON Microelectronics, Inc.

STATIC RAM DEVICES

FIFO

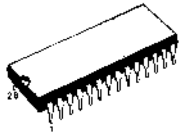
SGS-THOMSON
MICROELECTRONICS

MK4501(N,K)
-65/80/10/12/15/20

512 × 9 CMOS BiPORT FIFO

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 512 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE

Part No.	Access Time	R/W Cycle Time
MK4501-65	65 ns	80 ns
MK4501-80	80 ns	100 ns
MK4501-10	100 ns	120 ns
MK4501-12	120 ns	140 ns
MK4501-15	150 ns	175 ns
MK4501-20	200 ns	235 ns



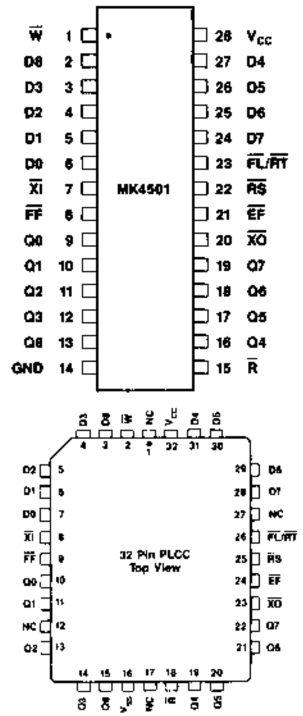
N
DIP-28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

PIN NAMES

$\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL}/\overline{RT}$ = First Load/ Retransmit
D = Data In
Q = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO}$ = Expansion Out
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{CC} = 5 Volts
GND = Ground

FIGURE 1. PIN CONNECTIONS


W̄ 1
D8 2
D3 3
D2 4
D1 5
D0 6
X̄Ī 7
F̄F̄ 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 VCC
27 D4
26 D5
25 D6
24 D7
23 F̄L̄/R̄T̄
22 R̄S̄
21 ĒF̄
20 X̄Ō
19 Q7
18 Q6
17 Q5
16 Q4
15 R̄
MK4501
D3 4
D8 3
W̄ 2
NC 1
VCC 32
D4 31
D5 30
D2 5
D1 6
D0 7
X̄Ī 8
F̄F̄ 9
Q0 10
Q1 11
NC 12
Q2 13
29 D6
28 D7
27 NC
26 F̄L̄/R̄T̄
25 R̄S̄
24 ĒF̄
23 X̄Ō
22 Q7
21 Q6
32 Pin PLCC
Top View
14 Q3
15 Q8
16 VSS
17 NC
18 R̄
19 Q4
20 Q5

DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

Unlike conventional shift register based FIFOs, the MK4501 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the MK4501 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired.

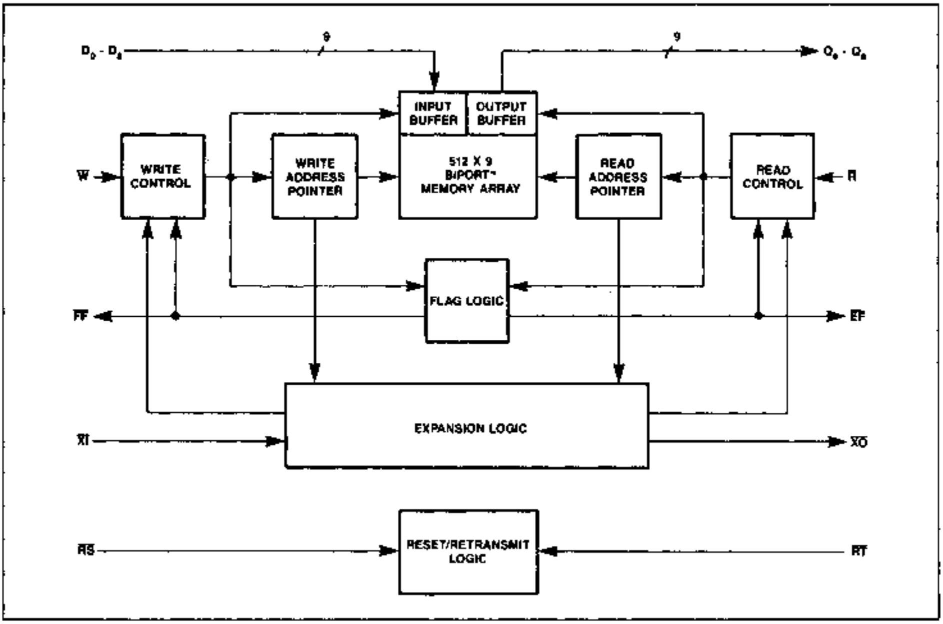
Twin address pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written.

Address pointers automatically loop back to address zero after reaching address 511. The empty/full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the address pointers to address zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4501 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4501 allows connecting the read, write, data in, and data out lines of the MK4501s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins as appropriate (see the Expansion Timing section for a more complete discussion).

FIGURE 2. MK4501 BLOCK DIAGRAM

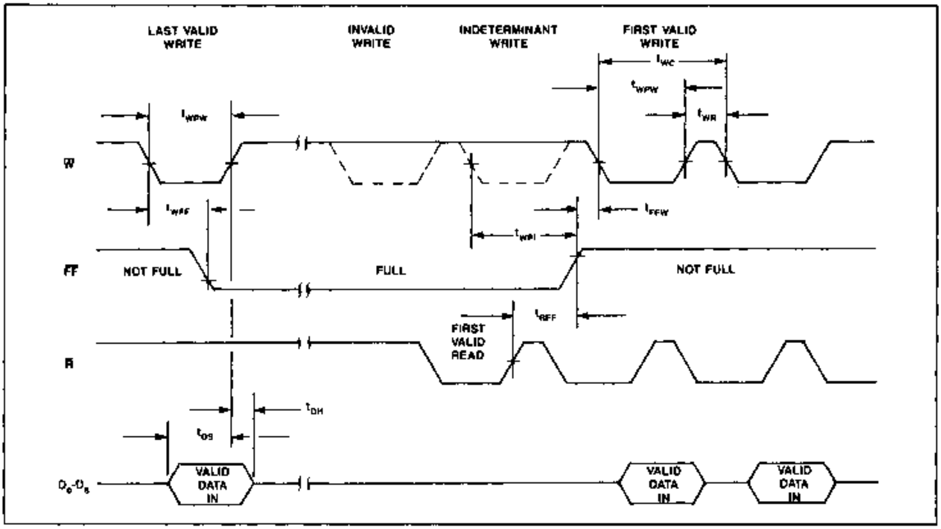


$D_0 - D_8$
9
9
$Q_0 - Q_8$
INPUT BUFFER
OUTPUT BUFFER
$\overline{W}$
WRITE CONTROL
WRITE ADDRESS POINTER
512 X 9 BIPORT™ MEMORY ARRAY
READ ADDRESS POINTER
READ CONTROL
$\overline{R}$
FLAG LOGIC
$\overline{FF}$
$\overline{EF}$
EXPANSION LOGIC
$\overline{XI}$
$\overline{XO}$
$\overline{RS}$
RESET/RETRANSMIT LOGIC
$\overline{RT}$

WRITE MODE

The MK4501 initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4501 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

FIGURE 3A. WRITE AND FULL FLAG TIMING


LAST VALID WRITE
INVALID WRITE
INDETERMINANT WRITE
FIRST VALID WRITE
t_{WC}
t_{WPW}
t_{WR}
t_{WPW}
W
t_{WFF}
t_{FFW}
t_{WPI}
FF
NOT FULL
FULL
NOT FULL
FIRST VALID READ
t_{RFF}
R
t_{DH}
t_{DS}
D_0-D_8
VALID DATA IN
VALID DATA IN
VALID DATA IN

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0$ volts ± 10%)

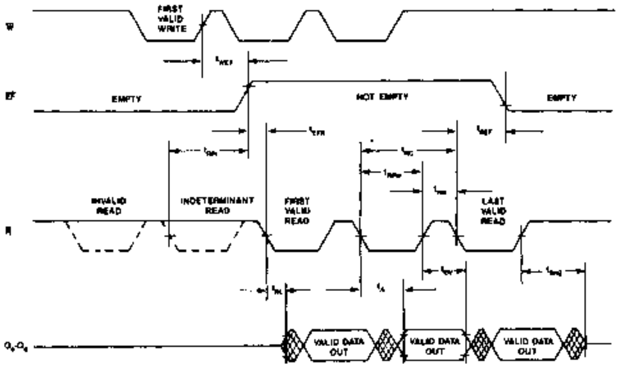
		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	20		25		35		40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		60		75		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		60		75		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant		35		35		35		35		35		35	ns	2

READ MODE

The MK4501 initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4501 provides a fast access to data from 9 of 4608 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

FIGURE 3B. READ AND EMPTY FLAG TIMING



AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{RC}	Read Cycle Time	80		100		120		140		175		235		ns	
t_A	Access Time		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from High $\overline{R}$	5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35	ns	2

FIGURE 4A. READ/WRITE TO FULL FLAG

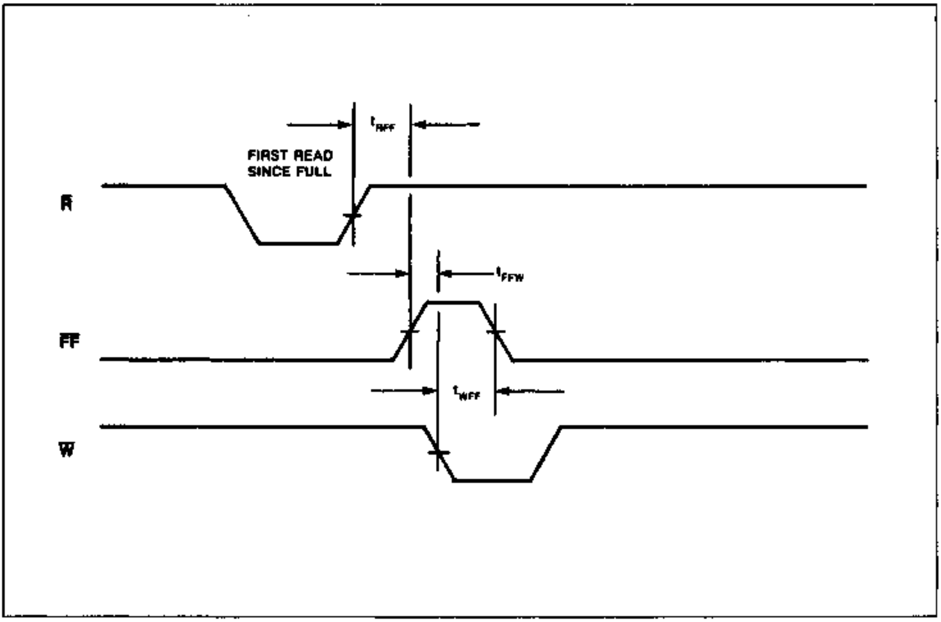
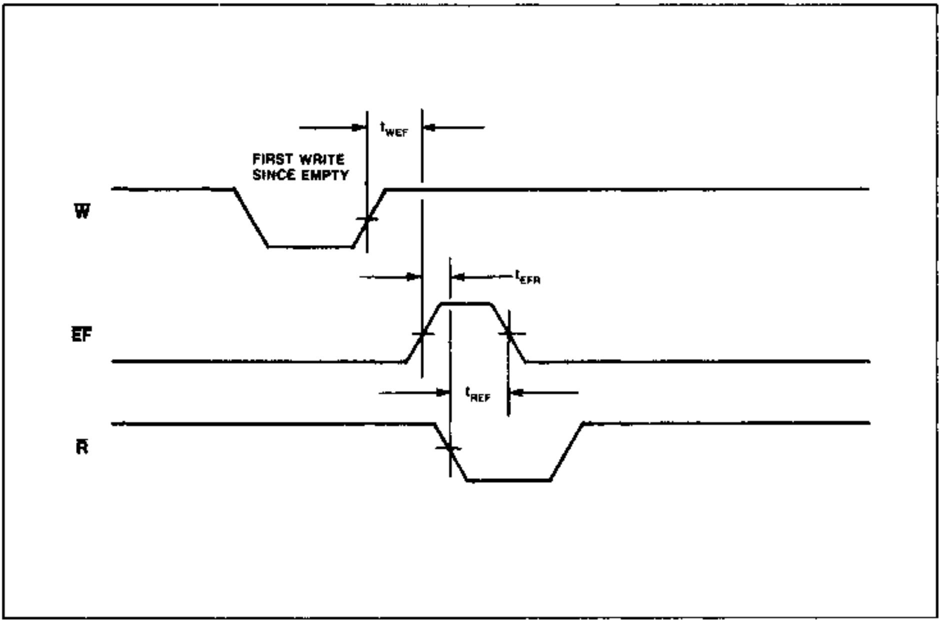

t_{RFF}
FIRST READ SINCE FULL
$\overline{R}$
t_{FFW}
$\overline{FF}$
t_{WFF}
$\overline{W}$

FIGURE 4B. WRITE/READ TO EMPTY FLAG

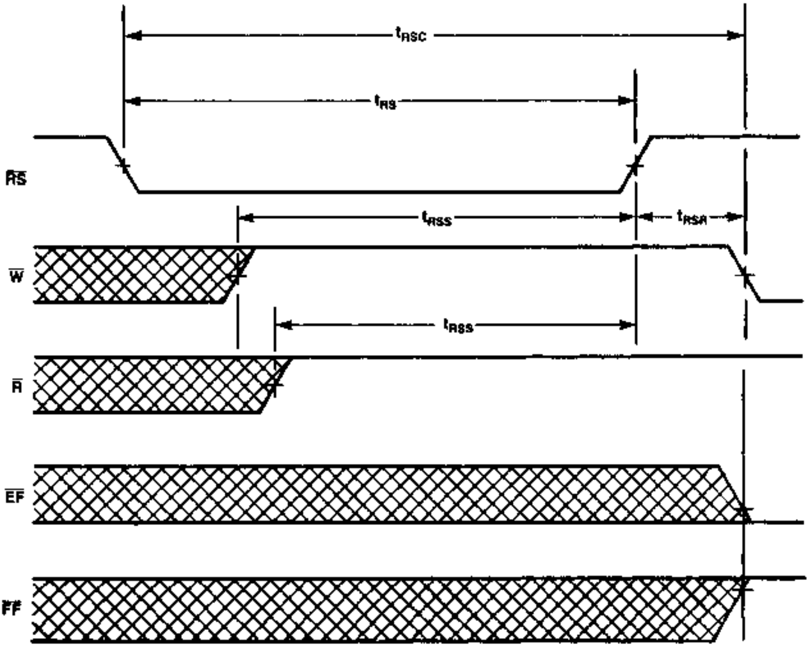

t_{WEF}
FIRST WRITE SINCE EMPTY
$\overline{W}$
t_{EFR}
$\overline{EF}$
t_{REF}
$\overline{R}$

RESET

The MK4501 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

FIGURE 5. RESET



NOTE
$\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

(0°C $\leq T_A \leq$ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4501-65 MIN	4501-65 MAX	4501-80 MIN	4501-80 MAX	4501-10 MIN	4501-10 MAX	4501-12 MIN	4501-12 MAX	4501-15 MIN	4501-15 MAX	4501-20 MIN	4501-20 MAX	UNITS	NOTES
t_{RSC}	Reset Cycle Time	80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	45		60		80		100		130		180		ns	

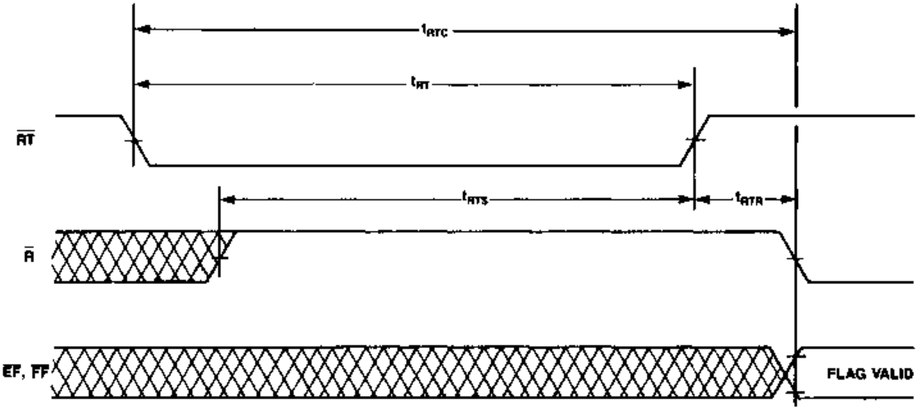
RETRANSMIT

The MK4501 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 512 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

FIGURE 6. RETRANSMIT



NOTE
EF and FF may change status during Retransmit,
but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4501-65 MIN	4501-65 MAX	4501-80 MIN	4501-80 MAX	4501-10 MIN	4501-10 MAX	4501-12 MIN	4501-12 MAX	4501-15 MIN	4501-15 MAX	4501-20 MIN	4501-20 MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	45		60		80		100		130		180		ns	

SINGLE DEVICE CONFIGURATION

A single MK4501 may be used when application requirements are for 512 words or less. The MK4501 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin $(\overline{XI})$ grounded (see Figure 7).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

FIGURE 7. A SINGLE 512 x 9 FIFO CONFIGURATION

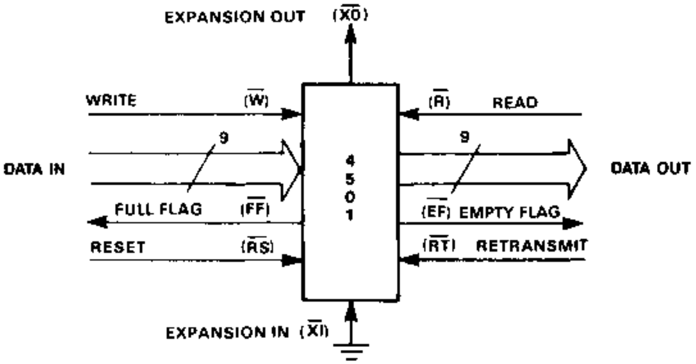
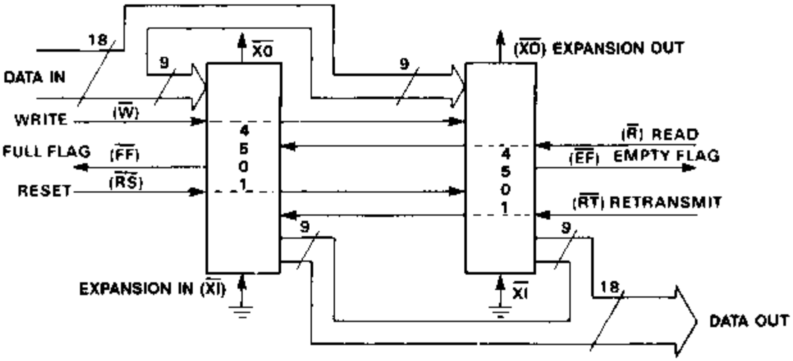

EXPANSION OUT ($\overline{XO}$)
WRITE ($\overline{W}$)
9
DATA IN
FULL FLAG ($\overline{FF}$)
RESET ($\overline{RS}$)
4501
($\overline{R}$) READ
9
DATA OUT
($\overline{EF}$) EMPTY FLAG
($\overline{RT}$) RETRANSMIT
EXPANSION IN ($\overline{XI}$)

FIGURE 8. A 512 x 18 FIFO CONFIGURATION (WIDTH EXPANSION)


18
DATA IN
9
WRITE ($\overline{W}$)
FULL FLAG ($\overline{FF}$)
RESET ($\overline{RS}$)
$\overline{XO}$
4501
9
EXPANSION IN ($\overline{XI}$)
9
($\overline{XO}$) EXPANSION OUT
4501
($\overline{R}$) READ
($\overline{EF}$) EMPTY FLAG
($\overline{RT}$) RETRANSMIT
9
$\overline{XI}$
18
DATA OUT

NOTE

Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

DEPTH EXPANSION (DAISY CHAIN)

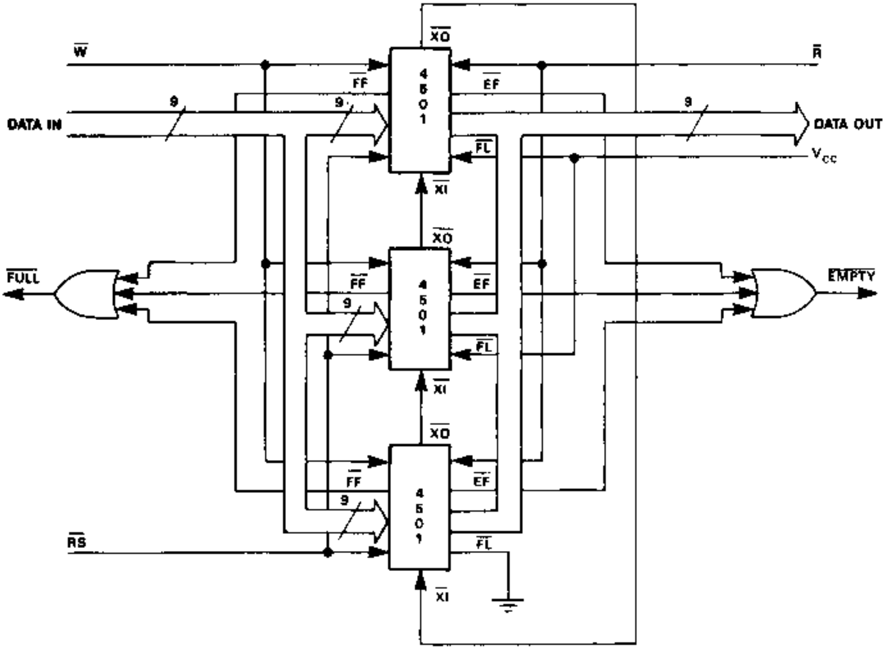
The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 9 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{\text{EF}}$s and the ORing of all FFs (i.e., all must be set to generate the correct composite $\overline{\text{FF}}$ or $\overline{\text{EF}}$).

The MK4501 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{\text{FL}}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{\text{FL}}$ in the high state.
3. The Expansion Out ($\overline{\text{XO}}$) pin of each device must be tied to the Expansion In ($\overline{\text{XI}}$) pin of the next device.

FIGURE 9. A 1536 x 9 FIFO CONFIGURATION (DEPTH EXPANSION)

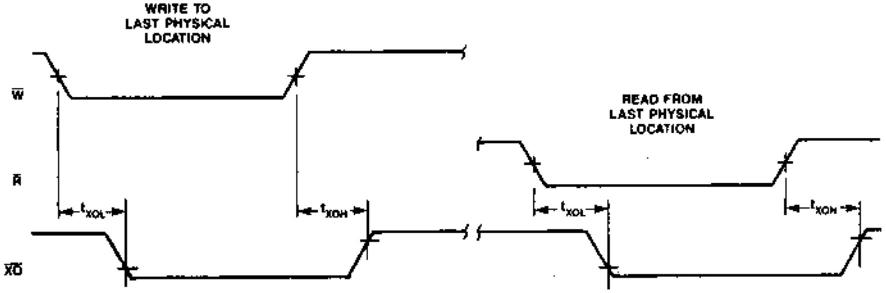


EXPANSION TIMING

Figures 10 and 11 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

FIGURE 10. EXPANSION OUT TIMING



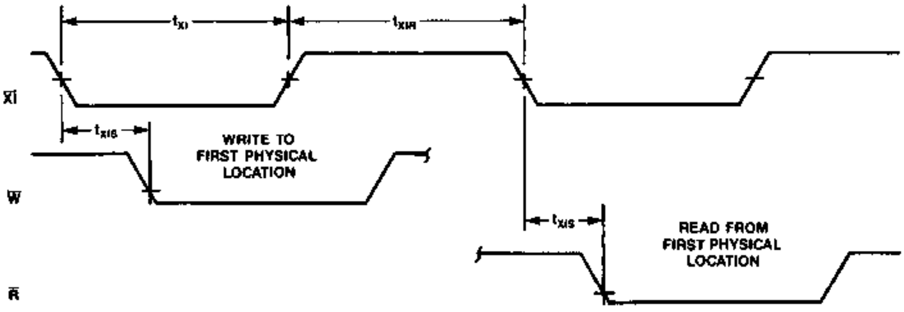
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4501-65 MIN	4501-65 MAX	4501-80 MIN	4501-80 MAX	4501-10 MIN	4501-10 MAX	4501-12 MIN	4501-12 MAX	4501-15 MIN	4501-15 MAX	4501-20 MIN	4501-20 MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4501 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4501 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

FIGURE 11. EXPANSION IN TIMING



tXI
tXIR
X̄I
tXIS
WRITE TO FIRST PHYSICAL LOCATION
W̄
tXIS
READ FROM FIRST PHYSICAL LOCATION
R̄

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4501-65		4501-80		4501-10		4501-12		4501-15		4501-20			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{XI}	Expansion In Pulse Width	60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	25		30		45		50		60		85		ns	

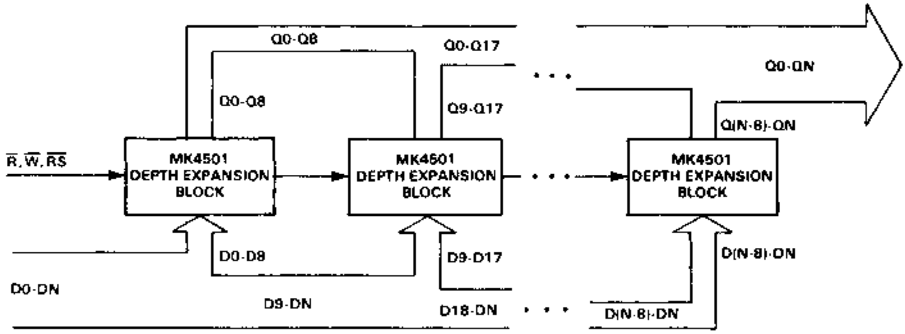
COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 12).

BIDIRECTIONAL APPLICATIONS

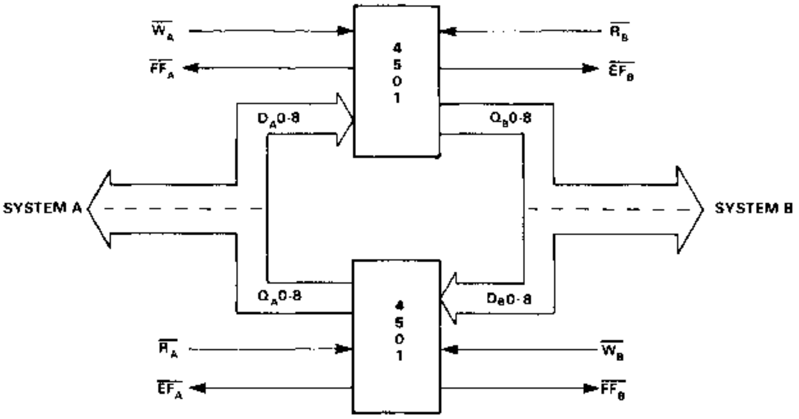
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 13. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

FIGURE 12. COMPOUND FIFO EXPANSION


Q0-Q8
Q0-Q17
Q0-QN
Q0-Q8
Q9-Q17
Q(N-8)-QN
R̄, W̄, R̄S̄
MK4501 DEPTH EXPANSION BLOCK
MK4501 DEPTH EXPANSION BLOCK
MK4501 DEPTH EXPANSION BLOCK
D0-D8
D9-D17
D(N-8)-DN
D0-DN
D9-DN
D18-DN
D(N-8)-DN

NOTES
1. For depth expansion block see DEPTH EXPANSION Section and Figure 9.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

FIGURE 13. BIDIRECTIONAL FIFO APPLICATION


W̄A
FF̄A
R̄B
ĒF̄B
4501
DA0-8
QB0-8
SYSTEM A
SYSTEM B
QA0-8
DB0-8
4501
R̄A
ĒF̄A
W̄B
FF̄B

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND .... -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) .... 0°C to + 70°C
Storage Temperature .... -55°C to + 125°C
Total Device Power Dissipation .... 1 Watt
Output Current per Pin .... 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + 1	V	3
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)		8	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		500	μA	7

AC ELECTRICAL CHARACTERISTICS

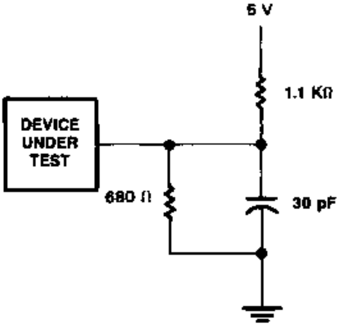
(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_Q	Capacitance on Output Pins		12 pF	8

NOTES

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.

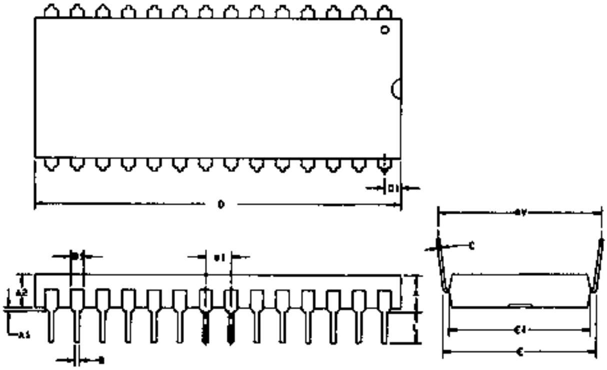
FIGURE 14. OUTPUT LOAD



AC TEST CONDITIONS:

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Level	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10%

FIGURE 15. MK4501 PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS

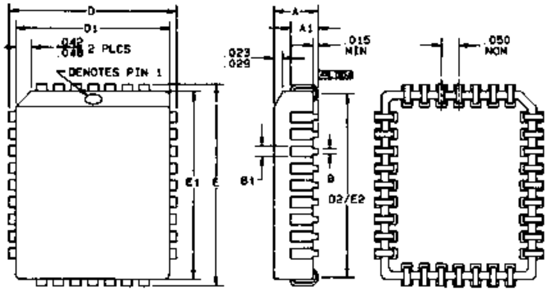


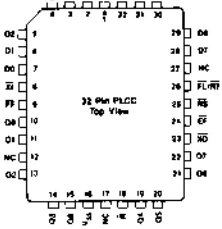
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

FIGURE 16. MK4501 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)


D
D1
.042
.048 2 PLCS
DENOTES PIN 1
E1
E
A
A1
.015 MIN
.023
.029
B1
B
D2/E2
.050 NOM


32 Pin PLCC
Top View
D2
D1
D0
XI
FF
Q0
Q1
NC
Q2
D6
D7
NC
FL/RT
RS
EF
XO
Q7
Q6
Q3
Q8
NC
Q4
Q5
D3
D8
NC
D4
D5

Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK4501N-65	65 ns	80 ns	12.5 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-80	80 ns	100 ns	10.0 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-10	100 ns	120 ns	8.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-12	120 ns	140 ns	7.1 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-15	150 ns	175 ns	5.7 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501N-20	200 ns	235 ns	4.2 MHz	28 Pin Plastic DIP	0° to 70°C
MK4501K-65	65 ns	80 ns	12.5 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-80	80 ns	100 ns	10.0 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-10	100 ns	120 ns	8.3 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-12	120 ns	140 ns	7.1 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-15	150 ns	175 ns	5.7 MHz	32 Pin Plastic LCC	0° to 70°C
MK4501K-20	200 ns	235 ns	4.2 MHz	32 Pin Plastic LCC	0° to 70°C

MK	4501	N	65
SGS-THOMSON Prefix	Device family and number identification	Package type N: Plastic DIP K: Plastic LCC	Speed grade Access Time

MK4503(N,K) -50/65/80/10/12/15/20

2048 × 9 CMOS BiPORT FIFO

PRELIMINARY DATA

- FIRST-IN, FIRST-OUT MEMORY BASED ARCHITECTURE
- FLEXIBLE 2048 x 9 ORGANIZATION
- LOW POWER HCMOS TECHNOLOGY
- ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE
- BIDIRECTIONAL APPLICATIONS
- FULLY EXPANDABLE BY WORD WIDTH OR DEPTH
- EMPTY AND FULL WARNING FLAGS
- RETRANSMIT CAPABILITY
- HIGH PERFORMANCE
- HALF FULL FLAG IN SINGLE DEVICE MODE

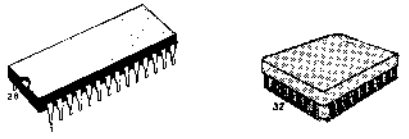
Part No.	Access Time	R/W Cycle Time
MK4503-50	50 ns	65ns
MK4503-65	65 ns	80 ns
MK4503-80	80 ns	100 ns
MK4503-10	100 ns	120 ns
MK4503-12	120 ns	140 ns
MK4503-15	150 ns	175 ns
MK4503-20	200 ns	235 ns

PIN NAMES

$\overline{W}$	= Write	$\overline{XI}$	= Expansion In
$\overline{R}$	= Read	$\overline{XO}/\overline{HF}$	= Expansion Out Half Full Flag
$\overline{RS}$	= Reset	$\overline{FF}$	= Full Flag
$\overline{FL}/\overline{RT}$	= First Load/ Retransmit	$\overline{EF}$	= Empty Flag
		V_{CC}	= 5 Volts
D	= Data In	GND	= Ground
Q	= Data Out	NC	= No Connection

DESCRIPTION

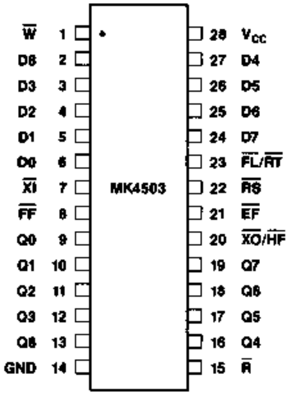
The MK4503 is a member of the BiPORT™ Memory Series, which utilizes special two-port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous



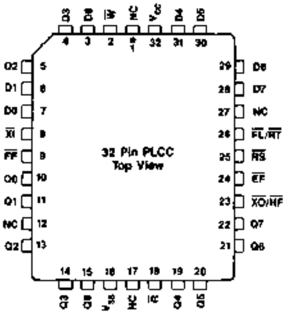
N
DIP-28
(Plastic Package)

K
PLCC32
(Plastic Chip Carrier)

FIGURE 1. PIN CONNECTIONS


$\overline{W}$ 1
D8 2
D3 3
D2 4
D1 5
D0 6
$\overline{XI}$ 7
$\overline{FF}$ 8
Q0 9
Q1 10
Q2 11
Q3 12
Q8 13
GND 14
28 V_{CC}
27 D4
26 D5
25 D6
24 D7
23 $\overline{FL}/\overline{RT}$
22 $\overline{RS}$
21 $\overline{EF}$
20 $\overline{XO}/\overline{HF}$
19 Q7
18 Q6
17 Q5
16 Q4
15 $\overline{R}$
MK4503

28 Pin Plastic DIP


D3 4
D8 3
$\overline{W}$ 2
NC 1
V_{CC} 32
D4 31
D5 30
D2 5
D1 6
D0 7
$\overline{XI}$ 8
$\overline{FF}$ 9
Q0 10
Q1 11
NC 12
Q2 13
29 D6
28 D7
27 NC
26 $\overline{FL}/\overline{RT}$
25 $\overline{RS}$
24 $\overline{EF}$
23 $\overline{XO}/\overline{HF}$
22 Q7
21 Q6
14 Q3
15 Q8
16 V_{SS}
17 NC
18 $\overline{R}$
19 Q4
20 Q5
32 Pin PLCC
Top View

read/write operations, full, half full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4503 is as a rate buffer, sourcing and absorbing data at different rates, (e.g., interfacing fast processors and slow peripherals). The full, half full and empty flags are provided to prevent data overflow and underflow. The data is loaded and emptied on a First-In, First-Out (FIFO) basis, and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future high-density devices. The ninth bit is provided to support control or parity functions.

FUNCTIONAL DESCRIPTION

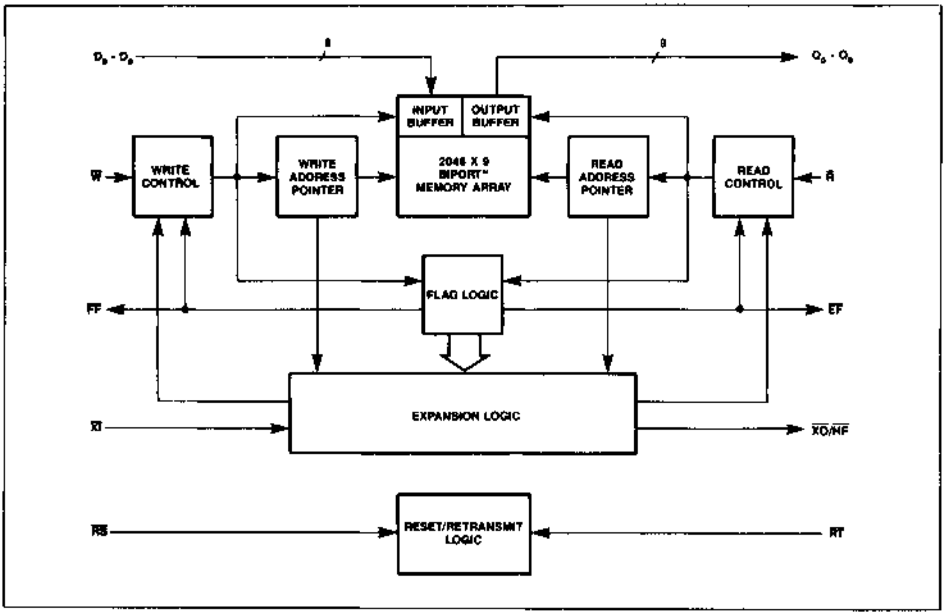
Unlike conventional shift register based FIFOs, the MK4503 employs a memory-based architecture wherein a byte written into the device does not "ripple-through." Instead, a byte written into the MK4503 is stored at a specific location, where it remains until over-written. The byte can be read and re-read as often as desired in the single device configuration.

Twin internal pointers (ring counters) automatically generate the addresses required for each write and read operation. The empty/full flag circuit prevents illogical operations, such as reading un-written bytes (reading while empty) or over-writing un-read bytes (writing while full). Once a byte stored at a given address has been read, it can be over-written. The address pointers automatically loop back to address zero after reaching address 2047. The empty/half full and full status of the FIFO is therefore a function of the distance between the pointers, not of their absolute location. As long as the pointers do not catch one another, the FIFO can be written and read continuously without ever becoming full or empty.

Resetting the FIFO simply resets the write and read pointers to location zero. Pulsing retransmit resets the read address pointer without affecting the write address pointer.

With conventional FIFOs, implementation of a larger FIFO is accomplished by cascading the individual FIFOs. The penalty of cascading is often unacceptable ripple-through delays. The 4503 allows implementation of very large FIFOs with no timing penalties. The memory-based architecture of the MK4503 allows connecting the read, write, data in, and data out lines of the MK4503s in parallel. The write and read control circuits of the individual FIFOs are then automatically enabled and disabled through the expansion-in and expansion-out pins.

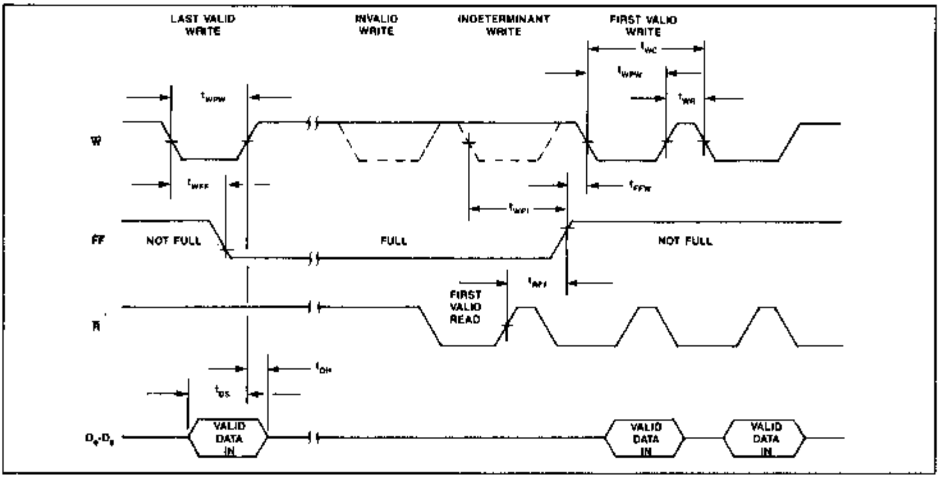
FIGURE 2. MK4503 BLOCK DIAGRAM


$D_0 - D_8$
9
9
$Q_0 - Q_8$
INPUT BUFFER
OUTPUT BUFFER
$\overline{W}$
WRITE CONTROL
WRITE ADDRESS POINTER
2048 X 9 BIPORT™ MEMORY ARRAY
READ ADDRESS POINTER
READ CONTROL
$\overline{R}$
$\overline{FF}$
FLAG LOGIC
$\overline{EF}$
EXPANSION LOGIC
$\overline{XI}$
$\overline{XO}/\overline{HF}$
$\overline{RS}$
RESET/RETRANSMIT LOGIC
$\overline{RT}$

WRITE MODE

The MK4503 initiates a Write Cycle (see Figure 3A) on the falling edge of the Write Enable control input ($\overline{W}$), provided that the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold-time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independent of any ongoing Read operations. $\overline{FF}$ is asserted during the last valid write as the MK4503 becomes full. Write operations begun with $\overline{FF}$ low are inhibited. $\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will again go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed (see Figure 4A). Writes beginning t_{FFW} after $\overline{FF}$ goes high are valid. Writes beginning after $\overline{FF}$ goes low and more than t_{WPI} before $\overline{FF}$ goes high are invalid (ignored). Writes beginning less than t_{WPI} before $\overline{FF}$ goes high and less than t_{FFW} later may or may not occur (be valid), depending on internal flag status.

FIGURE 3A. $\overline{W}$RITE AND FULL FLAG TIMING


LAST VALID WRITE
INVALID WRITE
INDETERMINANT WRITE
FIRST VALID WRITE
t_{WC}
t_{WPW}
t_{WR}
t_{WPW}
$\overline{W}$
t_{WFF}
t_{FFW}
t_{WPI}
$\overline{FF}$
NOT FULL
FULL
NOT FULL
FIRST VALID READ
t_{RFF}
$\overline{R}$
t_{DH}
t_{DS}
D_0-D_8
VALID DATA IN
VALID DATA IN
VALID DATA IN

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	65		80		100		120		140		175		235		ns	
t_{WPW}	Write Pulse Width	50		65		80		100		120		150		200		ns	1
t_{WR}	Write Recovery Time	15		15		20		20		20		25		35		ns	
t_{DS}	Data Set Up Time	30		30		40		40		40		50		65		ns	
t_{DH}	Data Hold Time	5		10		10		10		10		10		10		ns	
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low		45		60		70		95		115		145		195	ns	2
t_{FFW}	$\overline{FF}$ High to Valid Write	10		10		10		10		10		10		10		ns	2
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High		45		60		70		95		110		140		190	ns	2
t_{WPI}	Write Protect Indeterminant	35			35		35		35		35		35		35	ns	2

READ MODE

The MK4503 initiates a Read Cycle (see Figure 3B) on the falling edge of Read Enable control input ($\overline{R}$), provided that the Empty Flag ($\overline{EF}$) is not asserted. In the Read mode of operation, the MK4503 provides a fast access to data from 9 of 18432 locations in the static storage array. The data is accessed on a FIFO basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, data outputs will return to a high impedance condition until the next Read operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further Read operations will be inhibited (the data outputs will remain in high impedance). $\overline{EF}$ will go high t_{WEF} after completion of a valid Write operation. $\overline{EF}$ will again go low t_{REF} from the beginning a subsequent READ operation, provided that a second WRITE has not been completed (see Figure 4B). Reads beginning t_{EFR} after $\overline{EF}$ goes high are valid. Reads begun after $\overline{EF}$ goes low and more than t_{RPI} before $\overline{EF}$ goes high are invalid (ignored). Reads beginning less than t_{RPI} before $\overline{EF}$ goes high and less than t_{EFR} later may or may not occur (be valid) depending on internal flag status.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	65		80		100		120		140		175		235		ns	
t_A	Access Time		50		65		80		100		120		150		200	ns	2
t_{RR}	Read Recovery Time	15		15		20		20		20		25		35		ns	
t_{RPW}	Read Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RL}	$\overline{R}$ Low to Low Z	0		0		0		0		0		0		0		ns	2
t_{DV}	Data Valid from $\overline{R}$ High	5		5		5		5		5		5		5		ns	2
t_{RHZ}	$\overline{R}$ High to High Z		25		25		25		25		35		50		60	ns	2
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low		45		60		75		95		115		145		195	ns	2
t_{EFR}	$\overline{EF}$ High to Valid Read	10		10		10		10		10		10		10		ns	2
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High		45		60		75		95		110		140		190	ns	2
t_{RPI}	Read Protect Indeterminant		35		35		35		35		35		35		35	ns	2

FIGURE 3B. READ AND EMPTY FLAG TIMING

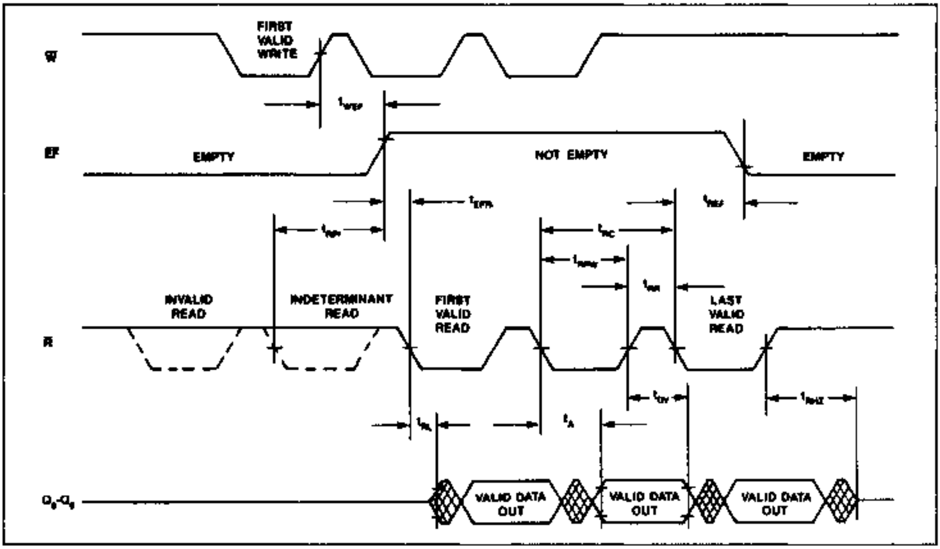

$\overline{W}$
FIRST VALID WRITE
t_{WEF}
$\overline{EF}$
EMPTY
NOT EMPTY
EMPTY
t_{EFR}
t_{REF}
t_{RPI}
t_{RC}
t_{RPW}
t_{RR}
INVALID READ
INDETERMINANT READ
FIRST VALID READ
LAST VALID READ
$\overline{R}$
t_{DV}
t_{RHZ}
t_{RL}
t_A
Q_0-Q_8
VALID DATA OUT
VALID DATA OUT
VALID DATA OUT

FIGURE 4A. READ/WRITE TO FULL FLAG

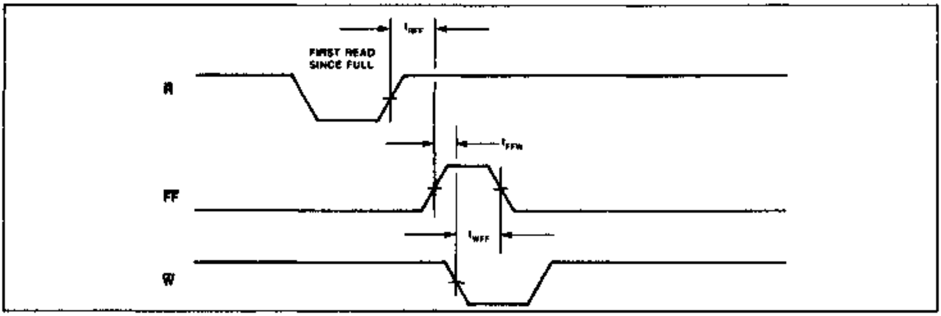
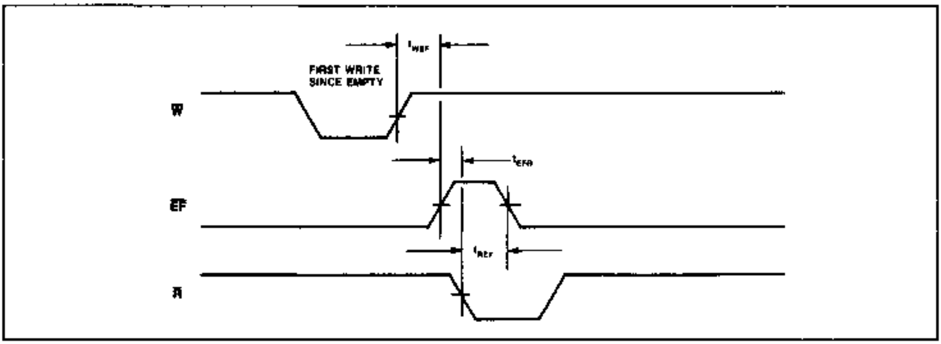

t_{RFF}
FIRST READ SINCE FULL
$\overline{R}$
t_{FFW}
$\overline{FF}$
t_{WFF}
$\overline{W}$

FIGURE 4B. WRITE/READ TO EMPTY FLAG

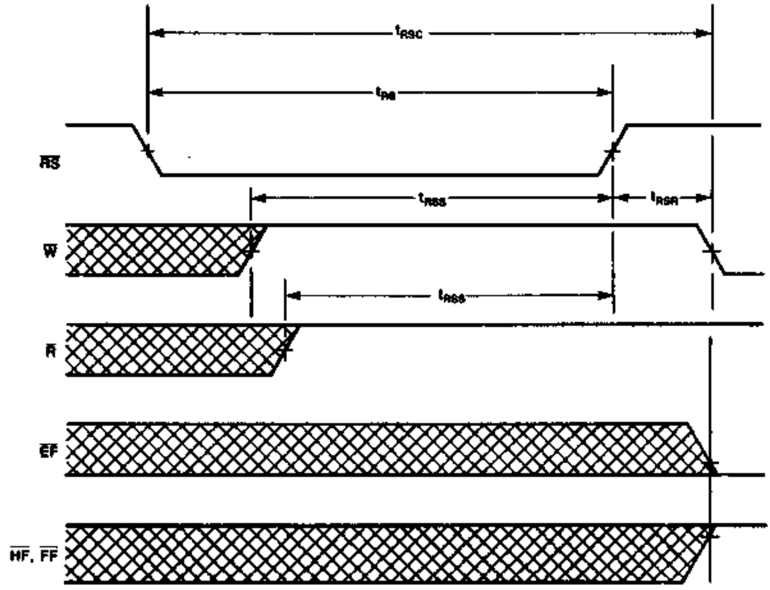

t_{WEF}
FIRST WRITE SINCE EMPTY
$\overline{W}$
t_{EFR}
$\overline{EF}$
t_{REF}
$\overline{R}$

RESET

The MK4503 is reset (see Figure 5) whenever the Reset pin ($\overline{RS}$) is in the low state. During a Reset, both the internal read and write pointers are set to the first location. Reset is required after power up, before a Write operation can begin.

Although neither $\overline{W}$ or $\overline{R}$ need be high when $\overline{RS}$ goes low, both $\overline{W}$ and $\overline{R}$ must be high t_{RSS} before $\overline{RS}$ goes high, and must remain high t_{RSR} afterwards. Refer to the following discussion for the required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$ during Reset.

FIGURE 5. RESET



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Reset, but flags will be valid at t_{RSC}.

AC ELECTRICAL CHARACTERISTICS

(0°C $\leq T_A \leq$ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RSC}	Reset Cycle Time	65		80		100		120		140		175		235		ns	
t_{RS}	Reset Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RSR}	Reset Recovery Time	15		15		20		20		20		25		35		ns	
t_{RSS}	Reset Set Up Time	30		45		60		80		100		130		180		ns	

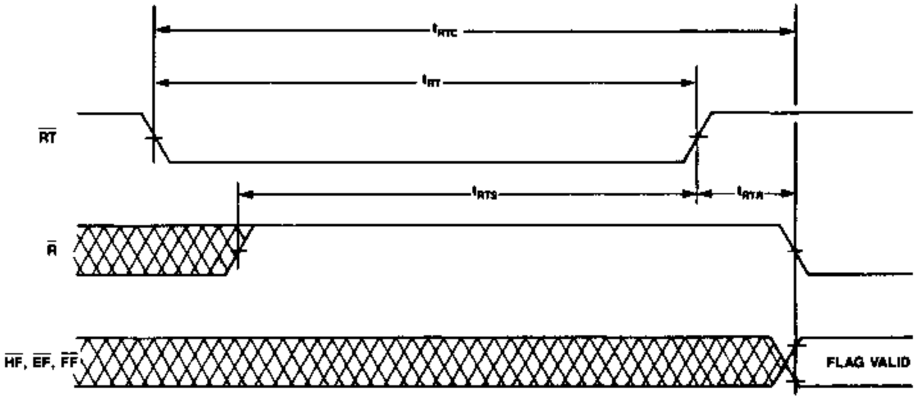
RETRANSMIT

The MK4503 can be made to retransmit (re-read previously read data) after the Retransmit pin ($\overline{RT}$) is pulsed low. (See Figure 6).

A Retransmit operation sets the internal read pointer to the first physical location in the array, but will not affect the position of the write pointer. $\overline{R}$ must be inactive t_{RTS} before $\overline{RT}$ goes high, and must remain high for t_{RTR} afterwards.

The Retransmit function is particularly useful when blocks of less than 2048 Writes are performed between Resets. The Retransmit feature is not compatible with Depth Expansion.

FIGURE 6. RETRANSMIT



NOTE
$\overline{HF}$, $\overline{EF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RTC}	Retransmit Cycle Time	65		80		100		120		140		175		235		ns	
t_{RT}	Retransmit Pulse Width	50		65		80		100		120		150		200		ns	1
t_{RTR}	Retransmit Recovery Time	15		15		20		20		20		25		35		ns	
t_{RTS}	Retransmit Setup Time	30		45		60		80		100		130		180		ns	

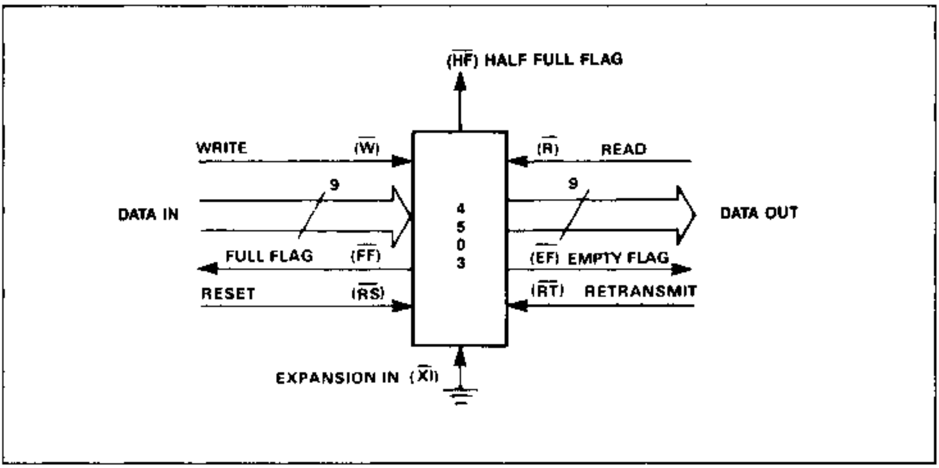
SINGLE DEVICE CONFIGURATION

A single MK4503 may be used when application requirements are for 2048 words or less. The MK4503 is placed in Single Device Configuration mode when the chip is Reset with the Expansion In pin ($\overline{XI}$) grounded (see Figure 7).

WIDTH EXPANSION

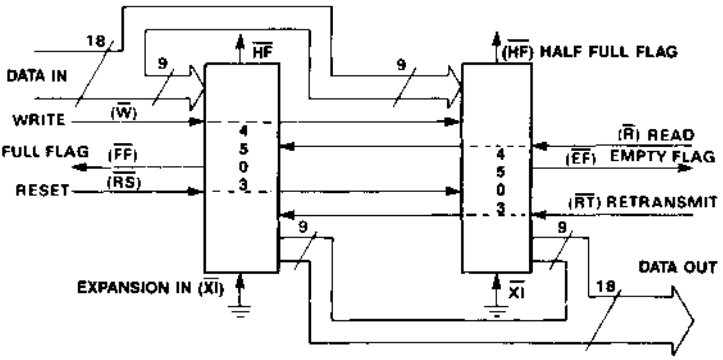
Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 8 demonstrates an 18-bit word width by using two MK4503s. Any word width can be attained by adding additional MK4503s. The half full flag ($\overline{HF}$) operates the same as in the single device configuration.

FIGURE 7. A SINGLE 2047 x 9 FIFO CONFIGURATION



($\overline{HF}$) HALF FULL FLAG
WRITE
($\overline{W}$)
($\overline{R}$)
READ
9
9
DATA IN
4503
DATA OUT
FULL FLAG
($\overline{FF}$)
($\overline{EF}$) EMPTY FLAG
RESET
($\overline{RS}$)
($\overline{RT}$)
RETRANSMIT
EXPANSION IN ($\overline{XI}$)

FIGURE 8. A 2048 x 18 FIFO CONFIGURATION (WIDTH EXPANSION)



18
DATA IN
9
$\overline{HF}$
9
($\overline{HF}$) HALF FULL FLAG
WRITE
($\overline{W}$)
FULL FLAG
($\overline{FF}$)
RESET
($\overline{RS}$)
4503
4503
($\overline{R}$) READ
($\overline{EF}$) EMPTY FLAG
($\overline{RT}$) RETRANSMIT
9
9
DATA OUT
18
EXPANSION IN ($\overline{XI}$)
$\overline{XI}$

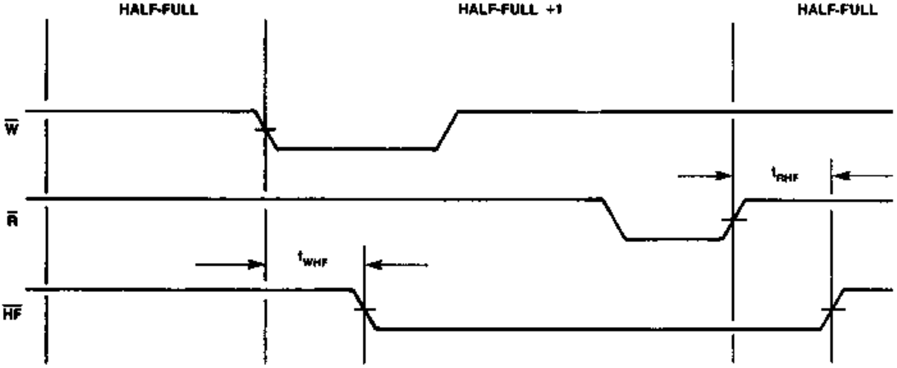
NOTE

Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect flag output signals together.

HALF FULL FLAG LOGIC

When in single device configuration, the ($\overline{HF}$) output acts as an indication of a half full memory. After half of the memory is filled, and at the falling edge of the next write operation, the half full flag ($\overline{HF}$) will be set low and remain low until the difference between the write pointer and read pointer is less than or equal to one half the total memory. The half full flag ($\overline{HF}$) is then reset by the rising edge of the read operation. See Figure 9.

FIGURE 9. HALF FULL FLAG TIMING



AC CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5 Volts ±10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WHF}	Write Low to Half Full Flag Low		65		80		100		120		140		175		235	ns	
t_{RHF}	Read High to Half Full Flag High		65		80		100		120		140		175		235	ns	

DEPTH EXPANSION (DAISY CHAIN)

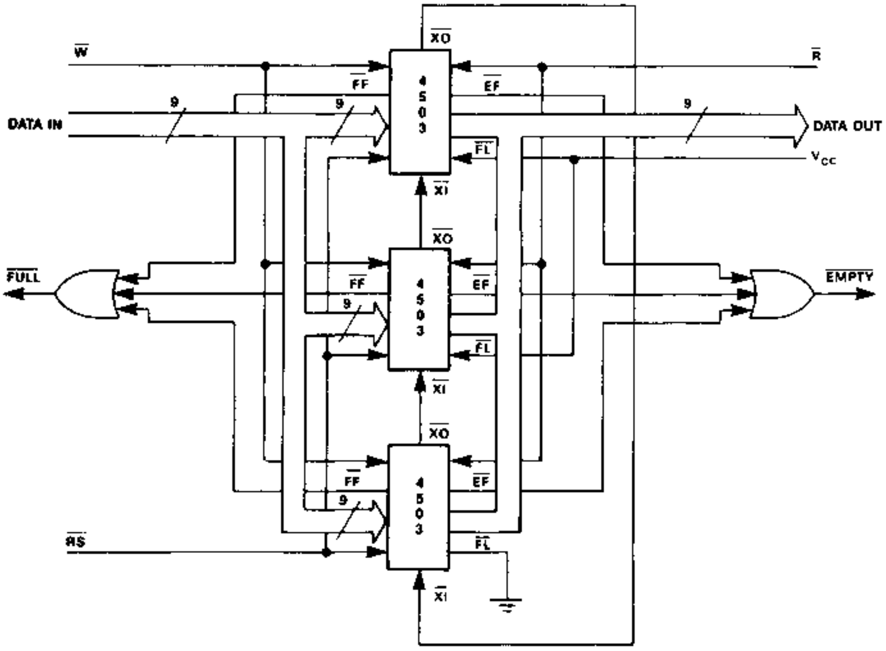
The MK4503 can easily be adapted to applications when the requirements are for greater than 2048 words. Figure 10 demonstrates Depth Expansion using three MK4503s. Any depth can be attained by adding additional MK4503s.

External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).

The MK4503 operates in the Depth Expansion configuration after the chip is Reset under the below listed conditions.

1. The first device must be designated by grounding the First Load pin ($\overline{FL}$). The Retransmit function is not allowed in the Depth Expansion Mode.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. The Half Full Flag ($\overline{HF}$) is disabled in this mode.

FIGURE 10. A 6K x 9 FIFO CONFIGURATION (DEPTH EXPANSION)

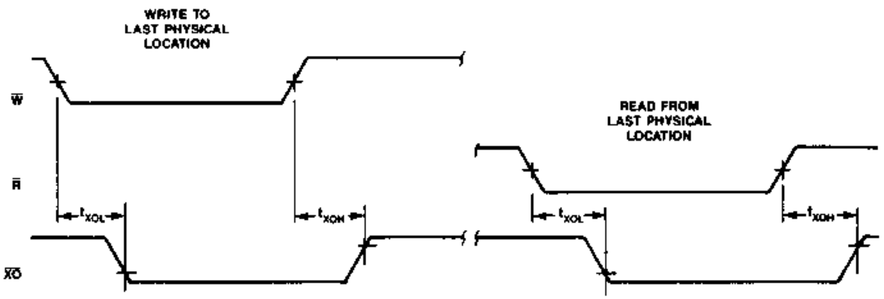

$\overline{W}$
$\overline{R}$
$\overline{XO}$
$\overline{FF}$
$\overline{EF}$
9
DATA IN
DATA OUT
4503
$\overline{FL}$
V_{CC}
$\overline{XI}$
$\overline{FULL}$
$\overline{EMPTY}$
$\overline{RS}$

EXPANSION TIMING

Figures 11 and 12 illustrate the timing of the Expansion Out and Expansion In signals. Discussion of Expansion Out/Expansion In timing is provided to clarify how Depth Expansion works. Inasmuch as Expansion Out pins are generally connected only to Expansion In pins, the user need not be concerned with actual timing in a normal Depth Expanded application unless extreme propagation delays exist between the $\overline{XO}/\overline{XI}$ pin pairs.

Expansion Out pulses are the image of the WRITE and READ signals that cause them; delayed in time by t_{XOL} and t_{XOH}. The Expansion Out signal is propagated when the last physical location in the memory array is written and again when it is read (Last Read). This is in contrast to when the Full and Empty Flags are activated, which is in response to writing and reading a last available location.

FIGURE 11. EXPANSION OUT TIMING



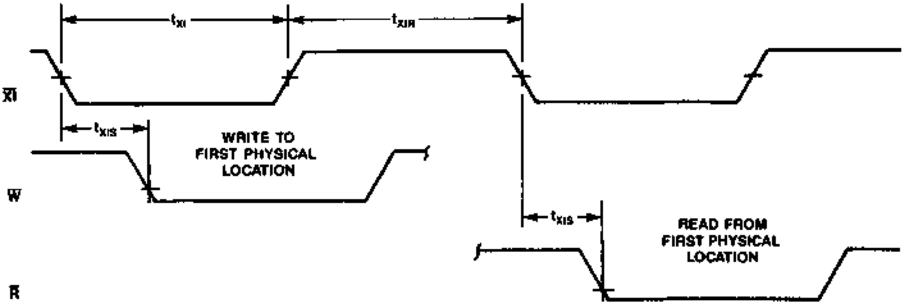
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XOL}	Expansion Out Low		40		55		70		75		90		115		150	ns	
t_{XOH}	Expansion Out High		45		60		80		90		100		125		155	ns	

When in Depth Expansion mode, a given MK4503 will begin writing and reading as soon as valid WRITE and READ signals begin, provided $\overline{FL}$ was grounded at RESET time. A MK4503 in Depth Expansion mode with $\overline{FL}$ high at RESET will not begin writing until after an Expansion In pulse occurs. It will not begin reading until a second Expansion In pulse occurs and the Empty Flag has gone high. Expansion In pulses must occur t_{XIS} before the WRITE and READ signals they are intended to enable. Minimum Expansion In pulse width, t_{XI}, and recovery time, t_{XIR}, must be observed.

FIGURE 12. EXPANSION IN TIMING


t_{XI}
t_{XIR}
$\overline{XI}$
t_{XIS}
WRITE TO FIRST PHYSICAL LOCATION
$\overline{W}$
t_{XIS}
READ FROM FIRST PHYSICAL LOCATION
$\overline{R}$

AC ELECTRICAL CHARACTERISTICS

(0°C $\leq T_A \leq$ +70°C) (V_{CC} = +5.0 volts ± 10%)

		4503-50		4503-65		4503-80		4503-10		4503-12		4503-15		4503-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{XI}	Expansion In Pulse Width	45		60		75		95		115		145		195		ns	1
t_{XIR}	Expansion In Recovery Time	15		15		20		20		20		25		35		ns	
t_{XIS}	Expansion In Setup Time	20		25		30		45		50		60		85		ns	

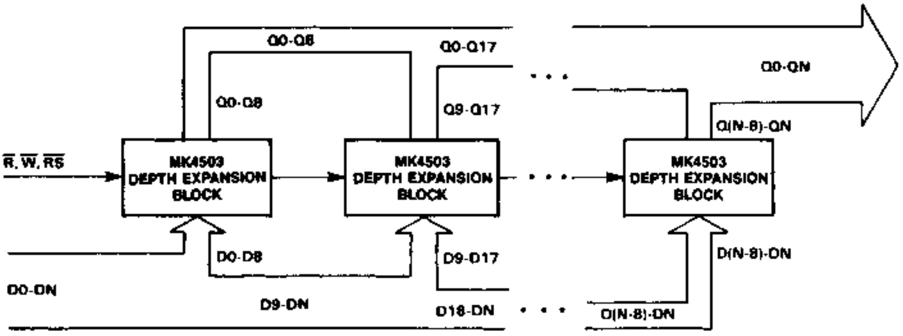
COMPOUND EXPANSION

The two expansion techiques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 13).

BIDIRECTIONAL APPLICATIONS

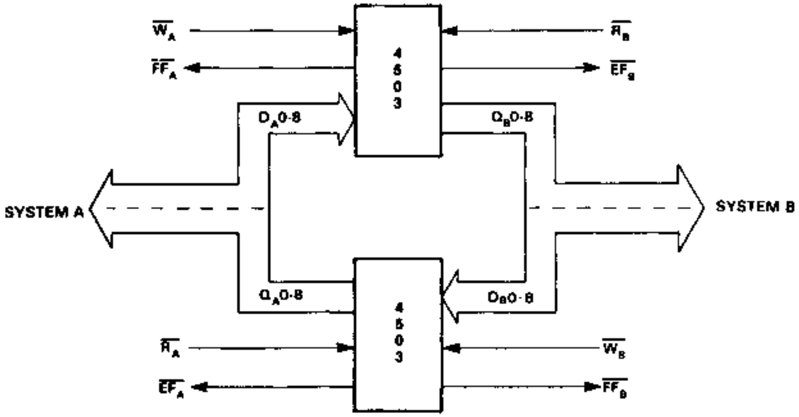
Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4503s, as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

FIGURE 13. COMPOUND FIFO EXPANSION


Q0-Q8
Q0-Q17
Q0-QN
Q0-Q8
Q9-Q17
Q(N-8)-QN
$\overline{R}$, $\overline{W}$, $\overline{RS}$
MK4503 DEPTH EXPANSION BLOCK
MK4503 DEPTH EXPANSION BLOCK
MK4503 DEPTH EXPANSION BLOCK
D0-D8
D9-D17
D(N-8)-DN
D0-DN
D9-DN
D18-DN
D(N-8)-DN

NOTES
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag operation see WIDTH EXPANSION Section and Figure 8.

FIGURE 14. BIDIRECTIONAL FIFO APPLICATION


$\overline{W_A}$
$\overline{FF_A}$
4503
$\overline{R_B}$
$\overline{EF_B}$
D_A0-8
Q_B0-8
SYSTEM A
SYSTEM B
Q_A0-8
D_B0-8
4503
$\overline{R_A}$
$\overline{EF_A}$
$\overline{W_B}$
$\overline{FF_B}$

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND .... -0.5 V to + 7.0 V
Operating Temperature T_A (Ambient) .... 0°C to + 70°C
Storage Temperature .... -55°C to + 125°C
Total Device Power Dissipation .... 1 Watt
Output Current per Pin .... 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + .3	V	3,9
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	3, 4, 9

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	3
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	3
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	7
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL}/\overline{RT} = V_{IH}$)		12	mA	7
I_{CC3}	Power Down Current (All Inputs ≥ V_{CC} -0.2 V)		4	mA	7

AC ELECTRICAL CHARACTERISTICS

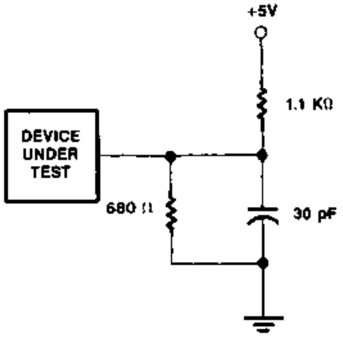
($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_Q	Capacitance on Output Pins		12 pF	8

NOTES

1. Pulse widths less than minimum values are not allowed.
2. Measured using output load shown in Output Load Diagram.
3. All voltages are referenced to ground.
4. −1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.0 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.0 \geq V_{OUT} \leq V_{CC}$.
7. I_{CC} measurements are made with outputs open.
8. With output buffer deselected.
9. Input levels tested at 500 ns cycle time.

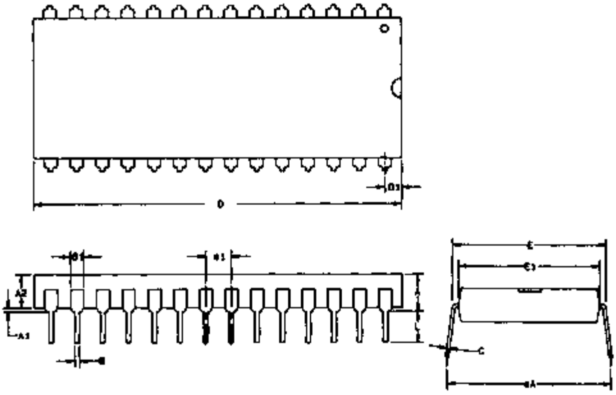
FIGURE 15. OUTPUT LOAD



AC TEST CONDITIONS:

Input Levels .... GND to 3.0 V
Transition Times .... 5 ns
Input Signal Timing Reference Level .... 1.5 V
Output Signal Timing Reference Level 0.8 V and 2.2 V
Ambient Temperature .... 0°C to 70°C
V_{CC} .... 5.0 V ± 10%

FIGURE 16. MK4503 PLASTIC (N TYPE) DUAL-IN-LINE, 28 PINS

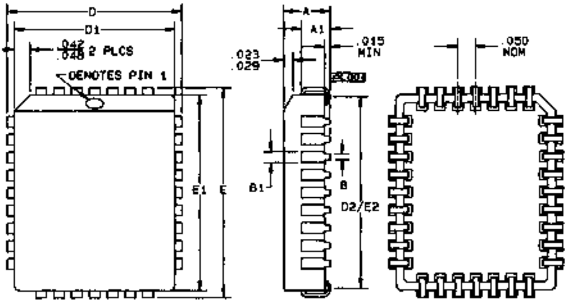


Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.534	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

FIGURE 17. MK4503 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

ORDERING INFORMATION

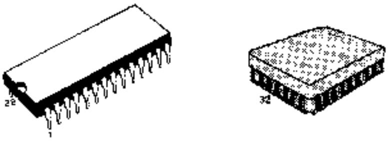
PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK4503N-50	50 ns	65 ns	15.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-65	65 ns	80 ns	12.5 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-80	80 ns	100 ns	10.0 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-10	100 ns	120 ns	8.3 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-12	120 ns	140 ns	7.1 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-15	150 ns	175 ns	5.7 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503N-20	200 ns	235 ns	4.2 MHz	28 Pin Plastic DIP	0° to 70°C
MK4503K-50	50 ns	65 ns	15.3 MHz	32 Pin PLCC	0° to 70°C
MK4503K-65	65 ns	80 ns	12.5 MHz	32 Pin PLCC	0° to 70°C
MK4503K-80	80 ns	100 ns	10.0 MHz	32 Pin PLCC	0° to 70°C
MK4503K-10	100 ns	120 ns	8.3 MHz	32 Pin PLCC	0° to 70°C
MK4503K-12	120 ns	140 ns	7.1 MHz	32 Pin PLCC	0° to 70°C
MK4503K-15	150 ns	175 ns	5.7 MHz	32 Pin PLCC	0° to 70°C
MK4503K-20	200 ns	235 ns	4.2 MHz	32 Pin PLCC	0° to 70°C

SGS-THOMSON
MICROELECTRONICS

MK4511(N,K)-12/15/20

512 × 8 CMOS BiPORT™ RAM

- SINGLE CHIP BI-DIRECTIONAL MESSAGE PASSING
- SOFTWARE CONTROLLED INTERRUPT OUTPUTS
- ADDRESSABLE STATUS/CONTROL FLAGS
- IDENTICAL PORTS, 3-WIRE CONTROLLED I/O



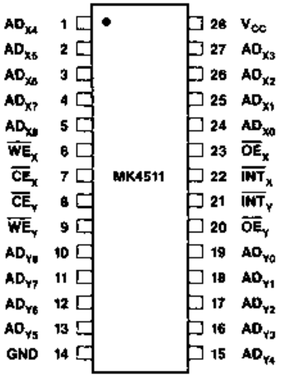
N
DIP-28
(Plastic Dip)

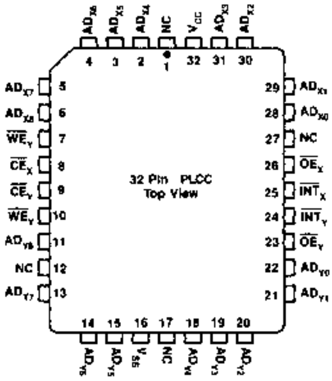
K
PLCC32
(Plastic Chip Carrier)

PIN NAMES

AD - Address/Data I/O	$\overline{\text{INT}}$ - Interrupt Output
$\overline{\text{CE}}$ - Chip Enable	GND - Ground
$\overline{\text{OE}}$ - Output Enable	V_{CC} - +5 Volts
$\overline{\text{WE}}$ - Write Enable	NC - No Connection

Part Number	Access Time	Cycle Time	Cycle Rate
MK4511-12	120 ns	150 ns	6.67 MHz
MK4511-15	150 ns	190 ns	5.26 MHz
MK4511-20	200 ns	250 ns	4.00 MHz


AD_{X4} 1
AD_{X5} 2
AD_{X6} 3
AD_{X7} 4
AD_{X8} 5
$\overline{WE}_X$ 6
$\overline{CE}_X$ 7
$\overline{CE}_Y$ 8
$\overline{WE}_Y$ 9
AD_{Y8} 10
AD_{Y7} 11
AD_{Y6} 12
AD_{Y5} 13
GND 14
MK4511
28 V_{CC}
27 AD_{X3}
26 AD_{X2}
25 AD_{X1}
24 AD_{X0}
23 $\overline{OE}_X$
22 $\overline{INT}_X$
21 $\overline{INT}_Y$
20 $\overline{OE}_Y$
19 AD_{Y0}
18 AD_{Y1}
17 AD_{Y2}
16 AD_{Y3}
15 AD_{Y4}


AD_{X6} 4
AD_{X5} 3
AD_{X4} 2
NC 1
V_{CC} 32
AD_{X3} 31
AD_{X2} 30
AD_{X7} 5
AD_{X8} 6
$\overline{WE}_Y$ 7
$\overline{CE}_X$ 8
$\overline{CE}_Y$ 9
$\overline{WE}_Y$ 10
AD_{Y8} 11
NC 12
AD_{Y7} 13
32 Pin PLCC
Top View
29 AD_{X1}
28 AD_{X0}
27 NC
26 $\overline{OE}_X$
25 $\overline{INT}_X$
24 $\overline{INT}_Y$
23 $\overline{OE}_Y$
22 AD_{Y0}
21 AD_{Y1}
14 AD_{Y6}
15 AD_{Y5}
16 V_{SS}
17 NC
18 AD_{Y4}
19 AD_{Y3}
20 AD_{Y2}

DESCRIPTION

The MK4511 dual port RAM contains a single 512 x 9 CMOS memory matrix that can be accessed simultaneously from both of the input/output ports. Dual port operation is achieved through the use of a memory array composed of BiPORT memory cells. Each memory cell is accessible from both ports at all times.

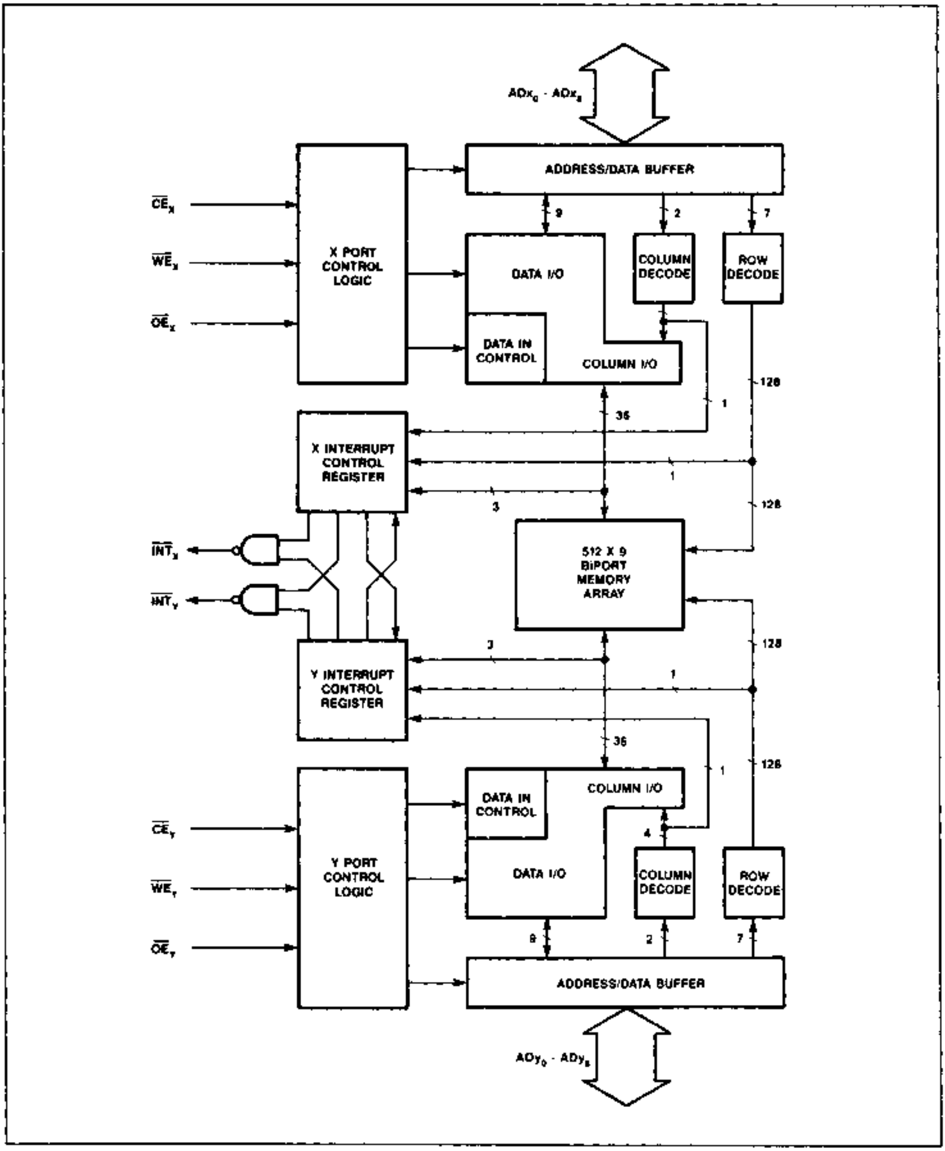
Pin count is kept low through the use of address/data multiplexing. This technique is being used on advanced microprocessors and other devices to keep pin counts and package sizes down.

The MK4511 incorporates all functions required for dual port operations, including software controlled interrupt outputs. Use of the interrupt outputs is optional, allowing both polled and interrupt controlled applications.

SINGLE PORT OPERATIONS

The MK4511 may be viewed from either port as an ordinary three wire controlled 512 x 9 static RAM. Timing of read and write operations is altogether conventional; the presence of the other port is effectively transparent to the accessing processor. Therefore, all timing parameters are specified without references that differentiate between the ports.

FIGURE 2. MK4511 BLOCK DIAGRAM

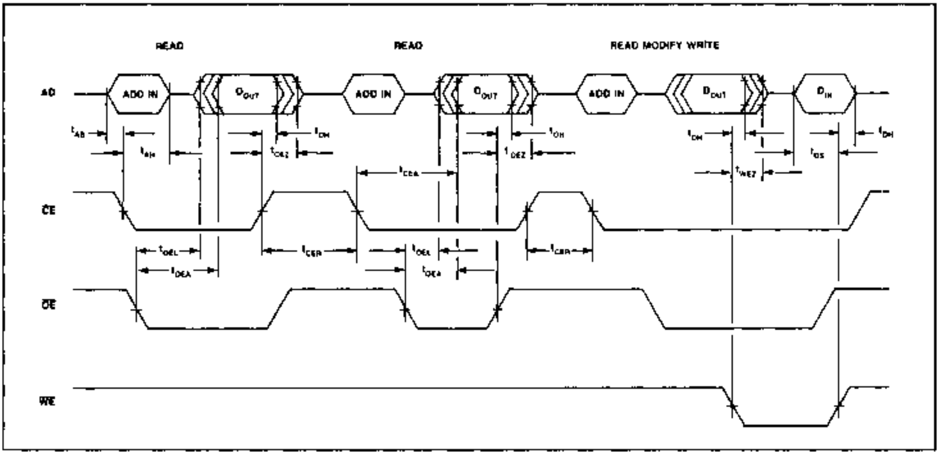

AD_{x_0} - AD_{x_8}
ADDRESS/DATA BUFFER
9
2
7
$\overline{CE}_X$
$\overline{WE}_X$
$\overline{OE}_X$
X PORT CONTROL LOGIC
DATA I/O
COLUMN DECODE
ROW DECODE
DATA IN CONTROL
COLUMN I/O
128
1
36
X INTERRUPT CONTROL REGISTER
1
3
128
$\overline{INT}_X$
$\overline{INT}_Y$
512 X 9 BIPORT MEMORY ARRAY
3
128
1
Y INTERRUPT CONTROL REGISTER
36
1
128
DATA IN CONTROL
COLUMN I/O
4
$\overline{CE}_Y$
$\overline{WE}_Y$
$\overline{OE}_Y$
Y PORT CONTROL LOGIC
DATA I/O
COLUMN DECODE
ROW DECODE
9
2
7
ADDRESS/DATA BUFFER
AD_{y_0} - AD_{y_8}

READ MODE

The MK4511 is in Read Mode whenever Chip Enable ($\overline{CE}$) is low and Write Enable ($\overline{WE}$) is high. A stable address must be placed onto the AD lines t_{AS} prior to Chip Enable becoming active. The address must be held valid for t_{AH} following the falling edge of $\overline{CE}$.

In Read Mode the bi-directional AD lines are driven alternately by the user and the MK4511. Bus contention will occur if the user's address driver remains active too long. An Output Enable input ($\overline{OE}$) is provided, offering an improved ability to avoid bus contention. The $\overline{OE}$ control keeps the AD lines in a high impedance state while held high and for t_{OEL} after it goes low. Output data will be valid at the latter of t_{OEA} or t_{CEA}. A Chip Enable recovery time (t_{CER}) must be observed between assertions of $\overline{CE}$.

FIGURE 3. READ-READ-READ MODIFY WRITE



READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0$ V ± 10 percent)

SYM	PARAMETERS	MK4511-12 MIN	MK4511-12 MAX	MK4511-15 MIN	MK4511-15 MAX	MK4511-20 MIN	MK4511-20 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		190		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AH}	Address Hold Time	20		25		35		ns	
t_{CEA}	Chip Enable Access Time		120		150		200	ns	1
t_{OEL}	Output Enable to Lo-Z	15		15		15		ns	
t_{OEA}	Output Enable Access Time		55		70		90	ns	1
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable Hi to Hi-Z		90		110		150	ns	
t_{OEZ}	Output Enable Hi to Hi-Z		40		50		65	ns	
t_{WEZ}	Write Enable Lo to Hi-Z		40		50		65	ns	
t_{CER}	Chip Enable Recovery Time	30		40		50		ns	

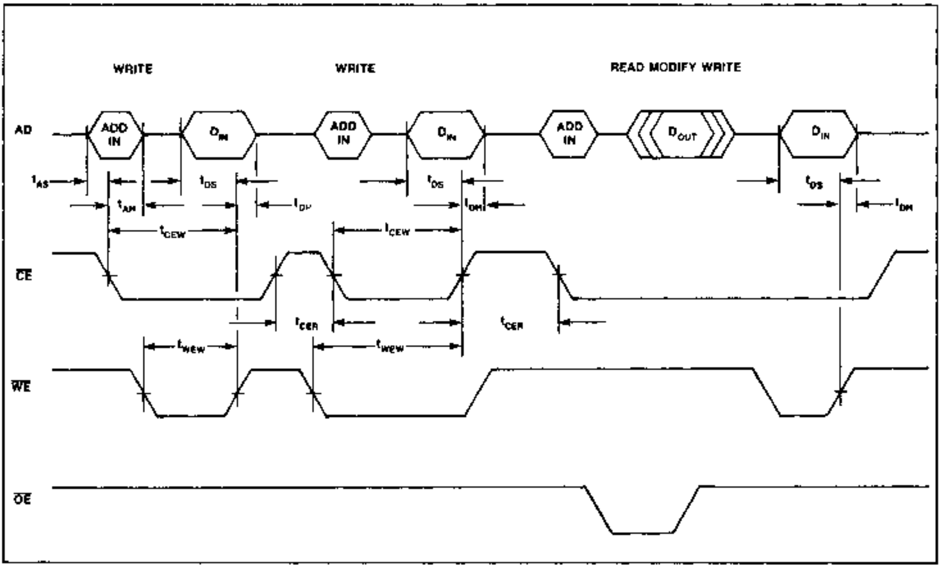
WRITE MODE

The MK4511 is in Write Mode whenever Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) are active low. As in Read Mode, the falling edge of $\overline{CE}$ latches the addresses present at the AD lines. The same addresses set-up and hold times apply. Input to the AD pins must then change from the address to input data. Input data present on the AD lines must be stable for t_{DS} prior to the end of write and must remain valid for t_{DH} afterward. A write cycle may be ended by the rising edge of $\overline{WE}$ or $\overline{CE}$. Chip Enable recovery time must also be observed in write mode.

Even if $\overline{WE}$ becomes active prior to $\overline{CE}$ becoming active, $\overline{CE}$ falling actually begins the cycle, latching the address present on the AD lines. Such cycles must reference t_{WEW}, t_{DS} and t_{DH} to the rising and falling edges of $\overline{CE}$ and $\overline{WE}$.

Read-Modify-Write cycles are possible if the outputs are enabled and the assertion of $\overline{WE}$ is delayed through t_{CEA}. The write cycle will begin when $\overline{WE}$ goes low. $\overline{WE}$ going low or $\overline{OE}$ going high will return the output drivers to high-Z within t_{WEZ} or t_{OEZ} respectively. The address latched when $\overline{CE}$ went low is still the valid address as the write cycle proceeds. The cycle is ended by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

FIGURE 4. WRITE-WRITE-READ MODIFY WRITE



WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	150		190		250		ns	
t_{CEW}	Chip Enable to End of Write	120		150		200		ns	
t_{WEW}	Write Enable to End of Write	80		105		130		ns	
t_{DS}	Data Setup Time	40		55		65		ns	
t_{DH}	Data Hold Time	10		10		10		ns	

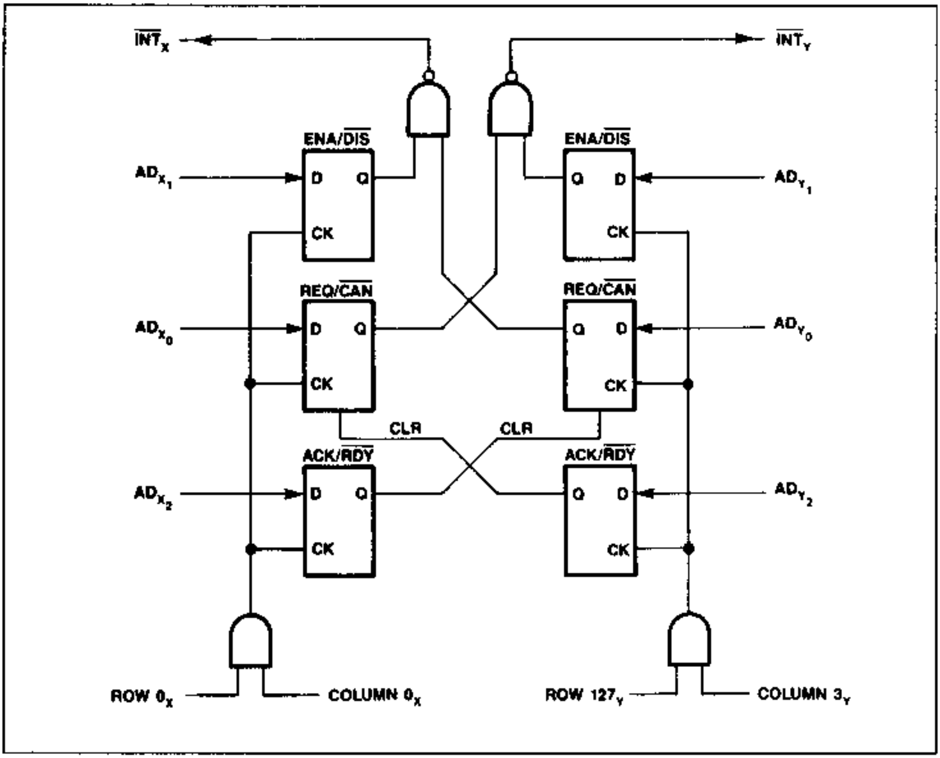
DUAL PORT OPERATIONS

INTERRUPT CONTROL

Although the Interrupt Control Registers for each port are accessed in parallel with RAM locations 000_H and $1FF_H$, they do not reside within the RAM array. They do not derive their control inputs from the RAM cells' status. In fact, changing the RAM location's contents via an opposite port will not affect a Interrupt Control Register at all. Therefore, for example, Port Y writing to address 000_H cannot affect the status of the Port X Interrupt Register.

The lower three bits of each byte written to the top and bottom addresses are the ones routed simultaneously to the Interrupt Control Registers. The Interrupt Control Registers consists of three flip-flops per port that serve as the Interrupt Request/Cancel flag (REQ/$\overline{\text{CAN}}$), Interrupt Output Enable/Disable flag (ENA/$\overline{\text{DIS}}$) and Interrupt Acknowledge/Ready flag (ACK/$\overline{\text{RDY}}$). As Figure 5 shows, the logic attached to the Interrupt Control Registers interprets interrupt status and drives the Interrupt Outputs.

FIGURE 5. MK4511 INTERRUPT CONTROL REGISTERS AND INTERRUPT LOGIC


$\overline{\text{INT}}_X$
$\overline{\text{INT}}_Y$
ENA/$\overline{\text{DIS}}$
ENA/$\overline{\text{DIS}}$
AD_{X_1}
D
Q
CK
Q
D
CK
AD_{Y_1}
REQ/$\overline{\text{CAN}}$
REQ/$\overline{\text{CAN}}$
AD_{X_0}
D
Q
CK
Q
D
CK
AD_{Y_0}
CLR
CLR
ACK/$\overline{\text{RDY}}$
ACK/$\overline{\text{RDY}}$
AD_{X_2}
D
Q
CK
Q
D
CK
AD_{Y_2}
ROW 0_X
COLUMN 0_X
ROW 127_Y
COLUMN 3_Y

INTERRUPT BYTE STRUCTURE

Because only the lower 3 bits of each interrupt byte are used to control the interrupt logic, the six MSBs written to the RAM have no affect on the state of the interrupt outputs, and may be used for any other purpose. The functions of the three control bits are:

Interrupt Output Enable/Disable
ENA/$\overline{\text{DIS}}_X$ (AD_{X1}) and ENA/$\overline{\text{DIS}}_Y$ (AD_{Y1})

Each port can disable its own interrupt outputs by writing a 0 ($XXXXXXX0X_2$) into its ENA/$\overline{\text{DIS}}$ bit. If disabled, the interrupt pin will remain high regardless of interrupt requests from the other port. If an interrupt is requested of a disabled port, and an enabling 1 is later written into ENA/$\overline{\text{DIS}}$ of the disabled port, the interrupt output will go low t_{WIL} following the rising edge of the enabling write. Disabling a port with an active interrupt output pin will result in the output going high t_{WIH} after the end of the disabling write.

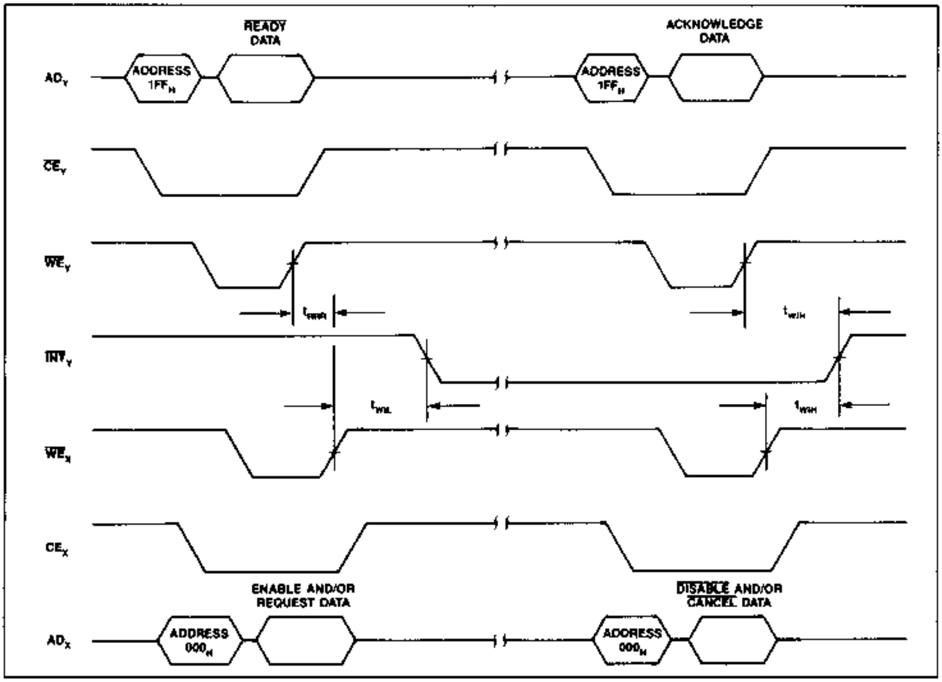
Interrupt Request/Cancel REQ/$\overline{\text{CAN}}_X$ (AD_{X0}) and REQ/$\overline{\text{CAN}}_Y$ (AD_{Y0})

Assuming that the Enable and Ready flags are set, writing a 1 into a REQ/$\overline{\text{CAN}}$ bit drives an enabled interrupt output pin on the opposite port low. The interrupt line will be driven low t_{WIL} following the end of the write that places a 1 in the REQ/$\overline{\text{CAN}}$ bit. For example, when $XXXXXXX1_2$ is written into location 000_H setting REQ/$\overline{\text{CAN}}_X$, $\overline{\text{INT}}_Y$ will go active low within t_{WIL}. Writing a 0 into the REQ/$\overline{\text{CAN}}$ bit cancels the interrupt request, returning the $\overline{\text{INT}}$ output to a high state t_{WIH} after the end of write.

Interrupt Acknowledge/Ready ACK/$\overline{\text{RDY}}_X$ (AD_{X2}) and ACK/$\overline{\text{RDY}}_Y$ (AD_{Y2})

Once an interrupt has been received at a port, the interrupt can be turned off by writing a 1 ($XXXXX1XX_2$) into the ACK/$\overline{\text{RDY}}$ bit of the receiving port. Writing an acknowledge will cause the interrupt output to go high t_{WIH} after the end of the write. The interrupt request flag cannot be set while the acknowledge flag is active. An acknowledge must always be followed with a ready (writing a 0 over the 1) before requests from the other port can be recognized. Interrupt requests can be recognized t_{RRR} after a ready.

FIGURE 6. INTERRUPT REQUEST TIMING


READY DATA
ACKNOWLEDGE DATA
AD_Y
ADDRESS 1FF_H
ADDRESS 1FF_H
$\overline{\text{CE}}_Y$
$\overline{\text{WE}}_Y$
t_RRR
t_WIH
$\overline{\text{INT}}_Y$
t_WIL
t_WIH
$\overline{\text{WE}}_X$
CE_X
ENABLE AND/OR REQUEST DATA
DISABLE AND/OR CANCEL DATA
AD_X
ADDRESS 000_H
ADDRESS 000_H

INTERRUPT OUTPUT TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12 MIN	MK4511-12 MAX	MK4511-15 MIN	MK4511-15 MAX	MK4511-20 MIN	MK4511-20 MAX	UNITS	NOTES
t_{WIL}	End of Write to $\overline{\text{INT}}$ Low		50		60		85	ns	
t_{WIH}	End of Write to $\overline{\text{INT}}$ High		50		60		85	ns	
t_{RRR}	Ready to Request Recognized		10		10		15	ns	

IMPLEMENTATION

Use of the interrupt feature is completely optional, allowing simple implementation of either interrupt driven or polled inter-processor communications applications. Either port can read or write any of the 512 bytes without restriction. Users who choose not to utilize the interrupt feature should leave the interrupt pins unconnected.

Any inter-processor communications application will doubtless employ some type of semaphore scheme. The use of the REQ/$\overline{\text{CAN}}$, ENA/$\overline{\text{DIS}}$ and ACK/$\overline{\text{RDY}}$ bits allow for each port to follow the exact status of the other port. The following example covers the case of port X interrupting port Y but applies equally well for port Y interrupting port X.

An Example Approach to Inter-processor Communications Using Pre-Allocated Memory Blocks and Interrupts

Pre-define six memory blocks of 85 bytes each (for a total of 510 bytes). Assign some number of blocks (probably three) to the X port and the balance to the Y port. Each port will write only to its assigned memory blocks, preventing port X and port Y attempting to load their messages into the same area.

Write the message to be passed into the Port X message area. When finished, read ACK/$\overline{\text{RDY}}_Y$. If ready, request an interrupt on port Y by writing a 1 into REQ/$\overline{\text{CAN}}_X$. Indicate which message block(s) contain valid message data, using the upper six bits of the interrupt register byte.

Now, acknowledge the interrupt to Port Y by writing a 1 to the acknowledge flag on Port Y. Begin reading the message via Port Y. The acknowledge should not be removed until after the message has been read. When it has been, set the ACK/$\overline{\text{RDY}}_Y$ flag to ready.

Check to see that the message was received. Monitor ACK/$\overline{\text{RDY}}_Y$ via Port X. Changes to the message block should not be made by Port X until ACK/$\overline{\text{RDY}}_Y$ is zero, indicating Port Y has finished reading its message.

COLLISION

The central objective of the MK4511 design effort was to produce a component that makes implementation of asynchronous, random access dual port memory applications, that can assure data integrity, as simple and inexpensive to design and implement as possible.

Data integrity can be called into question if port to port collision occurs. A collision is defined as both ports attempting to write at the same address or one port reading and one writing at the same address at the same time.

While a collision is generally considered undesirable, the conditions that can lead to ill-defined results are definable and manageable. In the case of a write/write collision, the data stored at the address in question may or may not have any similarity to either write attempted or the previously resident data if the delay between the ends of the writes (t_{WWL})is not long enough. On the other hand, write/read collisions do not affect the integrity of data storage, but do have an impact on the validity of output data at definable points in time (t_{ODI} and t_{ODV}). Figures 7 and 8 describe these conditions.

All of the parameters indicated reference the validity of the entire byte of data. Individual bits of a byte change state at slightly different rates. Though this is a subtle distinction, it is nonetheless important, particularly in the case of monitoring ACK/$\overline{\text{RDY}}$. Be aware that a read may catch the ready bit at a valid zero before the rest of the byte has finished transition. Nevertheless, because there is no reason for the ready bit to go low, other than that the opposite port is writing a zero into it, catching it low is a reliable indication that the other port is ready. This is all to say that single significant bit flag write/read operations can proceed reliably under collision conditions where byte wide operations cannot.

Simultaneous reads at the same address will always produce valid data and are therefore not considered a collision in this context.

FIGURE 7. MINIMUM WRITE TO WRITE LATENCY FOR VALID DATA STORAGE

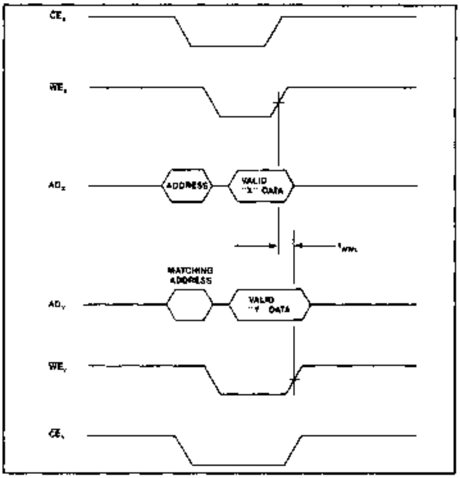
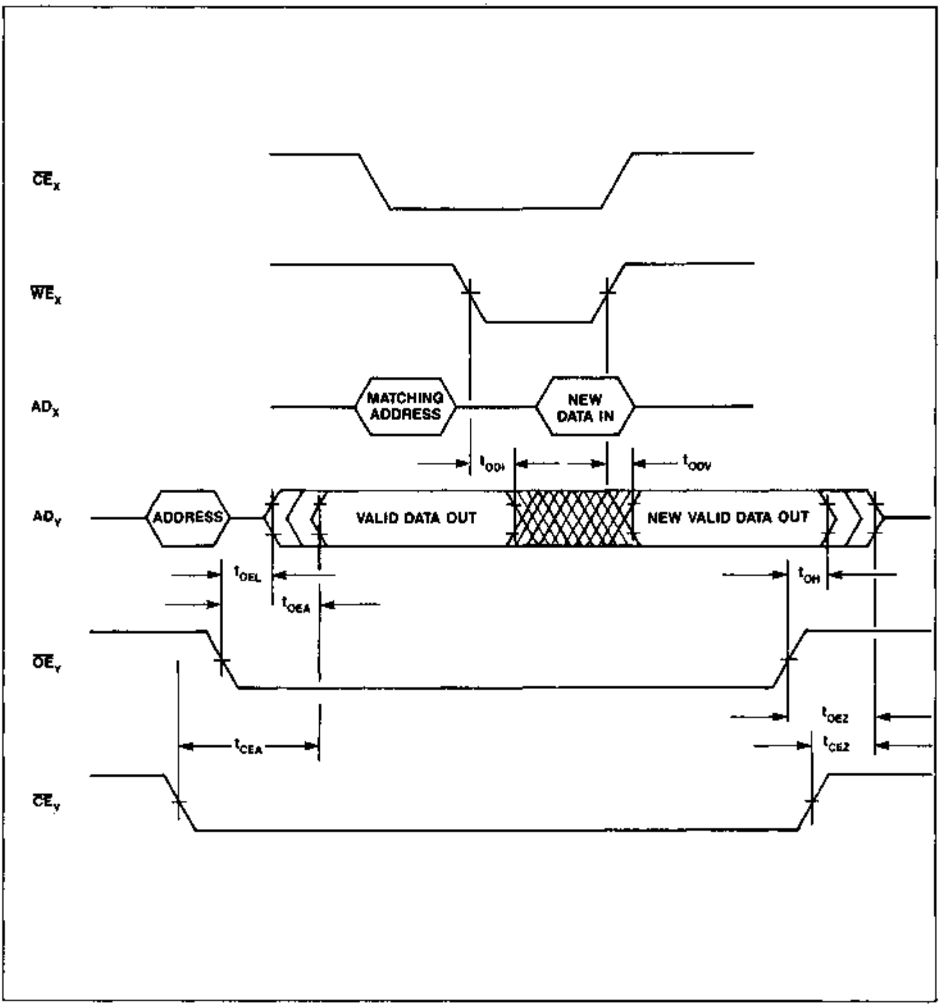


FIGURE 8. SIMULTANEOUS READ WRITE TIMING


$\overline{CE}_X$
$\overline{WE}_X$
AD_X
MATCHING ADDRESS
NEW DATA IN
t_{ODI}
t_{ODV}
AD_Y
ADDRESS
VALID DATA OUT
NEW VALID DATA OUT
t_{OEL}
t_{OEA}
t_{OH}
$\overline{OE}_Y$
t_{OEZ}
t_{CEA}
t_{CEZ}
$\overline{CE}_Y$

COLLISION TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{ODI}	Output Data Indeterminant	10		10		10		ns	
t_{ODV}	Output Data Valid		90		115		150	ns	
t_{WWL}	Write to Write Latency	80		105		130		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND	−0.3 V to +7.0 V
Ambient Operating Temperature (T_A)	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	20 mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 0.3	V	2,3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	2,3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current per Port		25	mA	4
I_{CC2}	TTL Standby Current per Port		2.5	mA	5
I_{CC3}	CMOS Standby Current per Port		1	mA	6
I_{IL}	Input Leakage Current	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−5	+5	μA	7
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	2
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 2.1 mA)		0.4	V	2

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETERS	TYP	UNITS	NOTES
C_I	Capacitance on any Input Pin	4	pF	8
C_O	Capacitance on any Output Pin	10	pF	8,9

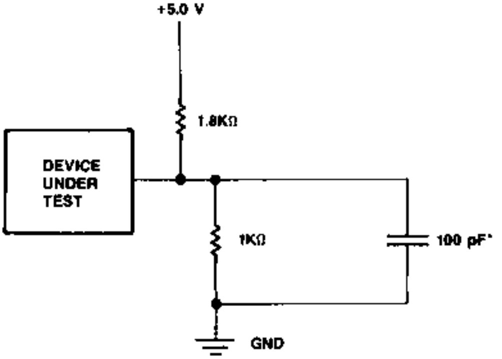
NOTES

1. Measured with load shown in Figure 9.
2. All voltages referenced to GND.
3. No more than one negative undershoot or positive overshoot of 1.5 V with a maximum pulse width of 10 ns is allowed once per cycle.
4. Output buffer is deselected, both ports are active.
5. All inputs = V_{IH}.
6. All inputs $\geq V_{CC} - 0.2V$
7. Measured with $GND \leq V_I \leq V_{CC}$ and outputs deselected.
8. Effective capacitance is calculated as follows: $C = \frac{\Delta Q}{\Delta V}$ $\Delta V = 3$ V
9. Output buffer is deselected.

AC TEST CONDITIONS

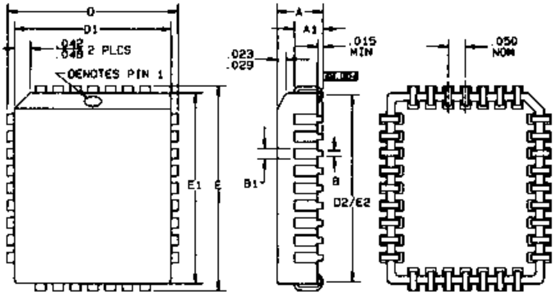
Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Levels	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 9. EQUIVALENT OUTPUT LOAD CIRCUIT


+5.0 V
1.8KΩ
DEVICE UNDER TEST
1KΩ
100 pF*
GND

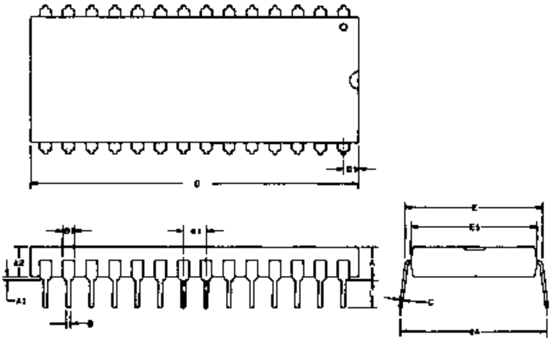
* INCLUDES SCOPE AND TEST JIG.

FIGURE 10. MK4511 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)


D
D1
.042
.048 2 PLCS
DENOTES PIN 1
E1
E
A
A1
.015
MIN
.023
.029
B1
B
D2/E2
.050
NOM

Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

FIGURE 11. MK4511 28 PIN PLASTIC DIP (N TYPE)



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	–	5.334	–	210	2
A1	0.381	–	.015	–	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	012	3
D	36.576	37.338	1.440	1 470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13 462	14.224	.530	.560	
e1	2.286	2.794	.090	110	
eA	15.24	17.78	.600	700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

MK4511	X	–XX	
ROOT PART NUMBER	PACKAGE	SPEED	TEMP RANGE

BLANK 0° TO 70°C

-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME

N 28 PIN DIP
K 32 PIN PLCC

SGS-THOMSON
MICROELECTRONICS

MK4505M/4505S(N) -25/33/50

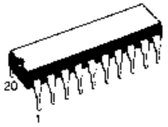
VERY HIGH-SPEED CMOS CLOCKED FIFO

PRELIMINARY DATA

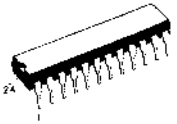
- 1024 x 5 ORGANIZATION
- VERY HIGH PERFORMANCE

Part No.	Cycle Time	Cycle Frequency	Access Time
4505-25	25 ns	40 MHz	15 ns
4505-33	33 ns	30 MHz	20 ns
4505-50	50 ns	20 MHz	25 ns

- RISING EDGE TRIGGERED CLOCK INPUTS
- SUPPORTS FREE-RUNNING 40% TO 60% DUTY CYCLE CLOCK INPUTS
- SEPARATE READ AND WRITE ENABLE INPUTS
- BiPORT™ RAM ARCHITECTURE ALLOWS FULLY ASYNCHRONOUS AND SIMULTANEOUS READ/WRITE OPERATION
- CASCADABLE TO ANY DEPTH WITH NO ADDITIONAL LOGIC
- WIDTH EXPANDABLE TO MORE THAN 40 BITS WITH NO ADDITIONAL LOGIC
- HALF FULL STATUS FLAG
- FULL AND EMPTY FLAGS, ALMOST FULL, ALMOST EMPTY, INPUT READY, OUTPUT VALID STATUS FLAGS (4505M)
- FULLY TTL COMPATIBLE
- 300 MIL PLASTIC DIP

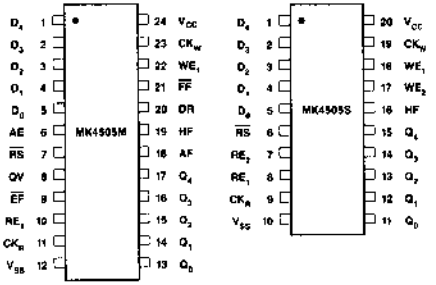


N
DIP-20
(Plastic Package)



N
DIP-24
(Plastic Package)

FIGURE 1. PIN CONFIGURATION


D_4 1
D_3 2
D_2 3
D_1 4
D_0 5
AE 6
$\overline{RS}$ 7
QV 8
$\overline{EF}$ 9
RE_1 10
CK_R 11
V_{SS} 12
24 V_{CC}
23 CK_W
22 WE_1
21 $\overline{FF}$
20 DR
19 HF
18 AF
17 Q_4
16 Q_3
15 Q_2
14 Q_1
13 Q_0
MK4505M
D_4 1
D_3 2
D_2 3
D_1 4
D_0 5
$\overline{RS}$ 6
RE_2 7
RE_1 8
CK_R 9
V_{SS} 10
20 V_{CC}
19 CK_W
18 WE_1
17 WE_2
16 HF
15 Q_4
14 Q_3
13 Q_2
12 Q_1
11 Q_0
MK4505S

PIN NAMES

D_0 - D_4	- Data Input
Q_0 - Q_4	- Data Output
CK_W, CK_R	- Write and Read Clock
WE_1	- Write Enable Input 1
RE_1	- Read Enable Input 1
$\overline{RS}$	- Reset (Active Low)
HF	- Half Full Flag
V_{CC}, V_{SS}	- +5 Volt, Ground

(4505M Only)

$\overline{FF}$, $\overline{EF}$	- Full and Empty Flag (Active Low)
AF, AE	- Almost Full, Almost Empty Flag
DR, QV	- Input Ready, Output Valid

(4505S Only)

WE_2	- Write Enable Input 2
RE_2	- Read Enable Input 2 (Rising Edge Triggered 3 State Control)

Supersedes publication for January 1988.

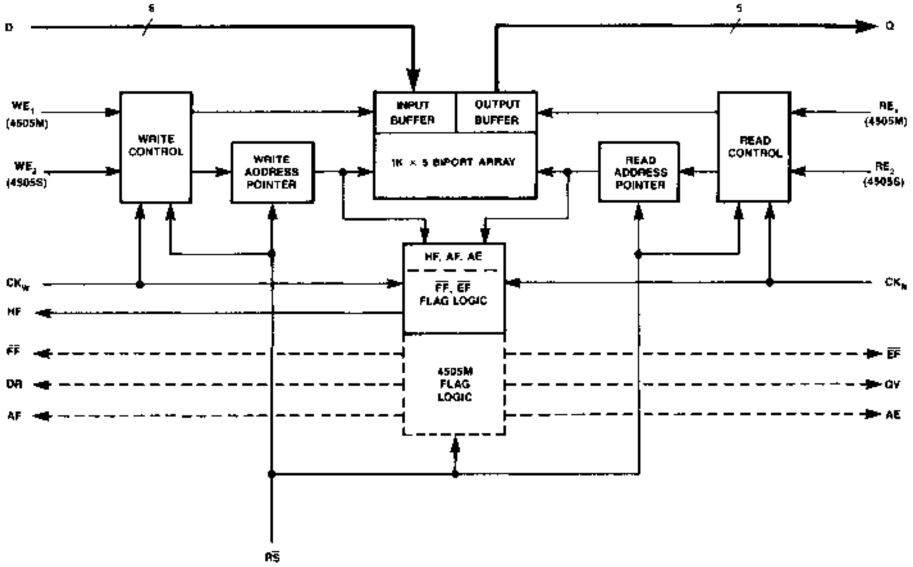
DESCRIPTION

The MK4505 is a Very High Speed 1K x 5 Clocked FIFO memory. It achieves its high performance through the use of a pipelined architecture, a 1.2μ full CMOS, single poly, double level metal process, and a memory array constructed using SGS-THOMSON's 8 transistor BiPORT memory cell.

The device is designed for use in applications where data is moving through a system on a square wave clock; applications such as digitized video and audio, image processing, A-to-D and D-to-A conversions, high speed data links, Radar return sampling or data tracing.

The device is available in two versions; a Master, the MK4505M, and a Slave, the MK4505S. The Master provides all of the control signals necessary for reliable, full speed, fully asynchronous width expansion and/or depth expansion. The Master also provides a full compliment of status flags, including Output Valid, Empty, Almost Empty, Half Full, Almost Full, Full, and Input Ready. The Master cannot be written while Full or read while Empty. The Slave, in contrast, can be forced to write and/or read continuously regardless of device status; a feature useful in triggered data acquisitions, or for retransmit (repeat reading) applications.

FIGURE 2. BLOCK DIAGRAM MK4505M/4505S


D
5
5
Q
WE_1 (4505M)
WE_2 (4505S)
WRITE CONTROL
WRITE ADDRESS POINTER
INPUT BUFFER
OUTPUT BUFFER
1K × 5 BIPORT ARRAY
READ ADDRESS POINTER
READ CONTROL
RE_1 (4505M)
RE_2 (4505S)
HF, AF, AE
$\overline{FF}$, $\overline{EF}$ FLAG LOGIC
CK_W
CK_R
HF
$\overline{FF}$
DR
AF
4505M FLAG LOGIC
$\overline{EF}$
OV
AE
$\overline{RS}$

4505M (MASTER) WRITE TRUTH TABLE

CK_W	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	WE_1	$\overline{FF}$	$\overline{OR}$		$\overline{FF}$	$\overline{OR}$	Q
X	0	X	X	X	Reset	1	1	Don't Care
↑	1	0	0	0	No-Op	?	?	Don't Care
↑	1	0	1	1	No-Op	1	1	Don't Care
↑	1	1	0	0	No-Op	?	?	Don't Care
↑	1	1	1	1	Write	?	?	Data In

? = The "Next State" logic level is unknown due to the possible occurrence of a read operation.

4505M (MASTER) READ TRUTH TABLE

CK_R	PRESENT STATE				NEXT OPERATION	NEXT STATE		
	$\overline{RS}$	RE_1	$\overline{EF}$	$\overline{OV}$		$\overline{EF}$	$\overline{OV}$	Q
X	0	X	X	X	Reset	0	0	Hi Z
↑	1	0	0	0	Inhibit	?	0	Hi Z
↑	1	0	0	1	Inhibit	?	0	Hi Z
↑	1	0	1	0	Hold	1	1	Previous Q
↑	1	0	1	1	Hold	1	1	Previous Q
↑	1	1	0	0	Inhibit	?	0	Hi Z
↑	1	1	0	1	Inhibit	?	0	Hi Z
↑	1	1	1	0	Read	?	1	Data Out
↑	1	1	1	1	Read	?	1	Data Out

? = The "Next State" logic level is unknown due to the possible occurrence of a write operation

4505S (SLAVE) WRITE TRUTH TABLE

CK_W	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	WE_1	WE_2		Q
X	0	X	X	Reset	Don't Care
↑	1	0	0	No-Op	Don't Care
↑	1	0	1	No-Op	Don't Care
↑	1	1	0	No-Op	Don't Care
↑	1	1	1	Write	Data In

4505S (SLAVE) READ TRUTH TABLE

CK_R	PRESENT STATE			NEXT OPERATION	NEXT STATE
	$\overline{RS}$	RE_1	RE_2		Q
X	0	X	X	Reset	Hi Z
↑	1	0	0	Inhibit	Hi Z
↑	1	0	1	Hold	Previous Q
↑	1	1	0	Inhibit	Hi Z
↑	1	1	1	Read	Data Out

X = Don't care

WRITE OPERATIONS

The device will perform a Write on the next rising edge of the Write Clock (CK_W) whenever (see figure 3):

- — (4505S) WE_1 and WE_2 are high at the rising edge of the clock.
- — (4505M) WE_1 and $\overline{FF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Full Flag ($\overline{FF}$) on the rising edge of CK_W, the appearance of an active Full Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_W will generate a NO-OP condition.

READ AND HOLD OPERATIONS

The device will perform a Read on the next rising edge of the Read Clock (CK_R) whenever (see figure 4):

- — (4505S) RE_1 and RE_2 are high at the rising edge of the clock.
- — (4505M) RE_1 and $\overline{EF}$ are high at the rising edge of the clock.

Because the device only re-evaluates and updates the Empty Flag ($\overline{EF}$) on the rising edge of CK_R, the appearance of an active Empty Flag at valid flag access time, t_{F1A}, assures the user that the next rising edge of CK_R will generate an inhibit condition. All Q outputs will be High Z at t_{QZ} from the rising edge of CK_R.

The device will perform a Hold Cycle (hold over previous data) if RE_1 is low at the rising edge of the clock (CK_R). If $\overline{EF}$ (4505M) or RE_2 (4505S) is low at the rising edge of the clock, then the outputs will go to High-Z.

RESET

$\overline{RS}$ is an asynchronous master reset input. A Reset is required after power-up, before first write. Reset commences on the falling edge of $\overline{RS}$ irrespective of the state of any other input or output. The user is required to observe Reset Set Up Time (t_{RSS}) only if the device is enabled (see Figure 6). The t_{RSS} specification is a don't care if the device remains disabled (WE_1 = RE_1 = LOW). All status flag outputs will be valid t_{RSA} from the falling edge of $\overline{RS}$, and all Q data outputs will be high impedance t_{RSOZ} from the same falling edge.

After Reset, if no valid Read operations have been performed since Reset, the "previous data" that will be output when executing the first Hold cycle will be all zeros (see Figure 7.)

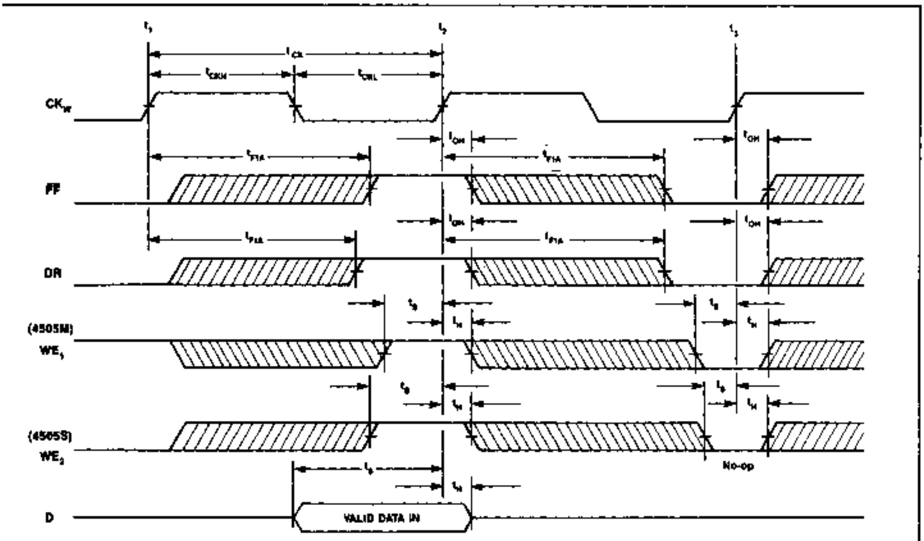
AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	4505-25		4505-33		4505-50		UNITS	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CK}	Clock Cycle Time	25		33		50		ns	1
t_{CKH}	Clock High Time	10		13		20		ns	1
t_{CKL}	Clock Low Time	10		13		20		ns	1
t_S	Set Up Time	10		13		16		ns	1
t_H	Hold Time	0		0		0		ns	
t_A	Output (Q) Access Time		15		20		25	ns	1,2
t_{F1A}	Flag 1 Access Time(7)		15		20		25	ns	1,2
t_{F2A}	Flag 2 Access Time(8)		20		25		30	ns	1,2
t_{OH}	Output Hold Time	5		5		5		ns	1,2
t_{QZ}	Clock to Outputs High-Z		15		20		25	ns	1,3
t_{OL}	Clock to Outputs Low-Z	5		5		5		ns	1,3
t_{RSS}	Reset Set Up Time	12		16		25		ns	1,4
t_{RS}	Reset Pulse Width	25		33		50		ns	
t_{RSA}	Reset Flag Access Time		50		66		100	ns	1,3
t_{RSQZ}	Reset to Outputs High-Z		25		33		50	ns	1,3
t_{FRL}	First Read Latency	50		66		100		ns	1,5
t_{FFL}	First Flag Cycle Latency	25		33		50		ns	1,6

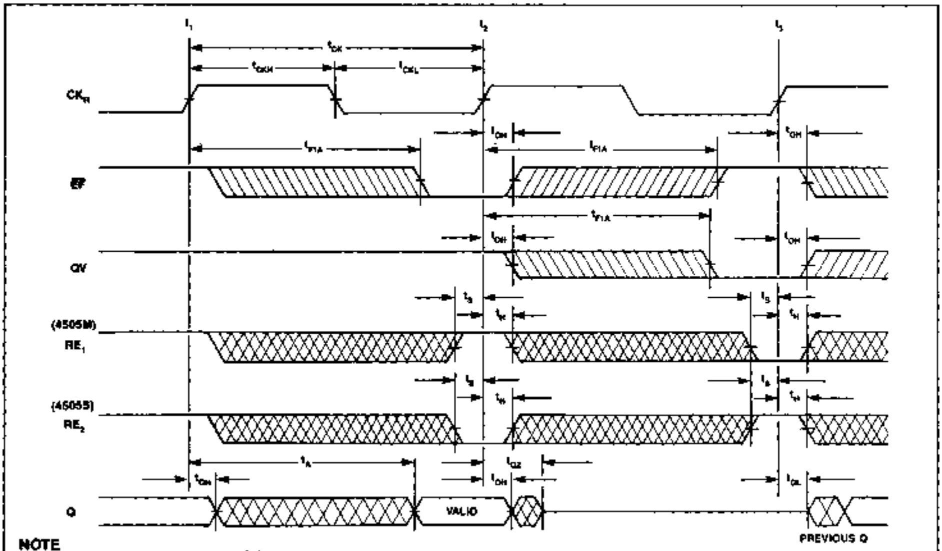
1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/40pf Output Load (Figure 15A).
3. Measured w/5pf Output Load (Figure 15B).
4. Need not be met unless device is Read and/or Write Enabled.
5. Minimum first Write to first Read delay required to assure valid first Read.
6. Minimum first Write to first Read Clock delay required to assure clearing the Empty Flag.
7. Flag 1 = $\overline{EF}$, $\overline{FF}$, QV, DR.
8. Flag 2 = AE, AF, HF.

IGURE 3. WRITE CYCLE TIMING


t1
t2
t3
tCK
tCKH
tCKL
CKW
tOH
tFIA
FF
tFIA
tOH
DR
tS
tH
(4505M) WE1
tS
tH
(4505S) WE2
No-op
tS
tH
D
VALID DATA IN

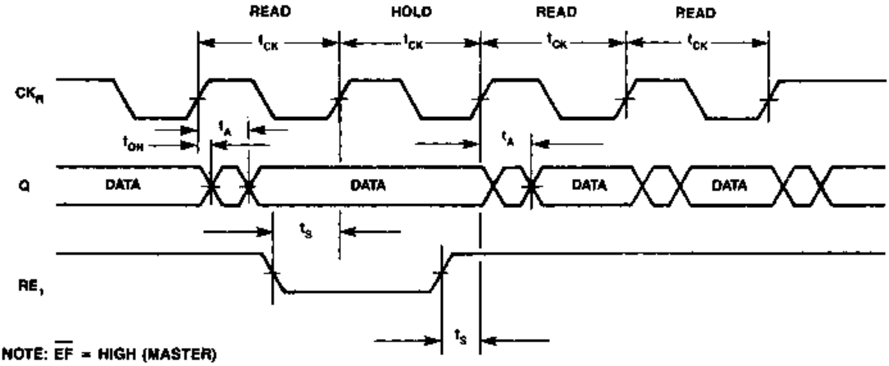
NOTE
For this particular diagram, the $\overline{FF}$ changes logic states presuming that a valid READ operation has occurred prior to the rising edge of CK_W at t_1.

FIGURE 4. READ CYCLE TIMING


t1
t2
t3
tCK
tCKH
tCKL
CKR
tOH
tFIA
EF
tFIA
tOH
OV
tS
tH
(4505M) RE1
tS
tH
(4505S) RE2
tA
tOH
tOZ
tOH
tOL
Q
VALID
PREVIOUS Q

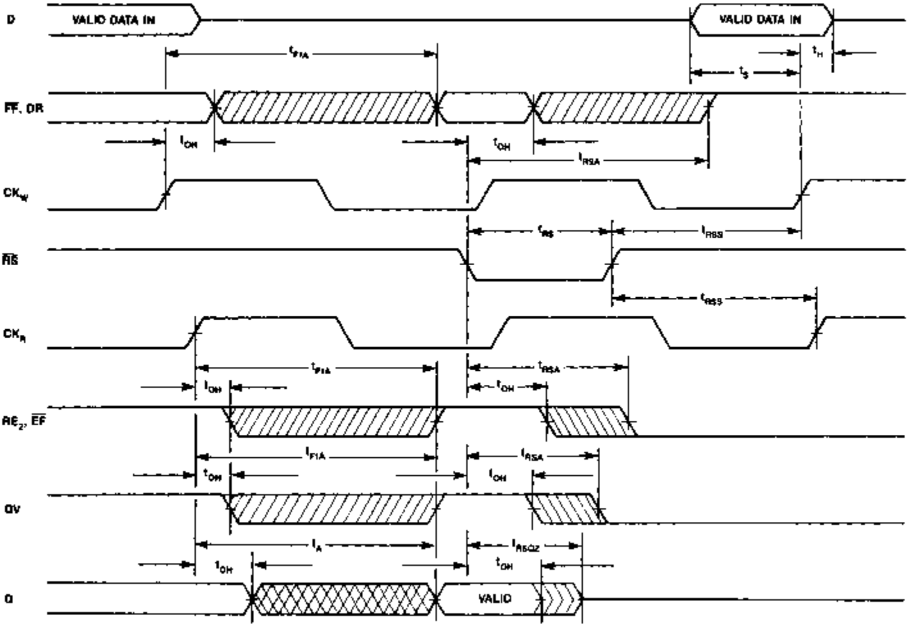
NOTE
For this particular diagram, the $\overline{EF}$ changes logic states presuming that a valid WRITE operation has occurred prior to the rising edge of CK_R at t_2.

FIGURE 5. HOLD CYCLE TIMING


READ
HOLD
READ
READ
t_{CK}
t_{CK}
t_{CK}
t_{CK}
CK_R
t_{OH}
t_A
t_A
Q
DATA
DATA
DATA
DATA
t_S
RE_1
t_S

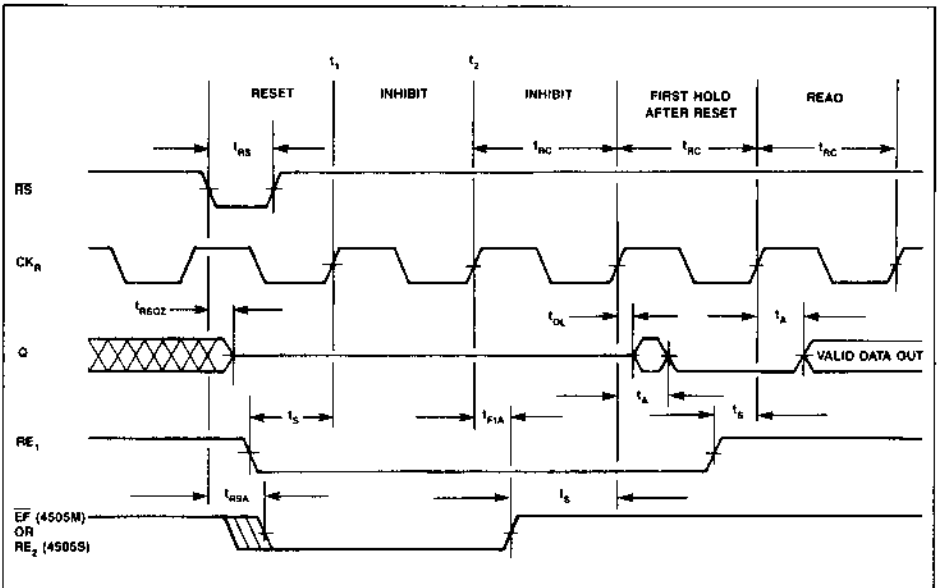
NOTE: $\overline{EF}$ = HIGH (MASTER)
RE_2 = HIGH (SLAVE)

FIGURE 6. RESET CYCLE TIMING (4505M/S


D
VALID DATA IN
VALID DATA IN
t_{FIA}
t_H
t_S
FF, OR
t_{OH}
t_{OH}
t_{RSA}
CK_W
t_{RS}
t_{RSS}
$\overline{RS}$
t_{RSS}
CK_R
t_{FIA}
t_{RSA}
t_{OH}
t_{OH}
RE_2, $\overline{EF}$
t_{FIA}
t_{RSA}
t_{OH}
t_{OH}
OV
t_A
t_{RSQZ}
t_{OH}
t_{OH}
Q
VALID

NOTE: t_{RSS} MUST BE MET IF THE DEVICE IS READ AND/OR WRITE ENABLED (WE_1, RE_1 = HIGH)

FIGURE 7. FIRST HOLD AFTER RESET


t1
t2
RESET
INHIBIT
INHIBIT
FIRST HOLD AFTER RESET
READ
tRS
tRC
tRC
tRC
RS
CKR
tRSQZ
tOL
tA
Q
VALID DATA OUT
tS
tF1A
tA
tS
RE1
tRSA
tS
EF (4505M) OR RE2 (4505S)

NOTE: A VALID WRITE OPERATION IS PRESUMED BETWEEN t_1 and t_2.

FIGURE 8. ALMOST EMPTY FLAG TIMING (4505M)

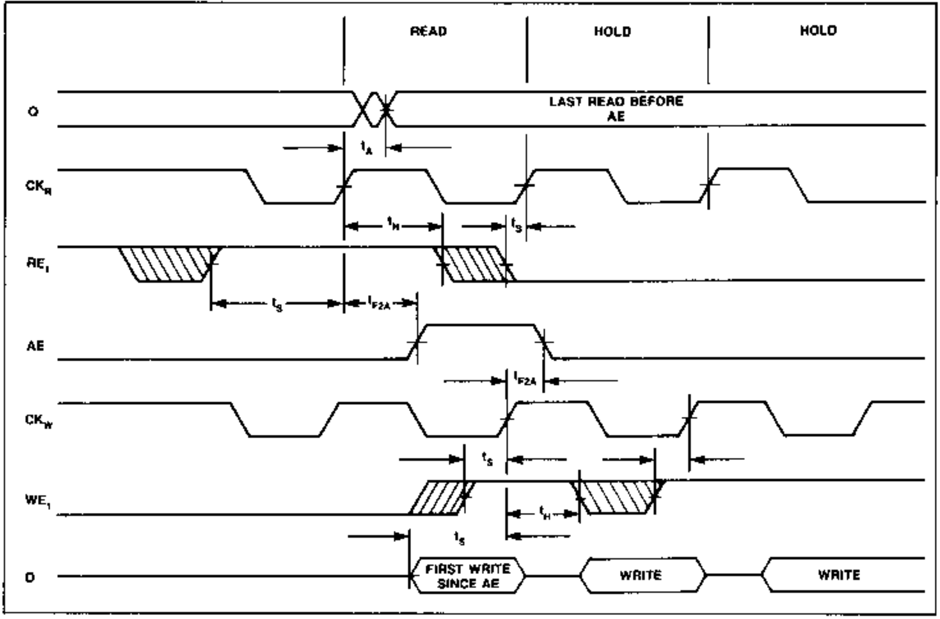
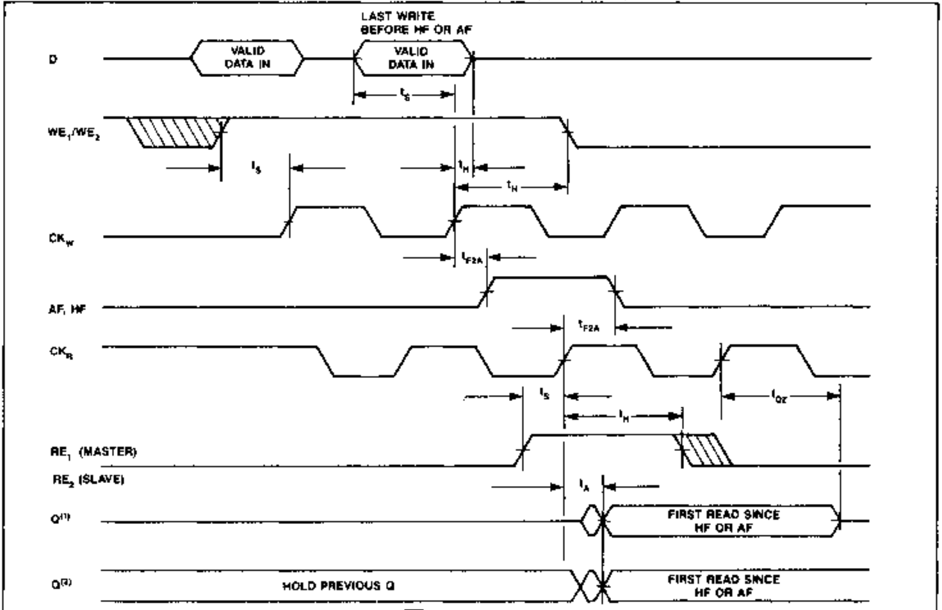

READ
HOLD
HOLD
Q
LAST READ BEFORE AE
tA
CKR
tH
tS
RE1
tS
tF2A
AE
tF2A
CKW
tS
WE1
tH
tS
D
FIRST WRITE SINCE AE
WRITE
WRITE

FIGURE 9. ALMOST FULL, HALF FULL FLAG TIMING (4505M/S)


LAST WRITE BEFORE HF OR AF
D
VALID DATA IN
VALID DATA IN
t_S
WE_1/WE_2
t_S
t_H
t_H
CK_W
t_{F2A}
AF, HF
t_{F2A}
CK_R
t_S
t_{OZ}
t_H
RE_1 (MASTER)
RE_2 (SLAVE)
t_A
$Q^{(1)}$
FIRST READ SINCE HF OR AF
$Q^{(2)}$
HOLD PREVIOUS Q
FIRST READ SINCE HF OR AF

1. Q outputs in Master/Slave Width Expansion ($RE_2 = \overline{EF}$), or when using MK4505S Slave separately.
2. Q outputs in Master-to-Master Depth Expansion (RE_1 with $\overline{EF}$ = HIGH), or when using the MK4505M separately.

Flag Interpretation Key

FLAG	CURRENT STATE	VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
		MIN	MAX	MIN	MAX
AE	1	1016	1024	0	8
	0	0	1015	9	1024
HF	1	0	512	512	1024
	0	513	1024	0	511
AF	1	0	8	1016	1024
	0	9	1024	0	1015

NOTE

The table describes the number of valid cycles that can be performed, including the next rising edge of the clock.

FIGURE 10. SIMULTANEOUS WRITE/READ TIMING (4505M)

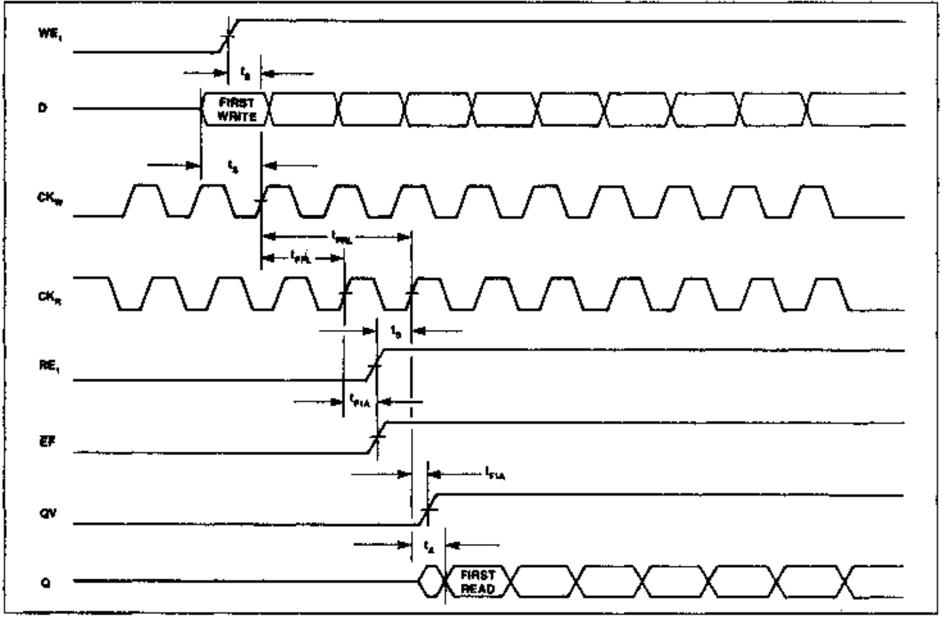
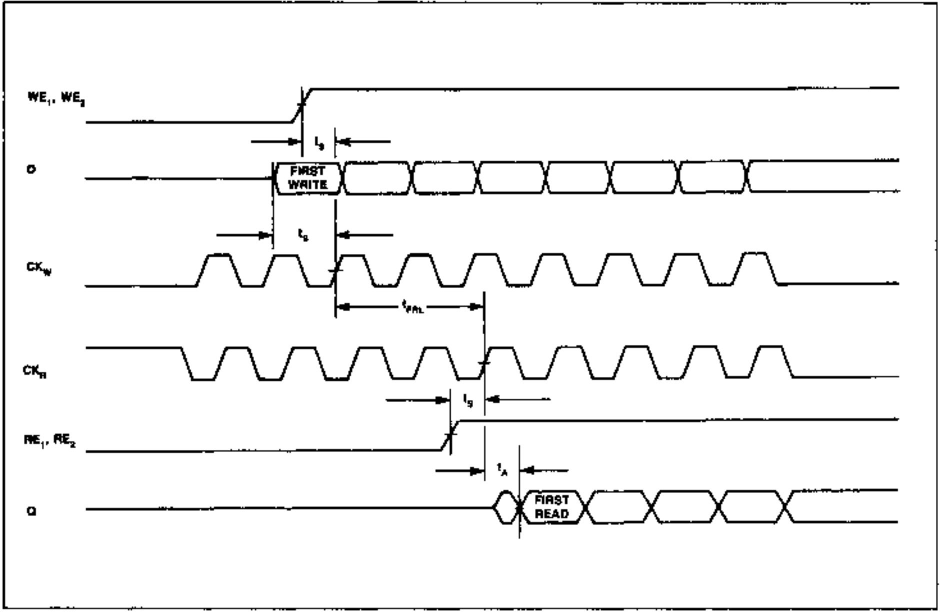

WE1
tS
D
FIRST WRITE
tS
CKW
tFRL
tEFL
CKR
tS
RE1
tFIA
EF
tFIA
QV
tA
Q
FIRST READ

FIGURE 11. SIMULTANEOUS WRITE/READ TIMING (4505S)


WE1, WE2
tS
D
FIRST WRITE
tS
CKW
tFRL
CKR
tS
RE1, RE2
tA
Q
FIRST READ

SIMULTANEOUS WRITE/READ TIMING

The Empty Flag ($\overline{EF}$) is guaranteed to clear (go HIGH)in response to the first rising edge of the read clock (CK_R) to occur t_{FFL} (First Flag Latency) after a valid First Write (from the rising edge of CK_W). Read clocks occurring less than t_{FFL} after a First Write may clear the $\overline{EF}$, but are not guaranteed (see Figure 10). As always, reads attempted in conjunction with an active Empty Flag are inhibited. Therefore, the next rising edge of CK_R following t_{FFL} will produce the first valid read. This is the t_{FRL} (First Read Latency) parameter, and must be observed for proper system operation with the latched $\overline{EF}$. Coming from an empty condition, the First Read operation should be accomplished by enabling RE_1 no less than t_S before the rising edge of CK_R at t_{FRL}. The Q outputs will present valid data t_A from the rising edge of CK_R.

When using the MK4505S (Slave) separately, the user must observe the t_{FRL} (First Read Latency) parameter to ensure first-write-to-first-read valid data. Referring to Figure 11, the first rising edge of CK_R to occur t_{FRL} after a First Write clock will guarantee valid data t_A from the rising edge of CK_R. Read operations attempted before t_{FRL} is satisfied may result in reading RAM locations not yet written. Careful observance of t_{FRL} by the user is a must when using free running asynchronous read/write clocks on the MK4505S; there is no automatic read and write protection circuitry in the Slave.

It should also be noted that the MK4505M/S has an expected "fall-through delay time" described as First Write data presented to the FIFO and clocked out to the outside world. This can be calculated as: $t_S + t_{FRL} + t_A$ (from Figure 10 or 11). Further occurring valid read clocks will present data to the Q outputs t_A from the rising edge of CK_R.

WIDTH AND DEPTH EXPANSION

A single Master (MK4505M) is required for each 1k of depth configured. The number of Slaves that can be driven by a single Master is limited only by the effects of adding extra load capacitance (Write and Read Enable Input Capacitance) onto the Input Ready (DR), Output Valid (QV), Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$) outputs. However, even 40 bits of width (8 devices) results in only 40pf of loading, which corresponds to the amount of load called out in the AC Test Conditions. Additional loading will slow the flags down, but as long as Enable Set Up time (t_S) is met, slowing the flags has no negative consequences.

WIDTH AND DEPTH EXPANSION EXAMPLES

The width and depth expansion interface timing diagrams (Figures 13 and 14) are in reference to the width and depth expansion schematic in Figure 12 (For simplicity all clocks have the same frequency and transistion rate). Example 1 - First Write Since Empty - Reading the timing diagram from the top left to bottom right, one can determine that Figure 13 illustrates the effects of the first WRITE/READ cycles from an EMPTY array of FIFOs. Both of the $\overline{EF}$ pins are initially low ($\overline{EF_X}$, $\overline{EF}$ and RE_2). As data is written into Bank A, the expansion clock reads data from Bank A and writes it to Bank B, the interface $\overline{EF}$ ($\overline{EF}$ and RE_2) and the external $\overline{EF}$ ($\overline{EF_X}$) go inactive (logic 1) while data is shifted through the FIFO array from Bank A through Bank B to the external output (Q_X). The $\overline{EF}$ logic goes valid (logic 0) once data is shifted out of its respective bank.

Example 2 - First Read Since Full - Reading the timing diagram from the bottom left to top right, one can determine that Figure 14 illustrates the effects of the first READs from a FULL array of FIFOs. As data is read out of the system (Q_X), it allows Bank B to receive data shifted from Bank A. As Bank B shifts data out via Q_X, allowing Bank A to shift data into Bank B, both banks will show a reset $\overline{FF}$ status (logic 1) on the expansion $\overline{FF}$ ($\overline{FF}$ and WE_2) as well as the external $\overline{FF}$ ($\overline{FF_X}$). When Bank A is no longer considered FULL, Data In from the system (D_X) is now written into Bank A and shifted to Bank B until the FIFO array is again completely Full.

APPLICATION

The MK4505 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the MK4505 can also interface to 5 volt CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK4505, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. A high frequency decoupling capacitor should be placed next to each FIFO. The capacitor should be 0.1 μF or larger. Also, a pull-up resistor in the range of 1K ohms is recommended for the $\overline{RESET}$ input pin to improve proper operation.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

FIGURE 12. MK4505M/S 2K x 10 WIDTH AND DEPTH EXPANSION SCHEMATIC

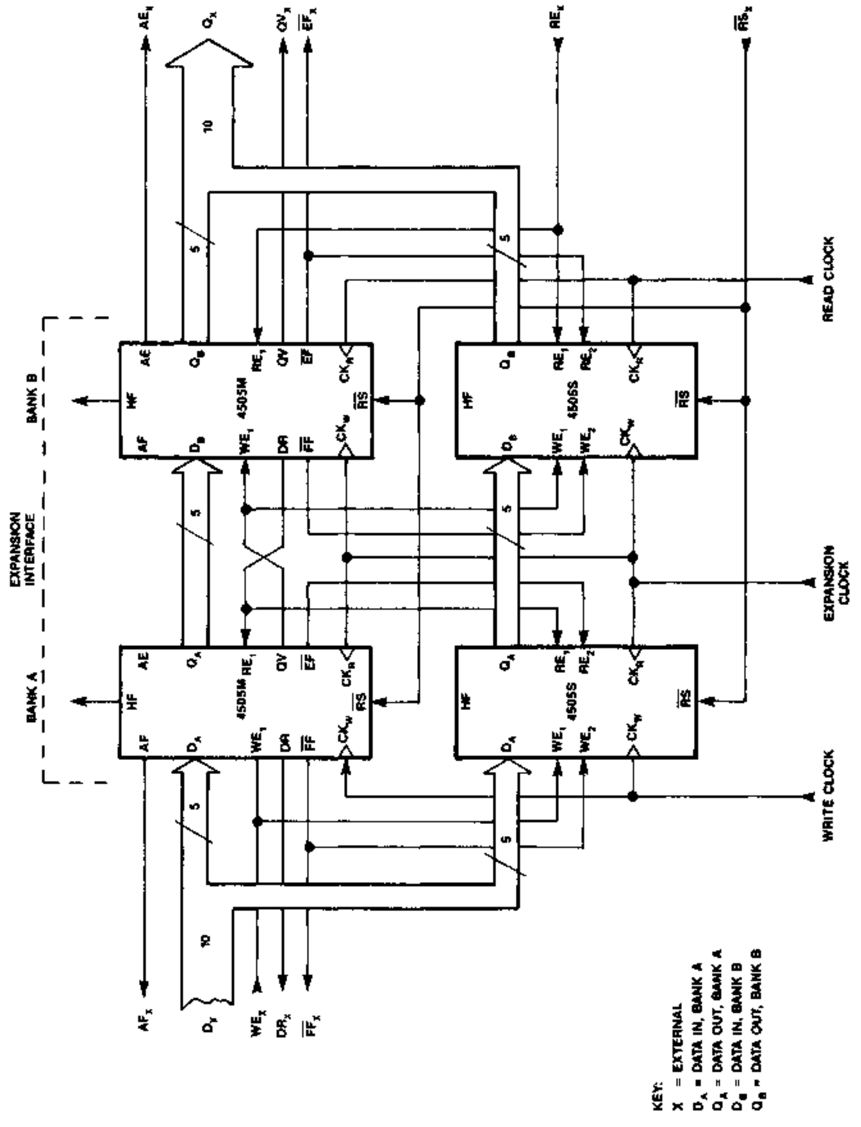
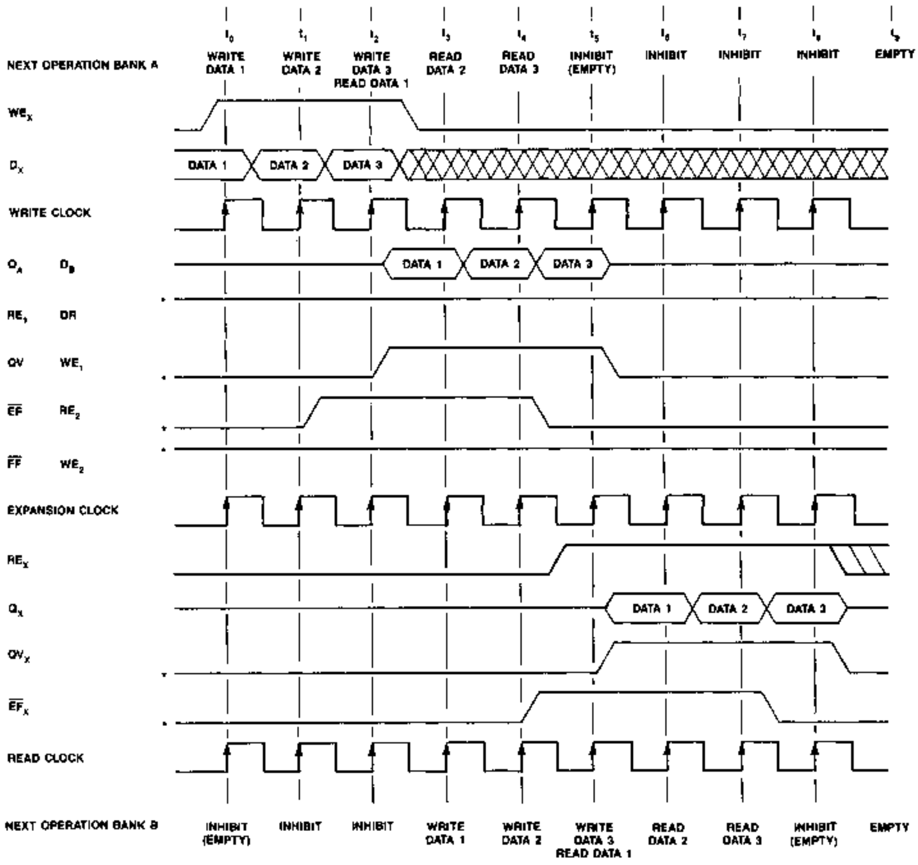
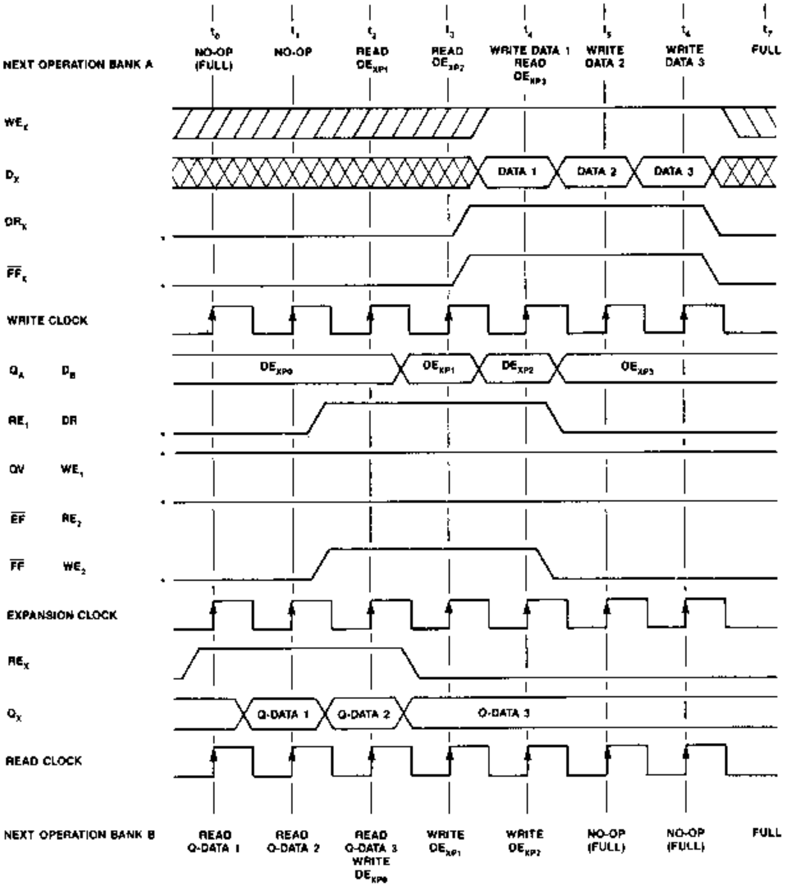

EXPANSION INTERFACE
BANK A
BANK B
4505M
4505S
AF
HF
AE
D_A
Q_A
D_B
Q_B
WE_1
WE_2
RE_1
RE_2
DR
QV
$\overline{FF}$
$\overline{EF}$
CK_W
CK_R
$\overline{RS}$
AF_X
D_X
WE_X
DR_X
$\overline{FF}_X$
AE_X
Q_X
QV_X
$\overline{EF}_X$
RE_X
$\overline{RS}_X$
10
5
WRITE CLOCK
EXPANSION CLOCK
READ CLOCK
KEY:
X = EXTERNAL
D_A = DATA IN, BANK A
Q_A = DATA OUT, BANK A
D_B = DATA IN, BANK B
Q_B = DATA OUT, BANK B

FIGURE 13. EXAMPLE 1 - WIDTH AND DEPTH EXPANSION INTERFACE TIMING


t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
t_8
t_9
NEXT OPERATION BANK A
WRITE DATA 1
WRITE DATA 2
WRITE DATA 3 READ DATA 1
READ DATA 2
READ DATA 3
INHIBIT (EMPTY)
INHIBIT
INHIBIT
INHIBIT
EMPTY
WE_X
D_X
DATA 1
DATA 2
DATA 3
WRITE CLOCK
Q_A D_B
DATA 1
DATA 2
DATA 3
RE_1 OR
OV WE_1
$\overline{EF}$ RE_2
$\overline{FF}$ WE_2
EXPANSION CLOCK
RE_X
Q_X
DATA 1
DATA 2
DATA 3
OV_X
$\overline{EF}_X$
READ CLOCK
NEXT OPERATION BANK B
INHIBIT (EMPTY)
INHIBIT
INHIBIT
WRITE DATA 1
WRITE DATA 2
WRITE DATA 3 READ DATA 1
READ DATA 2
READ DATA 3
INHIBIT (EMPTY)
EMPTY

* NOTE: EXAMPLE BEGINS WITH BOTH BANKS EMPTY, AS STATUS FLAGS INDICATE

FIGURE 14. EXAMPLE 2 - WIDTH AND DEPTH EXPANSION INTERFACE TIMING



t_0
t_1
t_2
t_3
t_4
t_5
t_6
t_7
NEXT OPERATION BANK A
NO-OP (FULL)
NO-OP
READ OE_{XP1}
READ OE_{XP2}
WRITE DATA 1 READ OE_{XP3}
WRITE DATA 2
WRITE DATA 3
FULL
WE_X
D_X
DATA 1
DATA 2
DATA 3
OR_X
$\overline{FF}_X$
WRITE CLOCK
Q_A D_B
OE_{XP0}
OE_{XP1}
OE_{XP2}
OE_{XP3}
RE_1 OR
QV WE_1
$\overline{EF}$ RE_2
$\overline{FF}$ WE_2
EXPANSION CLOCK
RE_X
Q_X
Q-DATA 1
Q-DATA 2
Q-DATA 3
READ CLOCK
NEXT OPERATION BANK B
READ Q-DATA 1
READ Q-DATA 2
READ Q-DATA 3 WRITE OE_{XP0}
WRITE OE_{XP1}
WRITE OE_{XP2}
NO-OP (FULL)
NO-OP (FULL)
FULL

* NOTE: EXAMPLE BEGINS WITH BOTH BANKS FULL, AS INDICATED BY STATUS FLAGS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . −1.0V to +7.0V
Ambient Operating Temperature (T_A) . . . . 0 to +70 C
Ambient Storage Temperature (Plastic) . . . . −55 to +125 C
Total Device Power Dissipation . . . . 1 Watt
RMS Output Current per Pin 25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		$V_{CC}+1.0$	V	1
V_{IL}	Logic 0 Input	−0.3		0.8	V	1

NOTES

1. All voltages referenced to GND.

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$), V_{CC} = 5.0 ± 10%)

SYM	PARAMETER	MK4505-25			MK4505-33			MK4505-50			UNITS	NOTE
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
I_{CC}	Average Power Supply Current		115	140		95	140		75	140	mA	1

SYM	PARAMETER	MIN	MAX		
I_{IL}	Input Leakage Current	−1	+1	μA	2
I_{OL}	Output Leakage Current	−10	+10	μA	2,3
V_{OH}	Logic 1 Output Voltage (I_{OUT} = −4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4

NOTES

1. Measured with both ports operating at t_{CK} Min, 50% duty cycle, outputs open, V_{CC} max. Typical values reflect t_{CK} Min, outputs open, with V_{CC} = 5.0, 25°C, with 50% duty cycle.
2. Measured with V = 0.0V to V_{CC}.
3. Measured at Q_0 - Q_4.
   Measured after clocking with RE_2 = LOW (4505S).
   Measured with QV = LOW (4505M).
4. All voltages referenced to GND.

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	LIMITS		UNITS	NOTE
		TYP	MAX		
C_I	Input Capacitance	4	5	pf	1
CO_1	Output Capacitance	8	10	pf	1,2
CO_2	Output Capacitance	12	15	pf	1,3

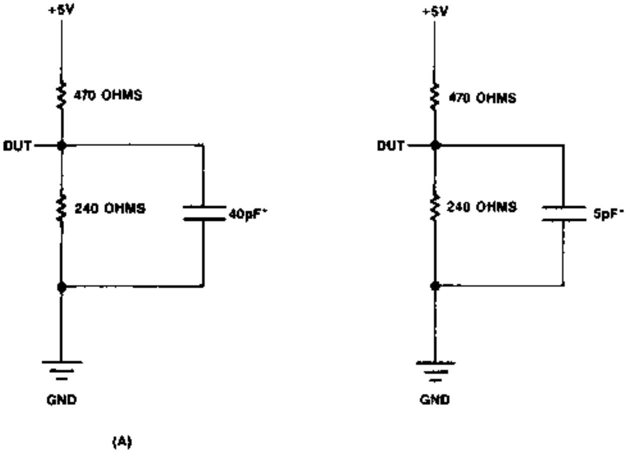
NOTES

1. Sampled, not 100% tested. Measured at 1MHz.
2. Measured at all data and flag outputs except $\overline{EF}$ and $\overline{FF}$.
3. Measured at $\overline{EF}$ and $\overline{FF}$.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0 to 70 C
V_{CC}	5.0 Volts ± 10%

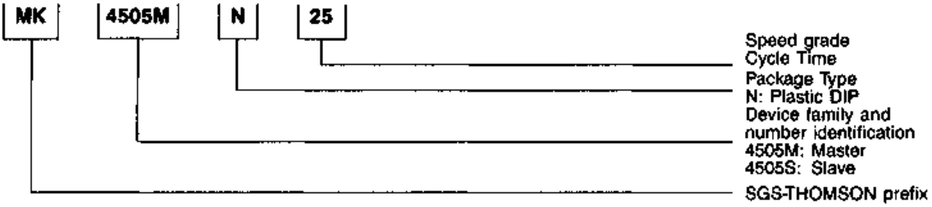
FIGURE 15. EQUIVALENT OUTPUT LOAD CIRCUIT


+5V
470 OHMS
DUT
240 OHMS
40pF*
GND
(A)
+5V
470 OHMS
DUT
240 OHMS
5pF*
GND

* INCLUDES SCOPE AND TEST JIG.

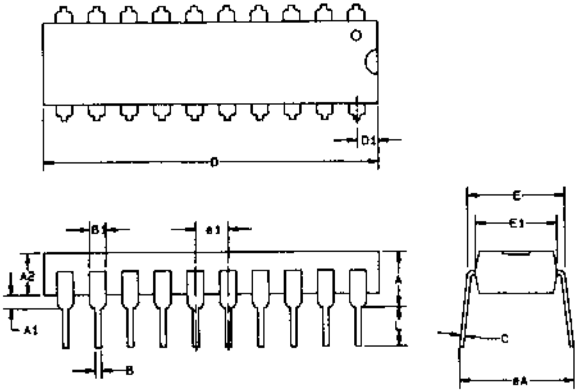
ORDERING INFORMATION

PART NUMBER	CYCLE TIME	ACCESS TIME	PACKAGE TYPE	TEMPERATURE
MK4505M(N)-25	25ns	15ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-33	33ns	20ns	24 pin Plastic DIP	0°C to 70°C
MK4505M(N)-50	50ns	25ns	24 pin Plastic DIP	0°C to 70°C
MK4505S(N)-25	25ns	15ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-33	33ns	20ns	20 pin Plastic DIP	0°C to 70°C
MK4505S(N)-50	50ns	25ns	20 pin Plastic DIP	0°C to 70°C


MK
4505M
N
25
Speed grade
Cycle Time
Package Type
N: Plastic DIP
Device family and
number identification
4505M: Master
4505S: Slave
SGS-THOMSON prefix

20 PIN "N" PACKAGE

PLASTIC DIP (MK4505S)



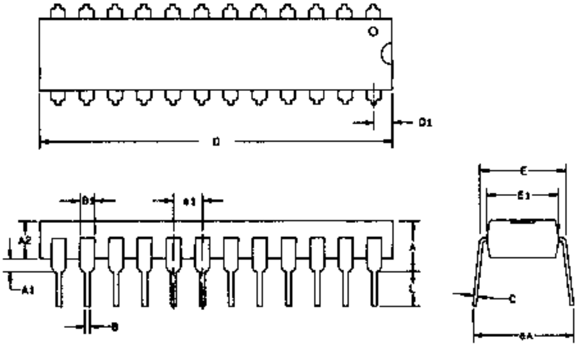
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

24 PIN "N" PACKAGE

PLASTIC DIP (4505M)



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	—	32.258	—	1.270	1
D1	1.524	2.286	.060	.090	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

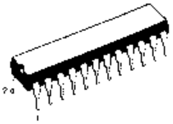
SGS-THOMSON
MICROELECTRONICS

MK45264/45265(N)-55/70

(64×5)×2 CMOS BIDIRECTIONAL BiPORT FIFO/TRANSCEIVER

ADVANCED DATA

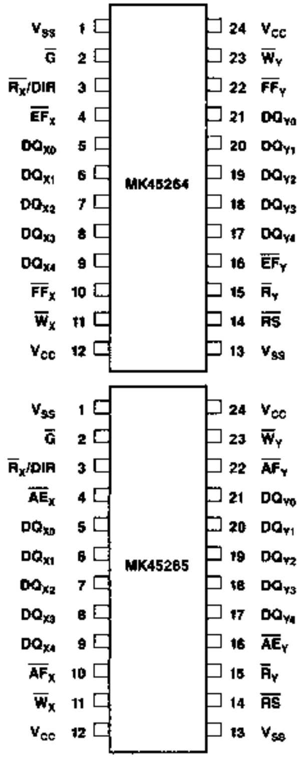
- DUAL 64x5 FIFOs PLUS A '245-TYPE TRANSCEIVER FUNCTION
- FULLY ASYNCHRONOUS DUAL PORT OPERATION
- EMPTY, FULL, ALMOST FULL AND ALMOST EMPTY STATUS FLAGS
- SPARE BITS FOR PARITY AND BEGINNING/END-OF-MESSAGE FLAGS
- +/− 12mA OUTPUT DRIVE CAPABILITY
- DUAL V_{CC} AND V_{SS} FOR IMPROVED MARGIN AND DRIVE
- 300 MIL DIP PACKAGE
- APPLICATION: ARBITRATION-FREE µP-TO-µP MESSAGE PASSING



N
DIP-24
(Plastic Package)

PART NUMBER	ACCESS TIME	CYCLE TIME	CYCLE RATE
MK45264N-55	55 ns	75 ns	13.3 MHz
MK45264N-70	70 ns	95 ns	10.5 MHz
MK45265N-55	55 ns	75 ns	13.3 MHz
MK45265N-70	70 ns	95 ns	10.5 MHz

FIGURE 1. PINOUT. 24 PIN, 300 MIL DIP


V_{SS} 1
$\overline{G}$ 2
$\overline{R}_X$/DIR 3
$\overline{EF}_X$ 4
DQ_{X0} 5
DQ_{X1} 6
DQ_{X2} 7
DQ_{X3} 8
DQ_{X4} 9
$\overline{FF}_X$ 10
$\overline{W}_X$ 11
V_{CC} 12
MK45264
24 V_{CC}
23 $\overline{W}_Y$
22 $\overline{FF}_Y$
21 DQ_{Y0}
20 DQ_{Y1}
19 DQ_{Y2}
18 DQ_{Y3}
17 DQ_{Y4}
16 $\overline{EF}_Y$
15 $\overline{R}_Y$
14 $\overline{RS}$
13 V_{SS}
V_{SS} 1
$\overline{G}$ 2
$\overline{R}_X$/DIR 3
$\overline{AE}_X$ 4
DQ_{X0} 5
DQ_{X1} 6
DQ_{X2} 7
DQ_{X3} 8
DQ_{X4} 9
$\overline{AF}_X$ 10
$\overline{W}_X$ 11
V_{CC} 12
MK45265
24 V_{CC}
23 $\overline{W}_Y$
22 $\overline{AF}_Y$
21 DQ_{Y0}
20 DQ_{Y1}
19 DQ_{Y2}
18 DQ_{Y3}
17 DQ_{Y4}
16 $\overline{AE}_Y$
15 $\overline{R}_Y$
14 $\overline{RS}$
13 V_{SS}

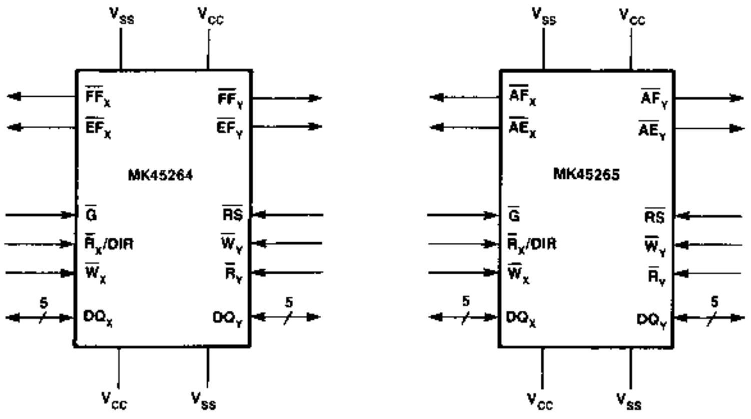
PIN NAMES

V_{CC}, V_{SS} = +5V, GND
DQ_{X0}-DQ_{X4} = X Port Data I/O
DQ_{Y0}-DQ_{Y4} = Y Port Data I/O
$\overline{W}_X$, $\overline{W}_Y$ = X & Y Port Write Enables
$\overline{R}_X$/DIR = X Port Read Enable and Transceiver Direction Control
$\overline{G}$ = Transceiver Enable
$\overline{R}_Y$ = Y Port Read Enable
$\overline{RS}$ = Master Reset
$\overline{EF}_X$, $\overline{FF}_Y$ = Y-to-X FIFO Empty/Full Flag
$\overline{EF}_Y$, $\overline{FF}_X$ = X-to-Y FIFO Empty/Full Flag
$\overline{AE}_Y$, $\overline{AF}_X$ = X-to-Y FIFO Almost Empty/Full
$\overline{AE}_X$, $\overline{AF}_Y$ = Y-to-X FIFO Almost Empty/Full

June 1988

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice

FIGURE 2. DEVICE LOGIC SYMBOL


V_{SS}
V_{CC}
$\overline{FF}_X$
$\overline{FF}_Y$
$\overline{EF}_X$
$\overline{EF}_Y$
MK45264
$\overline{G}$
$\overline{RS}$
$\overline{R}_X$/DIR
$\overline{W}_Y$
$\overline{W}_X$
$\overline{R}_Y$
5
DQ_X
DQ_Y
5
V_{CC}
V_{SS}
V_{SS}
V_{CC}
$\overline{AF}_X$
$\overline{AF}_Y$
$\overline{AE}_X$
$\overline{AE}_Y$
MK45265
$\overline{G}$
$\overline{RS}$
$\overline{R}_X$/DIR
$\overline{W}_Y$
$\overline{W}_X$
$\overline{R}_Y$
5
DQ_X
DQ_Y
5
V_{CC}
V_{SS}

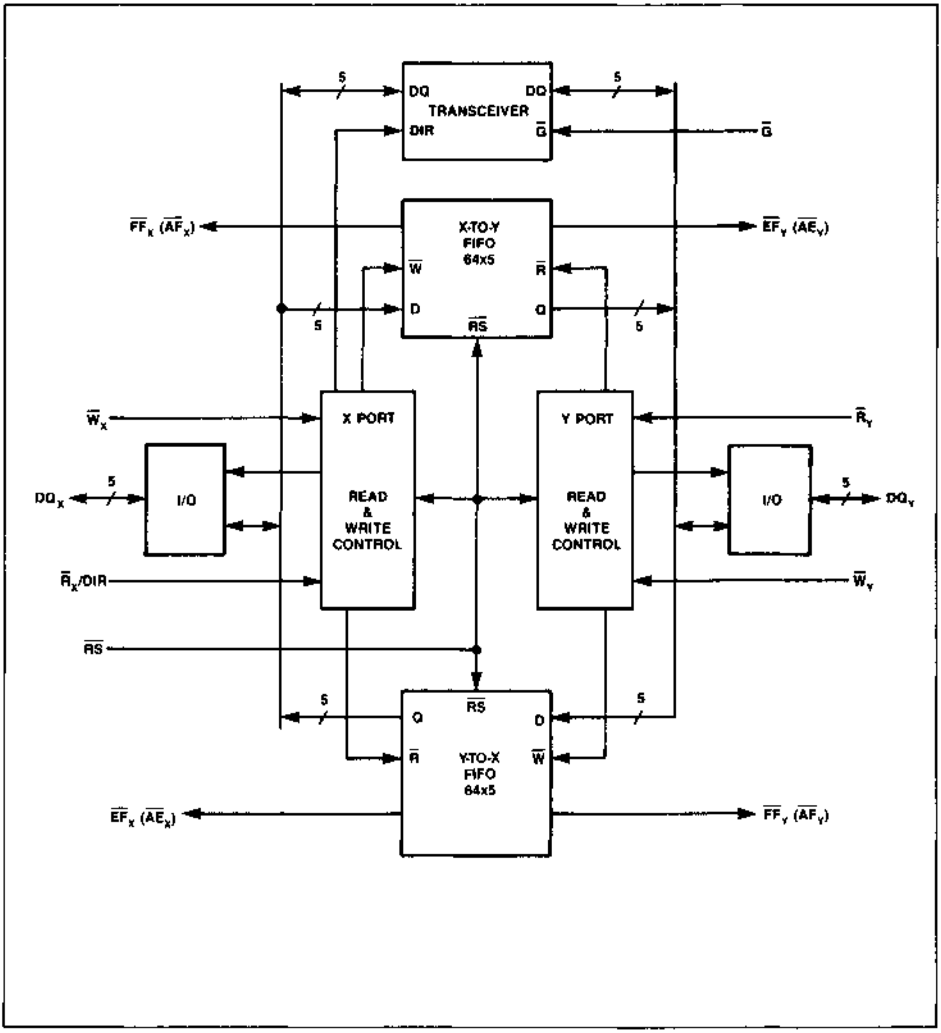
TRUTH TABLE

$\overline{RS}$	$\overline{G}$	$\overline{R_X}$/DIR	$\overline{W_X}$	$\overline{R_Y}$	$\overline{W_Y}$	MODE	DQ$_X$	DQ$_Y$
Lo	X	X	X	X	X	Master Reset	High Z	High Z
Hi	Lo	Hi	X	X	X	Transparent X-Y	Data In	DQ$_X$
Hi	Lo	Lo	X	X	X	Transparent Y-X	DQ$_Y$	Data In
Hi	Hi	Hi	Hi	Hi	Hi	Sby X / Sby Y	High Z	High Z
Hi	Hi	Hi	Hi	Lo	Hi	Sby X / Read Y	High Z	Data Out
Hi	Hi	Hi	Hi	X	Lo	Sby X / Write Y	High Z	Data In
Hi	Hi	Lo	Hi	Hi	Hi	Read X / Sby Y	Data Out	High Z
Hi	Hi	Lo	Hi	Lo	Hi	Read X / Read Y	Data Out	Data Out
Hi	Hi	Lo	Hi	X	Lo	Read X / Write Y	Data Out	Data In
Hi	Hi	X	Lo	Hi	Hi	Write X / Sby Y	Data In	High Z
Hi	Hi	X	Lo	Lo	Hi	Write X / Read Y	Data In	Data Out
Hi	Hi	X	Lo	X	Lo	Write X / Write Y	Data In	Data In

X = Don't Care

NOTE: Truth Table logic states presume all status flags to be inactive.

FIGURE 3. BLOCK DIAGRAM


DQ
TRANSCEIVER
DQ
DIR
$\overline{G}$
$\overline{G}$
5
5
$\overline{FF}_X$ ($\overline{AF}_X$)
X-TO-Y
FIFO
64x5
$\overline{EF}_Y$ ($\overline{AE}_Y$)
$\overline{W}$
D
$\overline{R}$
Q
$\overline{RS}$
$\overline{W}_X$
X PORT
READ
&
WRITE
CONTROL
Y PORT
READ
&
WRITE
CONTROL
$\overline{R}_Y$
DQ_X
I/O
I/O
DQ_Y
$\overline{R}_X$/DIR
$\overline{W}_Y$
$\overline{RS}$
Q
$\overline{RS}$
D
$\overline{R}$
Y-TO-X
FIFO
64x5
$\overline{W}$
$\overline{EF}_X$ ($\overline{AE}_X$)
$\overline{FF}_Y$ ($\overline{AF}_Y$)

DEVICE APPLICATION/FUNCTION

The MK45264/65 contains two independent single direction FIFOs, and a bidirectional transceiver, connected via two internal three state busses to I/O drive circuits. One FIFO is pointed X-to-Y, and the other pointed Y-to-X. Either port's FIFOs can be read or written asynchronous with FIFO read or write operations on the other port. The transceiver is activated with a low on $\overline{G}$.

Once the transceiver is activated, direction is controlled by the R_X/DIR pin. A high on R_X/DIR points the transceiver X-to-Y; a low points it Y-to-X. A low on $\overline{G}$ disables FIFO operations. Activating the Transceiver during FIFO operations may result in invalid or unpredictable FIFO operation.

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_P	$t_{RL\text{-}RH}$	Read Pulse Width	55		70		ns	
t_P	$t_{WL\text{-}WH}$	Write Pulse Width	55		70		ns	
t_P	$t_{GH\text{-}RH}$	X-ceiver Disable to end of Read	55		70		ns	
t_P	$t_{GH\text{-}WH}$	X-ceiver Disable to end of Write	55		70		ns	
t_R	$t_{RH\text{-}RL}$	Read Recovery Time	20		25		ns	
t_R	$t_{WH\text{-}WL}$	Write Recovery Time	20		25		ns	
t_R	$t_{RH\text{-}WL}$	Read Write Recovery Time	20		25		ns	
t_R	$t_{WH\text{-}RL}$	Write Read Recovery Time	20		25		ns	
t_C	$t_{RL\text{-}RL}$	Read Cycle Time	75		95		ns	
t_C	$t_{WL\text{-}WL}$	Write Cycle Time	75		95		ns	
t_{DS}	$t_{DV\text{-}WH}$	Data Set Up Time	20		25		ns	
t_{DH}	$t_{WH\text{-}DX}$	Data Hold Time	5		5		ns	
t_{QL}	$t_{RL\text{-}QL}$	$\overline{R}$ Low to Outputs Low-Z	5		5		ns	2
t_A	$t_{RL\text{-}QV}$	Read Access Time		55		70	ns	3
t_{OH}	$t_{RH\text{-}QX}$	Output Hold Time	5		5		ns	3
t_{OH}	$t_{WL\text{-}QX}$	Output Hold Time	5		5		ns	3
t_{QZ}	$t_{RH\text{-}QZ}$	$\overline{R}$ High to Outputs High-Z		30		40	ns	2
t_{WQZ}	$t_{WL\text{-}QZ}$	$\overline{W}$ Low to Outputs High-Z		45		55	ns	2
t_{FL1}	$t_{WL\text{-}FFL}$	$\overline{W}$ Low to Full Flag Low		60		80	ns	4
t_{FL1}	$t_{RL\text{-}EFL}$	$\overline{R}$ Low to Empty Flag Low		60		80	ns	4
t_{FH1}	$t_{WH\text{-}EFH}$	$\overline{W}$ Hi to Empty Flag High		50		65	ns	4
t_{FH1}	$t_{RH\text{-}FFH}$	$\overline{R}$ Hi to Full Flag High		50		65	ns	4
t_{FL2}	$t_{WL\text{-}AFL}$	$\overline{W}$ Low to Almost Full Flag Low		60		80	ns	5
t_{FL2}	$t_{RL\text{-}AEL}$	$\overline{R}$ Low to Almost Empty Flag Low		60		80	ns	5
t_{FH2}	$t_{WH\text{-}AEH}$	$\overline{W}$ Hi to Almost Empty Flag High		75		95	ns	5
t_{FH2}	$t_{RH\text{-}AFH}$	$\overline{R}$ Hi to Almost Full Flag High		75		95	ns	5
t_I	$t_{WL\text{-}FFH}$	Write Protect Indeterminate		25		30	ns	6
t_I	$t_{RL\text{-}EFH}$	Read Protect Indeterminate		25		30	ns	7
t_{FR}	$t_{FFH\text{-}WL}$	Full Flag Recovery	0		0		ns	6
t_{FR}	$t_{EFH\text{-}RL}$	Empty Flag Recovery	0		0		ns	7
t_{RS}	$t_{RSL\text{-}RSH}$	Reset Pulse Width	55		70		ns	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t_{RSR}	$t_{RSH\text{-}WH}$	Reset Recovery Time	75		95		ns	
t_{RFV}	$t_{RSL\text{-}FFH}$	Reset to Full Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL\text{-}AFH}$	Reset to $\overline{AF}$ Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL\text{-}EFL}$	Reset to Empty Flag Valid		70		90	ns	3
t_{RFV}	$t_{RSL\text{-}AEL}$	Reset to $\overline{AE}$ Flag Valid		70		90	ns	3
t_{RQX}	$t_{RSL\text{-}QX}$	Outout Hold from $\overline{RS}$ Low	0		0		ns	3
t_{RQZ}	$t_{RSL\text{-}QZ}$	RS Low to Output High Z		40		50	ns	2
t_{FG}	$t_{WH\text{-}GL}$	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{FG}	$t_{RH\text{-}GL}$	FIFO Mode to X-ceiver Mode	0		0		ns	
t_{GF}	$t_{GH\text{-}WL}$	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GF}	$t_{GH\text{-}RL}$	X-ceiver Mode to FIFO Mode	5		5		ns	
t_{GQL}	$t_{GL\text{-}QL}$	$\overline{G}$ to Output Low Z	0		0		ns	2
t_{GQV}	$t_{GL\text{-}QV}$	$\overline{G}$ to Output Valid		75		95	ns	3
t_{GQX}	$t_{GH\text{-}QX}$	Output Hold from $\overline{G}$	0		0		ns	3
t_{GQZ}	$t_{GH\text{-}QZ}$	$\overline{G}$ to Output High Z		40		50	ns	2
t_{DVQV}	$t_{DV\text{-}QV}$	Input to Output Valid		55		70	ns	3
t_{DXQX}	$t_{DX\text{-}QX}$	Input to Output Invalid	10		10		ns	3
t_{DQL}	$t_{DIRV\text{-}QL}$	$\overline{R}_X$/DIR to Output Low Z	0		0		ns	2
t_{DQV}	$t_{DIRV\text{-}QV}$	$\overline{R}_X$/DIR to Output Valid		55		70	ns	3
t_{DQX}	$t_{DIRV\text{-}QX}$	Output Hold from $\overline{R}_X$/DIR	0		0		ns	3
t_{DQZ}	$t_{DIRV\text{-}QZ}$	$\overline{R}_X$/DIR to Output High Z		40		50	ns	2

NOTES

1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/5pf Output Load. See Equivalent Load Circuit B.
3. Measured w/30pf Output Load. See Equivalent Load Circuit A.
4. Applies to $\overline{EF}_X$, $\overline{FF}_X$, $\overline{FF}_Y$, $\overline{EF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
5. Applies to $\overline{AE}_X$, $\overline{AF}_X$, $\overline{AE}_Y$, $\overline{AF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
6. Writes beginning a) more than t_I (max) before $\overline{FF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{FF}$ goes high may be performed. c) t_{FR} (min) after $\overline{FF}$ goes high will be performed.
7. Reads beginning a) more than t_I (max) before $\overline{EF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{EF}$ goes high may be performed. c) t_{FR} (min) after $\overline{EF}$ goes high will be performed.

Read/Write

The FIFOs utilize separate Read and Write enable inputs to control port activity and direction. A low on a Read Enable reads a port's receive FIFO. A high on a Read Enable or a low on a Write Enable disables a port's data outputs to a high impedance state. A low on a Write Enable initiates a write to a port's transmit FIFO, regardless of the state of Read Enable. Input data is latched into the FIFO on the rising edge of a Write Enable.

Full/Empty Flags

An active Full Flag indicates that a port's transmit FIFO is full and will accept no more data. Writes done to a FIFO while full are blocked. Once a read has occurred on a full FIFO, clearing a location in the FIFO, the Full Flag will go inactive, allowing another write to begin on the next falling edge of Write Enable.

An active Empty Flag indicates a port's receive FIFO is empty and can send no more data. Any reads done on a FIFO while empty are blocked. Once a write to an empty FIFO has occurred, the Empty Flag will go inactive, allowing another read to begin on the next falling edge of Read Enable.

Almost Flags

An inactive Almost Full flag indicates a port's transmit FIFO has room for at least four (4) more bytes, which is to say the flag will go active during the fourth write from full and stay active until after the fourth location from full has been vacated (read). An inactive Almost Empty flag indicates a port's receive FIFO has at least four (4) bytes of data in memory, ready to be read, which is to say that the flag will go active while reading the fourth remaining byte and remain active until after the fourth byte has been stored (written).

Reset

Reset is initiated by a low on the Master Reset ($\overline{RS}$) input. A reset returns all data outputs to a high impedance state, taking precedence over the read strobes ($\overline{R_X}$/DIR and $\overline{R_Y}$) and $\overline{G}$. The states of the FIFO control inputs ($\overline{R_X}$/DIR, $\overline{W_X}$, $\overline{R_Y}$ and $\overline{W_Y}$) are a Don't Care throughout reset. The read strobes are a Don't Care at the end of reset because the Empty Flag becomes active (goes low) during reset, blocking any attempted reads. The write strobes ($\overline{W_X}$ and $\overline{W_Y}$) may fall any time during or after reset, but must not go high until t_{RSR} after $\overline{RS}$ goes high.

FIGURE 4. WRITE TIMING

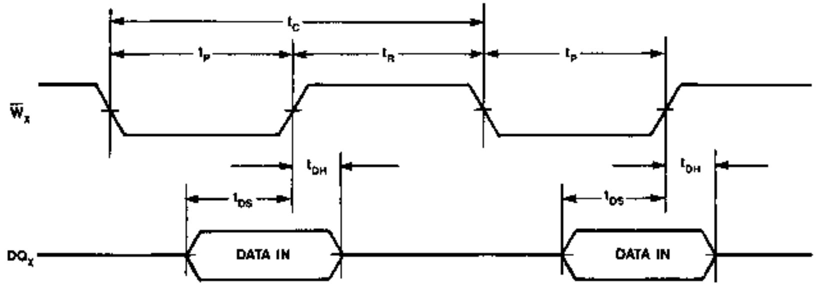


FIGURE 5. READ TIMING

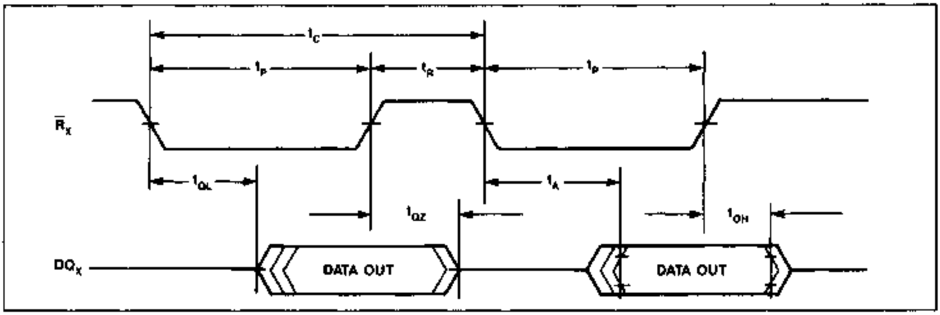

t_C
t_P
t_R
t_P
$\overline{R}_X$
t_{QL}
t_A
t_{QZ}
t_{OH}
DQ_X
DATA OUT
DATA OUT

FIGURE 6. WRITE/READ TIMING

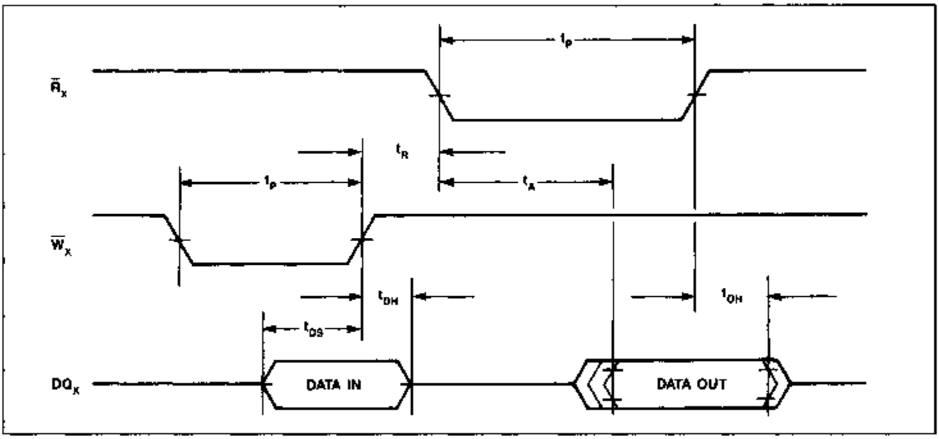

t_P
$\overline{R}_X$
t_R
t_P
t_A
$\overline{W}_X$
t_{DH}
t_{OH}
t_{DS}
DQ_X
DATA IN
DATA OUT

FIGURE 7. READ/WRITE TIMING

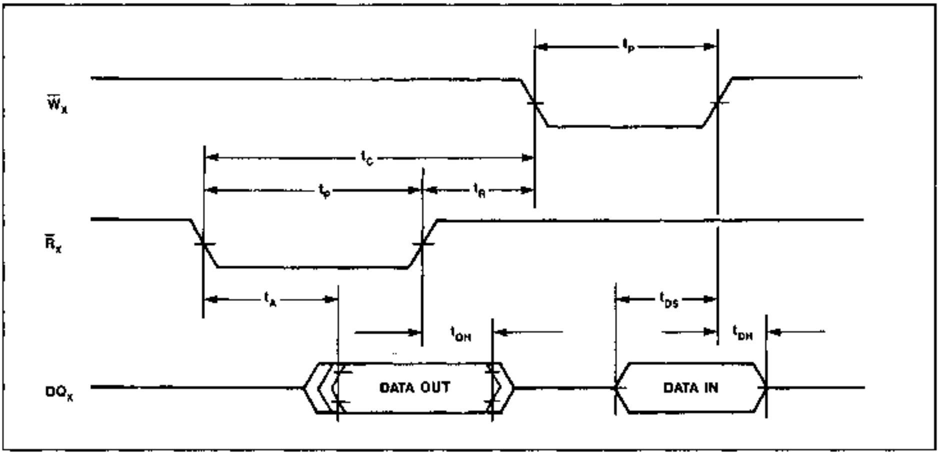

t_P
$\overline{W}_X$
t_C
t_P
t_R
$\overline{R}_X$
t_A
t_{DS}
t_{OH}
t_{DH}
DQ_X
DATA OUT
DATA IN

FIGURE 8. FULL (ALMOST FULL) FLAG TIMING

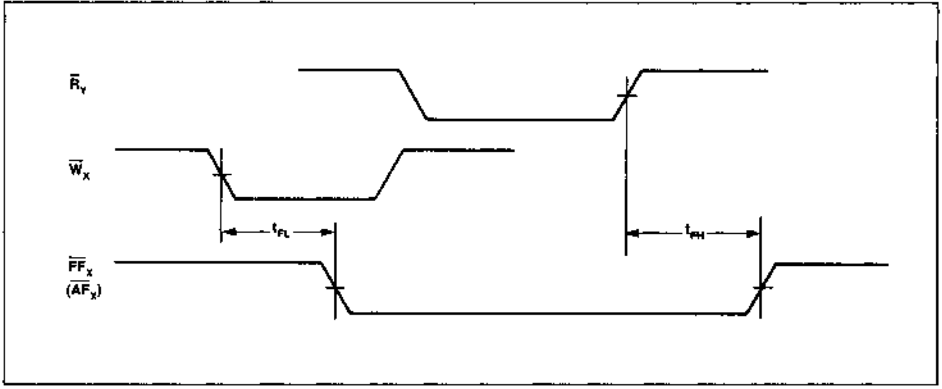

$\overline{R}_Y$
$\overline{W}_X$
t_{FL}
t_{FH}
$\overline{FF}_X$
$(\overline{AF}_X)$

FIGURE 9. EMPTY (ALMOST EMPTY) FLAG TIMING

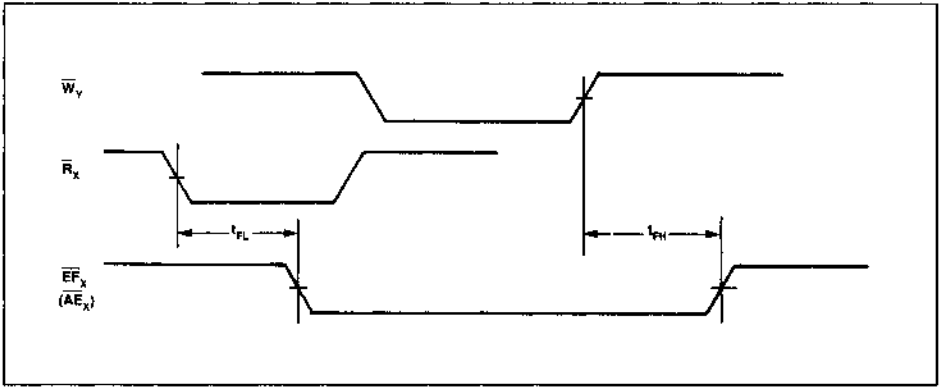

$\overline{W}_Y$
$\overline{R}_X$
t_{FL}
t_{FH}
$\overline{EF}_X$
$(\overline{AE}_X)$

FIGURE 10. FIRST WRITE AFTER FULL TIMING

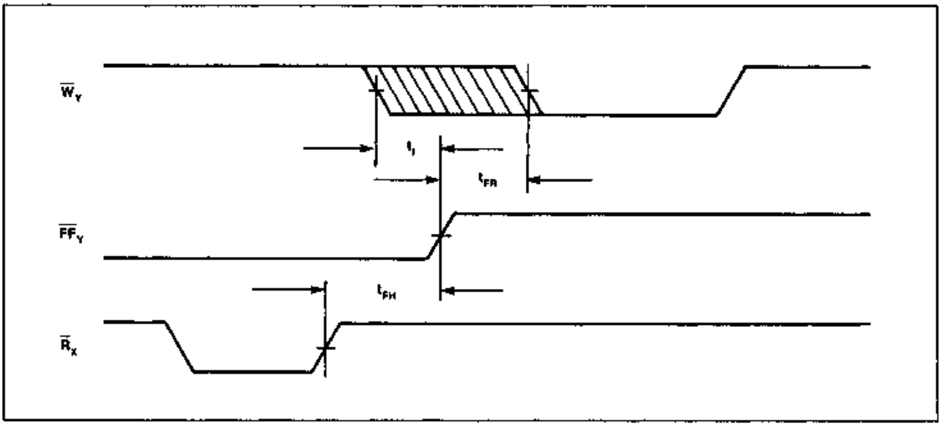
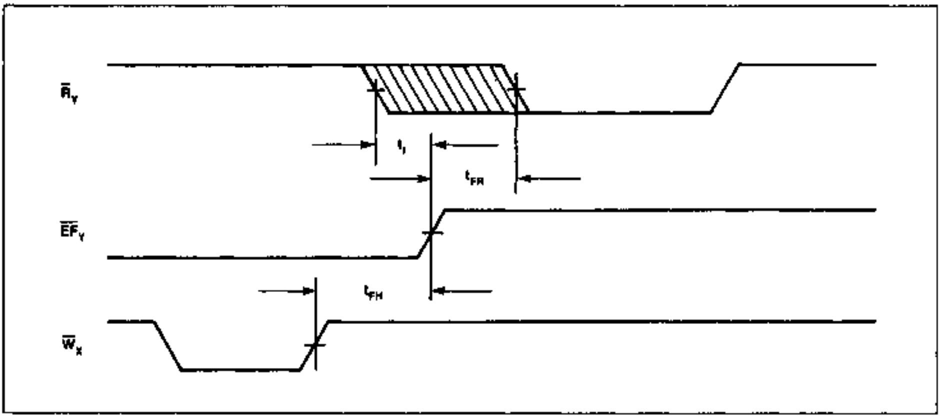
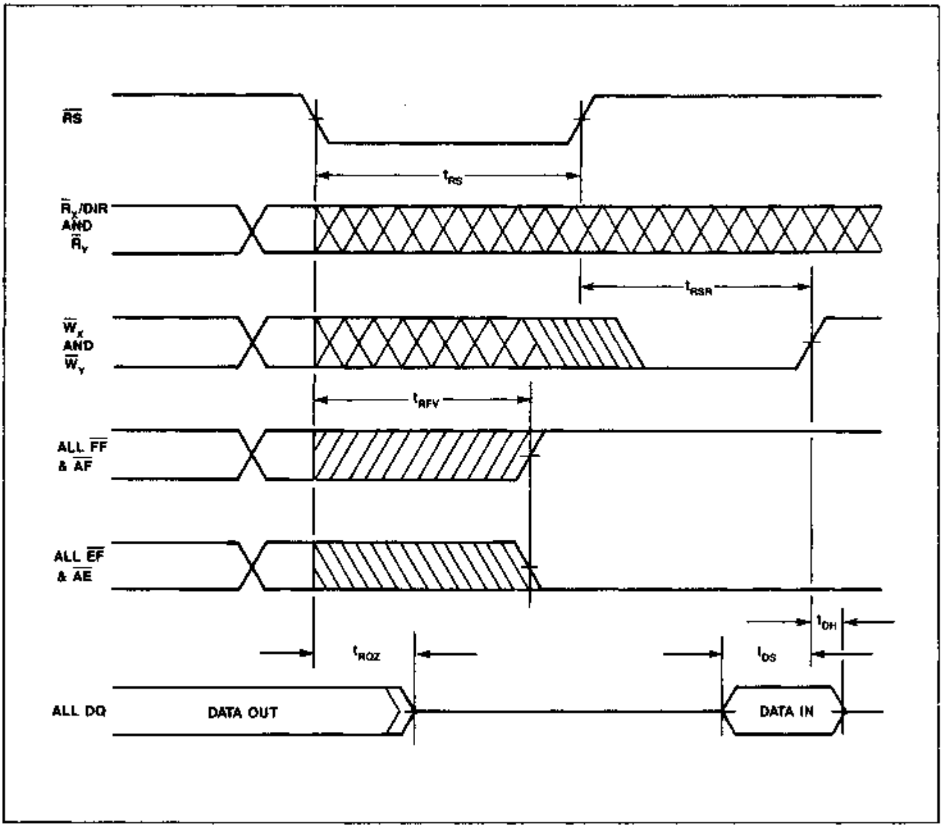

$\overline{W}_Y$
t_I
t_{FR}
$\overline{FF}_Y$
t_{FH}
$\overline{R}_X$

FIGURE 11. FIRST READ AFTER EMPTY TIMING



$\overline{R}_Y$
t_I
t_{FR}
$\overline{EF}_Y$
t_{FH}
$\overline{W}_X$

FIGURE 12. FIFO RESET TIMING



$\overline{RS}$
t_{RS}
$\overline{R}_X$/DIR AND $\overline{R}_Y$
t_{RSR}
$\overline{W}_X$ AND $\overline{W}_Y$
t_{RFV}
ALL $\overline{FF}$ & $\overline{AF}$
ALL $\overline{EF}$ & $\overline{AE}$
t_{DH}
t_{RQZ}
t_{DS}
ALL DQ
DATA OUT
DATA IN

FIGURE 13. TRANSCEIVER RESET TIMING (EXAMPLE SHOWN WITH $\overline{R_X}$/DIR HIGH)

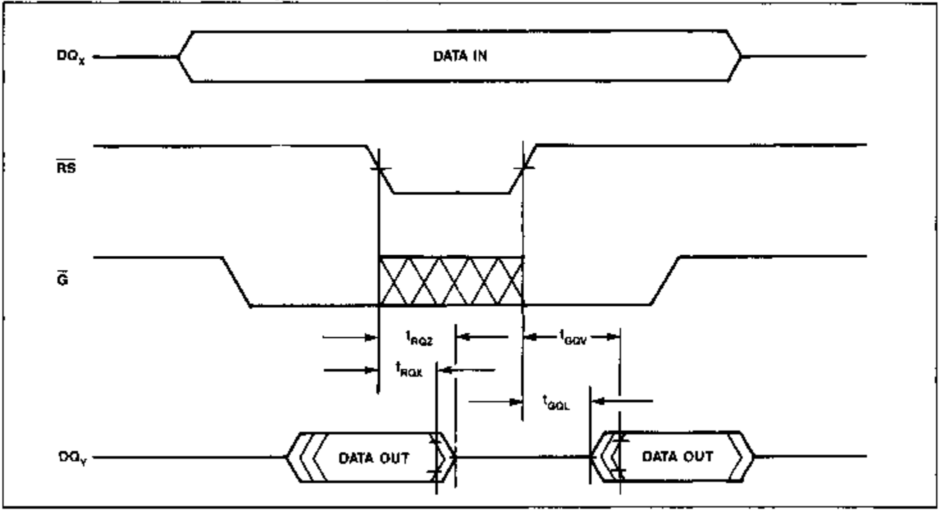

DQ_X
DATA IN
$\overline{RS}$
$\overline{G}$
t_{RQZ}
t_{GQV}
t_{RQX}
t_{GQL}
DQ_Y
DATA OUT
DATA OUT

FIGURE 14. FIFO MODE/TRANSCEIVER MODE TRANSITION

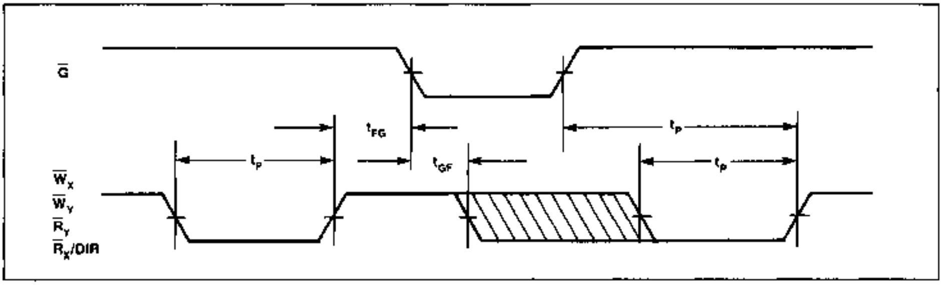

$\overline{G}$
t_{FG}
t_P
t_P
t_{GF}
t_P
$\overline{W}_X$
$\overline{W}_Y$
$\overline{R}_Y$
$\overline{R}_X$/DIR

FIGURE 15. TRANSCEIVER $\overline{G}$ TIMING (EXAMPLE SHOWN WITH $\overline{R_X}$/DIR HIGH)

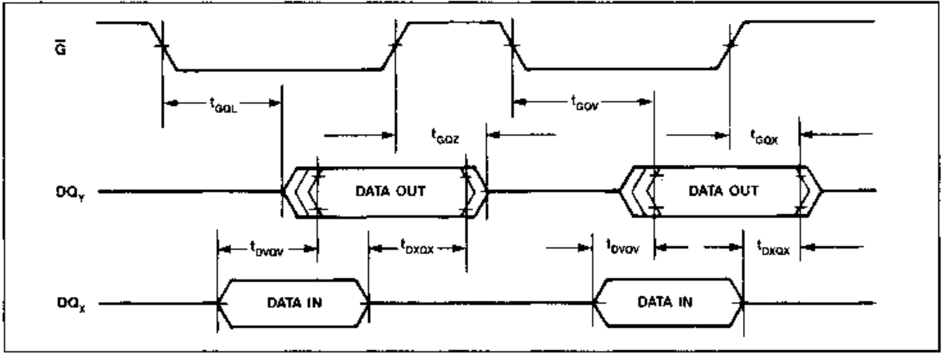

$\overline{G}$
t_{GQL}
t_{GQV}
t_{GQZ}
t_{GQX}
DQ_Y
DATA OUT
DATA OUT
t_{DVQV}
t_{DXQX}
t_{DVQV}
t_{DXQX}
DQ_X
DATA IN
DATA IN

FIGURE 16. TRANSCEIVER $\overline{R}_X$/DIR TIMING (EXAMPLE SHOWN WITH $\overline{G}$ LOW)

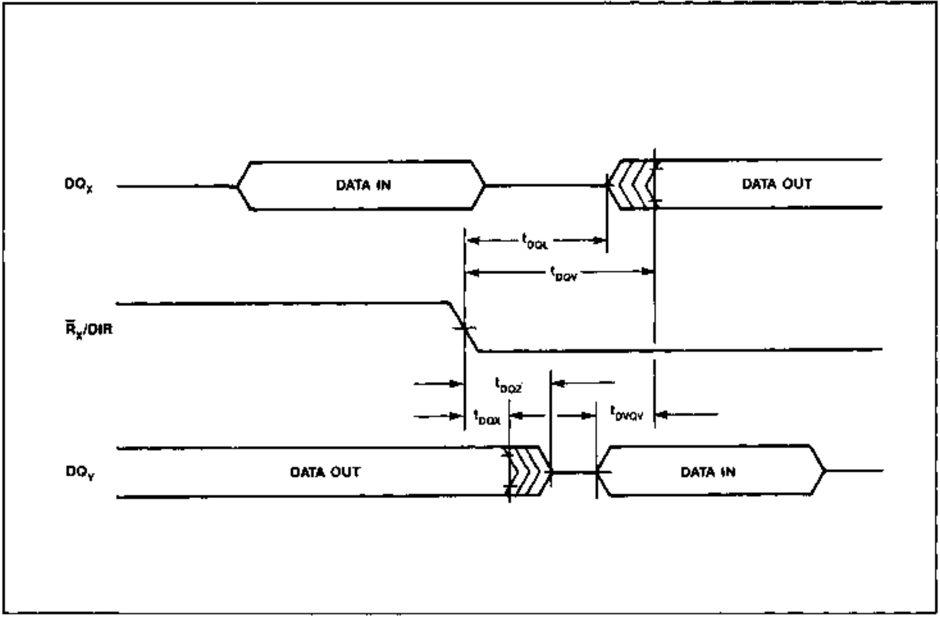

DQ$_X$
DATA IN
DATA OUT
t_{DQL}
t_{DQV}
$\overline{R}_X$/DIR
t_{DQZ}
t_{DQX}
t_{DVQV}
DQ$_Y$
DATA OUT
DATA IN

FIGURE 17. WRITE/ALMOST FULL/FULL FLAG TIMING SUMMARY

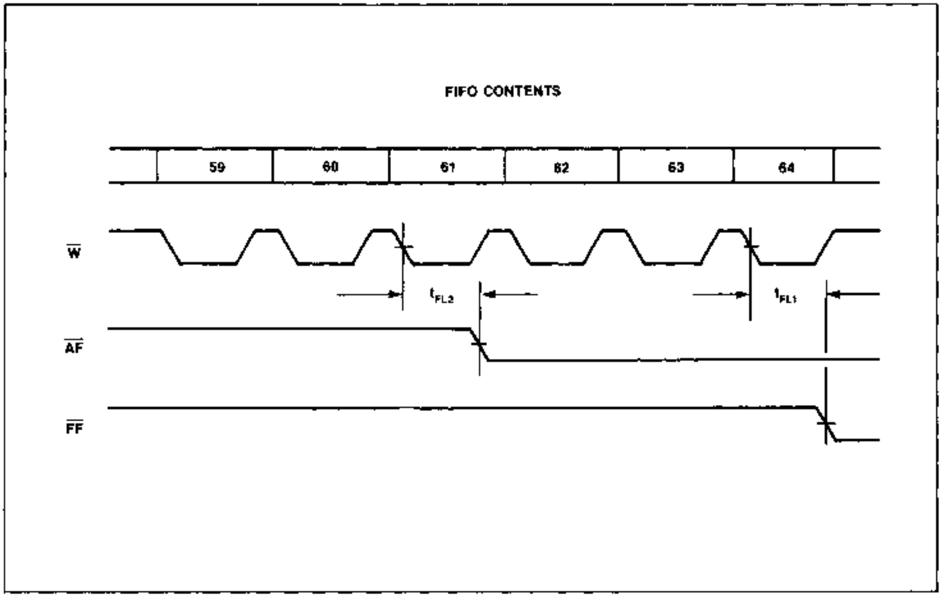

FIFO CONTENTS
59
60
61
62
63
64
$\overline{W}$
t_{FL2}
t_{FL1}
$\overline{AF}$
$\overline{FF}$

FIGURE 18. WRITE/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

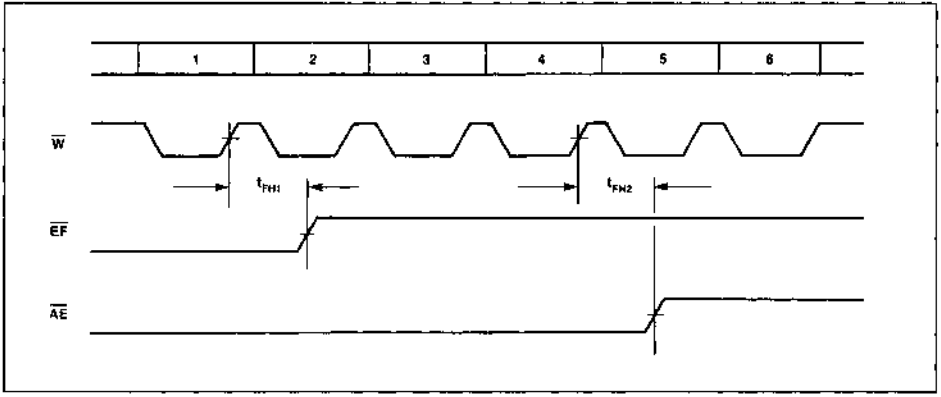

1
2
3
4
5
6
W̅
t_{FH1}
t_{FH2}
E̅F̅
A̅E̅

FIGURE 19. READ/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

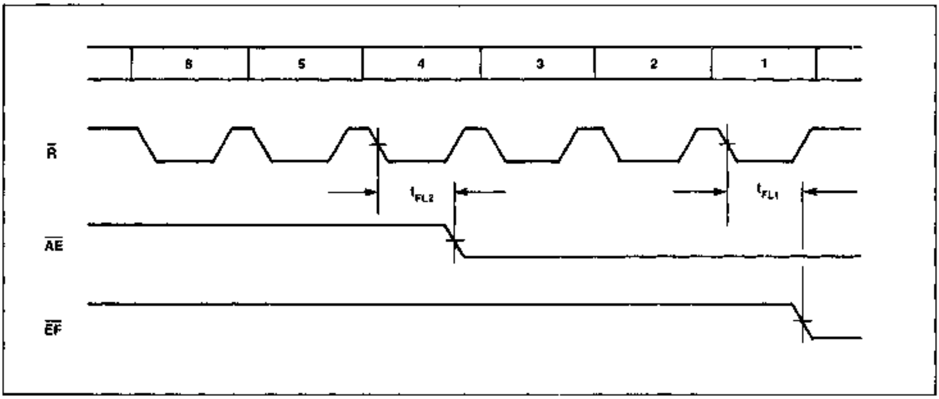
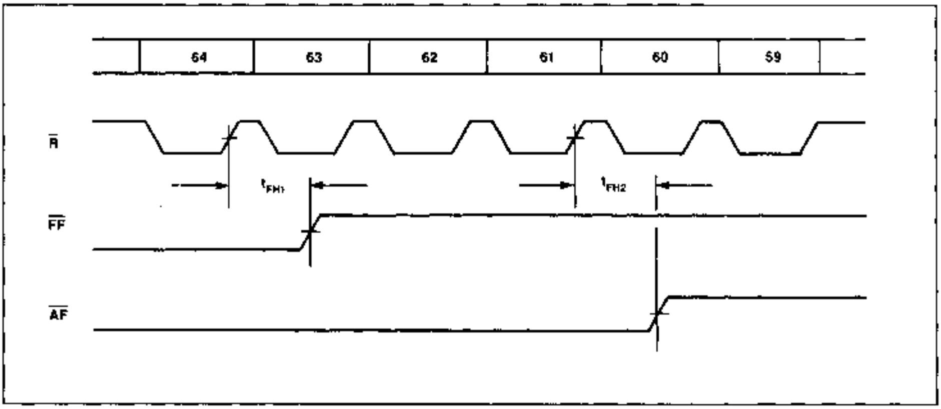

6
5
4
3
2
1
R̅
t_{FL2}
t_{FL1}
A̅E̅
E̅F̅

FIGURE 20. READ/ALMOST FULL/FULL FLAG TIMING SUMMARY


64
63
62
61
60
59
R̅
t_{FH1}
t_{FH2}
F̅F̅
A̅F̅

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . −1.5V to +7.0V
Ambient Operating Temperature (T_A) . . . . 0° to +70°C
Ambient Temperature under Bias . . . . −55° to +125°C
Ambient Storage Temperature (Plastic) . . . . −55° to +125°C
Allowable Total Device Power Dissipation . . . . 1 Watt
Allowable RMS Output Current per pin . . . . 80 mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0° to +70°C)

SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		V_{CC}+0.3	V	1
V_{IL}	Logic 0 Input	−0.3		0.8	V	1

NOTE: 1. All voltages referenced to V_{SS}.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70° C, V_{CC} = 5.0 ± 10%)

SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
I_{CCQ}	Quiescent Power Supply Current, per Port			5	mA	1,2
I_{CCA}	Active Power Supply Current, per Port			10	mA	1,3
I_{CCD}	Dynamic Power Supply Current, per Port			1.2	mA/MHz	1,4
I_{CCT}	Total Power Supply Current, both Ports			60	mA	1,5
I_{IL}	Input Leakage Current	−1		+1	μA	6
I_{OL}	Output Leakage Current	−10		+10	μA	7
V_{OH}	Logic 1 Output Voltage	2.4			V	7,8
V_{OL}	Logic 0 Output Voltage			0.4	V	7,9

NOTES

1. Measured with outputs open.
2. Measured with opposite port quiescent; $\overline{R}$, $\overline{W}$ and $\overline{G} \geq V_{IH}$ (Min).
3. Measured with opposite port quiescent; $\overline{R}$ or $\overline{W} \leq V_{IL}$ (Max) and $\overline{G} \geq V_{IH}$ (Min.).
4. Measured with opposite port quiescent; $\overline{R}$ or $\overline{W}$ toggling and $\overline{G} \geq V_{IH}$ (Min.).
5. Measured with both ports operating at t_C (Min.).
6. Measured with V_{IN} = 0.0V to V_{CC}.
7. All voltages referenced to V_{SS}.
8. Data Output Pins (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = −12mA; Flag Output Pins $\overline{EF}_X$, $\overline{EF}_Y$, $\overline{FF}_X$, $\overline{FF}_Y$, AE_X, $\overline{AE}_Y$, $\overline{AF}_X$, $\overline{AF}_Y$) I_{OUT} = −1mA.
9. Data Outputs (DQ_{X0}-DQ_{X4} and DQ_{Y0}-DQ_{Y4}) I_{OUT} = 12mA; Flag Output Pins $\overline{EF}_X$, $\overline{EF}_Y$, $\overline{FF}_X$, $\overline{FF}_Y$, AE_X, $\overline{AE}_Y$, $\overline{AF}_X$, $\overline{AF}_Y$) I_{OUT} = 4mA.

CAPACITANCE

(T_A = 0° to 70°C, V_{CC} = 5.0 ± 10%)

SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
C_I	Input Capacitance		4	5	pf	1
C_O	Output Capacitance		8	10	pf	1

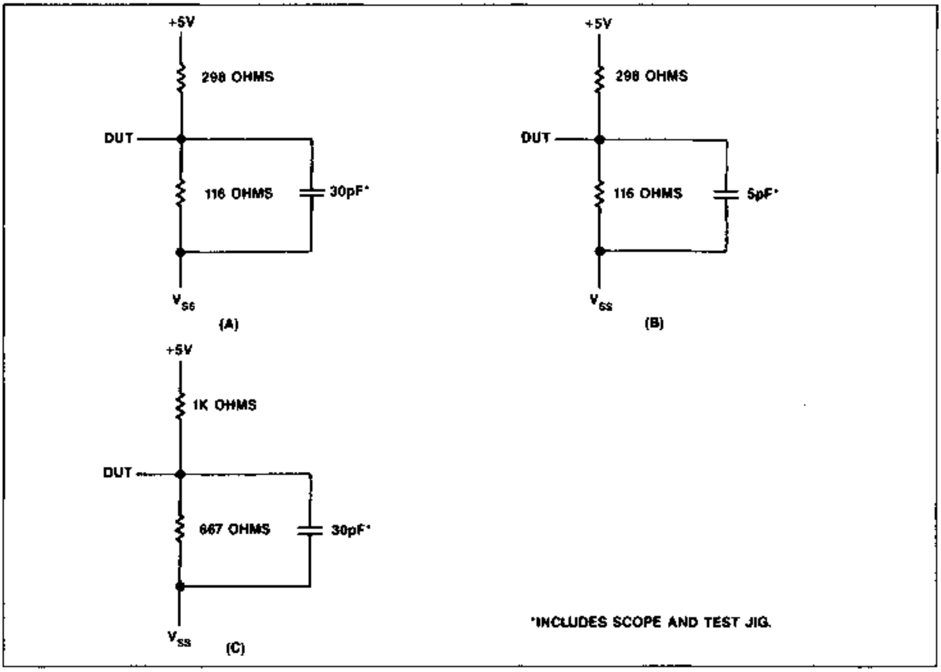
NOTE: 1. Sampled, not 100% tested. Measured at 1MHz.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0° to 70°C

V_{CC} = 5.0 Volts ± 10%

FIGURE 21. EQUIVALENT OUTPUT LOAD CIRCUIT



*INCLUDES SCOPE AND TEST JIG.

APPLICATION ISSUES

Width Expansion

The MK45264/65 is designed to be used in sets of two or more, as shown below. The MK45264/65 is supplied in two configurations, MK45264 and MK45265; the MK45264 having Empty and Full Flags, the MK45265 having Almost Empty and Almost Full Flags. This scheme allows a pair of devices to be connected in such a way as to assure that the PAIR present a full complement of status flags in BOTH directions, that is, both to the left and to the right.

The resulting 10 bit wide configuration allows both parity AND beginning or end of message flag bits to be carried along with an 8 bit byte of data. The 20 bit wide configuration allows carrying 2 bits of parity AND separate message start and stop bits in 16 bit applications.

The MK45264/65 was designed as a 5 bit wide device in order to allow the use of a 300 mil DIP package; allowing the MK45264/65 to: a) achieve the highest function/board space ratio possible for a fully featured bidirectional BiPORT FIFO, b) provide higher performance with improved noise margins than would be possible in higher pin count packages, and c) provide greater flexibility to users of various bus widths.

FIGURE 22. (64x10)x2 WIDTH EXPANSION

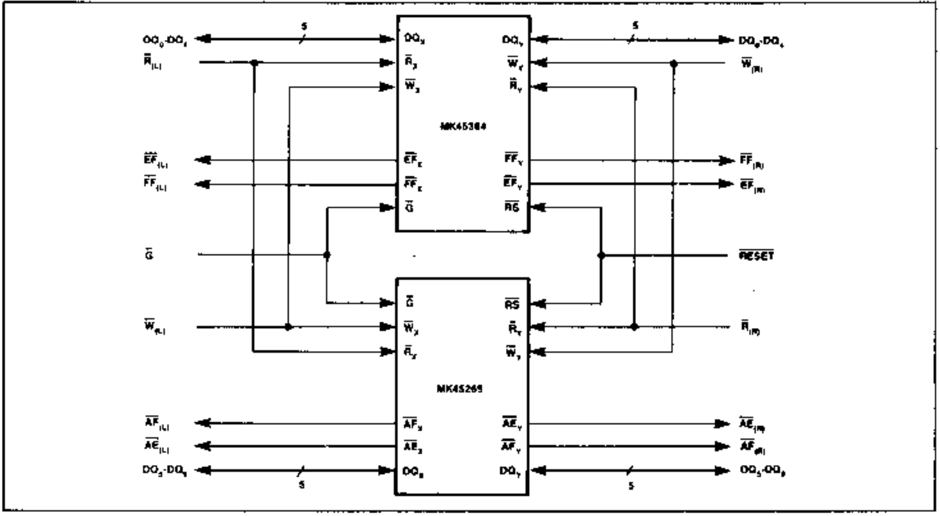
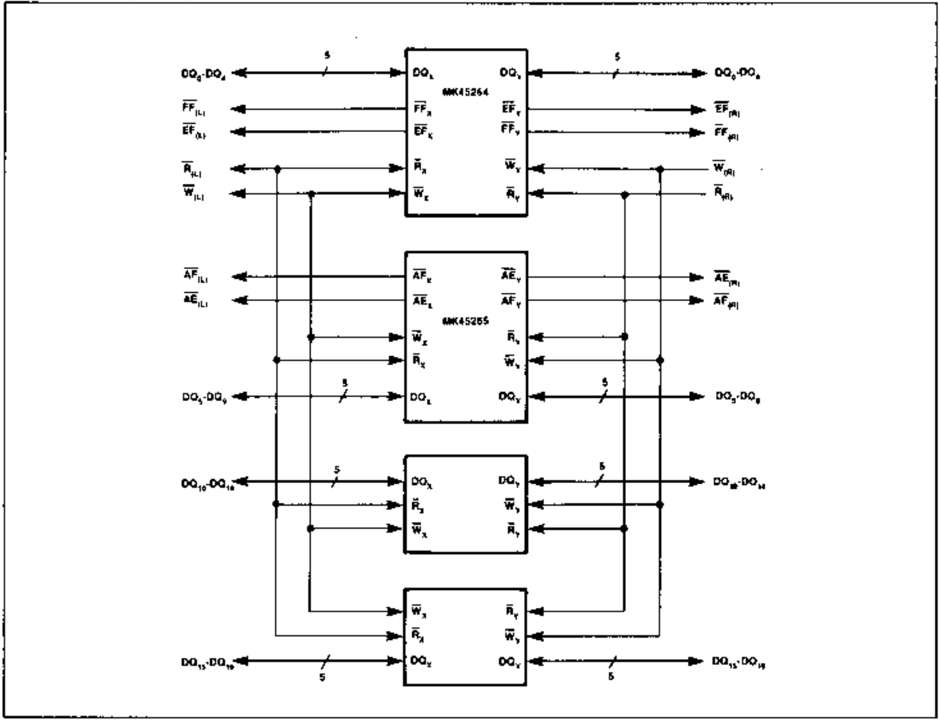

DQ0-DQ4
R(L)
5
DQX
RX
WX
MK45264
DQY
WY
RY
5
DQ0-DQ4
W(R)
EF(L)
FF(L)
EFX
FFX
G
FFY
EFY
RS
FF(R)
EF(R)
G
RESET
G
WX
RX
MK45265
RS
RY
WY
W(L)
R(R)
AF(L)
AE(L)
DQ5-DQ9
AFX
AEX
DQX
AEY
AFY
DQY
AE(R)
AF(R)
DQ5-DQ9
5
5

FIGURE 23. (64x20)x2 WIDTH EXPANSION


DQ0-DQ4
5
DQX
MK45264
DQY
5
DQ0-DQ4
FF(L)
EF(L)
FFX
EFX
EFY
FFY
EF(R)
FF(R)
R(L)
W(L)
RX
WX
WY
RY
W(R)
R(R)
AF(L)
AE(L)
AFX
AEX
MK45265
AEY
AFY
AE(R)
AF(R)
WX
RX
RY
WY
DQ5-DQ9
5
DQX
DQY
5
DQ5-DQ9
DQ10-DQ14
5
DQX
RX
WX
DQY
WY
RY
5
DQ10-DQ14
WX
RX
DQX
RY
WY
DQY
DQ15-DQ19
5
5
DQ15-DQ19

Width Expansion and Word-Skew

Word-skew, in this context, is defined as what happens when FIFOs that are wired in parallel for width expansion get out of sync with one another. Halting writes when full and reads when empty circumvents the problems altogether. Reading while empty and writing while full should, therefore, be avoided. The problem of word-skew can emerge if one is using the MK45264/65 in width expansion mode AND writing (or reading) WHILE full (or WHILE empty).

Slight differences in Full (or Empty) Flag response delays between different devices may result in "disagreements" between adjacent devices as they go from Full to Not Full or from Empty to Not Empty; resulting in one device accepting an attempted write (or read) while an adjacent device blocks the cycle. The simplest approach to avoiding word skew is configuring the system using the FIFOs to begin reading only when the Almost Empty flag has gone high, rather than right after the Empty flag has gone high. In like manner, waiting to write until the Almost Full flag goes high, rather than right after the Full flag goes high will prevent the problem, which is why the Almost flags are provided. However, should such a scheme prove unworkable in a particular appication, the addition of an external flag latching circuit can also solve the problem.

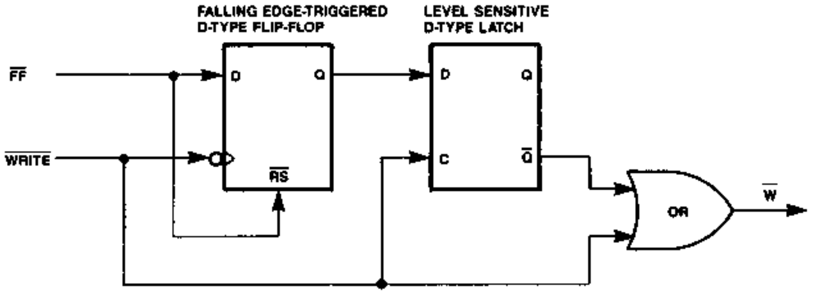
The circuit shown below, when connected to the Write strobe and Full Flag, latches the status of the flag at the beginning of a write. If the flag is inactive, the Write strobe is passed through to the FIFO. When the flag goes active (low) the falling-edge triggered flop is reset. The reset flop, in concert with the level-sensitive latch and the OR gate block the write strobe.

Tying the Flag to the Reset input of the edge-triggered flop assures that the Write strobe is blocked on the first write attempted after the flag falls. The level sensitive latch also prevents transitions in the flag from disturbing cycles that are already in progress. In the event that a write is begun just as the flag is going inactive (high) the falling edge-triggered flop will latch its interpretation of the metastable flag. If it interprets the metastable input as being low, the present and next cycle are blocked, as were their predecessors. If it interprets the flag as being high, the present cycle is still blocked, because the the level sensitive latch was still seeing an active flag as the cycle began. However, the next attempted cycle is passed through.

Although "throwing away" write cycles goes against the grain conceptually, it does not actually present a problem in this situation. It must be assumed that Writing while Full or Reading while Empty would only be allowed in applications where the write and/or read strobes are proceeding regardless of FIFO status anyway. "Throwing away" reads or writes cannot, by definition, be considered an error.

Remember, overall signal timing must comprehend the delays of the particular components chosen to implement the external circuit.

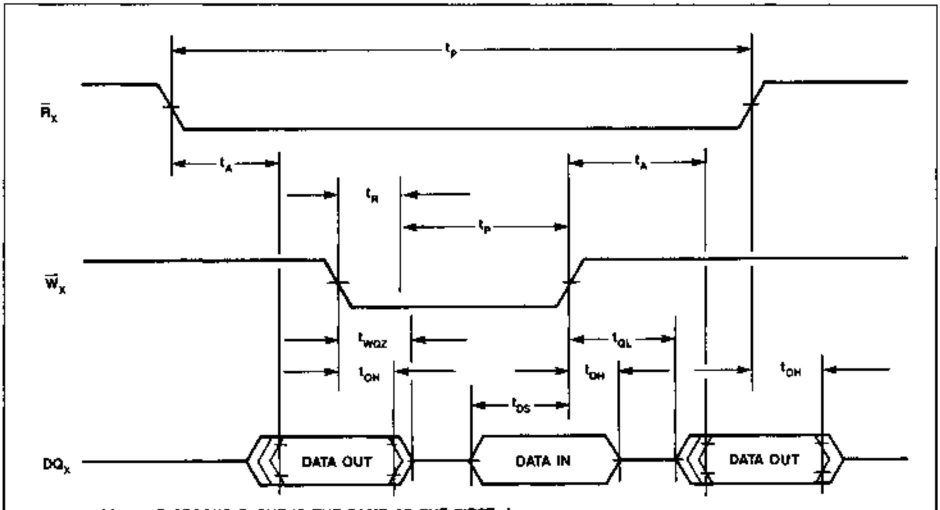
FIGURE 24. EXTERNAL ANTI-WORD-SKEW CIRCUIT



Overlapping Read and Write Strobes

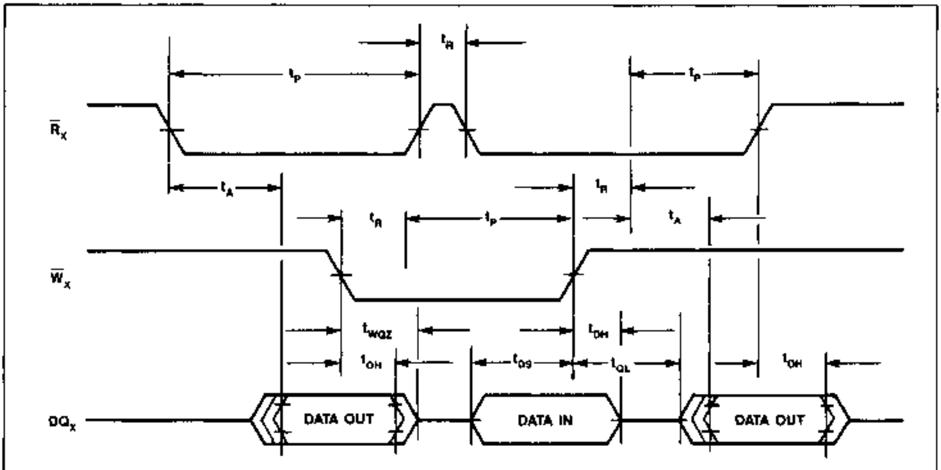
Overlapping Read and Write strobes on a given port is neither tested nor recommended. The following timing diagrams are provided only to illustrate the relationship between the control functions.

FIGURE 25. OVERLAPPING READ/WRITE TIMING


t_P
$\bar{R}_X$
t_A
t_A
t_R
t_P
$\bar{W}_X$
t_{WQZ}
t_{QL}
t_{OH}
t_{OH}
t_{OH}
t_{DS}
DQ_X
DATA OUT
DATA IN
DATA OUT

NOTE: THE SECOND D OUT IS THE SAME AS THE FIRST. A OVERLAPPING WRITE DOES NOT INCREMENT THE READ ADDRESS COUNTER.

FIGURE 26. OVERLAPPING READ/WRITE TIMING


t_R
t_P
t_P
$\bar{R}_X$
t_A
t_R
t_R
t_P
t_A
$\bar{W}_X$
t_{WQZ}
t_{OH}
t_{OH}
t_{DS}
t_{QL}
t_{OH}
DQ_X
DATA OUT
DATA IN
DATA OUT

NOTE: THE SECOND D OUT IS NOT THE SAME AS THE FIRST. IT IS, IN FACT, THE NEXT READ DATA. AN OVERLAPPING WRITE DOES NOT BLOCK THE READ STROBE FROM INCREMENTING THE READ ADDRESS COUNTER.

ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK45264N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45264N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C

STATIC RAM DEVICES

VERY FAST STATIC RAM

MK41H66/
MK41H67(N,P)-20/25/35

16K × 1 CMOS STATIC RAM

- 20, 25, AND 35 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 20-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUT AND OUTPUT PINS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- 50 µA CMOS STANDBY CURRENT (MK41H67)
- HIGH SPEED CHIP SELECT (MK41H66)
- JEDEC STANDARD PINOUT

MK41H66 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

X = Don't Care

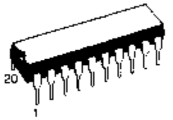
MK41H67 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

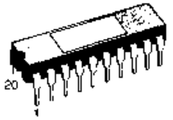
DESCRIPTION

The MK41H66 and MK41H67 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H67 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

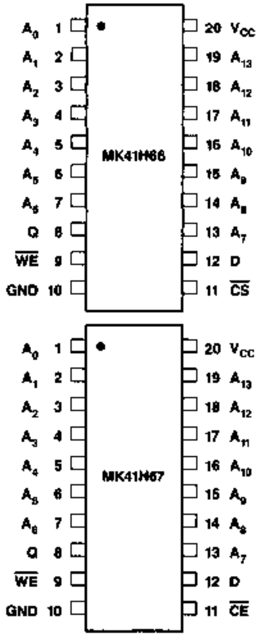


N
DIP-20
(Plastic Package)



P
DIP-20
(Ceramic Package)

FIGURE 1. PIN CONNECTIONS


A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
Q 8
WE 9
GND 10
20 VCC
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
13 A7
12 D
11 CS
MK41H66
A0 1
A1 2
A2 3
A3 4
A4 5
A5 6
A6 7
Q 8
WE 9
GND 10
20 VCC
19 A13
18 A12
17 A11
16 A10
15 A9
14 A8
13 A7
12 D
11 CE
MK41H67

PIN NAMES

A_0 - A_{13} - Address	$\overline{WE}$ - Write Enable
$\overline{CE}$ - Chip Enable (MK41H67)	GND - Ground
$\overline{CS}$ - Chip Select (MK41H66)	V_{CC} - + 5 volts
	D - Data In
	Q - Data Out

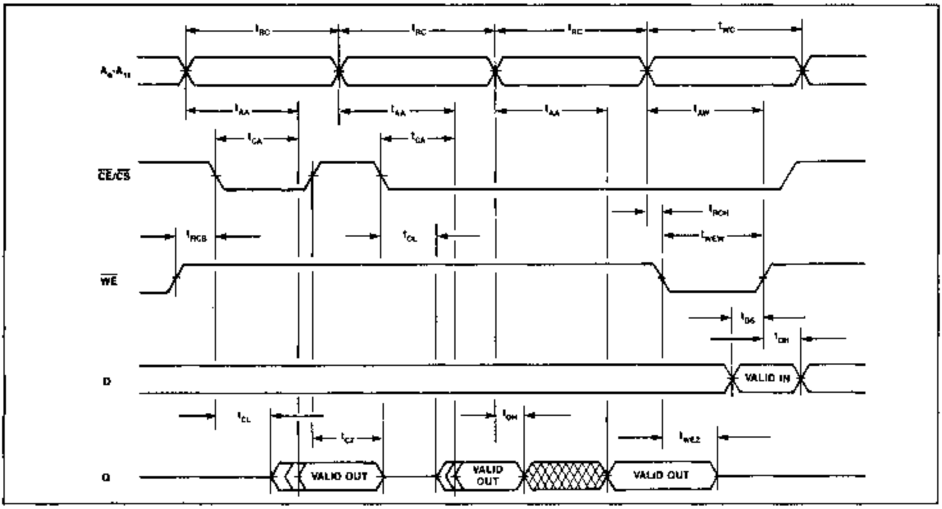
The MK41H66 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

OPERATIONS

READ MODE

The MK41H66/7 is in the Read Mode whenever $\overline{\text{WE}}$ (Write Enable) is high and $\overline{\text{CE}}/\overline{\text{CS}}$ (Chip Enable/Select) is low, providing a ripple-through access to any one of 16,384 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{\text{CE}}/\overline{\text{CS}}$ access time is satisfied. If $\overline{\text{CE}}/\overline{\text{CS}}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the $\overline{\text{CE}}/\overline{\text{CS}}$, and $\overline{\text{WE}}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

FIGURE 2. READ-READ-READ-WRITE TIMING



READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

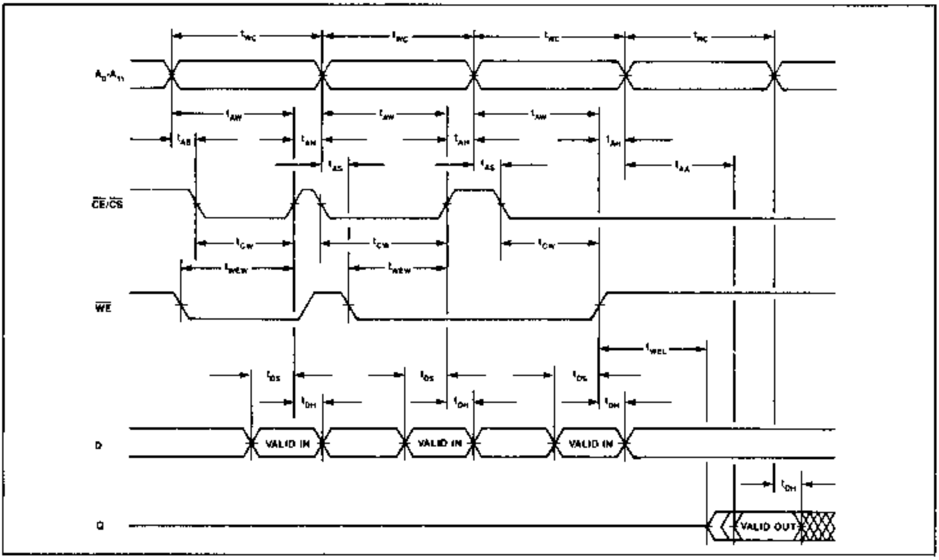
SYM	PARAMETER	MK41H6X-20 MIN	MK41H6X-20 MAX	MK41H6X-25 MIN	MK41H6X-25 MAX	MK41H6X-35 MIN	MK41H6X-35 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H67)	5		5		5		ns	2
t_{CL}	Chip Select to Low-Z (MK41H66)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41H67)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H66)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H67)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H66)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H66/7 is in the Write Mode whenever the $\overline{\text{WE}}$ and $\overline{\text{CE}}/\overline{\text{CS}}$ inputs are in the low state. $\overline{\text{CE}}/\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{\text{WE}}$ and $\overline{\text{CE}}/\overline{\text{CS}}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{\text{CE}}/\overline{\text{CS}}$, or $\overline{\text{WE}}$.

If the output is enabled ($\overline{\text{CE}}/\overline{\text{CS}}$ is low), then $\overline{\text{WE}}$ will return the output to high impedance within t_{WEZ} of its falling edge. Data-In must remain valid t_{DH} after the rising edge of $\overline{\text{CE}}/\overline{\text{CS}}$ or $\overline{\text{WE}}$.

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING

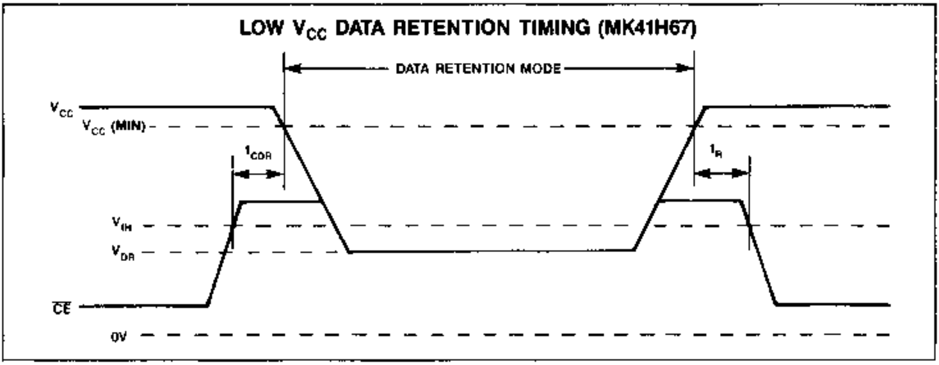


WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H6X-20 MIN	MK41H6X-20 MAX	MK41H6X-25 MIN	MK41H6X-25 MAX	MK41H6X-35 MIN	MK41H6X-35 MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 4. DATA RETENTION TIMING


LOW V_{CC} DATA RETENTION TIMING (MK41H67)
DATA RETENTION MODE
V_{CC}
V_{CC} (MIN)
t_{CDR}
t_R
V_{IH}
V_{DR}
$\overline{CE}$
0V

LOW V_{CC} DATA RETENTION CHARACTERISTICS

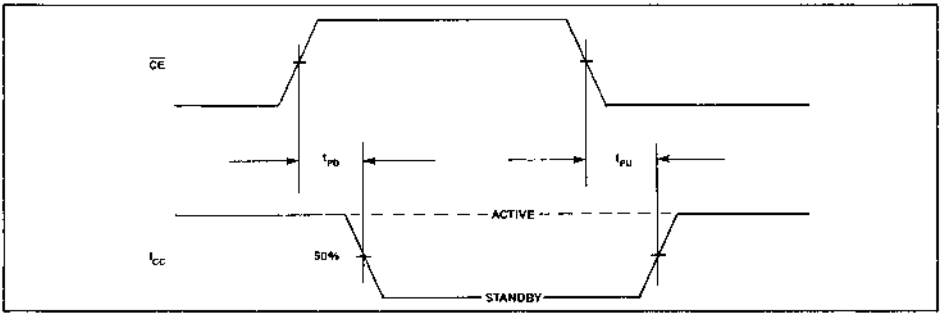
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	7
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	7
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H67 Only)

The MK41H67 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE TIMING


$\overline{CE}$
t_{PD}
t_{PU}
ACTIVE
I_{CC}
50%
STANDBY

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H67-20		MK41H67-25		MK41H67-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H66/7 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H66/7 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H66/7, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND	−1.0 V to +7.0 V
Ambient Operating Temperature (T_A)	0°C to +70°C
Ambient Storage Temperature (Plastic)	−55°C to +125°C
Ambient Storage Temperature (Ceramic)	−65°C to +150°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		$V_{CC}+1.0$	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.1		0.8	V	3, 4

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	5
I_{CC2}	TTL Standby Current (MK41H67 only)		10	mA	6
I_{CC3}	CMOS Standby Current (MK41H67 only)		50	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on Q pins	8	10	pF	5, 10

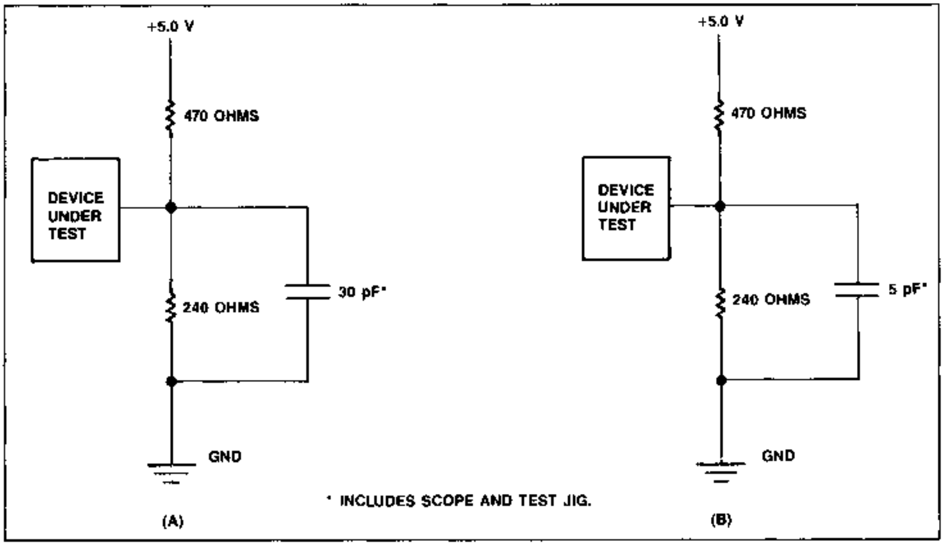
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. V_{IL} may undershoot to −2.0 volts for 200ns or less during input transitions.
5. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
6. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
7. V_{CC} (max) $\geq \overline{CE} \geq V_{CC} - 0.3$ V GND + 0.3 V $\geq A_0$-$A_{13} \geq V_{IL}$ (min) or V_{IH} (max) $\geq A_0$-$A_{13} \geq V_{CC} - 0.3$ V. All Other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
9. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE/CS}$ = V_{IH} and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS



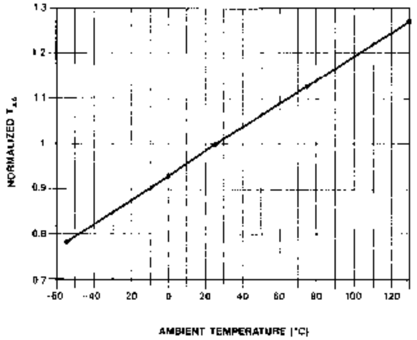
* INCLUDES SCOPE AND TEST JIG.

(A)

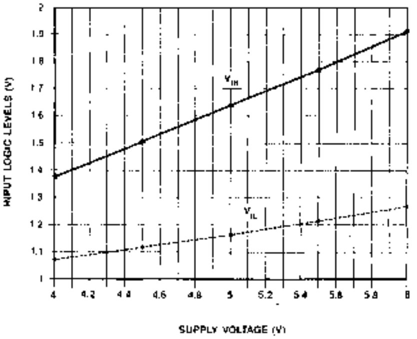
(B)

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

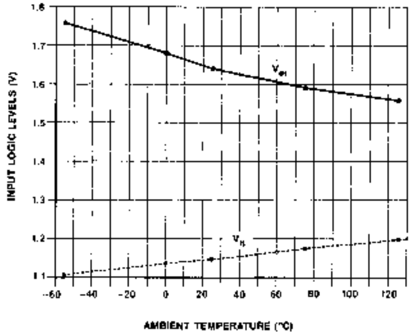
NORMALIZED CHIP ENABLE ACCESS TIME VS. AMBIENT TEMPERATURE V_{CC}=5.0V



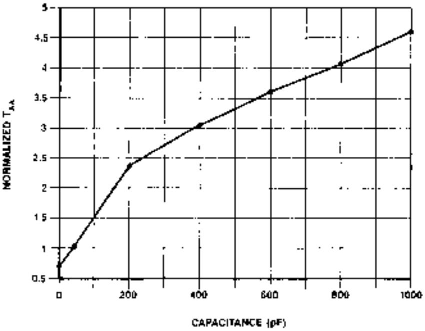
LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A=25°C



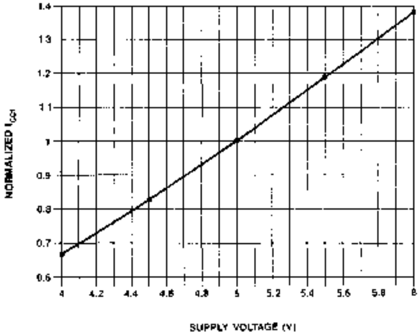
LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC}=5.0V



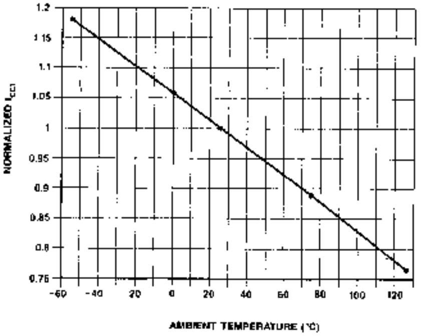
NORMALIZED ACCESS TIME VS. OUTPUT LOADING V_{CC}=5.0 V T_A=25°C



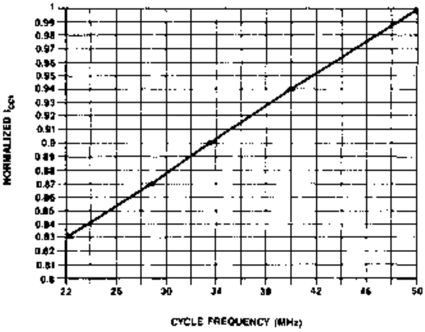
NORMALIZED SUPPLY CURRENT VS. SUPPLY VOLTAGE T_A=0°C



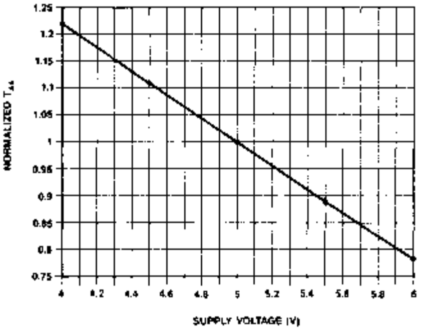
NORMALIZED SUPPLY CURRENT VS. AMBIENT TEMPERATURE V_{CC}=5.0V



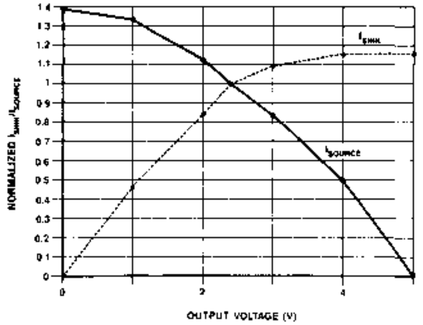
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



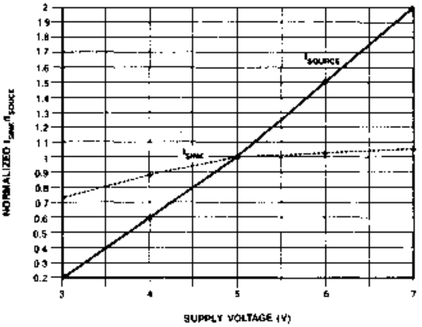
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME V_{CC}=5.0V T_A=25°C



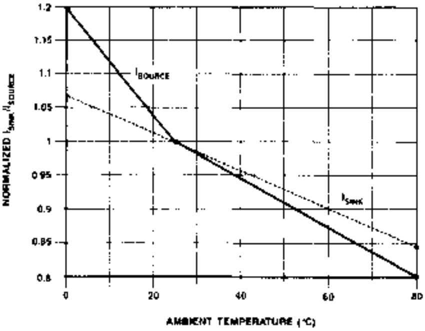
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE VOLTAGE V_{CC}=5.0V T_A=25°C



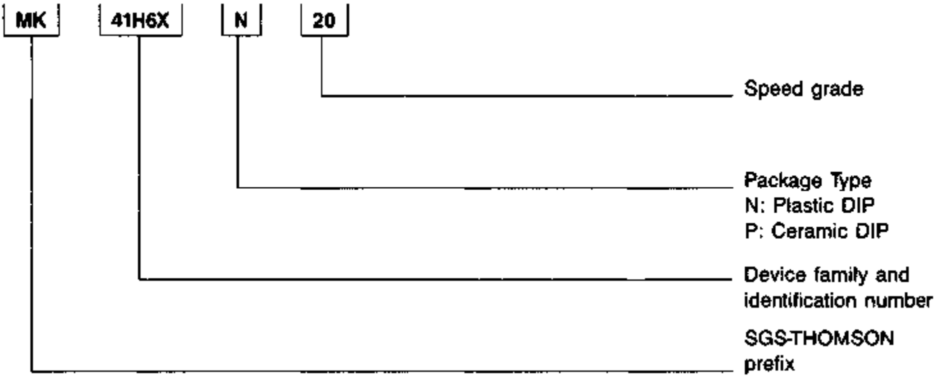
NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C



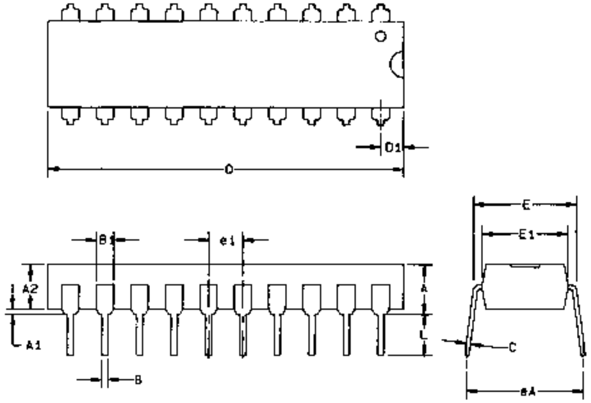
NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H67N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H66N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H67P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H67P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H67P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H66P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C


MK
41H6X
N
20
Speed grade
Package Type
N: Plastic DIP
P: Ceramic DIP
Device family and
identification number
SGS-THOMSON
prefix

20 PIN "N" PACKAGE, PLASTIC DIP

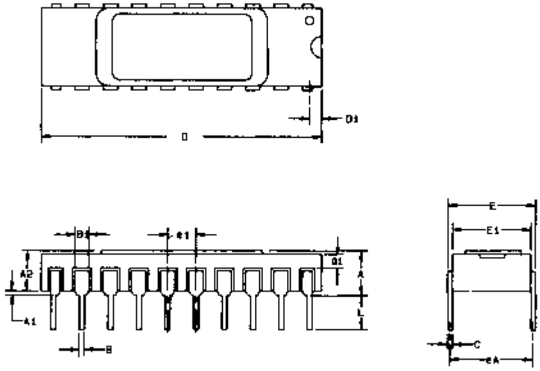


Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

20 PIN "P" PACKAGE, SIDE BRAZED CERAMIC DIP



Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	.015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	24.511	25.273	.965	.995	
D1	0.635	1.397	.025	.055	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.048	—	.120	—	
Q1	0.127	—	.005	—	

NOTES

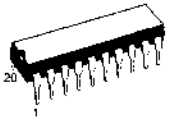
1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

SGS-THOMSON
MICROELECTRONICS

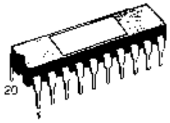
MK41H68/ MK41H69(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

- 20, 25, AND 35 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 20-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- 50 µA CMOS STANDBY CURRENT (MK41H68)
- TTL STANDBY CURRENT UNAFFECTED BY ADDRESS ACTIVITY (MK41H68)
- HIGH SPEED CHIP SELECT (MK41H69)
- JEDEC STANDARD PINOUT



N
DIP-20
(Plastic Package)



P
DIP-20
(Ceramic Package)

MK41H68 TRUTH TABLE

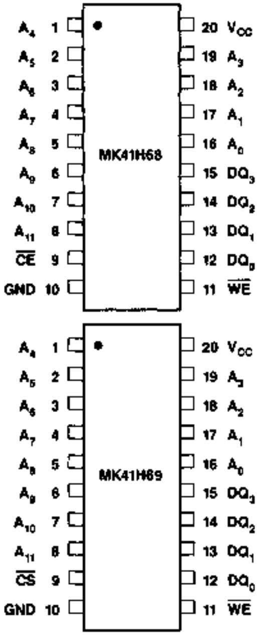
$\overline{CE}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

MK41H69 TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	DQ	Power
H	X	Deselect	High Z	Active
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

X = Don't Care

FIGURE 1. PIN CONNECTIONS


A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
CE 9
GND 10
20 VCC
19 A3
18 A2
17 A1
16 A0
15 DQ3
14 DQ2
13 DQ1
12 DQ0
11 WE
MK41H68
A4 1
A5 2
A6 3
A7 4
A8 5
A9 6
A10 7
A11 8
CS 9
GND 10
20 VCC
19 A3
18 A2
17 A1
16 A0
15 DQ3
14 DQ2
13 DQ1
12 DQ0
11 WE
MK41H69

PIN NAMES

A_0 - A_{11}	Address	$\overline{WE}$	Write Enable
DQ_0 - DQ_3	Data I/O	GND	Ground
$\overline{CE}$	Chip Enable (MK41H68)	V_{CC}	+ 5 volts
$\overline{CS}$	Chip Select (MK41H69)		

DESCRIPTION

The MK41H68 and MK41H69 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Both require only a single +5V ± 10 percent power supply. Both devices are fully TTL compatible.

The MK41H68 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced to microwatt levels by raising the $\overline{CE}$ pin to the full V_{CC} voltage.

The MK41H69 Chip Select pin provides a high speed chip select access, allowing fast read cycles despite decoder delays.

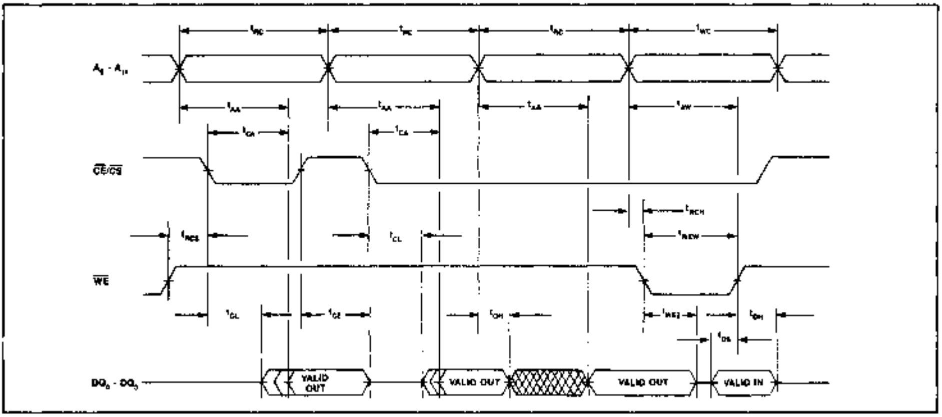
OPERATIONS

READ MODE

The MK41H68/9 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}/\overline{CS}$ (Chip Enable/Select) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}/\overline{CS}$ access time is satisfied. If $\overline{CE}/\overline{CS}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}/\overline{CS}$, and $\overline{WE}$ control signals. The data lines may be in an indeterminate state at t_{CL}, but the data lines will always have valid data at t_{AA}.

FIGURE 2. READ-READ-READ-WRITE TIMING



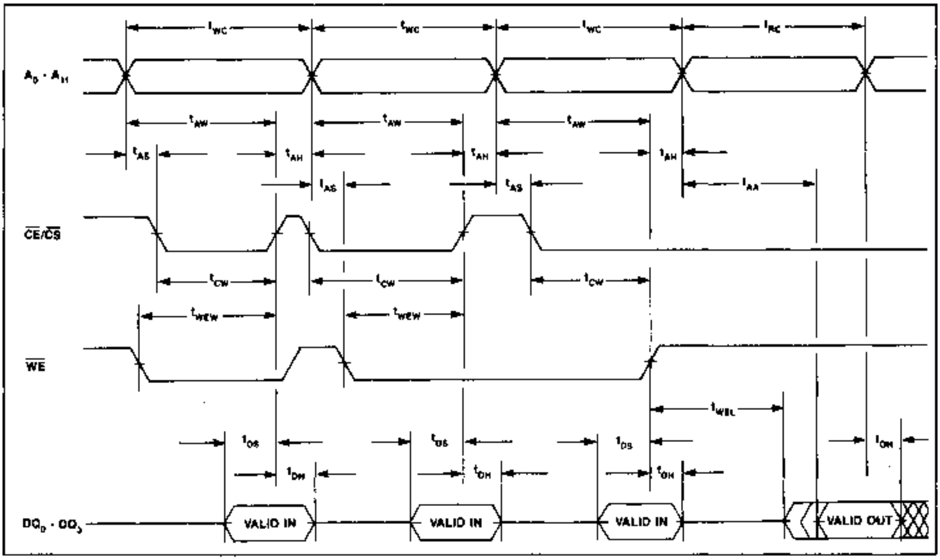
READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CL}	Chip Enable to Low-Z (MK41H68)	7		7		7		ns	2
t_{CL}	Chip Select to Low-Z (MK41H69)	5		5		5		ns	2
t_{CA}	Chip Enable Access Time (MK41H68)		20		25		35	ns	1
t_{CA}	Chip Select Access Time (MK41H69)		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CZ}	Chip Enable to High-Z (MK41H68)		8		10		13	ns	2
t_{CZ}	Chip Select to High-Z (MK41H69)		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

WRITE MODE

The MK41H68/9 is in the Write Mode whenever the $\overline{\text{WE}}$ and $\overline{\text{CE}}/\overline{\text{CS}}$ inputs are in the low state. $\overline{\text{CE}}/\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{\text{WE}}$ and $\overline{\text{CE}}/\overline{\text{CS}}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{\text{CE}}/\overline{\text{CS}}$, or $\overline{\text{WE}}$. If the output is enabled ($\overline{\text{CE}}/\overline{\text{CS}}$ is low), then $\overline{\text{WE}}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{\text{CE}}/\overline{\text{CS}}$ or $\overline{\text{WE}}$.

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING

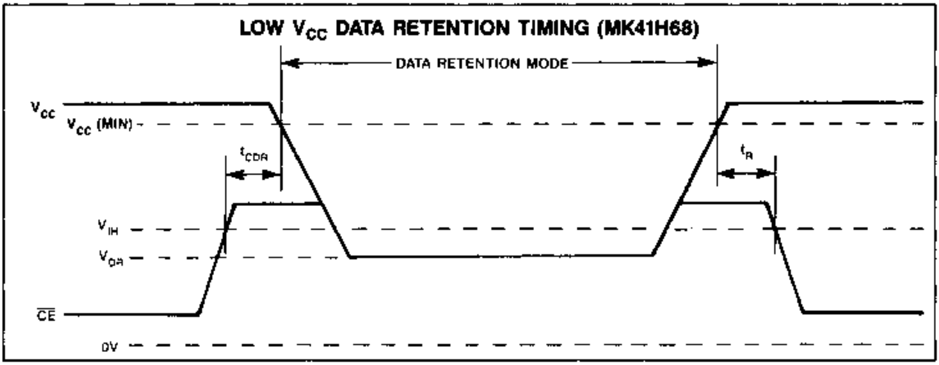


WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0$ V ± 10 percent)

		MK41H6X-20		MK41H6X-25		MK41H6X-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable/Select to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 4. DATA RETENTION TIMING


LOW V_{CC} DATA RETENTION TIMING (MK41H68)
DATA RETENTION MODE
V_{CC}
V_{CC} (MIN)
t_{CDR}
t_R
V_{IH}
V_{DR}
$\overline{CE}$
0V

LOW V_{CC} DATA RETENTION CHARACTERISTICS

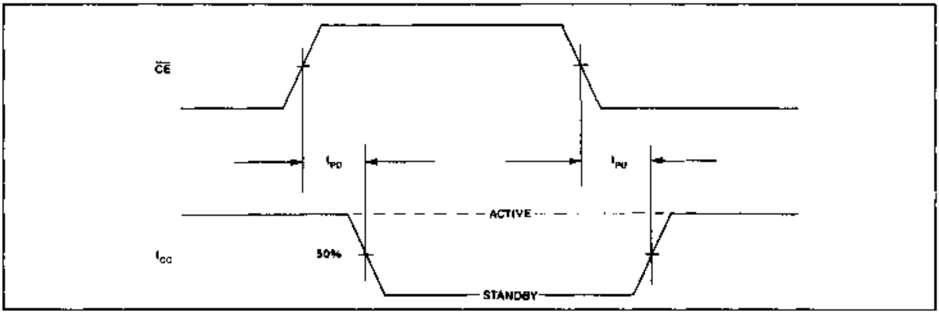
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	6
I_{CCDR}	Data Retention Power Supply Current	—	50	μA	6
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE (MK41H68 Only)

The MK41H68 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE TIMING


$\overline{CE}$
t_{PD}
t_{PU}
ACTIVE
I_{CC}
50%
STANDBY

STANDBY MODE
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

		MK41H68-20		MK41H68-25		MK41H68-35			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H68/9 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H68/9 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H68/9, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 μF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND	−1.0 V to +7.0 V
Ambient Operating Temperature (T_A)	0°C to +70°C
Ambient Storage Temperature (Plastic)	−55°C to +125°C
Ambient Storage Temperature (Ceramic)	−65°C to +150°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	4
I_{CC2}	TTL Standby Current (MK41H68 only)		8	mA	5
I_{CC3}	CMOS Standby Current (MK41H68 only)		50	μA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	5,9

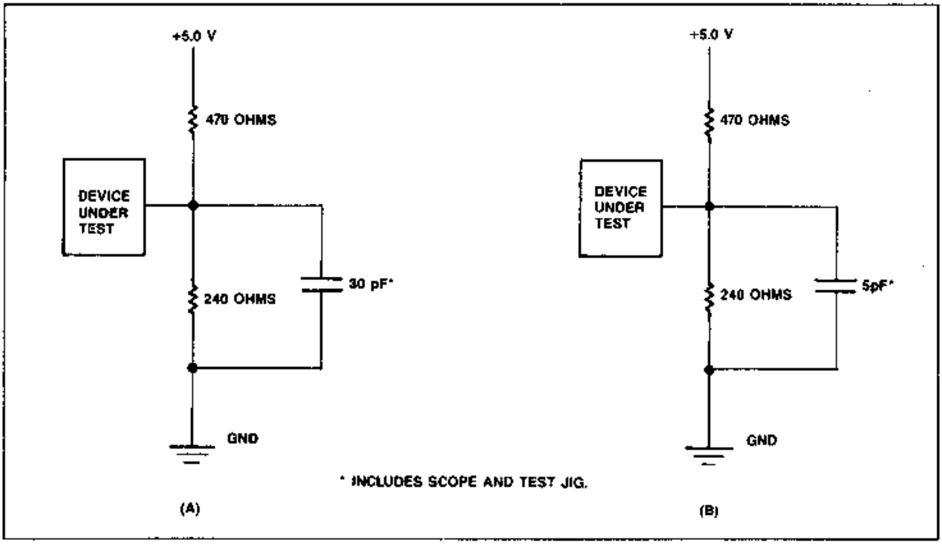
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
5. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
6. V_{CC} (max) $\geq \overline{CE} \geq V_{CC}$ − 0.3 V, All Other Inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}/\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

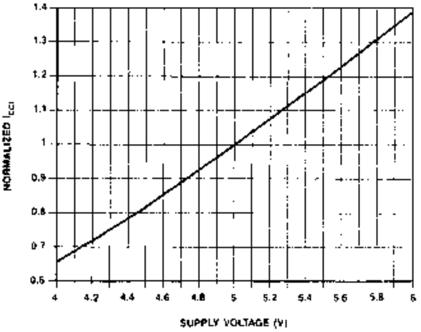
FIGURE 6. OUTPUT LOAD CIRCUITS



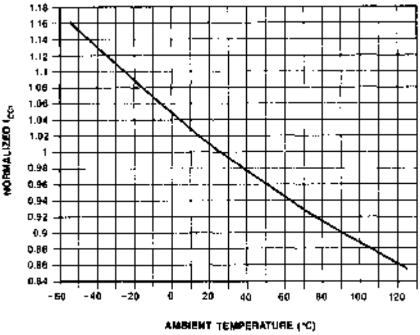
* INCLUDES SCOPE AND TEST JIG.

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

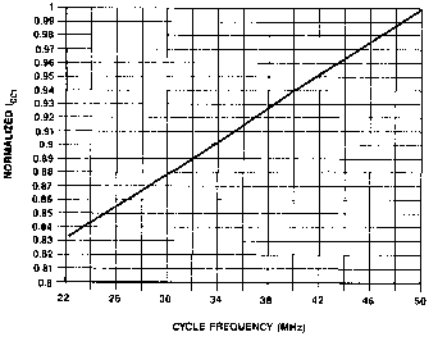
NORMALIZED SUPPLY CURRENT VS.
SUPPLY VOLTAGE $T_A = 0°C$



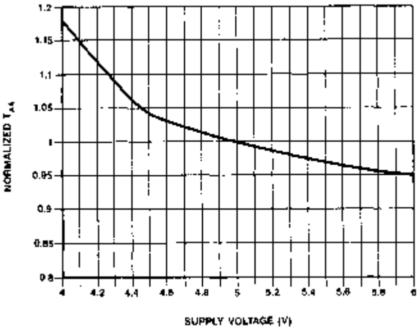
NORMALIZED SUPPLY CURRENT VS.
AMBIENT TEMPERATURE $V_{CC} = 5.0V$



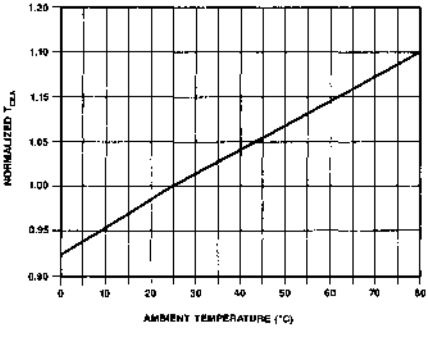
NORMALIZED SUPPLY CURRENT VS.
CYCLE TIME $V_{CC} = 5.0V$ $T_A = 25°C$



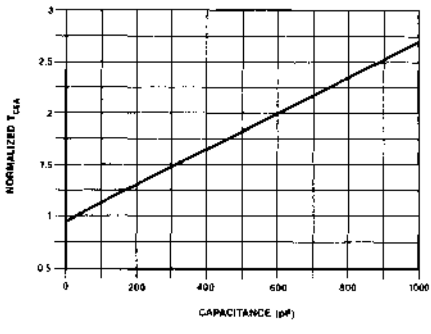
NORMALIZED ACCESS TIME VS.
SUPPLY VOLTAGE $T_A = 25°C$



NORMALIZED ACCESS TIME VS.
AMBIENT TEMPERATURE $V_{CC} = 5.0V$

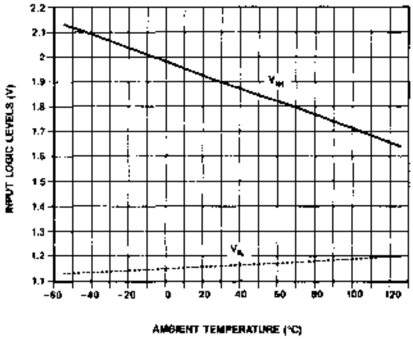


NORMALIZED ACCESS TIME VS.
OUTPUT LOADING $V_{CC} = 5.0V$ $T_A = 25°C$

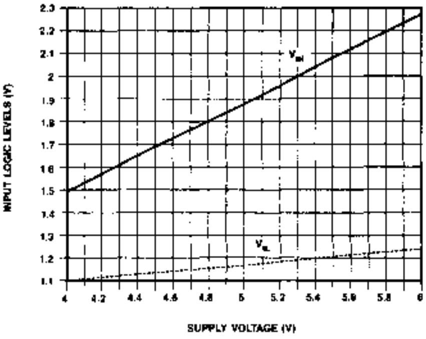


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

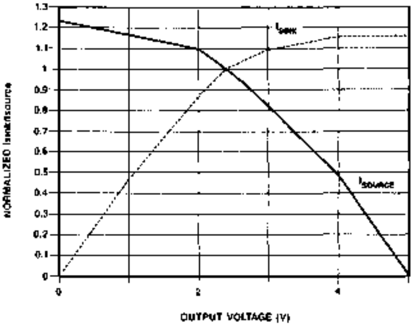
LOGIC THRESHOLD VOLTAGE VS.
AMBIENT TEMPERATURE V_{CC}=5.0V



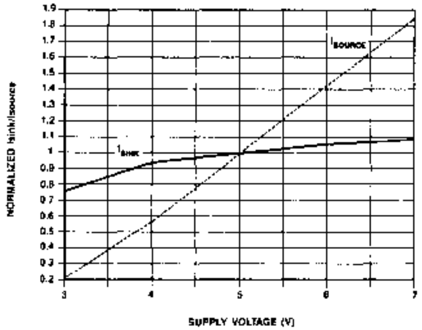
LOGIC THRESHOLD VOLTAGE VS.
SUPPLY VOLTAGE T_A=25°C



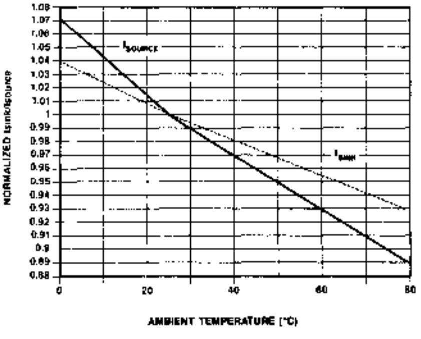
NORMALIZED SOURCE AND SINK CURRENTS VS.
OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS.
SUPPLY VOLTAGE T_A=25°C

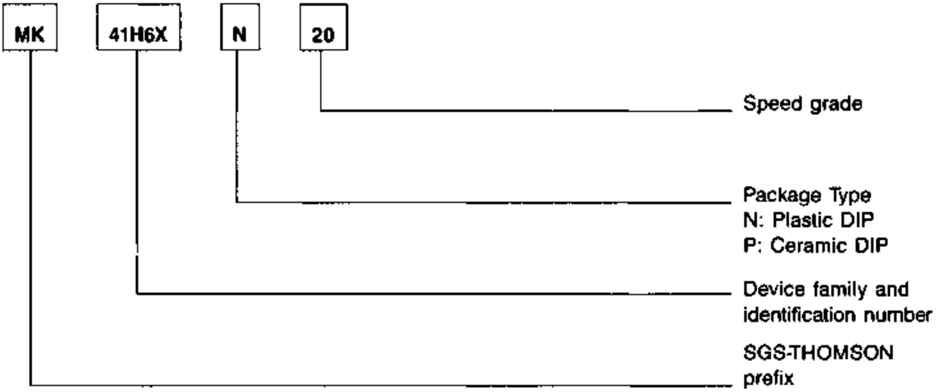


NORMALIZED SOURCE AND SINK CURRENTS VS.
AMBIENT TEMPERATURE V_{CC}=5.0V

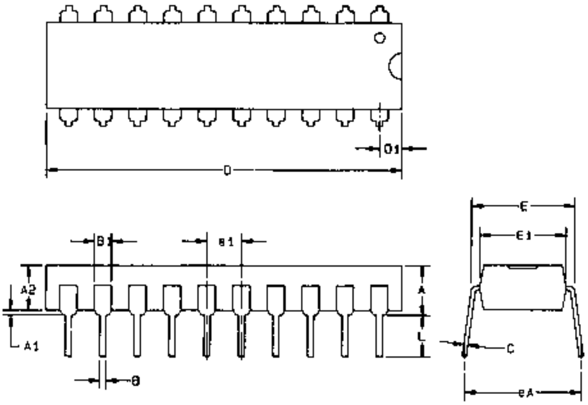


ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H68N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-20	20 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-25	25 ns	20 pin Plastic DIP	0°C to 70°C
MK41H69N-35	35 ns	20 pin Plastic DIP	0°C to 70°C
MK41H68P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H68P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H68P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-20	20 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-25	25 ns	20 pin Ceramic DIP	0°C to 70°C
MK41H69P-35	35 ns	20 pin Ceramic DIP	0°C to 70°C


MK
41H6X
N
20
Speed grade
Package Type
N: Plastic DIP
P: Ceramic DIP
Device family and identification number
SGS-THOMSON prefix

20 PIN "N" PACKAGE, PLASTIC DIP

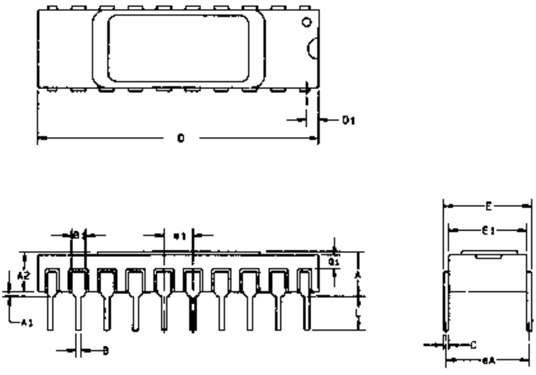


Dim.	mm		Inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	012	3
D	25.908	26.67	1.020	1.050	1
D1	1.524	1.905	.060	.075	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	400	
L	3.048	—	120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

20 PIN "P" PACKAGE, SIDE BRAZED CERAMIC DIP



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	24.511	25.273	.965	.995	
D1	0.635	1.397	.025	.055	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.048	—	.120	—	
Q1	0.127	—	.005	—	

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

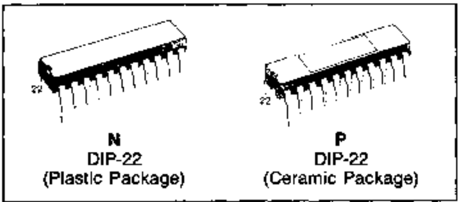
SGS-THOMSON
MICROELECTRONICS

MK41H79(N,P)-20/25/35

4K × 4 CMOS STATIC RAM

PRELIMINARY DATA

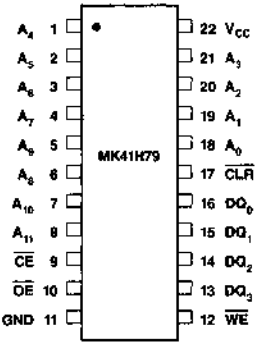
- 20, 25, AND 35 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 22-PIN, 300 MIL PLASTIC AND CERAMIC DIP
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- TTL STANDBY CURRENT UNAFFECTED BY ADDRESS ACTIVITY
- SEPARATE OUTPUT ENABLE CONTROL
- FLASH CLEAR FUNCTION



N
DIP-22
(Plastic Package)

P
DIP-22
(Ceramic Package)

FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{11} - Address
DQ_0 - DQ_3 - Data I/O
$\overline{CLR}$ - Flash Clear
$\overline{CE}$ - Chip Enable
$\overline{OE}$ - Output Enable
$\overline{WE}$ - Write Enable
GND - Ground
V_{CC} - + 5 volts

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{CLR}$	Mode	DQ	Power
H	X	X	X	Deselect	High Z	Standby
L	X	L	H	Write	D_{IN}	Active
L	L	H	H	Read	D_{OUT}	Active
L	H	H	H	Read	High Z	Active
L	X	L	L	Flash Clear	High Z	Active
L	L	H	L	Flash Clear	Low Z	Active
L	H	H	L	Flash Clear	High Z	Active

X = Don't Care

DESCRIPTION

The MK41H79 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. It requires a single +5V ± 10 percent power supply and is fully TTL compatible.

The device has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby power can be further reduced by raising the $\overline{CE}$ pin to the full V_{CC} voltage. An Output Enable ($\overline{OE}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus.
Flash $\overline{Clear}$ operation is provided on the MK41H79 via the $\overline{CLR}$ pin, and $\overline{CE}$ active (low). A low applied to the $\overline{CLR}$ pin clears all RAM bits to zero, making it especially useful for high speed cache and buffer storage applications.

OPERATIONS

READ MODE

The MK41H79 is in the Read Mode whenever $\overline{WE}$ (Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from four of 16,384 locations in the static storage array. The unique address specified by the 12 Address Inputs defines which one of 4096 nibbles of data is to be accessed.

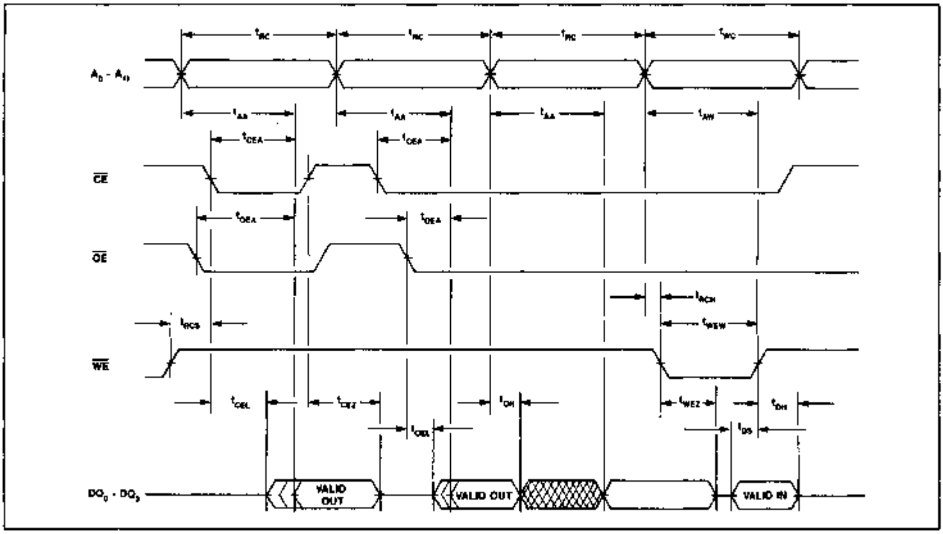
Valid data will be available at the four Data Output pins within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the four Data I/O pins is controlled by the $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ control signals. The data lines may be in an indeterminate state at t_{CEL} and t_{OEL}, but the data lines will always have valid data at t_{AA}.

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H79-20		MK41H79-25		MK41H79-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AA}	Address Access Time		20		25		35	ns	1
t_{CEL}	Chip Enable to Low-Z	7		7		7		ns	2
t_{CEA}	Chip Enable Access Time		20		25		35	ns	1
t_{OEL}	Output Enable to Low-Z	2		2		2		ns	2
t_{OEA}	Output Enable Access Time		10		12		15	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable to High-Z		8		10		13	ns	2
t_{OEZ}	Output Enable to High-Z		7		8		10	ns	2
t_{WEZ}	Write Enable to High-Z		8		10		13	ns	2

FIGURE 2. READ-READ-READ-WRITE TIMING



tRC
tRC
tRC
tWC
A0 - A13
tAA
tAA
tAA
tAW
tCEA
tCEA
CE
tOEA
tOEA
OE
tRCH
tRCS
tWEW
WE
tCEL
tCEZ
tOH
tWEZ
tDH
tOEL
tDS
DQ0 - DQ3
VALID OUT
VALID OUT
VALID IN

WRITE MODE

The MK41H79 is in the Write Mode whenever the $\overline{WE}$ and $\overline{CE}$ inputs are in the low state. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{WE}$ and $\overline{CE}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{CE}$ or WE. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

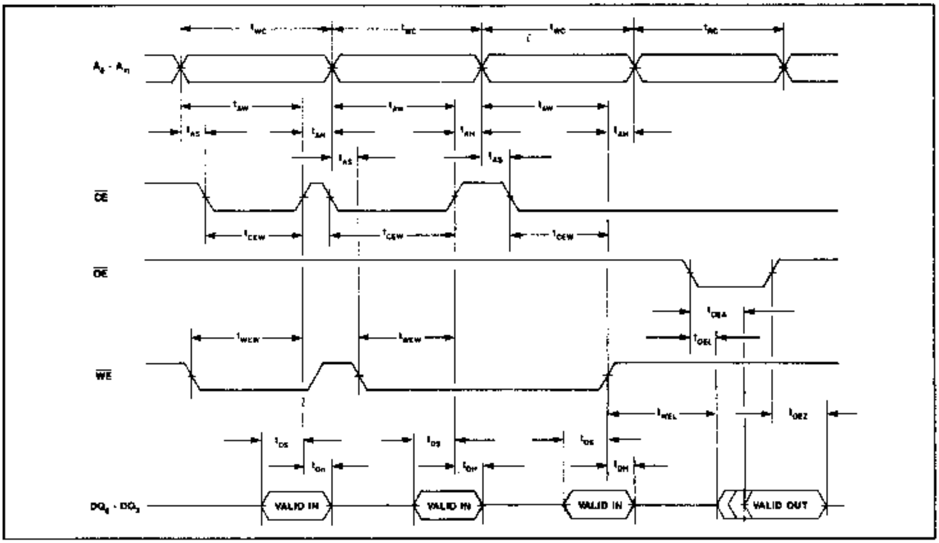
If the output is enabled ($\overline{CE}$ and $\overline{OE}$ low), then $\overline{WE}$ will return the outputs to high impedance within t_{WEZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-In must remain valid t_{DH} after the rising edge of $\overline{CE}$ or $\overline{WE}$.

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H79-20		MK41H79-25		MK41H79-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Stable to End of Write	16		20		30		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	18		22		32		ns	
t_{WEW}	Write Enable to End of Write	16		20		30		ns	
t_{DS}	Data Setup Time	12		14		15		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING


t_WC
t_WC
t_WC
t_RC
A₀ - Aₙ
t_AW
t_AW
t_AW
t_AS
t_AH
t_AH
t_AH
t_AS
t_AS
CE
t_CEW
t_CEW
t_CEW
OE
t_OEA
t_OEL
t_WEW
t_WEW
WE
t_WEL
t_OEZ
t_DS
t_DS
t_DS
t_DH
t_DH
t_DH
DQ₀ - DQ₇
VALID IN
VALID IN
VALID IN
VALID OUT

CLEAR CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

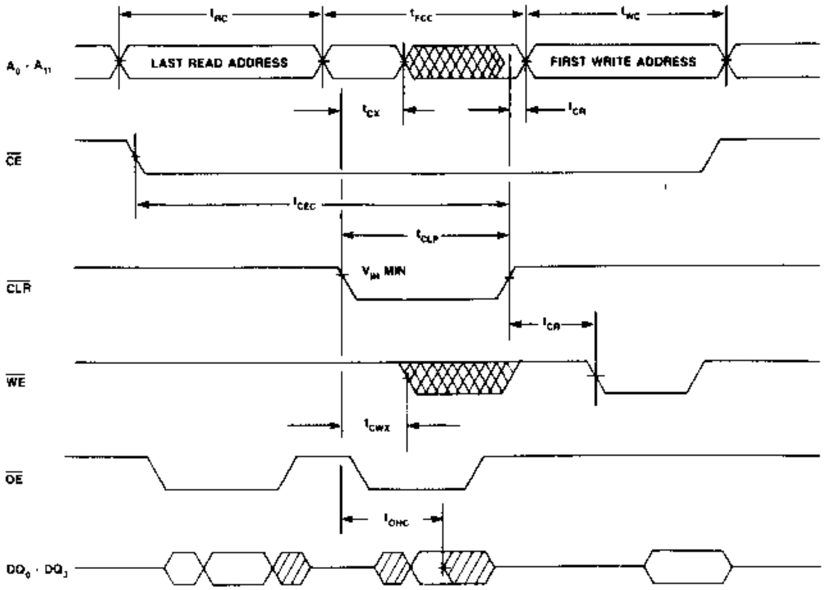
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

		MK41H79-20		MK41H79-25		MK41H79-35			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{FCC}	Flash Clear Cycle Time	40		50		70		ns	
t_{CEC}	Chip Enable Low to End of Clear	40		50		70		ns	
t_{CLP}	Flash Clear Low to End of Clear	38		48		68		ns	
t_{CX}	Clear to Inputs Don't Care	0		0		0		ns	
t_{CR}	End of Clear to Inputs Recognized	0		0		0		ns	
t_{CWX}	Clear to Write Enable Don't Care	0		0		0		ns	
t_{OHC}	Valid Data Out Hold from Clear	5		5		5		ns	1

FLASH CLEAR

A Flash Clear cycle sets all 16,384 bits in the RAM to logic zero. A Clear begins at the concurrence of a low on Chip Enable ($\overline{CE}$) and Flash Clear ($\overline{CLR}$). A Clear may be ended by a high on either $\overline{CE}$ or $\overline{CLR}$. A low on $\overline{CLR}$ has no effect if the device is disabled (CE high). A Clear may be executed within either a Read or a Write cycle. Figure 4 illustrates a Clear within a Read cycle. Clears within Write cycles are constrained only in that Write timing parameters must be observed as soon as the Flash Clear pin returns high.

FIGURE 4. LAST READ-FLASH CLEAR-FIRST WRITE



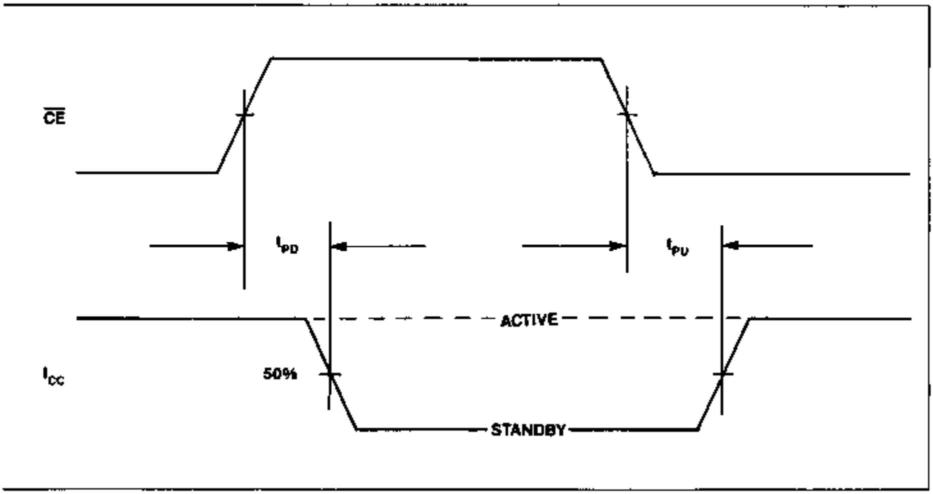
t_{RC}
t_{FCC}
t_{WC}
$A_0 - A_{11}$
LAST READ ADDRESS
FIRST WRITE ADDRESS
t_{CX}
t_{CR}
$\overline{CE}$
t_{CEC}
t_{CLP}
V_{IH} MIN
$\overline{CLR}$
t_{CR}
$\overline{WE}$
t_{CWX}
$\overline{OE}$
t_{OHC}
$DQ_0 - DQ_7$

CAUTION: APPLICATION OF TRANSIENT LEVELS BELOW V_{IH} MINIMUM ON THE CLR INPUT DURING NORMAL OPERATION MAY RESULT IN PARTIAL FLASH CLEAR.

STANDBY MODE

The MK41H79 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE



STANDBY MODE

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H79-20		MK41H79-25		MK41H79-35			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{PD}	Chip Enable High to Power Down		20		25		35	ns	
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	

APPLICATION

The MK41H79 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because he outputs can drive rail-to-rail into high impedance oads, the 41H79 can also interface to 5 volt CMOS on all inputs and outputs. Refer to the normalized performance curves that follow.

Since very high frequency current transients will be associated with the operation of the MK41H79, power line inductance must be minimized on the circuit board power distribution network. Power and ground tracegridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 µF or larger. A pull-up resistor is also recommended for CLR on the MK41H79. This will ensure that any low going system noise, coupled onto the input, does not drive CLR below V_{IH} minimum specifications.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND	−1.0 V to +7.0 V
Ambient Operating Temperature (T_A)	0°C to +70°C
Ambient Storage Temperature (Plastic)	−55°C to +125°C
Ambient Storage Temperature (Ceramic)	−65°C to +150°C
Total Device Power Dissipation	1 Watt
Output Current per Pin	50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		120	mA	4
I_{CC2}	TTL Standby Current		16	mA	5
I_{CC3}	CMOS Standby Current		8	mA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	9

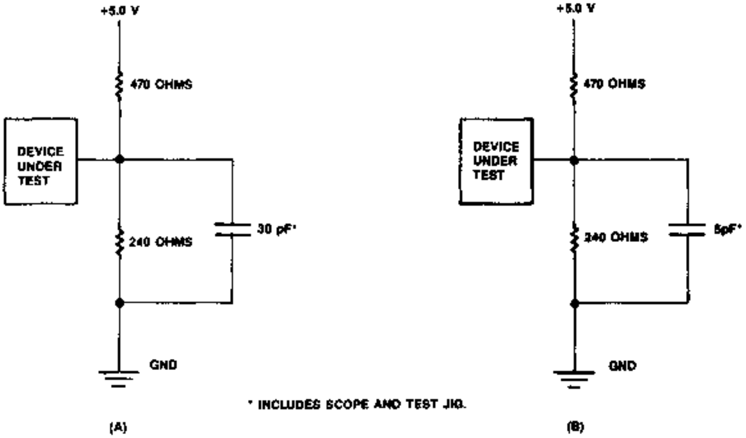
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuit. $t_{RC} = t_{RC}$ (min) is used.
5. $\overline{CE} = V_{IH}$, all other inputs = Don't Care.
6. V_{CC} (max) $\geq \overline{CE} \geq V_{CC} - 0.3$ V, all other inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that $0 V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
8. Output leakage current specifications are valid for all V_{OUT} such that $0 V < V_{OUT} < V_{CC}$, $\overline{CE} = V_{IH}$ and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

nput Levels .... GND to 3.0 V
Transition Times .... 5 ns
nput and Output Signal Timing Reference Level .... 1.5 V
Ambient Temperature .... 0°C to 70°C
V_{CC} .... 5.0 V ± 10 percent

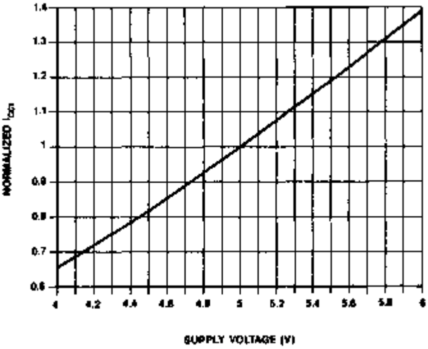
FIGURE 6. OUTPUT LOAD CIRCUITS


+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
30 pF*
GND
(A)
+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
5pF*
GND
(B)

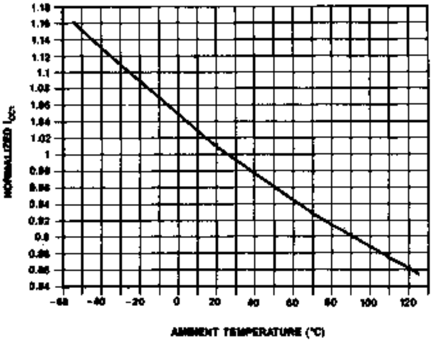
* INCLUDES SCOPE AND TEST JIG.

NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

NORMALIZED SUPPLY CURRENT VS. SUPPLY VOLTAGE $T_A = 0°C$

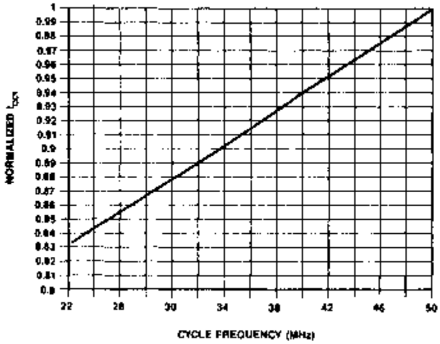


NORMALIZED SUPPLY CURRENT VS. AMBIENT TEMPERATURE $V_{CC} = 5.0V$

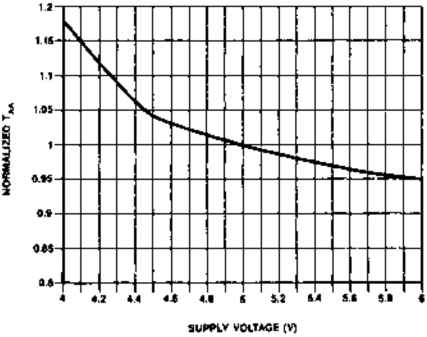


NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS

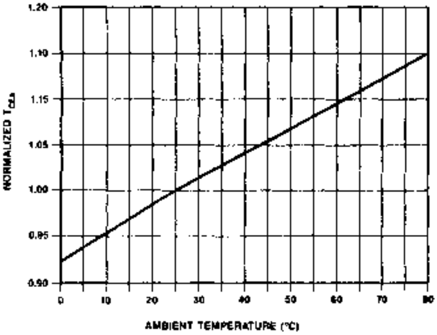
NORMALIZED SUPPLY CURRENT VS. CYCLE TIME V_{CC}=5.0V T_A=25°C



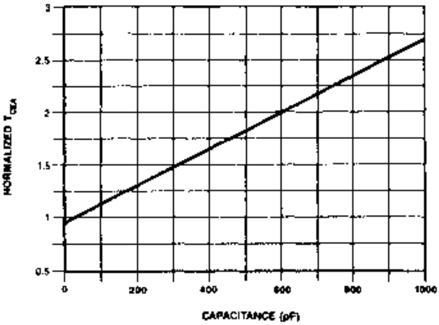
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE T_A=25°C



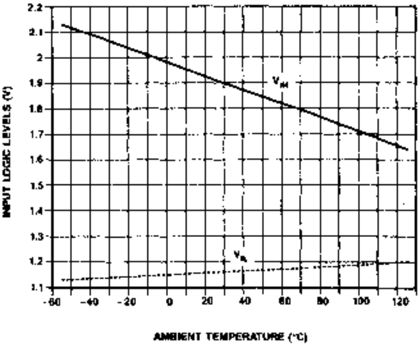
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE V_{CC}=5.0V



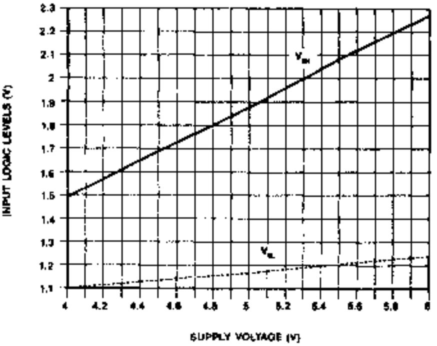
NORMALIZED ACCESS TIME VS. OUTPUT LOADING V_{CC}=5.0V T_A=25°C



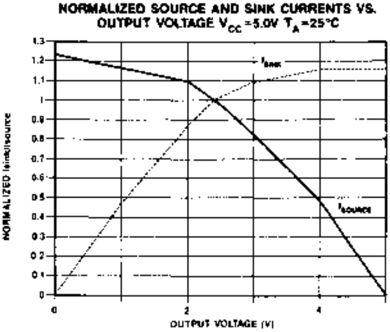
LOGIC THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE V_{CC}=5.0V



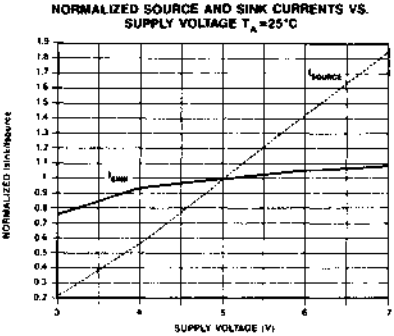
LOGIC THRESHOLD VOLTAGE VS. SUPPLY VOLTAGE T_A=25°C



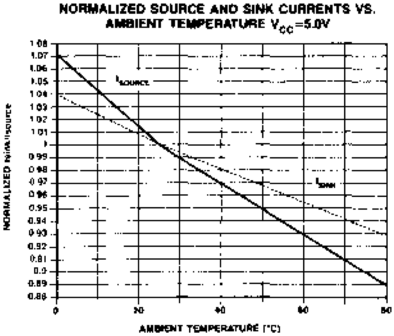
NORMALIZED DC AND AC PERFORMANCE CHARACTERISTICS



NORMALIZED SOURCE AND SINK CURRENTS VS. OUTPUT VOLTAGE V_{CC}=5.0V T_A=25°C

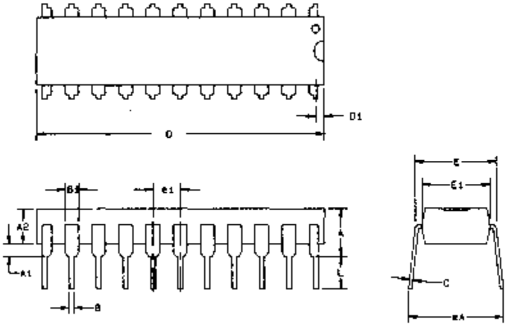


NORMALIZED SOURCE AND SINK CURRENTS VS. SUPPLY VOLTAGE T_A=25°C



NORMALIZED SOURCE AND SINK CURRENTS VS. AMBIENT TEMPERATURE V_{CC}=5.0V

22 PIN "N"PACKAGE PLASTIC DIP

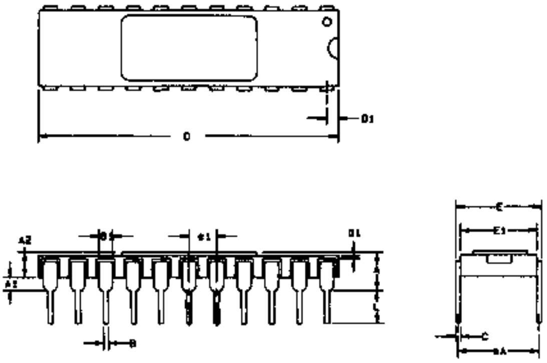


NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.143	1.778	.045	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.254	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	9.271	.300	.365	
L	3.175	—	.125	—	

22 PIN "P"PACKAGE SIDE BRAZED CERAMIC DIP


D
D1
A2
A1
B1
e1
Q1
A
L
B
E
E1
C
eA

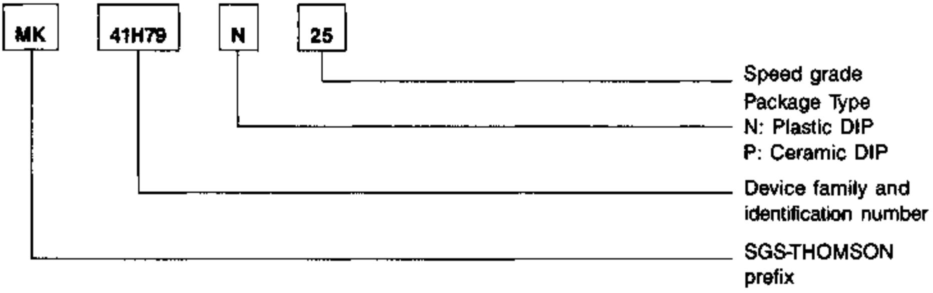
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	4.445	—	.175	1
A1	0.508	—	.020	—	1
A2	2.032	2.794	.080	.110	
B	0.381	0.533	.015	.021	2
B1	0.965	1.447	.038	.057	
C	0.203	0.304	.008	.012	2
D	27.559	28.321	1.085	1.115	
D1	0.889	1.651	.035	.065	
E	7.493	8.255	.295	.325	
E1	7.112	7.874	.280	.310	
e1	2.286	2.794	.090	.110	
eA	7.366	9.271	.290	.365	
L	3.175	—	.125	—	
Q1	0.127	—	.005	—	3

NOTES

1. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.
3. MEASURED FROM TOP OF CERAMIC TO NEAREST METALLIZATION.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H79N-20	20 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-25	25 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79N-35	35 ns	22 pin Plastic DIP	0°C to 70°C
MK41H79P-20	20 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-25	25 ns	22 pin Ceramic DIP	0°C to 70°C
MK41H79P-35	35 ns	22 pin Ceramic DIP	0°C to 70°C


MK
41H79
N
25
Speed grade
Package Type
N: Plastic DIP
P: Ceramic DIP
Device family and identification number
SGS-THOMSON prefix

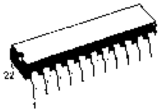
SGS-THOMSON
MICROELECTRONICS

MK41H87(N)-25/35/45

64K × 1 CMOS STATIC RAM

ADVANCE INFORMATION

- 25, 35, AND 45 NS ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- 22-PIN, 300 MIL PLASTIC DIP
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC DISCHARGE
- JEDEC STANDARD PINOUT



N
DIP-22
(Plastic Package)

IK41H87 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	Mode	Q	Power
H	X	Deselect	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

ESCRIPTION

The MK41H87 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The MK41H87 requires only a single +5V ± 10 percent power supply, and it is fully TTL compatible.

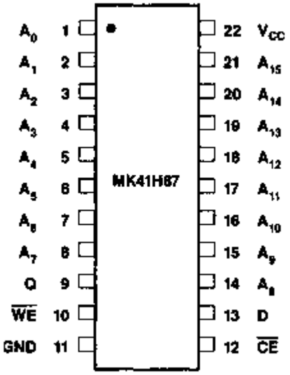
The MK41H87 has a Chip Enable power down feature which automatically reduces power dissipation when the $\overline{CE}$ pin is brought inactive (high). Standby Power can be further reduced by holding the Address and $\overline{CE}$ pins at full supply rail voltages.

PERATIONS

EAD MODE

The MK41H87 is in the Read Mode whenever $\overline{WE}$ Write Enable) is high and $\overline{CE}$ (Chip Enable) is low, providing a ripple-through access to data from one of 65,536 locations in the static storage array. Valid data will be available at the Data Output pin (Q) within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ access time is satisfied. f $\overline{CE}$ access time is not met, data access will be measured from the limiting parameter (t_{CA}) rather than the address. The state of the Data Output pin is controlled by the $\overline{CE}$ and $\overline{WE}$ control signals. The Q may be in an indeterminate state at t_{CL}, but the Q will always have valid data at t_{AA}.

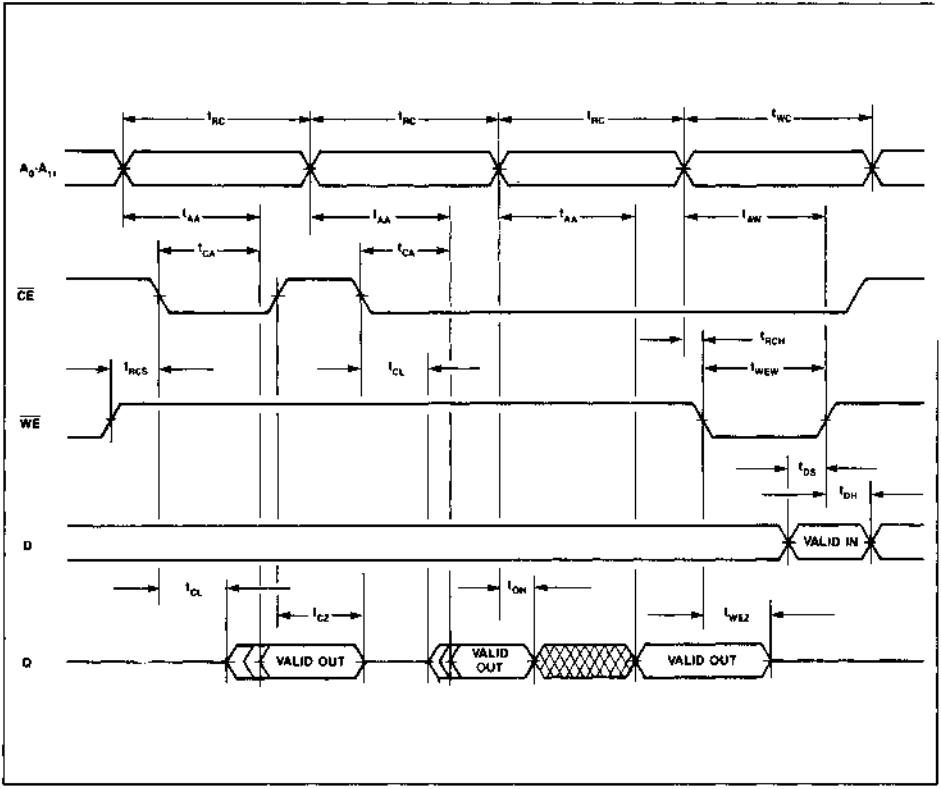
FIGURE 1. PIN CONNECTIONS



PIN NAMES

A_0 - A_{15} - Address
$\overline{CE}$ - Chip Enable
$\overline{WE}$ - Write Enable
GND - Ground
V_{CC} - + 5 volts
D - Data In
Q - Data Out

FIGURE 2. READ-READ-READ-WRITE TIMING


t_RC
t_RC
t_RC
t_WC
A0-A11
t_AA
t_AA
t_AA
t_AW
t_CA
t_CA
CE
t_RCH
t_RCS
t_CL
t_WEW
WE
t_DS
t_DH
D
VALID IN
t_CL
t_OH
t_CZ
t_WEZ
Q
VALID OUT
VALID OUT
VALID OUT

READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

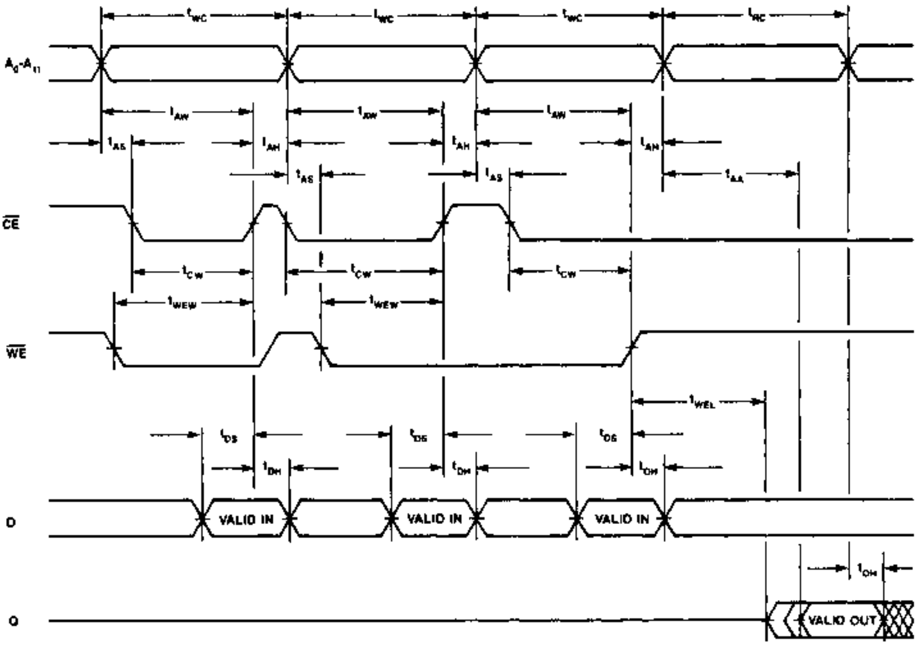
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

		MK41H87-25		MK41H87-35		MK41H87-45			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	25		35		45		ns	
t_{AA}	Address Access Time		25		35		45	ns	1
t_{CL}	Chip Enable to Low-Z	5		5		5		ns	2
t_{CA}	Chip Enable Access Time		25		35		45	ns	1
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{OH}	Valid Data Out Hold Time	3		3		3		ns	1
t_{CZ}	Chip Enable to High-Z		10		12		15	ns	2
t_{WEZ}	Write Enable to High-Z		12		14		17	ns	2

WRITE MODE

The MK41H87 is in the Write Mode whenever the $\overline{\text{WE}}$ and $\overline{\text{CE}}$ inputs are in the low state. $\overline{\text{CE}}$ or $\overline{\text{WE}}$ must be high during address transitions. Addresses must be held valid throughout a write cycle. The Write begins with the concurrence of a low on $\overline{\text{WE}}$ and $\overline{\text{CE}}$. Therefore, t_{AS} is referenced to the latter occurring edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$. If the output is enabled ($\overline{\text{CE}}$ is low), then $\overline{\text{WE}}$ will return the output to high impedance within t_{WEZ} of its falling edge. Data-In must remain valid t_{DH} after the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$.

FIGURE 3. WRITE-WRITE-WRITE-READ TIMING

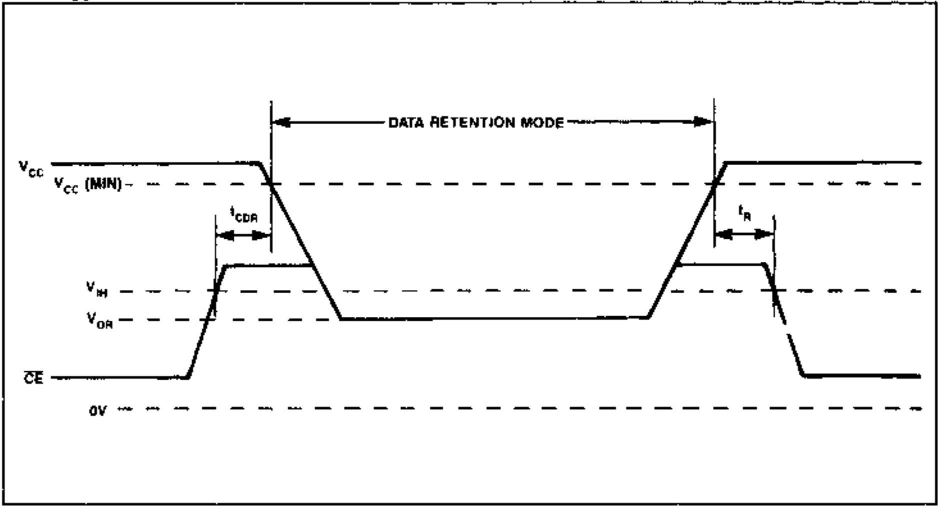

t_{WC}
t_{WC}
t_{WC}
t_{RC}
A_0-A_{11}
t_{AW}
t_{AW}
t_{AW}
t_{AS}
t_{AH}
t_{AH}
t_{AH}
t_{AS}
t_{AS}
t_{AA}
$\overline{\text{CE}}$
t_{CW}
t_{CW}
t_{CW}
t_{WEW}
t_{WEW}
$\overline{\text{WE}}$
t_{WEL}
t_{DS}
t_{DS}
t_{DS}
t_{DH}
t_{DH}
t_{DH}
D
VALID IN
VALID IN
VALID IN
t_{OH}
Q
VALID OUT

WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H87-25		MK41H87-35		MK41H87-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	25		35		45		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AW}	Address Valid to End of Write	20		30		40		ns	
t_{AH}	Address Hold after End of Write	0		0		0		ns	
t_{CW}	Chip Enable to End of Write	20		30		40		ns	
t_{WEW}	Write Enable to End of Write	20		25		30		ns	
t_{DS}	Data Setup Time	20		25		35		ns	
t_{DH}	Data Hold Time	0		0		0		ns	
t_{WEL}	Write Enable to Low-Z	5		5		5		ns	2

FIGURE 4. DATA RETENTION TIMING
LOW V_{CC} DATA RETENTION TIMING



LOW V_{CC} DATA RETENTION CHARACTERISTICS

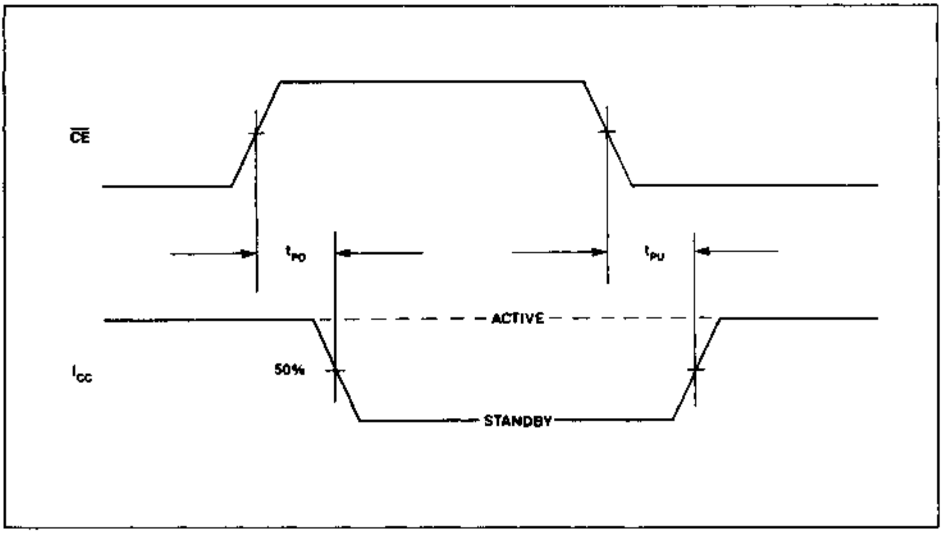
($0°C \leq T_A \leq 70°C$)

SYM	PARAMETERS	MIN	MAX	UNIT	NOTES
V_{DR}	V_{CC} for Data Retention	2.0	V_{CC} (min)	V	6
I_{CCDR}	Data Retention Power Supply Current	—	500	µA	6
t_{CDR}	Chip Deselection to Data Retention Time	0	—	ns	
t_R	Operation Recovery Time	t_{RC}	—	ns	

STANDBY MODE

The MK41H87 is in Standby Mode whenever $\overline{CE}$ is held at or above V_{IH}.

FIGURE 5. STANDBY MODE TIMING



STANDBY MODE
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MK41H87-25 MIN	MK41H87-25 MAX	MK41H87-35 MIN	MK41H87-35 MAX	MK41H87-45 MIN	MK41H87-45 MAX	UNITS	NOTES
t_{PD}	Chip Enable High to Power Down		25		35		45	ns	10
t_{PU}	Chip Enable Low to Power Up	0		0		0		ns	10

APPLICATION

The MK41H87 operates from a 5.0 volt supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaced with it, particularly TTL devices. Additionally, because the outputs can drive rail-to-rail into high impedance loads, the 41H87 can also interface to 5 volt CMOS on all inputs and outputs.

Since very high frequency current transients will be associated with the operation of the MK41H87, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or separate power planes can be employed to reduce line inductance. Additionally, a high frequency decoupling capacitor should be placed next to each RAM. The capacitor should be 0.1 µF or larger.

Though often times not thought of as such, the traces on a memory board are basically unterminated, low impedance transmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentation most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) . . . . 0°C to +70°C
Ambient Storage Temperature (Plastic) . . . . −55°C to +125°C
Ambient Storage Temperature (Ceramic) . . . . −65°C to +150°C
Total Device Power Dissipation . . . . 1 Watt
Output Current per Pin . . . . 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC}+1.0	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current		70	mA	4
I_{CC2}	TTL Standby Current		8	mA	5
I_{CC3}	CMOS Standby Current		1.5	mA	6
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	µA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	µA	8
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	9
C_2	Capacitance on DQ pins	8	10	pF	5,9

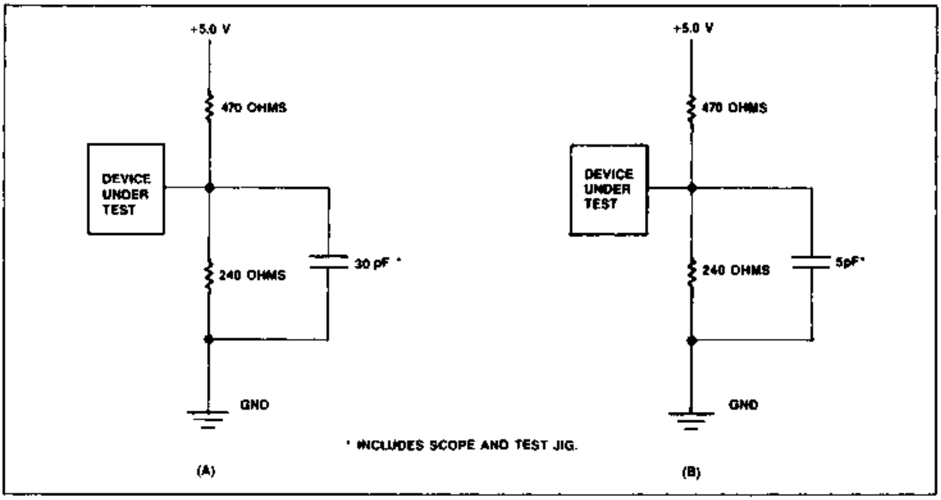
NOTES

1. Measured with load shown in Figure 6(A).
2. Measured with load shown in Figure 6(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. tcycle = min. duty cycle 100%.
5. $\overline{CE}$ = V_{IH}, All Other Inputs = Don't Care.
6. V_{CC} (max) ≥ $\overline{CE}$ ≥ V_{CC} − 0.3 V
   GND + 0.3 V ≥ A_0-A_{15} ≥ V_{IL} (min) or V_{IH} (max) ≥ A_0-A_{15} ≥ V_{CC} −0.3 V.
   All Other Inputs = Don't Care.
7. Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
8. Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}, $\overline{CE}/\overline{CS}$ = V_{IH} and V_{CC} in valid operating range.
9. Capacitances are sampled and not 100% tested.
10. Guaranteed, but not 100% tested.

AC TEST CONDITIONS

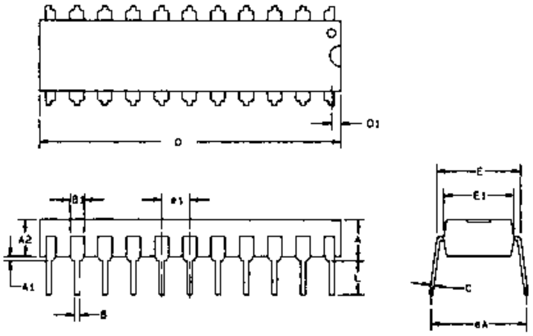
Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 6. OUTPUT LOAD CIRCUITS


+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
30 pF *
GND
(A)
+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
5pF*
GND
(B)

* INCLUDES SCOPE AND TEST JIG.

22 PIN "N" PACKAGE


D1
D
B1
e1
A2
A1
B
A
L
E
E1
C
eA

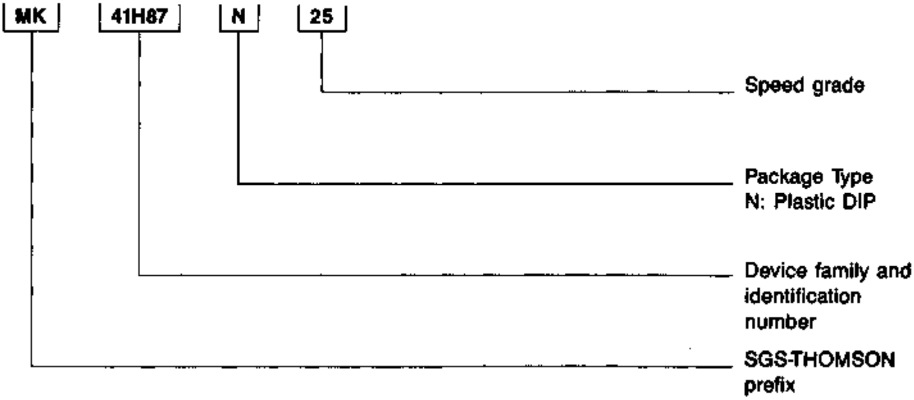
Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.048	3.556	.120	.140	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	25.908	26.67	1.020	1.050	1
D1	0.381	0.635	.010	.025	
E	7.62	8.255	.300	.325	
E1	6.096	6.858	.240	.270	
e1	2.286	2.794	.090	.110	
eA	7.62	10.16	.300	.400	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK41H87N-25	25 ns	22 pin 300 mil Plastic DIP	0°C to 70°C
MK41H87N-35	35 ns	22 pin 300 mil Plastic DIP	0°C to 70°C
MK41H87N-45	45 ns	22 pin 300 mil Plastic DIP	0°C to 70°C


MK
41H87
N
25
Speed grade
Package Type
N: Plastic DIP
Device family and
identification
number
SGS-THOMSON
prefix

SGS-THOMSON
MICROELECTRONICS

MK48H64/MK48H65(N,P) -35/45/55/70

64K (8K × 8-BIT) CMOS FAST STATIC RAM

ADVANCED DATA

- 35, 45, 55, AND 70 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- LOW V_{CC} DATA RETENTION 2 VOLTS
- ALL INPUTS AND OUTPUTS ARE CMOS AND TTL COMPATIBLE
- LOW POWER OPERATION, 10μA CMOS STANDBY CURRENT UTILIZING FULL CMOS 6-T CELL
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC OR 600 MIL CERAMIC DIP. MK48H65 AVAILABLE IN 300 MIL PLASTIC DIP.

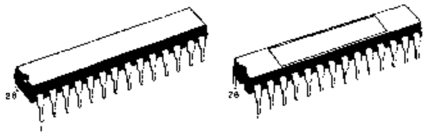
MK48H64/MK48H65 TRUTH TABLE

$\overline{W}$	$\overline{E1}$	E2	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	High-Z	Standby
X	X	L	X	Deselect	High-Z	Standby
H	L	H	H	Read	High-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

DESCRIPTION

The MK48H64 and MK48H65 are 65,536-bit fast static RAMs organized as 8K × 8 bits. They are fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The devices feature fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. They require a single +5V ± 10 % supply, and are fully TTL compatible.

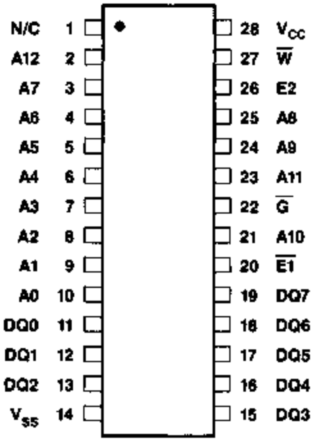
The MK48H64 and MK48H65 have a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive ($\overline{E1}$ goes high or E2 goes low). An Output



N
DIP-28
(Plastic Package)

P
DIP-28
(Ceramic Package)

FIGURE 1. PIN CONNECTIONS



PIN NAMES

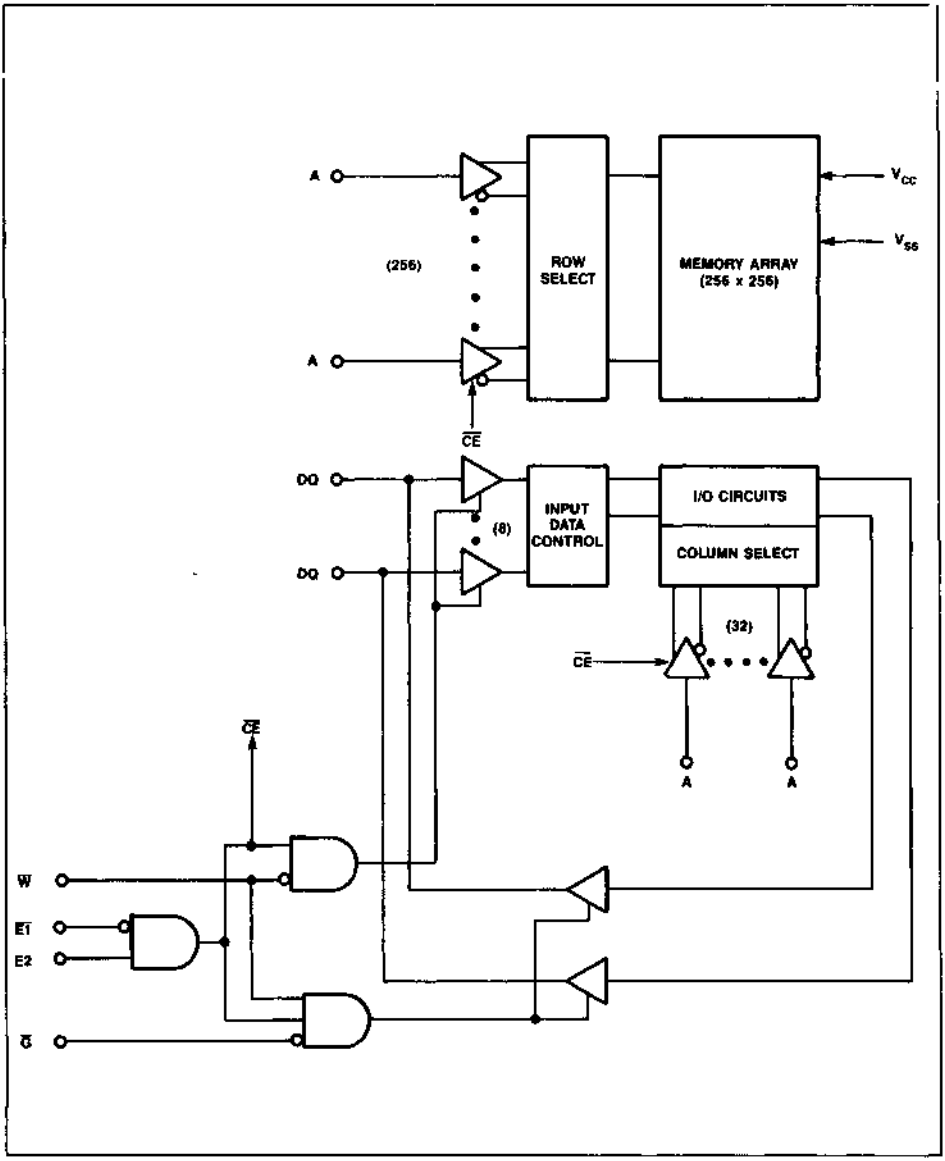
A0-A12	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{E1}$, E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
N/C	No Connection

This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, $\overline{E1}$, and E2, as summarized in the truth table.

The MK48H65 is a space saving 300 mil plastic DIP. The MK48H64 offers the standard 600 mil Plastic or Ceramic DIP.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM


A
A
(256)
$\overline{CE}$
ROW SELECT
MEMORY ARRAY (256 x 256)
V_{CC}
V_{SS}
DQ
DQ
(8)
INPUT DATA CONTROL
I/O CIRCUITS
COLUMN SELECT
(32)
$\overline{CE}$
A
A
$\overline{CE}$
$\overline{W}$
$\overline{E1}$
E2
$\overline{G}$

READ CYCLE TIMING

SYMBOLS			48H6X-35		48H6X-45		48H6X-55		48H6X-70			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	35		45		55		70		ns	
t_{AA}	t_{AVQV}	Address Access Time		35		45		55		70	ns	1
t_{CEA} 1&2	t_{E1LQV} t_{E2HQV}	Chip Enable 1 & 2 Access Time		35 35		45 45		55 55		70 70	ns ns	1
t_{OEA}	t_{GLQV}	Output Enable Access Time		20		25		30		35	ns	1
t_{CEL} 1&2	t_{E1LQX} t_{E2HQX}	Chip Enable 1 & 2 to Output Low-Z	5 5		5 5		5 5		5 5		ns ns	2
t_{OEL}	t_{GLQX}	Output Enable to Low-Z	0		0		0		0		ns	2
t_{CEZ} 1&2	t_{E1HQZ} t_{E2LQZ}	Chip Enable 1 & 2 to High-Z		15 15		20 20		25 25		30 30	ns ns	2
t_{OEZ}	t_{GHQZ}	Output Enable to High-Z		15		20		25		30	ns	2
t_{OH}	t_{AXQX}	Output Hold From Address Change	5		5		5		5		ns	1

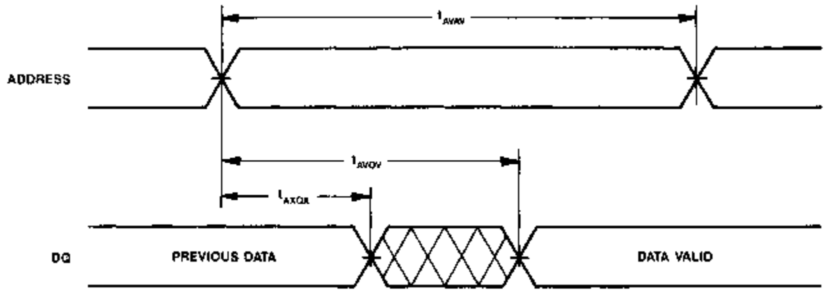
OPERATIONS

READ MODE

The MK48H64 and MK48H65 are in the read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and both Chip Enables ($\overline{E1}$ and E2) are active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

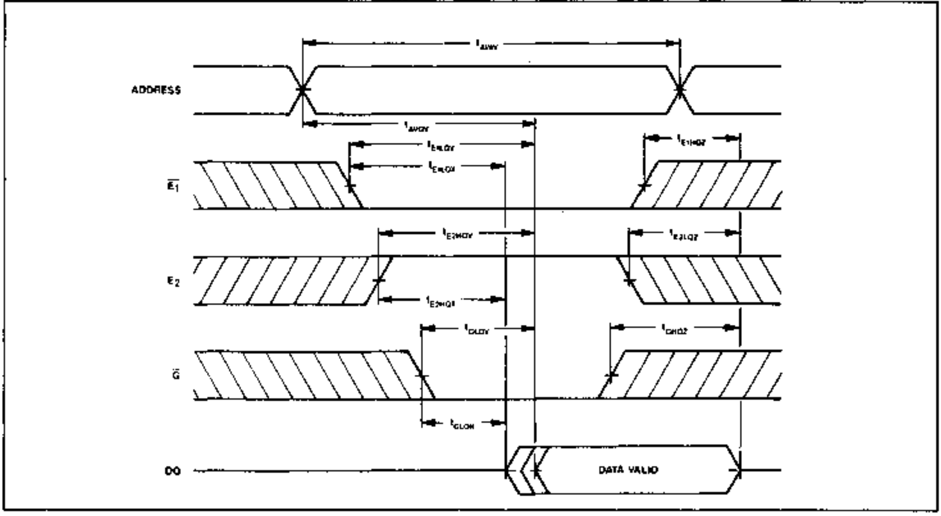
Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, $\overline{E1}$ is low, and E2 is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$ control signals. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

FIGURE 3. READ TIMING NO. 1 (ADDRESS ACCESS)



NOTE: Chip Enable and Output Enable are presumed valid.

FIGURE 4. READ TIMING NO. 2 ($\overline{W} = V_{IH}$)


t_{AVAV}
ADDRESS
t_{AVQV}
t_{E1LQV}
t_{E1LQX}
t_{E1HQZ}
$\overline{E_1}$
t_{E2HQV}
t_{E2LQZ}
E_2
t_{E2HQX}
t_{GLQV}
t_{GHQZ}
$\overline{G}$
t_{GLQX}
DQ
DATA VALID

WRITE CYCLE TIMING

SYMBOLS			48H6X-35		48H6X-45		48H6X-55		48H6X-70			
ALT.	STD.	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	35		45		55		70		ns	
t_{AS}	t_{AVWL}	Address Set-up Time to Write Enable Low	0		0		0		0		ns	
t_{AS}	t_{AVE1L} t_{AVE2H}	Address Set-up Time to Chip Enable	0		0		0		0		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	25		35		45		60		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	25		35		45		60		ns	
t_{AH}	t_{WHAX}	Address Hold Time after End of Write	0		0		0		0		ns	
t_{CEW}	t_{E1LE1H} t_{E2HE2L}	Chip Enable to End of Write	25		35		45		60		ns	
t_{WR}	t_{E1HAX} t_{E2LAX}	Write Recovery Time to Chip Disable	0		0		0		0		ns	
t_{DW}	t_{DVWH}	Data Valid to End of Write	25		30		30		40		ns	
t_{DH}	t_{WHDX}	Data Hold Time	0		0		0		0		ns	
t_{WEL}	t_{WHQX}	Write High to Output Low-Z (Active)	0		0		0		0		ns	2
t_{WEZ}	t_{WLQZ}	Write Enable to Output High-Z		15		20		25		30	ns	2

WRITE MODE

The MK48H64 and MK48H65 are in the Write mode whenever the $\overline{W}$ and $\overline{E1}$ pins are low, with E2 high. Either Chip Enable pin or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL}, t_{AVE1L}, and t_{AVE2H} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

If the Output is enabled ($\overline{E1}$ = low, E2 = high, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E1}$ or the falling edge of E2, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{E1}$ or $\overline{W}$, or the falling edge of E2.

FIGURE 5. WRITE TIMING NO. 1 ($\overline{W}$ CONTROL)

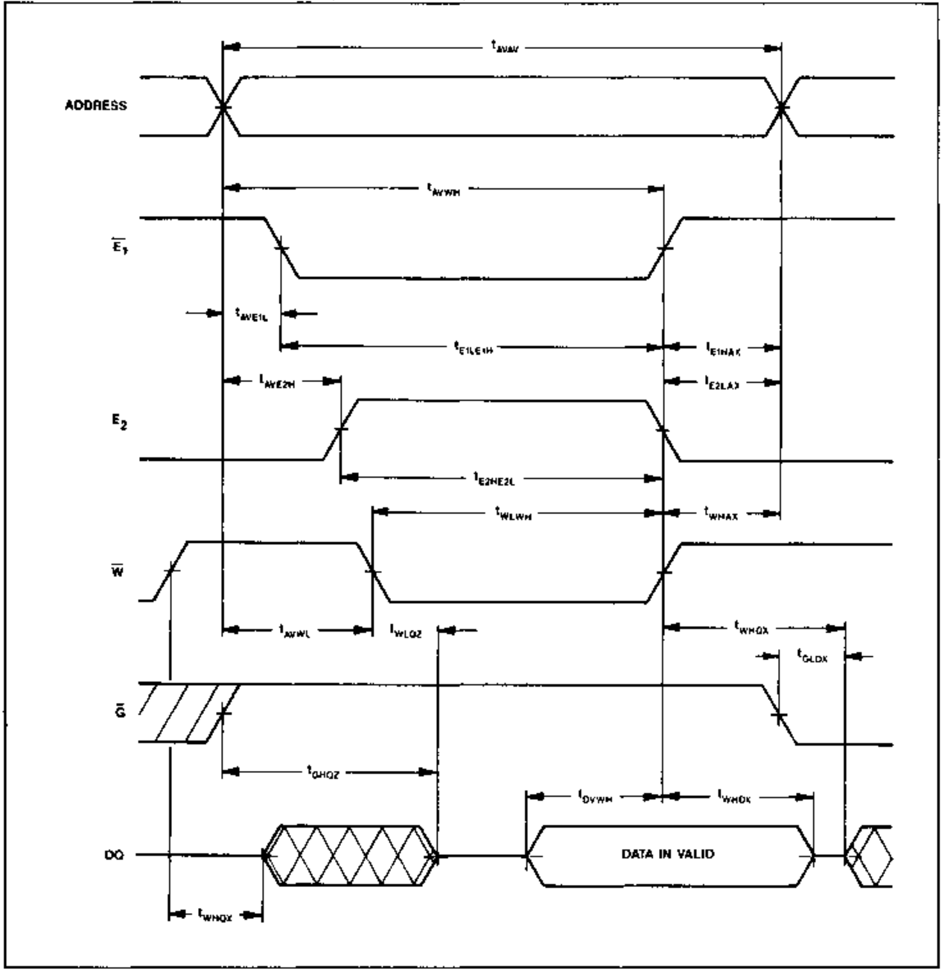
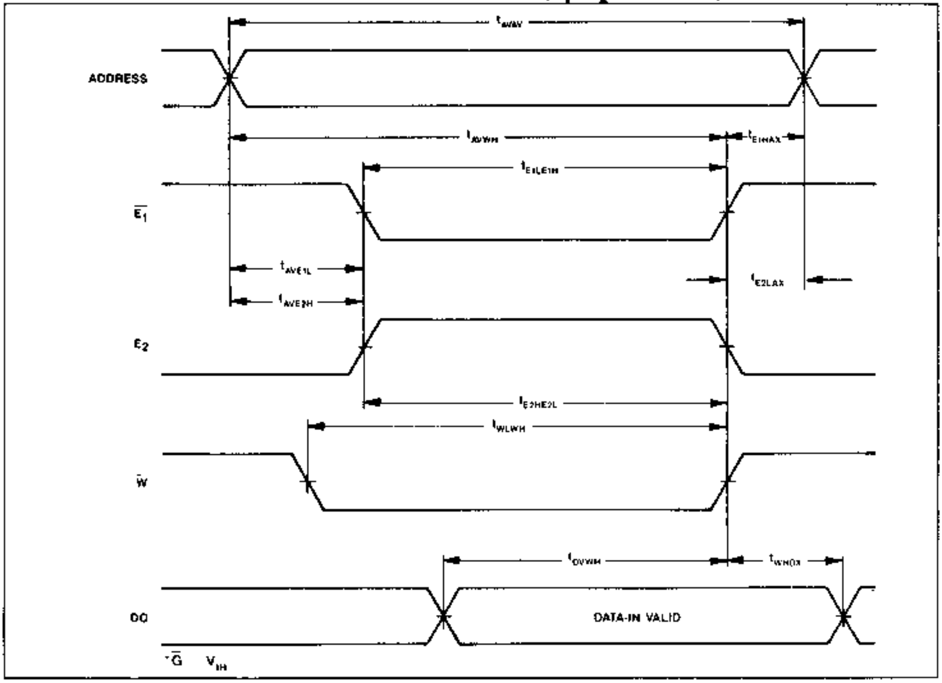

tAVAV
ADDRESS
tAVWH
E1
tAVE1L
tE1LE1H
tE1HAX
tAVE2H
tE2LAX
E2
tE2HE2L
tWLWH
tWHAX
W
tAVWL
tWLQZ
tWHQX
tGLQX
G
tGHQZ
tDVWH
tWHDX
DQ
DATA IN VALID
tWHQX

FIGURE 6. WRITE TIMING NO. 2 ($\overline{E_1}$, E_2 CONTROL)

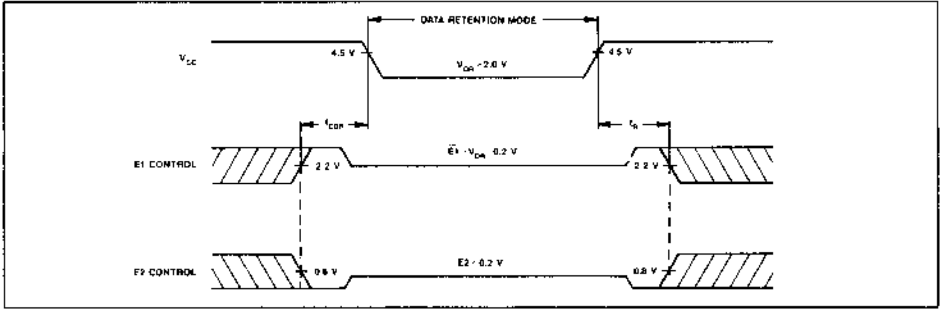

t_{AVAV}
ADDRESS
t_{AVWH}
t_{E1HAX}
t_{E1LE1H}
$\overline{E_1}$
t_{AVE1L}
t_{E2LAX}
t_{AVE2H}
E_2
t_{E2HE2L}
t_{WLWH}
$\overline{W}$
t_{DVWH}
t_{WHDX}
DQ
DATA-IN VALID
$\overline{G}$ V_{IH}

LOW V_{CC} DATA RETENTION CHARACTERISTICS

SYMBOLS	PARAMETERS	MIN	MAX	UNIT	NOTES
VDR	V_{CC} Data Retention	2.0	V_{CC}(min)	V	
I_{CC}DR	Data Retention Power Supply Current	—	10	μA	
t_{CDR}	Chip Deselection to Data Retention Time	0		nS	
t_R	Operation Recovery Time	t_{AVAV}*		nS	

* t_{AVAV} = READ CYCLE TIME

FIGURE 7. LOW V_{CC} DATA RETENTION TIMING


DATA RETENTION MODE
V_{CC}
4.5 V
$V_{DR} \geq 2.0$ V
4.5 V
t_{CDR}
t_R
E1 CONTROL
2.2 V
$\overline{E1} \geq V_{DR}$ -0.2 V
2.2 V
E2 CONTROL
0.8 V
E2 ≤ 0.2 V
0.8 V

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to GND . . . . −1.0 V to +7.0 V
Ambient Operating Temperature (T_A) . . . . 0°C to +70°C
Ambient Storage Temperature (Plastic) . . . . −55°C to +125°C
Ambient Storage Temperature (Ceramic) . . . . −65°C to +150°C
Total Device Power Dissipation . . . . 1 Watt
Output Current per Pin . . . . 50 mA

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	3
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		$V_{CC}+0.3$	V	3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	3

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current f = min cycle		90	mA	4
I_{CC2}	Average Power Supply Current f = 0		20	mA	5
I_{SB1}	TTL Standby Current		10	mA	6
I_{SB2}	CMOS Standby Current		10	μA	7
I_{IL}	Input Leakage Current (Any Input Pin)	−1	+1	μA	8
I_{OL}	Output Leakage Current (Any Output Pin)	−10	+10	μA	9
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −4 mA)	2.4		V	3
V_{OL}	Output Logic 0 Voltage (I_{OUT} = +8 mA)		0.4	V	3

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_1	Capacitance on input pins	4	5	pF	10
C_2	Capacitance on DQ pins	8	10	pF	10

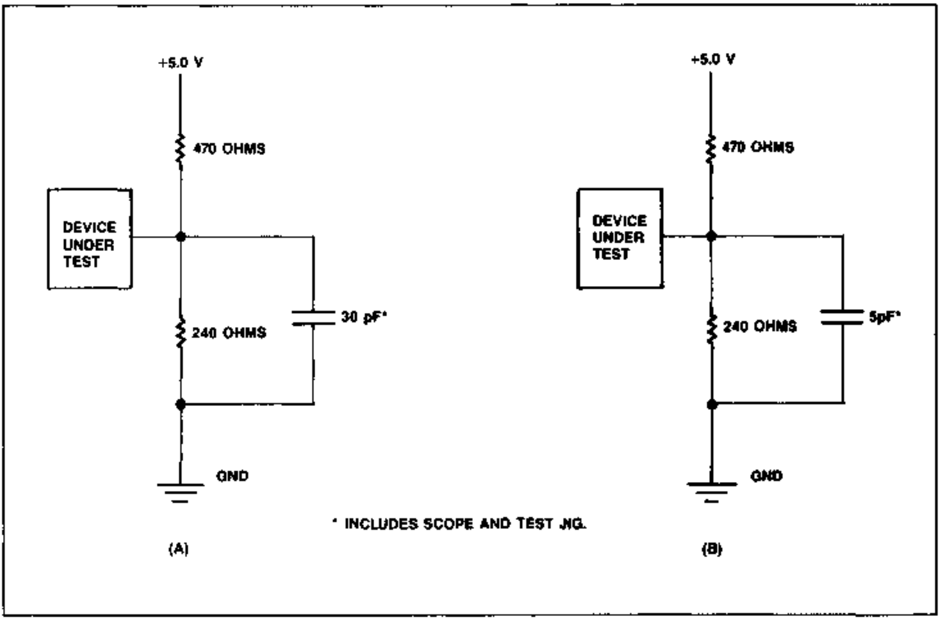
NOTES

1. Measured with load shown in Figure 8(A).
2. Measured with load shown in Figure 8(B).
3. All voltages referenced to GND.
4. I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. t_{AVAV} = t_{AVAV} (min) duty cycle 100%.
5. I_{CC2} is measured with outputs open circuit.
6. $\overline{E1}$ = V_{IH}, all other Inputs = Don't Care.
7. V_{CC} (max), and $E2 \leq V_{SS}$ + 0.3 V, all other Inputs = Don't Care.
8. Input leakage current specifications are valid for all V_{IN} such that $0 V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
9. Output leakage current specifications are valid for all V_{OUT} such that $0 V < V_{OUT} < V_{CC}$. $\overline{E1}$ = V_{IH} or E2 = V_{IL}, and V_{CC} in valid operating range.
10. Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input and Output Signal Timing Reference Level	1.5 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 8. OUTPUT LOAD CIRCUITS


+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
30 pF*
GND
(A)
+5.0 V
470 OHMS
DEVICE UNDER TEST
240 OHMS
5pF*
GND
(B)

* INCLUDES SCOPE AND TEST JIG.

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