256 Kilobit (32K x 8) SuperFlash MTP

SST27SF256, SST27VF256

Preliminary Specifications

FEATURES:

- **5.0-Volt Read Operation for 27SF256**
- **2.7-Volt Read Operation for 27VF256**
- **Superior Reliability**
  - Endurance: Minimum 1000 Cycles
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 20 mA (typical) for 5V and 10mA (typical) for 2.7V
  - Standby Current: 10 µA (typical) for both 27SF256 and 27VF256
- **Fast Access Time:**
  - 5.0-Volt Read - 55 and 70
  - 2.7-Volt Read - 120 and 150 ns
- **Fast Programming Operation**
  - 20 µs per byte (guaranteed)
  - 0.8 second for the entire chip
- **Features Electrical Erase:**
  - Does Not Require UV Source
  - Chip Erase Time: 100 ms
- **TTL I/O Compatibility**
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **12V Power Supply for Programming/Erase**
- **Packages Available**
  - 32-Pin PLCC
  - 28 Pin Plastic DIP
  - 28 Pin TSOP

PRODUCT DESCRIPTION

The 27SF256/27VF256 are 32K x 8 CMOS, many-time programmable (MTP) low cost flash, manufactured with SST's proprietary, high performance SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The 27SF256/27VF256 can be electrically erased and programmed at least 1000 times using an external programmer, e.g., to change the contents of devices in inventory. The 27SF256/27VF256 have to be erased prior to programming. The 27SF256/27VF256 conform to JEDEC standard pinouts for byte-wide memories.

Featuring high performance byte programming, the 27SF256/27VF256 provide a byte-program time of 20 µs. The entire memory can be programmed byte by byte in less than 0.8 seconds. Designed, manufactured, and tested for a wide spectrum of applications, the 27SF256/27VF256 are offered with an endurance of 1000 cycles. Data retention is rated at greater than 100 years.

The 27SF256/27VF256 are suited for applications that require infrequent rewrites and low power nonvolatile storage. The 27SF256/27VF256 will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the 27SF256/27VF256 are offered in 32-pin PLCC, 28-pin PDIP and 28-pin TSOP packages. See Figures 1 and 2 for pinouts.

Device Operation

The 27SF256/27VF256 are low cost flash solutions that can be used to replace existing UV-EPROM, OTP, and mask ROM sockets. They are functionally (read and program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, the device also supports Electrical Erase operation. The 27SF256/27VF256 do not require a UV source to erase, and therefore the packages do not have a window.

Read

The Read operation of the 27SF256/27VF256 are controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of T_{OE} from the falling edge of OE#, assuming that CE# pin has been low and the addresses have been stable for at least T_{CE} - T_{OE}. The V_{PP} pin must be V_{CC} or V_{SS} during read operation. When the CE# pin is high, the chip is deselected and a typical standby current of 10 µA is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.

Programming operation

The 27SF256/27VF256 are usually programmed by using an external programmer. The programming mode is activated by asserting 12V (±5%) on Vpp pin, Vcc = 5V±5%, V_{IL} on CE# pin, and V_{IH} on OE# pin. The device is programmed byte by byte with the desired data at the desired address using a single pulse (CE# pin low) of 20 µs**.** Using the SuperFlash programming algorithm, the byte programming process continues byte by byte until the entire chip (32 Kbytes) has been programmed.

Chip Erase Operation

The only way to change a data from a "0" to "1" is by electrical erase that changes every bit in the device to "1". Unlike traditional EPROMs, which use UV light to do the chip erase, the 27SF256/27VF256 use an electrical chip erase operation. This saves a significant amount of time (about 30 minutes for each erase operation, compared with UV erase). The entire chip can be erased in 100 ms (CE# pulse). In order to activate the erase mode, the 12V (±5%) is applied to V_{PP} and A_9 pins, Vcc = 5V±5%, V_{IL} on CE# pin, and V_{IH} on OE# pin. All other address and data pins are "don't care". The falling edge of CE# will start the Chip Erase operation. Once the chip has been erased, all bytes must be verified for FF. Refer to figure 8 for the flow chart.

The 27SF256/27VF256 can also be reprogrammed in the system. This requires the availability of 12V for V_{PP} to program and an additional 12V for address A_9 to erase.

Product Identification Mode

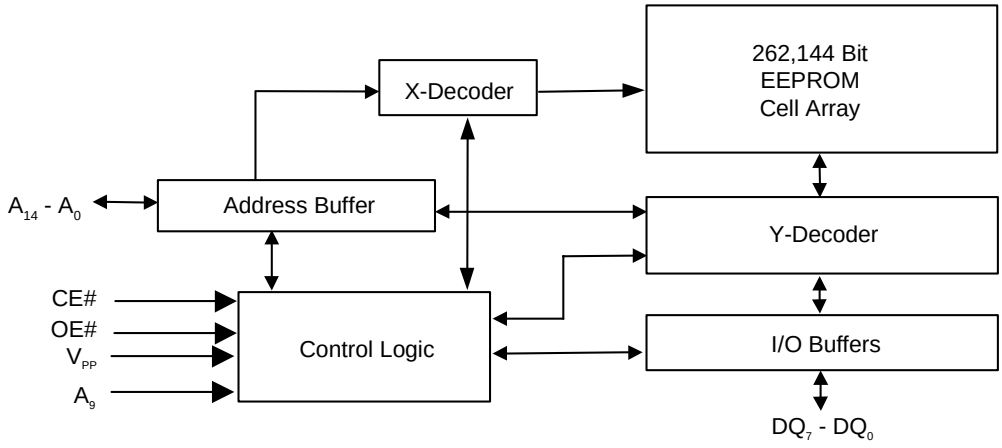
The product identification mode identifies the device as the 27SF256 or 27VF256 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V_H (12V±5%) on address A_9 with V_{PP} pin at 5V±10%. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0. For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Byte	Data
Manufacturer's Code	0000 H	BF H
27SF256 Device Code	0001 H	A3 H
27VF256 Device Code	0001 H	C3 H

321 PGM T1.0

FUNCTIONAL BLOCK DIAGRAM OF THE SST27SF256/27VF256



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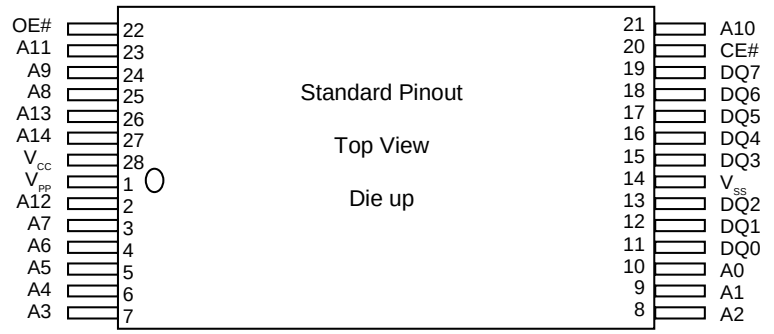

FIGURE 1: PIN ASSIGNMENTS FOR 28-PIN TSOP PACKAGES

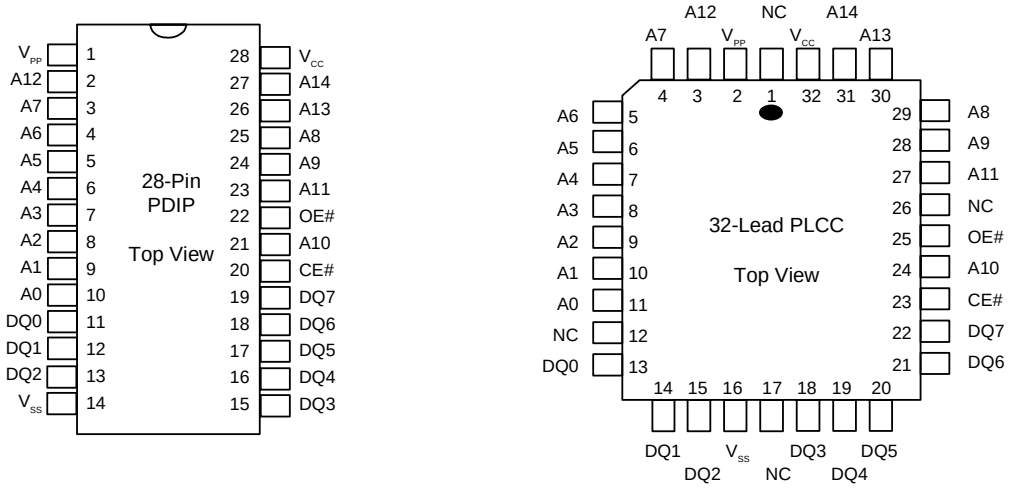

FIGURE 2: PIN ASSIGNMENTS FOR 28-PIN PLASTIC DIPS AND 32-LEAD PLCCS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{14}-A_0	Address Inputs	To provide memory addresses
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during program cycle, the outputs are in tri-state when OE# or CE# is high
CE#	Chip Enable	To activate the device when CE# is low
OE#	Output Enable	To gate the data output buffers during read operation and high voltage pin during chip erase and programming operation
V_{CC}	Power Supply	To provide 5-volt supply (±10%) for the 27SF256 and 3-volt supply (2.7-3.6 V) for the 27VF256
V_{PP}	Power Supply for Program or Erase	High voltage pin during chip erase and programming operation 12-volt (±5%)
V_{SS}	Ground	
NC	No Connection	Unconnected pins

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	V_{PP}	A_9	DQ	Address
Read	V_{IL}	V_{IL}	V_{CC} or V_{SS}	A_{IN}	D_{OUT}	A_{IN}
Output Disable	V_{IL}	V_{IH}	V_{CC} or V_{SS}	X	High Z	X
Program	V_{IL}	V_{IH}	V_{PPH}	A_{IN}	D_{IN}	A_{IN}
Standby	V_{IH}	X	V_{CC} or V_{SS}	X	High Z	X
Chip Erase	V_{IL}	V_{IH}	V_{PPH}	V_H	High Z	X
Program/Erase Inhibit	V_{IH}	X	V_{PPH}	X	High Z	X
Product Identification	V_{IL}	V_{IL}	V_{CC} or V_{SS}	V_H	Manufacturer Code (BF) Device Code (A3 for 27SF256 & C3 for 27VF256)	A_{14}-A_1 = V_{IL}, A_0 = V_{IL} A_{14}-A_1 = V_{IL}, A_0 = V_{IH}

Note: X = V_{IL} or V_{IH}
V_{PPH} = 12V±5%, V_H = 12V±5%

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC}+1.0V
Voltage on A_9 and Vpp Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

27SF256 OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	5V±10%
Industrial	-40°C to +85°C	5V±10%

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... 1 TTL Gate and C_L = 100 pF
See Figures 6 and 7

27VF256 OPERATING RANGE

Range	Ambient Temp	V_{CC}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... 1 TTL Gate and C_L = 100 pF
See Figures 6 and 7

TABLE 4: 27SF256 READ MODE DC OPERATING CHARACTERISTICS
V_{CC} = 5 V±10%, T_A = 0°C to 70°C (Commercial) or -40°C to +85°C (Industrial)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	V_{CC} Read Current		30	mA	CE# = OE# = V_{IL} all I/Os open, Address input = V_{IL}/V_{IH} at f = $1/T_{RC}$ Min., V_{CC} = V_{CC} Max
I_{PPR}	V_{PP} Read Current		100	µA	CE# = OE# = V_{IL}, all I/Os open, Address input = V_{IL}/V_{IH} at f = $1/T_{RC}$ Min., V_{CC} = V_{CC} Max ,Vpp = Vcc
I_{SB1}	Standby V_{CC} Current (TTL input)		3	mA	CE# = OE# = V_{IH}, V_{CC} = V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		50	µA	CE#=OE#=V_{CC}-0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0	Vcc+0.5	V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA, V_{CC} = V_{CC} Min.
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, A_9 = V_H Max.

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TABLE 5: 27VF256 READ MODE DC OPERATING CHARACTERISTICS
V_{CC} = 2.7-3.6V, T_A = 0°C to 70°C (Commercial) or -40°C to +85°C (Industrial)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Vcc Read Current		12	mA	CE#=OE#=V_{IL} all I/Os open, Address input = V_{IL}/V_{IH} at f=$1/T_{RC}$ Min., V_{CC}=V_{CC} Max
I_{PPR}	V_{PP} Read Current		100	µA	CE# = OE# = V_{IL}, all I/Os open, Address Input = V_{IL}/V_{IH} at f = $1/T_{RC}$ Min, V_{CC} = V_{CC} Max, Vpp = Vcc
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE#=OE#=V_{IH}, V_{CC} =V_{CC} Max.
I_{SB2}	Standby V_{CC} Current (CMOS input)		15	µA	CE#=OE#=V_{CC} -0.3V. V_{CC} = V_{CC} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage	2.0	Vcc+0.5	V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100 µA, V_{CC} = V_{CC} Min.
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, A_9 = V_H Max.

321 PGM T5.2

TABLE 6: 27SF256/27VF256 PROGRAM/ERASE DC OPERATING CHARACTERISTICS
V_{CC} = 5 V±10%, V_{pp} = V_{PPH}, T_A = 25°C±5°C

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CP}	V_{CC} Erase or Program Current		30	mA	CE# = V_{IL}, Vpp = 12V±5%, V_{CC} = V_{CC} Max
I_{PP}	V_{PP} Erase or Program Current		1	mA	CE# = V_{IL}, Vpp = 12V±5%, V_{CC} = V_{CC} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, V_{CC} = V_{CC} Max
V_H	Supervoltage for A_9	11.4	12.6	V	CE# = OE# = V_{IL}
I_H	Supervoltage Current for A_9		100	µA	CE# = OE# = V_{IL}, A_9 = V_H Max
V_{PPH}	High Voltage for V_{PP} Pin	11.4	12.6	V	

321 PGM T6.1

TABLE 7: POWER-UP TIMINGS

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$	Power-up to Read Operation	100	µs

321 PGM T7.0

TABLE 8: CAPACITANCE (T_A = 25 °C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

321 PGM T8.0

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	1000	Cycles	MIL-STD-883, Method 1033
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	300	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100	mA	JEDEC Standard 78

321 PGM T9.1

Note: (1) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 10: 27SF256 READ CYCLE TIMING PARAMETERS

Symbol	Parameter	27SF256-55		27SF256-70		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	55		70		ns
T_{CE}	Chip Enable Access Time		55		70	ns
T_{AA}	Address Access Time		55		70	ns
T_{OE}	Output Enable Access Time		25		30	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		20		25	ns
T_{OHZ}(1)	OE# High to High-Z Output		20		25	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

321 PGM T10.1

TABLE 11: 27VF256 READ CYCLE TIMING PARAMETERS

Symbol	Parameter	27VF256-120		27VF256-150		Units
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	120		150		ns
T_{CE}	Chip Enable Access Time		120		150	ns
T_{AA}	Address Access Time		120		150	ns
T_{OE}	Output Enable Access Time		50		60	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		30		30	ns
T_{OHZ}(1)	OE# High to High-Z Output		30		30	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

321 PGM T11.0

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

TABLE 12: PROGRAMMING/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{PRT}	V_{PP} Pulse Rise Time	50		ns
T_{AS}	Address Setup Time	2		µs
T_{AH}	Address Hold Time	2		µs
T_{VPS}	V_{PP} Setup Time	2		µs
T_{VPH}	V_{PP} Hold Time	2		µs
T_{PW}	CE# Program Pulse Width	20	40	µs
T_{EW}	CE# Erase Pulse Width	100	500	ms
T_{DS}	Data Setup Time	2		µs
T_{DH}	Data Hold Time	2		µs
T_{VR}	V_{PP} and A_9 Recovery Time	2		µs
T_{ART}	A_9 Rise Time to 12V during Erase	50		ns
T_{APS}	A_9 Setup Time during Erase	2		µs
T_{APH}	A_9 Hold Time during Erase	2		µs

321 PGM T12.1

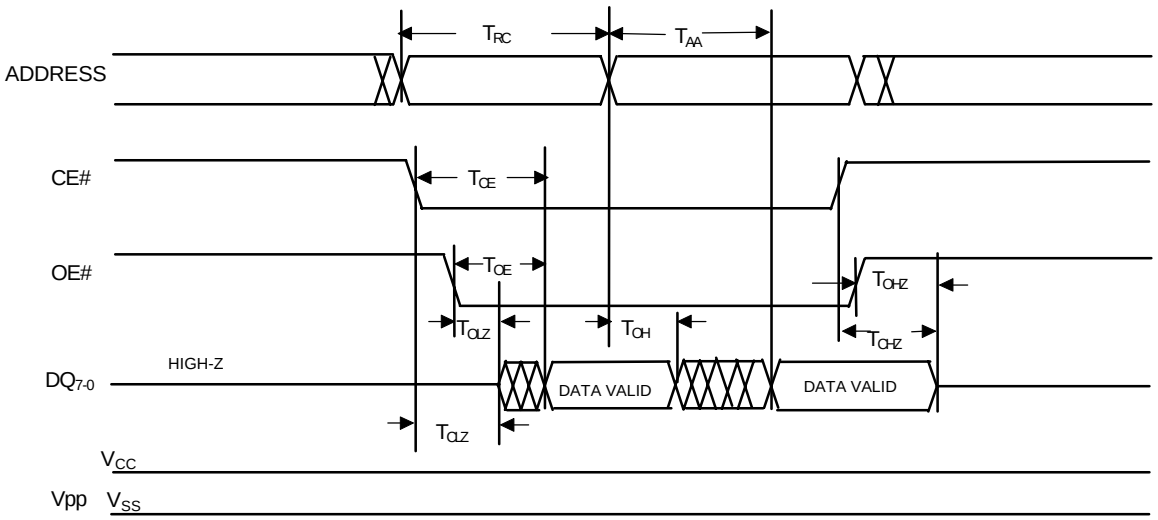

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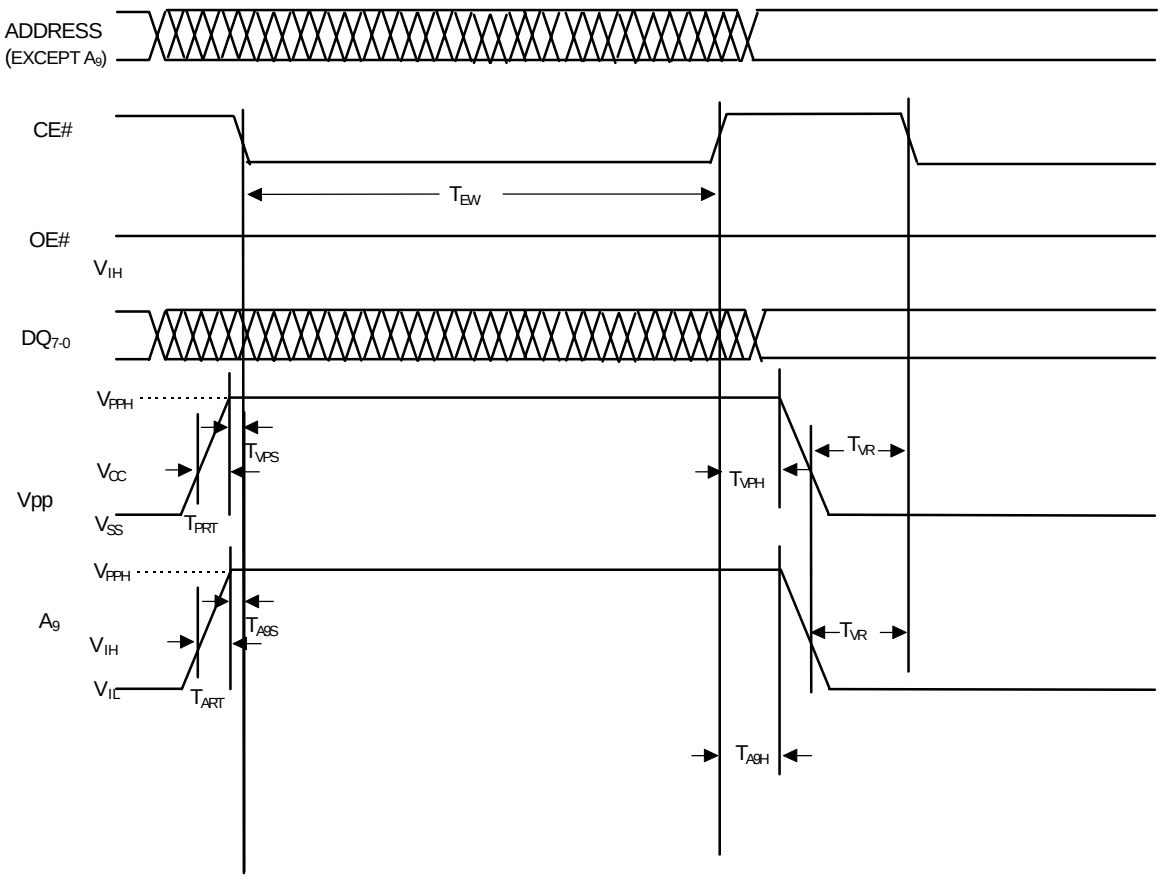
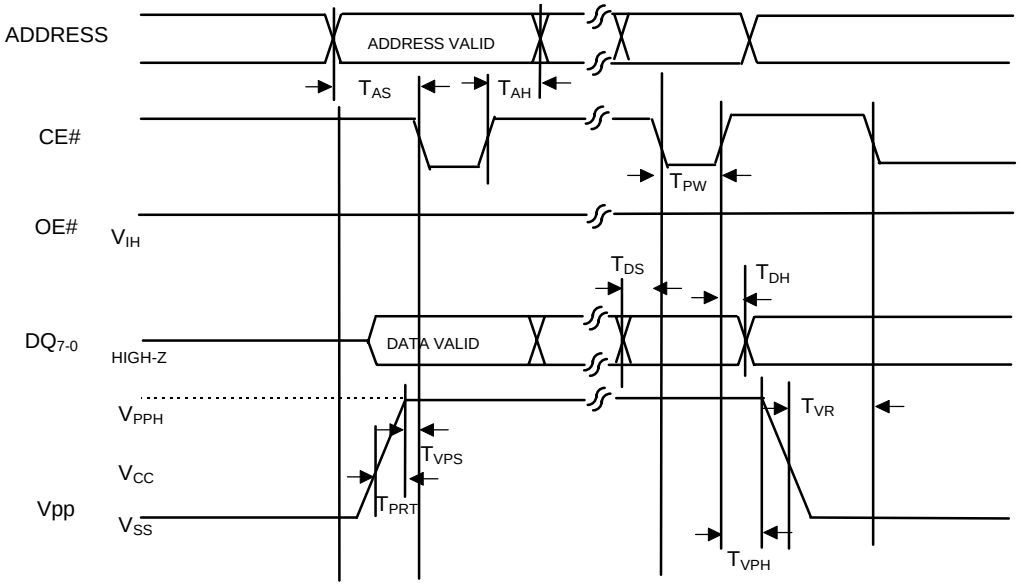
FIGURE 3: READ CYCLE TIMING DIAGRAM



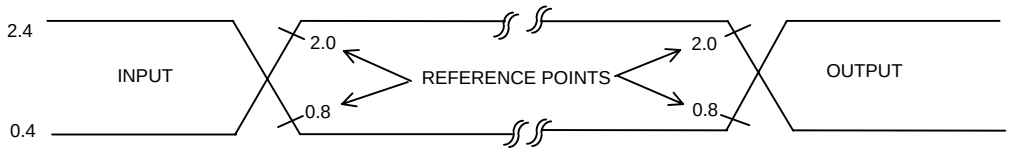
321 MSW F04.0

FIGURE 4: ERASE TIMING DIAGRAM



321 MSW F05.0

FIGURE 5: PROGRAM TIMING DIAGRAM



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AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

FIGURE 6: AC INPUT/OUTPUT REFERENCE WAVEFORMS

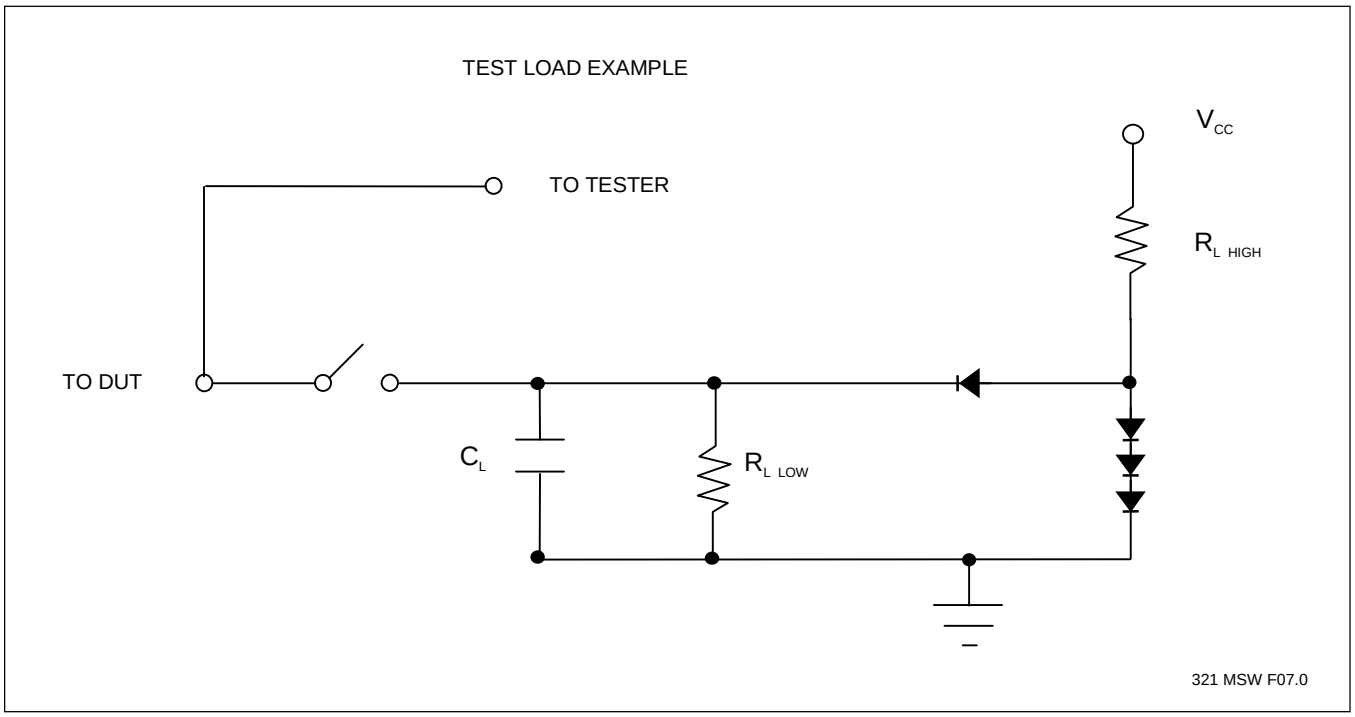


FIGURE 7: TEST LOAD EXAMPLE

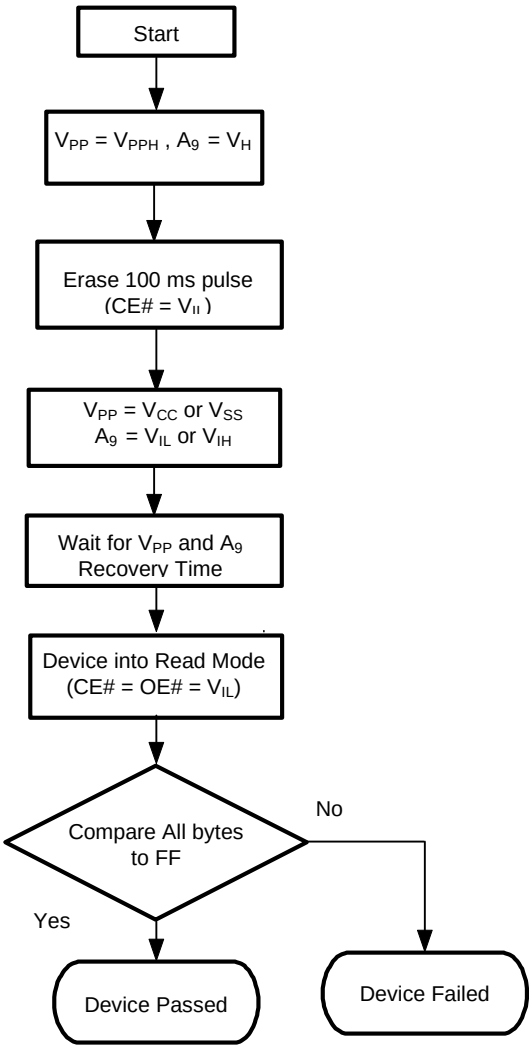


FIGURE 8: ERASE ALGORITHM

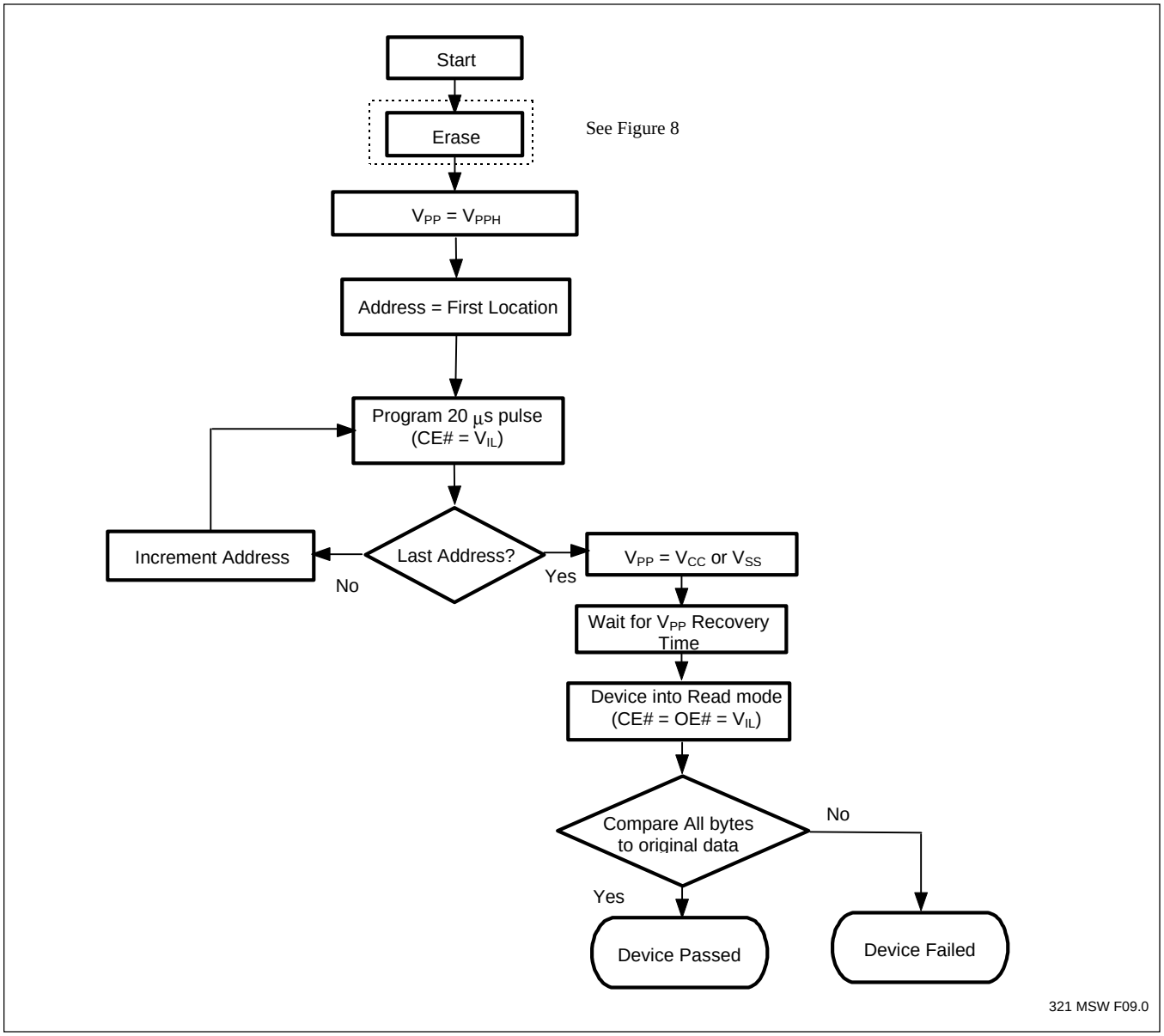
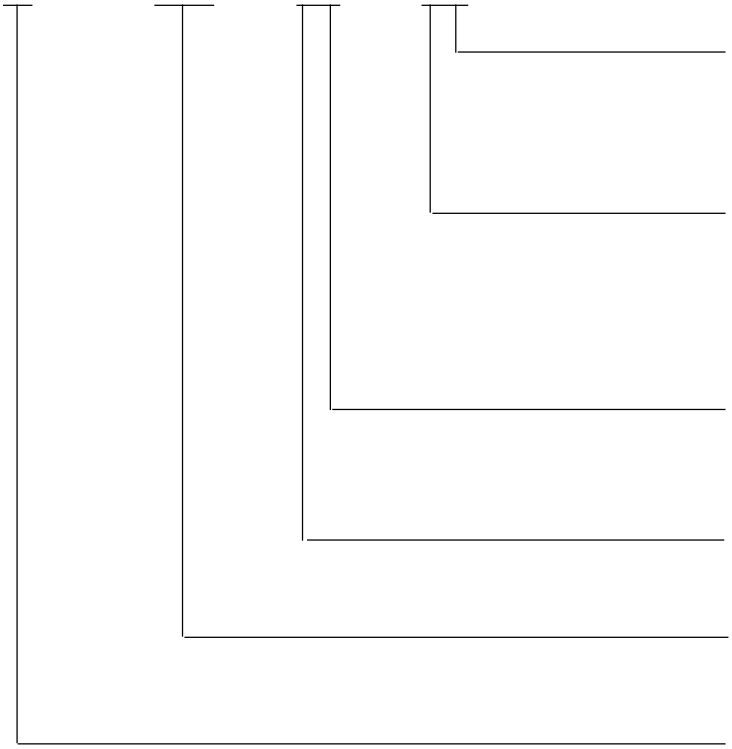


FIGURE 9: PROGRAMMING ALGORITHM

PRODUCT ORDERING INFORMATION

Device	Speed	Suffix1	Suffix2
SST27XF256	- XXX	- XX	- XX



Package Modifier
H = 32 leads,
G = 28 leads
Numeric = Die modifier

Package Type
P = PDIP
N = PLCC
K = TSOP (die up)
U = Unencapsulated die

Operating Temperature
C = Commercial = 0° to 70°C
I = Industrial = -40° to 85°C

Minimum Endurance
3 = 1000 cycles

Read Access Speed
55 = 55 ns, 70 = 70 ns,
120 = 120 ns, 150 = 150 ns

Read Voltage
S = 5.0 Volt Read
V = 2.7 Volt Read (2.7-3.6V)

27SF256 Valid combinations

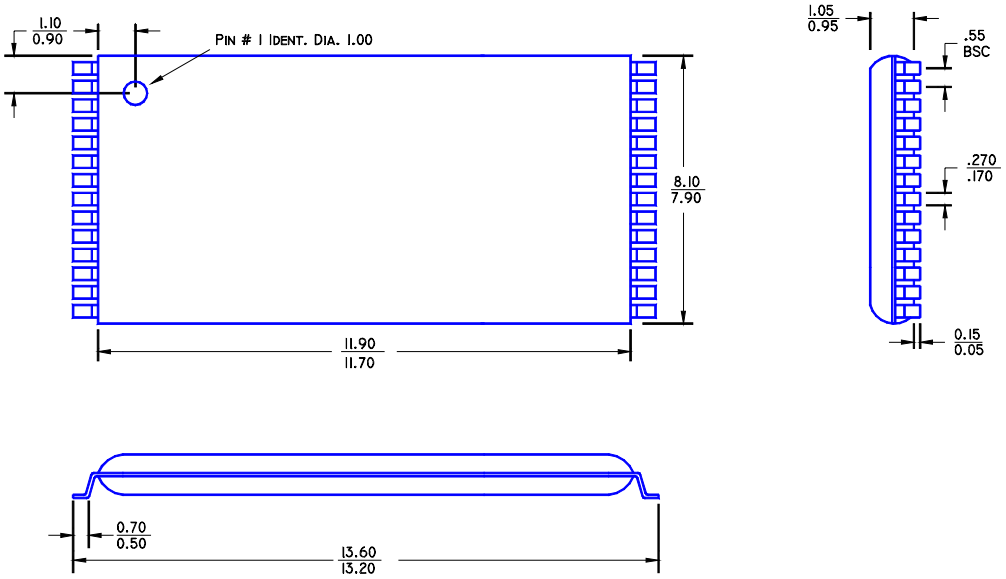
SST27SF256- 55-3C-KG	SST27SF256- 55-3C-NH	SST27SF256- 55-3C-PG
SST27SF256- 70-3C-KG	SST27SF256- 70-3C-NH	SST27SF256- 70-3C-PG
SST27SF256- 55-3I-KG	SST27SF256- 55-3I-NH	
SST27SF256- 70-3I-KG	SST27SF256- 70-3I-NH	SST27SF256- 70-3C-U1

27VF256 Valid combinations

SST27VF256- 120-3C-KG	SST27VF256- 120-3C-NH	SST27VF256- 120-3C-PG
SST27VF256- 150-3C-KG	SST27VF256- 150-3C-NH	SST27VF256- 150-3C-PG
SST27VF256- 120-3I-KG	SST27VF256- 120-3I-NH	
SST27VF256- 150-3I-KG	SST27VF256- 150-3I-NH	SST27VF256-150-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

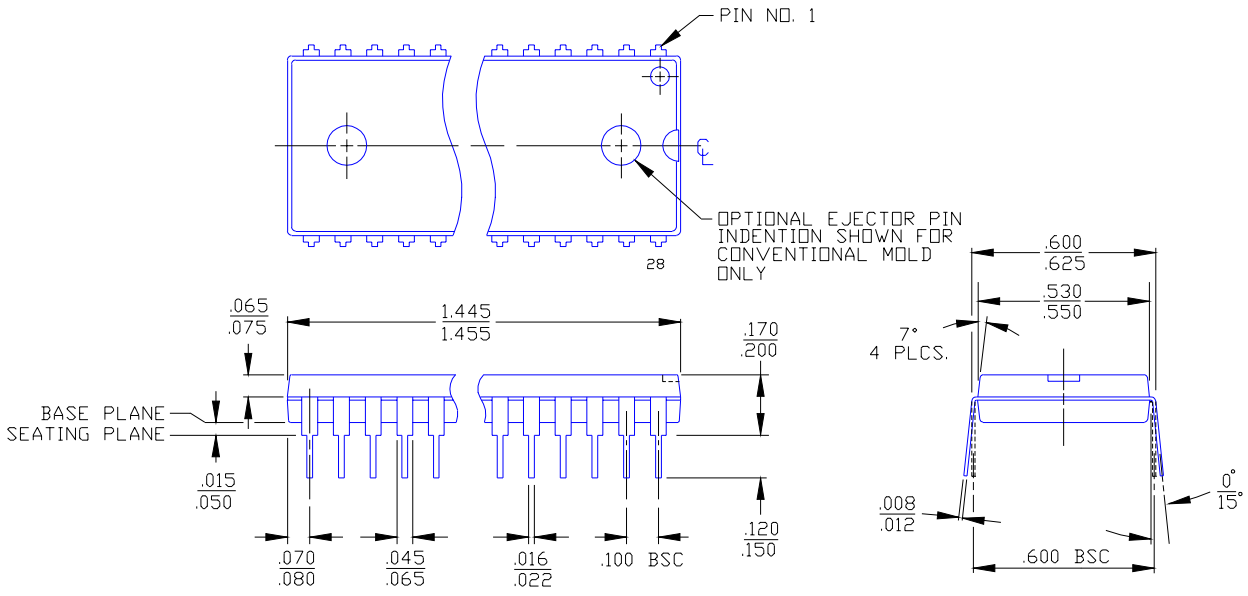
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-183 AA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

28pn TSOP KG AC.3

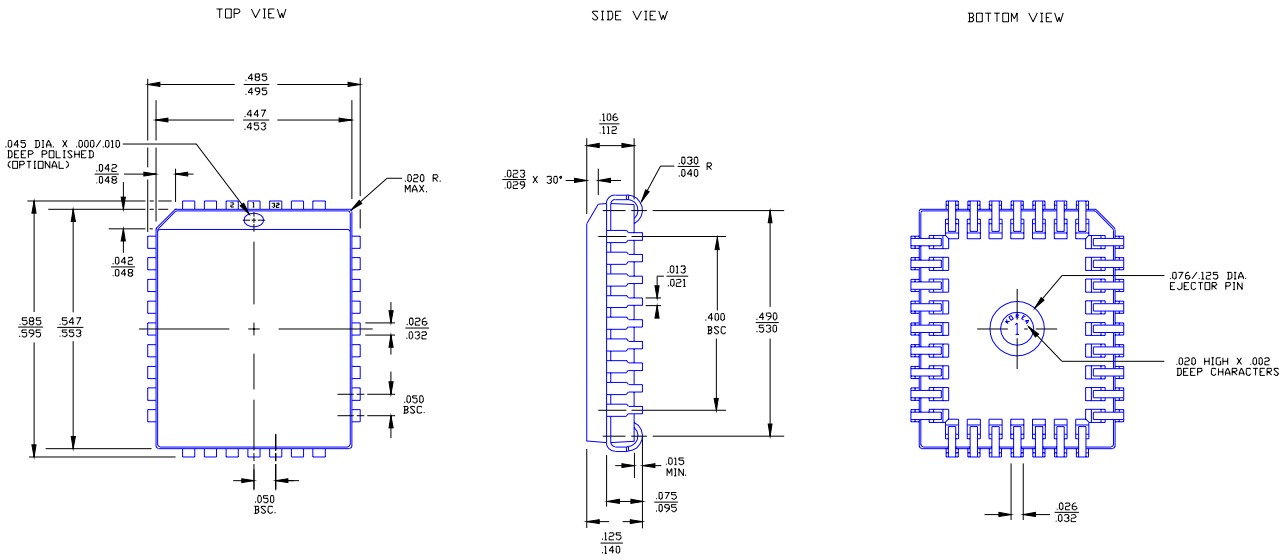
28-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: KG



Note: 1. Complies with JEDEC publication 95 MO-015 AH dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

28pn PDIP PG AC.2

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PG



32pn PLCC NH AC.3

Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)

SST PACKAGE CODE: NH