

RES

R87C

32K (4K × 8) CMOS UV EPROM

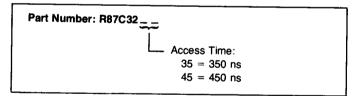
PRELIMINARY

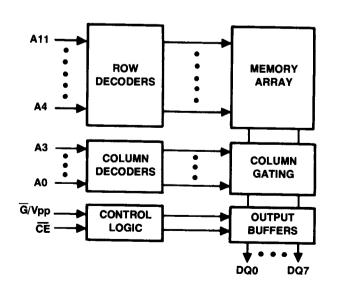
ORIG

FEATURES

- 4096 × 8 organization
- JEDEC approved pin-out
- Low Power
 - -Active: 132 mW (max.)
 - —Standby: 525 μ W (max.)
- Access time
 - -R87C32-45 450 ns (max.)
 - -R87C32-35 350 ns (max.)
- Single 5V power supply
- Static operation
 - -no clocks required
- Inputs and tri-state outputs TTL compatible during both read and program mode
- Standard 24-pin dual-in-line package
 - -Pin compatible with INTEL 2732A EPROM

ORDERING INFORMATION





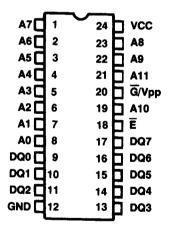
R87C32 Block Diagram

DESCRIPTION

The Rockwell R87C32 is a $4K \times 8$ (32,768 bits) ultraviolet (UV) light erasable programmable Read-Only-Memory (EPROM). It is manufactured using CMOS technology for low power dissipation in both active and standby operating modes. Single 5V operation allows simple circuit design in runtime environments.

Initially, all bits are in the "1" state. Programming is performed by applying 21V to \overline{G}/Vpp and a 50 ms "0" level to \overline{E} while the desired data is stable on DQ0-DQ7 lines and the address is stable on A0-A11 lines. All bits may be erased to the "1" state by exposure to a UV light source through the transparent window on the top of the device package.

The R87C32 EPROM is ideal for system development or low volume production applications requiring non-volatile memory in either multiple chip or single chip microcomputers with extended bus configurations. The low power requirements especially support applications using the R65C00 CMOS Microcomputer device family.



R87C32 Pin Configuration

A0-A11	ADDRESSES	
Ē	CHIP ENABLE	
<mark>G</mark> /∨pp	OUTPUT ENABLE/PROGRAM	
DQ0-DQ7	DATA OUTPUT	

R87C32 Pin Names

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	Vdc
Input Voltage All, except G/Vpp during Programming G/Vpp during Programming	V _{IN}	-0.3 to V _{CC} +0.3 -0.3 to +22.0	Vdc
Output Voltage	V _{OUT}	-0.3 to V _{CC} +0.3	Vdc
Temperature under Bias	T _A	-10 to +80	°C
Storage Temperature	T _{STG}	- 40 to 125	°C
Power Dissipation	Р	1.0	w

*NOTE: Stresses above those listed under ABSOLUTE MAX-IMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Read Mode	Program Mode	
V _{CC} Supply Voltage	5V ± 5%	5V ± 5%	
V _{PP} Supply Voltage		21V ± 0.5V	
Temperature Range	0 to 70°C	0 to 70°C	

DC OPERATING CHARACTERISTICS

 $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to $70^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
V _{OH}	Output High Voltage	2.4			V	$I_{OH} = -400 \mu\text{A}$
V _{OL}	Output Low Voltage			0.45	v	I _{OL} = 2.1 mA
V _{IH}	Input High Voltage	2.0	1	V _{cc}	V	
V _{IL}	Input Low Voltage	-0.1		0.8	V	
I _{CC1}	V _{CC} Standby Current			100	μА	$\overline{E} = V_{CC}$, $\overline{G} = 0V$, $V_{IN} = 0V$ or V_{CC}
I _{CC2}	V _{CC} Active Current			25	mA	$\overline{E} = \overline{G} = V_{IL}$
I _{PP}	V _{PP} Supply Current	······································		30	mA	$\overline{E} = V_{IL} \overline{G}/V_{PP} = V_{PP}$
I _{IN}	Input Leakage Current			±10	μΑ	V _{IN} = 0V to V _{CC}
lo	Output Leakage Current			±10	μΑ	V _{OUT} = 0V to V _{CC}

AC CHARACTERISTICS DURING READ

 $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to 70°C (unless otherwise specified)

	R87C32-35		R87C32-45					
Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Test Conditions
Address to Data Valid			350			450	ns	$\overline{\overline{E}} = \overline{\overline{G}} = V_{IL}$
Chip Enable to Data Valid			350			450	ns	$\overline{G} = V_{IL}$
Output Enable to Data Valid			120			120	ns	Ē = V _{IL}
Output Enable to High Impedance	0		100	0		100	ns	Ē = V _{IL}
Address to Output Hold	0	:		0			ns	$\overline{E} = \overline{G} = V_{IL}$
Chip Enable to High Impedance	0		100	0		100	ns	$\overline{G} = V_{II}$
	Address to Data Valid Chip Enable to Data Valid Output Enable to Data Valid Output Enable to High Impedance Address to Output Hold	Parameter Min. Address to Data Valid Chip Enable to Data Valid Output Enable to Data Valid Output Enable to High Impedance 0 Address to Output Hold 0	Parameter Min. Typ. Address to Data Valid Chip Enable to Data Valid Output Enable to Data Valid Output Enable to High Impedance 0 Address to Output Hold 0	Parameter Min. Typ. Max. Address to Data Valid 350 Chip Enable to Data Valid 350 Output Enable to Data Valid 120 Output Enable to High Impedance 0 100 Address to Output Hold 0	Parameter Min. Typ. Max. Min. Address to Data Valid Chip Enable to Data Valid Output Enable to Data Valid Output Enable to High Impedance Address to Output Hold Other Enable to High Impedance	Parameter Min. Typ. Max. Min. Typ. Address to Data Valid 350 Chip Enable to Data Valid 350 Output Enable to Data Valid 120 Output Enable to High Impedance 0 100 0 Address to Output Hold 0 0	ParameterMin.Typ.Max.Min.Typ.Max.Address to Data Valid350450Chip Enable to Data Valid350450Output Enable to Data Valid120120Output Enable to High Impedance01000Address to Output Hold000	ParameterMin.Typ.Max.Min.Typ.Max.UnitAddress to Data Valid350450nsChip Enable to Data Valid350450nsOutput Enable to Data Valid120120nsOutput Enable to High Impedance01000100nsAddress to Output Hold00ns

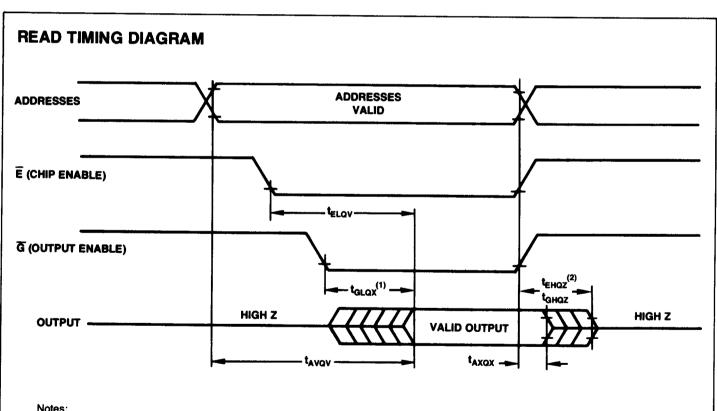
Notes:

Test Conditions:

Output Load: 1 TTL gate and $C_L = 100 pF$ Input Rise and Fall Times: <20 ns Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V



- 1. \overline{G} may be delayed up to $t_{AVQV}-t_{GLQX}$ after the falling edge of \overline{E} without impact on t_{AVQV} . 2. t_{GHQZ} , t_{EHQZ} is specified from \overline{G} or \overline{E} , whichever occurs first.

AC CHARACTERISTICS DURING PROGRAM

 $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Тур.	Max.	Units
t _{AVEL}	Address set-up time	2			μs
t _{GHEL}	G set-up time	2			μs
t _{DVEL}	Data set-up time	2			μs
t _{EHAX}	Address hold time	0			μs
t _{EHGL}	G hold time	2			μs
t _{EHDX}	Data hold time	2			μs
t _{EHQZ}	Output disable to output Hi-Z delay	0		100	ns
t _{ELQV}	Data valid from E			1	μs
t _{ELEH}	E pulse width during programming	45	50	55	ms
t _{PR}	G pulse rise time during programming	50			ns
t _{GLEL}	V _{PP} recovery time	2			μs

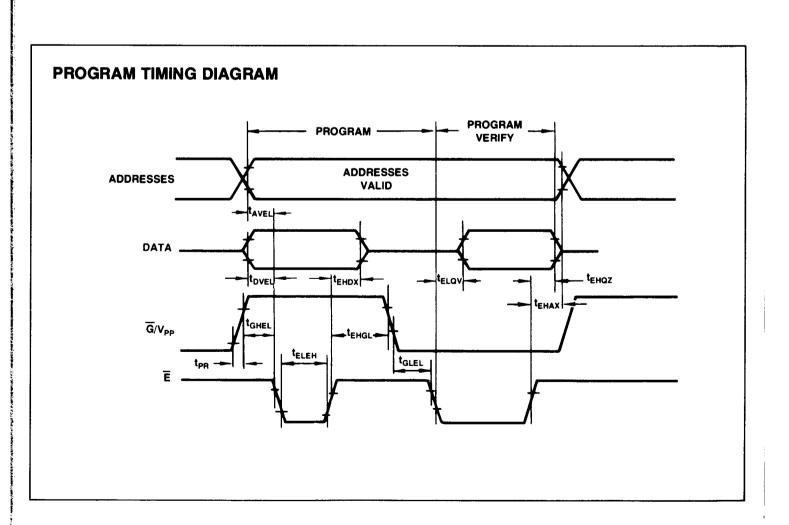
Notes:

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Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level: Inputs 1V and 2V

Outputs 0.8V and 2V



OPERATING MODES

The Rockwell R87C32 has five modes of operation (see table 1) and is pin compatible with Intel's 2732A.

The read mode is governed by two control pins, \overline{E} and \overline{G} . In order to obtain data at the outputs, both \overline{E} and \overline{G} must be V_{IL} . \overline{E} is the power control and should be used for device selection. \overline{G} is the output control and should be used to gate data to the output pins. Valid data will appear on the output pins after T_{AVQV} or T_{ELQV} times, depending on which is limiting.

The standby mode of the R87C32 reduces power dissipation. The R87C32 is placed in the standby mode by making $\overline{E} = V_{IH}$. This is independent of G and automatically puts the outputs in their high impedance (High-Z) state.

The R87C32 is in the programming mode when G/V_{PP} is at 21V. The data to be programmed is applied to the data output pins. When the address and data are stable, a 50 msec program pulse is applied to the \bar{E} input. Erasing the R87C32 for reprogramming is accomplished by exposing it to an ultraviolet light source for approximately 20 minutes.

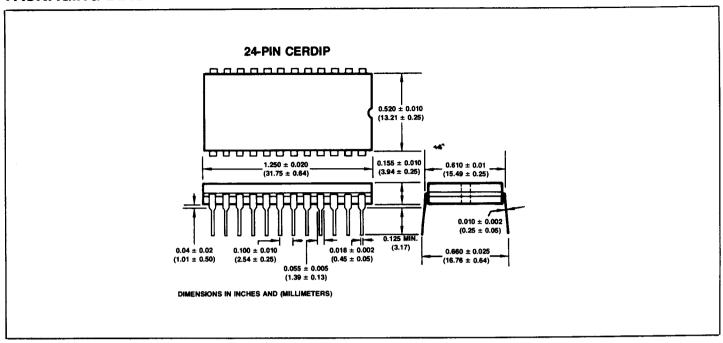
A program verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with \overline{G}/V_{PP} and \overline{E} at V_{IL} . Data should be verified t_{ELQV} after the falling edge of \overline{E} .

The program inhibit mode allows programming several R87C32 EPROMs simultaneously with different data for each by controlling which devices receive the program pulse on the $\overline{\mathbb{E}}$ pin.

Table 1. Mode Selection

Pin	E (18)	G/V _{PP} (20)	V _{CC} (24)	DQ0-DQ7 (9-11, 13-17)	
Read	V _{IL}	V _{IL}	+5	D _{out}	
Standby	V _{IH}	Don't care	+5	High-Z	
Program	Pulsed V _{IH} to V _{IL}	V _{PP}	+5	D _{IN}	
Program verify	V _{IL}	V _{IL}	+5	D _{OUT}	
Program inhibit	V _{IH}	V _{PP}	+5	High-Z	

PACKAGING DIAGRAM



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