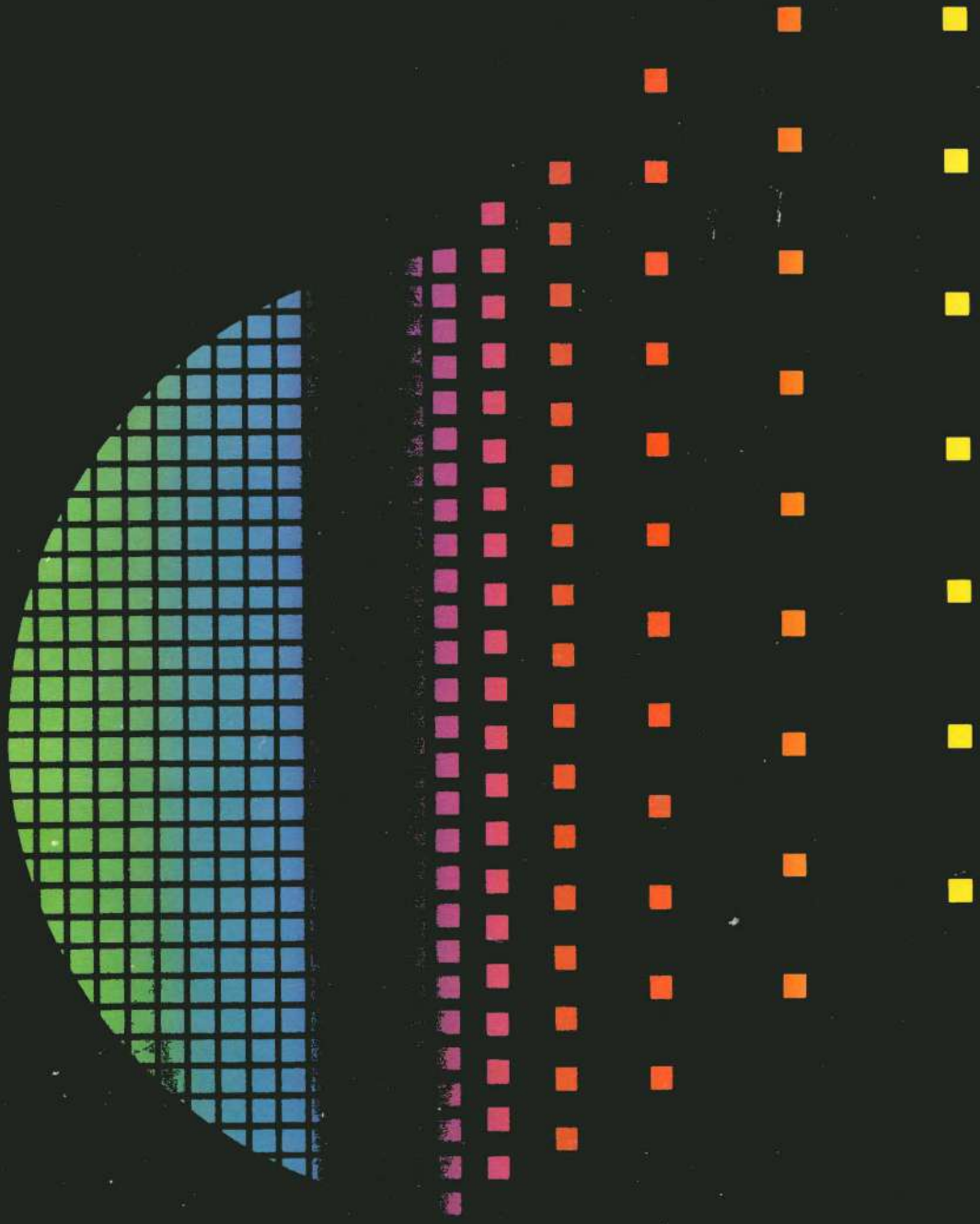
RAYTHEON DIGITAL



RAYTHEON DIGITAL

TOTAL
LOW-POWER SCHOTTKY
9LS/25LS/54LS/74LS

RAYTHEON
SEMICONDUCTOR DIVISION

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GENERAL DESCRIPTION

The Raytheon Low-Power Schottky TTL family utilizes advanced process technology, Schottky-barrier clamping, shallow diffusions, higher sheet resistivity and small geometries resulting in lower parasitic capacitance to achieve speeds comparable to 5400/7400 at one-fifth the power and 54H at one-tenth the power. The Raytheon TTL family is completely compatible with most of the popular TTL and DTL logic families and is equivalent in performance to the 9LS series.

Raytheon Schottky Diodes are produced by depositing platinum over the collector and base contact openings of Schottky transistors. A protective layer of Titanium/Tungsten alloy is deposited by a high-energy sputtering technique over the wafers. An alluminum layer is deposited and the interconnect pattern is etched-out during the final operation.

The tri-metal sandwich produced is one of the most reliable metalization systems available in the industry.

Raytheon has extensive experience in tri-metal metalization. For years similar techniques were used when producing tri-metal systems for the fabrication of Beam Lead devices.

FEATURES

- **High speed, Low-power**
- **5 nsec typical gate propagation delay time.**
- **2 mW typical gate power dissipation at 50% duty cycle.**

Table I compares Raytheon's Low-Power Schottky to the other TTL technologies.

Ease of System Design

- Switching times virtually insensitive to power supply, temperature variations.
- Low noise generation.
- High fan-out.
- Schottky-diode-clamped inputs minimize high-speed termination effects.
- Low output impedance gives low noise susceptibility, high capacitance drive capability.
- Power dissipation remains relatively low at operating frequencies up to 30 MHz.
- Smaller, lower-cost power supplies and cooling equipment.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (See Note 1) 7V
Input Voltage (See Notes 1 and 2) 7V
Interemitter Voltage (See Note 3) 5.5V
Output Voltage (See Notes 1 and 4). 7V
Operation Free-Air Temperature Range: . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C

NOTES:
1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. Except 54LS74, 109, 181, 196, 197. For 54LS74, 109, 181, 196, 197 rating is 5.5V.
3. This is the voltage between two emitters of a multiple-emitter transistor.
4. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

CIRCUIT CHARACTERISTICS

Dynamic Characteristic

The average propagation delay time is relatively insensitive to variations of power supply voltage and temperature. Figure 1 shows typical propagation delay of a gate versus temperature with two different capacitive loads.

TABLE I
SPEED POWER COMPARISON FOR TTL TECHNOLOGIES

Series		Avg. Gate Propagation Delay	Avg. Power Per Gate	Speed-Power Product
Low-Power Schottky	54LS (Ray)	5 ns	2mW	10 PJ
	54LS/74LS (T.I.)	10 ns	2mW	20 PJ
Schottky	54S/74S	3 ns	20mW	60 PJ
Standard	54/74	10 ns	10mW	100 PJ
Other	54H/74H	6 ns	23mW	138 PJ
	54L/74L	33 ns	1mW	33 PJ

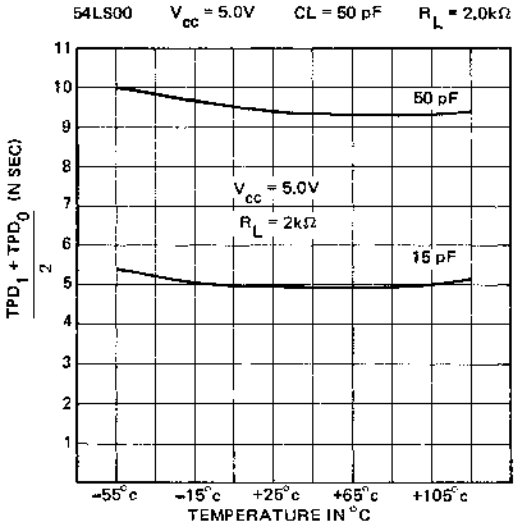


Figure 1. Propagation Delay Change With Temperature

The Raytheon LS family typically has 2 mW per gate power dissipation at 50% duty cycle, nearly constant to frequencies up to 5 MHz. P_D increases to 8 mW per gate at 30 MHz. Figure 2 shows the dynamic power dissipation at various frequencies for three different loading configurations.

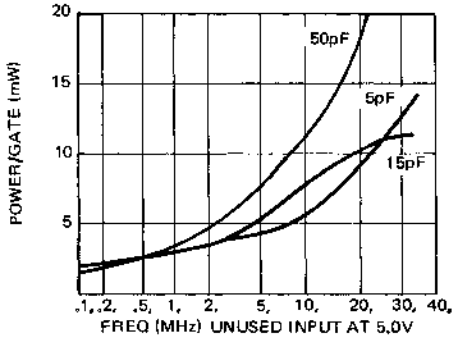


Figure 2. Dynamic Power Dissipation

With its advanced circuit technology, Raytheon LS devices have inherently low power dissipation and current spiking on the V_{CC} line during transitions. Far less than in standard TTL or high-power Schottky circuits. This advantage increases the "dynamic noise" margin of the overall system designed with 54LS. Figure 3 shows the V_{CC} spikes of Raytheon LS and standard 5400 and 54S circuits.

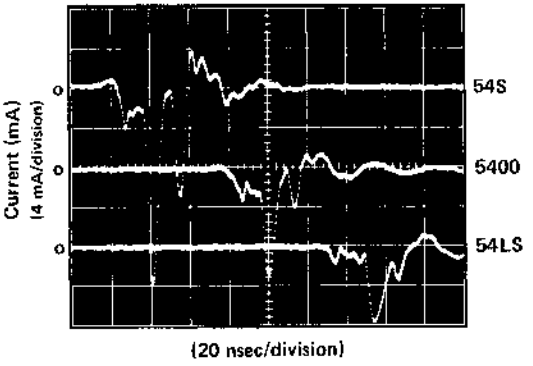


Figure 3. V_{CC} Current Spiking Raytheon 54LS, 54S, 5400 Comparison

A voltage higher than V_{OH} min should be maintained on the unused inputs of positive AND/NAND gates during dynamic testing. This will eliminate the distributed capacitance associated with the floating inputs, band wire, and package lead, and ensure that no degradation will occur in the propagation delay times. In addition to the circuits mentioned in Note 2, all Raytheon LS devices employ a DTL input circuitry with Schottky diodes. The unused inputs may be connected directly to V_{CC}.

INPUT CHARACTERISTIC

Schottky barrier diode clamping minimizes the high speed termination effects previously associated with TTL devices. Figure 4 shows input clamp diode voltage versus input current.

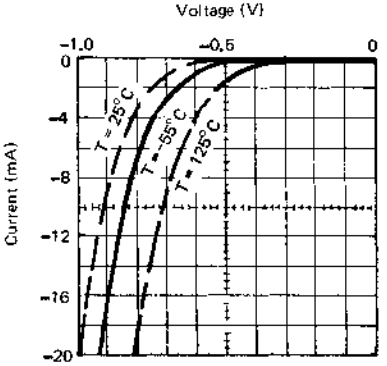


Figure 4. Clamp Diode Voltage Versus Input Current

OUTPUT CHARACTERISTIC

Figures 5 and 6 show the typical sinking capability of Raytheon Low-Power Schottky devices and the V_{IN} vs. V_{OUT} curves over the full military temperature range. As shown in the curves, Raytheon LS devices can be guaranteed with I_{OL} of 8.0 mA at V_{OL} of 0.45V max. and also high output fan-out of 22 over the full military temperature range.

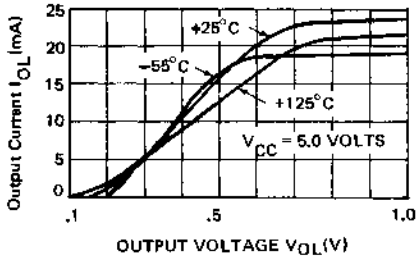


Figure 6

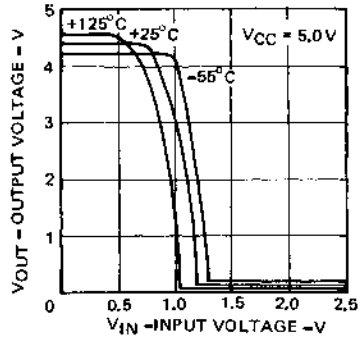


Figure 5. Typical Output vs. Input Voltage Characteristic

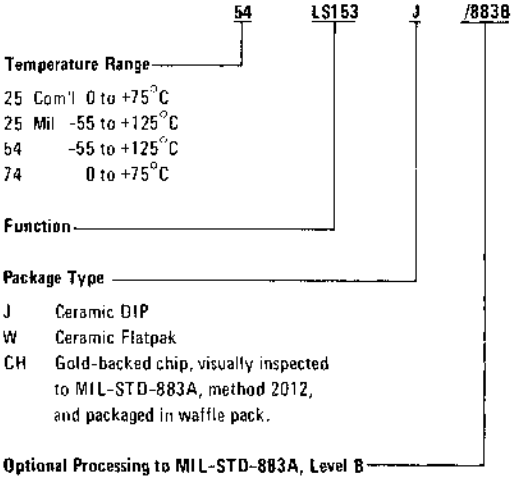
Ordering Information

Package Descriptions

BD	14-Pin Epoxy-B DIP	DB	14-Pin Epoxy-B DIP	L	16-Pin Metal Flatpak
BM	16-Pin Epoxy-B DIP	DC	14-Pin Ceramic DIP	MB	16-Pin Epoxy-B DIP
CJ	14-Pin Ceramic Flatpak	DM	16-Pin Ceramic DIP	MP	16-Pin Epoxy-B DIP
CK	14-Pin Ceramic Flatpak	J	14 or 16-Pin Ceramic DIP	R	24-Pin Ceramic DIP
CL	16-Pin Ceramic Flatpak	DP	14-Pin Epoxy-B DIP	N	24-Pin Glass/Metal Flatpak
CN	24-Pin Ceramic Flatpak	K	TO-3 Power Pack	W	14-Pin Ceramic Flatpak
D	14-Pin Metal DIP				

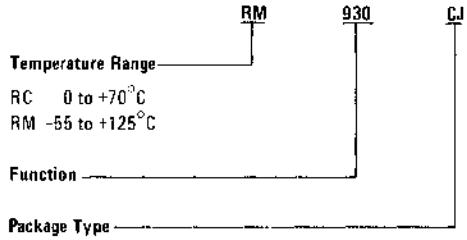
Ordering Information

Low Power Schottky

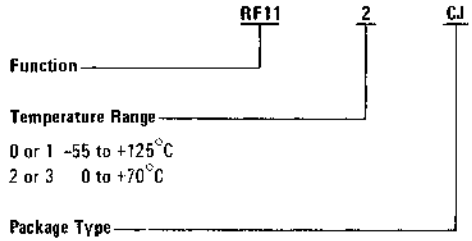


Notes:
1. 54LS orders will be branded 54LS
2. 9LS orders will be branded 9LS/54LS or 9LS/74LS depending upon temperature range.
3. 25LS orders will be branded 25LS
4. For MIL-M-38510 device types, order by the JAN part numbering system.

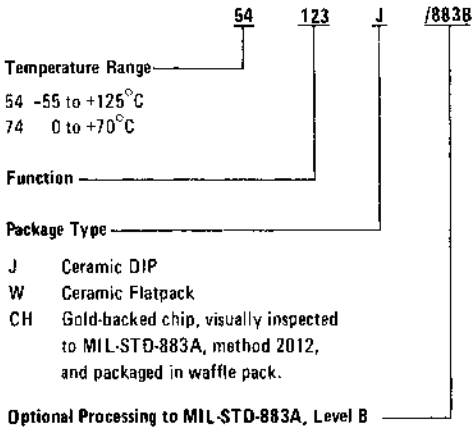
930 DTL Series



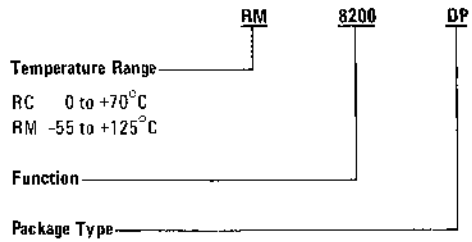
RAY I, II and III TTL Series



54/7400 SSI and MSI Series



8200 MSI Series



RAYTHEON

RAYACT-883A PROGRAM

The Raytheon Acceptance Testing Program called Rayact-883A involves in-process inspections which assure compliance with MIL-STD-883A test methods and MIL-M-38510 Program Plan Requirements.

Table 1 defines the Standard Process Flow for Raytheon Semiconductor's Military Level Integrated Circuits. After completion of the in-process inspections and 100% production screens, each lot is subjected to a quality conformance inspection as defined in Table 2. The screening and acceptance testing outlined in Tables 1 and 2 are provided at no extra cost.

In addition to the Standard Process Flow and acceptance testing, Qualification Tests in accordance with MIL-STD-883A, Method 5005 are conducted every three months on each product line. Generic Summary Data of Groups A, B, and C testing (Table 3) is available upon request.

The level of reliability you desire can be selected from Table 4. These tests are conducted in accordance with Method 5004 of MIL-STD-883A.

APPLICABLE DOCUMENTS:

Military: MIL-STD-883A
MIL-M-38510

Raytheon Semiconductor:
Quality Reliability Assurance Manual

Table 1—Standard Process Flow Summary for Integrated Circuits

MANUFACTURING OPERATION	MANUFACTURING INSPECTION	QUALITY/RELIABILITY INSPECTION
Manufacturing Stores	Purchased Item Verification	Receiving Inspection To Applicable M&SS and Blueprint Number
Mask Making	Mask Inspection	Mask Inspection
Materials Preparation	Wafer Preparation and Epitaxial Growing	Q.C. Monitor
Photoengraving and Diffusion	Electrical Probe Check and 100% Visual Inspection	Q.C. Monitor
Final Wafer Lot Acceptance	100% Visual Inspection	Q.C. Wafer Lot Acceptance
Electrical Test of Wafer	100% Electrical Test	Q.C. Monitor
Scribing and Dicing	100% Visual Inspection	Q.C. Monitor
Visual Die Sort MIL-STD-883A, Method 2010.2, Condition B	100% Die Sort Inspection	Dice Lot Acceptance
Die Attach	100% Visual Inspection	Q.C. Monitor
Lead Bond	100% Visual Inspection	Q.C. Monitor
Pre-Seal Inspection at 100X Magnification MIL-STD-883A, Method 2010, Condition B	100% Visual Inspection at High-Power Magnification	Q.C. Lot Acceptance
Pre-Seal Inspection at 30X Magnification MIL-STD-883A, Method 2010, Condition B	100% Visual Inspection at Low-Power Magnification	Q.C. Lot Acceptance

Table 1—Standard Process Flow Summary for Integrated Circuits (Cont.)

MANUFACTURING OPERATIONS	MANUFACTURING INSPECTION	QUALITY/RELIABILITY INSPECTION
Final Seal	Visual and Hermeticity	Q.C. Monitor
High-Temperature Bake 150°C 24 Hours Minimum (MIL-STD-883A, Method 1008, Condition C)	100% Processing	Q.C. Monitor
Temperature Cycling −65°C to +150°C, 10 Cycles (MIL-STD 883A, Method 1010, Condition C)	100% Processing	Q.C. Monitor
Centrifuge 30 KG Minimum Y_1 Axis (MIL-STD-883A, Method 2001, Condition E)	100% Processing	Q.C. Monitor
Lead Form	100% Visual Inspection	Q.C. Monitor
Carrier Load	100% Visual Inspection	Q.C. Monitor
Hermeticity MIL STD-883A, Method 1014		Q.C. Monitor
External Visual	100% Inspection	Q.C. Monitor
Electrical Test and Sort	100% Inspection	Q.C. Monitor

Table 2—Quality Conformance Inspection (Each Lot)

INSPECTION		LTPD/MAX. ACC. NO.	COMMENTS
External		7/2	MIL-STD-883A, Method 2009
Hermeticity		7/2	
Fine Leak			MIL-STD-883A, Method 1014, Condition A or B
Gross Leak			MIL-STD-883A, Mthod 1014, Condition C_2
Electrical			Per Applicable Electrical Test Specification
Static Parameters	+25°C	5/1	
	+125°C	7/1	
	−55°C	7/1	
Dynamic Parameters	+25°C	5/1	
	+125°C	7/1	
	−55°C	7/1	
Package and Ship		Quality Assurance Monitor	

NOTE:
Generic Qualification Data in accordance with MIL-STD-883A, Method 5005, can be supplied if negotiated prior to procurement.

Table 3A—Group A Electrical Tests—MIL-STD-883A

SUBGROUPS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1 Static tests at 25°C	5	5	5
Subgroup 2 Static tests at maximum rated operating temperature	5	7	10
Subgroup 3 Static tests at minimum rated operating temperature	5	7	10
Subgroup 4 Dynamic tests at 25°C	5	5	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	5	7	10
Subgroup 6 Dynamic tests at minimum rated operating temperature	5	7	10
Subgroup 7 Functional tests at 25°C	3	5	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperatures	5	10	15
Subgroup 9 Switching tests at 25°C	5	7	10
Subgroup 10 Switching tests at maximum rated operating temperature	5	10	15
Subgroup 11 Switching tests at minimum rated operating temperature	5	10	15

NOTE:

The specific parameters to be included for tests in each subgroup shall be as specified in the applicable reliability specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing shall be performed for that subgroup or test to satisfy group A requirements.

Table 3B—Group B Tests, MIL-STD-883A, Method 5005

	TEST	MIL-STD-883		CLASS A	CLASS B	CLASS C
		METHOD	CONDITION	LTPD	LTPD	LTPD
Subgroup 1	Physical dimensions	2016		10	15	20
Subgroup 2	Resistance to solvents	2015		3 devices (no failures)	3 devices (no failures)	3 devices (no failures)
	Visual and mechanical	2014	Criteria from design and construction requirements of applicable procurement document	1 device (no failures)	1 device (no failures)	1 device (no failures)
	Bond strength	2011		5	15	20
	Thermocompression		Test condition C or D			
	Ultrasonic or wedge		Test condition C or D			
Subgroup 3	Solderability	2003	Soldering temperature of 260°C ±10°	10	15	15
Subgroup 4	Lead fatigue	2004	Test condition B_2	10	15	15
	Seal: Fine, Gross	1014	As applicable			

Table 3C—Group C Tests, MIL-STD-883A, Method 5005

TEST	MIL-STD-883A		CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
	METHOD	CONDITION			
Subgroup 1 (Note 1)					
Thermal shock	1011	Test condition B as a minimum.	10	15	15
Temperature cycling	1010	Test condition C			
Moisture resistance	1004				
Seal	1014	As applicable			
a. Fine					
b. Gross (Note 7)					
Visual examination (Note 2)					
End point electrical parameters		As specified in the applicable procurement document.			
Subgroup 2 (Note 1)					
Mechanical shock	2002	Test condition B	10	15	15
Vibration, variable frequency	2007	Test condition A			
Constant acceleration	2001	Test condition E			
Seal	1014	As applicable			
a. Fine					
b. Gross (Note 7)					
Visual examination (Note 3)					
End point electrical parameters		As specified in the applicable procurement document.			
Subgroup 3					
Salt atmosphere (Note 4)	1009	Test condition A	10	15	15
Visual examination (Note 5)					
Subgroup 4					
High temperature storage (Note 6)	1008	Test condition C 1000 hours.	7	7	7
End point electrical parameters		As specified in the applicable procurement document.			
Subgroup 5					
Operating life test (Note 6)	1005	Test condition to be specified in the applicable procurement document (1000 hours).	5	5	5
End point electrical parameters		As specified in the applicable procurement document.			
Subgroup 6					
Steady state reverse bias	1005	Test condition A, 72 hours at 150°C.	7	–	–
End point electrical parameters		As specified in the applicable procurement document.			

NOTES:

1. Devices used for environmental tests in subgroup 1 may be used for mechanical tests in subgroup 2.
2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
3. Visual examination shall be performed at a magnification of 5X to 10X for evidence of defects of damage to case, leads, or seals resulting from testing (not fixturing) such damage shall consitute a failure.
4. Electrical reject devices from the same inspection lot may be used for samples.
5. Visual examination shall be performed in accordance with 3.3.1 of method 1009.
6. See 40.4 of appendix B of MIL-M-38510.
7. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.

Table 4—Optional Screening—MIL-STD-883A, Method 5004

SCREEN	CLASS A		CLASS B		CLASS C	
	METHOD	REQUIREMENT	METHOD	REQUIREMENT	METHOD	REQUIREMENT
Internal visual (Precap)	2010 test condition A	100%	2010 test condition B	100%	2010 test condition B	100%
Stabilization bake	1008, 24 hrs. test condition C, 150°C	100%	1008, 24 hrs. test condition C, 150°C	100%	1008, 24 hrs. test condition C, 150°C	100%
Thermal shock	1011, test condition A, 0°C-100°C 15 cycles	100%	Not required		Not required	
Temperature cycling	1010 test condition C, −65°C to +150°C 10 cycles	100%	1010, test condition C, −65°C to +150°C 10 cycles	100%	1010, test condition C, −65°C to +150°C 10 cycles	100%
Mechanical shock	2002**	100%	Not required		Not required	
Constant Acceleration	2001, test condition E Y_2 plane, then Y_1 plane, 30,000 G's	100%	2001, test condition E Y_1 plane, 30,000 G's	100%	2001, test condition E Y_1 plane, 30,000 G's	100%
Seal Fine, Gross	1014, Condition A Condition C Hermetic devices only	100%	1014, Condition A Condition C Hermetic devices only	100%	1014, Condition A Condition C Hermetic devices only	100%
Critical electrical parameters	*	100%	Go-No-Go		Not required	
Burn-in test	1015, 240 hrs. @ T_A = 125°C*	100%	1015, 168 hrs. @ T_A = 125°C*	100%	Not required	
Critical electrical parameters	*	100%	Not required		Not required	
Reverse bias burn-in	1015, test condition A or C, 72 hrs. @ 150°C	100%	Not required		Not required	
Final electrical test	*		*		*	
Static tests 25°C		100%		100%		100%
Maximum and minimum rated operating temp.		100%		100%		
Dynamic tests and switching tests 25°C		100%		100%		
Functional test 25°C (subgroup 7, table 1, 5005)		100%		100%		100%
Group A Testing	Per Table 3A		Per Table 3A		Per Table 3A	
Radiographic	2012	100%	Not required		Not required	
Qualification or quality conformance inspection Groups B and C optional, at extra cost	5005	*	5005	*	5005	*
External visual	2009	100%	2009	100%	2009	100%

*Per applicable procurement document

**Test Condition E one shock pulse in Y_1 plane only or five shock pulses at Condition B in Y_1 plane only.

Introduction

Raytheon's A+ program is designed to provide the Industrial and Commercial marketplace with product reliability. ■ Reliability consistent with application requirements. ■ Reliability that avoids an **overbuy** situation where the user pays for screening beyond the scope of his needs.

Raytheon offers three screening flows under the A+ program. Each having a separate reliability factor and cost saving. When deciding which A+ flow best suits your needs, you should consider the cost savings realized through elimination of outside lab services and the need to tighten incoming inspection. Users who do not presently have their integrated circuits screened should consider the cost of component replacement during system test and in the field. Substantial cost savings can now be realized by specifying Raytheon's A+ program.

The designations A+1 and A+2 are used for epoxy B packaged devices only. A+3 is reserved for ceramic devices. The appropriate screening level may be specified by simply adding the proper A+ suffix to the Raytheon part number, i.e., - - RC4136DB with A+2 screening would be designated RC4136DB2.

Customers who use the epoxy package may wish to obtain a copy of the **Epoxy Encapsulated Linear I.C. Quality Review**, available from your local Raytheon sales office.

Basic Reliability Measures

Raytheon has instituted an internal program to assure that products bearing the Raytheon logo are unsurpassed in reliability when used in the industrial environment. Several tests, including some normally reserved for military products, are applied to our industrial products on a continuing basis in support of this effort. A brief summary of these tests is given below.

1. Monitored Burn-In (all packages)

24 hours at +100°C with zero failures allowed. This RVT (reliability verification test), a Raytheon exclusive, is performed on 20 samples from each manufacturing lot.

2. Standard Burn-In (all packages)

168 hours at +125°C, 1% PDA. This RVT is performed on 200 samples from each EIA data code.

3. Operating Life (all packages)

1000 hours at +125°C, LTPD = 5. This RVT is performed on all new products and periodically on existing product types as an indicator of long-term reliability.

4. Pressure Cooker (epoxy packages only)

24 hours at +125°C in steam vapor, LTPD = 10. This RVT is performed on 25 samples from each EIA data code as to assure package and device integrity.

5. 85/85 (epoxy packages only)

168 hours with bias at +85°C and 85% relative humidity, STPD = 10. This RVT is performed on 25 samples from each EIA date code also as an indicator of package and device integrity.

6. Temperature Cycle (epoxy packages only)

100 cycles per method 1010.1, 0°C to 100°C. This RVT is performed on 25 samples from each EIA date code to mechanically stress the wire bond, die bond and package material.

7. Military Flow (ceramic packages and metal-cans)

Only dice lots which pass MIL-STD-883 condition B visual tests are used in these packages and the 883 class B flow is used up to point of electrical test. This provides military type product reliability at commercial prices.

A+ Programs Increase Reliability

Raytheon's A+ programs were designed to provide an even greater reliability assurance than standard process testing. Starting with devices which are processed with the basic reliability measures, various combinations of temperature cycle, burn-in, **Hot Rail** testing and tightened AQL lot acceptance are available as shown in the flow chart. The objectives of these 100% screens are:

1. Temperature Cycle (epoxy packages only)

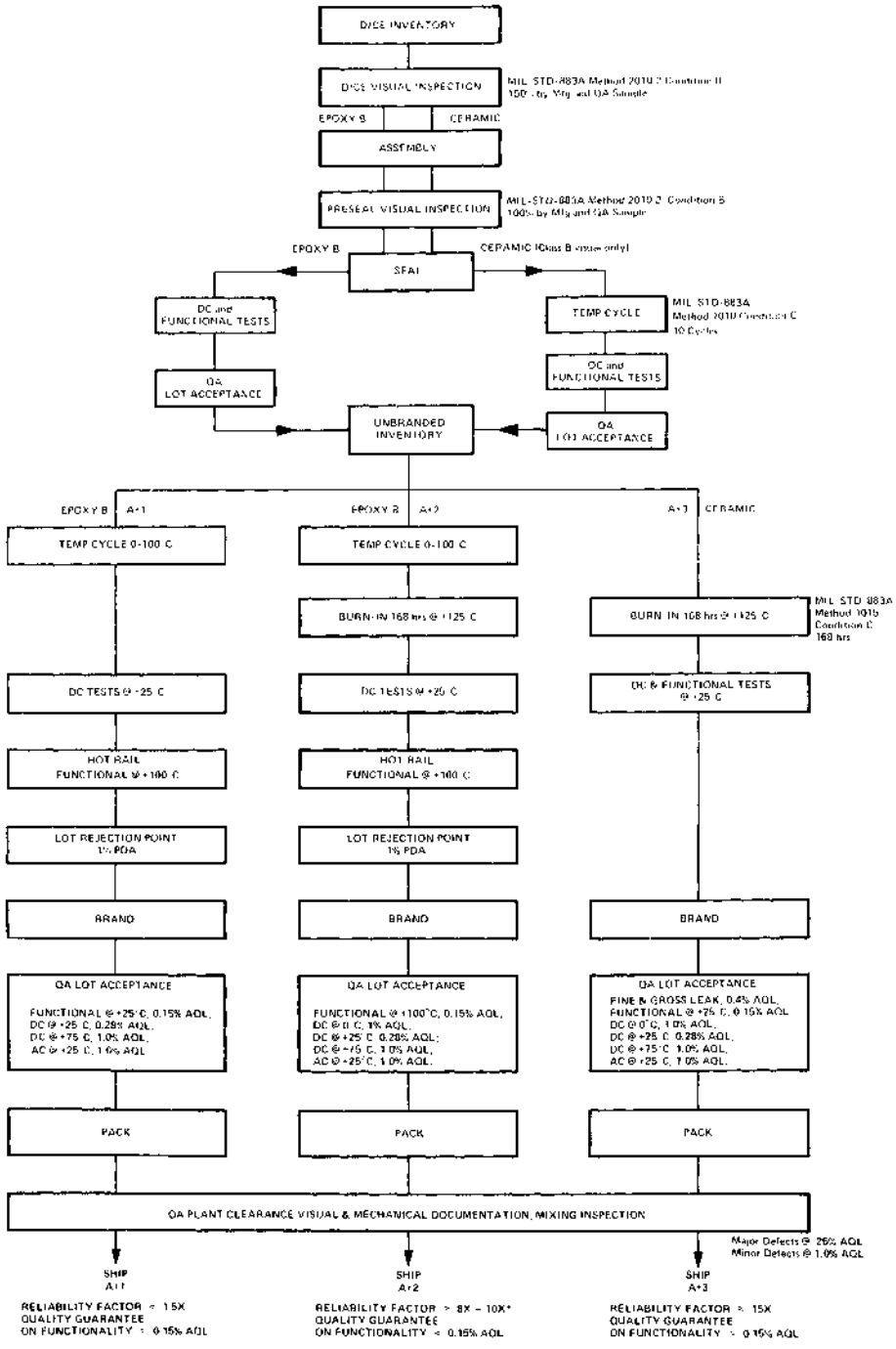
0°C to +100°C per method 1011, condition A. This is the first screening for the A+1 and A+2 flows. (A+3 ceramic and metal-can devices received temperature cycles as part of standard product flow.) The purpose of this screening is to stress wire bonds and die bonds mechanically to prove the integrity of the devices.

2. Burn-In (all packages)

168 hours at +125°C. This screening is performed in A+2 and A+3 flows.

3. High Temperature Functional Test (Hot Rail) (epoxy packages only)

+100°C. This screening serves to further prove bond integrity.



* Must be expressed as a range since a normally controlled environment (constant power and temperature) cannot be assured.

DEFINITIONS OF SYMBOLS AND TERMS

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element withing specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} Supply current, output(s) high
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} Supply current, output(s) low
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

*Current flowing out of a terminal is a negative value.

DYNAMIC CHARACTERISTICS (continued)

t_{HZ} Output disable time (of a three-state output) from high level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} Output disable time (of a three-state output) from low level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} Propagation delay time, low-to-high-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} Transition time, low-to-high-level output
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} Transisition time, high-to-low-level output
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high-level to the defined low-level.

t_w Average pulse width
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ Release time
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{setup} Setup time
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} Output enable time (of a three-state output) to high level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} Output enable time (of a three-state output) to low level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

SECTION 1
Selection Guide To Raytheon Digital Products

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FEATURES

- High Speed, Low Power
  - 5 ns typical gate propagation delay time
  - 2 mW typical gate power dissipation at 50% duty cycle = speed-power product of 10pJ
- Ease of System Design
  - Switching times virtually insensitive to power supply, temperature variations
  - Low noise generation
  - High fan-out
  - Schottky-diode-clamped inputs minimize high-speed termination effects
  - Low output impedance gives low noise susceptibility, high capacitance drive capability
  - Power dissipation remains relatively low at operating frequencies up to 30 MHz
  - Smaller, lower-cost power supplies and cooling equipment

9LS/54LS/74LS Low Power Schottky

Type Number	Description	Prop Delay[1] (ns) or Max. Op. Freq. (MHz)[2]	Pwr Diss. (mW)	Available Packages					
				14 Pin		16 Pin		24 Pin	
				J	W	J	W	J	W
9LS/54LS/74LS00	Quad 2-input NAND gate	10	8	X	X				
9LS/54LS/74LS01	Quad 2-input NAND gate, open collectors	20	8	X	X				
9LS/54LS/74LS02	Quad 2-input NOR gate	10	11	X	X				
9LS/54LS/74LS03	Quad 2-input NOR gate, open collectors	20	8	X	X				
9LS/54LS/74LS04	Hex inverter	10	12	X	X				
9LS/54LS/74LS05	Hex inverter, open collectors	20	12	X	X				
9LS/54LS/74LS08	Quad 2-input AND gate	12	17	X	X				
9LS/54LS/74LS09	Quad 2-input AND gate, open collectors	17.5	17	X	X				
9LS/54LS/74LS10	Triple 3-input NAND gate	10	6	X	X				
9LS/54LS/74LS11	Triple 3-input AND gate	12	13	X	X				
9LS/54LS/74LS12	Triple 3-input NAND gate, open collectors	20	6	X	X				
9LS/54LS/74LS13	Dual 4-input Schmitt trigger	20	60	X	X				
9LS/54LS/74LS14	Hex Schmitt trigger	20	60	X	X				
9LS/54LS/74LS15	Triple 3-input AND gate, open collectors	17.5	13	X	X				
9LS/54LS/74LS20	Dual 4-input NAND gate	10	4	X	X				
9LS/54LS/74LS21	Dual 4-input AND gate	17.5	8.5	X	X				
9LS/54LS/74LS22	Dual 4-input NAND gate, open collectors	20	4	X	X				
9LS/54LS/74LS26	LS03, 15 volt outputs	25	8	X	X				
9LS/54LS/74LS27	Triple 3-input NOR gate	10	18	X	X				
9LS/54LS/74LS28	Quad 2-input NOR gate buffer	15	22	X	X				
9LS/54LS/74LS30	Single 8-input NAND gate	13	2	X	X				
9LS/54LS/74LS32	Quad 2-inptu OR gate	11	20	X	X				
9LS/54LS/74LS33	LS28, open collectors	30	22	X	X				
9LS/54LS/74LS37	Quad 2-input NAND gate buffer	15	17	X	X				
9LS/54LS/74LS38	LS37, open collectors	30	17	X	X				
9LS/54LS/74LS40	Dual 4-input NAND gate buffer	15	9	X	X				
9LS/54LS/74LS42	1 of 10 decoder	11 ns	35			X	X		
9LS/54LS/74LS43	Excess 3 to decimal decoder	11 ns	35			X	X		
9LS/54LS/74LS44	Excess gray to decimal decoder	11 ns	35			X	X		
9LS/54LS/74LS51	Dual 2-wide AOI	13	5.5	X	X				

1. Maximum at 25°C
2. Guaranteed minimum at 25°C

9LS/54LS/74LS Low Power Schottky (Cont.)

Type Number	Description	Prop Delay[1] (ns) or Max. Op. Freq. (MHz)[2]	Pwr Diss. (mW)	Available Packages					
				14 Pin		16 Pin		24 Pin	
				J	W	J	W	J	W
9LS/54LS/74LS54	4-wide 2-3-3-2 input AOI	13	4.5	X	X				
9LS/54LS/74LS55	2-wide 4-input AOI	13	2.8	X	X				
9LS/54LS/74LS73	Dual J-K flip-flop, negative edge trigger	35 MHz	20	X	X				
9LS/54LS/74LS74	Dual D-type flip-flop	30 MHz	20	X	X				
9LS/54LS/74LS75	Quad transparent latch	12	32			X	X		
9LS/54LS/74LS76	Dual J-K flip-flop, preset and clear	35 MHz	20			X	X		
9LS/54LS/74LS77	Quad transparent latch	10	33	X	X				
9LS/54LS/74LS78	Dual J-K flip-flop, common clock and clear	35 MHz	20	X	X				
9LS/54LS/74LS83A	4-bit binary full adder	18	96			X	X		
9LS/54LS/74LS85	4-bit magnitude comparator	20	52			X	X		
9LS/54LS/74LS86	Quad 2-input exclusive OR gate	12	30	X	X				
9LS/54LS/74LS90	Decade Counter	32 MHz	45	X	X				
9LS/54LS/74LS91	8-bit shift register	32 MHz	45	X	X				
9LS/54LS/74LS92	Divide by 12 counter	32 MHz	45	X	X				
9LS/54LS/74LS93	4-bit binary counter	32 MHz	45	X	X				
9LS/54LS/74LS95B	4-bit bidirectional shift register	30 MHz	65	X	X				
9LS/54LS/74LS107	Dual J-K flip-flop with clear	35 MHz	20	X	X				
9LS/54LS/74LS109	Dual J-K flip-flop, positive edge trigger	30 MHz	20			X	X		
9LS/54LS/74LS112	Dual J-K flip-flop, preset and clear	35 MHz	20			X	X		
9LS/54LS/74LS113	Dual J-K flip-flop with preset	35 MHz	20	X	X				
9LS/54LS/74LS114	Dual J-K flip-flop, common clock	35 MHz	20	X	X				
9LS/54LS/74LS122	Retriggerable one-shot	25	45	X	X				
9LS/54LS/74LS123	Dual one-shot multivibrator	25	30	X	X				
9LS/54LS/74LS125	Quad buffer with tri-state output	15	15	X	X				
9LS/54LS/74LS126	LS125, inverting	15	22	X	X				
9LS/54LS/74LS132	Quad 2-input Schmitt trigger	20	40	X	X				
9LS/54LS/74LS136	LS86 with open collectors	23	30	X	X				
9LS/54LS/74LS138	3-to-8 line decoder/demultiplexer	23	31			X	X		
9LS/54LS/74LS139	Dual 2-to-4 line decoder/demultiplexer	23	34			X	X		
9LS/54LS/74LS151	8-to-1 line multiplexer, compl. outputs	20	30			X	X		
9LS/54LS/74LS152	8-to-1 line multiplexer	20	34	X	X				
9LS/54LS/74LS153	Dual 4-to-1 line multiplexer	15	31			X	X		
9LS/54LS/74LS155	Dual 2-to-4 line decoder/demultiplexer	40	30			X	X		
9LS/54LS/74LS156	LS155, open collectors	40	31			X	X		
9LS/54LS/74LS157	Quad 2-to-1 line multiplexer	15	49			X	X		
9LS/54LS/74LS158	LS157, inverting	12	24			X	X		
9LS/54LS/74LS160	BCD decade counter, asynchronous clear	30 MHz	93			X	X		
9LS/54LS/74LS161	4-bit binary counter, asynchronous clear	30 MHz	93			X	X		
9LS/54LS/74LS162	BCD decade counter, synchronous clear	30 MHz	93			X	X		
9LS/54LS/74LS163	4-bit binary counter, synchronous clear	30 MHz	93			X	X		
9LS/54LS/74LS164	8-bit shift register	35 MHz	80	X	X				
9LS/54LS/74LS170	4 x 4 register file, open collectors	30	25			X	X		
9LS/54LS/74LS174	Hex D-type flip-flop	40 MHz	80			X	X		
9LS/54LS/74LS175	Quad D-type flip-flop	40 MHz	55			X	X		
9LS/54LS/74LS181	4-bit arithmetic logic unit	40	102					X	X

1. Maximum at 25°C
2. Guaranteed minimum at 25°C

9LS/54LS/74LS Low Power Schottky (Cont.)

Type Number	Description	Prop Delay[1] (ns) or Max. Op. Freq. (MHz)[2]	Pwr Diss. (mW)	Available Packages					
				14 Pin		16 Pin		24 Pin	
				J	W	J	W	J	W
9LS/54LS/74LS190	BCD decade counter, mode control	25 MHz	90			X	X		
9LS/54LS/74LS191	4-bit binary counter, mode control	25 MHz	90			X	X		
9LS/54LS/74LS192	BCD decade counter, up/down	30 MHz	85			X	X		
9LS/54LS/74LS193	4-bit binary counter, up/down	30 MHz	85			X	X		
9LS/54LS/74LS194A	4-bit bidirectional universal shift register	30 MHz	75			X	X		
9LS/54LS/74LS195A	4-bit parallel access shift register	30 MHz	70			X	X		
9LS/54LS/74LS196	4-bit presettable decade counter	35 MHz	60	X	X				
9LS/54LS/74LS197	4-bit presettable binary counter	35 MHz	60	X	X				
9LS/54LS/74LS221	Dual one-shot	40	95*			X	X		
9LS/54LS/74LS251	LS151 with tri-state outputs	25	35			X	X		
9LS/54LS/74LS253	LS153 with tri-state outputs	15	35			X	X		
9LS/54LS/74LS255	LS155 with tri-state outputs	25	35			X	X		
9LS/54LS/74LS257	LS157 with tri-state outputs	18	50			X	X		
9LS/54LS/74LS258	LS158 with tri-state outputs	15	35			X	X		
9LS/54LS/74LS261	2 x 4 parallel binary multiplexer	35	110			X	X		
9LS/54LS/74LS266	Quad 2-input exclusive NOR open collectors	20	40	X	X				
9LS/54LS/74LS279	Quad latch	27	12			X	X		
9LS/54LS/74LS283	4-bit full adder, fast carry	18	96			X	X		
9LS/54LS/74LS295A	LS95B with tri-state outputs	30 MHz	70	X	X				
9LS/54LS/74LS298	Quad 2 multiplexer with output register	16	65			X	X		
9LS/54LS/74LS365	Hex buffer (tri-state, common enable)	15	68			X	X		
9LS/54LS/74LS366	Hex inverter (tri-state, common enable)	15	60			X	X		
9LS/54LS/74LS367	Hex buffer (tri-state, 4 x 2 bit)	15	68			X	X		
9LS/54LS/74LS368	Hex inverter (tri-state, 4 x 2 bit)	15	60			X	X		
9LS/54LS/74LS375	Quad latch (rotated LS75)	12	32			X	X		
9LS/54LS/74LS386	Quad 2-input exclusive OR gate	12	30	X	X				
9LS/54LS/74LS395	4-bit shift register (tri-state)	35 MHz	75			X	X		
9LS/54LS/74LS670	4 x 4 register file (tri-state)	40	150			X	X		

1. Maximum at 25°C 2. Guaranteed minimum at 25°C

Beam Lead Low Power Schottky Devices

Type	Description	Die Size (Mils)	Layout		Mech. Outline Dwg.
			No. of Beams	EIA Std.	
54LS00BL	Quad 2-input NAND gate	45 x 45	16	X	9
54LS03BL	Quad 2-input NAND gate, open collector outputs	45 x 45	16	X	9
54LS04BL	Hex inverter	45 x 45	16	X	9
54LS05BL	Hex inverter, open collector outputs	45 x 45	16	X	9
54LS10BL	Triple 3-input NAND gate	45 x 45	16	X	9
54LS11BL	Triple 3-input AND gate	45 x 45	16	X	9
54LS15BL	Triple 3-input AND gate, open collector outputs	45 x 45	16	X	9
54LS153BL	Dual 4-to-1 line multiplexer	55 x 55	20	X	12
54LS253BL	Dual 4-to-1 line multiplexer, tri-state output	55 x 55	20	X	12

25LS High-Performance Low Power Schottky

Type Number	Description	Prop Delay[1] (ns) or Max. Op. Freq. (MHz)[2]	Pwr. Diss. (mW)	Available Packages					
				14 Pin		16 Pin		20 Pin	
				J	W	J	W	J	W
25LS14	8-bit serial/parallel multiplier	40 MHz	455			X	X		
25LS15	Quad serial adder/subtractor	40 MHz	240					X	X
25LS22	8-bit serial/parallel register	70 MHz	200					X	X
25LS23	8-bit shift/storage register	50 MHz	190					X	X
25LS138	3-to-8 line decoder/demultiplexer	12	31			X	X		
25LS139	Dual 2-to-4 line decoder/demultiplexer	10	34			X	X		
25LS151	8-to-1 line multiplexer, compl. outputs	9	30			X	X		
25LS153	Dual 4-in-1 line multiplexer	10	31			X	X		
25LS157	Quad 2-to-1 line multiplexer	6	40			X	X		
25LS158	LS157, inverting	6	24			X	X		
25LS160	BCD decade counter, async. clear	40 MHz	93			X	X		
25LS161	4-bit binary counter, async. clear	40 MHz	93			X	X		
25LS162	BCD decade counter, sync. clear	40 MHz	93			X	X		
25LS163	4-bit binary counter, sync. clear	40 MHz	93			X	X		
25LS170	4 x 4 register file, open collector	20	125			X	X		
25LS174	Hex D-type flip-flop	50 MHz	80			X	X		
25LS175	Quad D-type flip-flop	50 MHz	55			X	X		
25LS181[3]	4-bit arithmetic logic unit	12	102						
25LS190	BCD decade counter, mode control	35 MHz	90			X	X		
25LS191	4-bit binary counter, mode control	35 MHz	90			X	X		
25LS192	BCD decade counter, up/down	35 MHz	85			X	X		
25LS193	4-bit binary counter, up/down	35 MHz	85			X	X		
25LS194A	4-bit bidirectional-universal shift register	40 MHz	75			X	X		
25LS195A	4-bit parallel access shift register	40 MHz	70			X	X		
25LS251	LS151 with tri-state outputs	9	35			X	X		
25LS253	LS153 with tri-state outputs	9	35			X	X		
25LS257	LS157 with tri-state outputs	7	50			X	X		
25LS258	LS158 with tri-state outputs	7	35			X	X		
25LS299	8-bit shift/storage register	50 MHz	190					X	X
25LS670	LS170 with tri-state outputs	20	150			X	X		

1. Maximum at 25°C
2. Guaranteed minimum at 25°C
3. Available in 24-pin J or W package.

Standard TTL 2's Complement Multipliers

Type Number	Description	Prop Delay[1] (ns)	Pwr Diss. (mW)	Available Packages	
				N	R
2505	4-bit by 2-bit 2's complement multiplier	20	450	X	X
2506	4-bit arithmetic logic unit/function generator with output latch	20	450	X	X

1. Maximum at 25°C

54/74 SSI Series

Type	Description	Prop Delay (ns) or Max. Op. Freq. (MHz)	Pwr [1] Diss. (mW)	Available Packages 14 Pin	
				DC	CJ
54/7400	Quadruple 2-input NAND gate	10	10	X	X
54/7401	Quadruple 2-input NAND gate, open collectors	22	10	X	X
54/7403	Quadruple 2-input NAND gate, open collectors	22	10	X	X
54/7404	Hex inverter	10	10	X	X
54/7405	Hex inverter, open collectors	22	10	X	X
54/7408	Quadruple 2-input AND gate	15	19	X	X
54/7409	Quadruple 2-input AND gate, open collectors	18.5	19.4	X	X
54/7410	Triple 3-input NAND gate	10	10	X	X
54/7411	Triple 3-input AND gate	15	19	X	X
54/7412	Triple 3-input NAND gate, open collectors	22	10	X	X
54/7415	Triple 3-input AND gate, open collectors	18.5	19.4	X	X
54/7420	Dual 4-input NAND gate	10	10	X	X
54/7421	Dual 4-input AND gate	15	19	X	X
54/7422	Dual 4-input NAND gate, open collectors	22	10	X	X
54/7437	Quad 2-input NAND gate	10	10	X	X
54/7438	Quad 2-input NAND gate, open collectors	10	10	X	X
54/7474	Dual D-type flip-flop	25 MHz	43	X	X
54/7486	Quad 2-input exclusive OR gate	14	150	X	X
54/74136	54/7486 with open collectors	27	150	X	X

[1] Power dissipation is given for V_{CC} = 5.0 volts. Propagation delays given are for the average path. Operating temperature range, 5400 Types: -55°C to +125°C; 7400 Types: 0°C to +70°C.

54/74 MSI Series

Type	Description	Prop Delay (ns) or Max. Op. Freq. (MHz)	Pwr[1] Diss (mW)	Available Packages					
				14 Pin		16 Pin		24 Pin	
				DC	CJ	CL	DD	N	R
54/7442	BCD-to-Decimal Decoder	22	140			X	X		
54/7443	Excess 3-to-Decimal Decoder	22	140			X	X		
54/7444	Excess 3 Gray-to-Decimal Decoder	22	140			X	X		
54/7445	BCD-to-Decimal Decoder/Driver (30V Breakdown)	30	215			X	X		
54/7483	4-Bit Binary Full Adder	13	300			X	X		
54/74123	Dual Retriggerable Monostable Multivibrator	21	230			X	X		
54/74145	BCD-to-Decimal r ecoder Driver (15V Breakdown)	30	215			X	X		
54/74150	16-to-1 Line Data Selector/Multiplexer	11	200					X	X
54/74151	8-to-1 Line Data Selector/Multiplexer	11	145			X	X		
54/74152	8-to-1 Line Data Selector/Multiplexer	11	130			X	X		
54/74153	Dual 4-in-1 Line Data Selector/Multiplexer	14	180			X	X		
54/74154	4-to-16 Line Decoder/Demultiplexer	23	170					X	X
54/74155	Dual 2-to-4 Line Decoder/Demultiplexer	21	250			X	X		
54/74156	Dual 2-to-4 Line Decoder/Demultiplexer (Open Coll.)	21	250			X	X		
54/74157	Quad 2-to-1 Line Data Selector/Multiplexer	9	150			X	X		
54/74158	Quad 2-to-1 Line Data Selector/Multiplexer (Inv. Data)	9	150			X	X		
54/74159	4-to-16 Line Decoder/Demultiplexer (Open Coll.)	24	170					X	X
54/74160	BCD Decade Counter, Async. Clear	32 MHz	305			X	X		
54/74161	4-Bit Finary Counter, Async. Clear	32 MHz	305			X	X		
54/74162	BCD Decade Counter, Sync. Clear	32 MHz	305			X	X		
54/74163	4-Bit Binary Counter, Sync. Clear	32 MHz	305			X	X		
54/74164	8-Bit Parallel-Out Serial Shift Register (S.I.P.O.)	36 MHz	167	X	X				
54/74165	Parallel-Load 8-Bit Shift Register (P.I.S.O.)	26 MHz	210			X	X		
54/74166	8-Bit Shift Register with Clear (P.I.S.O.)	35 MHz	360			X	X		
54/74170	4x4 Register File	20	625			X	X		
54/74174	Hex D-Type Flip-Flop	35 MHz	225			X	X		
54/74175	Quad D-Type Flip-Flop	35 MHz	150			X	X		
54/74180	9-Bit Odd/Even Parity Generator/Checker	32	170	X	X				
54/74181	4-Bit Arithmetic Logic Unit	17	440					X	X
54/74182	Look-Ahead Carry Generator	13	180			X	X		
54/74190	BCD Decade Up/Down Counter	25 MHz	325			X	X		
54/74191	4-Bit Binary Up/Down Counter	25 MHz	325			X	X		
54/74192	BCD Decade Up/Down Counter (Dual Clock)	30 MHz	325			X	X		
54/74193	4-Bit Binary Up/Down Counter (Dual Clock)	30 MHz	325			X	X		
54/74194	4-Bit Bidirectional Universal Shift Register	36 MHs	195			X	X		
54/74195	4-Bit Parallel Access Shift Register	39 MHz	195			X	X		
54/74198	8-Bit Right/Left Shift Register (P.I.P.O.)	35 MHz	360					X	X
54/74199	8-Bit Shift Register (P.I.P.O.)	35 MHz	360					X	X
54/74255	54/74155 with 3-State Outputs	21	250			X	X		
54/74283	4-Bit Binary Full Adder with Fast Carry	13	300			X	X		

1. Power dissipation is given for V_{CC} = 5.0 Volts. Propagation delays given are for the average path. Operating temperature range, 5400 Types: -55°C to +125°C; 7400 Types: 0°C to +70°C.

8200 MSI Series

Type	Description	Prop Delay (ns) or Max. Op. Freq. (MHz)	Pwr[1] Diss (mW)	Available Packages									
				14 Pin				16 Pin				24 Pin	
				DP	DC	CJ	DB	CL	DD	MB	MP	N	R
RM/RC8T09	Quad Bus Driver (Tri-State Outputs)	16	235		X	X							
RM/RC8T10	Quad D-Type Bus Flip-Flop (Tri-State Outputs)	50 MHz	250					X	X				
RM/RC8T20	Bidirectional One-Shot	30	250					X	X	X	X		
RM/RC8200	Dual 5-Bit Buffer Register	35 MHz	400									X	X
RM/RC8201	Dual 5-Bit Buffer Register (Inv. Outputs)	35 MHz	400									X	X
RM/RC8202	10-Bit Buffer Register	35 MHz	400									X	X
RM/RC8203	10-Bit Buffer Register (Inv. Outputs)	35 MHz	400									X	X
RM/RC8230	8-Input Multiplexer	11	184					X	X		X		
RM/RC8231	8-Input Multiplexer (Open Coll. f Output)	13	184					X	X		X		
RM/RC8232	8-Input Multiplexer	11	172					X	X		X		
RM/RC8233	2-Input 4-Bit Multiplexer	16	200					X	X		X		
RM/RC8234	2-Input 4-Bit Multiplexer (Open Coll.)	16	160					X	X				
RM/RC8235	2-Input 4-Bit Multiplexer (Open Coll.)	16	230					X	X				
RM/RC8241	Quad Exclusive OR Gate	14	225	X	X	X							
RM/RC8242	4-Bit Comparator (Open Coll.)	14	170		X	X							
RM/RC8243	8-Bit Position Scaler	25	315									X	X
RM/RC8250	Binary-to-Octal Decoder	20	125		X	X							
RM/RC8251	BCD to Decimal Decoder	20	135					X	X		X		
RM/RC8252	(9301) BCD to Decimal Decoder	20	135					X					
RM/RC8260	Arithmetic Logic Element	14	400									X	X
RM/RC8261	Fast Carry Extender	13	115	X	X	X							
RM/RC8262	9-Bit Parity Generator/Checker	30	300		X	X							
RM/RC8263	3-Input 4-Bit Multiplexer	17	378									X	X
RM/RC8264	3-Input 4-Bit Multiplexer (Open Coll.)	25	400									X	X
RM/RC8266	2-Input 4-Bit Multiplexer	14	200					X	X				
RM/RC8267	2-Input 4-Bit Multiplexer (Open Coll.)	17	200					X	X	X			
RM/RC8270	4-Bit Shift Register	23 MHz	168	X	X	X							
RM/RC8271	4-Bit Shift Register	22 MHz	270					X	X	X	X		
RM/RC8273	10-Bit Serial-In, Parallel-Out Shift Register	35 MHz	340					X	X	X	X		
RM/RC8274	10-Bit Parallel-In, Serial-Out Shift Register	25 MHz	380					X	X	X	X		
RM/RC8277	Dual 8-Bit Shift Register	20 MHz	400					X	X	X	X		
RM/RC8280	Decade Counter	25 MHz	185	X	X	X	X						
RM/RC8281	4-Bit Binary Counter	25 MHz	185	X	X	X	X						
RM/RC8284	Binary Hex Synchronous Up/Down Counter	30 MHz	315		X	X							
RM/RC8285	BCD Decade Synchronous Up/Down Counter	30 MHz	315	X	X	X							
RM/RC8290	Presettable High Speed Decade Counter	60 MHz	190	X	X	X	X						
RM/RC8291	Presettable High Speed Binary Counter	60 MHz	190	X	X	X	X						

[1] Power dissipation is given for V_{CC} = 5.0 volts; propagation delays are given for the average path. Operating temperature range, RM Types: -55°C to +125°C; RC Types: 0°C to +70°C.

930 Series DTL

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	Avg. Pwr. Function (mW) 50% Duty	DC Noise Margin (V)	Available Packages 14 Pin: CJ		D	DB	DC	DP	J		
RM/RC930	Dual 4 NAND/NOR gate with nodes[3]	8	30	8.5/gate	0.5	X		X		X	X	X		
RM/RC932	Dual 4 NAND/NOR buffer	22	40	28/gate	0.5	X		X		X	X	X		
RM/RC933	Dual four expander	NA	NA	NA	NA	X		X		X	X	X		
RM/RC934	Hex Inverter[3]	8	30	8.5/gate	0.5	X		X		X	X	X		
RM/RC935	Hex Inverter[3]	8	30	7/gate	0.5	X		X		X		X		
RM/RC936	Hex Inverter[2]	8	30	8.5/gate	0.5	X		X		X		X		
RM/RC937	Hex Inverter[4]	8	30	8.5/gate	0.5	X		X	X	X		X		
RM/RC940	Hex Inverter	8	30	8.5/gate	0.5	X		X		X		X		
RM/RC941	Hex Inverter	8	30	8.5/gate	0.5	X		X		X		X		
RM/RC944	Dual 4 NAND/NOR power gate	25	27	22/gate	0.5	X		X		X		X		
RM/RC945	Clocked Flip-Flop[3]	9	52	35	0.5	X		X		X		X		
RM/RC946	Quad two NAND/NOR gate[3]	8	30	8.5/gate	0.5	X		X	X	X	X	X		
RM/RC948	Clocked Flip-Flop[4]	9	50	40	0.5	X		X		X		X		
RM/RC949	Quad two NAND/NOR gate[4]	7	25	8.5/gate	0.5	X		X		X		X		
RM/RC950	Pulse triggered binary flip-flop	8	30	22	0.5	X		X		X	X	X		
RM/RC951	Monostable multivibrator	9	50	35	–	X		X		X	X	X		
RM/RC957	Quad 2 input buffers	22	40	28/gate	0.5	X		X		X		X		
RM/RC958	Quad 2 NAND power gates	25	27	22/gate	0.5	X		X		X		X		
RM/RC961	Dual 4 NAND/NOR gate with nodes[4]	7	25	8.5/gate	0.5	X		X		X		X		
RM/RC962	Triple three NAND/NOR gate[3]	8	30	8.5/gate	0.5	X		X		X	X	X		
RM/RC963	Triple three NAND/NOR gate[4]	7	25	8.5/gate	0.5	X		X		X	X	X		
RM/RC988	Monostable multivibrator	10	–	–	1.0	X		X		X		X		
RM/RC993	Dual RM945[3] } separate clock, separate	9	52	70	0.5	X		X		X		X		
RM/RC994	Dual RM948[4] } direct set, no direct clear	9	50	80	0.5	X		X		X		X		
RM/RC997	Dual RM948[4] } common clock, common	9	50	80	0.5	X		X		X		X		
RM/RC999	Dual RM945[3] } direct clear, direct set	9	52	70	0.5	X		X		X		X		

NOTES

1. Operating temperature range; RM types: -55°C to +125°C; RC types: 0°C to +75°C
2. Without collector pull-up resistor, Rc
3. 6KΩ pull-up resistor
4. 2KΩ pull-up resistor

RAY I and II Series TTL

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	Avg. Pwr. Function (mW) 50% Duty	DC Noise Margin (V)	Available Packages: 14 Pin CJ	CK	D	DC
RF30	Single phase SRT flip-flop	15	15 MHz	30	+1.1, -1.5	X	X	X	X
RF31	Single phase SRT flip-flop	7	15 MHz	30	+1.1, -1.5	X	X	X	X
RF32	J-K flip-flop (AND inputs)	12	15 MHz	30	+1.1, -1.5	X	X	X	X
RF33	J-K flip-flop (AND inputs)	6	15 MHz	30	+1.1, -1.5	X	X	X	X
RF50	J-K flip-flop (AND inputs)	15	20 MHz	50	+1.1, -1.5	X	X	X	X
RF51	J-K flip-flop (AND inputs)	7	20 MHz	50	+1.1, -1.5	X	X	X	X
RF52	F-K flip-flop (AND inputs)	12	20 MHz	50	+1.1, -1.5	X	X	X	X
RF53	J-K flip-flop (AND inputs)	6	20 MHz	50	+1.1, -1.5	X	X	X	X
RF60	J-K flip-flop (OR inputs)	15	20 MHz	55	+1.1, -1.5	X	X	X	X
RF61	J-K flip-flop (OR inputs)	7	20 MHz	55	+1.1, -1.5	X	X	X	X
RF62	J-K flip-flop (OR inputs)	12	20 MHz	55	+1.1, -1.5	X	X	X	X
RF63	J-K flip-flop (OR inputs)	6	20 MHz	55	+1.1, -1.5	X	X	X	X
RF100	Dual J-K flip-flop (separate clocks)	11	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF101	Dual J-K flip-flop (separate clocks)	6	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF102	Dual J-K flip-flop (separate clocks)	9	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF103	Dual J-K flip-flop (separate clocks)	5	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF110	Dual J-K flip-flop (common clock)	11	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF111	Dual J-K flip-flop (common clock)	6	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF112	Dual J-K flip-flop (common clock)	9	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF113	Dual J-K flip-flop (common clock)	5	35 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF120	Dual J-K flip-flop (separate clocks)	11	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF121	Dual J-K flip-flop (separate clocks)	6	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF122	Dual J-K flip-flop (separate clocks)	9	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF123	Dual J-K flip-flop (separate clocks)	5	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF130	Dual J-K flip-flop (common clock)	11	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF131	Dual J-K flip-flop (common clock)	6	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF132	Dual J-K flip-flop (common clock)	9	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF133	Dual J-K flip-flop (common clock)	5	50 MHz	55/flip-flop	+1.0, -1.5	X	X	X	X
RF200	J-K flip-flop (AND inputs)	11	50 MHz	55	+1.0, -1.5	X	X	X	X
RF201	J-K flip-flop (AND inputs)	6	50 MHz	55	+1.0, -1.5	X	X	X	X
RF202	J-K flip-flop (AND inputs)	9	50 MHz	55	+1.0, -1.5	X	X	X	X
RF203	J-K flip-flop (AND inputs)	5	50 MHz	55	+1.0, -1.5	X	X	X	X
RF210	J-K flip-flop (OR inputs)	11	50 MHz	55	+1.0, -1.5	X	X	X	X
RF211	J-K flip-flop (OR inputs)	6	50 MHz	55	+1.0, -1.5	X	X	X	X
RF212	J-K flip-flop (OR inputs)	9	50 MHz	55	+1.0, -1.5	X	X	X	X
RF213	J-K flip-flop (OR inputs)	5	50 MHz	55	+1.0, -1.5	X	X	X	X
RF250	J-K flip-flop (AND inputs)	11	30 MHz	50	+1.1, -1.5	X	X	X	X
RF251	J-K flip-flop (AND inputs)	6	30 MHz	50	+1.1, -1.5	X	X	X	X
RF252	J-K flip-flop (AND inputs)	9	30 MHz	50	+1.1, -1.5	X	X	X	X
RF253	J-K flip-flop (AND inputs)	5	30 MHz	50	+1.1, -1.5	X	X	X	X
RF260	J-K flip-flop (OR inputs)	11	30 MHz	55	+1.1, -1.5	X	X	X	X
RF261	J-K flip-flop (OR inputs)	6	30 MHz	55	+1.1, -1.5	X	X	X	X
RF262	J-K flip-flop (OR inputs)	9	30 MHz	55	+1.1, -1.5	X	X	X	X
RF263	J-K flip-flop (OR inputs)	5	30 MHz	55	+1.1, -1.5	X	X	X	X

1. Operating temperature range, final digits 0 or 1: –55°C to +125°C; final digits 2 or 3: 0°C to +70°C.

RAY I and II Series TTL (Cont.)

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	TYPICAL CHARACTERISTICS: Avg. Pwr. Function (mW) 50% Duty	TYPICAL CHARACTERISTICS: DC Noise Margin (V)	Available Packages: 14 Pin CJ	CK	D	DC
RF9601	Retriggerable monostable multivibrator (−55°C to +125°C)	10 mA	25	100	+1.0, −1.5	X	X	X	X
RF9602	Retriggerable monostable multivibrator (0°C to +75°C)	12.8 mA	25	100	+1.0, −1.5				
RG40	Dual 4 input NAND gate	15	10	15/gate	+1.1, −1.5	X	X	X	X
RG41	Dual 4 input NAND gate	7	10	15/gate	+1.1, −1.5	X	X	X	X
RG42	Dual 4 input NAND gate	12	10	15/gate	+1.1, −1.5	X	X	X	X
RG43	Dual 4 input NAND gate	6	10	15/gate	+1.1, −1.5	X	X	X	X
RG50	Exp. 4-wide, 2-2-2-3 input AOI gate	15	12	30	+1.1, −1.5	X	X	X	X
RG51	Exp. 4-wide, 2-2-2-3 input AOI gate	7	12	30	+1.1, −1.5	X	X	X	X
RG52	Exp. 4-wide, 2-2-2-3 input AOI gate	12	12	30	+1.1, −1.5	X	X	X	X
RG53	Exp. 4-wide, 2-2-2-3 input AOI gate	6	12	30	+1.1, −1.5	X	X	X	X
RG60	Single 8 input NAND gate	15	12	15	+1.1, −1.5	X	X	X	X
RG61	Single 8 input NAND gate	7	12	15	+1.1, −1.5	X	X	X	X
RG62	Single 8 input NAND gate	12	12	15	+1.1, −1.5	X	X	X	X
RG63	Single 8 input NAND gate	6	12	15	+1.1, −1.5	X	X	X	X
RG70	Dual 2-wide, 2 input AOI gate, one side exp.	15	12	20/gate	+1.1, −1.5	X	X	X	X
RG71	Dual 2-wide, 2 input AOI gate, one side exp.	7	12	20/gate	+1.1, −1.5	X	X	X	X
RG72	Dual 2-wide, 2 input AOI gate, one side exp.	12	12	20/gate	+1.1, −1.5	X	X	X	X
RG73	Dual 2-wide, 2 input AOI gate, one side exp.	6	12	20/gate	+1.1, −1.5	X	X	X	X
RG80	Dual pulse shaper/delay AND gate	15	11	30/gate	+1.1, −1.5	X	X	X	X
RG81	Dual pulse shaper/delay AND gate	7	11	30/gate	+1.1, −1.5	X	X	X	X
RG82	Dual pulse shaper/delay AND gate	12	11	30/gate	+1.1, −1.5	X	X	X	X
RG83	Dual pulse shaper/delay AND gate	6	11	30/gate	+1.1, −1.5	X	X	X	X
RG90	Exclusive OR gate with complement	15	11	35	+1.1, −1.5	X	X	X	X
RG91	Exclusive OR gate with complement	7	11	35	+1.1, −1.5	X	X	X	X
RG92	Exclusive OR gate with complement	12	11	35	+1.1, −1.5	X	X	X	X
RG93	Exclusive OR gate with complement	6	11	35	+1.1, −1.5	X	X	X	X
RG100	Exp. 3-wide, 3 input AOI gate	15	12	25	+1.1, −1.5	X	X	X	X
RG101	Exp. 3-wide, 3 input AOI gate	7	12	25	+1.1, −1.5	X	X	X	X
RG102	Exp. 3-wide, 3 input AOI gate	12	12	25	+1.1, −1.5	X	X	X	X
RG103	Exp. 3-wide, 3 input AOI gate	6	12	25	+1.1, −1.5	X	X	X	X
RG110	Exp. 2-wide, 4 input AOI gate	15	12	20	+1.1, −1.5	X	X	X	X
RG111	Exp. 2-wide, 4 input AOI gate	7	12	20	+1.1, −1.5	X	X	X	X
RG112	Exp. 2-wide, 4 input AOI gate	12	12	20	+1.1, −1.5	X	X	X	X
RG113	Exp. 2-wide, 4 input AOI gate	6	12	20	+1.1, −1.5	X	X	X	X
RG120	Expandable single 8 NAND gate	15	18	15/gate	+1.1, −1.5	X	X	X	X
RG121	Expandable single 8 NAND gate	7	18	15/gate	+1.1, −1.5	X	X	X	X
RG122	Expandable single 8 NAND gate	12	18	15/gate	+1.1, −1.5	X	X	X	X
RG123	Expandable single 8 NAND gate	6	18	15/gate	+1.1, −1.5	X	X	X	X
RG130	Dual 4-input line driver	30	15	30/gate	+1.1, −1.5	X	X	X	X
RG131	Dual 4 input line driver	30	15	30/gate	+1.1, −1.5	X	X	X	X
RG132	Dual 4 input line driver	24	15	30/gate	+1.1, −1.5	X	X	X	X
RG133	Dual 4 input line driver	12	15	30/gate	+1.1, −1.5	X	X	X	X

1. Operating temperature range, final digits 0 or 1: −55°C to +125°C; final digits 2 or 3: 0°C to +70°C.

RAY I and II Series TTL (Cont.)

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	TYPICAL CHARACTERISTICS: Avg. Pwr. Function (mW) 50% Duty	TYPICAL CHARACTERISTICS: DC Noise Margin (V)	Available Packages: 14 Pin: CJ	CK	D	DC
RG140	Quad 2 input NAND gate	15	10	15/gate	+1.1, -1.5	X	X	X	X
RG141	Quad 2 input NAND gate	7	10	15/gate	+1.1, -1.5	X	X	X	X
RG142	Quad 2 input NAND gate	12	10	15/gate	+1.1, -1.5	X	X	X	X
RG143	Quad 2 input NAND gate	6	10	15/gate	+1.1, -1.5	X	X	X	X
RG150	4-wide, 2-2-2-3 input AOI expander	–	4	5/gate	+1.1, -1.5	X	X	X	X
RG151	4-wide, 2-2-2-3 input AOI expander	–	4	5/gate	+1.1, -1.5	X	X	X	X
RG152	4-wide, 2-2-2-3 input AOI expander	–	4	5/gate	+1.1, -1.5	X	X	X	X
RG153	4-wide, 2-2-2-3 input AOI expander	–	4	5/gate	+1.1, -1.5	X	X	X	X
RG160	Triple 2 input buss driver	22	15	15/gate	+1.1, -1.5	X	X	X	X
RG161	Triple 2 input buss driver	11	15	15/gate	+1.1, -1.5	X	X	X	X
RG162	Triple 2 input buss driver	18	15	15/gate	+1.1, -1.5	X	X	X	X
RG163	Triple 2 input buss driver	9	15	15/gate	+1.1, -1.5	X	X	X	X
RG170	2-wide, 4 input AOI expander	–	1	5/gate	+1.1, -1.5	X	X	X	X
RG171	2-wide, 4 input AOI expander	–	1	5/gate	+1.1, -1.5	X	X	X	X
RG172	2-wide, 4 input AOI expander	–	1	5/gate	+1.1, -1.5	X	X	X	X
RG173	2-wide, 4 input AOI expander	–	1	5/gate	+1.1, -1.5	X	X	X	X
RG180	Dual 4 input NAND expander	–	1	1	+1.1, -1.5	X	X	X	X
RG181	Dual 4 input NAND expander	–	1	1	+1.1, -1.5	X	X	X	X
RG182	Dual 4 input NAND expander	–	1	1	+1.1, -1.5	X	X	X	X
RG183	Dual 4 input NAND expander	–	1	1	+1.1, -1.5	X	X	X	X
RG200	Expandable single 8 NAND gate	11	8	22/gate	+1.0, -1.5	X	X	X	X
RG201	Expandable single 8 NAND gate	6	8	22/gate	+1.0, -1.5	X	X	X	X
RG202	Expandable single 8 NAND gate	9	8	22/gate	+1.0, -1.5	X	X	X	X
RG203	Expandable single 8 NAND gate	5	8	22/gate	+1.0, -1.5	X	X	X	X
RG210	Expandable 2-wide, 4 input AOI gate	11	7	30	+1.0, -1.5	X	X	X	X
RG211	Expandable 2-wide, 4 input AOI gate	6	7	30	+1.0, -1.5	X	X	X	X
RG212	Expandable 2-wide, 4 input AOI gate	9	7	30	+1.0, -1.5	X	X	X	X
RG213	Expandable 2-wide, 4 input AOI gate	5	7	30	+1.0, -1.5	X	X	X	X
RG220	Quad 2 input NAND gate	11	8	22/gate	+1.0, -1.5	X	X	X	X
RG221	Quad 2 input NAND gate	6	6	22/gate	+1.0, -1.5	X	X	X	X
RG222	Quad 2 input NAND gate	9	6	22/gate	+1.0, -1.5	X	X	X	X
RG223	Quad 2 input NAND gate	5	6	22/gate	+1.0, -1.5	X	X	X	X
RG230	4-wide, 2-2-2-3 input AOI expander	–	2	7/gate	+1.0, -1.5	X	X	X	X
RG231	4-wide, 2-2-2-3 input AOI expander	–	2	7/gate	+1.0, -1.5	X	X	X	X
RG232	4-wide, 2-2-2-3 input AOI expander	–	2	7/gate	+1.0, -1.5	X	X	X	X
RG233	4-wide, 2-2-2-3 input AOI expander	–	2	7/gate	+1.0, -1.5	X	X	X	X
RG240	Dual 4 input NAND gate	11	6	22/gate	+1.0, -1.5	X	X	X	X
RG241	Dual 4 input NAND gate	6	6	22/gate	+1.0, -1.5	X	X	X	X
RG242	Dual 4 input NAND gate	9	6	22/gate	+1.0, -1.5	X	X	X	X
RG243	Dual 4 input NAND gate	5	6	22/gate	+1.0, -1.5	X	X	X	X
RG250	Expandable 4-wide, 2-2-2-3 input AOI gate	11	8	40	+1.0, -1.5	X	X	X	X
RG251	Expandable 4-wide, 2-2-2-3 input AOI gate	6	8	40	+1.0, -1.5	X	X	X	X
RG252	Expandable 4-wide, 2-2-2-3 input AOI gate	9	8	40	+1.0, -1.5	X	X	X	X
RG253	Expandable 4-wide, 2-2-2-3 input AOI gate	5	8	40	+1.0, -1.5	X	X	X	X

1. Operating temperature range, final digits 0 or 1: -55°C to +125°C; final digits 2 or 3: 0°C to +70°C.

RAY I and II Series TTL (Cont.)

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	Avg. Pwr. Function (mW) 50% Duty	DC Noise Margin (V)	Available Packages: 14 Pin CJ	CK	D	DC
RG260	Single 8 input NAND gate	11	8	22	+1.0, -1.5	X	X	X	X
RG261	Single 8 input NAND gate	6	8	22	+1.0, -1.5	X	X	X	X
RG262	Single 8 input NAND gate	9	8	22	+1.0, -1.5	X	X	X	X
RG263	Single 8 input NAND gate	5	8	22	+1.0, -1.5	X	X	X	X
RG270	2-wide, 4 input AOI expander	–	1	7/gate	+1.0, -1.5	X	X	X	X
RG271	2-wide, 4 input AOI expander	–	1	7/gate	+1.0, -1.5	X	X	X	X
RG272	2-wide, 4 input AOI expander	–	1	7/gate	+1.0, -1.5	X	X	X	X
RG273	2-wide, 4 input AOI expander	–	1	7/gate	+1.0, -1.5	X	X	X	X
RG280	Expandable dual 4 input AND gate	15	11	38/gate	+1.1, -1.5	X	X	X	X
RG281	Expandable dual 4 input AND gate	7	11	38/gate	+1.1, -1.5	X	X	X	X
RG282	Expandable dual 4 input AND gate	12	11	38/gate	+1.1, -1.5	X	X	X	X
RG283	Expandable dual 4 input AND gate	6	11	38/gate	+1.1, -1.5	X	X	X	X
RG290	Dual 2 and 3 input AND/OR gate exp.	–	7	15/gate	+1.1, -1.5	X	X	X	X
RG291	Dual 2 and 3 input AND/OR gate exp.	–	7	15/gate	+1.1, -1.5	X	X	X	X
RG292	Dual 2 and 3 input AND/OR gate exp.	–	7	15/gate	+1.1, -1.5	X	X	X	X
RG293	Dual 2 and 3 input AND/OR gate exp.	–	7	15/gate	+1.1, -1.5	X	X	X	X
RG300	Expandable 3-wide, 3 input AOI gate	11	7	35	+1.0, -1.5	X	X	X	X
RG301	Expandable 3-wide, 3 input AOI gate	6	7	35	+1.0, -1.5	X	X	X	X
RG302	Expandable 3-wide, 3 input AOI gate	9	7	35	+1.0, -1.5	X	X	X	X
RG303	Expandable 3-wide, 3 input AOI gate	5	7	35	+1.0, -1.5	X	X	X	X
RG310	Dual 2-wide, 2 input AOI gate, one side exp.	11	7	30/gate	+1.0, -1.5	X	X	X	X
RG311	Dual 2-wide, 2 input AOI gate, one side exp.	6	7	30/gate	+1.0, -1.5	X	X	X	X
RG312	Dual 2-wide, 2 input AOI gate, one side exp.	9	7	30/gate	+1.0, -1.5	X	X	X	X
RG313	Dual 2-wide, 2 input AOI gate, one side exp.	5	7	30/gate	+1.0, -1.5	X	X	X	X
RG320	Triple 3 input NAND gate	11	6	22/gate	+1.0, -1.5	X	X	X	X
RG321	Triple 3 input NAND gate	6	6	22/gate	+1.0, -1.5	X	X	X	X
RG322	Triple 3 input NAND gate	9	6	22/gate	+1.0, -1.5	X	X	X	X
RG323	Triple 3 input NAND gate	5	6	22/gate	+1.0, -1.5	X	X	X	X
RG370	Hex inverter	15	10	15/inverter	+1.1, -1.5	X	X	X	X
RG371	Hex inverter	7	10	15/inverter	+1.1, -1.5	X	X	X	X
RG372	Hex inverter	12	10	15/inverter	+1.1, -1.5	X	X	X	X
RG373	Hex inverter	6	10	15/inverter	+1.1, -1.5	X	X	X	X
RG380	Hex inverter	11	6	22/inverter	+1.0, -1.5	X	X	X	X
RG381	Hex inverter	6	6	22/inverter	+1.0, -1.5	X	X	X	X
RG382	Hex inverter	9	6	22/inverter	+1.0, -1.5	X	X	X	X
RG383	Hex inverter	5	6	22/inverter	+1.0, -1.5	X	X	X	X
RG7510	Quad 2 input line driver	30	15	30/gate	+1.1, -1.5	X	X	X	X
RG7511	Quad 2 input line driver	15	15	30/gate	+1.1, -1.5	X	X	X	X
RG7512	Quad 2 input line driver	24	15	30/gate	+1.1, -1.5	X	X	X	X
RG7513	Quad 2 input line driver	12	15	30/gate	+1.1, -1.5	X	X	X	X
RG7520	Quad 2 input lamp driver	40 mA	15	30/gate	+1.1, -1.5	X	X	X	X
RG7521	Quad 2 input lamp driver	20 mA	15	30/gate	+1.1, -1.5	X	X	X	X
RG7522	Quad 2 input lamp driver	40 mA	15	30/gate	+1.1, -1.5	X	X	X	X
RG7523	Quad 2 input lamp driver	20 mA	15	30/gate	+1.1, -1.5	X	X	X	X

1. Operating temperature range, final digits 0 or 1: -55°C to +125°C; final digits 2 or 3: 0°C to +70°C

RAY I and II Series TTL (Cont.)

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	Avg. Pwr. Function (mW) 50% Duty	DC Noise Margin (V)	Available Packages: 14 Pin CJ	CK	D	DC
RL10	Fast full adder	10	Pin	90 mW	+0.6, -1.4	X	X	X	X
RL11	Fast full adder	10	5 24 ns	90 mW	+0.6, -1.4	X	X	X	X
RL12	Fast full adder	10	6 12 ns	90 mW	+0.6, -1.3	X	X	X	X
RL13	Fast full adder	10	7 13 ns	90 mW	+0.6, -1.3	X	X	X	X
RL20	Dependent carry fast adder	10	Pin	125 mW	+0.6, -1.4	X	X	X	X
RL21	Dependent carry fast adder	10	5 25 ns	125 mW	+0.6, -1.4	X	X	X	X
RL22	Dependent carry fast adder	10	6 22 ns	125 mW	+0.6, -1.3	X	X	X	X
RL23	Dependent carry fast adder	10	7 13 ns	125 mW	+0.6, -1.3	X	X	X	X
RL30	Dependent carry fast adder	10	Pin	125 mW	+0.6, -1.4	X	X	X	X
RL31	Dependent carry fast adder	10	5 25 ns	125 mW	+0.6, -1.4	X	X	X	X
RL32	Dependent carry fast adder	10	6 22 ns	125 mW	+0.6, -1.3	X	X	X	X
RL33	Dependent carry fast adder	10	7 13 ns	125 mW	+0.6, -1.3	X	X	X	X
					Expander				
RL40	Carry decoder	10	See note 2	20 mW	+0.7, -2.35	X	X	X	X
RL41	Carry decoder	10		20 mW	+0.7, -2.35				
RL42	Carry decoder	10		20 mW	+0.7, -2.25	X	X	X	X
RL43	Carry decoder	10		20 mW	+0.7, -2.25	X	X	X	X
RL60	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL61	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL62	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL63	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL70	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL71	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL72	4-bit storage register	11	25 ns	175 mW	+1.1, -1.5	X	X	X	X
RL73	4-bit storage register	11	25 ns	175 MW	+1.1, -1.5	X	X	X	X
RL80	16-bit scratch pad memory	6	27 ns	250 mW	+1.1, -1.5	X	X	X	X
RL81	16-bit scratch pad memory	6	27 ns	250 mW	+1.1, -1.5	X	X	X	X
RL82	16-bit scratch pad memory	6	27 ns	250 mW	+1.1, -1.5	X	X	X	X
RL83	16-bit scratch pad memory	6	27 ns	250 mW	+1.1, -1.5	X	X	X	X

1. Operating temperature range, final digits 0 or 1: -55°C to +125°C; final digits 2 or 3: 0°C to +70°C.
2. Pin 5, $\Delta \leqslant$ 4.0 nS (add 1 Δ/1 pfd)

RAY III Series TTL

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	Avg. Pwr. Function (mW) 50% Duty	DC Noise Margin (V)	Available Packages: Pins 14: CJ	CK	D	DC	Pins 24: R
RF3120	Dual J-K flip-flop (separate clocks)	11	75 MHz	55/FF	+1.1, -1.5	X	X	X		
RF3122	Dual J-K flip-flop (separate clocks)	10	75 MHz	55/FF	+1.1, -1.5	X	X	X		
RF3130	Dual J-K flip-flop (common clock)	11	75 MHz	55/FF	+1.1, -1.5	X	X	X		
RF3132	Dual J-K flip-flop (common clock)	10	75 MHz	55/FF	+1.1, -1.5	X	X	X		
RF3200	AND input J-K flip-flop	11	75 MHz	55	+1.1, -1.5	X	X	X		
RF3202	AND input J-K flip-flop	10	75 MHz	55	+1.1, -1.5	X	X	X		
RF3210	OR input J-K flip-flop	11	75 MHz	55	+1.1, -1.5	X	X	X		
RF3212	OR input J-K flip-flop	10	75 MHz	55	+1.1, -1.5	X	X	X		
RF3220	Triple latch flip-flop (sep. neg. edge clocks)	11	50 MHz	60/FF	+1.1, -1.5	X	X	X		
RF3222	Triple latch flip-flop (sep. neg. edge clocks)	10	50 MHz	60/FF	+1.1, -1.5	X	X	X		
RF3230	Dual D-type flip-flop	11	60 MHz	75/FF	+1.1, -1.5	X	X	X		
RF3232	Dual D-type flip-flop	10	60 MHz	75/FF	+1.1, -1.5	X	X	X		
RF3240	Triple latch flip-flop (com. pos. edge clock)	11	50 MHz	70/FF	+1.1, -1.5	X	X	X		
RF3242	Triple latch flip-flop (com. pos. edge clock)	10	50 MHz	70/FF	+1.1, -1.5	X	X	X		
RF3250	5-channel selector flip-flop	11	50 MHz	150	+1.1, -1.5	X	X	X		
RF3252	5-channel selector flip-flop	10	50 MHz	150	+1.1, -1.5	X	X	X		
RG3180	Dual 4 input NAND gate expander	–	1	–	+1.1, -1.5	X	X	X		
RG3182	Dual 4 input NAND gate expander	–	1	–	+1.1, -1.5	X	X	X		
RG3200	Expandable single 8 NAND gate	11	6.5	22	+1.1, -1.5	X	X	X		
RG3202	Expandable single 8 NAND gate	10	6.5	22	+1.1, -1.5	X	X	X		
RG3210	Expandable 2-wide, 4 input AOI gate	11	5.5	30	+1.1, -1.5	X	X	X		
RG3212	Expandable 2-wide, 4 input AOI gate	10	5.5	20	+1.1, -1.5	X	X	X		
RG3220	Quad 2 input NAND gate	11	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3222	Quad 2 input NAND gate	10	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3230	4-wide, 2-2-3-3 input AOI expander	–	2	7/gate	+1.1, -1.5	X	X	X		
RG3232	4-wide, 2-2-3-3 input AOI expander	–	2	7/gate	+1.1, -1.5	X	X	X		
RG3240	Dual 4 input NAND gate	11	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3242	Dual 4 input NAND gate	10	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3250	Expandable 4-wide, 2-2-2-3 input AOI gate	11	6.0	40	+1.1, -1.5	X	X	X		
RG3252	Expandable 4-wide, 2-2-2-3 input AOI gate	10	6.0	40	+1.1, -1.5	X	X	X		
RG3260	Single 8 input NAND gate	11	5.5	22	+1.1, -1.5	X	X	X		
RG3262	Single 8 input NAND gate	10	5.5	22	+1.1, -1.5	X	X	X		
RG3270	2-wide, 4 input AOI expander	–	1	7/gate	+1.1, -1.5	X	X	X		
RG3272	2-wide, 4-input AOI expander	–	1	7/gate	+1.1, -1.5	X	X	X		
RG3300	Expandable 3-wide, 3 input AOI gate	11	6.0	35	+1.1, -1.5	X	X	X		
RG3302	Expandable 3-wide, 3 input AOI gate	10	6.0	35	+1.1, -1.5	X	X	X		
RG3310	Dual 2-wide, 2 input AOI gate, one side exp.	11	5.5	30/gate	+1.1, -1.5	X	X	X		
RG3312	Dual 2-wide, 2 input AOI gate, one side exp.	10	5.5	30/gate	+1.1, -1.5	X	X	X		
RG3320	Triple 3 input NAND gate	11	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3322	Triple 3 input NAND gate	10	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3380	Hex inverter	11	4.5	22/inverter	+1.1, -1.5	X	X	X		
RG3382	Hex inverter	10	4.5	22/inverter	+1.1, -1.5	X	X	X		
RG3390	Dual 4 input AND gate, split outputs	11	6.5	30/gate	+1.1, -1.5	X	X	X		
RG3392	Dual 4 input AND gate, split outputs	10	6.5	20/gate	+1.1, -1.5	X	X	X		

[1] Operating temperature range, final digit 0: -55°C to +125°C; final digit 2: 0°C to +70°C.

RAYTHEON

RAY III Series TTL (Cont.)

Type[1] Number	Description	Fanout Function	TYPICAL CHARACTERISTICS: Tpd (ns) or Toggle Rate (Min)	TYPICAL CHARACTERISTICS: Avg. Pwr. Function (mW) 50% Duty	TYPICAL CHARACTERISTICS: DC Noise Margin (V)	Available Packages: Pins 14: CJ	CK	D	DC	Pins 24: R
RG3400	Quad 2 input AND gate	11	6.5	30/gate	+1.1, -1.5	X	X	X		
RG3402	Quad 2 input AND gate	10	6.5	30/gate	+1.1, -1.5	X	X	X		
RG3410	Quad 2 input NOR gate	11	4.5	30/gate	+1.1, -1.5	X	X	X		
RG3412	Quad 2 input NOR gate	10	4.5	30/gate	+1.1, -1.5	X	X	X		
RG3420	Dual 4 input NAND gate, split outputs	11	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3422	Dual 4 input NAND gate, split outputs	10	4.5	22/gate	+1.1, -1.5	X	X	X		
RG3430	Single 8 input NAND gate, split outputs	11	5.5	22	+1.1, -1.5	X	X	X		
RG3432	Single 8 input NAND gate, split outputs	10	5.5	22	+1.1, -1.5	X	X	X		
RG3440	Dual 2-wide, 2 input AOI gate, split outputs	11	5.5	30/gate	+1.1, -1.5	X	X	X		
RG3442	Dual 2-wide, 2 input AOI gate, split outputs	10	5.5	30/gate	+1.1, -1.5	X	X	X		
RG3450	4-wide, 2-2-3-4 input AOI gate	11	5.5	40	+1.1, -1.5	X	X	X		
RG3452	4-wide, 2-2-3-4 input AOI gate	10	5.5	40	+1.1, -1.5	X	X	X		
RL3002	10-bit parity generator/checker	14	25 ns	325 mW	+1.1, -1.7				X	
RL3100	4-bit full adder	10	15 ns	350	+1.4, -1.7					X
RL3102	4-bit full adder	10	15 ns	350	+1.4, -1.7					X

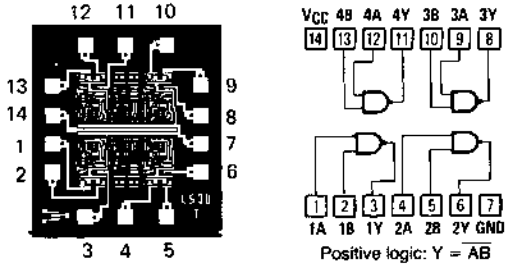
[1] Operating temperature range, final digit 0: -55°C to +125°C; final digit 2: 0°C to +70°C.

SECTION 2
9LS/54LS/74LS
Low-Power Schottky

CONTENTS PAGE

PIN-OUT AND LOGIC DIAGRAMS

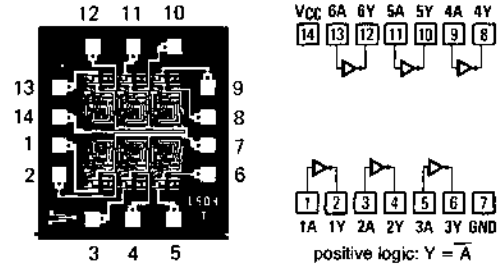
LS00
QUADRUPLE 2-INPUT NAND GATE



Positive logic: $Y = \overline{AB}$

Die Size .060 x .067

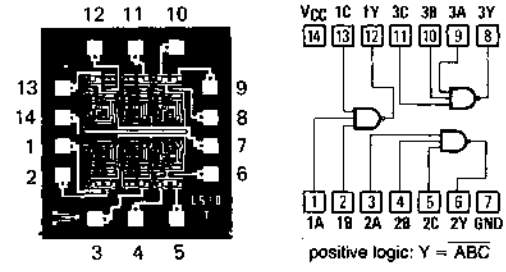
LS04
HEX INVERTER



positive logic: $Y = \overline{A}$

Die Size .060 x .067

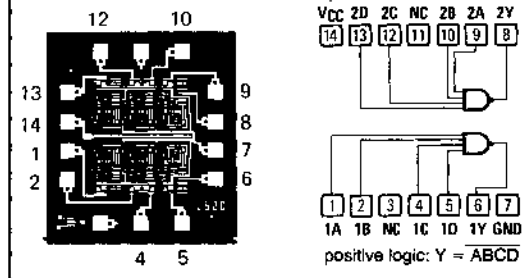
LS10
TRIPLE 3-INPUT NAND GATE



positive logic: $Y = \overline{ABC}$

Die Size .060 x .067

LS20
DUAL 4-INPUT NAND GATE

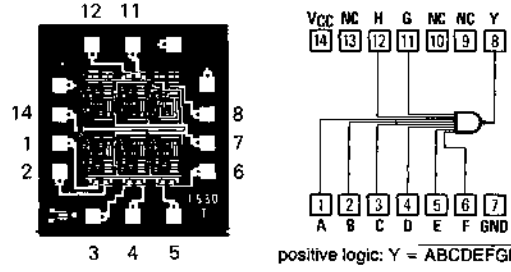


positive logic: $Y = \overline{ABCD}$

Die Size .060 x .067

NC — No internal connection

LS30
8-INPUT NAND GATE



positive logic: $Y = \overline{ABCDEFGH}$

Die Size .060 x .067

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Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IL}=V_{IL}max, I_{OH}=-400μA, V_{IL}=0.7V		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V	I_{OL}=4 mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8 mA					0.3	0.45	V
I_I	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}	V_{CC}=MAX,		-15		-100	-15		-100	mA
I_{CCH}	V_{CC}=MAX, All inputs at 0V (Per Gate)	LS00,04,10,20		0.2	0.4		0.2	0.4	mA
		LS30		0.35	0.5		0.35	0.5	
I_{CCL}	V_{CC}=MAX, All inputs at 4.5 (Per Gate)			0.6	1.1		0.6	1.1	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

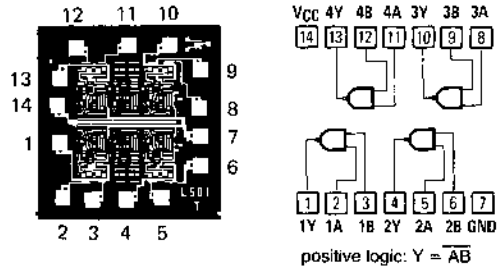
Parameter		-55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS00,04, 10,20		6	12	3.0	5.0	10		7	12	ns
	LS30		7	11	4.0	6	11		9	15	
t_{PHL}	LS00,04,10,		9	15	3.0	5.0	10		8	14	ns
	LS20		10	16	4.0	8.0	12		10	16	
	LS30		18	25	6.0	15	20		10	17	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS00,04, 10,20		9	15		9	15		10	16	ns
	LS30		8	13		8	13		12	18	
t_{PHL}	LS00,04,10,		11	17		10	16		10	16	ns
	LS20		12	16		12	16		12	18	
	LS30		27	35		21	28		16	23	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

Positive-NAND Gates, Hex Inverters With Open-Collector Outputs

PIN-OUT AND LOGIC DIAGRAMS

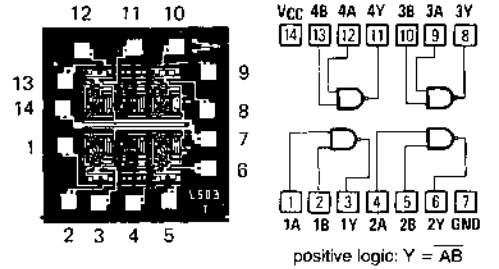
LS01
QUADRUPLE 2-INPUT NAND GATE



positive logic: $Y = \overline{AB}$

Die Size .060 x .067

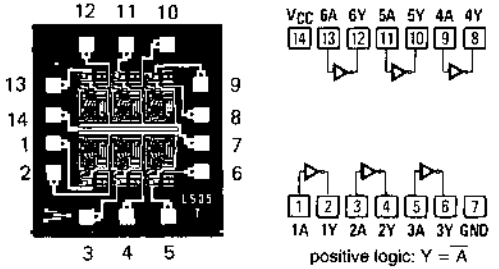
LS03
QUADRUPLE 2-INPUT NAND GATE



positive logic: $Y = \overline{AB}$

Die Size .060 x .067

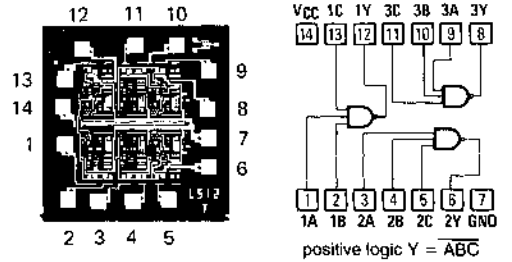
LS05
HEX INVERTER



positive logic: $Y = \overline{A}$

Die Size .060 x .067

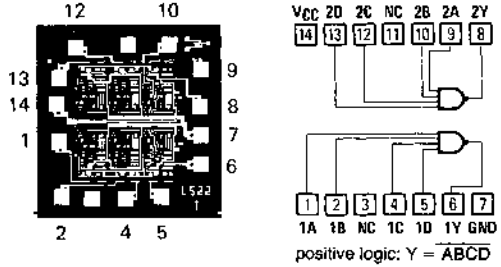
LS12
TRIPLE 3-INPUT NAND GATE



positive logic $Y = \overline{ABC}$

Die Size .060 x .067

LS22
DUAL 4-INPUT NAND GATE



positive logic: $Y = \overline{ABCD}$

Die Size .060 x .067

NC – No internal connection

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125			70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*			9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=−18mA				−1.5			−1.5	V
I_{OH}	V_{CC}=MIN,	V_{OH}=5.5V	V_{IL}=0.7V			100			100	μA
V_{OL}	V_{CC}=MIN,	V_{IH}=2V	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.3	0.5	
I_I	V_{CC}=MAX,	V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX,	V_I=0.4V				−0.4			−0.4	mA
I_{CCH}	V_{CC}=MAX,	All inputs at 0V (Per Gate)			0.2	0.4		0.2	0.4	mA
I_{CCL}	V_{CC}=MAX,	All inputs at 4.5V (Per Gate)			0.6	1.1		0.6	1.1	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

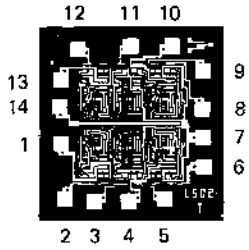
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

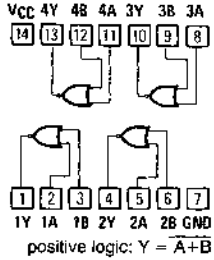
Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure B, page 2-174)										
t_{PLH}	7.0	16	28	7.0	14	22	7.0	15	28	ns
t_{PHL}	6.0	12	22	4.0	10	18	4.0	10	18	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure B, page 2-174)										
t_{PLH}	12	18.0	36	12	20	30	12	21	35	ns
t_{PHL}	6.0	12	25	6.0	12	20	6.0	12	25	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PIN-OUT AND LOGIC DIAGRAMS

LS02
QUADRUPLE 2-INPUT NOR GATE

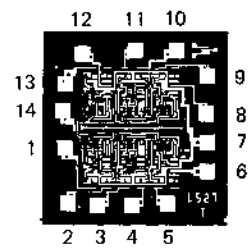


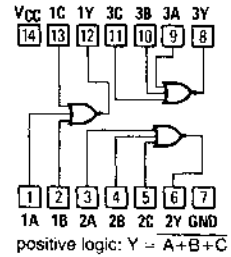


positive logic: $Y = \overline{A+B}$

Die Size .053 x .053

LS27
TRIPLE 3-INPUT NOR GATE





positive logic: $Y = \overline{A+B+C}$

Die Size .053 x .053

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, I_{OH}=-400μA	V_{IL}=0.7V	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN,	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}	V_{CC}=MAX,		-15		-100	-15		-100	mA
I_{CCH}†	V_{CC}=MAX, All inputs at 0V	LS02		1.6	3.2		1.6	3.2	mA
		LS27		2.0	4.0		2.0	4.0	
I_{CCL}	V_{CC}=MAX, All inputs at 5V	LS02		2.8	5.4		2.8	5.4	mA
		LS027		3.4	6.8		3.4	6.8	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		5	11		6.0	11		8	13	ns
t_{PHL}		7	14		6.0	12		4	14	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		8	13		8	13		10	15	ns
t_{PHL}		10	15		7	14		7	15	ns

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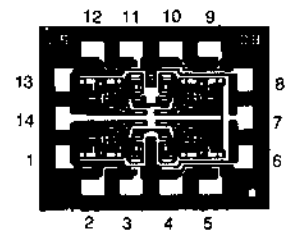
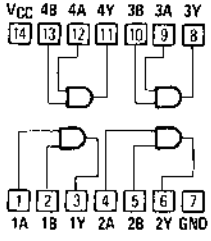
PIN-OUT AND LOGIC DIAGRAMS

LS08
QUADRUPLE 2-INPUT AND GATES

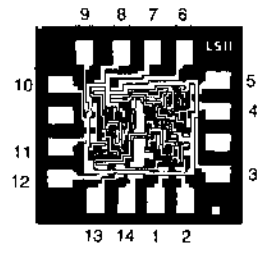


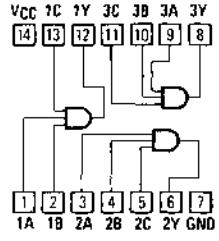


positive logic: Y = AB

Die Size .045 x .056

LS11
TRIPLE 3-INPUT AND GATES

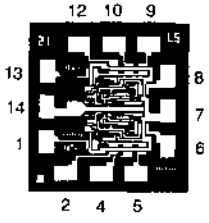


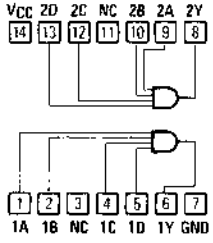


positive logic: Y = ABC

Die Size .052 x .054

LS21
DUAL 4-INPUT AND GATES





positive logic: Y = ABCD

Die Size .042 x .044

NC – No internal connection

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			11			20	
Operating free-air temperature, T_A		−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, I_{OH}=−400μA	V_{IH}=2.0V	2.5	3.4		2.7	3.4		V
V_{OL}		I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CCH}	V_{CC}=MAX, All inputs at 4.5V (Per Gate)			0.6	1.2		0.6	1.2	mA
I_{CCL}	V_{CC}=MAX, All inputs at 0V (Per Gate)			1.1	2.2		1.1	2.2	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS08,11		9	4		8.5	13		9	14	ns
	LS21		10	15		9	14		10	15	
t_{PHL}	LS08,11		6	11		6	10		8	12	ns
	LS21		6	11		6	10		8	12	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS08,11		11	17		10	15		11	16	ns
	LS21		12	22		12	20		12	23	
t_{PHL}	LS08,11		10	15		8	12		11	16	ns
	LS21		14	22		12	20		12	23	

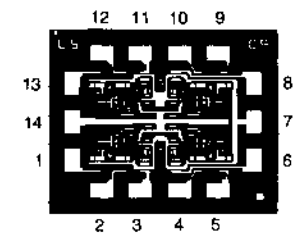
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Positive-AND Gates
With Open-Collector Outputs

LS09 LS15

PIN-OUT AND LOGIC DIAGRAMS

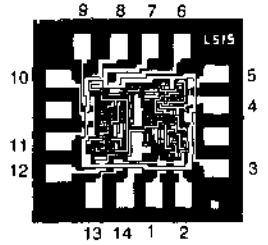
LS09
QUADRUPLE 2-INPUT AND GATES



Die Size .045 x .056

positive logic: Y = AB

LS15
TRIPLE 3-INPUT AND GATES



Die Size .052 x .054

positive logic: Y = ABC

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{OH}=5.5V, V_{IH}=2.0V				100			100	μA
I_{OH}	V_{CC}=MIN, V_{IL}=V_{IL}MAX	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{CCH}	V_{CC}=MAX, All inputs at 4.5V (Per Gate)			0.6	1.2		0.6	1.2	mA
I_{CCL}	V_{CC}=MAX, All inputs at 0V (Per Gate)			1.1	2.2		1.1	2.2	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. B, page 2-174)										
t_{PLH}		14	20		14	21		28	42	ns
t_{PHL}		10	15		8	12		9	13	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. B, page 2-174)										
t_{PLH}		30	38		30	38		40	54	ns
t_{PHL}		16	23		12	17		13	17	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

Schmitt-Trigger Positive-NAND Gates and Inverters with Totem-Pole Outputs

FEATURES

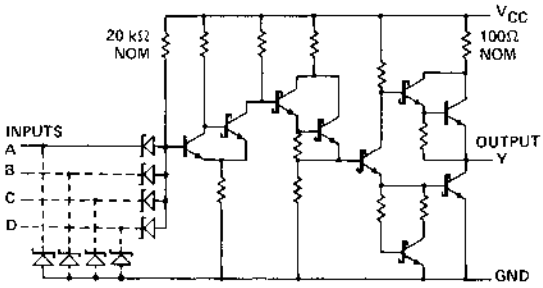
- Operation from Very Slow Transitions
- Temperature-Compensated Threshold Levels
- Temperature-Compensated Hysteresis, Typically 0.8V
- High Noise Immunity

DESCRIPTION

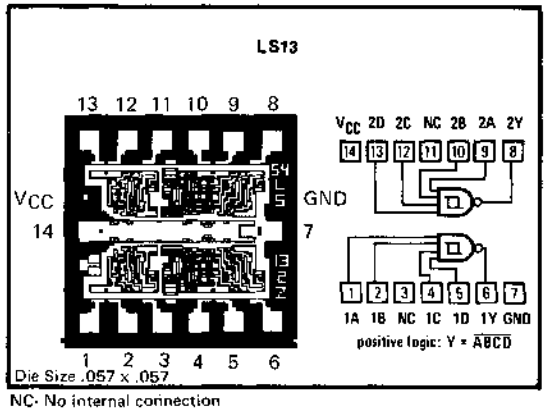
Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

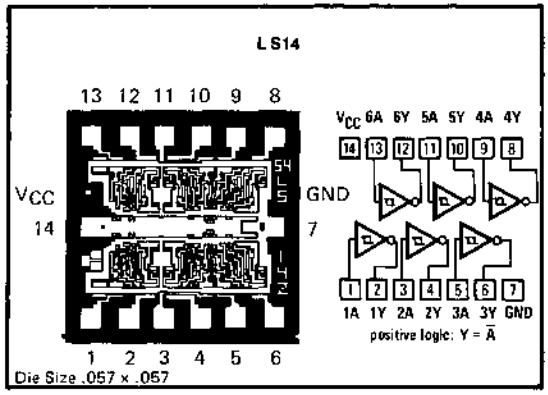
SCHEMATIC (EACH GATE)



PIN-OUT AND LOGIC DIAGRAMS



NC- No internal connection



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

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Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{T+}	V_{CC}=5V		1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	V_{CC}=5V		.5	.8	1.0	.5	.8	1.0	V
$V_{T+} - V_{T-}$	V_{CC}=5V		0.4	0.8		0.4	0.8		V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, I_{OH}=−400μA, V_I=0.6V		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_I=2V	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_{T+}	V_{CC}=5V, V_I=V_{T+}			−0.14			−0.14		mA
I_{T-}	V_{CC}=5V, V_I=V_{T-}			−0.18			−0.18		mA
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CCH}	V_{CC}=MAX, V_I=0V	LS13		2.9	6		2.9	6	mA
		LS14		8.6	16		8.6	16	
I_{CCL}	V_{CC}=MAX, V_I=4.5V	LS13		4.1	7		4.1	7	mA
		LS14		12	21		12	21	

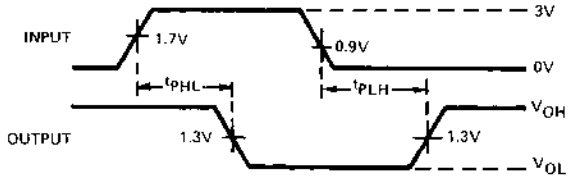
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS13	16	28			15	22		16	30	ns
	LS14	16	28			15	22		16	30	ns
t_{PHL}	LS13	22	38			18	27		20	38	ns
	LS14	17	32			15	22		16	30	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)											
t_{PLH}	LS13	20	38			20	27		20	38	ns
	LS14	20	38			20	27		21	38	ns
t_{PHL}	LS13	25	42			25	33		25	42	ns
	LS14	21	38			20	27		21	38	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PARAMETER MEASUREMENT INFORMATION

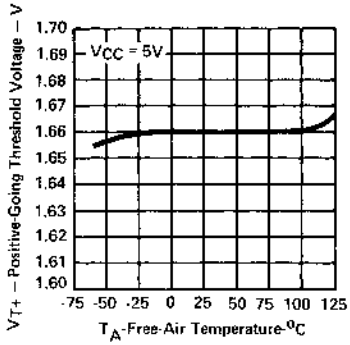


VOLTAGE WAVEFORMS

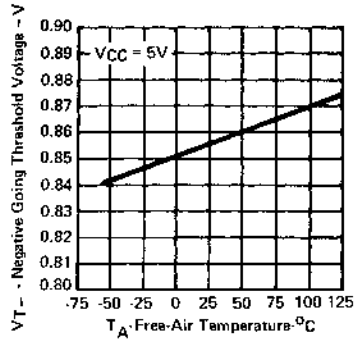
NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50Ω and PRR ≤ 1 MHz, t_r ≤ 15 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

TYPICAL CHARACTERISTICS†

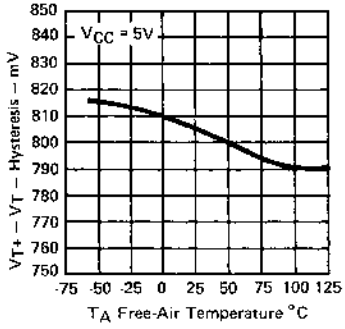
POSITIVE-GOING THRESHOLD VOLTAGE VS FREE-AIR TEMPERATURE



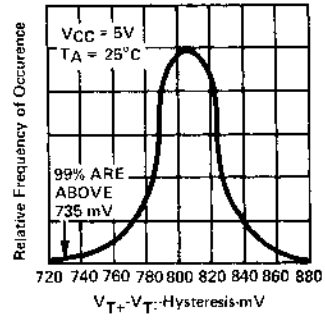
NEGATIVE-GOING THRESHOLD VOLTAGE VS FREE-AIR TEMPERATURE



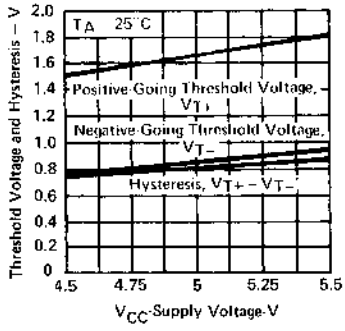
HYSTERESIS VS FREE-AIR TEMPERATURE



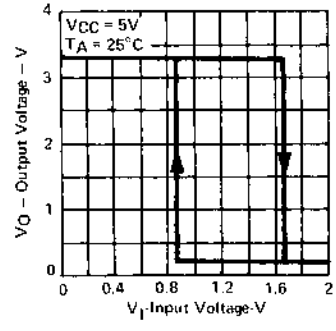
DISTRIBUTION OF UNITS FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS VS SUPPLY VOLTAGE

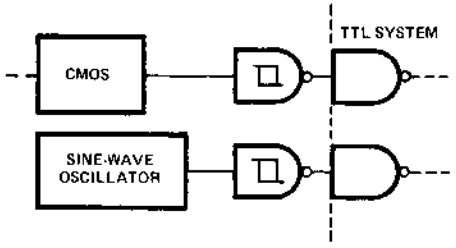


OUTPUT VOLTAGE VS INPUT VOLTAGE

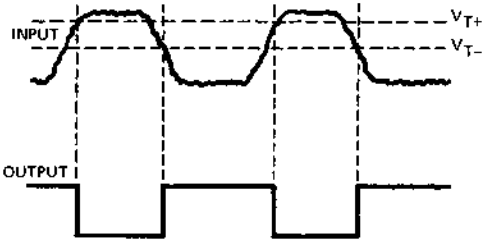


†Data for temperatures below 0°C and above 70°C and supply voltages below 4.75V and above 5.25 are applicable for 9LS/54LS13, and 9LS/54LS14.

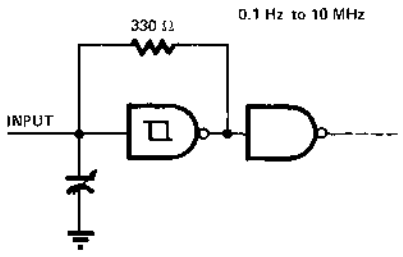
TYPICAL APPLICATION DATA



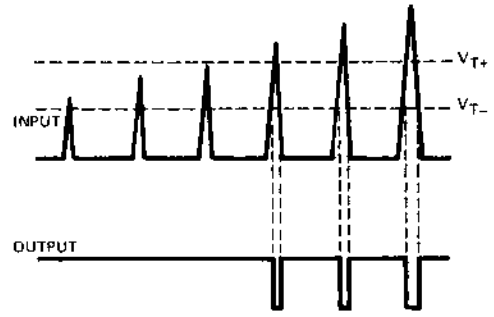
TTL SYSTEM INTERFACE FOR SLOW INPUT WAVEFORMS



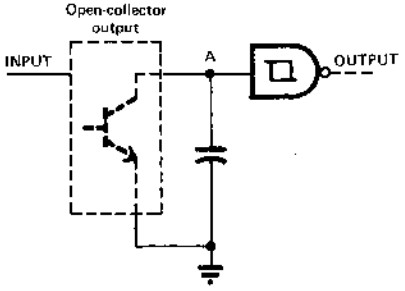
PULSE SHAPER

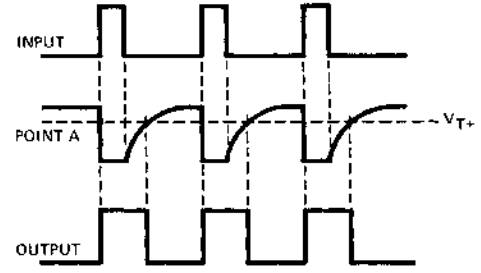


MULTIVIBRATOR



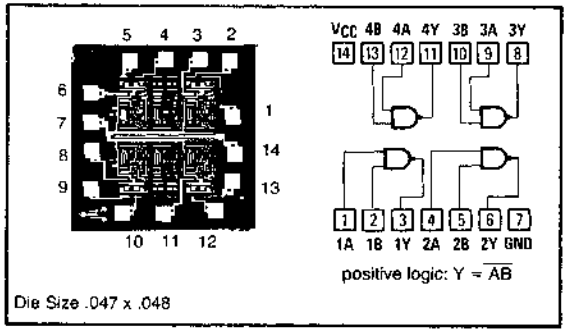
THRESHOLD DETECTOR





PULSE STRETCHER

PIN-OUT AND LOGIC DIAGRAM (OPEN-COLLECTOR OUTPUTS)



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
I_{OH}	V_{CC}=MIN, V_{IL}=V_{IL} max	V_{OH}=12V			50			50	μA
		V_{OH}=15V			1			1	mA
V_{OL}	V_{CC}=MIN, V_{IH}=2V	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{CCH}	V_{CC}=MAX, All inputs at 0V			0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC}=MAX, All inputs at 4.5V			2.4	4.4		2.4	4.4	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.

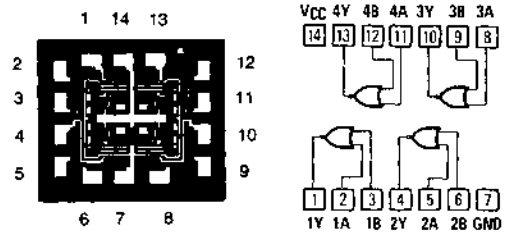
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. B, page 2-174)										
t_{PLH}	7.0	16	28	7.0	14	22	7.0	15	28	ns
t_{PHL}	6.0	12	22	4.0	10	18	4.0	10	18	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. B, page 2-174)										
t_{PLH}	12	18	35	12	20	30	12	21	35	ns
t_{PHL}	6.0	12	25	6.0	12	20	6.0	12	25	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PIN-OUT AND LOGIC DIAGRAMS

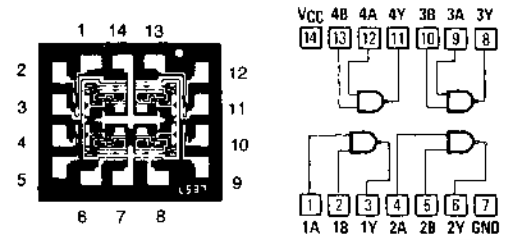
LS28
QUADRUPLE 2-INPUT NOR BUFFER



Die Size .045 x .052

positive logic: $Y = \overline{A+B}$

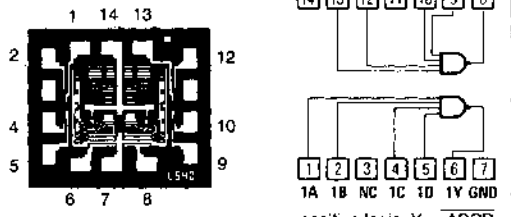
LS37
QUADRUPLE 2-INPUT NAND BUFFER



Die Size .045 x .052

positive logic: $Y = \overline{AB}$

LS40
DUAL 4-INPUT NAND BUFFER



Die Size .045 x .052

positive logic: $Y = \overline{ABCD}$

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			60			60	
	Low logic level			30			60	
Operating free-air temperature, T_A		−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, I_{OH}=−1.2mA	V_{IL}=0.7V	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V	I_{OL}=12mA		0.25	0.4		0.25	0.4	V
		I_{OL}=22mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}	V_{CC}=MAX		−30		−100	−30		−100	mA
I_{CCH}	V_{CC}=MAX, All inputs at 0V (Per Gate)	LS28		0.45	0.9		0.45	0.9	mA
		LS37,40		0.23	0.5		0.23	0.5	
I_{CCL}	V_{CC}MAX, All inputs at 5V (Per Gate)	LS28		1.7	3.45		1.7	3.45	mA
		LS37,40		1.5	3.0		1.5	3.0	

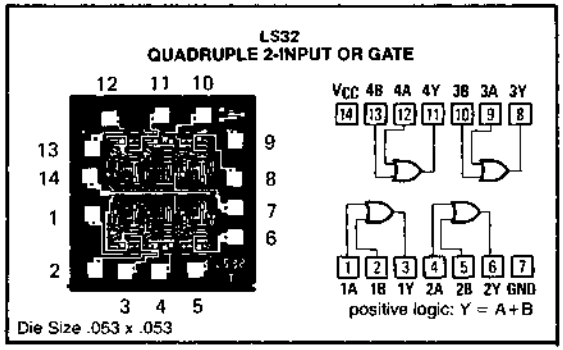
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45pF, R_L = 667Ω (See Fig. A, page 2-174)										
t_{PLH}		6	10		5	11		6	14	ns
t_{PHL}		9	14		7	15		7	15	ns
Test Conditions: C_L = 125pF, R_L = 667Ω (See Fig. A, page 2-174)										
t_{PLH}		8	16		7	15		8	16	ns
t_{PHL}		14	20		10	18		10	20	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PIN-OUT AND LOGIC DIAGRAM



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Operating free-air temperature, T_A		−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=−18mA			−1.5			−1.5	V
V_{OH}	V_{CC}=MIN,	I_{OH}=−400μA, V_{IL}=0.7V	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX,	V_I=7V			0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V			20			20	μA
I_{IL}	V_{CC}=MAX,	V_I=0.4V			−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CCH}	V_{CC}=MAX,	All inputs at 5V		3.1	6.2		3.1	6.2	mA
I_{CCL}	V_{CC}=MAX,	All inputs at 0V		4.9	9.8		4.9	9.8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

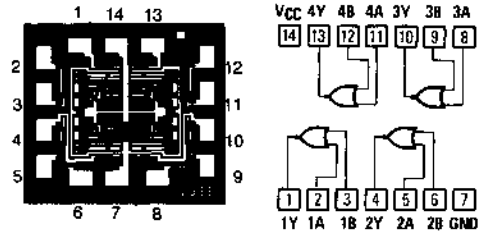
Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		7	12		7	11		9	13	ns
t_{PHL}		7	13		7	12		9	14	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		9	14		8	13		10	15	ns
t_{PHL}		11	17		10	15		12	18	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

NOR, NAND Buffers With Open-Collector Outputs

PIN-OUT AND LOGIC DIAGRAMS

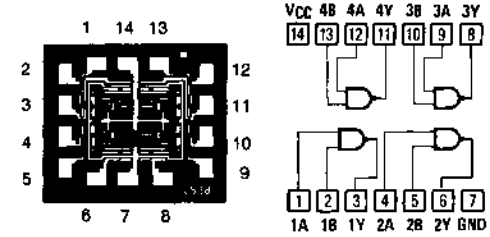
LS33
QUADRUPLE 2-INPUT NOR BUFFER



Die Size .045 x .052

positive logic: $Y = \overline{A+B}$

LS38
QUADRUPLE 2-INPUT NAND BUFFER



Die Size .045 x .052

positive logic: $Y = \overline{AB}$

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			22			22	mA
Operating free-air temperature, T_A	-55		125				°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
I_{OH}	V_{CC}=MIN, $V_{IL}=V_{IL}$max	V_{OH}=5.5V			250			250	μA
V_{OL}	V_{CC}=MIN, V_{IH}=2V	I_{OL}=12mA		0.25	0.4		0.25	0.4	V
		I_{OL}=24mA					0.35	0.5	V
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{CCH}	V_{CC}=MAX, All inputs at 0V	LS33		1.8	3.6		1.8	3.6	mA
		LS38		0.9	2.0		0.9	2.0	
I_{CCL}	V_{CC}=MAX, All inputs at 4.5V	LS33		6.9	13.8		6.9	1.38	mA
		LS38		6.0	12.0		6.0	12.0	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45pF, R_L = 667Ω (See Figure B, page 2-174)										
t_{PLH}		17	25	7.0	17	25		29	37	ns
t_{PHL}		13	22	4.0	9	16		10	17	ns
Test Conditions: C_L = 125pF, R_L = 667Ω (See Figure B, page 2-174)										
t_{PLH}		30	45		32	42		44	56	ns
t_{PHL}		22	36		18	35		15	35	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

RAYTHEON

4-Line To 10-Line Decoders (1-of-10) LS42 LS43 LS44

FEATURES

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  - 4-Line to 16-Line Decoders
  - 3-Line to 8-Line Decoders

DESCRIPTION

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The LS42 BCD-to-decimal decoders, the LS43 excess-3-to-decimal decoders, and the LS44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits.

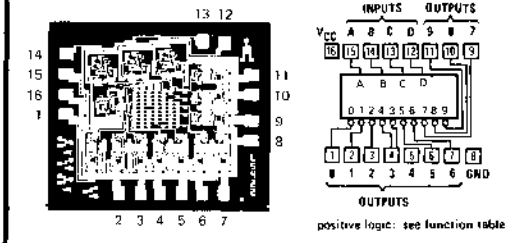
54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; 74LS circuits are characterized for operation from 0°C to 70°C.

NO.	LS42 BCD INPUT				LS43 EXCESS-3 INPUT				LS44 EXCESS 3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

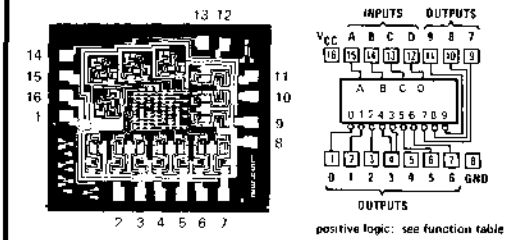
PIN-OUT DIAGRAM

LS42
BCD-TO-DECIMAL DECODER



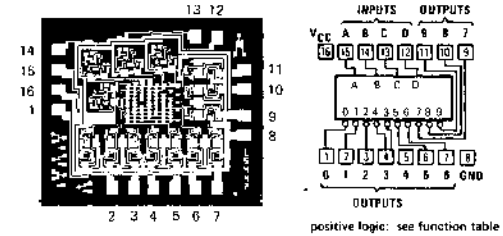
Die Size .077 x .065

LS43
EXCESS-3-TO-DECIMAL DECODER



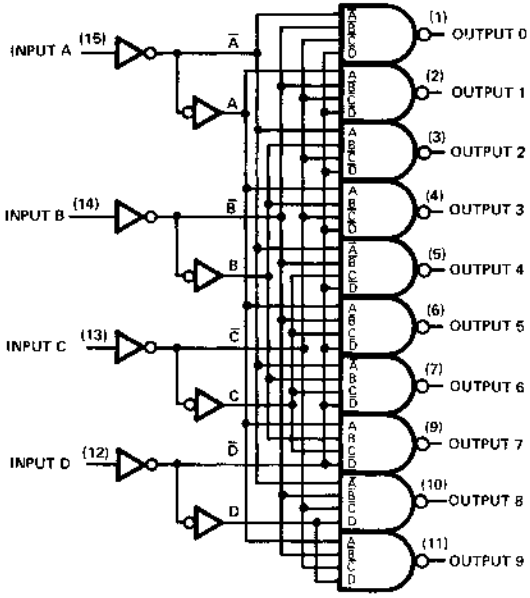
Die Size .077 x .065

LS44
EXCESS-3-GRAY-TO-DECIMAL DECODER

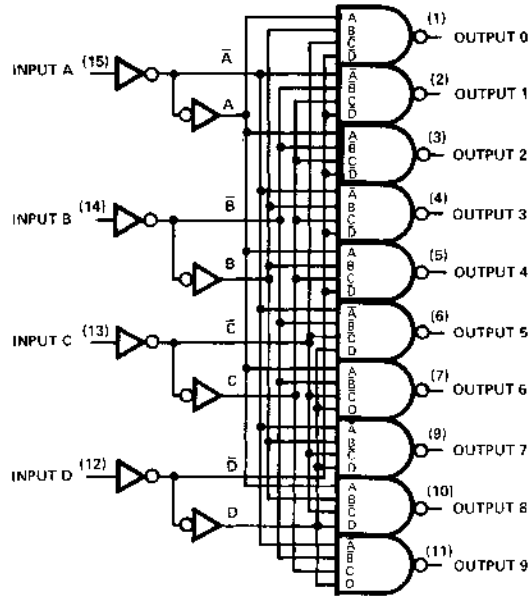


Die Size .077 x .065

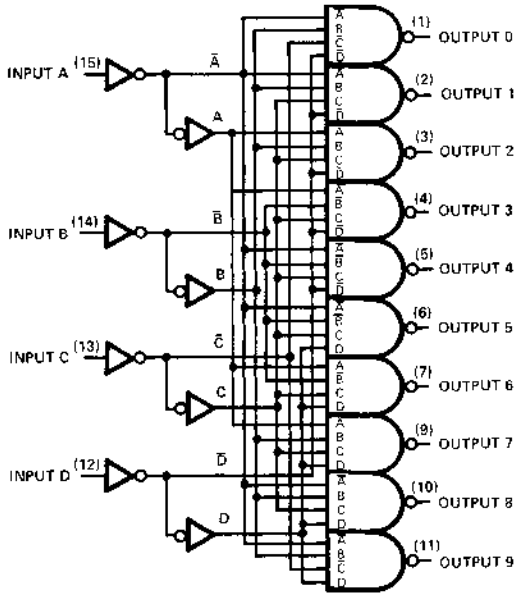
LOGIC DIAGRAMS



LS42
BCD-TO-DECIMAL DECODERS



LS43
EXCESS-3-TO-DECIMAL DECODERS



LS44
EXCESS-3-GRAY-TO-DECIMAL-DECODERS

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OH}=-400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX,			7	13		7	13	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all outputs open and inputs grounded.

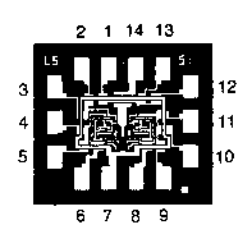
Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

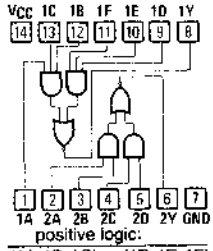
Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PHL}	A,B,C or D	Any output 2 gate delay		15	26		14	25		15	26	ns
t_{PHL}	A,B,C or D	Any Output 3 gate delay		17	31		17	30		18	31	ns
t_{PLH}	A,B,C or D	Any output 2 gate delay		11	27		10	25		11	26	ns
t_{PLH}	A,B,C or D	Any output 3 gate delay		22	35		17	30		20	34	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PHL}	A,B,C or D	Any Output 2 gate delay		18	32		18	31		19	33	ns
t_{PHL}	A,B,C or D	Any Output 3 gate delay		21	35		22	35		23	36	ns
t_{PHL}	A,B,C or D	Any Output 2 gate delay		21	33		20	32		21	33	ns
t_{PLH}	A,B,C or D	Any Output 3 gate delay		29	36		25	38		28	40	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PIN-OUT AND LOGIC DIAGRAMS

LS51
DUAL 2-WIDE AOI GATE

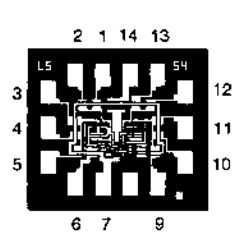


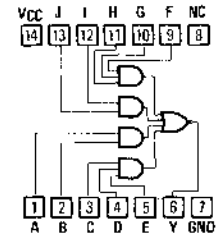


positive logic:
$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

Die Size .041 x .046

LS54
4-WIDE 2-3-3-2-INPUT AOI GATE

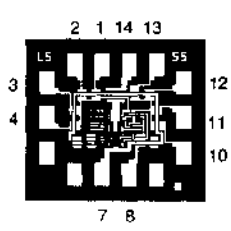


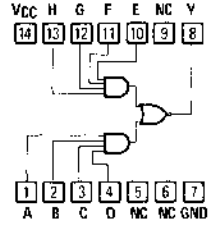


positive logic:
$Y = \overline{(AB) + (CDE) + (FGH) + (IJ)}$

Die Size .041 x .046

LS55
2-WIDE 4-INPUT AOI GATE





positive logic:
$Y = \overline{(ABCD) + (EFGH)}$

Die Size .041 x .046

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*			9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN,	I_{OH}=−400μA	V_{IL}=0.7V	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN,	V_{IH}=2V	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX,	V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX,	V_I=0.4V				−0.4			−0.4	mA
I_{OS}	V_{CC}=MAX			−15		−100	−15		−100	mA
I_{CCH}	V_{CC}=MAX,	See Note 1	LS51		0.8	1.6		0.8	1.6	mA
			LS54		0.8	1.6		0.8	1.6	
			LS55		0.4	0.8		0.4	0.8	
I_{CCL}	V_{CC}=MAX,	See Note 2	LS51		1.4	2.8		1.4	2.8	mA
			LS54		1.0	2.0		1.0	2.0	
			LS55		0.7	1.3		0.7	1.3	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

NOTES:
1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5V, the remaining inputs grounded, and the outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		8	13		8.0	13		8	12	ns
t_{PHL}		12	17		8.0	13		9	13	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		13	18		12	18		13	17	ns
t_{PHL}		15	20		12	18		13	17	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

Dual J-K Negative-Edge-Triggered Flip-Flops

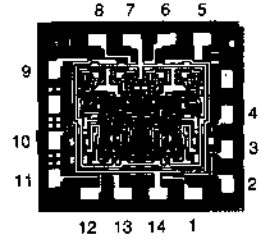
•Pin-for-Pin and functional equivalents to 5473, 5476, 54107, 54S112, 54S113

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

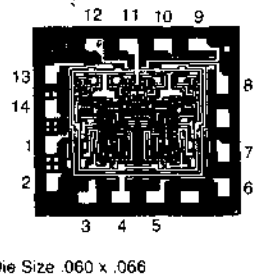
PIN-OUT DIAGRAMS

LS113



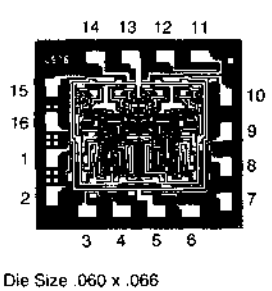
Die Size .060 x .066

LS73



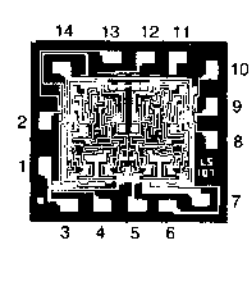
Die Size .060 x .066

LS76



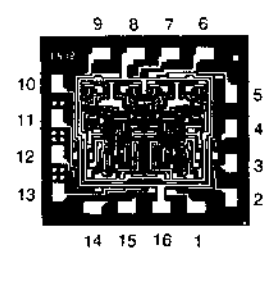
Die Size .060 x .066

LS107



Die Size .060 x .066

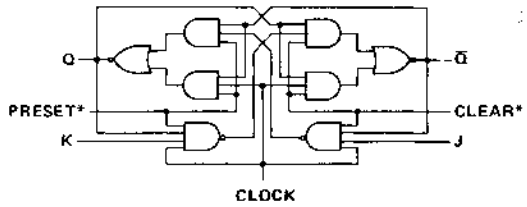
LS112



Die Size .060 x .066

RAYTHEON

LOGIC DIAGRAM (½)



	PRESET	CLEAR
LS73		X
LS76	X	X
LS107		X
LS112	X	X
LS113	X	

LS73, LS107
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

LS113
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

LS76, LS112
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Dual J-K Negative-Edge-Triggered Flip-Flops

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		15			15			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time, t_{setup}		15			15			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0	0	70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the falling edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the falling edge of the clock in order to insure recognition. These devices require no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.50	
I_I	J or K					0.1			0.1	mA
	Clock	V_{CC}=MAX, V_I=7V				0.4			0.4	
	Preset or Clear					0.3			0.3	
I_{IH}	J or K					20			20	μA
	Clock	V_{CC}=MAX, V_I=2.7V				80			80	
	Preset or Clear					60			60	
I_{IL}	J or K					−0.4			−0.4	mA
	Clock	V_{CC}=MAX, V_I=0.4V				−0.8			−0.8	
	Preset or Clear					−0.8			−0.8	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX, See Note 1			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5V; then with clock, J, K, and preset grounded and clear at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)											
f_{max}					35	50					MHz
t_{PLH}	CLR,PR		8	12		8	12		11	15	ns
t_{PHL}	CLR,PR		14	19		11	17		13	18	ns
t_{PLH}	CK		8	12		8	12		10	14	ns
t_{PHL}	CK		13	18		11	16		11	16	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)											
f_{max}											MHz
t_{PLH}	CLR,PR		10	14		10	15		13	17	ns
t_{PHL}	CLR,PR		19	24		17	22		18	23	ns
t_{PLH}	CK		10	14		10	14		14	18	ns
t_{PHL}	CK		18	23		15	20		15	20	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

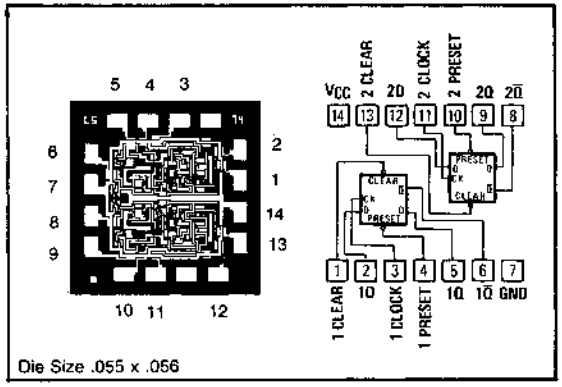
Dual D-Type Positive-Edge-Triggered Flip-Flop

DESCRIPTION

This monolithic dual edge-triggered D-type flip-flop features individual D, clock, preset, and clear inputs.

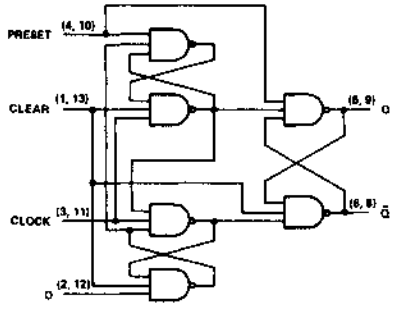
Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

PIN-OUT DIAGRAM



Die Size .055 x .056

LOGIC DIAGRAM (½)



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		17			17			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time, t_{setup}	High-level data	10			10			ns
	Low-level data	10			10			
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the D input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the D input after the rising edge of the clock in order to insure recognition. This device requires no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.50	
I_I	D input	V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
	Clock or preset					0.2			0.2	
	Clear					0.3			0.3	
I_{IH}	D input	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Clock or preset					40			40	
	Clear					60			60	
I_{IL}	D input	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	Clock or preset					−0.8			−0.8	
	Clear					−1.2			−1.2	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

†† I_{CC} is measured with outputs open with D, clock, and preset grounded; then with D, clock, and clear grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (Input)	To (Output)	−55°C			+25°C			+125°C			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A, page 2-174)													
f_{max}		maximum	clock frequency				30	45					MHz
t_{PLH}		set or clear	Q or $\overline{Q}$		12	18		10	15		16	23	ns
t_{PHL}	CK Low	set or clear	Q or $\overline{Q}$		22	29		18	24		21	28	ns
	CK High	set or clear	Q or $\overline{Q}$		29	39		26	35		27	38	
t_{PHL}		clock	Q or $\overline{Q}$		13	20		12	18		13	20	ns
t_{PHL}		clock	Q or $\overline{Q}$		17	27		14	22		15	24	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A, page 2-174)													
t_{PLH}					16	22		13	19		19	26	ns
t_{PHL}	CK Low	set or clear	Q or $\overline{Q}$		26	33		21	27		24	31	ns
	CK High	set or clear	Q or $\overline{Q}$		33	44		29	38		30	41	
t_{PLH}		clock	Q or $\overline{Q}$		17	24		15	22		16	25	ns
t_{PHL}		clock	Q or $\overline{Q}$		22	31		18	26		19	28	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

4-Bit Bistable Latches

DESCRIPTION

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in various 16-pin packages. For higher component density applications, the 'LS77 4-bit latch is available in 14-pin flat packages.

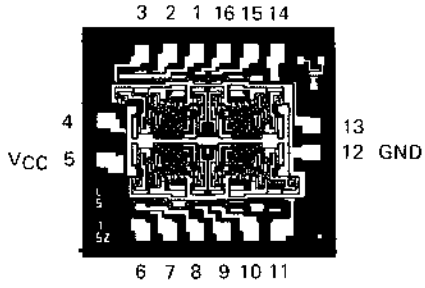
These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design.

FUNCTION TABLE
(Each Latch)

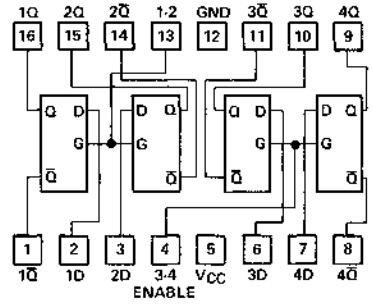
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevent
Q_0 = the level of Q before the high-to-low transition of G

LS75

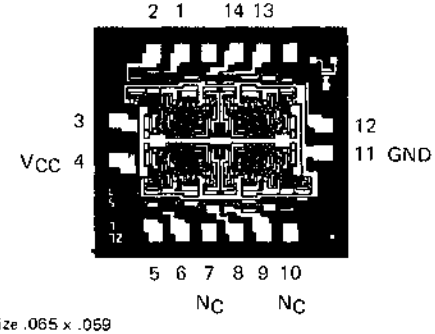


Die Size .065 x .059

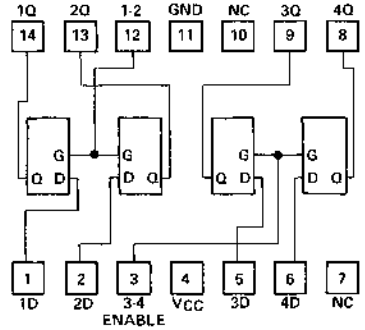


logic: see function table

LS77

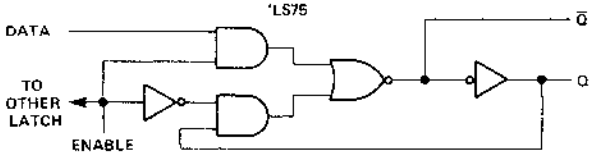


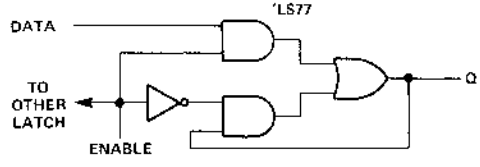
Die Size .065 x .059



logic: see function table

FUNCTIONAL BLOCK DIAGRAMS (each latch)





RAYTHEON

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS†		9LS/54LS			9LS/74LS			Unit
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC}=MIN, I_I=-8mA				-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max, I_{OH}=-440 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4 mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=MAX, V_I=7 V	D input			0.1			0.1	mA
			G input			0.4			0.4	
I_{IH}	High-level input current	V_{CC}=MAX, V_I=2.7 V	D input			20			20	μA
			G input			80			80	
I_{IL}	Low-level input current	V_{CC}=MAX, V_I=0.4 V	D input			-0.4			-0.4	mA
			G input			-1.6			-1.6	
I_{OS}	Short-circuit output current§	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	Supply current	V_{CC}=MAX, See Note 1	'LS75		6.3	12		6.3	12	mA
			'LS77		6.9	13				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is tested with all input grounded and all outputs open.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS75									Unit
			-55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Condition: C_L = 15pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		18	31		15	27		18	31	ns
t_{PHL}				12	16		9	17		12	16	
t_{PHL}	D	$\overline{Q}$		15	19		12	20		15	19	ns
t_{PHL}				10	14		7	15		10	14	
t_{PLH}	G	Q		18	22		15	27		18	22	ns
t_{PHL}				17	21		14	25		17	21	
t_{PLH}	G	$\overline{Q}$		19	23		16	30		19	23	ns
t_{PHL}				10	14		7	15		10	14	
Test Condition: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		22	37		19	33		22	37	ns
t_{PHL}				16	22		13	18		16	22	
t_{PLH}	D	$\overline{Q}$		19	25		16	21		19	25	ns
t_{PHL}				14	20		11	16		14	20	
t_{PLH}	G	Q		22	28		19	24		22	28	ns
t_{PHL}				21	27		18	23		21	27	
t_{PLH}	G	$\overline{Q}$		23	29		20	25		23	29	ns
t_{PHL}				14	20		11	16		14	20	

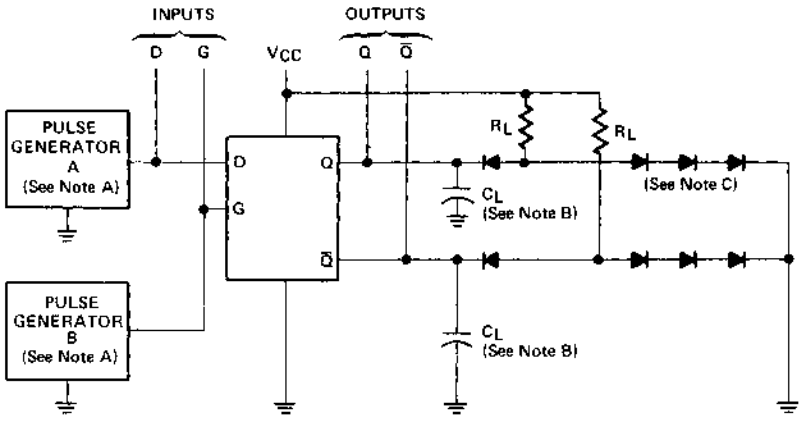
Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

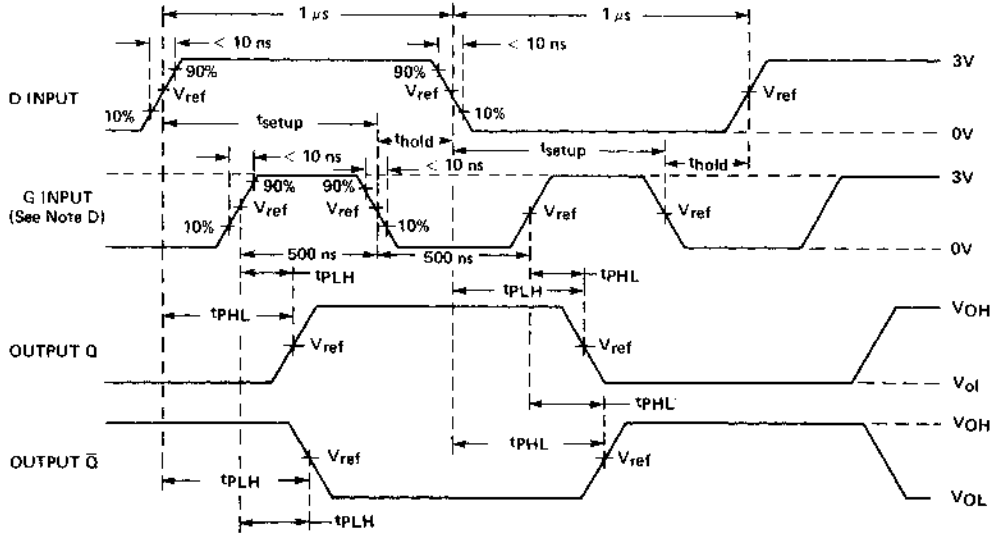
Parameter	From (Input)	To (Output)	9LS/54LS77									Unit
			-55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1 page 2-32)												
t_{PLH}	D	Q		15	24		11	19		14	23	ns
t_{PHL}				12	20		9	17		12	20	
t_{PLH}	G	Q		13	21		10	18		13	21	ns
t_{PHL}				13	21		10	18		13	21	
Test Conditions: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174 and Fig. 1, page 2-32)												
t_{PLH}	D	Q		17	28		15	24		18	28	ns
t_{PHL}				16	26		13	22		17	26	
t_{PLH}	G	Q		17	27		14	23		18	27	ns
t_{PHL}				17	27		14	23		18	27	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1.

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for pulse generator A, PRR≤500 kHz; for pulse generator B, PRR≤1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
E. $V_{ref} = 1.3$ V.
† Complementary Q outputs are on the 'LS75 only.

Dual J-K Negative-Edge-Triggered Flip-Flops

DESCRIPTION

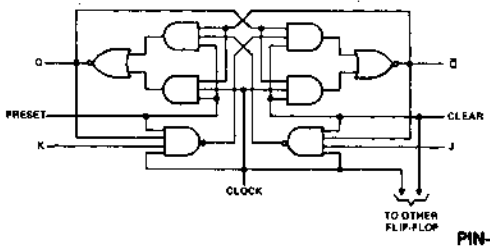
These monolithic dual J-K edge-triggered flip-flops feature individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE (EACH FLIP-FLOP)

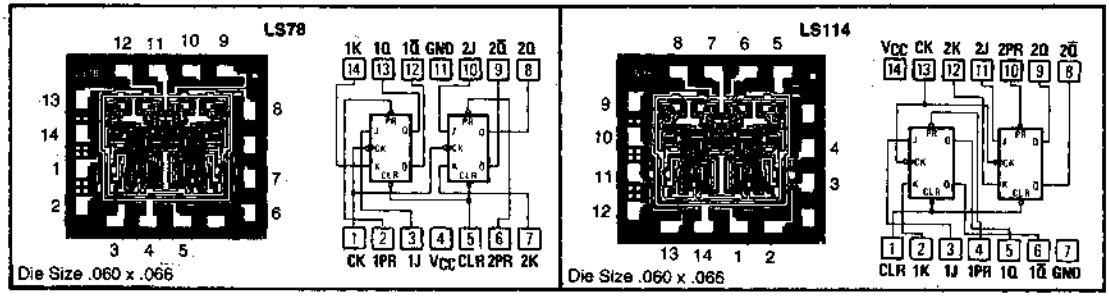
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

LOGIC DIAGRAM (½)



PIN-OUT DIAGRAMS



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		15			15			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time, t_{setup}		15			15			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the falling edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the falling edge of the clock in order to insure recognition. These devices require no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{CC}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	J or K	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	Preset					0.3			0.3	
	Clear					0.6			0.6	
	Clock					0.8			0.8	
I_{IH}	J or K	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Preset					60			60	
	Clear					120			120	
	Clock					160			160	
I_{IL}	J or K	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Preset					-0.8			-0.8	
	Clear					-1.6			-1.6	
	Clock					-1.6			-1.6	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX,			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

†† I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5V; then with clock, J, K, and preset grounded and clear at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A, page 2-174)												
f_{max}	maximum clock frequency					35	50					MHz
t_{PLH}	clear or preset	Q or $\overline{Q}$		8	12		8	12		11	15	ns
t_{PHL}				15	19		13	17		13	17	ns
t_{PLH}	clock	Q or $\overline{Q}$		8	12		8	12		11	15	ns
t_{PHL}				14	19		13	18		13	18	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A, page 2-174)												
t_{PLH}	clear or preset	Q or $\overline{Q}$		10	14		10	14		13	17	ns
t_{PHL}				19	24		16	21		16	21	ns
t_{PLH}	clock	Q or $\overline{Q}$		9	14		10	14		13	18	ns
t_{PHL}				19	24		17	21		17	22	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

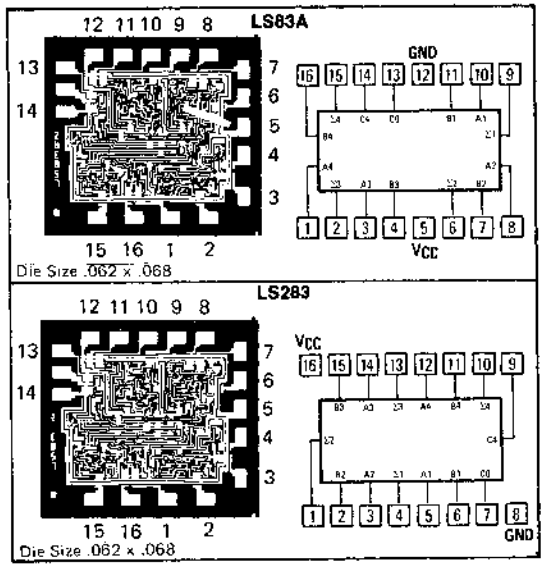
DESCRIPTION

These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

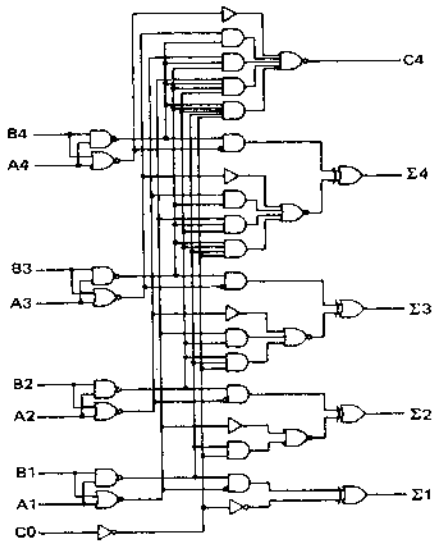
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

The LS83A and the LS283 are identical in performance; only the pin out is different. They are designed to replace the 5483A and the 54283 respectively. The LS283 is recommended for new designs, V_{CC} and ground on corner pins simplify board layout.

PIN-OUT DIAGRAMS



LOGIC DIAGRAM



FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE:

Input conditons at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A2, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

4-Bit Binary Full Adders With Fast Carry

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I Any A or B	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
I_I C0					0.1			0.1	
I_{IH} Any A or B	V_{CC}=MAX, V_I=2.7V				40			40	μA
I_{IH} C0					20			20	
I_{IL} Any A or B	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
I_{IL} C0					-0.4			-0.4	
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	V_{CC}=MAX, Outputs open	All inputs grounded		22	39		22	39	mA
		All B low, other inputs at 4.5V		19	34		19	34	
		All inputs at 4.5V		19	34		19	34	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

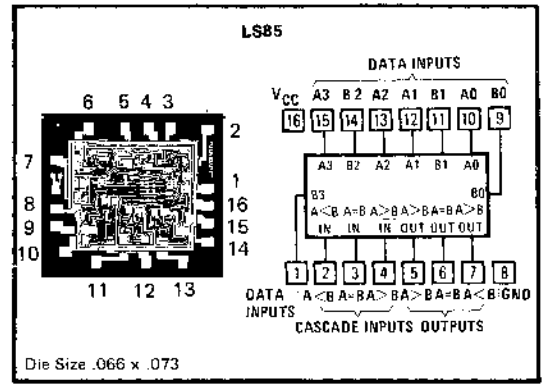
Parameter	From (input)	To (output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	C0	Any Σ		15	20		14	19		15	21	ns
t_{PHL}				15	21		16	22		20	27	
t_{PLH}	A_i or B_i	Σ_i		20	30		18	24		21	27	ns
t_{PHL}				19	29		15	24		17	25	
t_{PLH}	C0	C4		9	14		7	12		11	18	ns
t_{PHL}				9	14		9	13		11	16	
t_{PLH}	A_i or B_i	C4		9	15		8	13		11	17	ns
t_{PHL}				10	14		9	14		11	16	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	C0	Any Σ		16	21		15	20		17	22	ns
t_{PHL}				19	25		19	25		25	30	
t_{PLH}	A_i or B_i	Σ_i		25	32		18	26		25	32	ns
t_{PHL}				24	30		18	26		25	31	
t_{PLH}	C0	C4		11	16		10	15		12	19	ns
t_{PHL}				12	17		10	16		13	18	
t_{PLH}	A_i or B_i	C4		11	17		10	15		13	19	ns
t_{PHL}				13	18		12	16		14	20	

NOTE: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

DESCRIPTION

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A,B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A =B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, and 'LS85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

PIN-OUT AND LOGIC DIAGRAM

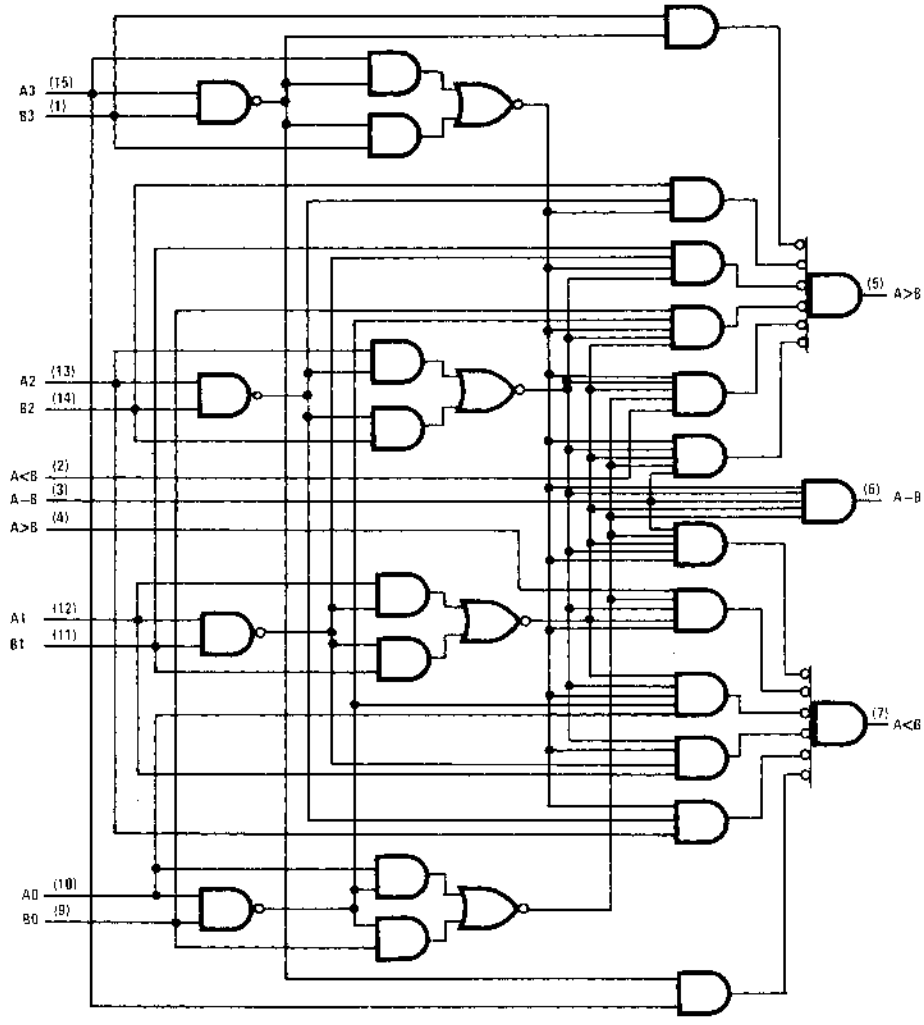


FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2>B2	X	X	X	X	X	H	L	L
A3 = B3	A2<B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1>B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1<B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0>B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0<B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level; L = low level, X = irrelevant

LOGIC DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	A<B, A>B inputs	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	all other inputs					0.3			0.3	
I_{IH}	A<B, A>B inputs	V_{CC}=MAX, V_I=2.7V				20			20	μA
	all other inputs					60			60	
I_{IL}	A<B, A>B inputs	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	all other inputs					−1.2			−1.2	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			10.4	20		10.4	20	mA

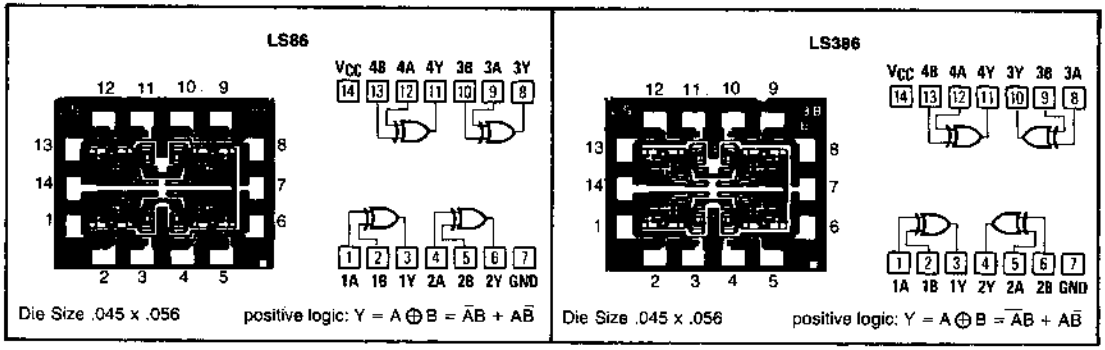
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (output)	No. of Gate Levels	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	Any A or B data input	A<B, A>B	1		14			14			14		ns
			2		20			19			19		
			3		25	42		24	36		24	41	
		A = B	4		28	50		27	45		26	48	
t_{PHL}	Any A or B data input	A<B, A>B	1		11			11			12		ns
			2		15			15			16		
			3		21	34		20	30		20	33	
		A = B	4		22	48		23	45		22	48	
t_{PLH}	A<B or A = B	A > B	1		14	27		14	22		14	27	ns
t_{PHL}	A<B or A = B	A > B	1		12	23		11	17		11	22	ns
t_{PLH}	A = B	A = B	2		13	23		13	20		12	22	ns
t_{PHL}	A = B	A = B	2		14	30		13	26		14	30	ns
t_{PLH}	A>B or A = B	A < B	1		16	26		14	22		15	25	ns
t_{PHL}	A>B or A = B	A < B	1		12	21		11	17		11	20	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	Any A or B data input	A<B, A>B	1		20			18			20		ns
			2		26			25			26		
			3		29	42		28	40		29	42	
		A = B	4		30	48		32	48		32	48	
t_{PHL}	Any A or B data input	A<B, A>B	1		15			14			15		ns
			2		18			18			18		
			3		26	36		26	36		26	36	
		A = B	4		38	50		36	48		37	49	
t_{PLH}	A<B or A = B	A > B	1		17	28		17	27		18	30	ns
t_{PHL}	A<B or A = B	A > B	1		14	21		14	20		15	21	ns
t_{PLH}	A = B	A = B	2		17	25		16	24		16	24	ns
t_{PHL}	A = B	A = B	2		15	31		14	30		16	32	ns
t_{PLH}	A>B or A = B	A < B	1		18	27		17	26		17	30	ns
t_{PHL}	A>B or A = B	A < B	1		15	22		14	21		14	22	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PIN-OUT AND LOGIC DIAGRAMS



LS86 and LS386 are electrically identical. The LS386 is a pin-for-pin replacement for the L386.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max,	I_{OL}=4mA		0.25	0.4	0.25	0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				40			40	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX,			6.1	10		6.1	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with the inputs grounded and the outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)		−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ												
t_{PLH}	A or B	Other input low		9	17		8	16		10	18	ns
t_{PHL}				9	14		8	13		10	14	
t_{PLH}	A or B	Other input high		7	14		7	15		10	17	ns
t_{PHL}				7	15		6	12		6	12	
Test Conditions: C_L = 50pF, R_L = 2kΩ												
t_{PLH}	A or B	Other input low		11	19		20	10		18	12	ns
t_{PHL}				13	17		17	11		16	12	
t_{PLH}	A or B	Other input high		9	16		19	9		17	12	ns
t_{PHL}				12	19		15	9		16	9	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

DESCRIPTION

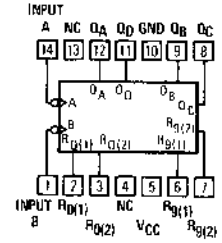
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90, divide-by-six for the 'LS92, and divide-by-eight for the 'LS93.

All of these counters have a gated zero reset and 'LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

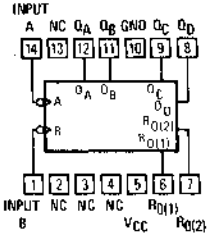
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

PIN-OUT DIAGRAMS

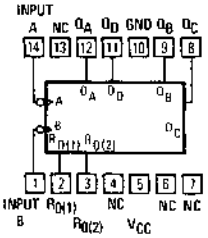
LS90



LS92



LS93



RAYTHEON

LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

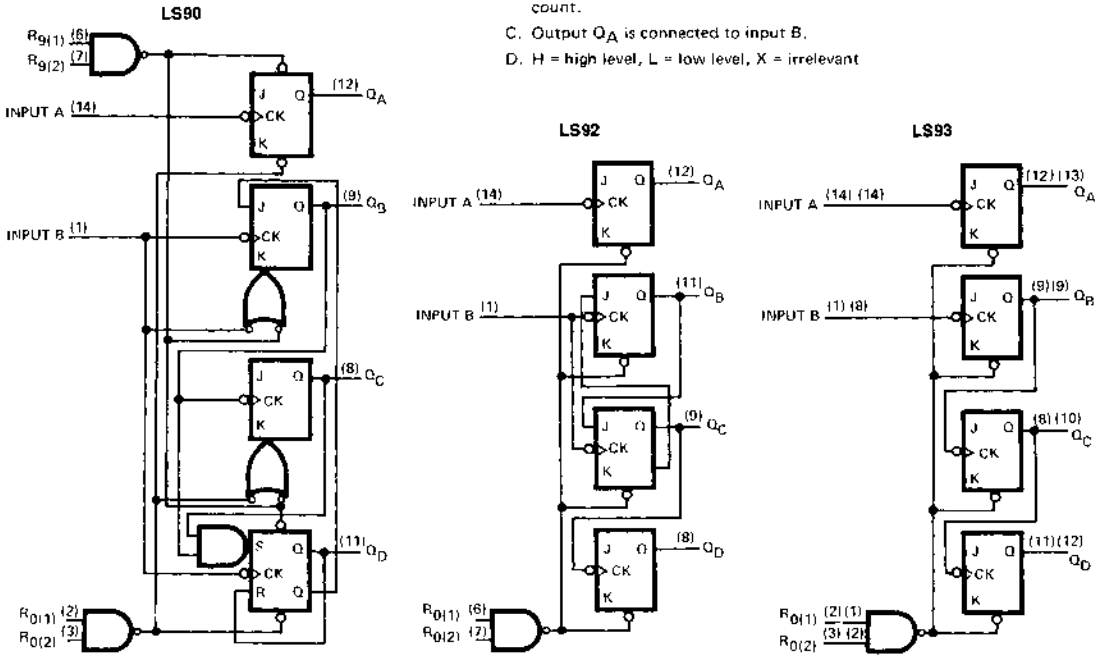
LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant



LOGIC DIAGRAMS

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1 on 2-46)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{setup}		25			25			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS90/92			9LS/74LS90/92			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max,	I_{OL}=4mA¶		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA¶					0.35	0.5	
I_I	Any reset	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	A input	V_{CC}=MAX, V_I=5.5V				0.2			0.2	
	B input					0.4			0.4	
I_{IH}	Any reset	V_{CC}=MAX, V_I=2.7V				20			20	μA
	A input					40			40	
	B input					80			80	
I_{IL}	Any reset	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	A input					-2.4			-2.4	
	B input					-3.2			-3.2	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX,	LS90		9	15		9	15	mA
			LS92		9	15		9	15	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

†† I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

¶ Outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS93			9LS/74LS93			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA¶		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA¶					0.35	0.5	
I_I	Any reset	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	A or B input	V_{CC}=MAX, V_I=5.5V				0.2			0.2	
I_{IH}	Any reset	V_{CC}=MAX, V_I=2.7V				20			20	μA
	A or B input					40			40	
I_{IL}	Any reset	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	A input					−2.4			−2.4	
	B input					−1.6			−1.6	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			9	15		9	15	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

†† I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

¶ Outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

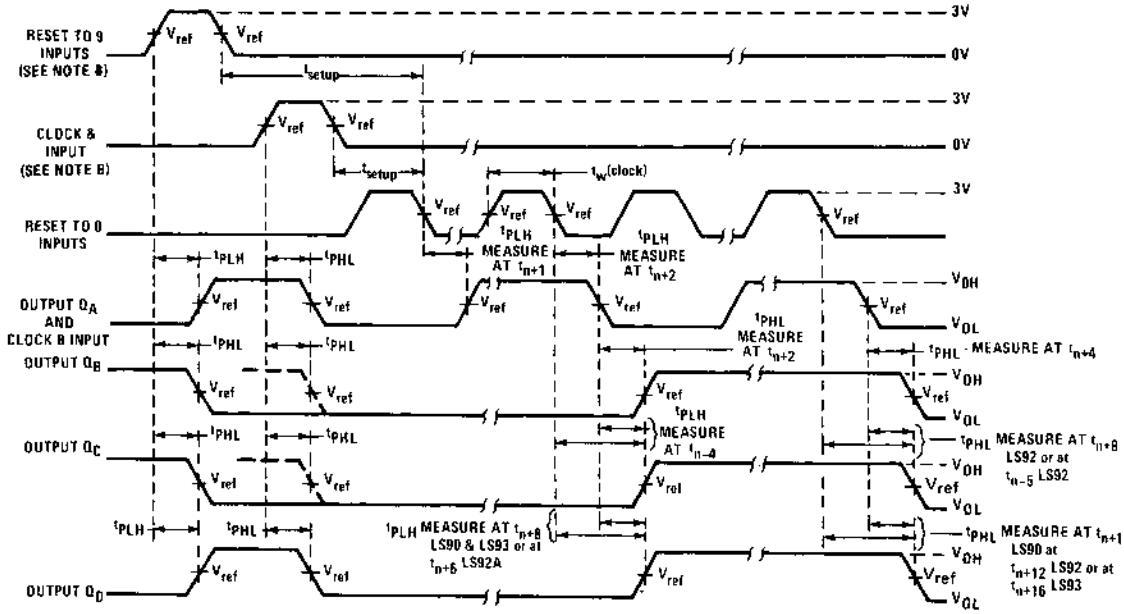
Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1, page 2-49)													
f_{max}	LS90	A	Q_A				32	42					MHz
		B	Q_B				16						
f_{max}	LS92	A	Q_A				32	42					MHz
		B	Q_B				16						
f_{max}	LS93	A	Q_A				32	42					MHz
		B	Q_B				16						
t_{PLH}	LS90	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS92	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS93	A	Q_A		13	20		10	16		13	20	ns
t_{PHL}					15	22		12	18		15	22	
t_{PLH}	LS90	A	Q_D		35	51		32	48		35	51	ns
t_{PHL}					37	56		34	50		37	56	
t_{PLH}	LS92	A	Q_D		35	54		32	48		35	54	ns
t_{PHL}					37	56		34	50		37	56	
t_{PLH}	LS93	A	Q_D		49	76		46	70		49	76	ns
t_{PHL}					49	76		46	70		49	76	
t_{PLH}	LS90	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS92	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS93	B	Q_B		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS90	B	Q_C		24	39		21	32		24	39	ns
t_{PHL}					27	42		23	35		27	42	
t_{PLH}	LS92	B	Q_C		13	20		10	16		13	20	ns
t_{PHL}					17	27		14	21		17	27	
t_{PLH}	LS93	B	Q_C		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS90	B	Q_D		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS92	B	Q_D		24	39		21	32		24	39	ns
t_{PHL}					27	41		23	35		27	41	
t_{PLH}	LS93	B	Q_D		38	57		34	51		38	57	ns
t_{PHL}					38	57		34	51		38	57	
t_{PHL}	LS90	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PHL}	LS92	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PHL}	LS93	Set-to-0	Any		30	47		26	40		30	47	ns
t_{PLH}	LS90	Set-to-9	Q_A, Q_D		24	35		20	30		24	35	ns
t_{PHL}			Q_B, Q_C		24	47		26	24		24	47	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1, page 2-49)													
t_{PLH}	LS90	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS92	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	A	Q_A		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS90	A	Q_D		39	56		36	52		39	56	ns
t_{PHL}					41	58		38	54		41	58	
t_{PLH}	LS92	A	Q_D		39	56		36	52		39	56	ns
t_{PHL}					41	58		38	54		41	58	
t_{PLH}	LS93	A	Q_D		53	82		50	78		53	82	ns
t_{PHL}					53	82		50	78		53	82	
t_{PLH}	LS90	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS92	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	B	Q_B		17	25		14	21		17	25	ns
t_{PHL}					41	27		16	23		19	27	
t_{PLH}	LS90	B	Q_C		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS92	B	Q_C		17	25		14	21		17	25	ns
t_{PHL}					19	27		16	23		19	27	
t_{PLH}	LS93	B	Q_C		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS90	B	Q_D		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS92	B	Q_D		29	41		26	37		29	41	ns
t_{PHL}					30	42		27	38		30	42	
t_{PLH}	LS93	B	Q_D		43	63		40	58		43	62	ns
t_{PHL}					43	62		40	58		43	62	
t_{PHL}	LS90	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PHL}	LS92	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PHL}	LS93	Set-to-0	Any		33	50		30	46		33	50	ns
t_{PLH}	LS90	Set-to-9	Q_A, Q_D		28	40		25	36		28	40	ns
t_{PHL}			Q_B, Q_C		33	49		30	45		33	49	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.



NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ns, $t_f \leq 5$ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} = 50 ohms

B. Each reset input is tested separately with the other reset at 4.5V.

C. Reference waveforms are shown with dashed lines.

FIGURE 1. VOLTAGE WAVEFORMS

FEATURES

- For Use In Digital Computer Systems
- For Use In Data-Handling Systems
- For Use In Control Systems

DESCRIPTION

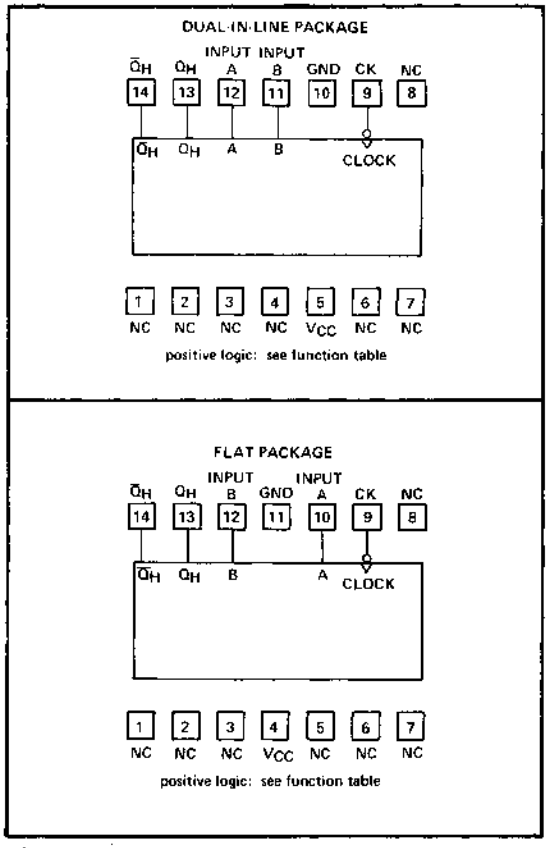
These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

FUNCTION TABLE

Inputs AT t_n		Outputs AT t_{n+8}	
A	B	Q_H	$\overline{Q}_H$
H	H	H	H
L	X	L	H
X	L	L	H

H = high, L = low,
X = irrelevant
t_n = Reference bit time, clock low
t_{n+8} = Bit time after 8 low-to-high clock transitions.

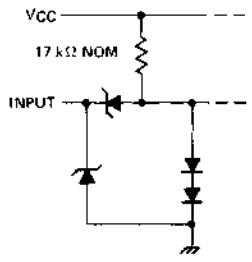
PIN-OUT DIAGRAM



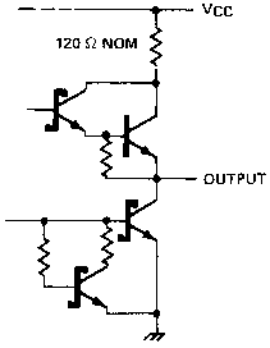
NC—No Internal Connection

SCHEMATICS OF INPUTS AND OUTPUTS

LS91
EQUIVALENT OF EACH INPUT

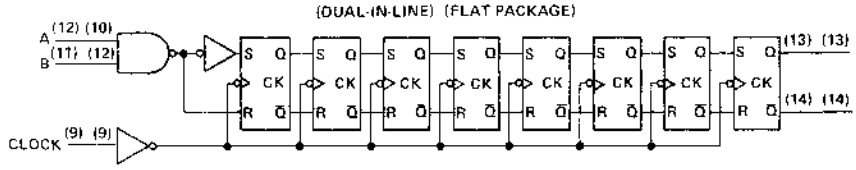


LS91
TYPICAL OF BOTH OUTPUTS



FUNCTIONAL BLOCK DIAGRAM

(DUAL-IN-LINE) (FLAT PACKAGE)



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_W	25			25			ns
Setup time, t_{su} (See Figure 1)	25			25			ns
Hold time, t_h (See Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

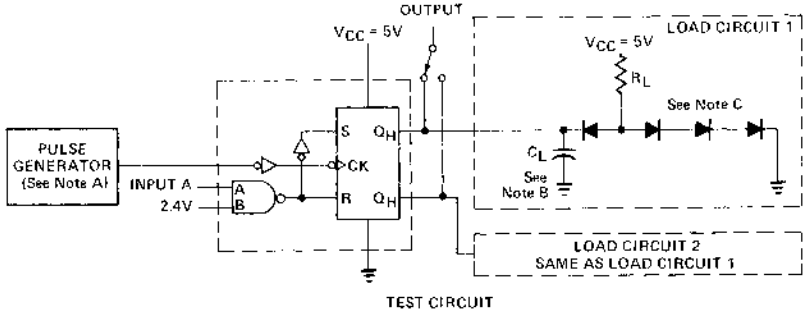
Parameter	Test Conditions†		9LS/54LS			9LS/74LS			Unit
			Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = V_{IL} max, I_{OH} = −400μA		2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = Max, V_I = 7V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL} Low-level input current	V_{CC} = Max, V_I = 0.4V				−0.4			−0.4	mA
I_{OS} Short-circuit current§	V_{CC} = Max		15		−100	15		−100	mA
I_{CC} Supply current	V_{CC} = Max, See Note 1			12	20		12	20	mA

†For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 1. I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

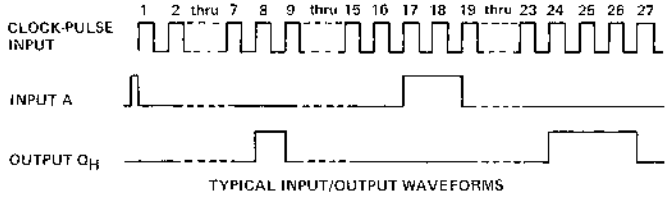
Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS									Unit
			-55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0kΩ (See Fig. A, page 2-174 and Fig. 1, page 2-55)												
f(max)						10	18					MHz
T_{PLH}	clock	Q_H		26	42		24	40		26	42	ns
T_{PHL}	clock	Q_H		28	45		27	40		28	45	ns
Test Conditions: C_L = 50pF, R_L = 2.0kΩ (See Fig. A, page 2-174 and Fig. 1, page 2-55)												
T_{PLH}	clock	Q_H		30	47		27	45		30	47	ns
T_{PHL}	clock	Q_H		33	52		30	48		33	52	ns

PARAMETER MEASUREMENT INFORMATION

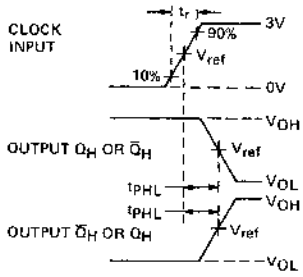


TEST CIRCUIT

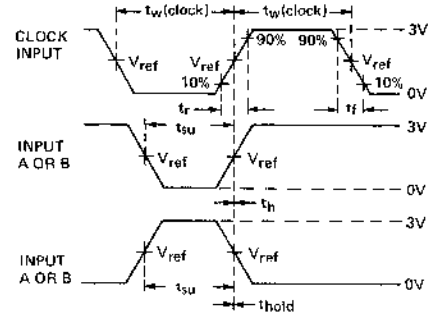


TYPICAL INPUT/OUTPUT WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



SWITCHING TIMES VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING TIMES

NOTES: A. The generator has the following characteristics: t_w(clock) = 500 ns; PRR ≤ 1 MHz; $Z_{out} \approx 50\ \Omega$; $t_r \approx 15$ ns, and $t_f = 6$ ns.
B. C_L includes probe and jig capacitance
C. All diodes are 1N3064 or 1N916
D. $V_{ref} = 1.3V$

4-Bit Bi-Directional Parallel-Access Shift Register

LS95B

DESCRIPTION

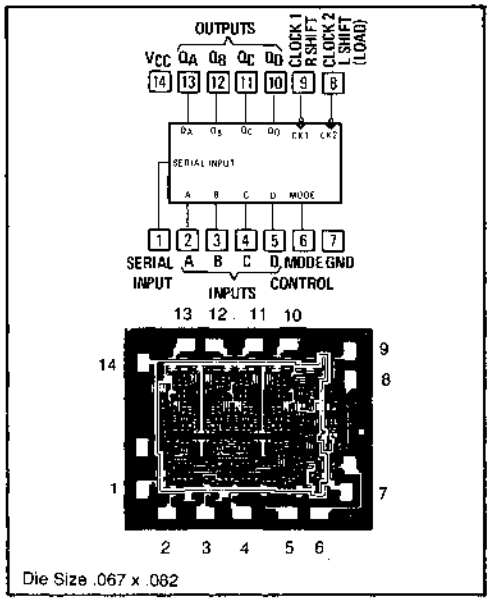
This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

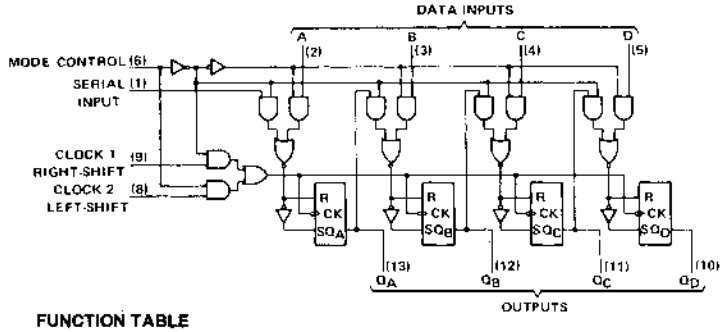
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS			
MODE	CLOCKS		SERIAL	PARALLEL							
CONTROL	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_{B}↑	Q_{C}↑	Q_{D}↑	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at input, A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 2 page 2-57)	25			25			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1 page 2-57)	0			0			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1 page 2-57)	20			20			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2 page 2-57)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2 page 2-57)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2 page 2-57)	10			10			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 1 page 2-57)	10			10			ns
Operating free-air temperature T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	Mode inputs	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	Mode inputs	V_{CC}=MAX, V_I=2.7V				40			40	μA
	Other inputs					20			20	
I_{IL}	Mode inputs	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
	Other inputs					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX,		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX, See Note 1			13	21		13	21	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with all outputs and serial inputs open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V then ground, applied to both clock inputs.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1 and 2, page 2-57)										
f_{max}				20	30					MHz
t_{PLH}		28	37		27	35		28	37	ns
t_{PHL}		32	45		30	40		32	45	ns
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174 and Fig. 1 and 2, page 2-57)										
t_{PLH}		32	42		31	40		32	42	ns
t_{PHL}		36	50		34	45		36	50	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PARAMETER MEASUREMENT INFORMATION

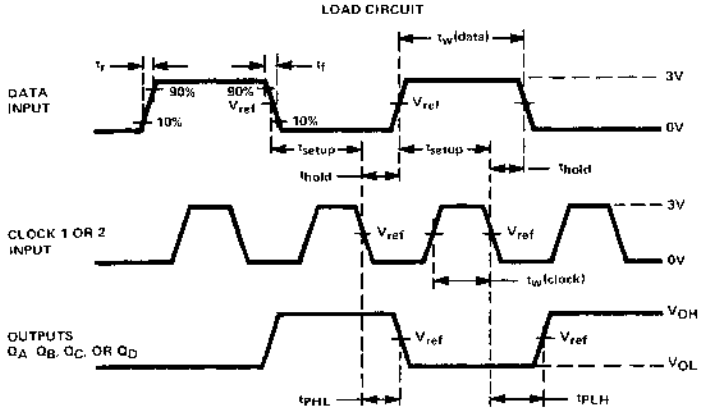


FIGURE 1 – SWITCHING TIMES

NOTES:

A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \cong 50\Omega$. For the data pulse generator, PRR = 500kHz; for the clock pulse generator, PRR = 1MHz. When testing f_{max}, vary PRR. $t_{w(data)} \geq 20$ ns, $t_{w(clock)} \geq 15$ ns.

B. $V_{ref} = 1.3V$.

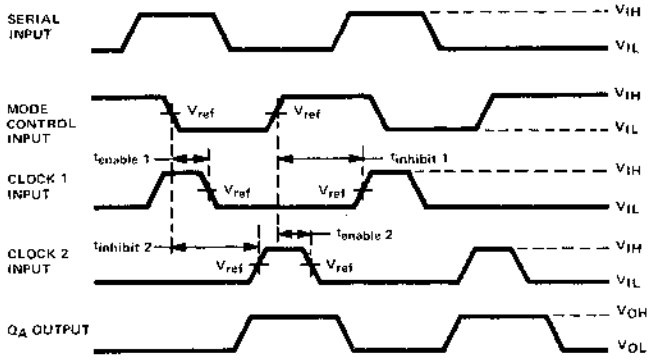


FIGURE 2 – CLOCK ENABLE/INHIBIT TIMES

NOTES:

A. Input A is at a low level.

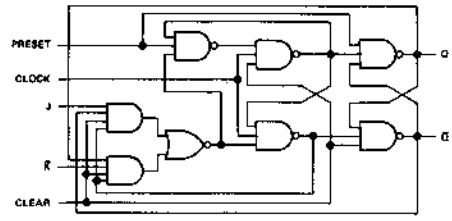
B. $V_{ref} = 1.3V$.

DESCRIPTION

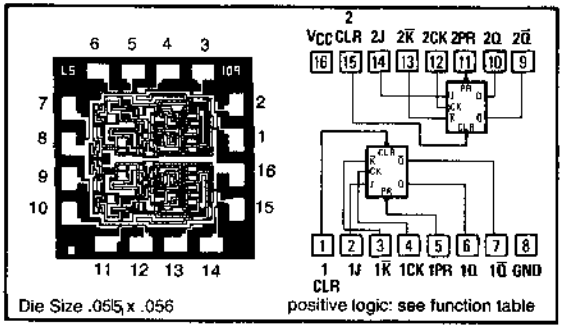
This monolithic dual J-$\overline{K}$ edge-triggered flip-flop features individual J, $\overline{K}$, clock, preset, and clear inputs. A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs.

The J and $\overline{K}$ data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and $\overline{K}$ inputs together.

LOGIC DIAGRAM (½)



PIN-OUT DIAGRAM



Die Size .055 x .056

positive logic: see function table

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
TOGGLE: each output changes to the complement of its previous level on each ↑ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			20	
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		17			17			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			15			ns
Input setup time t_{setup}		15			15			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the clock transition in order to insure recognition. This device requires no hold time.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	J or $\overline{K}$	V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
	clock or preset					0.2			0.2	
	Clear					0.4			0.4	
I_{IH}	J or $\overline{K}$	V_{CC}=MAX, V_I=2.7V				20			20	μA
	clock or preset					40			40	
	Clear					80			80	
I_{IL}	J or $\overline{K}$	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	clock or preset					−0.8			−0.8	
	Clear					−1.6			−1.6	
I_{OS}†		V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††		V_{CC}=MAX,			4	8		4	8	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		−55°C			+25°C			+125°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A on page 2-174)											
t_{PLH}			12	18		10	15		16	23	ns
t_{PHL}	CK Low		22	29		12	18		21	28	ns
	CK High		29	39		16	24		27	38	
t_{PLH}			13	20		12	18		13	20	ns
t_{PHL}			17	27		14	22		15	24	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A on page 2-174)											
t_{PLH}			16	22		13	19		19	26	ns
t_{PHL}	CK Low		26	33		21	27		24	31	ns
	CK High		33	44		29	38		30	41	ns
t_{PLH}			17	24		15	22		16	25	ns
t_{PHL}			22	31		18	26		19	29	ns

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

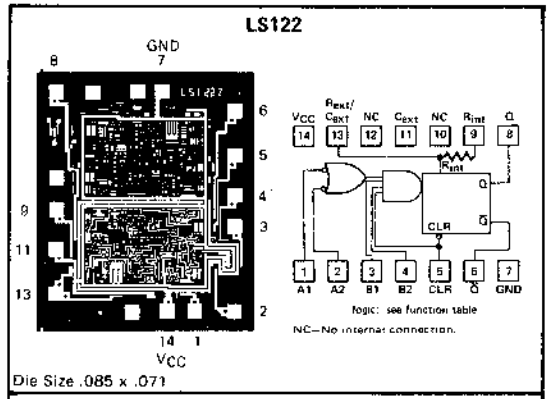
t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the clock transition in order to insure recognition. This device requires no hold time.

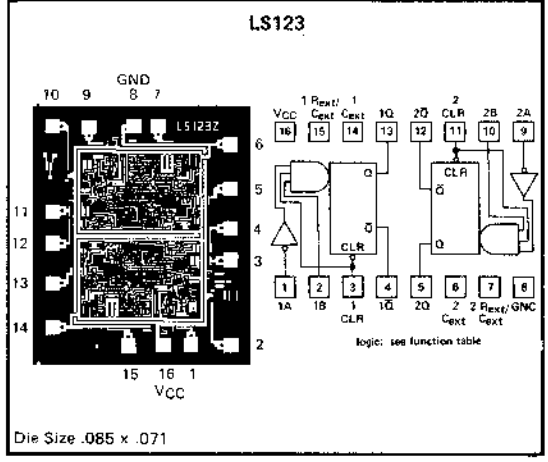
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Single and Dual Retriggerable Monostable Multivibrators with Clear

FEATURES

- Functionally and Mechanically Identical to 54122 and 54123
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Low Power Dissipation:
  - 'LS122 . . . 30 mW Typical
  - 'LS123 . . . 60 mW Typical
- Compensated for V_{CC} and Temperature Variations
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- 'LS122 Has Internal 10 kΩ Timing Resistor
- Diode-Clamped Inputs
- Compatible for Use with TTL or DTL





DESCRIPTION

The 'LS122 and 'LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.

'LS122 FUNCTION TABLE
(SEE NOTE 1)

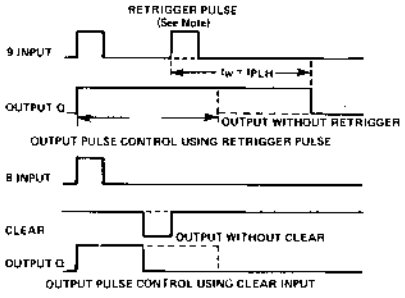
INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎍
H	L	X	H	↑	⎍	⎍
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎍
H	X	L	H	↑	⎍	⎍
H	H	↓	H	H	⎍	⎍
H	↓	↓	H	H	⎍	⎍
H	↓	H	H	H	⎍	⎍
↑	L	X	H	H	⎍	⎍
↑	X	L	H	H	⎍	⎍

'LS123 FUNCTION TABLE
(SEE NOTE 1)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

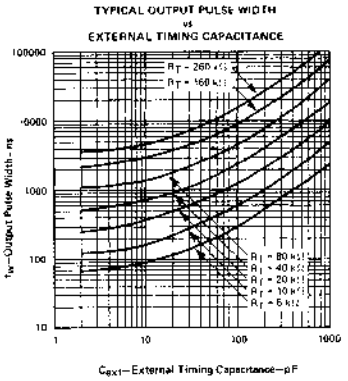
RAYTHEON

NOTES: 1. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, H = one high-level pulse, L = one low-level pulse, X = irrelevant (any input, including transitions).
2. To use the internal timing resistor of 'LS122, connect R_{int} to V_{CC}.
3. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
4. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
5. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.



NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 1—Typical Input/Output Pulses



†These values of resistance exceed the maximum recommended for use over the full temperature range of the 9LS/54LS' circuits.

FIGURE 2

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The 'LS122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.4 \cdot R_T \cdot C_{ext}$$

where

R_T is in kΩ (either internal or external timing resistor),
C_{ext} is in pF,
t_w is in ns.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 2.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–400			–400	μA
Low-level output current, I_{OL}				4			8	mA
Pulse width, t_w	A or B inputs high	40			40			ns
	A or B inputs low	40			40			
	Clear low	40			40			
External timing resistance, R_{ext}		5		225	5		360	kΩ
External capacitance, C_{ext}		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		–55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†			9LS/54LS			9LS/74LS			Unit
					Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−150	−30		−150	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 2	'LS122		6	11		6	11	mA
				'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k C_{ext} = 0pf, R_{ext} = 5.0kΩ (See Fig. 3, page 2-61 and Fig. A, page 2-174)												
t_{PLH}	A	Q		25	37		22	33		25	37	ns
	B			32	48		29	44		32	48	
t_{PHL}	A	$\overline{Q}$		33	49		30	45		33	49	ns
	B			40	61		37	56		40	61	
t_{PHL}	clear	Q		21	31		18	27		21	31	ns
t_{PLH}		$\overline{Q}$		33	50		30	45		33	50	ns
t_{wQ}(min)	A or B	Q		140	250		116	200		140	250	ns
*t_{wQ}	A or B	Q	—	—	—	4.0	4.5	5.0	—	—	—	μs
Test Conditions: C_L = 50pF, R_L = 2.0k, C_{ext} = 0pf, R_{ext} = 5.0kΩ (See Fig. 3, page 2-61 and Fig. A, page 2-174)												
t_{PLH}	A	Q		30	43		26	38		30	43	ns
	B			37	54		33	49		37	54	
t_{PHL}	A	$\overline{Q}$		38	55		34	50		38	55	ns
	B			45	67		41	62		45	67	
t_{PHL}	clear	Q		26	37		22	32		26	37	ns
t_{PLH}		$\overline{Q}$		39	55		35	50		39	55	ns
t_{wQ}(min)	A or B	Q		155	270		127	240		155	270	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

*For this test R_{ext} = 10kΩ, C_{ext} = 1000pF.

TYPICAL APPLICATION DATA

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leqslant 1000$ pF.

When $C_{ext} \geqslant 1000$ pF, the output pulse width is defined as:

$$t_w = 0.45 \bullet R_T \bullet C_{ext}$$

where

R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

t_w is in nanoseconds

For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.

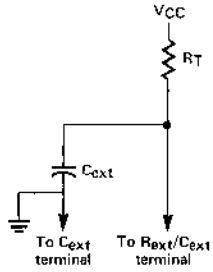
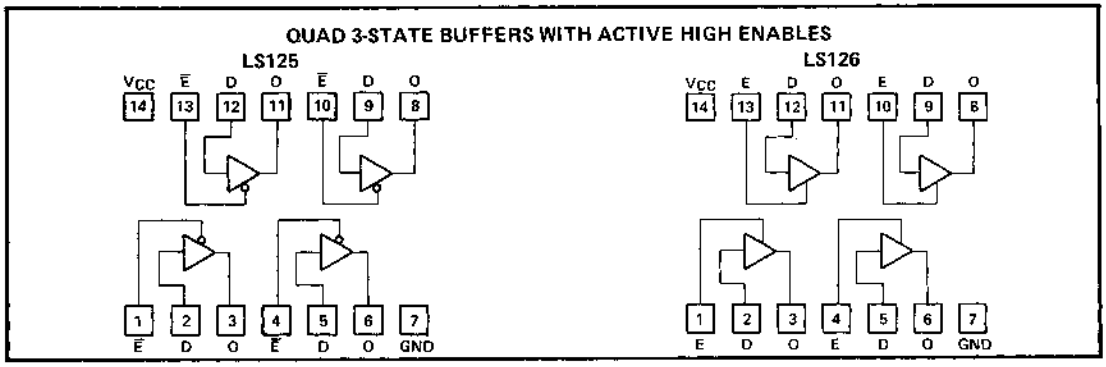


FIGURE 3
TIMING COMPONENT CONNECTIONS

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES



Recommended Operating Conditions.

	9LS/54LS			9LS/74LS			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
High Level Output I_{OH}			−1.0		−1.0	−2.6	mA
Low Level Output I_{OL}			12		12	24	mA
Operating Free Air Temperature	−55		+125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions		9LS/54LS			9LS/74LS			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH} Input HIGH Voltage		Guaranteed Input HIGH Voltage for All Inputs		2.0			2.0			V
V_{IL} Input LOW Voltage		Guaranteed Input LOW Voltage for All Inputs				0.7			0.8	V
V_{CD} Input Clamp Diode Voltage		V_{CC} = MIN, I_{IN} = −18mA			−0.65	−1.5			−1.5	V
V_{OH} Output HIGH Voltage		I_{OH} = −1.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or	2.4	3.4					V
		I_{OH} = −2.6mA	V_{IL} per Truth Table					2.4	3.1	V
V_{OL} Output LOW Voltage		I_{OL} = 12mA	V_{CC} = MIN, V_{IN} = V_{IH} or		0.25	0.4		0.25	0.4	V
		I_{OL} = 24mA	V_{IL} per Truth Table					0.35	0.5	V
I_{OZH} Output Off Current HIGH		V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}				20			20	μA
I_{OZL} Output Off Current LOW		V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}				−20			−20	μA
I_{IH} Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20			20	μA
		V_{CC} = MAX, V_{IN} = 10V				0.1			0.1	mA
I_{IL} Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V				−0.4			−0.4	mA
I_{OS} Output Short Circuit Current (Note 3)		V_{CC} = MAX, V_{OUT} = 0V		−15		−100	−15		−100	mA
I_{CC} Power Supply Current, Outputs LOW	LS125	V_{CC} = MAX, V_{IN} = 0V, $V_{\bar{E}}$ = 0V				16			16	mA
	LS126	V_{CC} = MAX, V_{IN} = 0V, V_E = 4.5V				20			20	mA
I_{CC} Power Supply Current, Outputs Off	LS125	V_{CC} = MAX, V_{IN} = 0V, V_E = 4.5V				20			20	mA
	LS126	V_{CC} = MAX, V_{IN} = 0V, V_E = 0V				24			24	mA

NOTES: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameters	From * (Input)	To (Output)	9LS/54LS									Units
			-55°C			+25°C			+125°C			
			Min	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667Ω (See Fig. C, page 2-174)												
t_{PLH}	D	O		10	15		6	10		10	14	ns
t_{PHL}	D	O		13	20		10	16		13	20	ns
t_{PZH}	$\overline{E}$ or E	O		13	20		10	16		13	20	ns
t_{PZL}	$\overline{E}$ or E	O		13	20		10	16		13	20	ns
Test Conditions: C_L = 5pF, R_L = 667Ω (See Fig. C, page 2-174)												
t_{PLZ}	$\overline{E}$ or E	O		13	19		10	15		13	20	ns
t_{PHZ}	$\overline{E}$ or E			13	27		15	23		18	27	ns
Test Conditions: C_L = 45pF, R_L = 667Ω (See Fig. C, page 2-174)												
t_{PLH}	D	O		13	20		10	15		13	19	ns
t_{PHL}	D	O		18	25		15	21		18	25	ns
t_{PZH}	$\overline{E}$ or E	O		18	25		15	21		18	25	ns
t_{PZL}	$\overline{E}$ or E	O		18	25		15	21		18	25	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

*For LS125 use $\overline{E}$ and for LS126 use E.

TRUTH TABLES

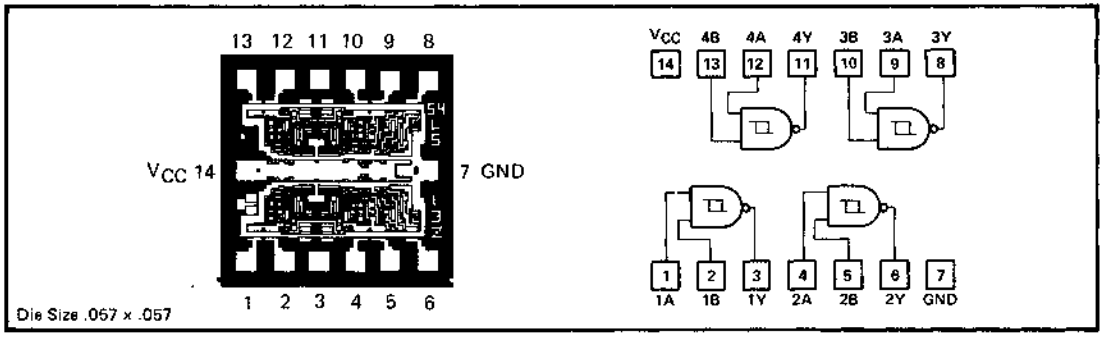
9LS125

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

9LS126

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage, V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	V
High level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		+125			70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†	9LS/54LS			9LS/74LS			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V	0.5	0.8	1.0	0.5	0.8	1.0	V
	Hysteresis (V_{T+}-V_{T-})	V_{CC} = 5V	0.4	0.8		0.4	0.8		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = -18mA		-0.65	-1.5		-0.65	-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = MAX, V_I = V_{T-}MIN	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = V_{T+}MAX, I_{OL} = MAX		0.25	0.40		0.35	0.50	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5V, V_I = V_{T+}		-0.14			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5V, V_I = V_{T-}		-0.18			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_{IL} = 0.4V			-0.4			-0.4	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX	-15		-100	-15		-100	mA
I_{CCH}	Supply Current High	V_{CC} = MAX, V_{IN} = 0V		8.6	16		8.6	16	mA
I_{CCL}	Supply Current Low	V_{CC} = MAX, V_{IN} = 4.5V		12	21		12	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS									Units
			−55°C			+25°C			+125°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k (See Fig. A, page 2-174)												
t_{PLH}	A or B	Y		16	24		13	20		16	24	ns
t_{PHL}				16	24		13	20		16	24	ns
Test Conditions: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174)												
t_{PLH}	A or B	Y		20	29		17	25		20	29	ns
t_{PHL}				20	29		17	25		20	29	ns

PARAMETER MEASUREMENT INFORMATION

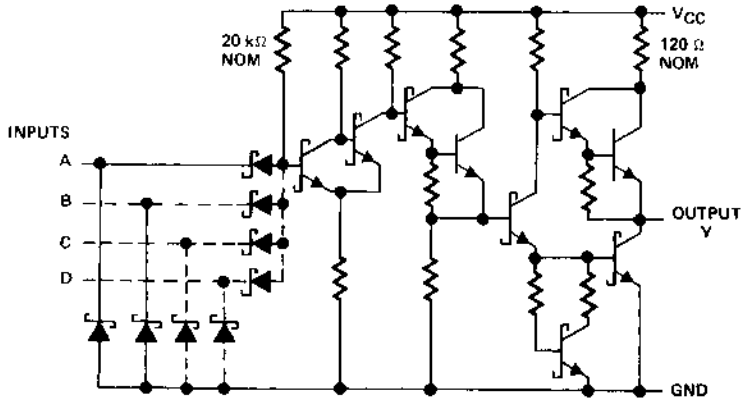
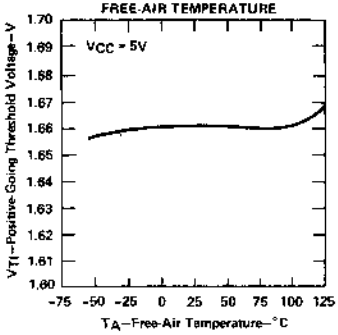


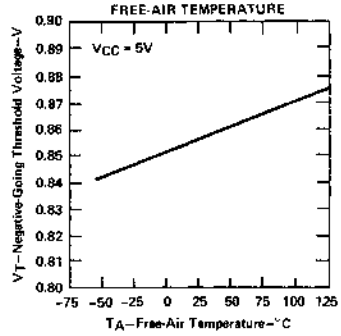
FIGURE 1

TYPICAL CHARACTERISTICS

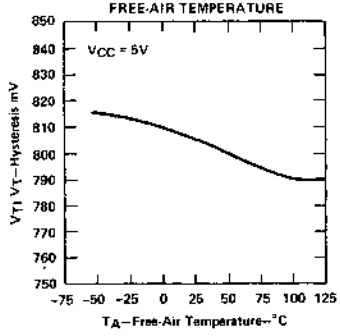
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



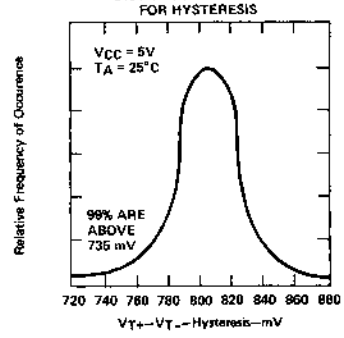
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



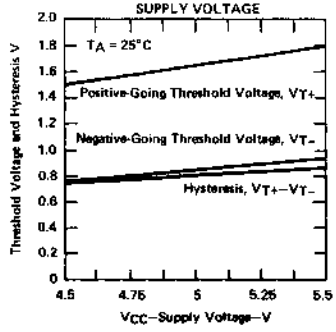
HYSTERISIS
vs
FREE-AIR TEMPERATURE



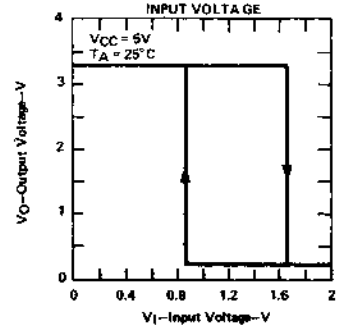
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

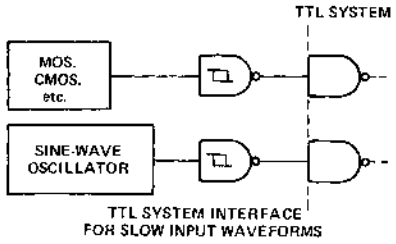


OUTPUT VOLTAGE
vs
INPUT VOLTAGE

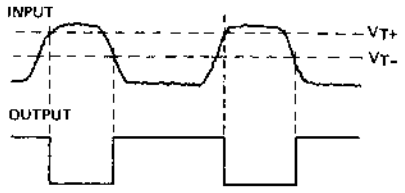


RAYTHEON

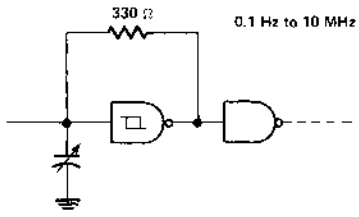
TYPICAL APPLICATIONS DATA



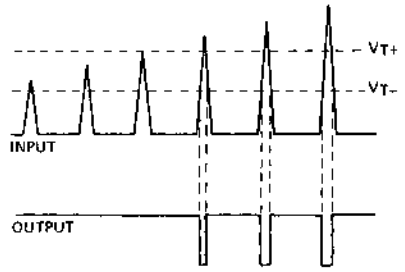
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



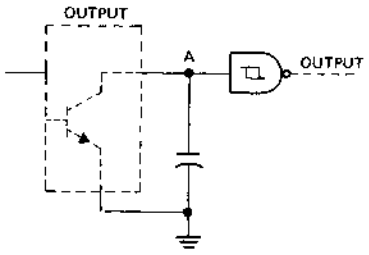
PULSE SHAPER

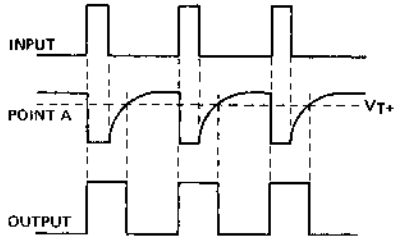


MULTIVIBRATOR



THRESHOLD DETECTOR



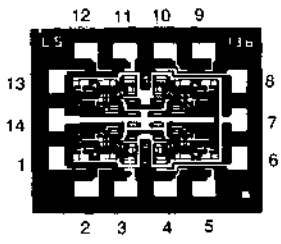


PULSE STRETCHER

Quadruple 2-Input Exclusive-OR, -NOR Gates With Open-Collector Outputs

PIN-OUT AND LOGIC DIAGRAMS

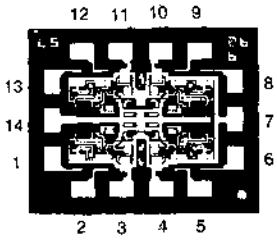
LS136
QUADRUPLE 2-INPUT EXCLUSIVE-OR WITH OPEN-COLLECTOR OUTPUTS



Die Size .045 x .056

positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR WITH OPEN COLLECTOR OUTPUTS



Die Size .045 x .056

positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\overline{B}$

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
I_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, V_{OH}=5.5V				100			100	μA
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I		V_{CC}=MAX, V_I=7V				0.2			0.2	mA
I_{IH}		V_{CC}=MAX, V_I=2.7V				40			40	μA
I_{IL}		V_{CC}=MAX, V_I=0.4V				−0.8			−0.8	mA
I_{CC}†	LS266	V_{CC}=MAX,			8	13		8	13	mA
	LS136				6.1	10		6.1	10	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure B on page 2-174)												
t_{PLH}	A or B	Other input low		14	18		13	17		20	26	ns
t_{PHL}				10	16		9	14		10	16	
t_{PLH}	A or B	Other input high		12	16		13	17		8	12	ns
t_{PHL}				10	16		18	13		7	12	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure B on page 2-174)												
t_{PLH}	A or B	Other input low		31	35		30	35		36	42	ns
t_{PHL}				16	23		13	19		14	21	
t_{PLH}	A or B	Other input high		30	35		31	36		35	41	ns
t_{PHL}				19	23		13	19		13	19	

Note: AC specification shown under −55°C and +125°C *are* for 9LS devices only. All 50pF specifications are for 9LS only.

FEATURES

- **LS138: 3-Line-to-8-Line Decoder**
  1-of-8 Demultiplexer
- **LS139: Dual 2-Line-to-4-Line Decoder**
  Dual 1-of-4 Demultiplexer
- **LS138 is expandable to 5-lines-to-32-lines decoder using 4 LS138's and one inverter.**

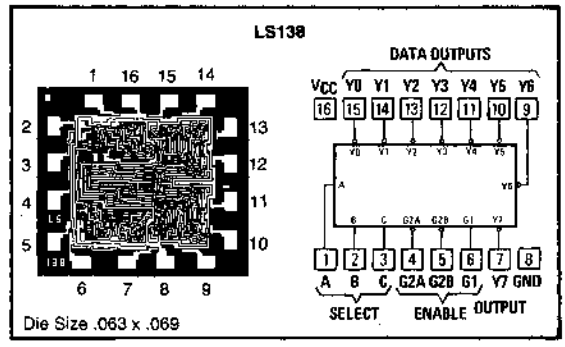
DESCRIPTION

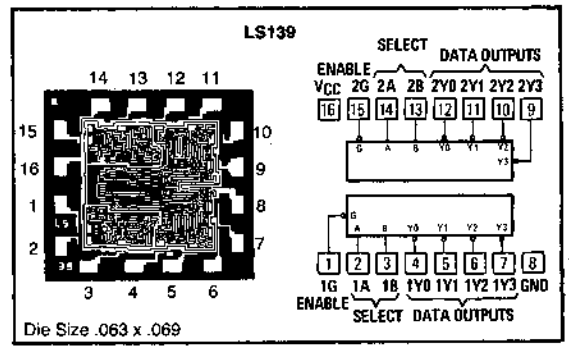
The LS138 decodes one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

These circuits are designed to be used in high-performance memory-decoding and data-routing applications requiring very short delay times.

PIN-OUT DIAGRAMS





LS138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

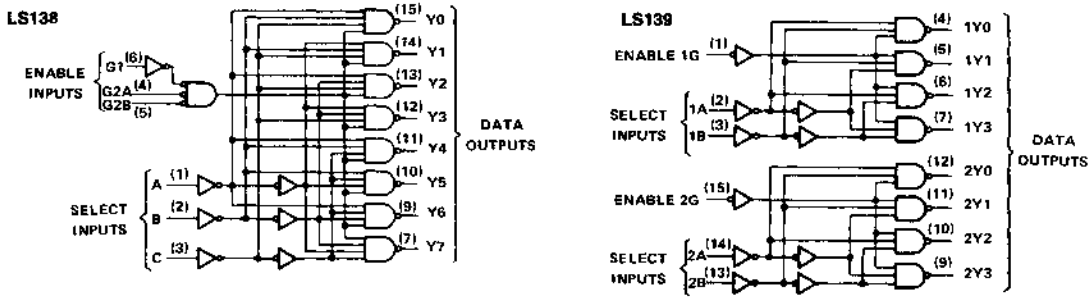
H = high level, L = low level, X = don't care

LS139
FUNCTION TABLE (½)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

LOGIC DIAGRAMS



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}	V_{CC}=MAX, Outputs enabled and open	LS138		6.3	10		6.3	10	mA
		LS139		6.8	11		6.8	11	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

LS138

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	Levels of Delay	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	Binary Select	Any		11	16		10	15		13	18	ns
t_{PHL}					17	24		17	24		21	27	ns
t_{PLH}	3				16	22		16	21		21	28	ns
t_{PHL}					22	30		21	28		24	32	ns
t_{PLH}	2	Enable	Any		11	16		10	15		13	18	ns
t_{PHL}					19	26		18	25		23	30	ns
t_{PLH}	3				16	22		16	22		21	27	ns
t_{PHL}					22	30		20	28		24	31	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	Binary Select	Any		13	19		12	17		14	20	ns
t_{PHL}					23	31		22	29		26	33	ns
t_{PLH}	3				17	24		17	23		23	29	ns
t_{PHL}					26	35		25	32		28	36	ns
t_{PLH}	2	Enable	Any		11	16		12	18		15	20	ns
t_{PHL}					23	30		24	33		26	34	ns
t_{PLH}	3				18	24		18	23		24	30	ns
t_{PHL}					26	34		24	32		28	37	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

LS139

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	Levels of Delay	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	Binary Select	Any		12	21		12	17		13	20	ns
t_{PHL}					13	21		12	17		13	20	ns
t_{PLH}	3				16	28		15	22		17	27	ns
t_{PHL}					18	30		17	25		18	30	ns
t_{PLH}	2	Enable	Any		12	22		11	15		11	22	ns
t_{PHL}					11	22		11	16		12	22	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	Binary Select	Any		15	26		15	21		16	25	ns
t_{PHL}					16	26		15	21		16	25	ns
t_{PLH}	3				19	33		18	26		20	32	ns
t_{PHL}					21	35		20	29		21	35	ns
t_{PLH}	2	Enable	Any		15	27		14	19		14	27	ns
t_{PHL}					14	27		14	20		15	27	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

FEATURES

- Select one of eight data sources
- Perform parallel-to-serial conversion
- LS151 has complementary outputs; LS152 has inverting output only
- LS151 has strobe input

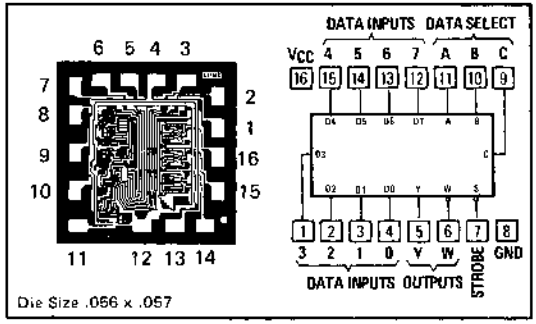
DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources. The LS151 has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output low.

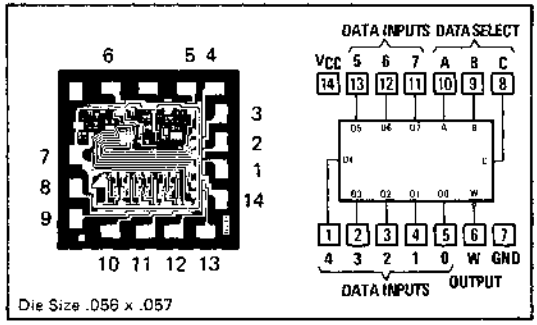
The LS151 features complementary W and Y outputs whereas the LS152 has an inverted (W) output only.

PIN-OUT DIAGRAMS

LS151



LS152



LS151
FUNCTION TABLE

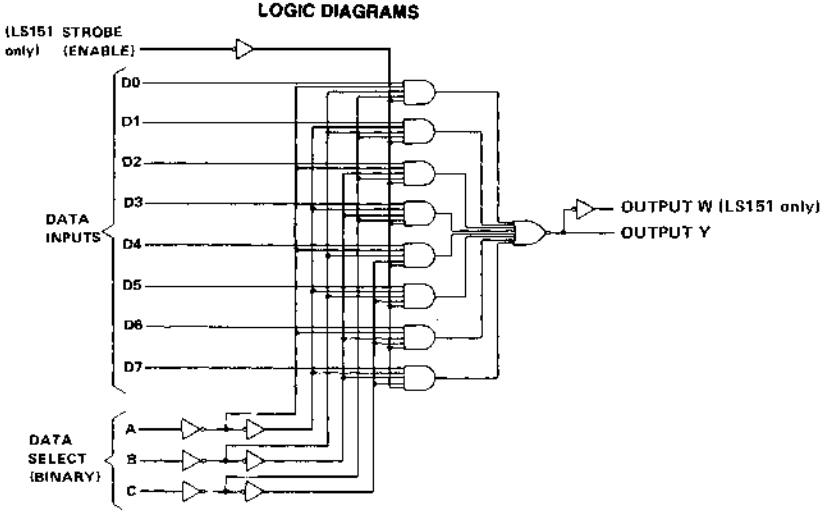
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

LS152
FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

H = high level, L = low level, X = don't care
D0, D1 . . . D7 = the level of the D respective input

LOGIC DIAGRAMS



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OH}=−400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.3	0.45		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}	V_{CC}=MAX, Outputs open, All inputs at 4.5V	LS151		6.0	10		6.0	10	mA
		LS152		5.6	9		5.6	9	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max*	Min	Typ	Max*	Min	Typ	Max*	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, or C (4 levels)	W (54LS151 only)		15	22		15	22		18	25	ns
t_{PHL}				19	26		18	25		20	26	
t_{PLH}	A, B, or C (3 levels)	Y		24	32		24	31		29	36	ns
t_{PHL}				21	30		20	28		22	31	
t_{PLH}	Strobe	W (54LS151 only)		12	17		11	17		13	19	ns
t_{PHL}				13	20		13	19		14	20	
t_{PLH}	Strobe	Y (54LS151 only)		18	26		18	26		21	29	ns
t_{PHL}				18	27		16	24		17	25	
t_{PLH}	Any D	W (54LS151 only)		8	13		9	14		11	17	ns
t_{PHL}				6	12		5	12		6	13	
t_{PLH}	Any D	Y		11	18		11	17		13	19	ns
t_{PHL}				14	22		14	20		15	22	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, or C (4 levels)	W (54LS151 only)		17	24		17	24		20	27	ns
t_{PHL}				22	31		21	29		22	31	
t_{PLH}	A, B, or C (3 levels)	Y		26	33		26	32		29	38	ns
t_{PHL}				27	37		25	35		29	38	
t_{PLH}	Strobe	W (54LS151 only)		14	20		13	19		15	21	ns
t_{PHL}				16	24		15	23		16	24	
t_{PLH}	Strobe	Y (54LS151 only)		20	28		20	27		23	30	ns
t_{PHL}				24	35		20	31		21	32	
t_{PLH}	Any D	W (54LS151 only)		9	15		10	16		13	19	ns
t_{PHL}				9	16		8	14		8	14	
t_{PLH}	Any D	Y		14	20		14	19		15	21	ns
t_{PHL}				19	30		18	27		20	29	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

*Tentative data, subject to change without notice

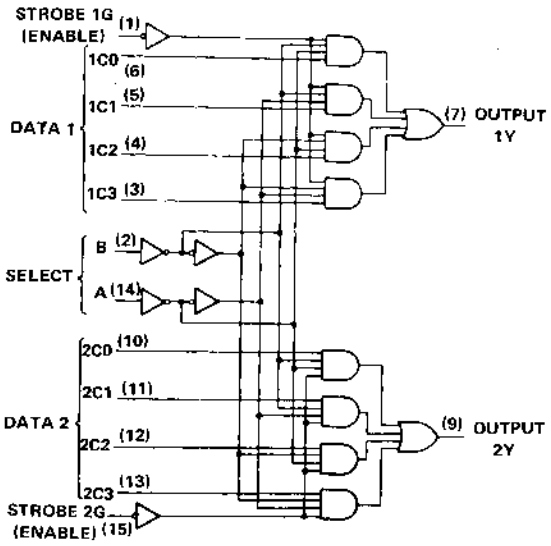
FEATURES

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (Enable) line provided for cascading (N lines to n lines)
- Non-inverting

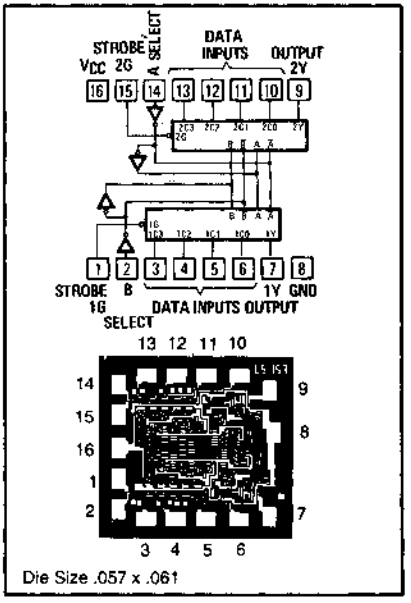
DESCRIPTION

The LS153 is a high speed Dual 4-Line-to-1-Line Multiplexer with common select inputs and separate strobe (enable) inputs for each half. Each half can select one bit of four and present it at the output in non-inverted form.

LOGIC DIAGRAM



PIN-OUT DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care

RAYTHEON

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.5	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CCL}††	V_{CC}=MAX			6.2	10		6.2	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CCL} is measured with the outputs open and all inputs grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Data	Y		8	13		8	13		11	16	ns
t_{PHL}	Data	Y		13	18		14	18		17	22	ns
t_{PLH}	Select	Y		15	21		17	22		22	28	ns
t_{PHL}	Select	Y		17	23		16	21		21	26	ns
t_{PLH}	Strobe	Y		14	20		16	21		21	26	ns
t_{PHL}	Strobe	Y		17	23		16	21		20	25	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Data	Y		10	15		10	15		15	22	ns
t_{PHL}	Data	Y		17	23		17	22		22	27	ns
t_{PLH}	Select	Y		18	24		19	24		25	30	ns
t_{PHL}	Select	Y		22	27		19	25		24	30	ns
t_{PLH}	Strobe	Y		17	23		18	23		23	28	ns
t_{PHL}	Strobe	Y		21	27		20	24		23	28	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Dual 2-Line-To-4-Line Decoders/Demultiplexers

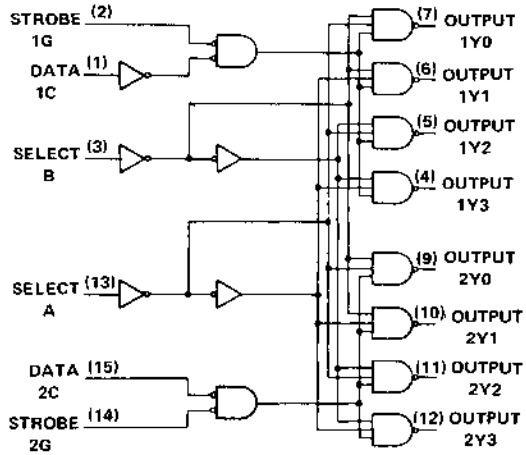
FEATURES

- LS156 has open-collector outputs
- Applications:
  - Dual 2-Line-to-4-Line Decoder
  - Dual 1-Line-to-4-Line Demultiplexer
  - 3-Line-to-8-Line Decoder
  - 1-Line-to-8-Line Demultiplexer

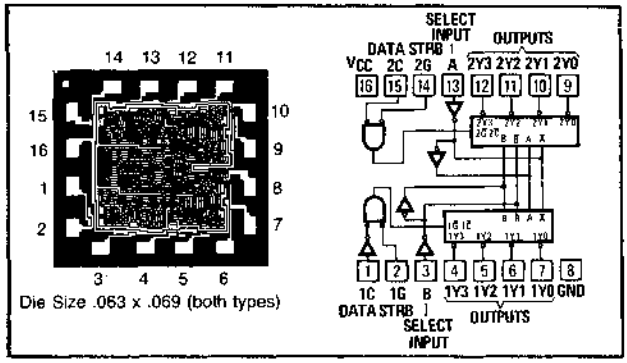
DESCRIPTION

These circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

LOGIC DIAGRAM



PIN-OUT DIAGRAM



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	I	H	H	H
I	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = don't care

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

	9LS/54LS			9LS/74LS			Unit
	Min	Typ**	Max	Min	Typ**	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Output voltage, V_{OH} (LS156 only)			5.5			5.5	V
Low-level output, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
I_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, V_{OH}=5.5V (LS156 only)				100			100	μA
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX			6.1	10		6.1	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.

LS155

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	Levels of Logic	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	2C, 1G, or 2G	Y		11	17		10	16		12	18	ns
t_{PHL}	2	2C, 1G, or 2G	Y		15	24		15	23		17	26	ns
t_{PLH}	3	A or B	Y		16	23		16	24		19	27	ns
t_{PHL}	3	A or B	Y		20	30		19	30		20	31	ns
t_{PLH}	3	1C	Y		15	21		15	22		19	26	ns
t_{PHL}	3	1C	Y		20	30		19	28		21	31	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	2	2C, 1G, or 2G	Y		13	19		13	19		15	21	ns
t_{PHL}	2	2C, 1G, or 2G	Y		21	29		18	26		22	31	ns
t_{PLH}	3	A or B	Y		18	25		18	25		22	29	ns
t_{PHL}	3	A or B	Y		26	36		22	30		26	36	ns
t_{PLH}	3	1C	Y		18	23		18	24		22	29	ns
t_{PHL}	3	1C	Y		25	35		23	31		25	35	ns

LS156

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

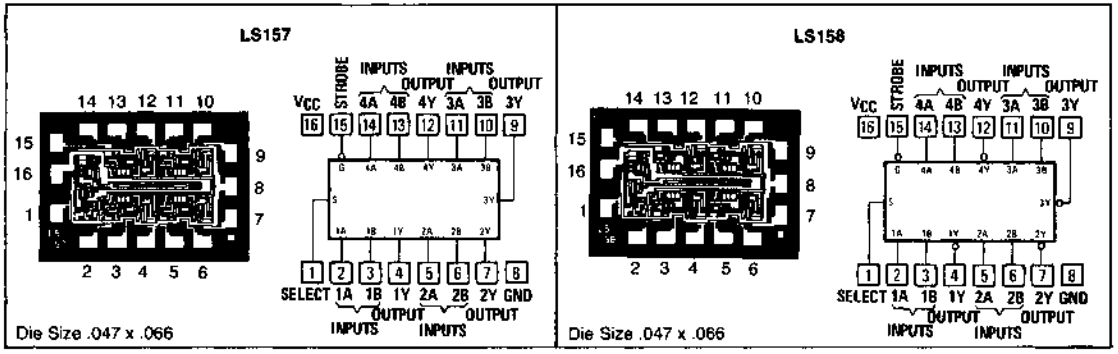
Parameter	Levels of Logic	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. B, page 2-174)													
t_{PLH}	2	2C, 1G, or 2G	Y		24	34		22	30		24	34	ns
t_{PHL}	2	2C, 1G, or 2G	Y		18	27		16	24		18	27	ns
t_{PLH}	3	A or B	Y		29	40		27	37		29	40	ns
t_{PHL}	3	A or B	Y		24	34		22	30		24	34	ns
t_{PLH}	3	1C	Y		27	38		25	34		27	38	ns
t_{PHL}	3	1C	Y		25	35		23	31		25	35	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. B, page 2-174)													
t_{PLH}	2	2C, 1G, or 2G	Y		27	39		25	34		27	39	ns
t_{PHL}	2	2C, 1G, or 2G	Y		21	32		19	28		21	32	ns
t_{PLH}	3	A or B	Y		32	45		30	41		32	45	ns
t_{PHL}	3	A or B	Y		27	39		25	34		27	39	ns
t_{PLH}	3	1C	Y		30	43		28	38		30	43	ns
t_{PHL}	3	1C	Y		28	40		26	35		28	40	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

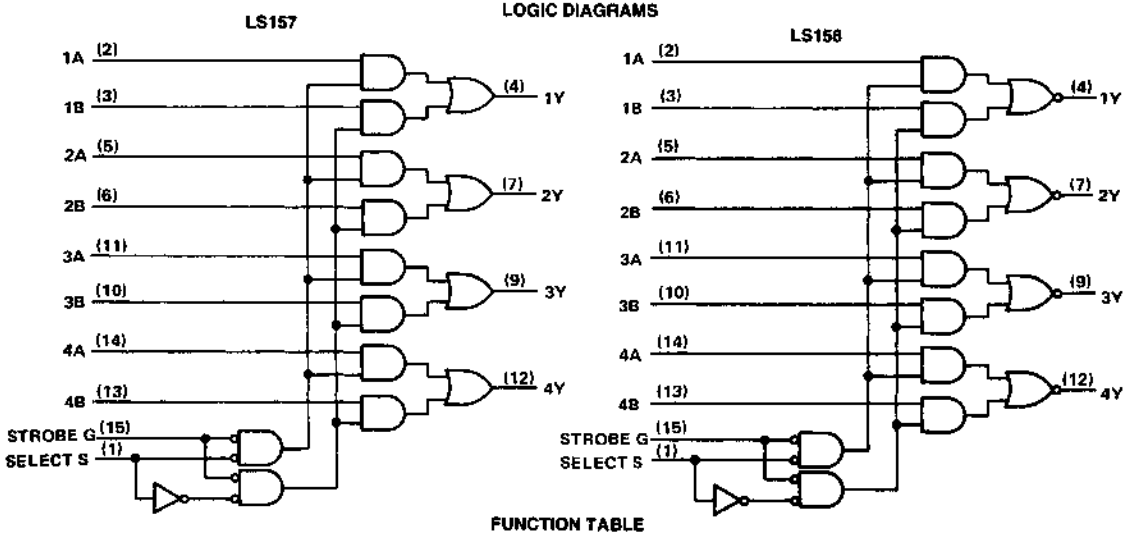
DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The LS157 presents true data; the LS158 presents inverted data.

PIN-OUT DIAGRAMS



LOGIC DIAGRAMS



FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	54LS157	54LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = don't care
Low level at S selects A inputs
High level at S selects B inputs
Strobe is active low

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	S or G input	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	A or B input					0.1			0.1	
I_{IH}	S or G input	V_{CC}=MAX, V_I=2.7V				40			40	μA
	A or B input					20			20	
I_{IL}	S or G input	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
	A or B input					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX,	LS157		9.7	16		9.7	16	mA
			LS158		4.8	8		4.8	8	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with 4.5V applied to all inputs and all outpus open.

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Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (Input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	LS157	Data	Y		6	11		5	10		9	16	ns
t_{PHL}					8	13		7	12		7	13	
t_{PLH}	LS158	Data	Y		6	11		6	11		8	14	ns
t_{PHL}					7	12		4	9		4	8	
t_{PLH}	LS157	Strobe	Y		10	16		10	16		16	22	ns
t_{PHL}					12	17		9	14		9	14	
t_{PLH}	LS158	Strobe	Y		10	16		9	14		10	15	ns
t_{PHL}					10	15		10	15		12	17	
t_{PLH}	LS157	Select	Y		11	17		11	17		16	24	ns
t_{PHL}					13	18		11	16		12	19	
t_{PLH}	LS158	Select	Y		10	16		10	16		13	20	ns
t_{PHL}					10	16		10	14		12	17	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	LS157	Data	Y		8	14		7	14		10	17	ns
t_{PHL}					11	16		9	15		10	16	
t_{PLH}	LS158	Data	Y		7	13		8	13		10	16	ns
t_{PHL}					10	16		7	13		7	12	
t_{PLH}	LS157	Strobe	Y		12	17		12	17		18	25	ns
t_{PHL}					15	20		12	17		13	18	
t_{PLH}	LS158	Strobe	Y		12	17		11	16		12	17	ns
t_{PHL}					14	19		13	18		15	21	
t_{PLH}	LS157	Select	Y		12	18		13	18		16	21	ns
t_{PHL}					15	21		14	19		14	20	
t_{PLH}	LS158	Select	Y		12	18		12	18		15	22	ns
t_{PHL}					14	19		13	18		15	21	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

FEATURES

- 4-bit synchronous counters
- Synchronously programmable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- Advanced low-power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

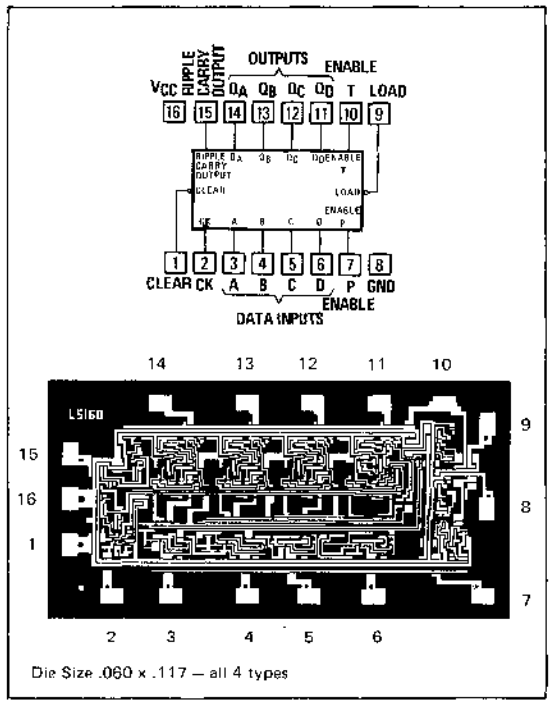
DESCRIPTION

The LS160, LS161, LS162 and LS163 synchronous, presettable counts have internal look-ahead carry and ripple carry output for high-speed counting applications. The LS160 and LS162 are decade counters and the LS161 and LS163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition.

The LS160 and LS161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The LS162 and LS163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection.

PIN-OUT DIAGRAM



Die Size .060 x .117 — all 4 types

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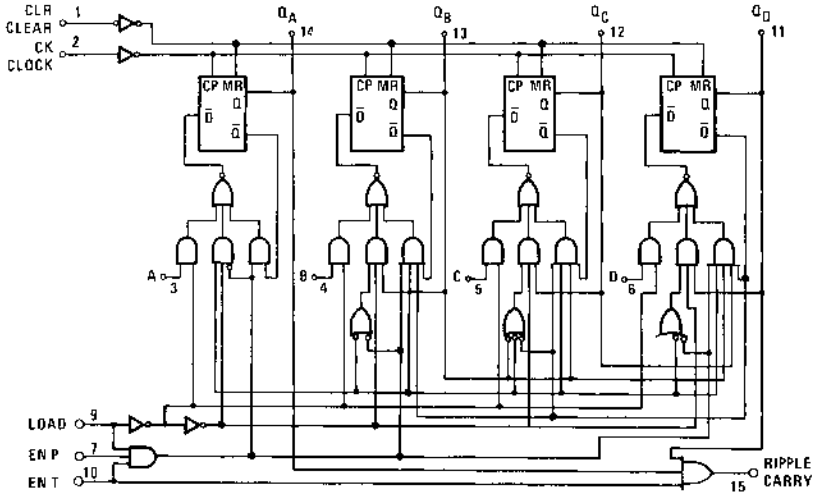
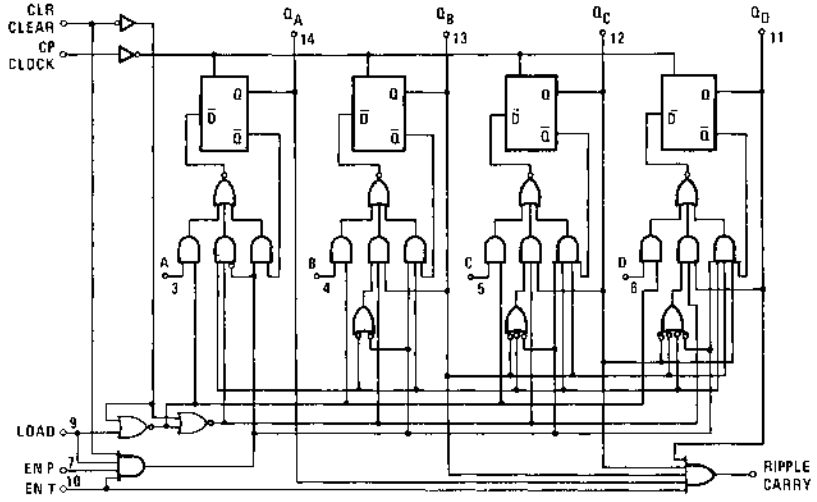
LOGIC DIAGRAMS

LS160 Synchronous Decade Counter



LS162 synchronous decade counters are similar; however, the clear is synchronous as shown for the LS163 binary counters.

LS163 SYNCHRONOUS BINARY COUNTER



LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the LS160 decade counters.

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5.0	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 3 and 4)	Data inputs A, B, C, D	0			0			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear◇	20			20			
Hold time, t_{hold}	Data inputs A, B, C, D	25¶			25			ns
	Other inputs	10¶			10			
Operating free-air temperature, T_A		-55		125	0		70	°C

◇ This applies only for LS162 and LS163, which have synchronous clear inputs.

¶ The minimum hold time is as specified or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max,	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_I	Data or enable P	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	Load, clock, or enable T					0.2			0.2	
	Clear (LS160,161)					0.1			0.1	
	Clear (LS162,163)					0.2			0.2	
I_{IH}	Data or enable P	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Load, clock, or enable T					40			40	
	Clear (LS160,161)					20			20	
	Clear (LS162,163)					40			40	
I_{IL}	Data or enable P	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Load, clock, or enable T					-0.8			-0.8	
	Clear (LS160,161)					-0.4			-0.4	
	Clear (LS162,163)					-0.8			-0.8	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CCH}		V_{CC}=MAX, See Note 1			18	31		18	31	mA
I_{CCL}		V_{CC}=MAX, See Note 2			19	32		19	32	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

NOTES:

1. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
2. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 and 2 and Notes 3 and 4 and Fig. A, page 2-174)												
f_{max}						30	40					MHz
t_{PLH}	Clock	Ripple carry		28	39		25	35		28	39	ns
t_{PHL}				23	39		20	35		23	39	
t_{PLH}	Clock (load input high)	Any Q		13	22		10	18		13	22	ns
t_{PHL}				18	24		15	20		18	24	
t_{PLH}	Clock (load input low)	Any Q		13	22		10	18		13	22	ns
t_{PHL}				18	24		14	20		18	24	
t_{PLH}	Enable T	Ripple carry		18	25		15	20		18	25	ns
t_{PHL}				13	18		9	14		13	18	
t_{PHL}	Clear	Any Q		17	32		14	28		17	32	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 and 2 and Notes 3 and 4 and Fig. A, page 2-174)												
t_{PLH}	Clock	Ripple carry		31	44		28	39		31	44	ns
t_{PHL}				26	44		23	39		26	44	
t_{PLH}	Clock (load input high)	Any Q		16	27		13	22		16	27	ns
t_{PHL}				21	29		18	24		21	29	
t_{PLH}	Clock (load input low)	Any Q		16	27		13	22		16	27	ns
t_{PHL}				21	29		17	24		21	29	
t_{PLH}	Enable T	Ripple carry		21	30		18	24		21	30	ns
t_{PHL}				16	23		12	18		16	23	
t_{PHL}	Clear	Any Q		20	37		17	32		20	37	ns

NOTES:

3. Propagation delay for clearing is measured from the clear input for the LS160 and LS161 or from the clock input transition for the LS162 and LS163.
4. AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

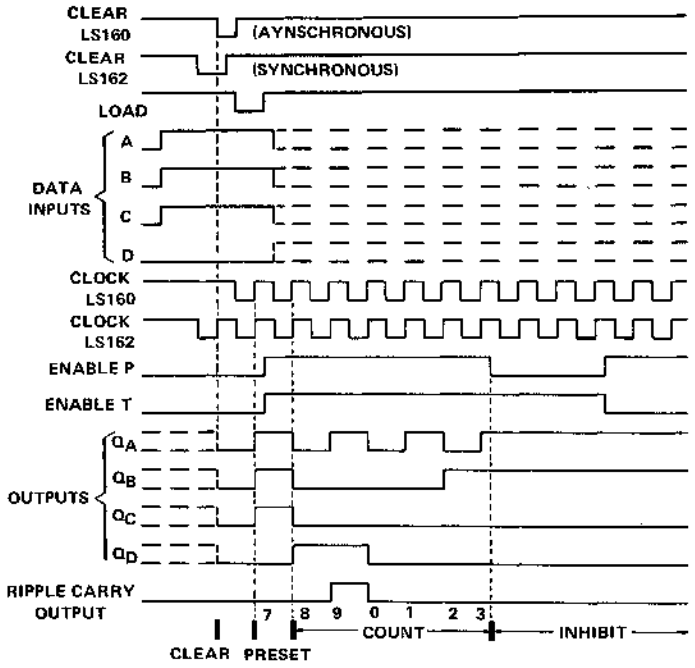


FIGURE 1

LS160, LS162

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

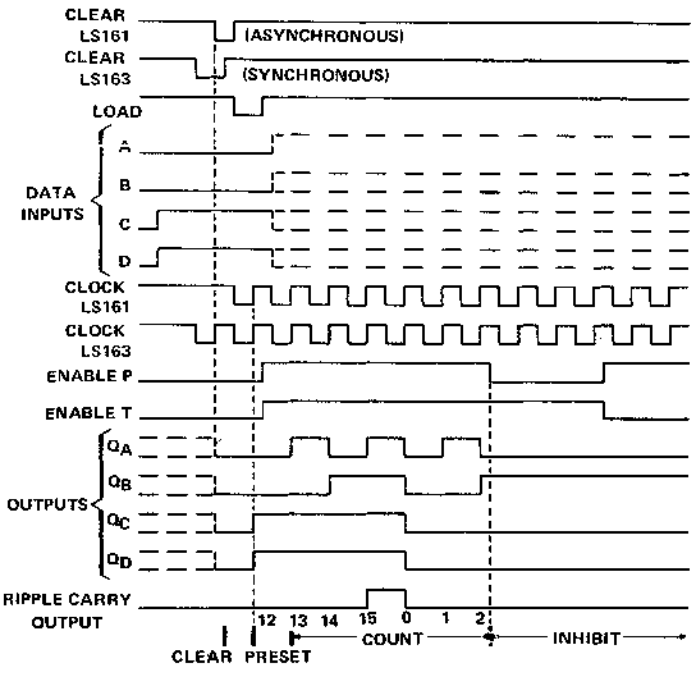


FIGURE 2

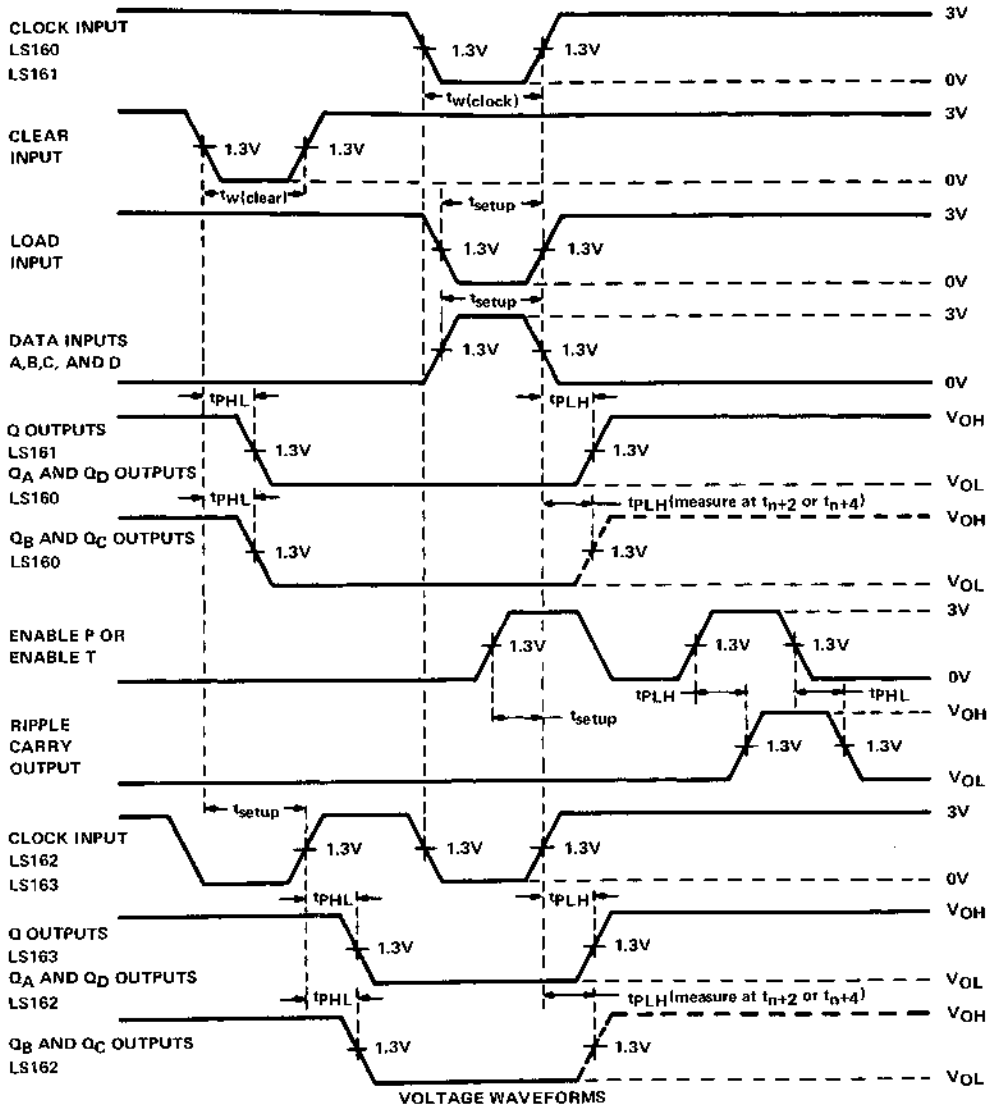
LS161, LS163

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen; fourteen fifteen, zero, one, and two
4. Inhibit

RAYTHEON

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

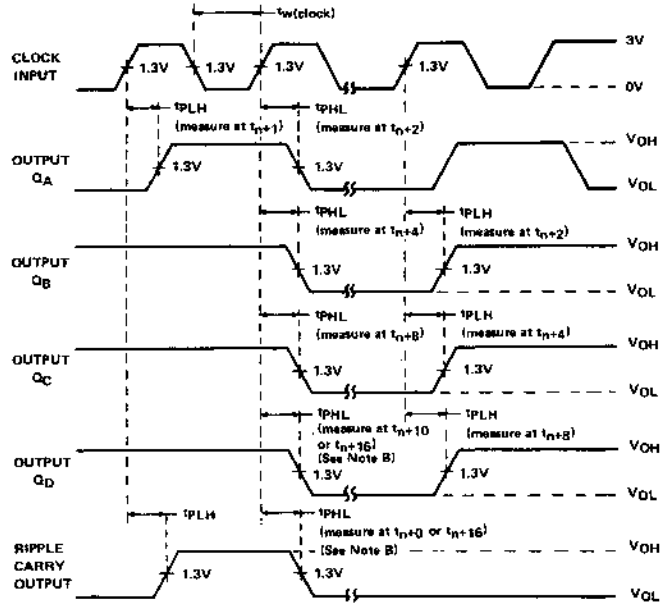
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at $t_n = 0$.

FIGURE 4

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

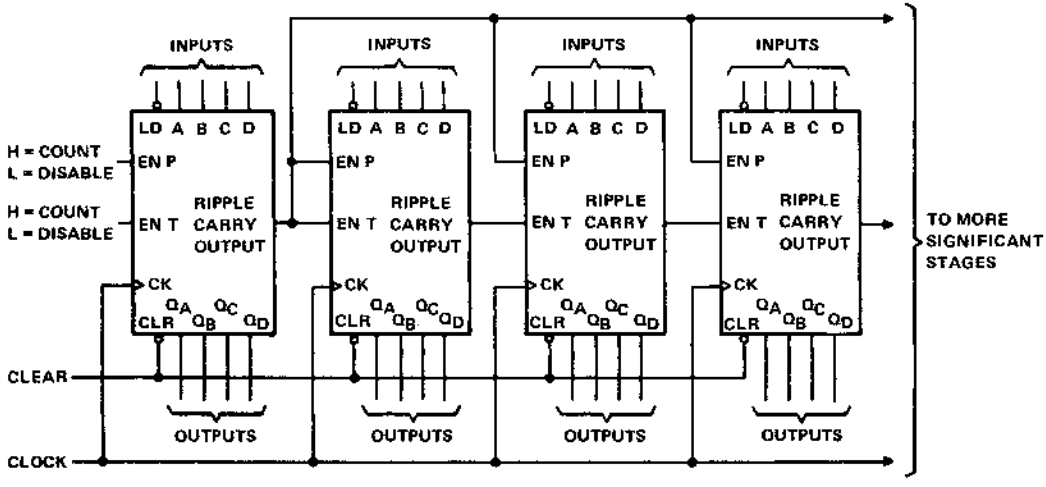
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$: $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} LS160, LS162, and at t_{n+16} for LS161, LS163 where t_n is the bit time when all outputs are low.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The LS160 or LS162 will count in BCD and the LS163 will count in binary. Virtually any count mode (modulo-N, N_1-to N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



RAYTHEON

FEATURES

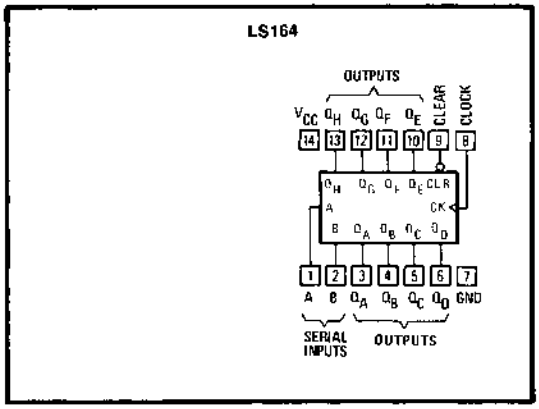
- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

DESCRIPTION

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

9LS/54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; 9LS/74LS devices are characterized for operation from 0°C to 70°C.

PIN-OUT DIAGRAM



FUNCTION TABLES

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B ... Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

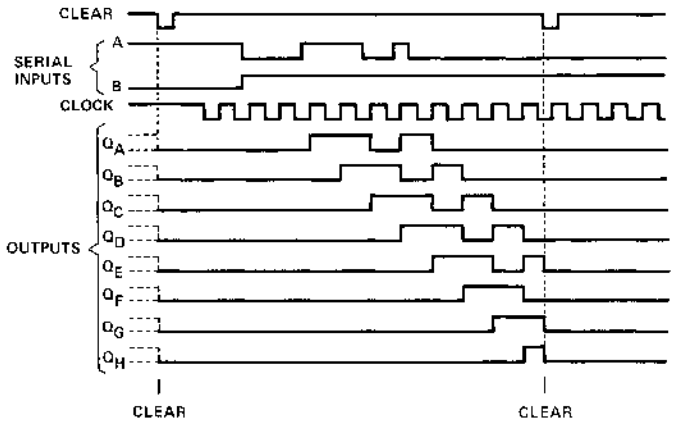
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

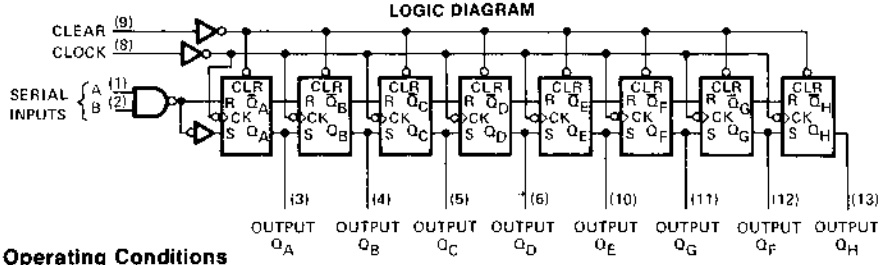
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



LOGIC DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	15			15			ns
Data hold time, t_{hold} (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}††	V_{CC}=MAX			16	27		16	27	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to clear.

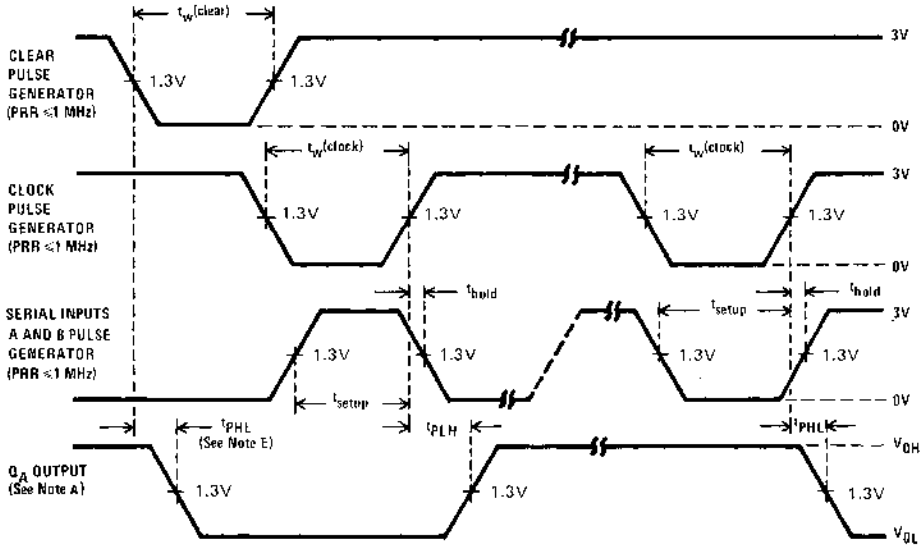
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1, page 2-95 and Fig. A, page 2-174)										
f_{max}				25	36					MHz
t_{PHL}		26	38		24	36		26	38	ns
t_{PLH}		20	30		17	27		20	30	ns
t_{PHL}		24	35		21	32		24	35	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1, page 2-95 and Fig. A, page 2-174)										
t_{PHL}		29	42		27	40		29	42	ns
t_{PLH}		23	34		20	31		23	34	ns
t_{PHL}		27	39		24	36		27	39	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.

B. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

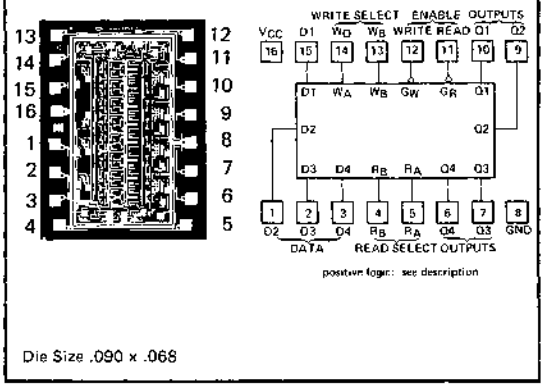
4-By-4 Register Files with Open-Collector Outputs

FEATURES

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
  - Scratch-Pad Memory
  - Buffer Storage between Processors
  - Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current: 20μA

PIN-OUT DIAGRAM

LS170



Die Size .090 x .068

DESCRIPTION

The 'LS170 MSI 16-bit TTL register file incorporates the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

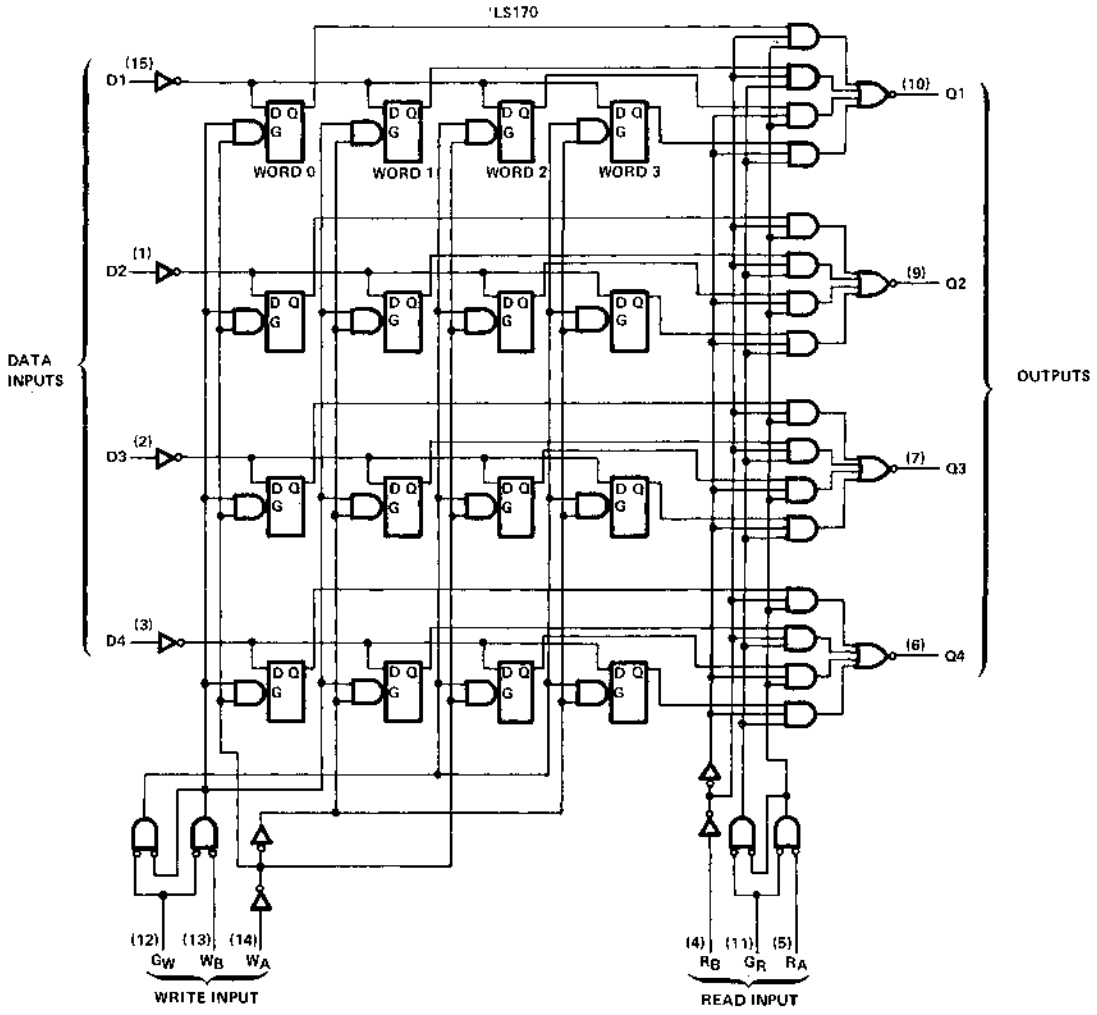
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 1 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 2)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 1. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

2. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		9LS/54LS			9LS/74LS			Unit
				Min.	Typ‡	Max.	Min.	Typ‡	Max.	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_I Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH} High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{OH} = 5.5V, V_{IH} = 2V			20			20	mA
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	Any D, R, or W	V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
	G_R or G_W					0.2			0.2	
I_{IH} High-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 2.7V			20			20	mA
	G_R or G_W					40			40	
I_{IL} Low-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
	G_R or G_W					−0.8			−0.8	
I_{CC} Supply current		V_{CC} = MAX,	See Note 3		25	40		25	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

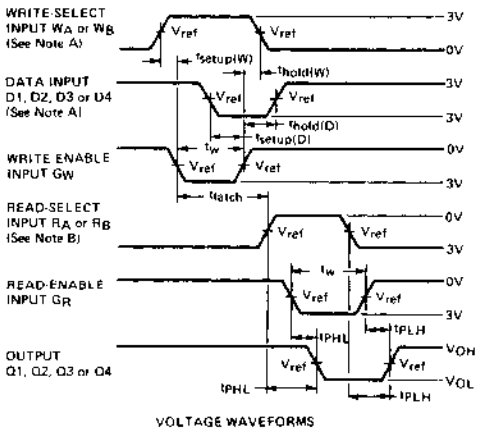
‡All typical values are at V_{CC} = 5V, T_A = 25°C.

NOTE 3. I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

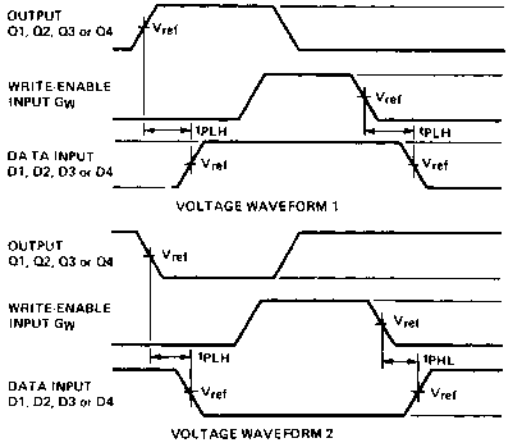
Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: R_L = 2.0k, C_L = 15pF, (See Figs. 1 and 2 and Fig. B, page 2-174)												
t_{PLH}	Read enable	Any Q		22	34		20	30		23	34	ns
t_{PHL}				22	34		20	30		23	34	
t_{PLH}	Read select	Any Q		26	44		25	40		28	44	ns
t_{PHL}				27	44		24	40		27	44	
t_{PLH}	Write enable	Any Q		33	49		30	45		33	49	ns
t_{PHL}				29	44		25	40		28	44	
t_{PLH}	Data	Any Q		32	49		30	45		33	49	ns
t_{PHL}				25	39		22	35		25	39	
Test Condition: R_L = 2.0k, C_L = 50pF, (See Figs. 1 and 2 and Fig. B, page 2-174)												
t_{PLH}	Read enable	Any Q		27	39		24	35		27	39	ns
t_{PHL}				27	39		24	35		27	39	
t_{PLH}	Read select	Any Q		32	49		29	45		32	49	ns
t_{PHL}				31	49		28	45		31	49	
t_{PLH}	Write	Any Q		37	54		34	50		37	54	ns
t_{PHL}				32	49		29	45		32	49	
t_{PLH}	Data	Any Q		37	54		34	50		37	54	ns
t_{PHL}				29	44		26	40		29	44	

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 1



VOLTAGE WAVEFORM 1

VOLTAGE WAVEFORM 2

FIGURE 2

NOTES: A. High-level input pulses at the select and data inputs are illustrated in Figure 1; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

D. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 15$ ns and $t_f \leq 6$ ns.

E. V_{ref} = 1.3 V.

FEATURES

- Positive edge-triggered common clock
- Asynchronous common reset
- Clock-to-output delays of 14 ns

DESCRIPTION

The LS174 is a six-bit register with single-rail outputs and the LS175 is a four-bit register with complementary outputs. Both consist of D-type flip-flops with a buffered common clock and an asynchronous, active-Low buffered clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

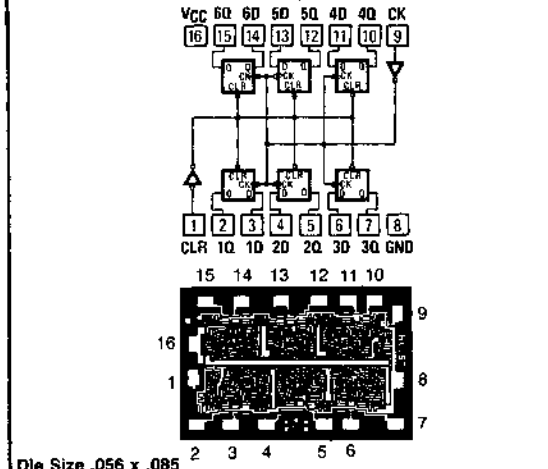
FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = LS175 only

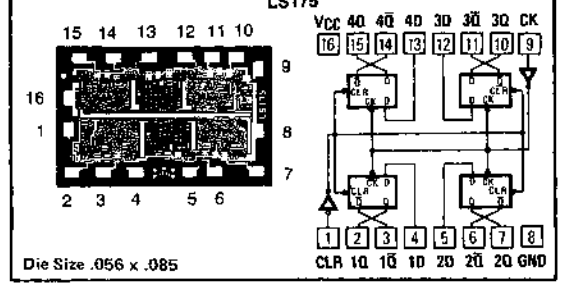
PIN-OUT DIAGRAMS

LS174



Die Size .056 x .085

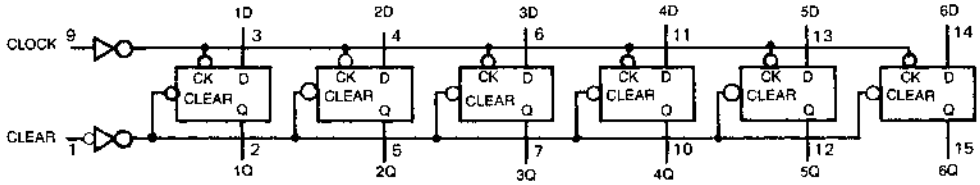
LS175



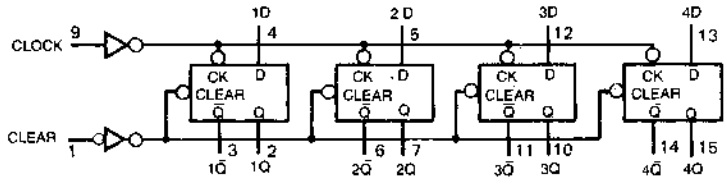
Die Size .056 x .085

LOGIC DIAGRAMS

LS174



LS175



RAYTHEON

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, t_w (Low)		15			15			ns
Width of clear pulse, t_w (Low)		20			20			ns
Setup time	Data input t_{setup}	10			10			ns
	Clear recovery, t_{rec}	12			12			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the data input prior to the rising edge of the clock in order to be recognized and transferred to the output.

t_{hold} is the minimum time required for the logic level to be maintained at the data input after the rising edge of the clock in order to insure recognition.

t_{rec} is the minimum time required between the end of the clear pulse and the rising edge of the clock in order to transfer High data to the Q output.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	LS174		16	26		16	26	mA
		LS175		11	18		11	18	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured, after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Figure A on page 2-174)												
f_{max}	maximum clock frequency					35	45					MHz
t_{PLH}	clear (LS175 only)	$\overline{Q}$		19	25		19	25		25	31	ns
t_{PHL}	clear (LS175 only)	Q		23	29		19	25		22	27	ns
t_{PLH}	clock	Q or $\overline{Q}$		14	20		13	17		14	19	ns
t_{PHL}	clock	Q or $\overline{Q}$		16	23		13	18		13	18	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Figure A on page 2-174)												
t_{PLH}	clear (LS175 only)	$\overline{Q}$		21	27		22	27		28	35	ns
t_{PHL}	clear (LS175 only)	Q		25	33		23	28		25	30	ns
t_{PLH}	clock	Q or $\overline{Q}$		16	22		15	19		17	21	ns
t_{PHL}	clock	Q or $\overline{Q}$		20	28		17	23		17	22	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

4-Bit Arithmetic Logic Unit

LS181

FEATURES

- **Provides 16 arithmetic operations**
- **Provides 16 logic operations**
- **Full look-ahead for high-speed arithmetic operation on long words**

DESCRIPTION

The LS181 is an arithmetic logic unit (ALU)/function generator which has a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182, full carry ahead look-ahead circuits, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	F_0	F_1	F_2	F_3	C_n	C_{n+4}	$\overline{F}$	$\overline{G}$

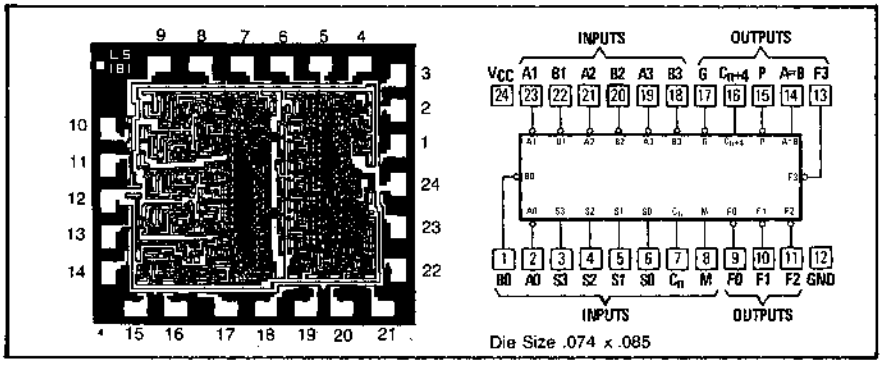
Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1 which requires an end-around or forced carry to provide A-B.

The LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs, S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT $\overline{C}_n$	OUTPUT $\overline{C}_{n+4}$	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A ≤ B	A ≥ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≥ B	A ≤ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

PIN-OUT DIAGRAM



ALU SIGNAL DESIGNATIONS

The LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

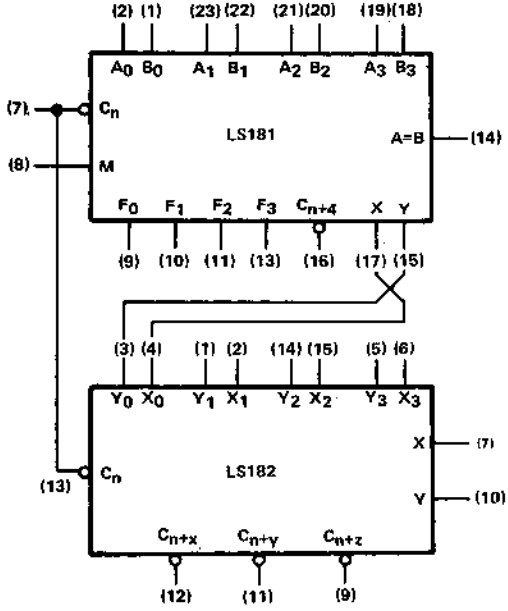


FIGURE 1
(FOR TABLE 1)

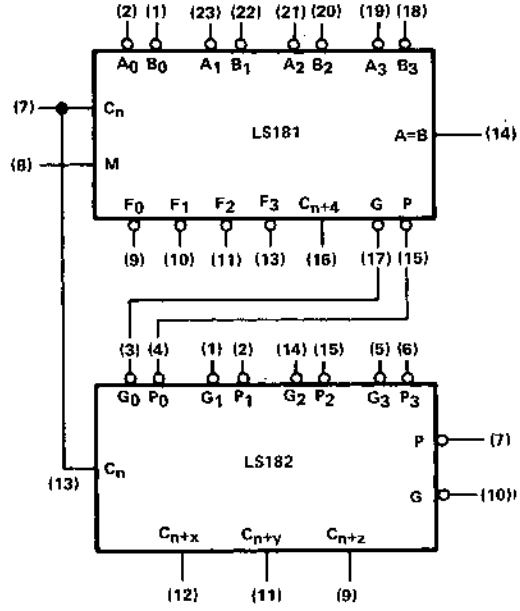


FIGURE 2
(FOR TABLE 2)

TABLE 1

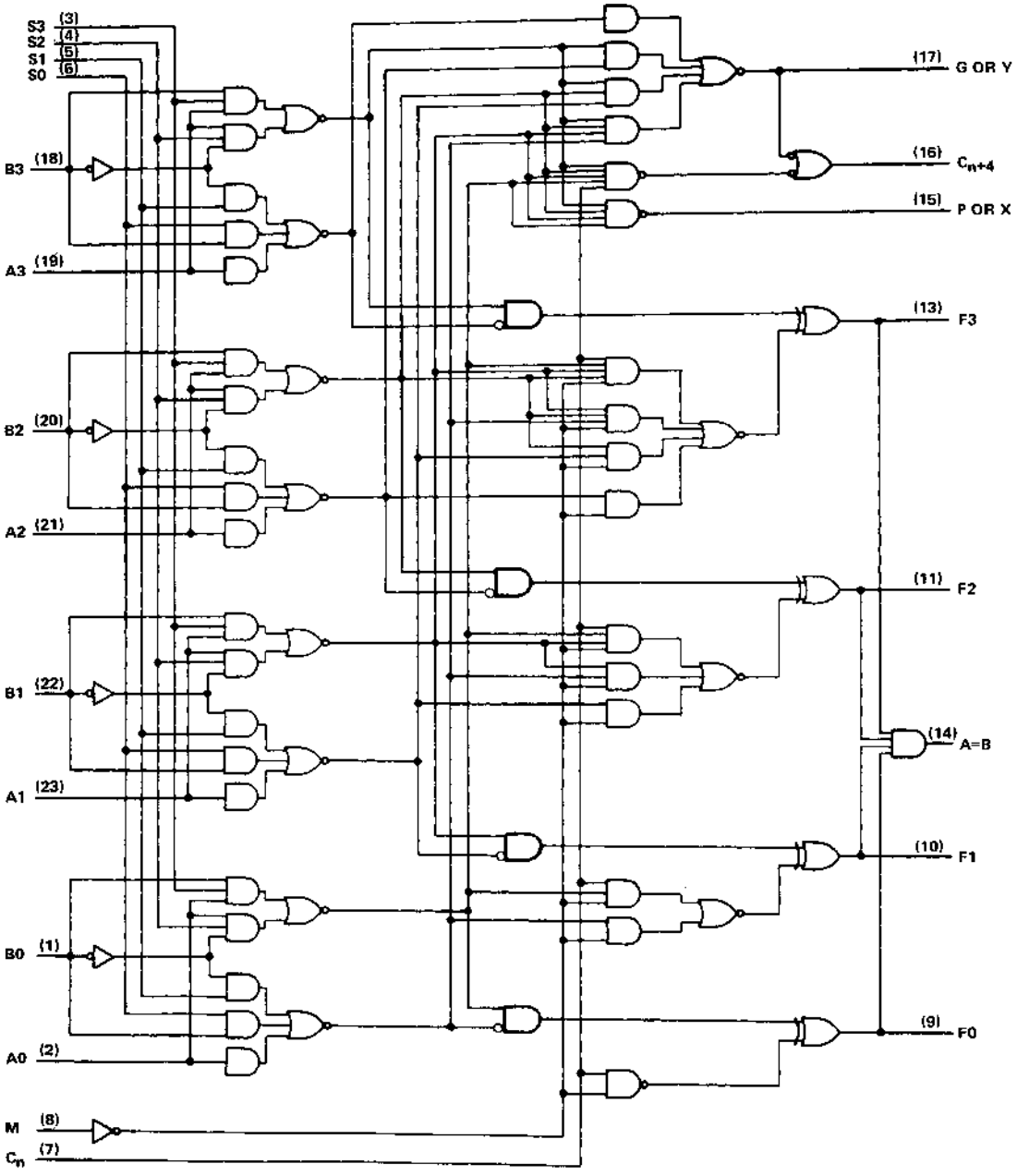
SELECTION S3 S2 S1 S0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = H (no carry)	Cn = L (no carry)
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE 2

SELECTION S3 S2 S1 S0	ACTIVE LOW DATA: M = H LOGIC FUNCTIONS	M = L; ARITHMETIC OPERATIONS: Cn = L (with carry)	Cn = H (with carry)
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = AB	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = A$\overline{B}$	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	Any Output except A = B	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
I_{OH}	A = B Output only	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, V_{OH}=5.5V				100			100	μA
V_{OL}	All outputs	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA		0.35	0.6		0.35	0.5	
	Output G		I_{OL}=16mA		0.47	0.7		0.47	0.7	
I_I	Mode input	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
	Any A or B input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.5			0.5	
I_{IH}	Mode input	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Any A or B					60			60	
	Any S input					80			80	
	Carry input					100			100	
I_{IL}	Mode input	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Any A or B input					-1.2			-1.2	
	Any S input					-1.6			-1.6	
	Carry input					-2			-2	
I_{OS}†	Any Output except A=B	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX	Condition A		20	32		20	34	mA
			Condition B		21	35		21	37	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M and A inputs are at 4.5V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A on page 2-174)												
t_{PLH}	C_n	C_{n+4}		17	28		14	24		17	28	ns
t_{PHL}				16	24		13	20		16	24	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	Any A or B	C_{n+4}		27	39		24	35		27	39	ns
t_{PHL}				20	34		17	30		20	34	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	C_{n+4}		27	42		24	38		27	42	ns
t_{PHL}				28	42		25	38		28	42	
M = 0V, (SUM or DIFF mode)												
t_{PLH}	C_n	Any F		15	28		12	24		15	28	ns
t_{PHL}				15	24		12	20		15	24	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	Any A or B	G		15	33		12	29		15	33	ns
t_{PHL}				18	27		15	23		18	27	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	G		23	34		20	30		23	34	ns
t_{PHL}				20	30		17	26		20	30	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 4.5V (SUM mode)												
t_{PLH}	Any A or B	P		17	32		14	28		17	32	ns
t_{PHL}				23	34		20	30		23	34	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	P		23	34		20	30		23	34	ns
t_{PHL}				25	37		22	33		25	37	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	A_i or B_i	F_i		18	34		15	30		18	34	ns
t_{PHL}				16	24		13	20		16	24	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	A_i or B_i	F_i		24	36		21	32		24	36	ns
t_{PHL}				18	27		15	23		18	27	
M = 4.5V (logic mode)												
t_{PLH}	A_i or B_i	F_i		20	34		17	30		20	34	ns
t_{PHL}				18	33		15	29		18	33	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	A = B		36	56		33	50		36	56	ns
t_{PHL}				32	50		29	45		32	50	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A on page 2-174)												
t_{PLH}	C_n	C_{n+4}		21	33		18	29		21	33	ns
t_{PHL}				19	29		17	25		19	29	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	Any A or B	C_{n+4}		30	44		28	40		30	44	ns
t_{PHL}				23	39		31	35		23	39	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	C_{n+4}		30	47		28	43		30	47	ns
t_{PHL}				31	47		29	43		31	47	
M = 0V, (SUM or DIFF mode)												
t_{PLH}	C_n	Any F		18	33		16	29		18	33	ns
t_{PHL}				18	29		16	25		18	29	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	Any A or B	G		18	38		16	34		18	39	ns
t_{PHL}				21	32		19	28		21	32	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	G		26	39		24	35		26	39	ns
t_{PHL}				23	35		21	31		23	35	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 4.5V (SUM mode)												
t_{PLH}	Any A or B	P		20	37		18	33		20	37	ns
t_{PHL}				26	39		24	35		26	39	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	P		26	39		24	35		26	39	ns
t_{PHL}				28	42		26	38		28	42	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)												
t_{PLH}	A_i or B_i	F_i		21	39		19	35		21	39	ns
t_{PHL}				19	29		18	25		19	29	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	A_i or B_i	F_i		27	41		25	37		27	41	ns
t_{PHL}				21	32		19	28		21	32	
M = 4.5V (logic mode)												
t_{PLH}	A_i or B_i	F_i		23	39		21	35		23	39	ns
t_{PHL}				21	38		19	34		21	38	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)												
t_{PLH}	Any A or B	A = B		39	61		37	55		39	61	ns
t_{PHL}				35	55		33	50		35	55	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

PARAMETER MEASUREMENT INFORMATION

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In -Phase

LS190 Synchronous BCD Decade Up/Down Counter

LS191 Synchronous 4-Bit Binary Up/Down Counter

FEATURES

- Single up/down count mode control line
- Asynchronous parallel load
- Count enable, parallel load control inputs
- Cascadable

DESCRIPTION

The LS190 and LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

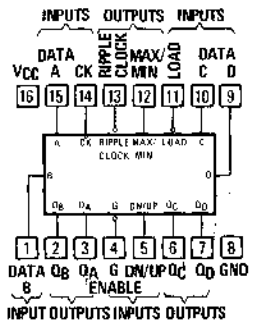
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable and down/up inputs should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

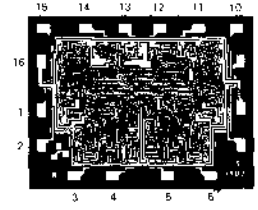
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN-OUT DIAGRAM

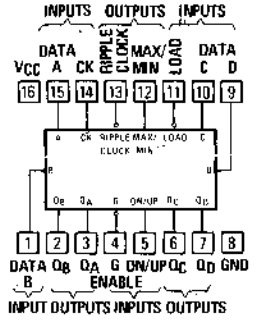


LOW INPUT TO LOAD SETS Q_A = A, Q_B = B, Q_C = C, Q_D = D

LS190

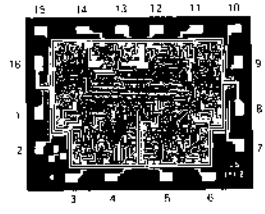


Die Size .100 x .077



LOW INPUT TO LOAD SETS Q_A = A, Q_B = B, Q_C = C, Q_D = D

LS191



Die Size .100 x .077

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Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Input clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (see Figures 1 and 2)	20			20			ns
Enable to clock setup time, t_{setup}	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA					0.35	0.5	
I_I	Enable	V_{CC}=MAX, V_I=7V				0.3			0.3	mA
	Others					0.1			0.1	
I_{IH}	Enable	V_{CC}=MAX, V_I=2.7V				60			60	μA
	Others					20			20	
I_{IL}	Enable	V_{CC}=MAX, V_I=0.4V				-1.2			-1.2	mA
	Others					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX			20	35		20	35	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all inputs grounded and all outputs open.

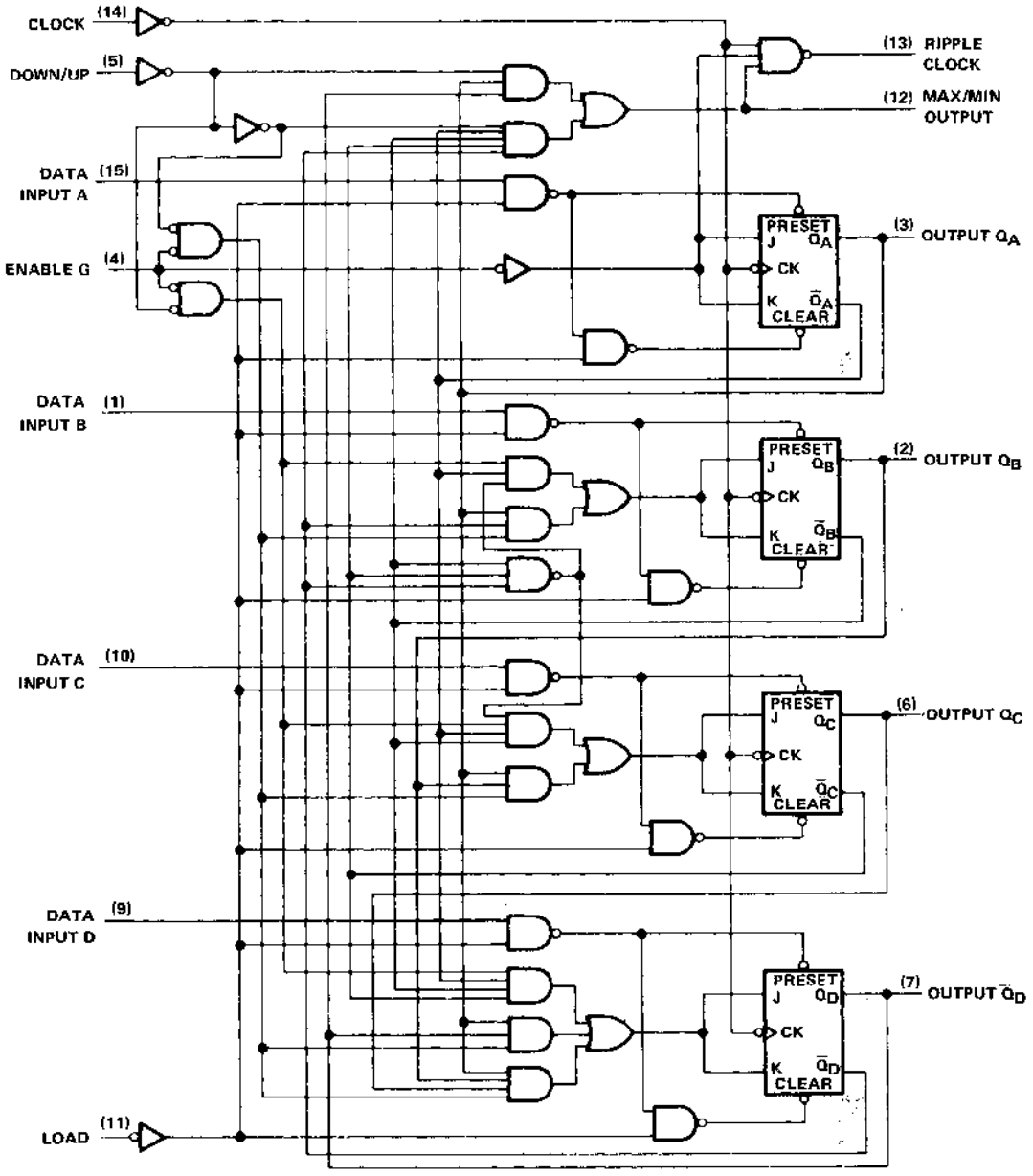
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 thru 7 on pages 2-115 and 2-116 and Fig. A on page 2-174)												
f_{max}						20	25					MHz
t_{PLH}	Load	Q_A,Q_B,Q_C,Q_D		25	37		22	33		25	37	ns
t_{PHL}				36	54		33	50		36	54	
t_{PLH}	Data A,B,C,D	Q_A,Q_B,Q_C,Q_D		17	26		14	22		17	26	ns
t_{PHL}				38	56		35	50		38	56	
t_{PLH}	Clock	Ripple Clock		16	24		13	20		16	24	ns
t_{PHL}				19	28		16	24		19	28	
t_{PLH}	Clock	Q_A,Q_B,Q_C,Q_D		19	28		16	24		19	28	ns
t_{PHL}				27	40		24	36		27	40	
t_{PLH}	Clock	Max/Min		31	46		28	42		31	46	ns
t_{PHL}				40	56		37	52		40	56	
t_{PLH}	Down/Up	Ripple Clock		33	49		30	45		33	49	ns
t_{PHL}				33	49		30	45		33	49	
t_{PLH}	Down/Up	Max/Min		24	37		21	33		24	37	ns
t_{PHL}				25	38		22	33		25	38	
t_{PLH}	Enable	Ripple Clock		24	37		21	33		24	37	ns
t_{PHL}				25	38		22	33		25	38	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 thru 7 on pages 2-115 and 2-116 and Fig. A on page 2-174)												
t_{PLH}	Load			28	42		25	37		28	42	ns
t_{PHL}				39	59		36	54		39	59	
t_{PLH}	Data A,B,C,D	Q_A,Q_B,Q_C,Q_D		20	31		17	26		20	31	ns
t_{PHL}				41	61		38	54		41	61	
t_{PLH}	Clock	Ripple Clock		19	29		16	24		19	29	ns
t_{PHL}				22	33		19	28		22	33	
t_{PLH}	Clock	Q_A,Q_B,Q_C,Q_D		22	33		19	28		22	33	ns
t_{PHL}				30	45		27	40		30	45	
t_{PLH}	Clock	Max/Min		34	51		31	46		34	51	ns
t_{PHL}				43	61		40	56		43	61	
t_{PLH}	Down/Up	Ripple Clock		36	54		33	49		36	54	ns
t_{PHL}				36	54		33	49		36	54	
t_{PLH}	Down/Up	Max/Min		27	42		24	37		27	42	ns
t_{PHL}				28	43		25	37		28	43	
t_{PLH}	Enable	Ripple Clock		27	42		24	37		27	42	ns
t_{PHL}				28	43		25	37		28	33	

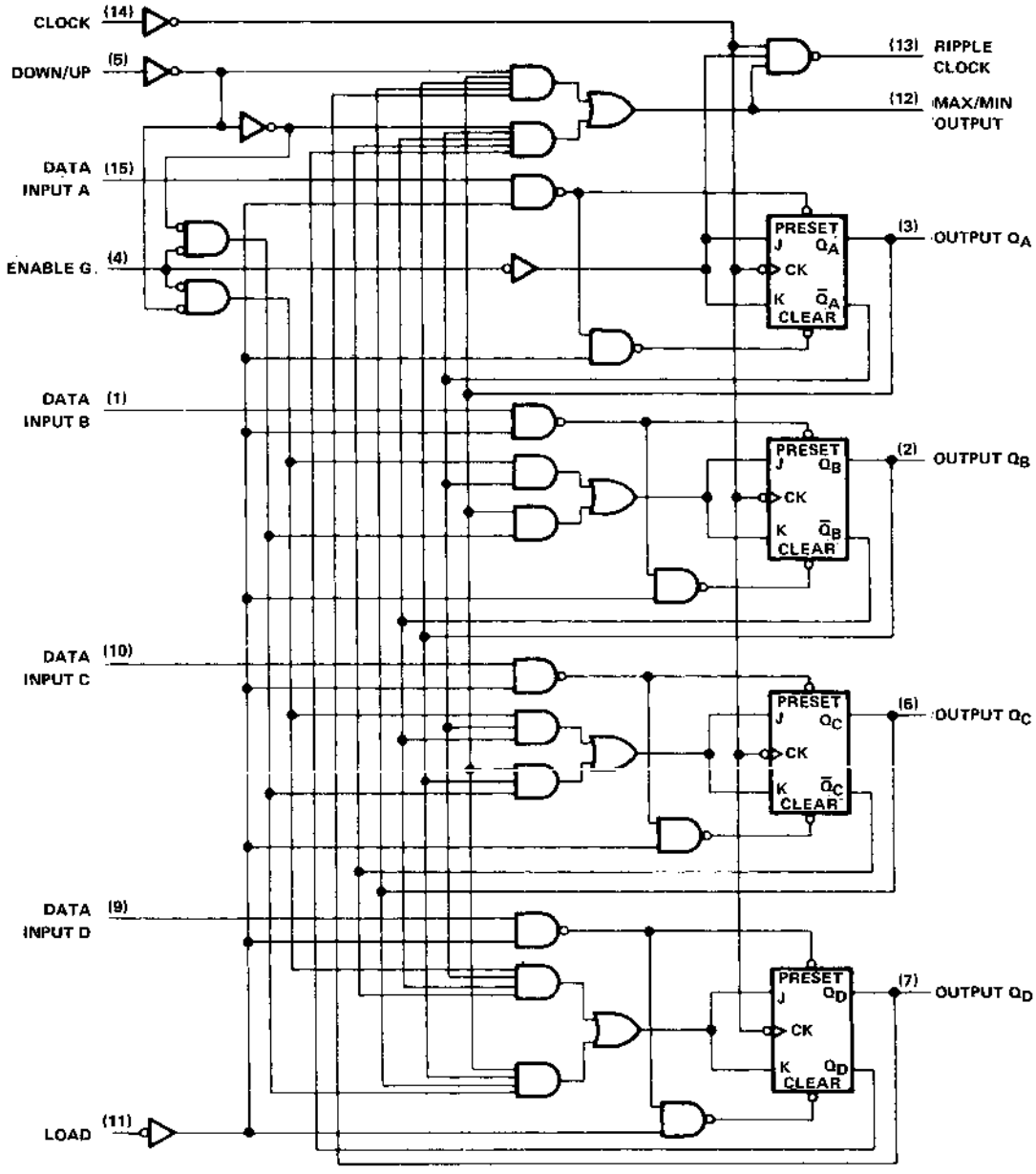
Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

LOGIC DIAGRAM

LS190



LOGIC DIAGRAM
LS191



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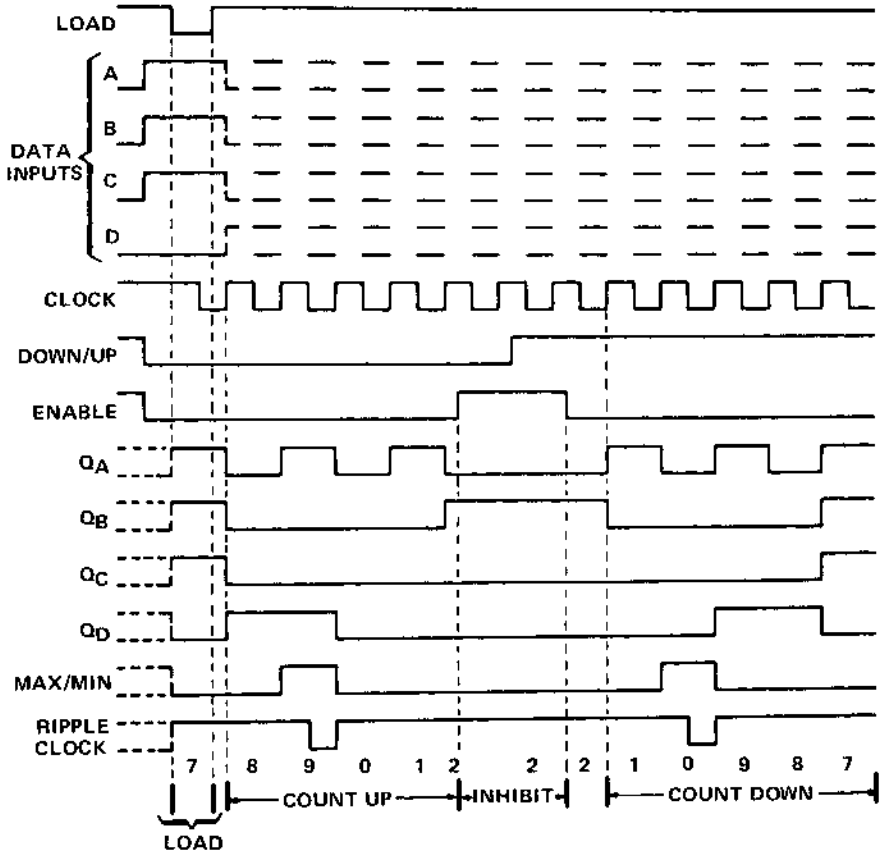
LS190 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

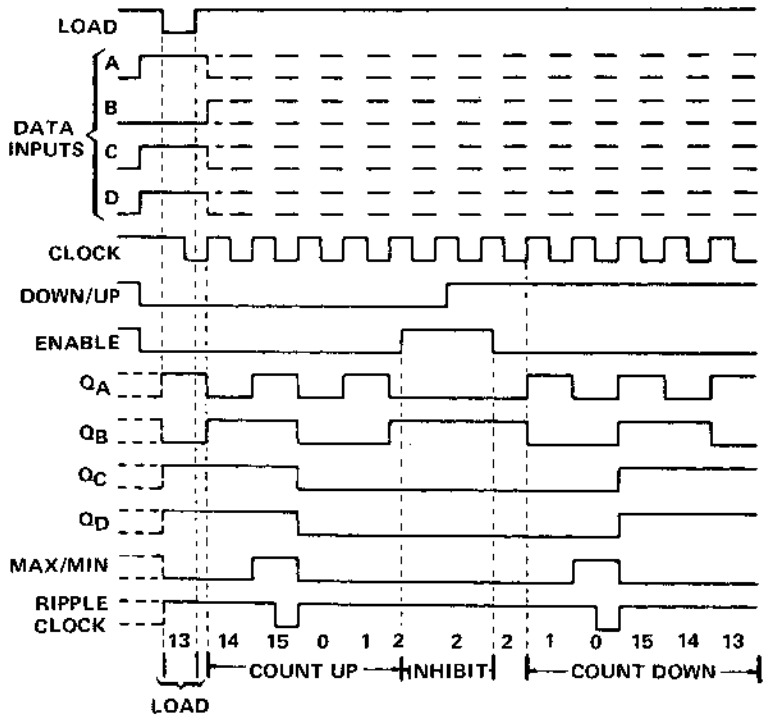
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



LS191 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



PARAMETER MEASUREMENT INFORMATION

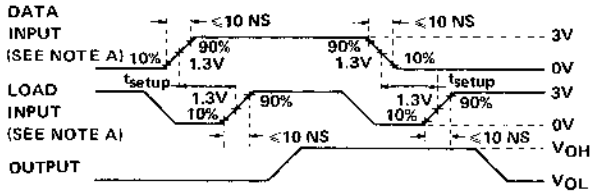
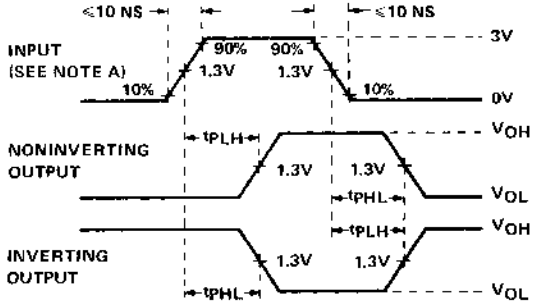


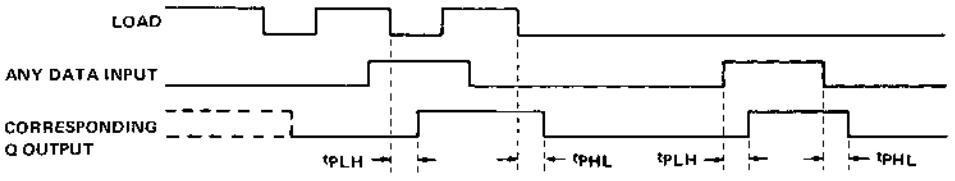
FIGURE 1–DATA SETUP TIME VOLTAGE WAVEFORMS

See waveform sequences in Figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in Figures 4 through 7.

FIGURE 2– GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

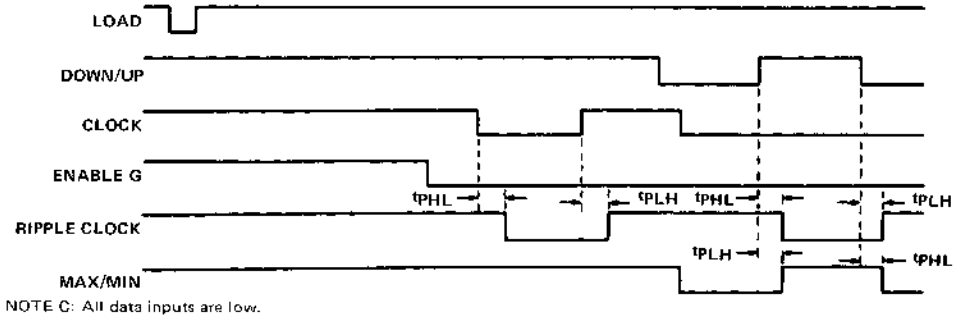


NOTES:
A. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50Ω, duty cycle ≤ 50%, PRR ≤ 1MHz.



NOTE B: Conditions on other inputs are irrelevant.

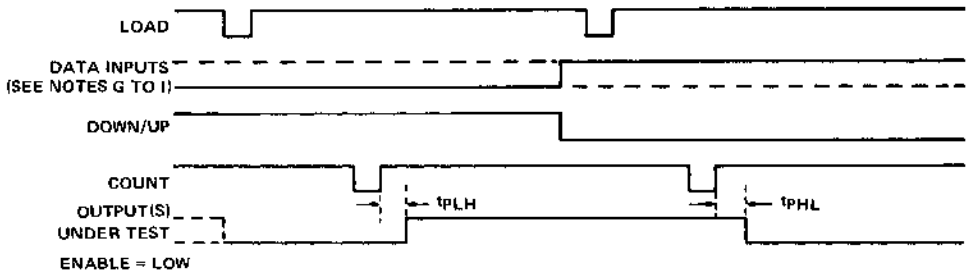
FIGURE 3–LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE C: All data inputs are low.

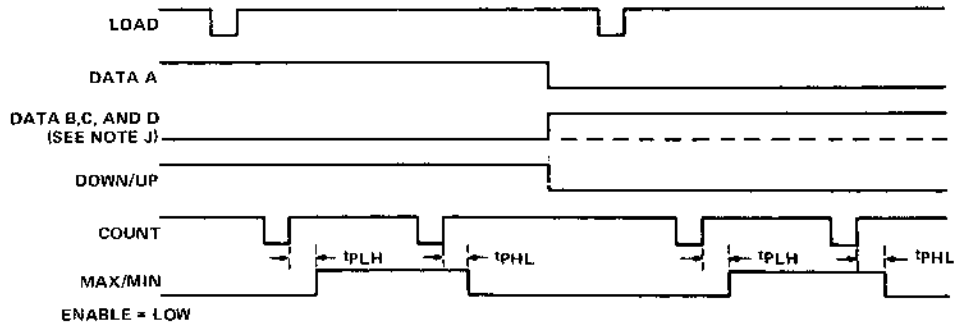
FIGURE 4–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO MAX/MIN

PARAMETER MEASUREMENT INFORMATION (Continued)



F. to test Q_A, Q_B, and Q_C outputs of LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
G. To test Q_D output of LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
H. To test Q_A, Q_B, Q_C, and Q_D outputs of LS191: All four data inputs are shown by the solid line.

FIGURE 5–CLOCK TO OUTPUT



NOTE I:
Data inputs B and C are shown by the dashed line for the LS190 and the solid line for the LS191: Data input D is shown by the solid line for both devices.

FIGURE 6–CLOCK TO MAX/MIN

Synchronous BCD Decade Up/Down Counter — LS192

Synchronous 4-Bit Binary Up/Down Counter — LS193

FEATURES

- Separate clock inputs for count-up, count-down
- Asynchronous parallel load and clear
- Cascadable

DESCRIPTION

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The LS192 is a BCD counter and the LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

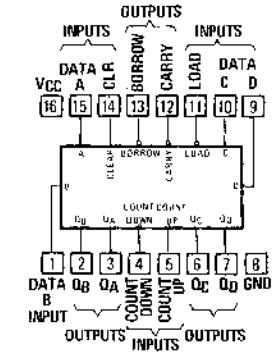
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

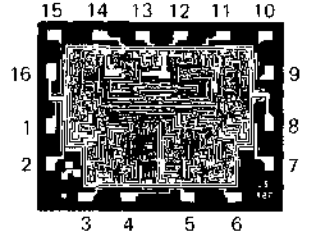
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN-OUT DIAGRAM

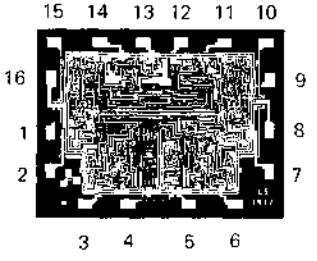


Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

LS192



LS193



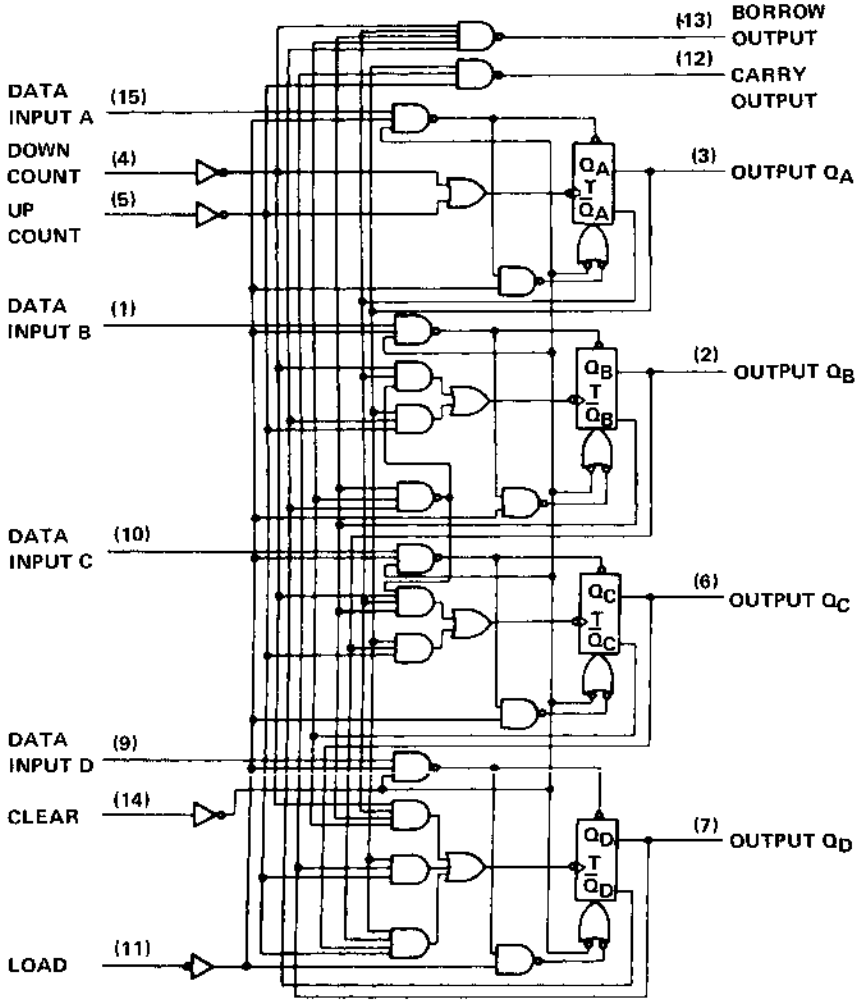
Die Size .100 x .077 (both types)

Recommended Operating Conditions

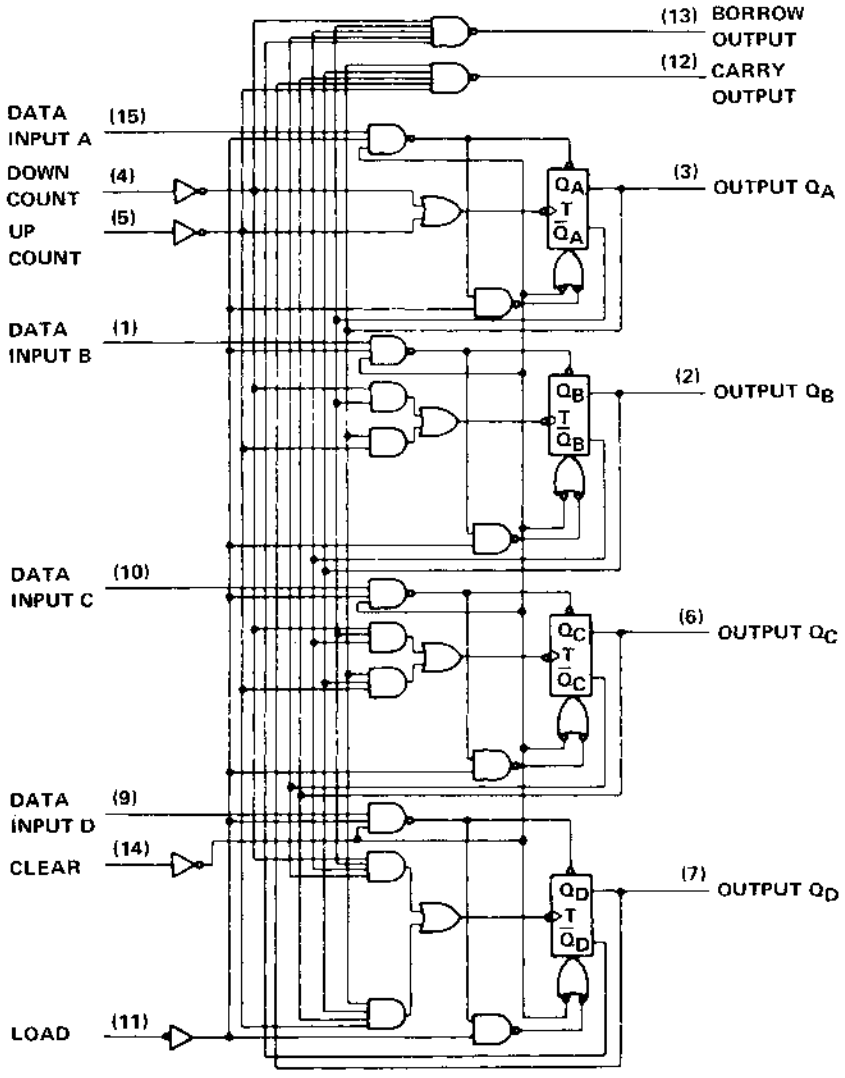
	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature range, T_A	–55		125	0		70	°C

LOGIC DIAGRAM

LS192



LOGIC DIAGRAM
LS193



Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX			19	34		19	34	mA

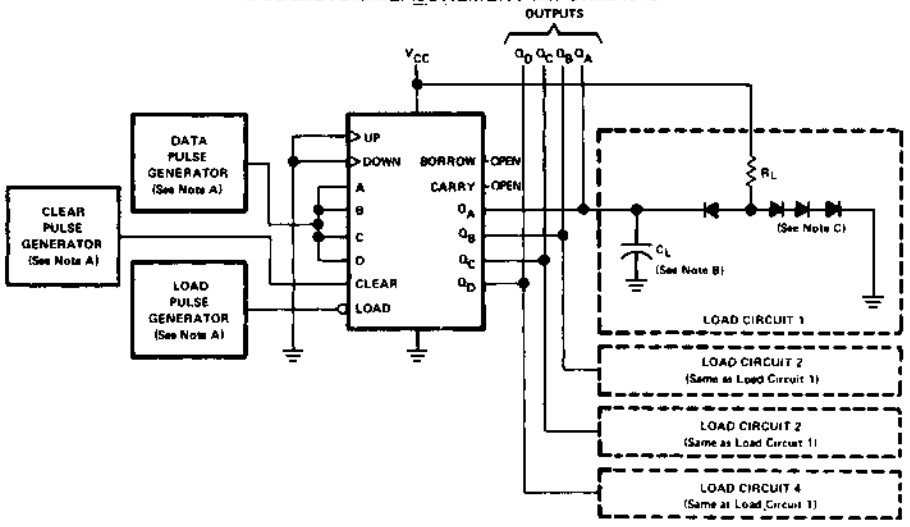
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

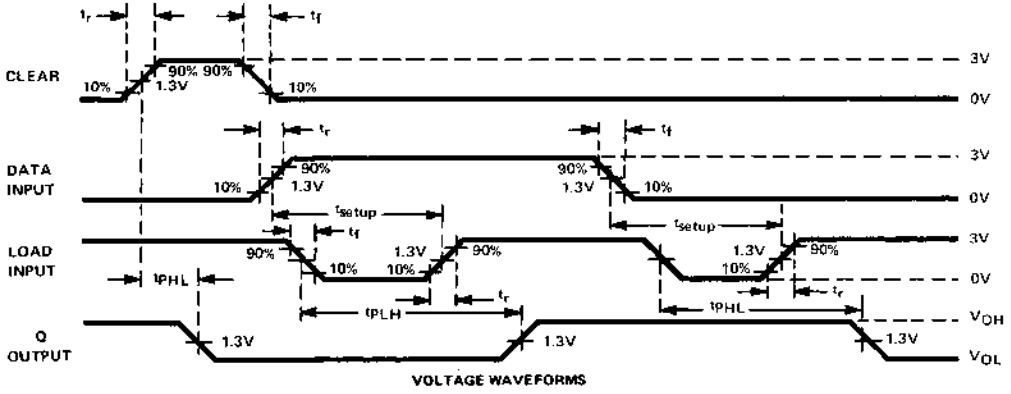
Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 and 2)												
f_{max}						25	32					MHz
t_{PLH}	Count-up	Carry		19	29		17	26		19	29	ns
t_{PHL}				18	28		16	24		18	28	
t_{PLH}	Count-down	Borrow		18	28		16	24		18	28	ns
t_{PHL}				18	28		16	24		18	28	
t_{PLH}	Either Count	Q		27	42		25	38		27	42	ns
t_{PHL}				33	51		31	47		33	51	
t_{PLH}	Load	Q		29	44		27	40		29	44	ns
t_{PHL}				31	44		29	40		31	44	
t_{PHL}	Clear	Q		24	39		22	35		24	39	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 and 2)												
												MHz
t_{PLH}	Count-up	Carry		23	34		21	31		23	34	ns
t_{PHL}				22	32		20	30		22	32	
t_{PLH}	Count-down	Borrow		22	32		20	30		22	32	ns
t_{PHL}				22	32		20	30		22	32	
t_{PLH}	Either Count	Q		31	47		29	43		31	47	ns
t_{PHL}				37	56		34	51		37	56	
t_{PLH}	Load	Q		33	49		31	44		33	49	ns
t_{PHL}				35	49		33	45		35	49	
t_{PHL}	Clear	Q		28	44		26	40		28	44	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$ and for the data pulse generator PRR < 500KHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.

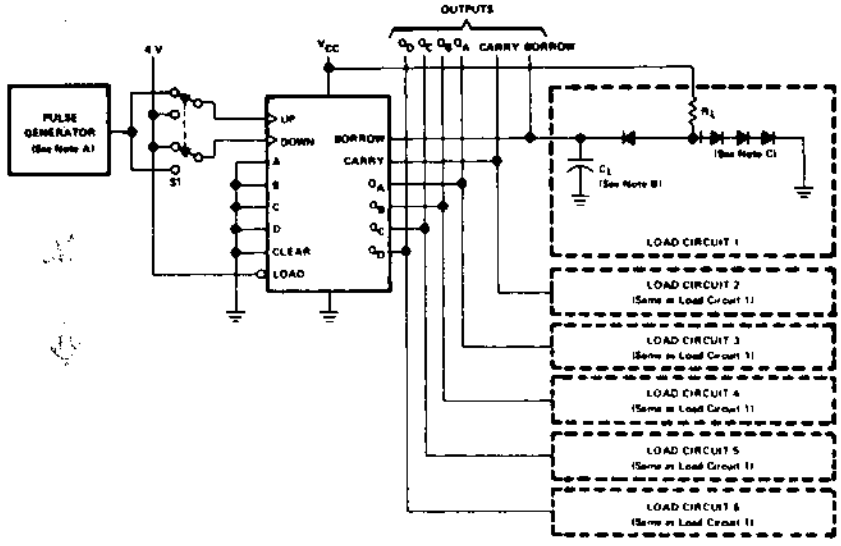
B. C_L includes probe and jig capacitance.

C. Diodes are 1N3064.

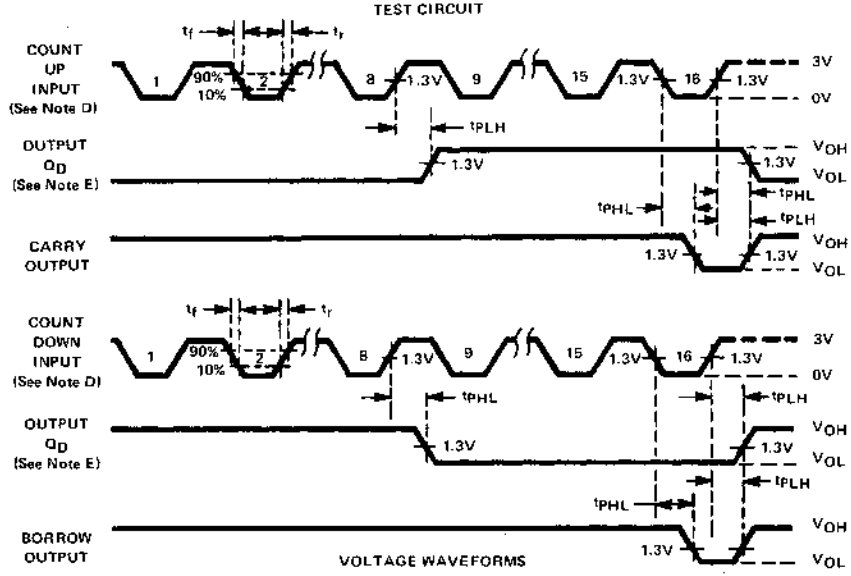
D. t_r and $t_f \leq 7$ ns.

FIGURE 1 — CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION (Continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generator has the following characteristics: PRR ≤ 1MHz, Z_{out} = 50Ω, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. Count-up and count-down pulse shown is for the LS193 binary counter. Count cycle for LS192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and t_f ≤ 7ns.

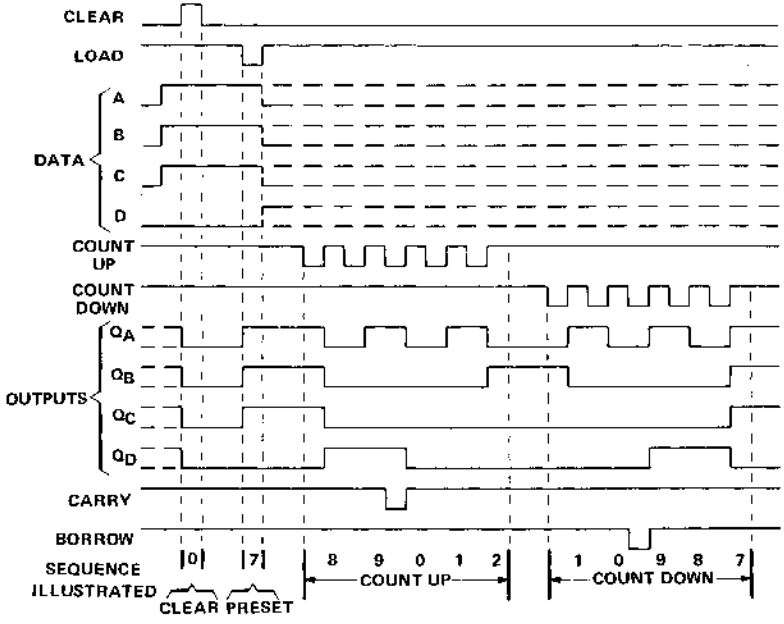
FIGURE 2–PROPAGATION DELAY TIMES

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

LS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



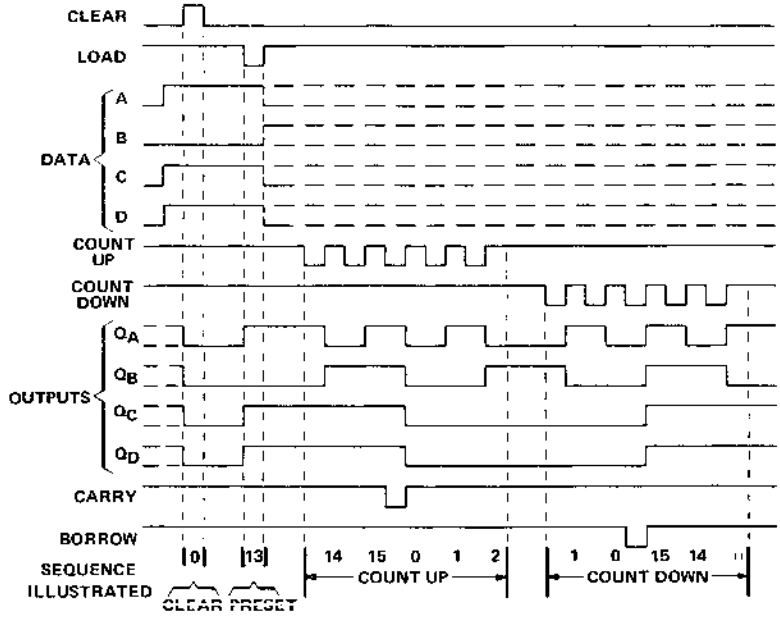
NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

LS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

DESCRIPTION

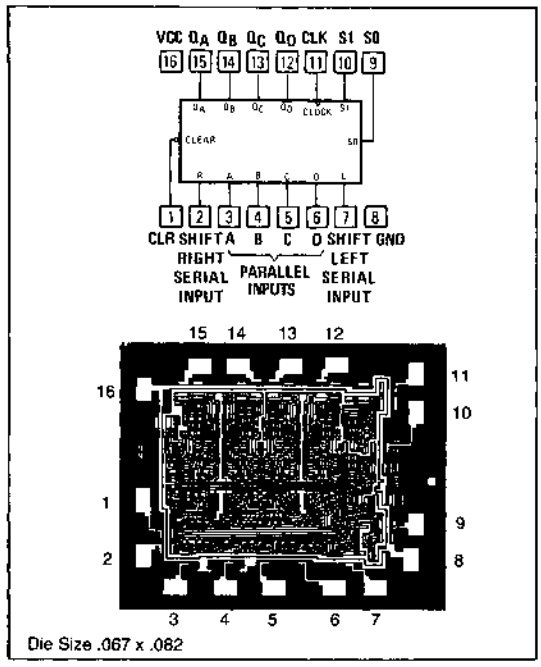
This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct over-riding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flop is inhibited when both mode control inputs are low.

PIN-OUT DIAGRAM



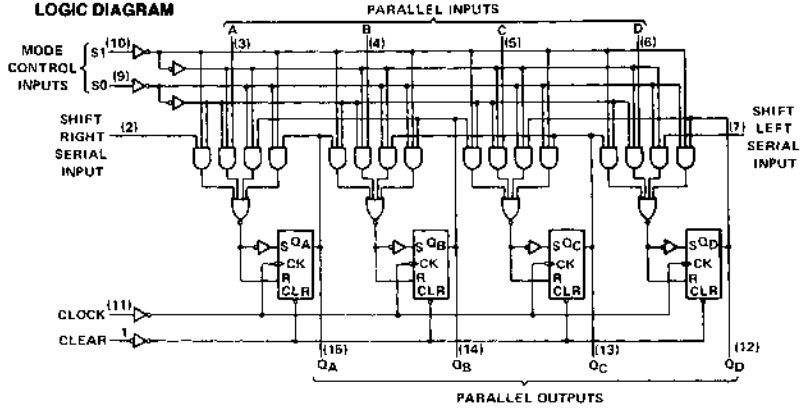
Die Size .067 x .082

FUNCTION TABLE

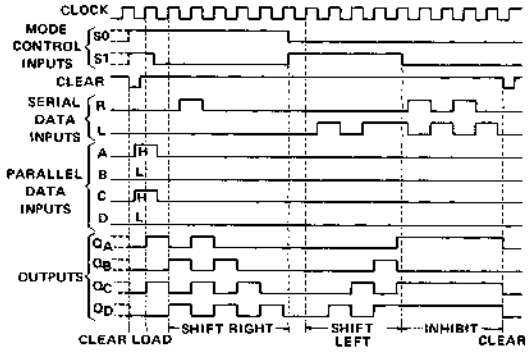
INPUTS									OUTPUTS			
CLEAR	MODE S1	MODE S0	CLOCK	SERIAL LEFT	SERIAL RIGHT	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, $2Q_{D0}$ = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

LOGIC DIAGRAM



TYPICAL TIMING SEQUENCES



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		30			30			ns
Setup time, t_{setup}	Mode control	30			30			ns
	Serial and parallel data	16			16			ns
	Clear inactive-state	18			18			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.5		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX			15	23		12	23	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

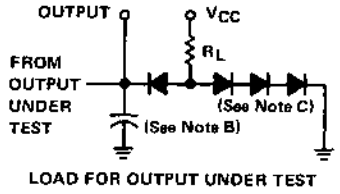
††With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5V, applied to clock.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	−55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. below)										
f_{max}				30	40					MHz
t_{PHL}		27	34		24	30		27	34	ns
t_{PLH}		14	22		11	18		14	22	ns
t_{PHL}		18	26		15	22		18	26	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. below)										
t_{PHL}		31	39		28	36		31	39	ns
t_{PLH}		18	27		15	23		18	27	ns
t_{PHL}		22	31		19	27		22	31	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

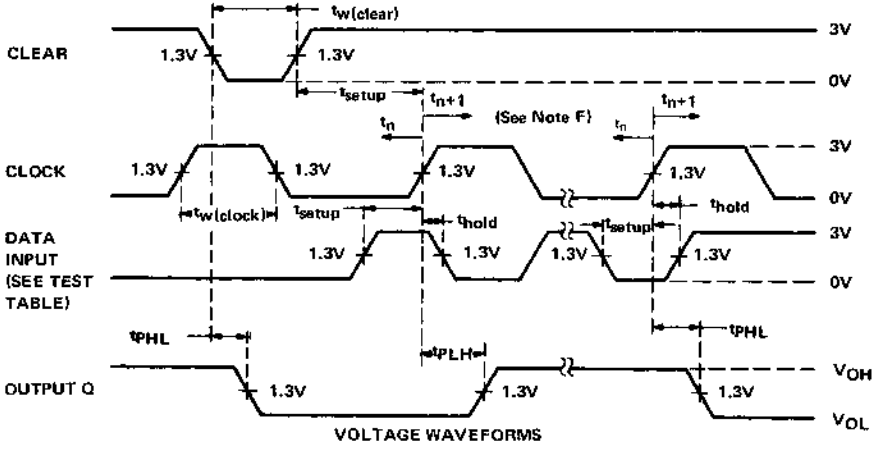
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\Omega$ and PRR ≤ 1 MHz, $t_r \leq 15$ ns and $t_f \leq 6$ ns. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064 or 1N916.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

F. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

DESCRIPTION

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

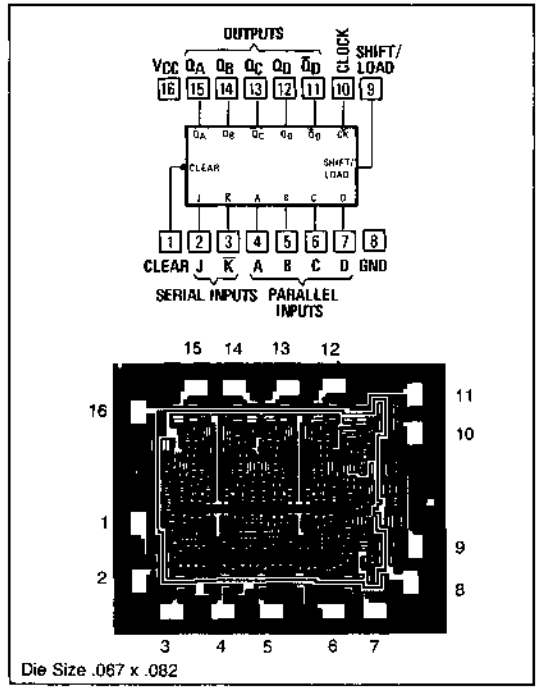
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as J-K, D-, or T-type flip-flop as shown in the function table.

FUNCTION TABLE

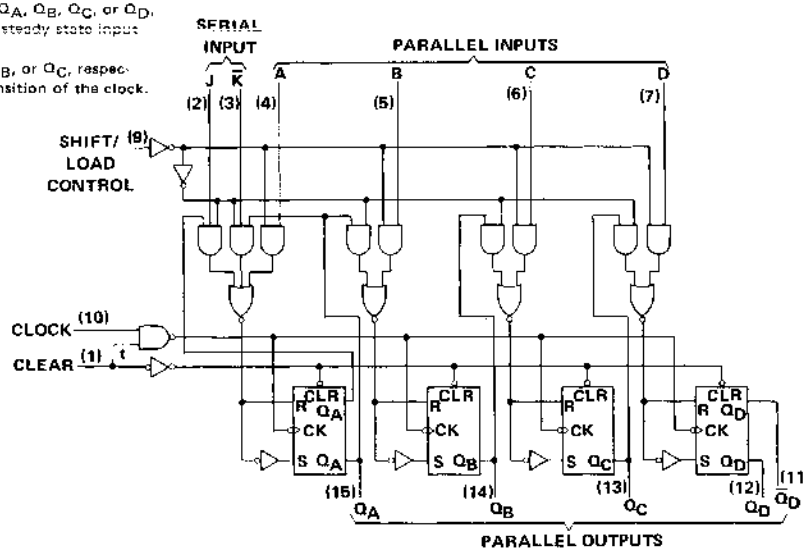
INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



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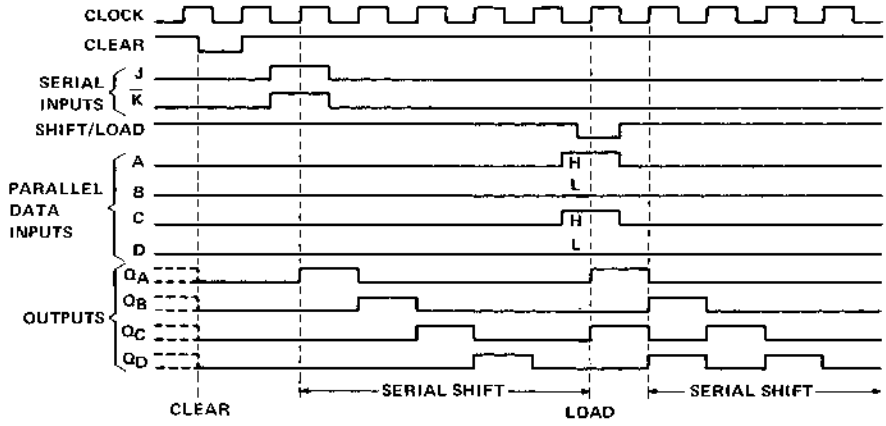
TYPICAL TIMING SEQUENCES



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$		18			18			ns
Width of clear input pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				0			0	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 on page 2-132)										
f_{max}				30	40					MHz
t_{PHL} (from clear)		26	23		26	33		35	49	ns
t_{PLH} (from clk)		14	20		14	19		21	31	ns
t_{PHL} (from clk)		20	26		18	24		24	32	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1 on page 2-132)										
t_{PHL} (from clear)		27	36		27	36		37	47	ns
t_{PLH} (from clk)		16	22		16	21		24	31	ns
t_{PHL} (from clk)		22	29		21	27		33	46	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

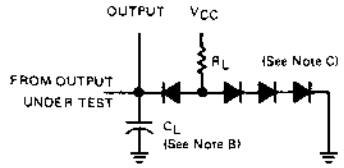
Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA					0.35	0.50	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX			14	21		10	17	mA

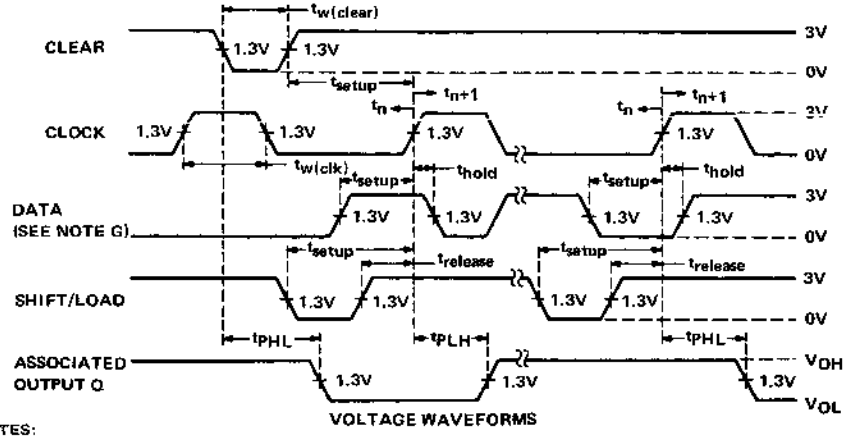
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††With all outputs open, shift/load grounded and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V to clock.

PARAMETER MEASUREMENT INFORMATION

FIGURE 1



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES:
A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR ≤ MHz, $t_r \leq 15$ ns, and $t_f \leq 6$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
F. J and $\overline{K}$ are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

Presettable BCD Decade Ripple Counter — LS196

Presettable 4-Bit Binary Ripple Counter — LS197

FEATURES

- BCD, bi-quinary, binary counting modes
- Asynchronous clear
- Fully programmable
- May be used as 4-Bit latches

DESCRIPTION

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (LS196) or a divide-by-two and a divide-by-eight counter (LS197). THese four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

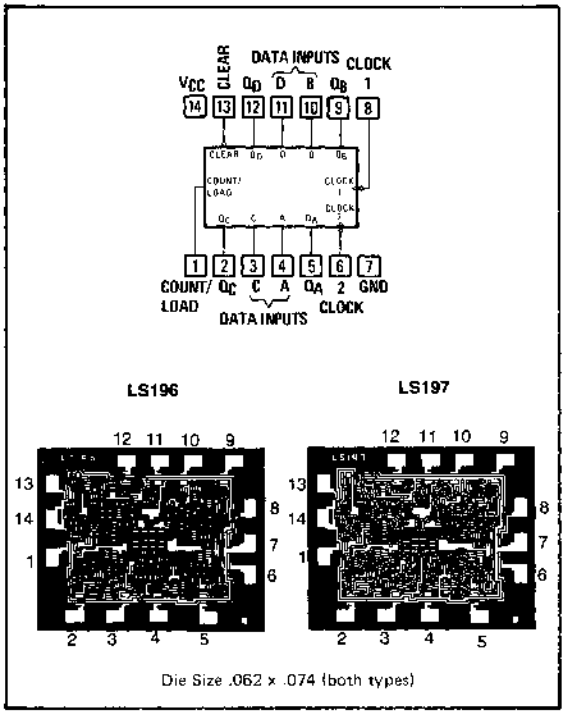
These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

PIN-OUT DIAGRAM



Die Size .062 x .074 (both types)

LS196
FUNCTION TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

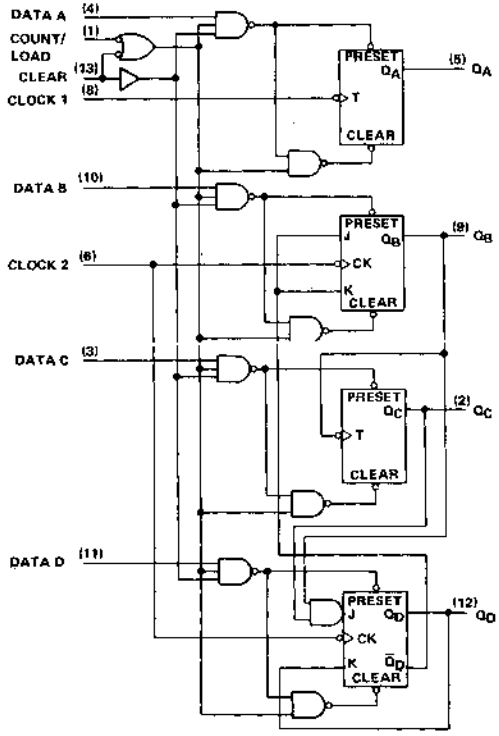
1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the function table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit-ripple-through counter.

LS197 FUNCTION TABLE
(See Note A)

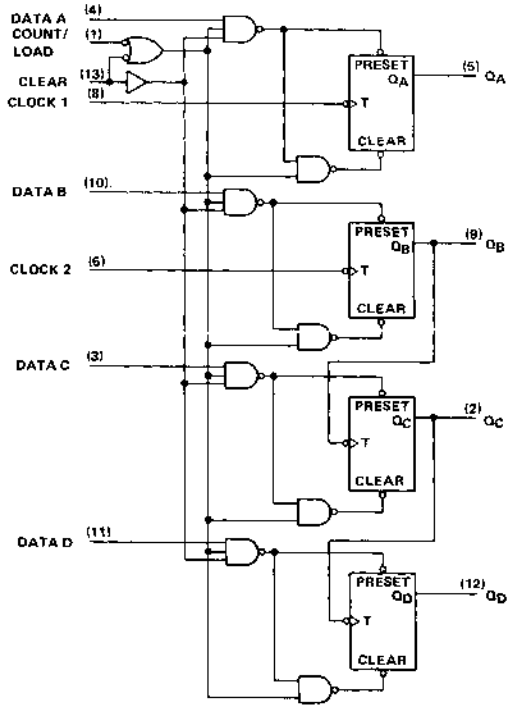
COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level
NOTE A: Output Q_A connected to clock-2 input.

LOGIC DIAGRAM LS196



LOGIC DIAGRAM LS197



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Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.75	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency	Clock-1 input	0			0			MHz
	Clock-2 input	0			0			
Pulse width, t_w	Clock-1 input	20			20			ns
	Clock-2 input	30			30			
	Clear	15			15			
	Load	20			20			
Input hold time, t_{hold}	High-level data	$t_{w\ (load)}$						ns
	Low-level data	$t_{w\ (load)}$						
Input setup time, t_{setup}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (see Note 1)		20			20			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

NOTE1:
Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I= -18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}= -400μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA¶		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA					0.35	0.50	
I_I	Data, count/load	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
	Clear, clock 1					0.2			0.2	
	Clock 2 of LS196					0.4			0.4	
	Clock 2 of LS197					0.2			0.2	
I_{IH}	Data, count/load	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Clear, clock 1					40			40	
	Clock 2 of LS196					80			80	
	Clock 2 of LS197					40			40	
I_{IL}	Data, count/load	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
	Clear					-0.8			-0.8	
	Clock 1					-2.4			-2.4	
	Clock 2 of LS196					-2.8			-2.8	
	Clock 2 of LS197					-1.3			-1.3	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††		V_{CC}=MAX			12	20		12	20	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
††I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A on page 2-174)													
f_{max}	LS196	Clock 1	Q_A				45	70					MHz
f_{max}	LS197	Clock 1	Q_A				45	60					MHz
t_{PLH}	LS196	Clock 1	Q_A		10	15		8	12		10	15	ns
t_{PHL}					14	19		12	16		14	19	
t_{PLH}	LS197	Clock 1	Q_A		10	15		8	12		10	15	ns
t_{PHL}					14	19		12	16		14	19	
t_{PLH}	LS196	Clock 2	Q_B		13	18		11	15		13	18	ns
t_{PHL}					16	22		14	19		16	22	
t_{PLH}	LS197	Clock 2	Q_B		12	18		10	15		12	18	ns
t_{PHL}					15	21		13	18		15	21	
t_{PLH}	LS196	Clock 2	Q_C		24	37		22	34		24	37	ns
t_{PHL}					31	43		29	40		31	43	
t_{PLH}	LS197	Clock 2	Q_C		24	37		22	34		24	37	ns
t_{PHL}					28	37		26	34		28	37	
t_{PLH}	LS196	Clock 2	Q_D		13	21		11	18		13	21	ns
t_{PHL}					18	23		16	20		18	23	
t_{PLH}	LS197	Clock 2	Q_D		36	55		34	50		36	55	ns
t_{PHL}					42	60		40	55		42	60	
t_{PLH}	LS196	A, B, C, D	Q_A, Q_B, Q_C, Q_D		14	22		12	18		14	22	ns
t_{PHL}					23	38		21	34		23	38	
t_{PLH}	LS197	A, B, C, D	Q_A, Q_B, Q_C, Q_D		23	22		21	18		23	22	ns
t_{PHL}					23	38		21	34		23	38	
t_{PLH}	LS196	Load	Any		22	34		20	30		22	34	ns
t_{PHL}					33	49		31	45		33	49	
t_{PLH}	LS197	Load	Any		22	34		20	30		22	34	ns
t_{PHL}					33	49		31	45		33	49	
t_{PHL}	LS196	Clear	Any		34	49		32	45		34	49	ns
t_{PHL}	LS197	Clear	Any		34	49		32	45		34	49	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
f_{max}	LS196	Clock 1	Q_A				48	74					MHz
f_{max}	LS197	Clock 1	Q_A				48	64					MHz
t_{PLH}	LS196	Clock 1	Q_A		14	20		11	16		14	20	ns
t_{PHL}					18	24		15	20		18	24	
t_{PLH}	LS197	Clock 1	Q_A		14	20		11	16		14	20	ns
t_{PHL}					18	24		15	20		18	24	
t_{PLH}	LS196	Clock 2	Q_B		17	23		14	19		17	23	ns
t_{PHL}					20	27		17	23		20	27	
t_{PLH}	LS197	Clock 2	Q_B		16	23		13	19		16	23	ns
t_{PHL}					19	26		16	22		19	26	
t_{PLH}	LS196	Clock 2	Q_C		28	42		25	38		28	42	ns
t_{PHL}					35	48		32	44		35	48	
t_{PLH}	LS197	Clock 2	Q_C		28	42		25	38		28	42	ns
t_{PHL}					32	42		29	38		32	42	
t_{PLH}	LS196	Clock 2	Q_D		17	26		14	22		17	26	ns
t_{PHL}					22	27		19	24		22	27	
t_{PLH}	LS197	Clock 2	Q_D		40	60		37	54		40	60	ns
t_{PHL}					46	65		43	59		46	65	
t_{PLH}	LS196	A, B, C, D	Q_A, Q_B, Q_C, Q_D		18	27		15	22		18	27	ns
t_{PHL}					27	43		24	38		27	43	
t_{PLH}	LS197	A, B, C, D	Q_A, Q_B, Q_C, Q_D		27	27		24	22		27	27	ns
t_{PHL}					27	43		24	38		27	43	
t_{PLH}	LS196	Load	Any		26	39		23	34		26	39	ns
t_{PHL}					37	54		34	49		37	54	
t_{PLH}	LS197	Load	Any		26	39		23	34		26	39	ns
t_{PHL}					37	54		34	49		37	54	
t_{PHL}	LS196	Clear	Any		38	54		35	49		38	54	ns
t_{PHL}	LS197	Clear	Any		38	54		35	49		38	54	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Dual Monostable Multivibrator with Schmitt-Trigger Inputs

FEATURES

- **LS221 is Dual Version of 54LS123, One Shot on a Monolithic Chip**
- **Pulse-Width Variance is Typically Less than ± 0.5% for 98% of the Units**
- **Pin-Out is Identical to the LS123**

DESCRIPTION

The 'LS221 is monolithic dual multivibrators with performance characteristics virtually identical to those of the LS123. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

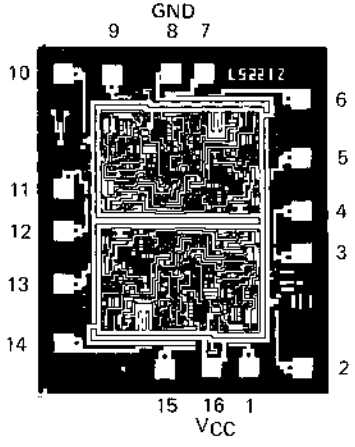
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also privided by internal latching circuitry.

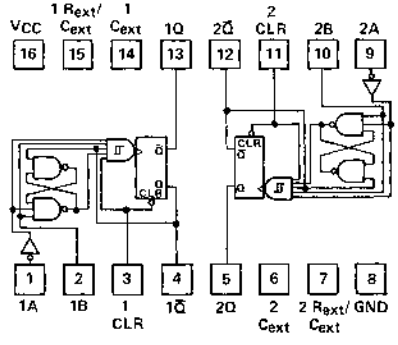
Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temparature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and 2 kΩ to 70 kΩ for 54LS221 and 2 kΩ to 100 kΩ for the 74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} \approx C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

Pin assignments for this device is identical to that of the LS123 so that the 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.





Positive Logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

Die Size .085 x .071

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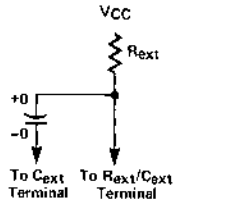
FUNCTION TABLE (EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
Also see description and switching characteristics				

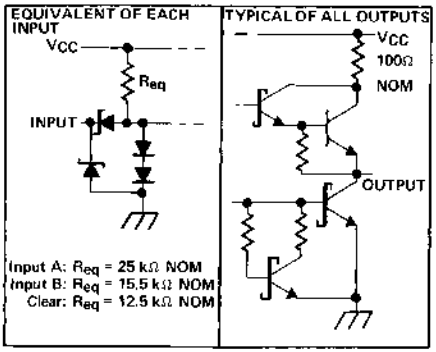
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high-level pulse
⎍ = one low-level pulse
X = irrelevant



TIMING COMPONENT CONNECTIONS

FIGURE 1

SCHEMATICS OF INPUTS AND OUTPUTS



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–400			–400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	40			40			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{setup}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			67			67	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		–55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter			Test Conditions†		9LS/54LS			9LS/74LS			Unit
					Min.	Typ.‡	Max.	Min.	Typ‡	Max.	
V_{T+}	Positive-going threshold voltage at A input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input		V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive-going threshold voltage at B input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input		V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	Input A	V_{CC} = MAX, V_I = 0.4V				−0.36			−0.36	mA
		Input B					−0.44			−0.44	
		Clear					−0.54			−0.54	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−100	−15		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
				Triggered		19	27		19	27	

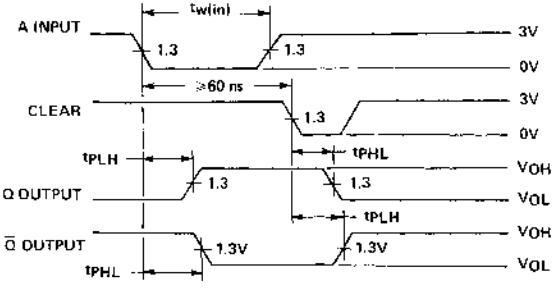
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 80pF, R_{ext} = 2.0kΩ (See Fig. 1 on 2-139)												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	77	138	175	70	120	150	77	138	175	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 0, R_{ext} = 2.0kΩ (See Fig. 1 on page 2-139)												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	22	50	80	20	47	70	22	50	80	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 100pF, R_{ext} = 10kΩ (See Fig. 1 on page 2-139)												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	600	725	870	600	670	750	620	750	870	ns
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 1pF, R_{ext} = 10kΩ (See Fig. 1 on page 2-139)												
$TW_{(out)}$	A or B	Q or $\overline{Q}$	6.0	7.7	8.5	6.0	6.7	7.5	6.0	7.7	8.5	ms
Test Conditions: R_L = 2.0k, C_L = 15pF, C_{ext} = 80pF, R_{ext} = 2.0kΩ (See Fig. 1 on page 2-139)												
t_{PLH}	A	Q		48	74		45	70		48	74	ns
	B	Q		38	59		35	55		38	59	
t_{PHL}	A	$\overline{Q}$		53	84		50	80		53	84	ns
	B	$\overline{Q}$		43	69		40	65		43	69	
t_{PHL}	Clear	Q		38	59		35	55		38	59	ns
t_{PLH}	Clear	$\overline{Q}$		47	69		44	65		47	69	ns

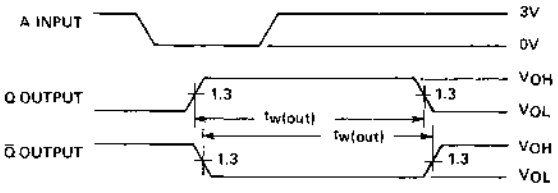
Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

PARAMETER MEASUREMENT INFORMATION



B input is high

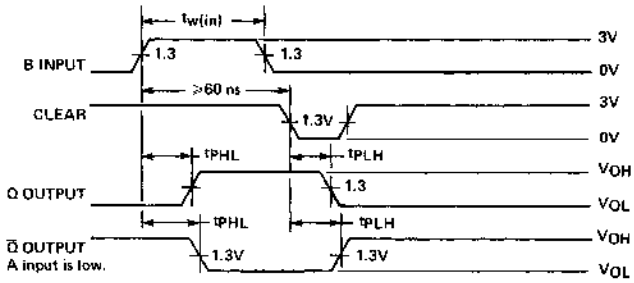
TRIGGER FROM A, THEN CLEAR



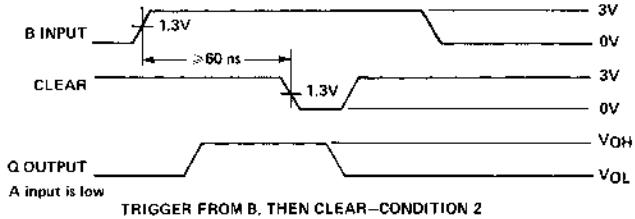
B and clear inputs are high

TRIGGER FROM A

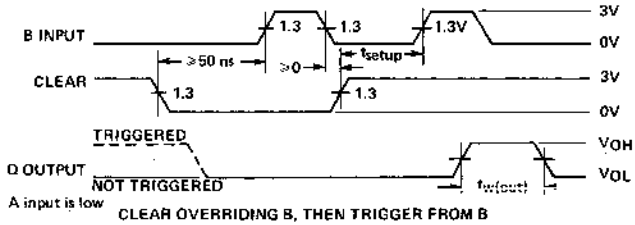
PARAMETER MEASUREMENT INFORMATION



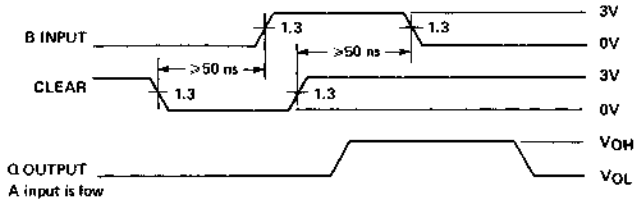
TRIGGER FROM B, THEN CLEAR–CONDITION 1



TRIGGER FROM B, THEN CLEAR–CONDITION 2



CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

8-Line-To-1-Line Multiplexer With Three-State Outputs

LS251

FEATURES

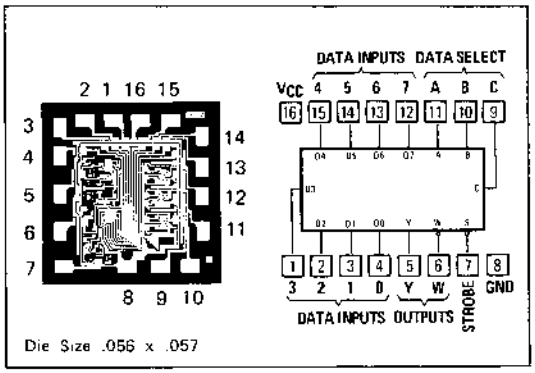
- Selects one of eight data sources
- Performs parallel-to-serial conversion
- Complementary 3-state outputs

DESCRIPTION

This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources and features a strobe-controlled three-state output. The strobe must be at a low logic level to enable this device. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

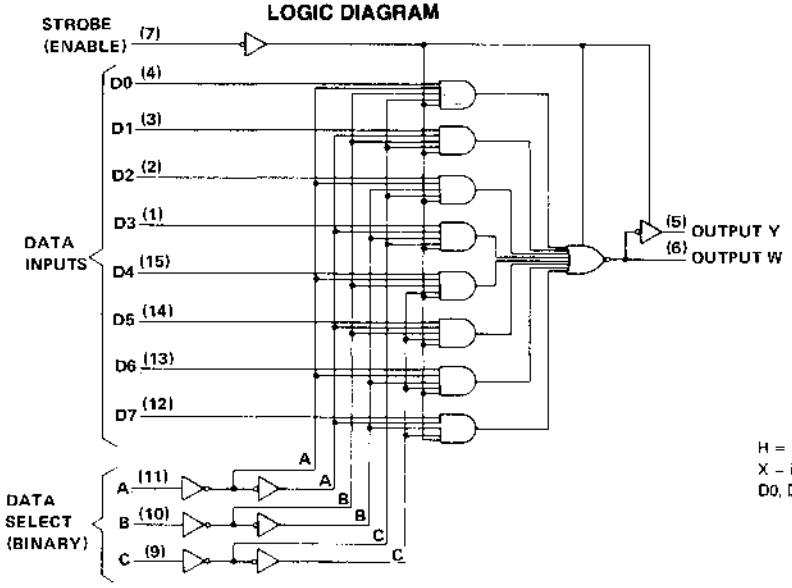
PIN-OUT DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=MAX		2.4	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX,	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
$I_{O(off)}$	V_{CC}=MAX, V_{IH}=2V	V_O=2.7V			20			20	μA
		V_O=0.4V			-20			-20	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	Condition A		6.1	10		6.1	10	mA
		Condition B		7.1	12		7.1	12	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:

A. Strobe grounded.

B. Strobe at 4.5V

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, or C (4 levels)	Y		23	32		23	34		27	42	ns
t_{PHL}				21	29		20	28		24	34	
t_{PLH}	A, B, or C (3 levels)	W		16	24		17	25		21	30	ns
t_{PHL}				16	25		15	24		17	26	
t_{PLH}	Any D	Y		11	17		11	20		18	26	ns
t_{PHL}				12	17		11	16		14	20	
t_{PLH}	Any D	W		9	16		10	17		13	19	ns
t_{PHL}				5	10		5	10		5	10	
t_{ZH}	Strobe	Y		8	13		8	14		10	16	ns
t_{ZL}				12	18		11	18		15	22	
t_{ZH}	Strobe	W		11	17		14	21		11	17	ns
t_{ZL}				12	19		12	18		13	19	
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C on page 2-174)												
t_{HZ}	Strobe	Y		10	15		8	13		7	12	ns
t_{LZ}				7	11		6	11		8	13	
t_{HZ}	Strobe	W		13	18		11	16		10	15	ns
t_{LZ}				7	11		6	10		7	14	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, or C (4 levels)	Y		25	34		26	37		33	44	ns
t_{PHL}				27	35		25	32		28	37	
t_{PLH}	A, B, or C (3 levels)	W		17	25		18	26		22	31	ns
t_{PHL}				19	27		18	27		20	29	
t_{PLH}	Any D	Y		13	20		14	22		20	28	ns
t_{PHL}				18	23		16	21		19	25	
t_{PLH}	Any D	W		10	17		11	18		14	21	ns
t_{PHL}				7	13		6	12		6	12	
t_{ZH}	Strobe	Y		11	16		11	17		13	19	ns
t_{ZL}				18	24		17	23		20	27	
t_{ZH}	Strobe	W		13	19		17	23		15	21	ns
t_{ZL}				14	21		16	22		17	23	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

Dual 4-Line-To-1-Line Multiplexer With Three-State Outputs

FEATURES

- **Three-state version of LS153**
- **Non-inverting**
- **Permits multiplexing from N lines to 1 line**
- **Performs parallel-to-serial conversion**

DESCRIPTION

The LS253 is a high-speed dual 4-line-to-1-line multiplexer with common select inputs and separate output control inputs for each half. Each half can select one bit of four and present it at the output in non-inverted form.

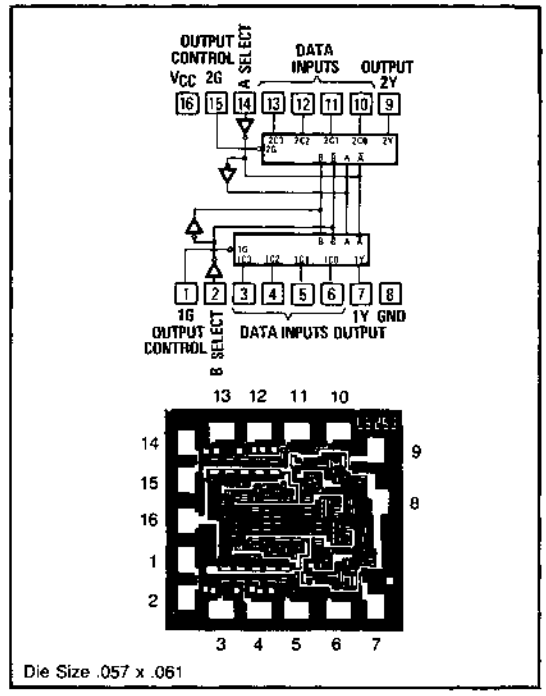
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

FUNCTION TABLE

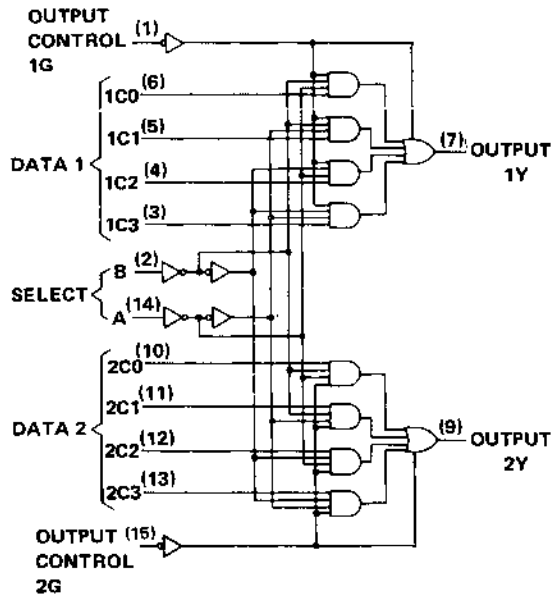
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

PIN-OUT DIAGRAM



LOGIC DIAGRAM



RAYTHEON

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=MAX		2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA					0.35	0.50	
$I_{O(off)}$	V_{CC}=MAX, V_{IH}=2V	V_O=2.7V			20			20	μA
		V_O=0.4V			-20			-20	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	Condition A		7	12		7	12	mA
		Condition B		8.5	14		8.5	14	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5V, all inputs grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Data	Y		9	15		7	12		9	15	ns
t_{PHL}				14	22		12	17		14	22	
t_{PLH}	Select	Y		20	30		18	25		20	30	ns
t_{PHL}				20	31		18	27		20	31	
t_{ZH}	Output Control	Y		12	21		10	16		12	21	ns
t_{ZL}				15	23		13	18		15	23	
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C on page 2-174)												
t_{HZ}	Output Control	Y		9	16		7	15		9	16	ns
t_{LZ}				13	22		12	19		13	22	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Data	Y		13	20		10	16		13	20	ns
t_{PHL}				18	27		15	21		18	27	
t_{PLH}	Select	Y		24	35		21	29		24	35	ns
t_{PHL}				24	36		21	29		24	36	
t_{ZH}	Output Control	Y		16	26		13	20		16	26	ns
t_{ZL}				19	28		16	21		19	28	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Dual 2-Line-To-4-Line Decoder/Demultiplexer With Three-State Outputs

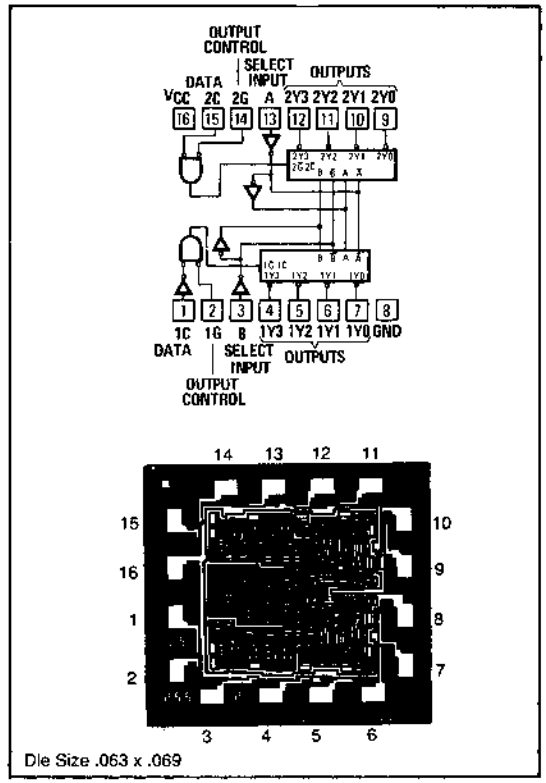
FEATURES

- Three-state version of LS155
- Applications:
  - Dual 2-Line-to-4-Line Decoder
  - Dual 1-Line-to-4-Line Demultiplexer
  - 3-Line-to-8-Line Decoder
  - 1-Line-to-8-Line Demultiplexer

DESCRIPTION

The LS255 features dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the output controls, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual controls permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

PIN-OUT DIAGRAM



Die Size .063 x .069

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		CONTROL	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	Z	Z	Z	Z
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

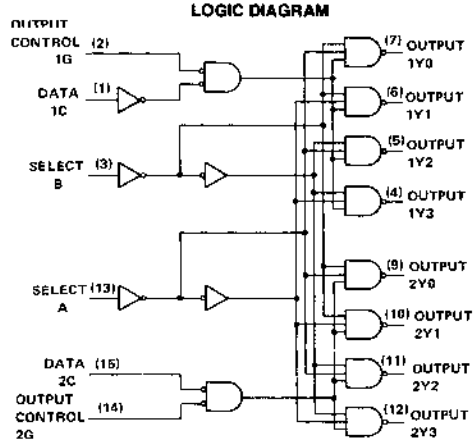
INPUTS				OUTPUTS			
SELECT		CONTROL	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	Z	Z	Z	Z
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			CONTROL OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

LOGIC DIAGRAM



RAYTHEON

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=MAX		2.4	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
$I_{O(off)}$	V_{CC}=MAX, V_{IH}=2V	V_O=2.7V			20			20	μA
		V_O=0.4V			-20			-20	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	Condition A		6	10		6	10	mA
		Condition B		11	17		11	17	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with the outputs open under the following conditions:
A. A, B, and 1C inputs at 4.5V, and 2C, 1G, and 2G inputs grounded.
B. Same as Condition A except inputs 1G and 2G at 4.5V.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, 1C or 2C	Y		15	21		13	18		15	21	ns
t_{PHL}				18	24		16	22		18	24	
t_{PLH}	A or B (3 levels)	Y		18	24		16	22		18	24	ns
t_{PHL}				22	29		20	26		22	29	
t_{ZH}	Output Control	Y		12	18		10	15		12	18	ns
t_{ZL}				14	20		12	18		14	20	
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C on page 2-174)												
t_{HZ}	Output Control	Y		11	18		9	15		11	18	ns
t_{LZ}				17	23		15	20		17	23	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	A, B, 1C or 2C	Y		19	27		16	22		19	27	ns
t_{PHL}				22	30		20	28		22	30	
t_{PLH}	A or B (3 levels)	Y		22	30		20	28		22	30	ns
t_{PHL}				26	34		24	32		26	34	
t_{ZH}	Output Control	Y		16	22		14	20		16	22	ns
t_{ZL}				18	26		16	22		18	26	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

Quadruple 2-Line-To-1-Line Multiplexers With Three-State Outputs

DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The LS257 presents true data; the LS258 presents inverted data. With Output Control HIGH, the outputs are forced to a high impedance state.

FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	LS257	LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

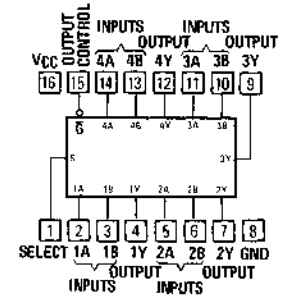
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

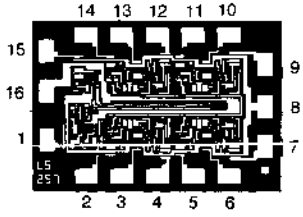
Low level at S selects A inputs.

High level at S selects B inputs.

PIN-OUT DIAGRAMS

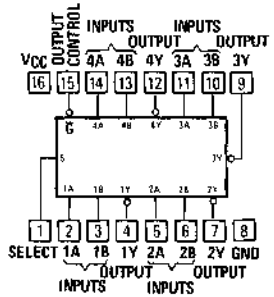
LS257

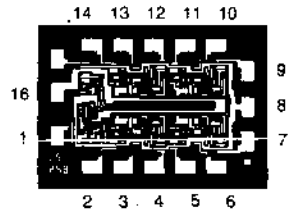




Die Size .047 x .066

LS258

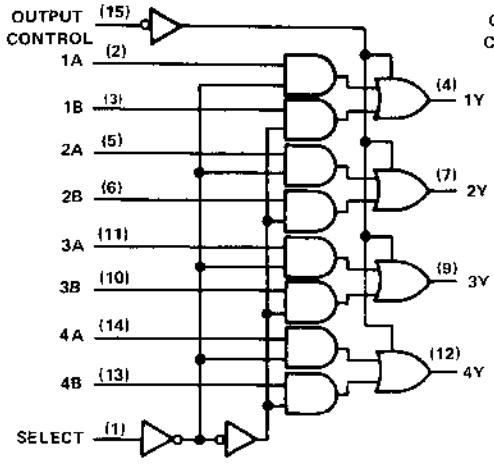




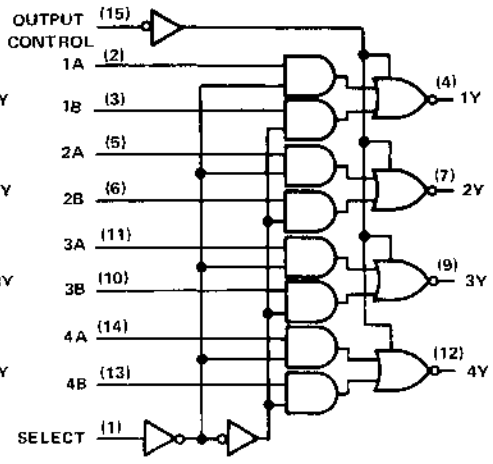
Die Size .047 x .066

LOGIC DIAGRAMS

LS257



LS258



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=MAX		2.4	3.4		2.4	3.1		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
			I_{OL}=8mA					0.35	0.5	
I_{OZH}		V_{CC}=MAX, V_{IH}=2V, V_O=2.4V				20			20	μA
I_{OZL}		V_{CC}=MAX, V_{IH}=2V, V_O=0.4V				-20			-20	μA
I_I	S input	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	Any other					0.1			0.1	
I_{IH}	S input	V_{CC}=MAX, V_I=2.7V				40			40	μA
	Any other					20			20	
I_{IL}	S input	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
	Any other					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	All outputs high	V_{CC}=MAX	LS257		5.9	10		5.9	10	mA
	All outputs low				9.2	16		9.2	16	
	All outputs off				10	17		10	17	
	All outputs high		LS258		4.1	7		4.1	7	
	All outputs low				6.2	11		6.2	11	
	All outputs off				7.0	12		7.0	12	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter		From (Input)	To (output)	−55°C			+25°C			+125°C			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. C on page 2-174)													
t_{PLH}	LS257	Data	Any		8	15		6	12		8	15	ns
t_{PHL}					9	15		7	12		9	15	
t_{PLH}	LS258	Data	Any		10	17		8	14		10	17	ns
t_{PHL}					7	15		5	12		7	15	
t_{PLH}	LS257	Select	Any		14	21		12	18		14	21	ns
t_{PHL}					14	21		12	18		14	21	
t_{PLH}	LS258	Select	Any		14	21		12	18		14	21	ns
t_{PHL}					12	21		10	18		12	21	
t_{ZH}	LS257	Output Control	Any		12	21		10	18		12	21	ns
t_{ZL}					12	19		10	16		12	19	
t_{ZH}	LS258	Output Control	Any		12	21		10	18		12	21	ns
t_{ZL}					13	21		11	18		13	21	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{HZ}	LS257	Output Control	Any		12	18		10	15		12	18	ns
t_{LZ}					12	21		10	18		12	21	
t_{HZ}	LS258	Output Control	Any		11	18		9	15		11	18	ns
t_{LZ}					10	18		8	15		10	18	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)													
t_{PLH}	LS257	Data	Any		12	19		10	17		12	19	ns
t_{PHL}					13	20		11	17		13	20	
t_{PLH}	LS258	Data	Any		14	22		12	19		14	22	ns
t_{PHL}					11	19		9	17		11	19	
t_{PLH}	LS257	Select	Any		18	25		16	23		18	25	ns
t_{PHL}					18	25		16	23		18	25	
t_{PLH}	LS258	Select	Any		18	25		16	23		18	25	ns
t_{PHL}					16	25		14	23		16	25	
t_{ZH}	LS257	Output Control	Any		16	25		14	23		16	25	ns
t_{ZL}					16	24		14	21		16	24	
t_{ZH}	LS258	Output Control	Any		16	25		14	23		16	25	ns
t_{ZL}					17	25		15	23		17	25	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

FEATURES

- Fast Multiplication . . . 5-Bit Product in 26ns Typ
- Power Dissipation . . . 110mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

DESCRIPTION

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

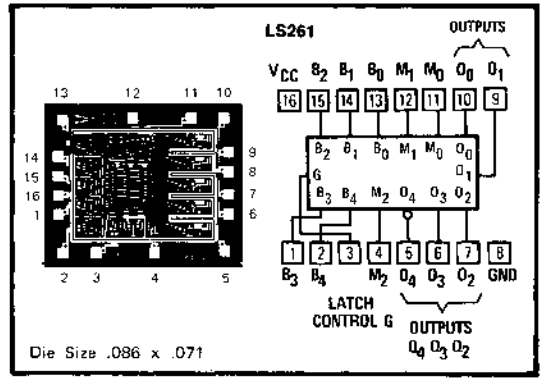
The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

The 9LS/54L261 is characterized for operation over the full military temperature range of −55°C to 125°C; the 9LS/74LS261 for operation from 0°C to 70°C.

PIN-OUT DIAGRAM



FUNCTION TABLE

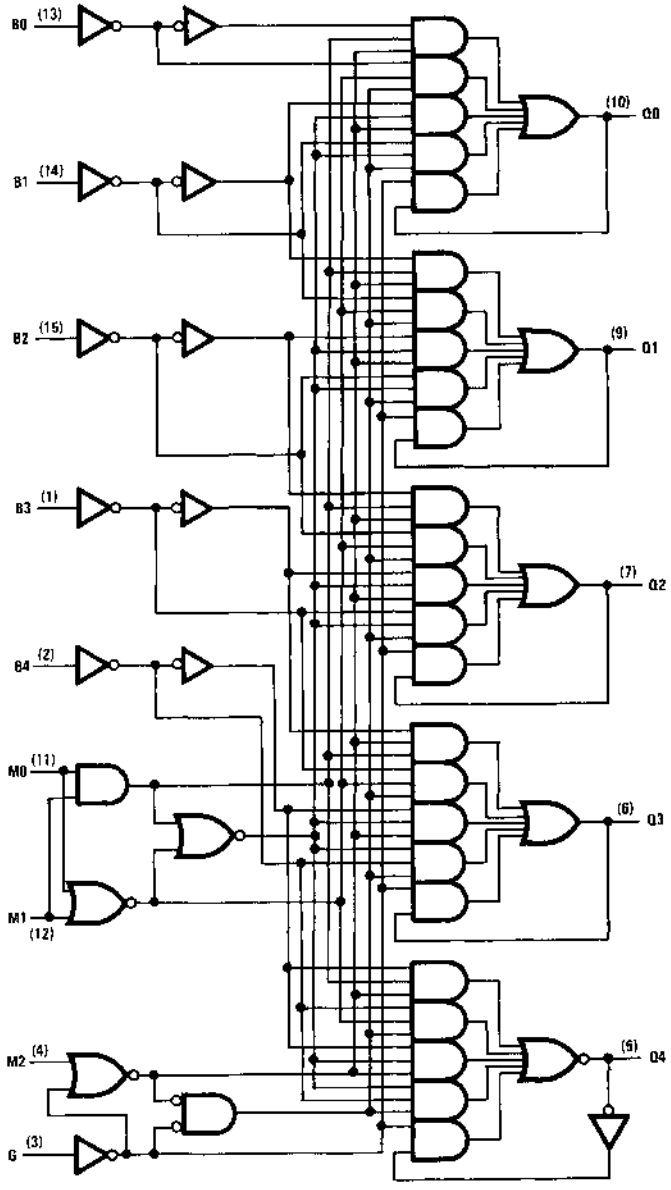
INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER M2	M1	M0	$\bar{Q}4$	Q3	Q2	Q1	Q0
L	X	X	X	$Q4_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\bar{B}4$	B4	B3	B2	B1
H	L	H	L	$\bar{B}4$	B4	B3	B2	B1
H	L	H	H	$\bar{B}4$	B3	B2	B1	B0
H	H	L	L	B4	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$	$\bar{B}0$
H	H	L	H	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	L	B4	$\bar{B}4$	$\bar{B}3$	$\bar{B}2$	$\bar{B}1$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant

$\bar{Q}4_0$ . . . $Q0_0$ = The logic level of the same output before the high-to-low transition of G.

B4 . . . B0 = The logic level of the indicated multiplicand (B) input

LOGIC DIAGRAM



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_w		25			25			ns
Setup time, t_{setup}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_{hold}	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		−55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.2	V
V_I	V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−1mA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX		−15		−100	−15		−100	mA
I_{CC}	V_{CC}=MAX, All inputs at 0V, Outputs open			22	38		22	40	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	−55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Enable G	Any Q		25	39		22	35		25	39	ns
t_{PHL}				23	34		20	30		23	34	
t_{PLH}	Any M input	Any Q		28	44		25	40		28	44	ns
t_{PHL}				25	39		22	35		25	39	
t_{PLH}	Any B input	Any Q		30	46		27	42		30	46	ns
t_{PHL}				27	41		24	37		27	41	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	Enable G	Any Q		30	44		26	40		30	44	ns
t_{PHL}				28	39		24	35		28	39	
t_{PLH}	Any M input	Any Q		33	49		29	45		33	49	ns
t_{PHL}				30	44		26	40		30	44	
t_{PLH}	Any B input	Any Q		35	51		31	47		35	51	ns
t_{PHL}				32	46		28	42		32	46	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only.
All 50pF specifications are for 9LS only.

FEATURES

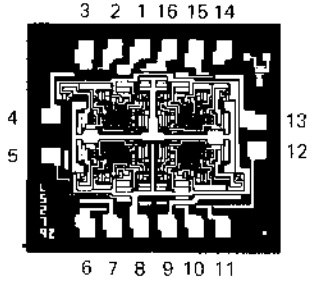
- **Functionally and Mechanically Identical to 54279**
- **Features Low Power Dissipation of 19 mW Typical**

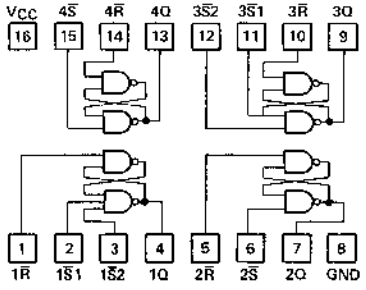
FUNCTION TABLE (EACH LATCH)

INPUTS $\overline{S}$†	INPUTS $\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable: that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

PIN-OUT DIAGRAM





logic: see function table

Die Size .065 x .059

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Unit
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1. Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†			9LS/54LS			9LS/74LS			Unit
				Min.	Typ‡	Max.	Min.	Typ‡	Max.	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_I Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{IL} = V_{IL} max		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.4			−0.4	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC} Supply current	V_{CC} = MAX,	See Note 2			3.8	7		3.8	7	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2. I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5 V, and all outputs open.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)												
t_{PLH}	$\overline{S}$	Q		15	26		12	22		15	26	ns
t_{PHL}	$\overline{S}$	Q		12	19		9	15		12	19	ns
t_{PHL}	$\overline{R}$	Q		19	30		15	27		19	30	ns
Test Conditions: C_L = 50pF, R_L = 2.0k (See Fig. A, page 2-174)												
t_{PLH}	$\overline{S}$	Q		19	30		16	26		19	30	ns
t_{PHL}	$\overline{S}$	Q		16	23		13	19		16	23	ns
t_{PHL}	$\overline{R}$	Q		22	35		19	31		23	35	ns

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

4-Bit Bi-Directional Shift Register With Three-State Outputs

LS295A

FEATURES

- **Three-state version of LS95B parallel-access shift register**

DESCRIPTION

This 4-bit register features parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The register has three modes of operation:

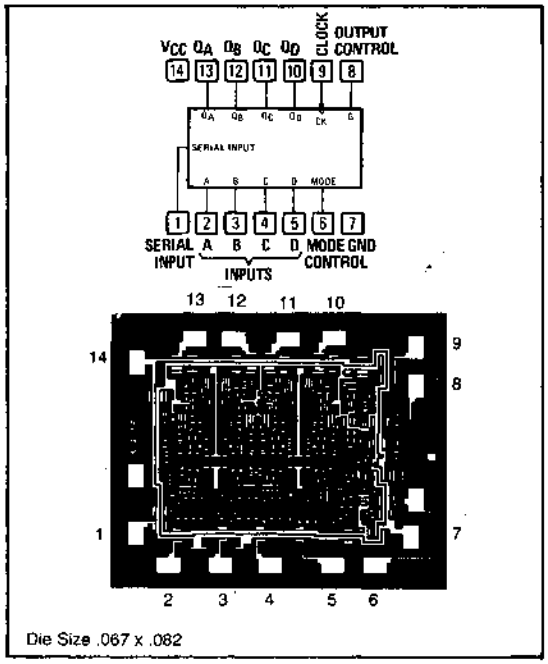
Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

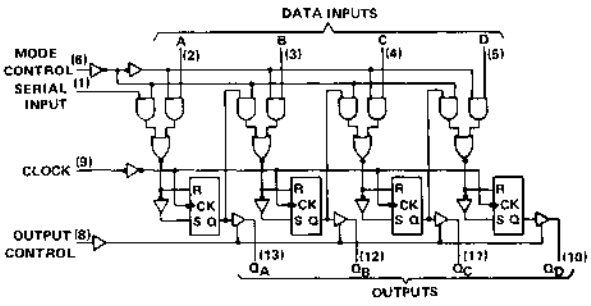
Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus bus line; however, sequential operation of the register is not affected.

PINOUT DIAGRAM



LOGIC DIAGRAM



INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	↑	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (*any* input, including transitions)
↑ = transition from high to low level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Setup time, high-level or low-level data, t_{setup}	10			10			ns
Hold time, high-level or low-level data, t_{hold}	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=MAX		2.4	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
		I_{OL}=8mA					0.35	0.5	
I_{OZH}	V_{CC}=MAX, V_{IL}=V_{IL}max, V_O=2.7V				20			20	μA
I_{OZL}	V_{CC}=MAX, V_{IH}=2V, V_O=0.4V				-20			-20	μA
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX	Condition A		14	23		14	23	mA
		Condition B		15	25		15	25	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:

A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.

B. Output control and clock input grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
f_{max}				30	40					MHz
t_{PLH}		29	38		27	35		29	38	ns
t_{PHL}		37	48		35	45		37	48	ns
t_{ZH}		12	21		10	18		12	21	ns
t_{ZL}		12	21		10	18		12	21	ns
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. C on page 2-174)										
t_{HZ}		21	32		19	28		21	32	ns
t_{LZ}		26	36		24	32		26	36	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		32	42		30	39		32	42	ns
t_{PHL}		40	52		38	49		40	52	ns
t_{ZH}		15	25		13	22		15	25	ns
t_{ZL}		15	25		13	22		15	25	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

RAYTHEON

FEATURES

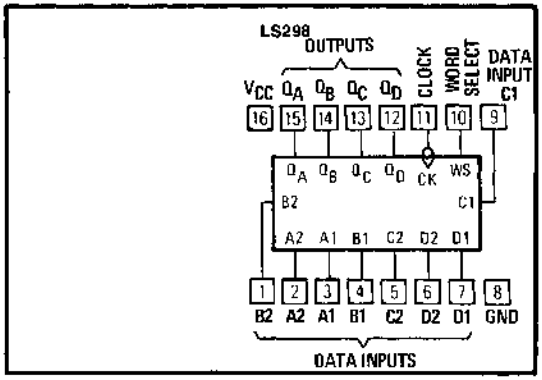
- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock.
- Applications:
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data.
  - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability.
  - Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities.

DESCRIPTION

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (54157/74157 or 54LS157/74LS157 and 54175/74175 or 54LS175/74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

PIN-OUT DIAGRAM

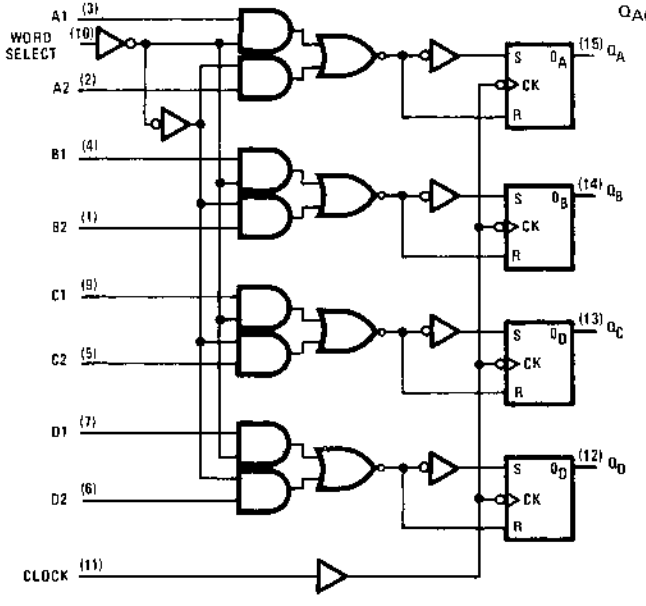


FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0} etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

LOGIC DIAGRAM



Dynamic input activated by a transition from a high level to a low level

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-400			-400	μA
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{setup}	Data	15			15			ns
	Word select	25			25			
Hold time, t_{hold}	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-6		-40	-5		-42	mA
I_{CC}††	V_{CC}=MAX,			13	21		13	21	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5V, followed by ground, to the clock input.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		20	31		18	27		20	31	ns
t_{PHL}		23	35		21	32		23	35	
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. A, page 2-174)										
t_{PLH}		23	36		21	32		23	36	ns
t_{PHL}		26	40		24	37		26	40	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

Hex Buffers, Tri-State, Common Enable — LS365 LS366

Hex Buffers, Tri-State, 4-Bit and 2-Bit — LS367 LS368

DESCRIPTION

The LS365/366/367/368 are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15TTL Unit Loads on 60 Low Power Schottky loads when the Enable ($\overline{E}$) is LOW.

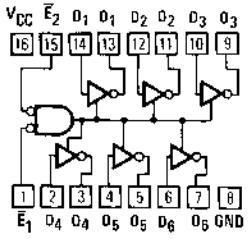
When Output Enable Input ($\overline{E}$) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

PIN-OUT DIAGRAMS

LS365
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE

TRUTH TABLE

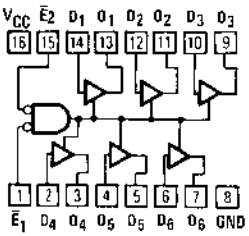
INPUTS $\overline{E}_1$	INPUTS $\overline{E}_2$	INPUTS D	OUTPUTS
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)



LS366
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE

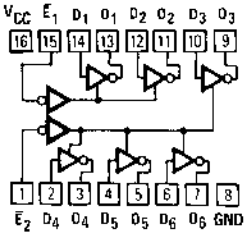
TRUTH TABLE

INPUTS $\overline{E}_1$	INPUTS $\overline{E}_2$	INPUTS D	OUTPUTS
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)



LS367
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS

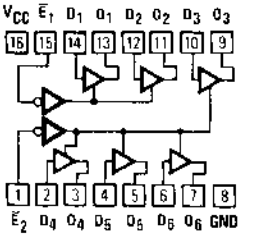
INPUTS $\overline{E}$	INPUTS D	OUTPUTS
L	L	L
L	H	H
H	X	(Z)



LS368
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS

TRUTH TABLE

INPUTS $\overline{E}$	INPUTS D	OUTPUTS
L	L	H
L	H	L
H	X	(Z)



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-Level Output Current, I_{OH}			-1			-2.6	mA
Low-Level Output Current, I_{OL}			12			24	mA
Operating Free-Air Temperature, T_A	-55		125	0		75	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}	Guaranteed Input HIGH Voltage for All Inputs		2.0			2.0			V
V_{IL}	Guaranteed Input LOW Voltage for All Inputs				.7	2.0		.8	V
V_{CD}	V_{CC}=MIN, I_{IN}=-18mA			-0.65	-1.5		-0.65	-1.5	V
V_{OH}	V_{CC}=MIN, V_{IN}=V_{IH} or V_{IL} per Truth Table	I_{OH}=-1.0mA	2.4	3.4					V
		I_{OH}=-2.6mA				2.4	3.1		
V_{OL}	V_{CC}=MIN, V_{IN}=V_{IH} or V_{IL} per Truth Table	I_{OL}=12mA		0.25	0.4		0.25	0.40	V
		I_{OL}=24mA					0.35	0.5	
I_{OZH}	V_{CC}=MAX, V_{out}=2.4V, $\overline{E}$=2.0V				20			20	µA
I_{OZL}	V_{CC}=MAX, V_{out}=0.4V, $\overline{E}$=2.0V				-20			-20	µA
I_{IH}	V_{CC}=MAX, V_{IN}=2.7V				20			20	µA
	V_{CC}=MAX, V_{IN}=7.0V				-.1			-.1	mA
I_{IL}	V_{CC}=MAX, V_{IN}=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX, V_{OUT}=0V		-30		-100	-30		-100	mA
I_{CC}	V_{CC}=MAX, V_{IN}=0V, $\overline{E}$=4.5V	LS365/367		13.5	24		13.5	24	mA
		LS366/368		11.8	21		11.8	21	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	-55°C			+25°C			+125°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 45pF (See Fig. A, page 2-174)												
t_{PLH} (LS365/367)	D_i	O_i		9	14		7	10		9	14	ns
t_{PHL} (LS365/367)				12	20		10	16		12	20	
t_{PLH} (LS366/368)	D_i	O_i		9	14		7	10		9	14	ns
t_{PHL} (LS366/368)				12	20		10	16		12	20	
t_{ZH}	$\overline{E}$	O_i		12	20		10	16		12	20	ns
t_{ZL}				20	36		18	30		20	36	
Test Conditions: C_L = 5pF, R_L = 667Ω (See Fig. C, page 2-174)												
t_{LZ}	$\overline{E}$	O_i		12	20		10	15		12	20	ns
t_{HZ}				19	27		17	23		19	27	
Test Conditions: C_L = 125pF, (See Fig. A, page 2-174)												
t_{PLH} (LS365/367)	D_i	O_i		12	20		10	15		12	20	ns
t_{PHL} (LS365/367)				15	26		15	21		15	26	
t_{PLH} (LS366/368)	D_i	O_i		12	20		10	15		12	20	ns
t_{PHL} (LS366/368)				15	26		15	21		15	20	
t_{ZH}	$\overline{E}$	O		16	26		13	20		16	26	ns
t_{ZL}				24	42		21	35		24	40	

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

4-Bit Cascadable Shift Registers with 3-State Outputs

LS395A

FEATURES

- Three-State, 4-Bit, Cascadable, Parallel-In, Parallel-Out Registers
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 75mW Typical (Enabled)
- Applications: N-Bit Serial-To-Parallel Converter
  N-Bit Parallel-To-Serial Converter
  N-Bit Storage Register
- Pin for pin compatible with LS395

DESCRIPTION

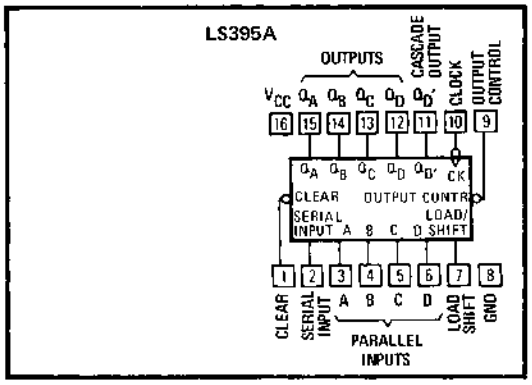
These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independentiy from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the reigsters is not affected. During the high-impedance mode, the output at $Q_{D'}$ is still available for cascading.

The 9LS/54LS395A is characterized for operation over the full military temperature range of −55°C to 125°C; the 9LS/74LS395A is characterized for operation from 0°C to 70°C.

PIN-OUT DIAGRAM



FUNCTION TABLE

INPUTS					3-STATE OUTPUTS				CASCADE
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A B C D	Q_A	Q_B	Q_C	Q_D	OUTPUT Q_D
L	X	X	X	X X X X	L	L	L	L	L
H	H	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a b c d	a	b	c	d	d
H	L	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D are not affected.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Setup time, high-level or low-level data, t_{setup}	20			20			ns
Hold time, high-level or low-level data, t_{hold}	10			10			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*			9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IL}=V_{IL}max,	V_{IH}=2V, I_{OH}=MAX		2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC}=MIN V_{IL}=V_{IL} max, V_{IH}=2V	Q_A, Q_B	I_{OL}=12mA		0.25	0.4		0.25	0.40	V
		Q_C, Q_D	I_{OC}=24mA					0.35	0.50	
		Q_D	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
			I_{OL}=8mA					0.35	0.50	
I_{OZH}	V_{CC}=MAX, V_O=2.7V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			20			20	µA
I_{OZL}	V_{CC}=MAX, V_O=0.4V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			-20			-20	µA
I_I	V_{CC}=MAX,	V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V				20			20	µA
I_{IL}	V_{CC}=MAX,	V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX			-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX,		Condition A		18	29		18	29	mA
			Condition B		15	25		15	25	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:

A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.

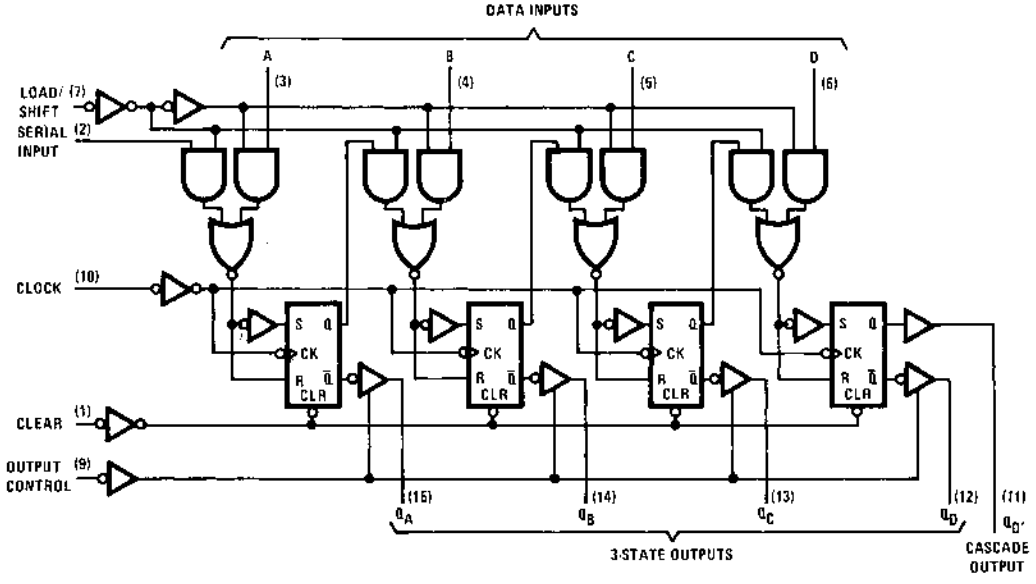
B. Output control and clock input grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameters	–55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. C, page 2-174)										
f_{max}				25	35					MHz
t_{PHL} Clear to output		27	40		23	35		27	40	ns
t_{PLH}		27	40		23	35		27	40	ns
t_{PHL}		24	35		20	30		24	35	ns
t_{PZH}		17	25		13	20		17	25	ns
t_{PZL}		28	41		24	36		28	41	ns
t_{PHZ}		15	22		11	17		15	22	ns
t_{PLZ}		19	27		15	23		19	27	ns
Test Conditions: C_L = 5.0pF, R_L = 2kΩ (See Fig. C, page 2-174)										
t_{HZ}		13	22		11	17		13	22	ns
t_{LZ}		18	27		15	23		18	27	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. C, page 2-174)										
t_{PHL}		30	44		26	39		30	44	ns
t_{PLH}		30	44		26	39		30	44	ns
t_{PHL}		27	38		23	34		27	38	ns
t_{PZH}		20	29		18	24		22	27	ns
t_{PZL}		31	45		27	40		30	45	ns
t_{PHZ}		18	26		14	20		19	26	ns
t_{PLZ}		22	32		18	27		22	32	ns

Note: AC specification shown under –55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

LOGIC DIAGRAM



4-By-4 Register Files with 3-State Outputs

FEATURES

- **Separate Read/Write Addressing Permits Simultaneous Reading and Writing**
- **Fast Access Times . . . Typically 20 ns**
- **Organized as 4 Words of 4 Bits**
- **Expandable to 512 Words of n-Bits**
- **For Use as:**
  - **Scratch-Pad Memory**
  - **Buffer Storage Between Processors**
  - **Bit Storage in Fast Multiplication Designs**
- **3-State Outputs**

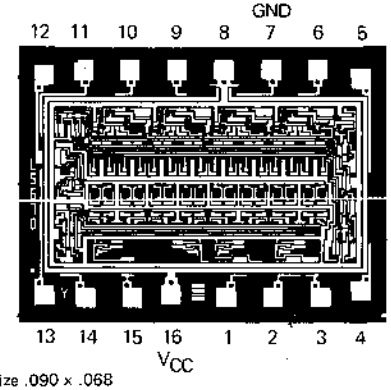
DESCRIPTION

The LS670 and MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

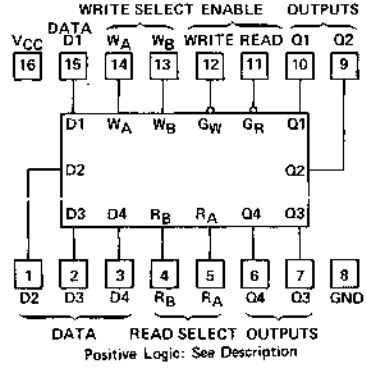
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.



Die Size .090 x .068



RAYTHEON

LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

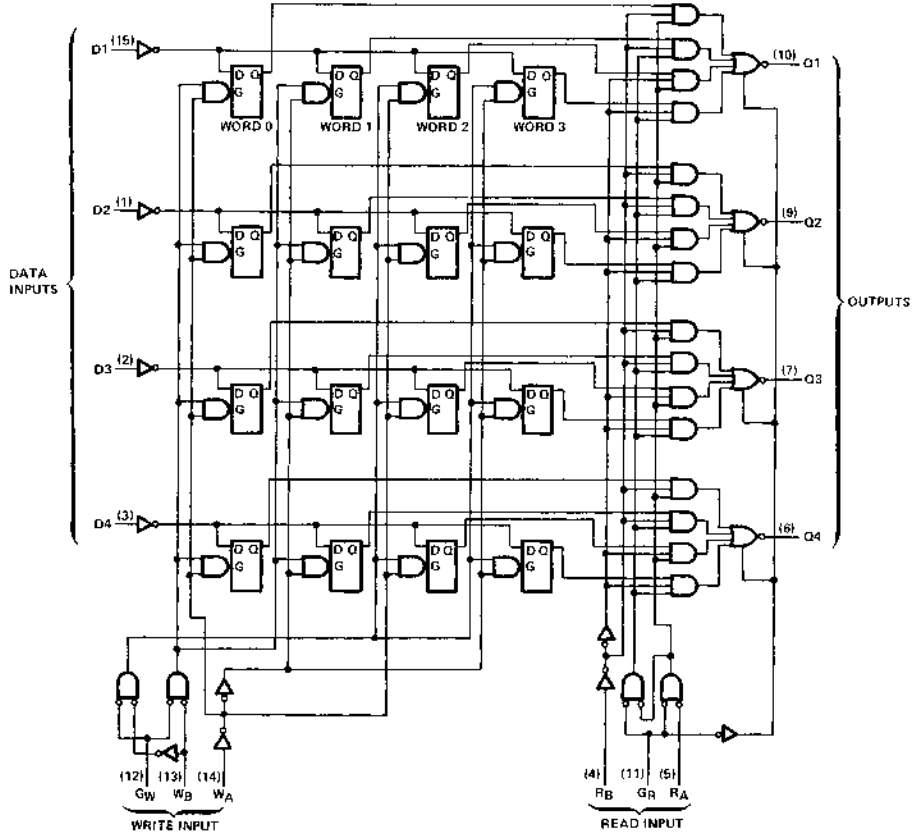
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	Write select with respect to write enable, $t_{setup(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_{hold(D)}$	15			15			ns
	Write select with respect to write enable, $t_{hold(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temparature range, T_A		−55		125	0		70	°C

NOTES 1. Voltage values are with respect to network ground terminal.

2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†			9LS/54LS			9LS/74LS			Unit
					Min.	Typ‡	Max.	Min.	Typ‡	Max.	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V,	I_{OH} = −1mA	2.4	3.4					V
				I_{OH} = −2.6mA				2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V,	I_{OL} = 4mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2V,	V_O = 2.7V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2V,	V_O = 0.4V			−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7V	Any D, R, or W				0.1			0.1	mA
			G_W				0.2			0.2	
			G_R				0.3			0.3	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	Any D, R, or W				20			20	μA
			G_W				40			40	
			G_R				60			60	
I_{IL}	Low-level input current	V_{CC} = MAX	Any D, R, or W				−0.4			−0.4	mA
			G_W				−0.8			−0.8	
			G_R				−1.2			−1.2	
I_{OS}	Short-circuit output current#	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4			30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5V, T_A = 25°C.

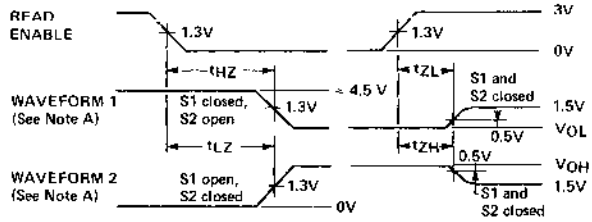
#Not more than one output should be shorted at a time.

NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	−55°C			+25°C			+125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0kΩ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. A on page 2-174)												
t_{PLH}	Read Select	Any Q		26	44		23	40		26	45	ns
t_{PHL}				28	49		25	45		28	50	
t_{PLH}	Write enable	Any Q		30	49		26	45		30	50	ns
t_{PHL}				31	54		28	50		31	55	
t_{PLH}	Data	Any Q		28	49		25	45		28	50	ns
t_{PHL}				26	44		23	40		26	45	
Test Conditions: C_L = 5pF, R_L = 2.0kΩ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. C on page 2-174)												
t_{ZH}	Read enable	Any Q		18	39		15	35		18	40	ns
t_{ZL}				25	44		22	40		25	45	
t_{HZ}				33	54		30	50		33	55	
t_{LZ}				19	39		16	35		19	40	
Test Conditions: C_L = 50pF, R_L = 2.0kΩ (See Figs. 1, 2, 3 on pages 2-172 and 2-173 and Fig. A on page 2-174)												
t_{PLH}	Read Select	Any Q		30	49		27	44		31	50	ns
t_{PHL}				32	54		29	49		33	55	
t_{PLH}	Write enable	Any Q		34	54		30	49		35	55	ns
t_{PHL}				35	59		32	54		36	60	
t_{PLH}	Data	Any Q		32	53		29	49		33	55	ns
t_{PHL}				30	49		27	44		31	50	

Note: AC specification shown under −55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

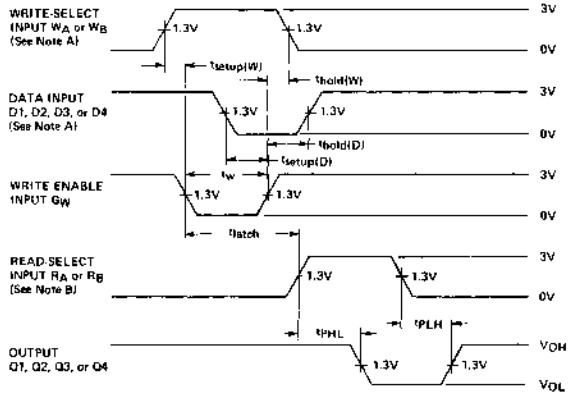
FIGURE 1

NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.

B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION



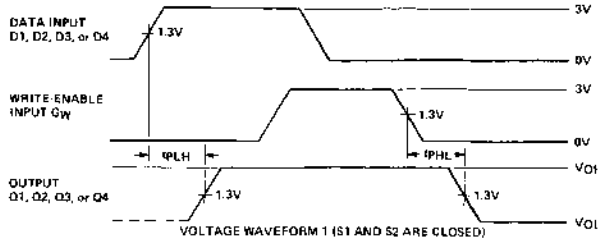
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

FIGURE 2

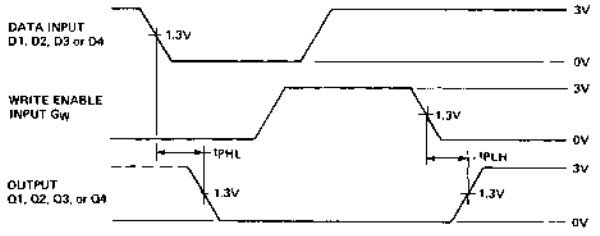
NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read select input, the read-enable input is low.

C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.



VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)

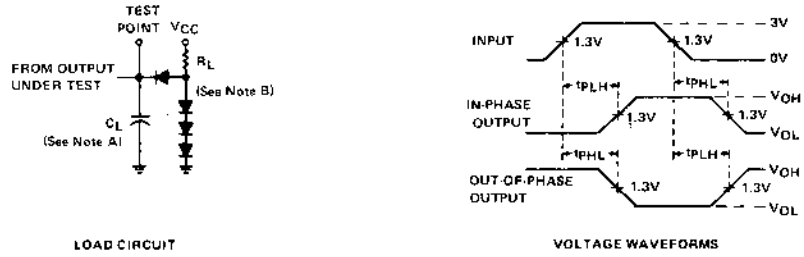


VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

FIGURE 3

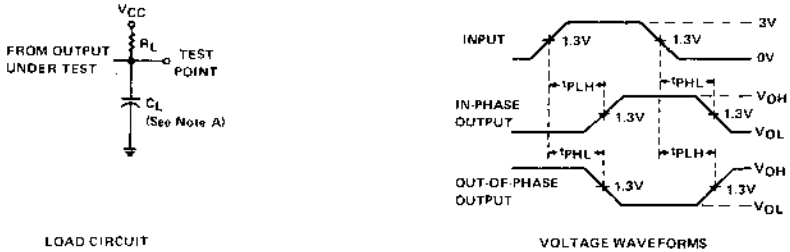
NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.



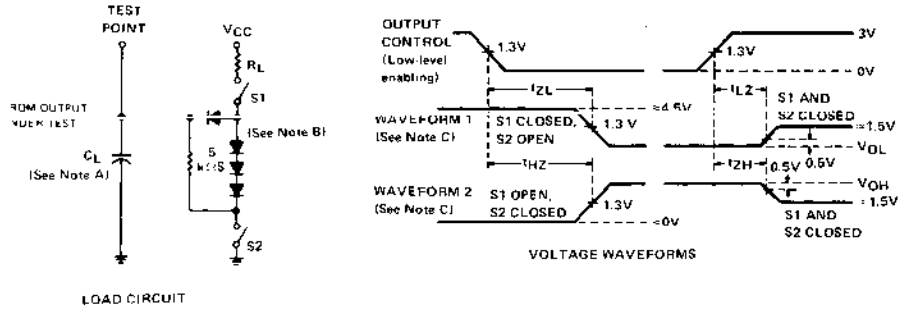
LOAD CIRCUIT VOLTAGE WAVEFORMS

FIGURE A — FOR TOTEM-POLE OUTPUTS



LOAD CIRCUIT VOLTAGE WAVEFORMS

FIGURE B — FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT VOLTAGE WAVEFORMS

FIGURE C — FOR THREE-STATE OUTPUTS

NOTES:

A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

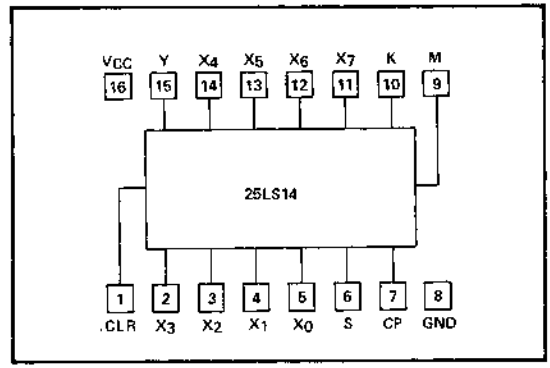
E. All input pulses are supplied by generators having the following characteristics. $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, and $t_w = 100$ ns.

25LS
HIGH-PERFORMANCE
LOW-POWER SCHOTTKY

8-Bit Serial/Parallel Two's Complement Multiplier

FEATURES

- Two's Complement Multiplication Without Correction
- Magnitude Only Multiplication
- Cascadable for any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 25 MHz Minimum Clock Frequency
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883



FUNCTIONAL DESCRIPTION

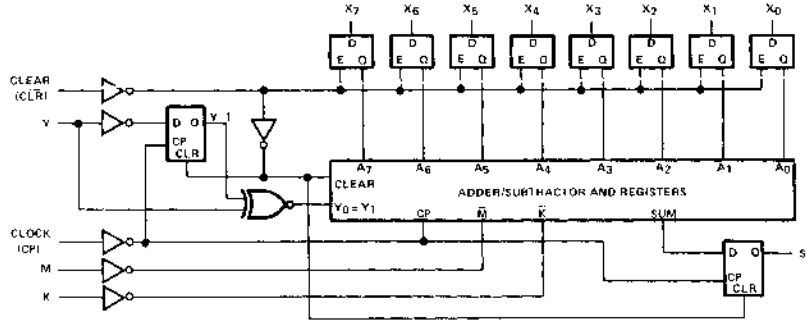
The 25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream—least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The 25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM



Recommended Operating Conditions

	Military			Commercial			Units
	Min.	Nom	Max.	Min.	Nom.	Max.	
Supply Voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level Output Current, I_{OH}			−1			−1	mA
Low-level Output Current, I_{OL}		8	12		8	12	mA
Operating Free-Air Temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters		Test Conditions (Note 1)		Military			Commercial			Units
				Min.	Typ. (2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = -1.0mA V_{IN} = V_{IH} or V_{IL}		2.5	3.4		2.7	3.4		V
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4			0.40	V
			I_{OL} = 12mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = -18mA				-1.2			-1.2	V
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			-0.48			-0.48	mA
			K' $\overline{CLR}$			-1.2			-1.2	
			CP			-1.6			-1.6	
			Y			-3.2			-3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20			20	µA
			K, $\overline{CLR}$			30			30	
			CP			40			40	
			Y			80			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		-40		-100	-40		-100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			91	155		91	155	mA

Switching Characteristics, V_{cc} = 5V

Parameter	From (Input)	To (Output)	+25°C			Units
			Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	Clock	Y		13	20	ns
t_{PHL}	Clock	Y		13	20	ns
t_{PHL}	Clear	X		17	25	ns
t_s	Set up time	Y to Clock	32			ns
t_h	Hold time		0			ns
t_s	Set up time	K to Clock	18			ns
t_h	Hold time		0			ns
t_s	Set up time	Xi to Clear	13			ns
t_h	Hold time		0			ns
t_{pw}	Clock Pulse Width	Clock Hi	15			ns
		Clock Low	15			ns
t_{pw}	Clear Pulse Width		20			ns
t_s	Clear Recovery Time		18			ns
f_{max}	Max. Clock Frequency		25	40		MHz

FUNCTION TABLE

Inputs						Internal	Output	Function
$\overline{CLR}$	CP	K	M	X_i	Y	Y_{-1}	S	
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

H = HIGH
L = LOW
↑ = LOW to HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

DEFINITION OF FUNCTIONAL TERMS

X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7 The eight data inputs for the multiplicand (X) data.

Y The serial input for the multiplier (Y) data—least significant bit first.

S The serial output for the product of X · Y—least significant bit first.

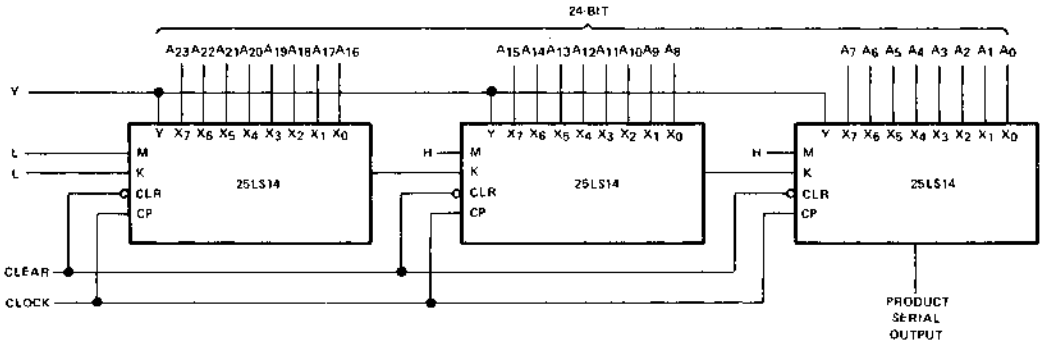
CP Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.

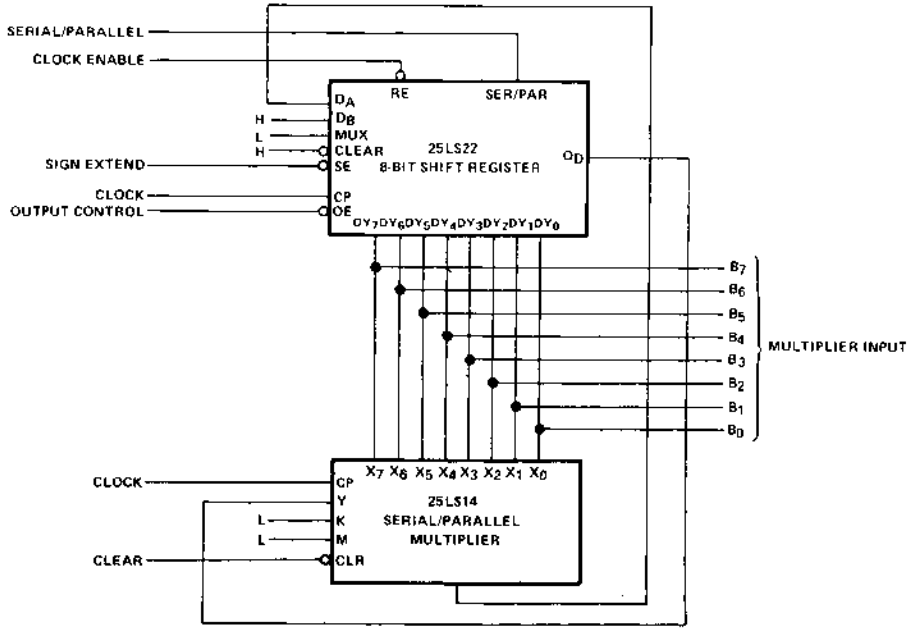
CLR Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.

K The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.

M The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

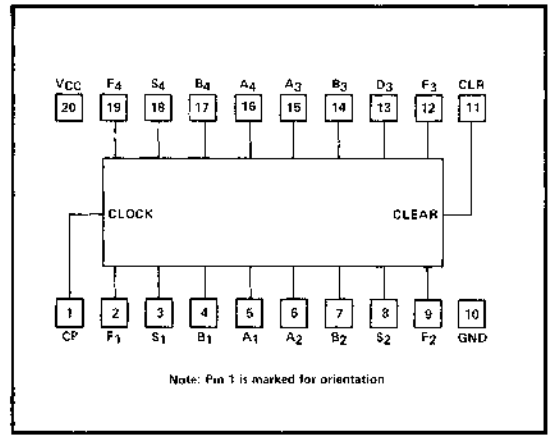
APPLICATIONS





FEATURES

- **Four Independent Adder/Subtractors**
- **Use with Two's Complement Arithmetic**
- **Magnitude Only Addition/Subtraction**
- **Advanced Low-Power Schottky Processing**
- **100% Reliability Assurance Testing in Compliance With MIL-STD-883**



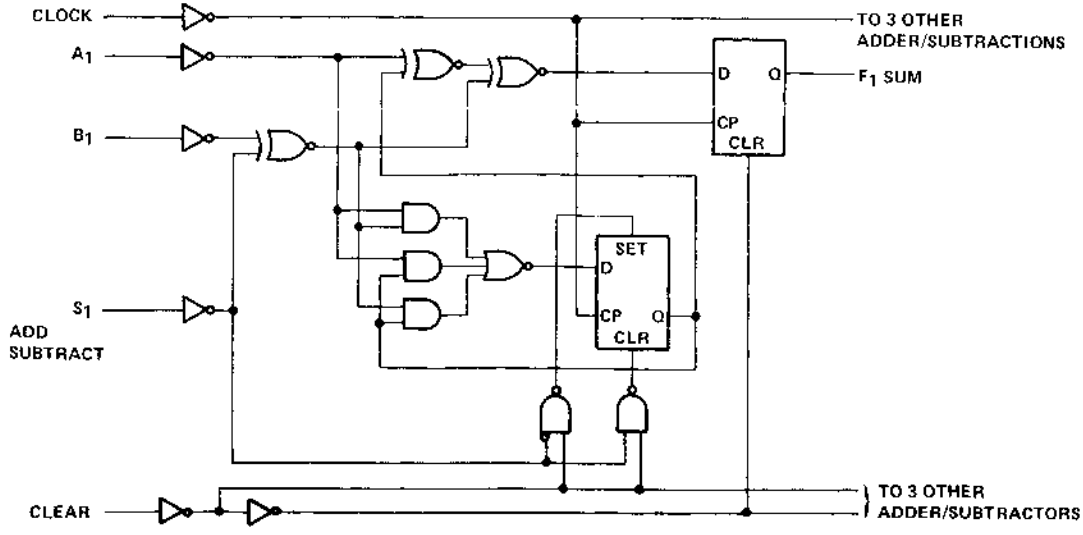
DESCRIPTION

The 25LS15 is a serial/parallel two's complement adder/subtractor designed for use in association with the 25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic one in subtract mode. This least significant plus one is self propagating in the subtract mode as long as zeroes are applied at the LSB's.

The 25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in fast fourier transforms.

LOGIC DIAGRAM
(One of Four Similar Functions)



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Recommended Operating Conditions

	Military			Commercial			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5.0	5.25	V
High-Level Output Current I_{OH}			-440			-440	μA
Low Level Output Current I_{OL}			8			8	mA
Operating Free Air Temperature	-55		+125	0		+70	°C

Electrical characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)		Military			Commercial			Units
				Min.	Typ. (Note 2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = -440μA V_{IN} = V_{IH} or V_{IL}		2.5			2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	Volts
			I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = -18mA				1.5			1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				-0.36			-0.36	Volts
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20			20	Volts
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1			0.1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		-30		-85	-30		-85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.			48	75		48	75	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Input Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

Switch Characteristics V_{CC} = 5.0V, T_A = +25°C

Parameters	From (Input)	To (Output)		+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{PLH}	Clock	F			14	22	ns
t_{PHL}					14	22	
t_{PHL}	Clear	F			20	30	ns
t_s	Set up time	A, B, S		10			ns
t_h	Hold time			0			
t_s	Clear Recovery time			25			ns
t_h	Clear Hold time			0			
t_{pw}	Clock Pulse Width	Clock	HIGH	17			ns
			LOW	17			
t_{pw}	Clear Pulse Width			20			ns
f_{MAX}	Max. Clock Frequency			30	40		MHz

FUNCTION TABLE

External Inputs					Internal Point		Output	Function
CP	CLR	S	A	B	C	C_1	F	
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	Add
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	Subtract
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data In the Carry Flip-Flop Before the Clock Transition
C_1 = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

A_1,A_2,A_3,A_4 The "A" input into each adder/subtractor

B_1,B_2,B_3,B_4 The "B" input into each adder/subtractor

S_1,S_2,S_3,S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A−B.

F_1,F_2,F_3,F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

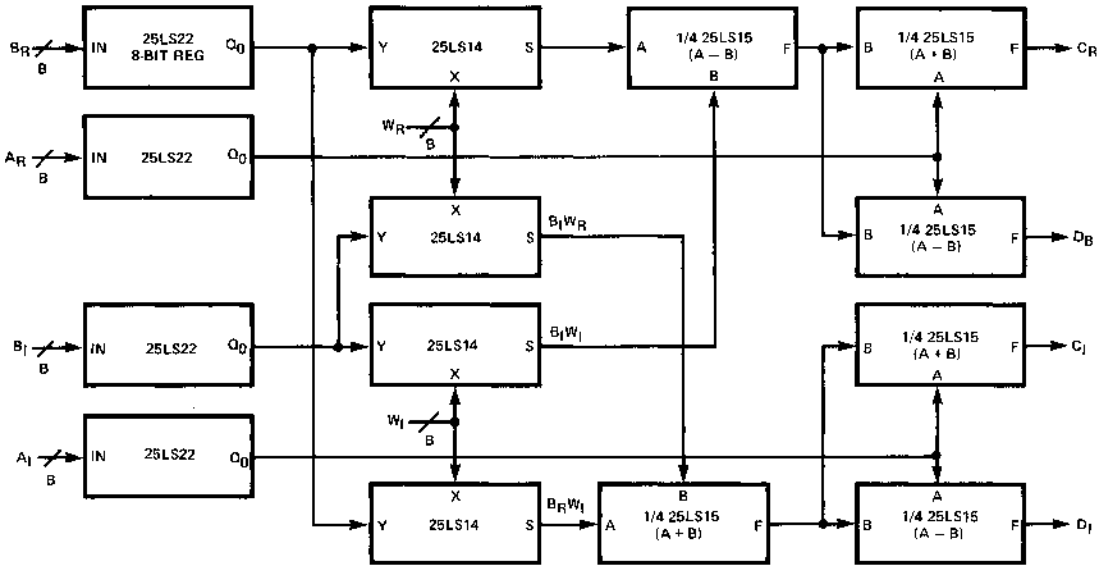
$A = A_R + jA_I$
$B = B_R + jB_I$
$W = W_R + iW_I$

The outputs C and D are also complex numbers and are evaluated as:

$C = C_R + jC_I = (A_R + B_R W_R - B_I W_I) + j(A_I + B_R W_I + B_I W_R)$
$D = C_R + jD_I = (A_R - B_R W_R + B_I W_I) + J(A_I - B_R W_I - B_I W_R)$

The four multiplications can be implemented using four 25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the 25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

FAST FOURIER TRANSFORM (FFT) BUTTERFLY



An FFT butterfly connection for complex arithmetic inputs and outputs.

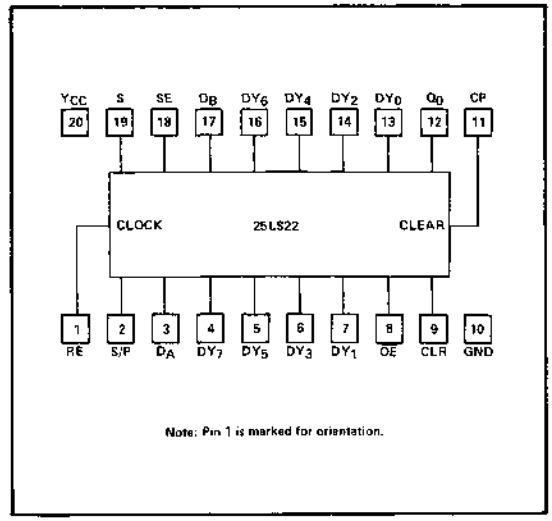
FEATURES

- Three-State Outputs
- Multiplexed Serial Data Input
- Sign Extend Function
- Advanced Low-Power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

DESCRIPTION

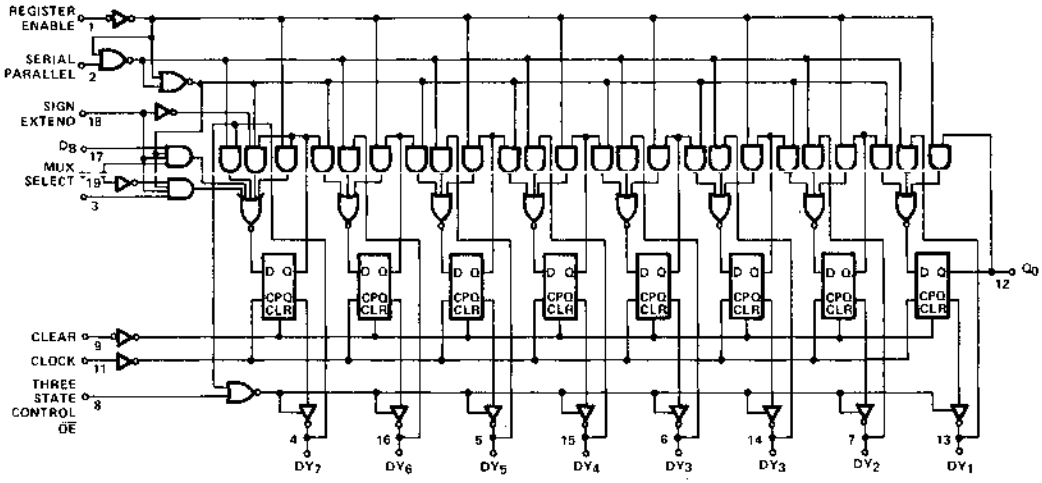
The 25LS22 is an 8-bit Serial/Parallel register with 3-state outputs. Data may also be loaded in a serial manner from inputs D_A or D_B under control of a multiplexer select input A register enable function also provides parallel load, shift and hold functions.

The 25LS22 has a sign extend function which is specifically designed for use with the 25LS14 eight by one serial/parallel two's complement multiplier. Typical shift frequency is 50MHz. The 25LS22 is packaged in a standard 20-pin package.



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



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Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	V
High Level Output Current I_{OH}	Q_0			-0.44			-0.44	mA
	DY_i			-1.0			-2.6	
Low Level Output Current I_{OL}			4	8		4	8	mA
Operating Free Air Temperature		-55		+125	0		70	°C

Electrical Characteristics Over Operating Temp. Range (Unless Otherwise Noted)

	Description	Test Conditions (Note 1)		Military			Commercial			Unit
				Min.	Typ. (2)	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q_0, I_{OH} = -440µA	2.5			2.7			V
			DY_i, I_{OH} = -1.0mA	2.4			2.4			
			DY_i, I_{OH} = -2.6mA	2.4			2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	V
			I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = -18mA				-1.5			-1.5	V
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{SE}$			-1.08			-1.08	mA
			S			-0.72			-0.72	
			Others			-0.36			-0.36	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)	$\overline{SE}$			60			60	µA
			S			40			40	
			Others			20			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V (Except DY_i)	SE			0.3			0.3	mA
			S			0.2			0.2	
			Others			0.1			0.1	
I_O	Off State (High Impedance) Output Current (DY_i)	V_{CC} = MAX.	V_O = 2.4V			40			40	µA
			V_O = 0.4V			-100			-100	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		-30		-85	-30		-85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			40	65		40	65	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = +25°C

Parameters	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 50pF, R_L = 2kΩ (see Fig. C on page 2-174)						
t_{PLH}	Clock	DY_i		16.5	24	ns
t_{PHL}				18	26	
t_{PHL}	Clear	DY_i		23	30	ns
t_{PLH}	Clock	Q_0		16.5	24	ns
t_{PHL}				18	26	
t_{PHL}	Clear	Q_0		23	30	ns
Test Conditions: C_L = 15pF, R_L = 2kΩ (see Fig. C on page 2-174)						
t_{ZH}	$\overline{OE}$	DY_i		13	21	ns
t_{ZL}				18	26	
t_{HZ}				13	21	
t_{LZ}				18	26	
t_{ZH}	SER/PAR	DY_i		18	26	ns
t_{ZL}				23	32	
t_{HZ}				18	26	
t_{LZ}				23	32	
t_s	Set Up Time RE To Clock		20			ns
t_s	Set Up Time SE To Clock		10			
t_s	Set Up Time S To Clock		15			
t_s	Set Up Time DA/DB to Clock		15			
t_s	Set Up Time DY_i To Clock		15			
t_s	Clear to Recovery To Clock		8.0			
t_s	Set Up Time S/P To Clock		15			ns
t_h	Hold Time Any Input		0			
t_h	Clear Hold Time		0			ns
t_{pw}	Clock Pulse Width	HIGH	8.0			ns
		LOW	8.0			
t_{pw}	Clear Pulse Width		20			ns
f_{max}	Max. Clock Frequency		50	70		MHz

FUNCTION TABLE

Mode	INPUTS Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	OUTPUTS DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
H = HIGH
↑ = Clock LOW-to-HIGH Transition
NC = No Change
X = Don't Care
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D_7, D_6 . . . D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n} . . . Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

DEFINITION OF FUNCTIONAL TERMS

DY_i The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.

Q_0 The continuous output from the Q_0 flip-flop of the register. This output is used for serial shifting.

$\overline{RE}$ Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extended) are inhibited.

S/P Serial/Parallel. When S/P is LOW, the register can by synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.

$\overline{SE}$ Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the Q_7 flip-flop will be repeated in the Q_7 flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer (D_A and D_B) is enabled to enter data during the serial shift right. The Q_7 flip-flop (DY_7) is normally considered the MSB of the register for arithmetic definitions.

D_A, D_B The serial inputs to the device.

S Multiplexer Select. When S is LOW, the D_A serial input is selected. When S is HIGH, the D_B serial input is selected.

CLR Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.

CP Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.

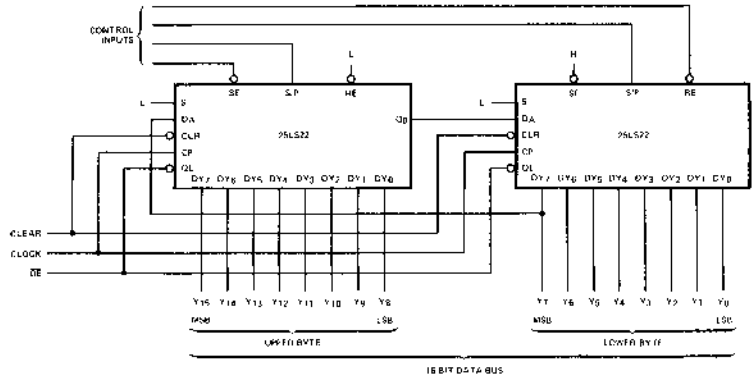
$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the eight DY_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

LOADING RULES (In Unit Loads)

Input/ Output	Pin No.'s	LOW Input Unit Load	Fan-Out Output HIGH	Fan-Out Output LOW 4mA	Fan-Out Output LOW 8mA
$\overline{RE}$	1	1	–	–	–
S/P	2	1	–	–	–
D_A	3	1	–	–	–
DY_7	4	0.3	50/130	11	22
DY_5	5	0.3	50/130	11	22
DY_3	6	0.3	50/130	11	22
DY_1	7	0.3	50/130	11	22
$\overline{OE}$	8	.1	–	–	–
CLR	9	1	–	–	–
GND	10	–	–	–	–
CP	11	1	–	–	–
Q_0	12	–	22	11	22
DY_0	13	0.3	50/130	11	22
DY_2	14	0.3	50/130	11	22
DY_4	15	0.3	50/130	11	22
DY_6	16	0.3	50/130	11	22
D_B	17	1	–	–	–
$\overline{SE}$	18	3	–	–	–
S	19	2	–	–	–
V_{CC}	20	–	–	–	–

Low-Power Schottky TTL unit load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

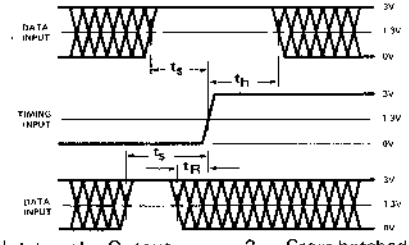
APPLICATIONS



SYSTEM OPERATION	25LS22 UPPER BYTE				25LS22 LOWER BYTE				FUNCTION
	SE	S/P	RE	OE	SE	S/P	RE	OE	Description
Load lower byte and extend lower byte sign to upper byte	H	H	L	X	X	L	L	X	Load from Bus
	L	H	L	H	X	X	H	H	7 clock cycles to extend sign
Load upper byte and extend upper byte sign while shifting value to lower byte position	X	L	L	X	X	X	X	X	Load from Bus
	H	H	L	H	H	H	L	H	8 clock cycles to extend upper byte sign and shift upper byte into lower byte position
Read 16-bit word to Bus	X	X	X	L	X	X	X	L	Unload

Two 25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

SET-UP, HOLD, AND RELEASE TIMES



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.

2. Cross-hatched area is don't care condition.

RAYTHEON

8-Bit Shift/Storage Register with Synchronous Clear

25LS23

FEATURES

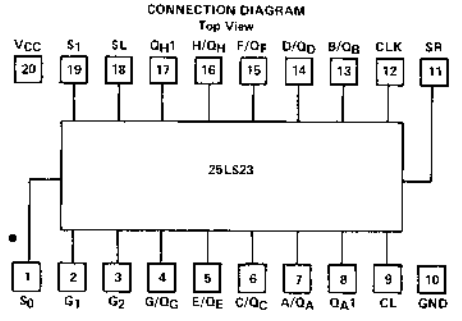
- Synchronous Clear
- Three-State Outputs
- Common Input/Output Pins
- Advanced Low-Power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883

DESCRIPTION

The 25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the 25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops A and H.

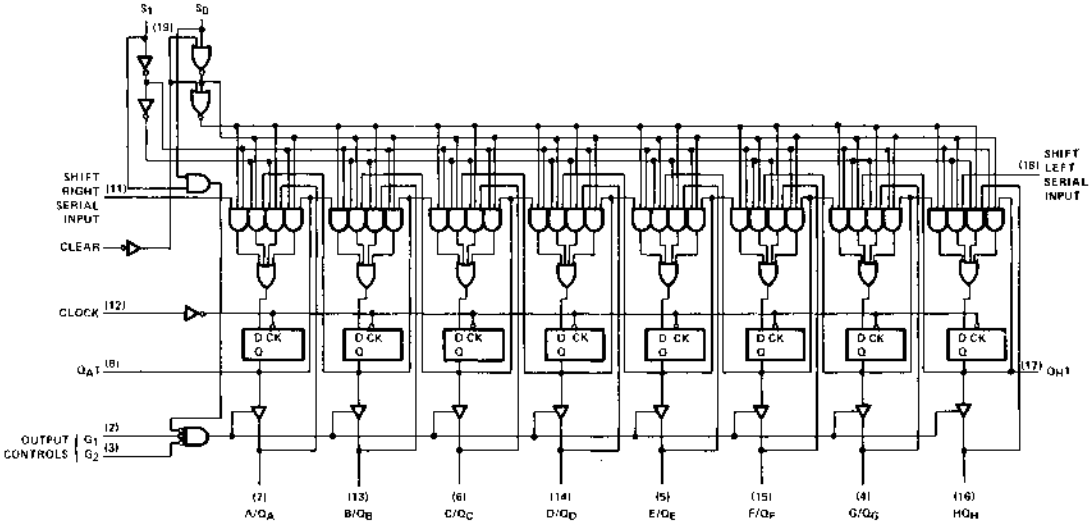
Four modes of operation are possible—Hold (store), Shift-left, Shift-right and Load Data. The 25LS23 has a typical shift frequency of 50MHz. The 25LS23 is packaged in a standard 20-pin package.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

LOGIC DIAGRAM



Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	V
High Level Output Current I_{OH}	Q_0–Q_7			-0.44			-0.44	mA
	DY_0–DY_7			-1.0			-2.6	
Low-Level Output Current I_{OH}			4.0	8.0		4.0	8.0	mA
Operating Free Air Temperature T_A		-55		+125	0°		70	°C

Electrical Characteristics Over Operating Temperature Range (Unless Otherwise Noted)

	Description	Test Conditions (Note 1)			Military			Commercial			Units
					Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q_0, Q_7	I_{OH} = -440µA	2.5			2.7			V
			DY_0–DY_7	I_{OH} = -1.0mA	2.4						
				I_{OH} = -2.6mA				2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8.0mA		0.35	0.45		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.7			0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = -18mA					-1.5			-1.5	V
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	S_0, S_1				-0.8			-0.8	mA
			All others				-0.4			-0.4	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)	S_0, S_1				40			40	µA
			All others				20			20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V (Except DY_i)	S_0, S_1				0.2			0.2	mA
			All others				0.1			0.1	
I_O	Off-State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4V				-100			-100	µA
			V_O = 2.4V				40			400	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			-30		-85	-30		-85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				38	57		38	57	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules)
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC}—measured with clock input HIGH and output controls HIGH.

Switching Characteristics (T_a = +25°C, V_{CC} = 5.0V)

Parameters	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Units
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	Clock	Q_0 or Q_7		19		ns
t_{PHL}				23		
t_{PLH}	Clock	DY_i		18		
t_{PHL}				21		
t_s	S_i, S_0 Setup Prior to Clock		20			ns
t_s	S_R, S_L Setup Prior to Clock		20			
t_{pw}	Clock Pulse Width		25			
t_h	Hold Time		3.0			
t_s	Clear Setup Prior to Clock		20			
t_{ZH}	S_i, S_0	DY_i		20		ns
t_{ZL}				19		
t_{ZH}	$\overline{G}_1$, G_2	DY_i		20		
t_{ZL}				18		
f_{max}	Maximum Frequency			50		mHz
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C, page 2-174)						
t_{LZ}	S_1, S_0	DY_i		22		ns
t_{HZ}				20		
t_{LZ}	G_1, G_2	DY_i		20		
t_{HZ}				16		

TRUTH TABLE

Function	INPUTS								OUTPUTS		INPUTS/OUTPUTS							
	S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\bar{G}_1$	$\bar{G}_2$	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear	X	X	L	↑	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control	X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
M Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
O Load (Note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
D Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
E Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedance ↑ = Transition LOW-to-HIGH Notes: 1. Either LOW to observe outputs.
H = HIGH X = Don't Care NC = No Change 2. In this mode DY_i are inputs.

DEFINITION OF FUNCTIONAL TERMS

S_R Shift right data input to Q_7

S_L Shift left data input to Q_0

Clear Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled.

Clock A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition.

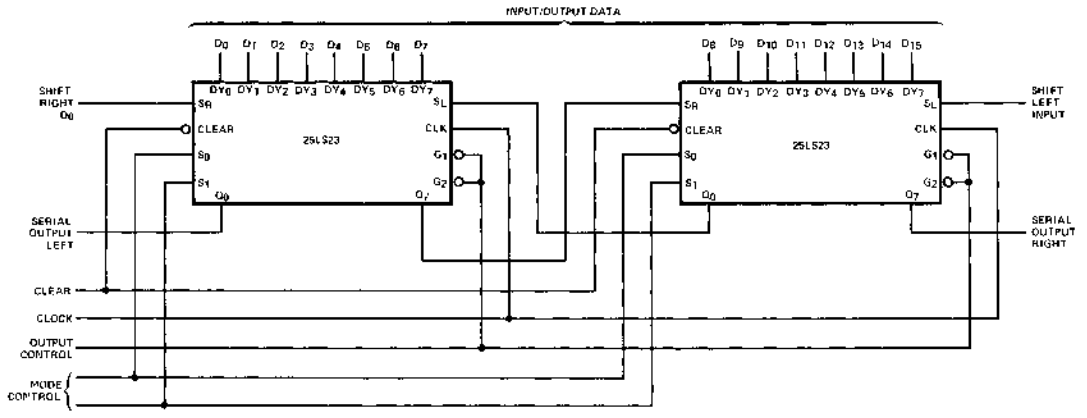
S_0, S_1 Mode selection control lines used to control input (output during load) conditions

$\bar{G}_1$, $\bar{G}_2$ Active LOW input to control three-state output in active LOW AND configuration.

Q_0, Q_7 The only two direct outputs; used to cascade shift operations

DY_0–DY_7 Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\bar{G}_1$, $\bar{G}_2$).

APPLICATION



16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register

Single and Dual Retriggerable Monostable Multivibrators with Clear

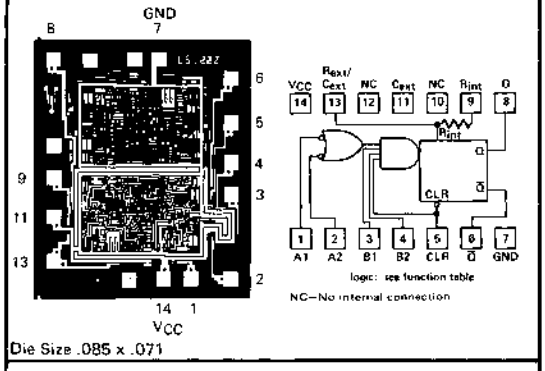
FEATURES

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Low Power Dissipation:
  - 25LS122 . . . 30 mW Typical
  - 25LS123 . . . 60 mW Typical
- Compensated for V_{CC} and Temperature Variations
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- 25LS122 Has Internal 10 kΩ Timing Resistor
- Diode-Clamped Inputs
- Compatible for Use with TTL or DTL
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

DESCRIPTION

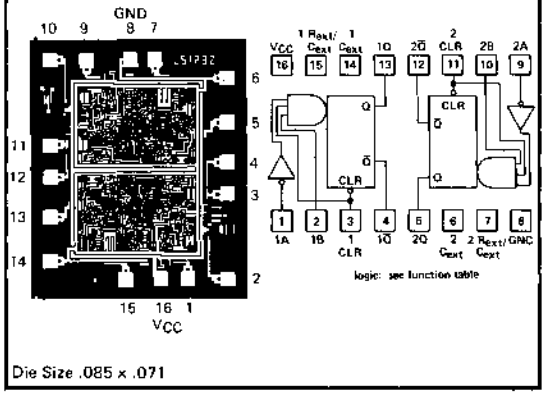
The 25LS122 and 25LS123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Enough Schmitt hysteresis is provided to ensure jitter-free triggering from the B inputs with transition rates as slow as 1 volt per second. Figure 1 illustrates triggering the one-shot with the high-level-active (B) inputs.

25LS122



Die Size .085 x .071

25LS123



Die Size .085 x .071

25LS122 FUNCTION TABLE
(SEE NOTE 1)

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

25LS123 FUNCTION TABLE
(SEE NOTE 1)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

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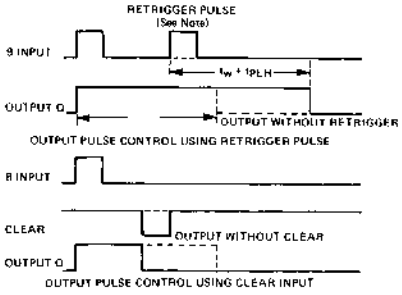
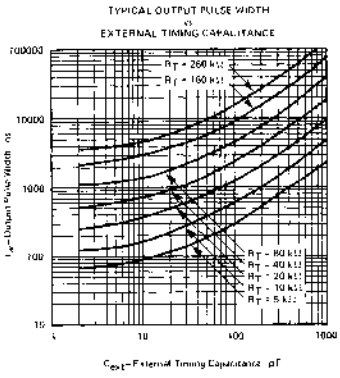
NOTES: 1. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, H = one high-level pulse, L = one low-level pulse, X = irrelevant (any input, including transitions).
2. To use the internal timing resistor of 25LS122, connect R_{int} to V_{CC}.
3. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
4. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
5. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.



NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 1—Typical Input/Output Pulses



†These values of resistance exceed the maximum recommended for use over the full temperature range of the 9LS/54LS' circuits.

FIGURE 2

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The 25LS122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_W) is defined as:

$$t_W = 0.4 \cdot R_T \cdot C_{ext}$$

where

R_T is in kΩ (either internal or external timing resistor),
C_{ext} is in pF,
t_W is in ns.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 2.

Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–440			–440	μA
Low-level output current, I_{OL}		4		8	4		8	mA
Pulse width, t_W	A or B inputs high	40			40			ns
	A or B inputs low	40			40			
	Clear low	40			40			
External timing resistance, R_{ext}		5		226	5		360	kΩ
External capacitance, C_{ext}		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		–55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†			Military			Commercial			Unit
					Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2V, I_{OH} = −440 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.45		0.35	0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−15		−85	−15		−85	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 2	25LS122		6	11		6	11	mA
				25LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Switching Characteristics V_{CC} = 5.0V Over Recommended Free-Air Temperature Range.

Parameters	From (Input)	To (Output)	+25°C			Unit
			Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2.0k C_{ext} = 0pF, R_{ext} = 5.0 kΩ (See Fig. 3, page 3-19, and Fig. A, page 2-174)						
t_{PLH}	A	Q		20	30	ns
	B			26	38	
t_{PHL}	A	$\overline{Q}$		28	40	ns
	B			35	48	
t_{PHL}	Clear	Q		16	22	ns
t_{PLH}		$\overline{Q}$		25	40	ns
$t_w Q$(min)	A or B	Q		116	200	ns
*$t_w Q$	A or B	Q	4.0	4.5	5.0	ns

*For this test R_{ext} = 10 kΩ, C_{ext} = 1000 pF.

FEATURES

- 25LS138: 3-Line-to-8-Line Decoder
  1-of-8 Demultiplexer
- 25LS139: Dual 2-Line-to-4-Line Decoder
  Dual 1-of-4 Demultiplexer
- Higher Speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

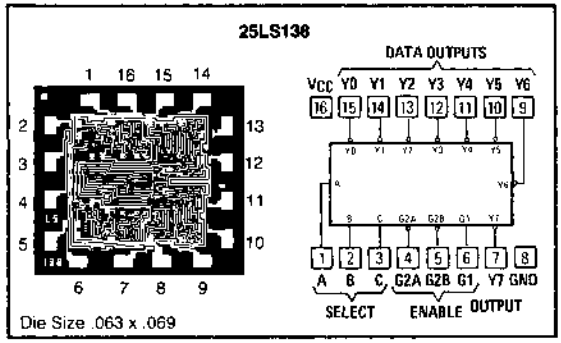
DESCRIPTION

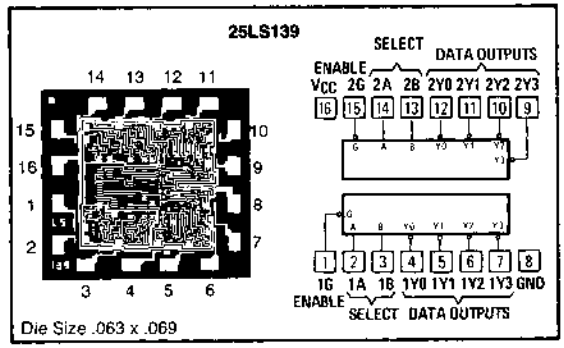
The 25LS138 decodes one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 25LS139 comprises two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

These circuits are designed to be used in high-performance memory-decoding and data-routing applications requiring very short delay times.

PIN-OUT DIAGRAMS





25LS138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

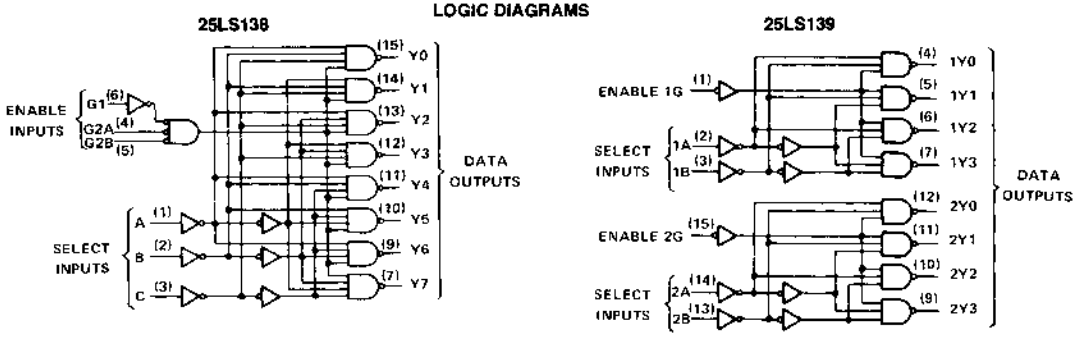
H = high level, L = low level, X = don't care

25LS139
FUNCTION TABLE (½)

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

LOGIC DIAGRAMS



Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–440			–440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=–18mA				–1.5			–1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}= –440μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
		I_{OL}=8mA		0.3	0.45		0.35	0.45	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				–0.36			–0.36	mA
I_{OS}†	V_{CC}=MAX		–15		–85	–15		–85	mA
I_{CC}	V_{CC}=MAX, Outputs enabled and open	25LS138		6.3	10		6.3	10	mA
		25LS139		6.8	11		6.8	11	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

25LS138
Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter	Levels of Delay	From (input)	To (output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{PLH}	2	Binary Select	Any		10	15	ns
t_{PLH}					14	20	ns
t_{PLH}	3				15	23	ns
t_{PLH}					18	27	ns
t_{PLH}	2	Enable	Any		10	15	ns
t_{PLH}					15	23	ns
t_{PLH}	3				12	18	ns
t_{PLH}					18	27	ns

25LS139
Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameters	Levels of Delay	From (input)	To (output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{PLH}	2	Binary Select	Any		10	15	ns
t_{PLH}					12	18	ns
t_{PLH}	3				13	20	ns
t_{PLH}					14	21	ns
t_{PLH}	2	Enable	Any		9	12	ns
t_{PLH}					11	16	ns

FEATURES

- Select one of eight data sources
- Perform parallel-to-serial conversion
- 25LS151 has complementary outputs
- 25LS151 has strobe input
- Higher Speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

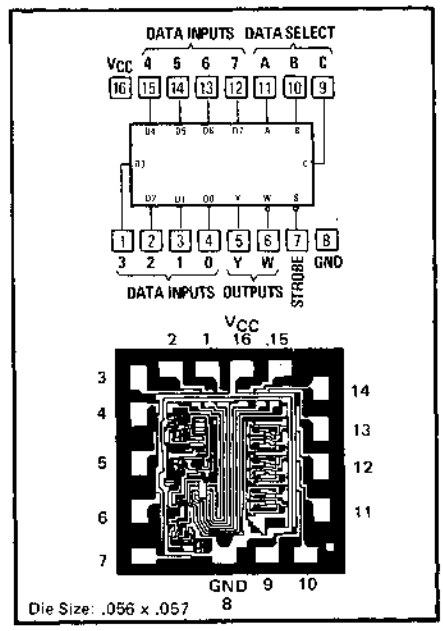
DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources. The 25LS151 has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output low.

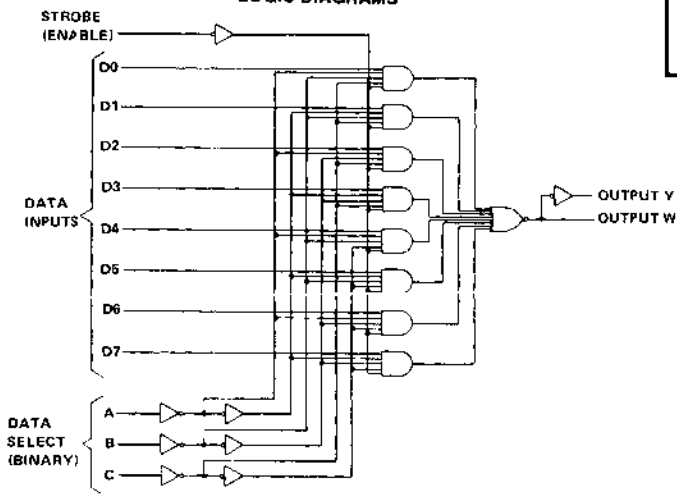
The 25LS151 features complementary W and Y outputs.

PIN-OUT DIAGRAMS

25LS151



LOGIC DIAGRAMS



25LS151 FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = don't care
D0, D1 . . . D7 = the level of the D respective input

Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–440			–440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=–18mA				–1.5			–1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max I_{OH}= –440μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40			0.40	V
		I_{OL}=8mA		0.3	0.45		0.35	0.45	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				–0.4			–0.4	mA
I_{OS}†	V_{CC}=MAX		–15		–85	–15		–85	mA
I_{CC}	V_{CC}=MAX, Outputs open, All inputs at 4.5V			6.0	10		6.0	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter	From (input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	A, B or C (4 levels)	Y		27	41	ns
t_{PHL}				20	30	
t_{PLH}	A, B, or C (3 levels)	W		16	23	ns
t_{PHL}				22	32	
t_{PLH}	Strobe	Y		22	33	ns
t_{PHL}				18	27	
t_{PLH}	Strobe	W		13	20	ns
t_{PHL}				17	26	
t_{PLH}	Any D	Y		17	26	ns
t_{PHL}				15	23	
t_{PLH}	Any D	W		10	15	ns
t_{PHL}				10	15	

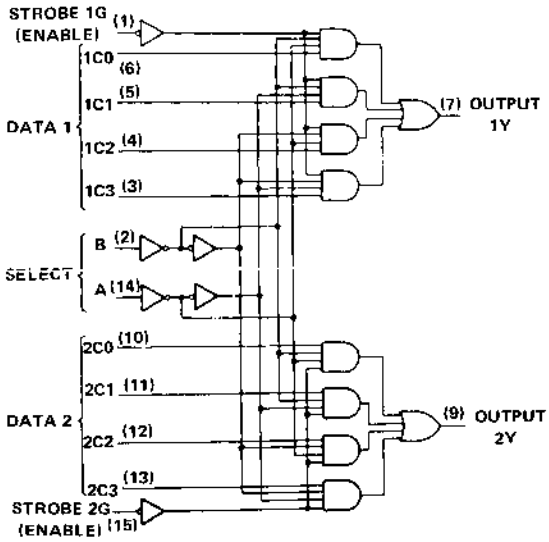
FEATURES

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (Enable) line provided for cascading (N lines to n lines)
- Non-inverting
- Higher Speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

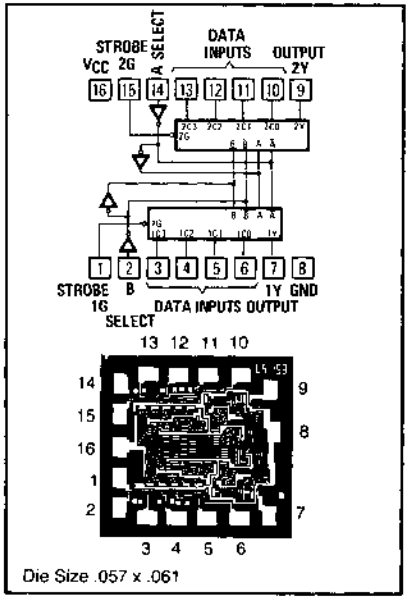
DESCRIPTION

The 25LS153 is a high speed Dual 4-Line to 1-Line Multiplexer with common select inputs and separate strobe (enable) inputs for each half. Each half can select one bit of four and present it at the output in non-inverted form.

LOGIC DIAGRAM



PIN-OUT DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care

RAYTHEON

Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.5	V
High-level output current, I_{OH}			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40			0.40	V
		I_{OL}=8mA		0.3	0.45		0.35	0.45	
I_I	V_{CC}=MAX, V_I=7.0V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.36			-0.36	mA
I_{OS}†	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CCL}††	V_{CC}=MAX			6.2	10		6.2	10	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CCL} is measured with the outputs open and all inputs grounded.

Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter	From (Input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	Data	Y		7	13	ns
t_{PLH}	Data	Y		10	16	ns
t_{PLH}	Select	Y		16	24	ns
t_{PLH}	Select	Y		20	25	ns
t_{PLH}	Strobe	Y		13	n-,20	ns
t_{PLH}	Strobe	Y		15	20	ns

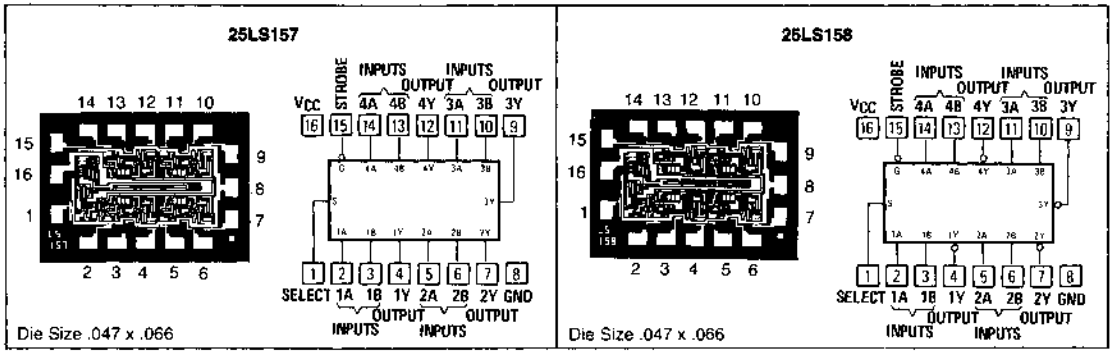
DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The 25LS157 presents true data; the 25LS158 presents inverted data.

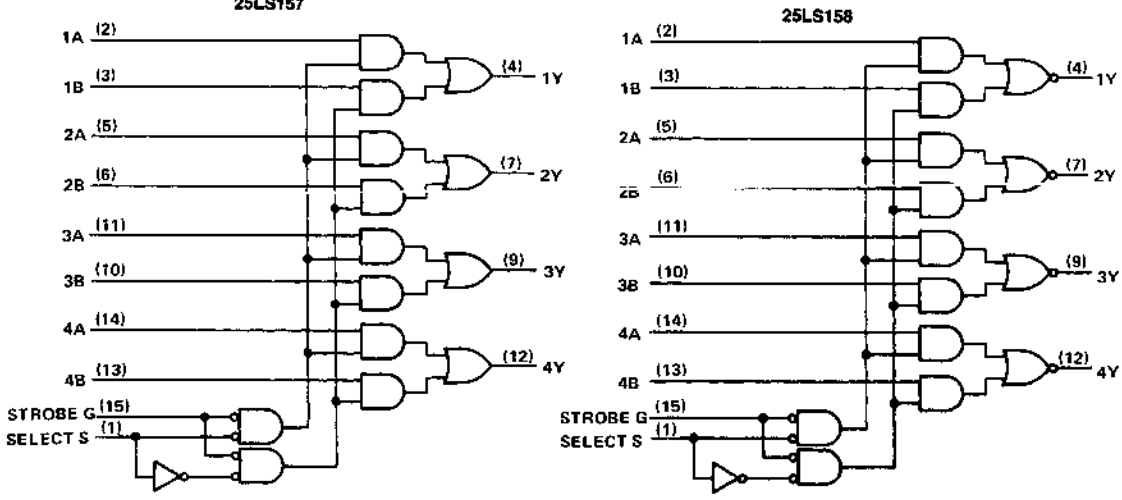
FEATURES

- Higher Speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883

PIN-OUT DIAGRAMS



LOGIC DIAGRAMS



FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	25LS157	25LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = don't care
Low level at S selects A inputs
High level at S selects B inputs
Strobe is active low

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Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA		0.3	0.45		0.35	0.45	
I_I	S or G input	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	A or B input					0.1			0.1	
I_{IH}	S or G input	V_{CC}=MAX, V_I=2.7V				40			40	μA
	A or B input					20			20	
I_{IL}	S or G input	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
	A or B input					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††		V_{CC}=MAX	25LS157		9.7	16		9.7	16	mA
			25LS158		4.8	8		4.8	8	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
†† I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

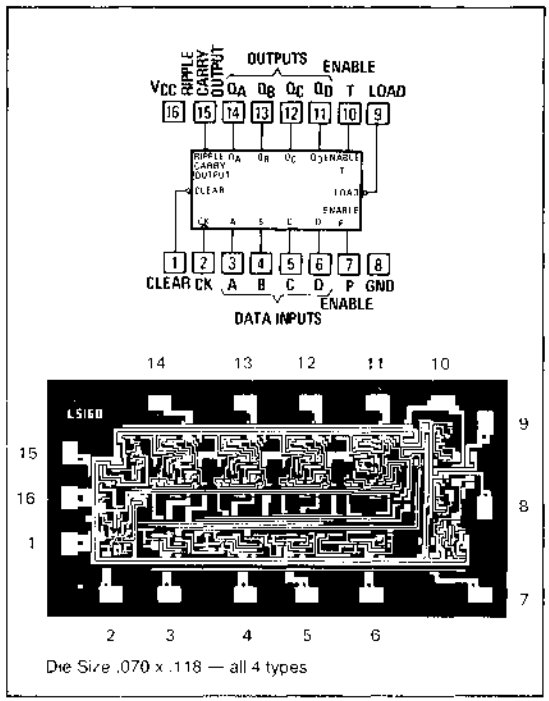
Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter		From (input)	To (output)	+25°C			Unit
				Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{PLH}	25LS157	Data	Y_i		5	10	ns
t_{PLH}					7	12	
t_{PLH}	25LS158	Data	Y_i		7	12	ns
t_{PLH}					5	10	
t_{PLH}	25LS157	Strobe	Y_i		13	20	ns
t_{PLH}					8	16	
t_{PLH}	25LS158	Strobe	Y_i		8	12	ns
t_{PLH}					12	17	
t_{PLH}	25LS157	Select	Y_i		10	20	ns
t_{PLH}					11	20	
t_{PLH}	25LS158	Select	Y_i		11	20	ns
t_{PLH}					10	20	

FEATURES

- 4-bit synchronous counters
- Synchronously programmable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- Advanced low-power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current

PIN-OUT DIAGRAM



Die Size .070 x .118 — all 4 types

DESCRIPTION

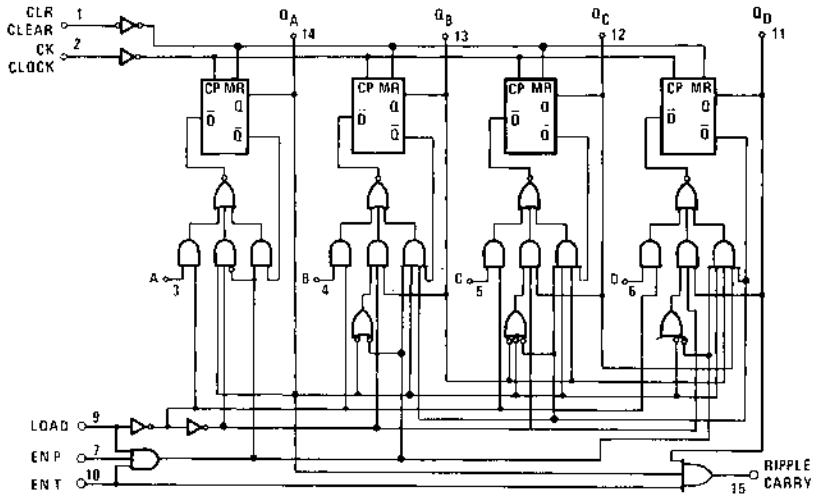
The 25LS160, 25LS161, 25LS162 and 25LS163 synchronous, presettable counts have internal look-ahead carry and ripple carry output for high-speed counting applications. The 25LS160 and 25LS162 are decade counters and the 25LS161 and 25LS163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition.

The 25LS160 and 25LS161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The 25LS162 and 25LS163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection.

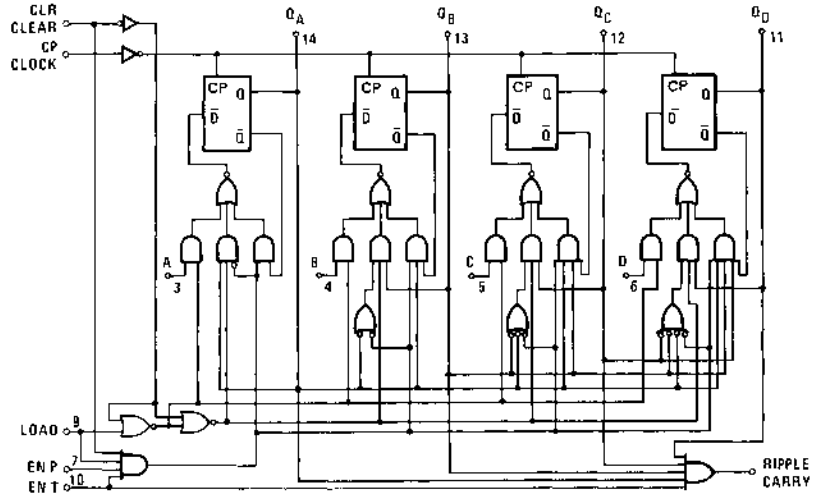
LOGIC DIAGRAMS

25LS160
Synchronous Decade Counter



25LS162 synchronous decade counters are similar; however, the clear is synchronous as shown for the 25LS163 binary counters.

25LS163 SYNCHRONOUS
BINARY COUNTER



25LS161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the 25LS160 decade counters.

Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−440			−440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-5.5		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=−18mA				−1.5			−1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=−440μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max,	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA		0.35	0.45		0.35	0.45	
I_I	Data or enable P	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
	Load, clock, or enable T					0.2			0.2	
	Clear (LS160,161)					0.1			0.1	
	Clear (LS162,163)					0.2			0.2	
I_{IH}	Data or enable P	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Load, clock, or enable T					40			40	
	Clear (LS160,161)					20			20	
	Clear (LS162,163)					40			40	
I_{IL}	Data or enable P	V_{CC}=MAX, V_I=0.4V				−0.4			−0.4	mA
	Load, clock, or enable T					−0.8			−0.8	
	Clear(LS160,161)					−0.4			−0.4	
	Clear(LS162,163)					−0.8			−0.8	
I_{OS}†		V_{CC}=MAX		−15		−85	−15		−85	mA
I_{CCH}		V_{CC}=MAX, See Note 1			18	31		18	31	mA
I_{CCL}		V_{CC}=MAX, See Note 2			19	32		19	32	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.

NOTES:
1. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
2. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

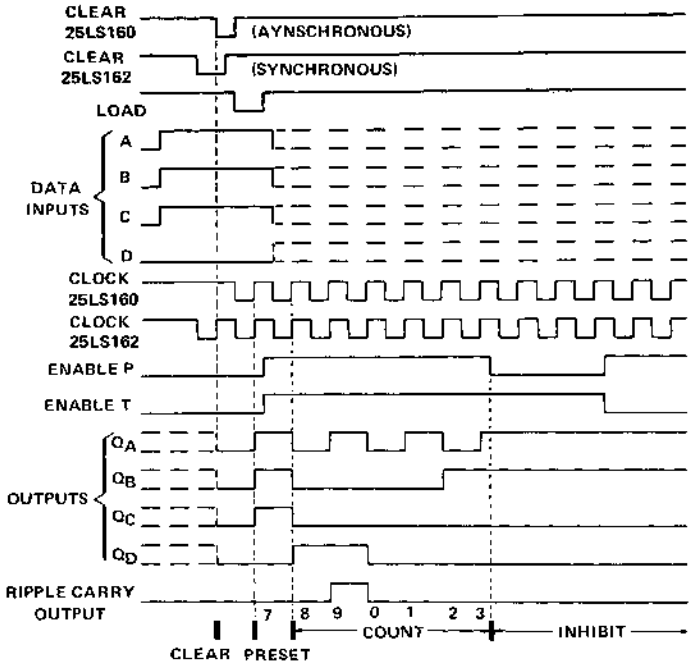
Switching Characteristics, V_{CC} = 5V, T_A = + 25°C

Parameters	From (Inputs)	To (Outputs)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (see Fig. A on page 2-174)						
t_{PLH}	Clock	Carry		25	35	ns
t_{PHL}				20	35	
t_{PLH}	Clock (Load Input High)	Q		10	18	ns
t_{PHL}				15	20	
t_{PLH}	Clock (Load Input Low)	Q		10	18	ns
t_{PHL}				14	20	
t_{PLH}	Enable T	Carry		15	20	ns
t_{PHL}				9	14	
t_{PHL}	Clear (Note 1)	Q		14	28	ns
t_{pw}	Pulse Width	Clock	25			ns
		Clear	20			
t_s	Set up time	Data A,B,C,D	20			ns
		ENABLE P	20			
		Load, Enable T	20			
		Clear (Note 2)	20			
t_h	Hold time	Any input	3			ns
f_{max}	Maximum Frequency		30	40		MHz

NOTES:

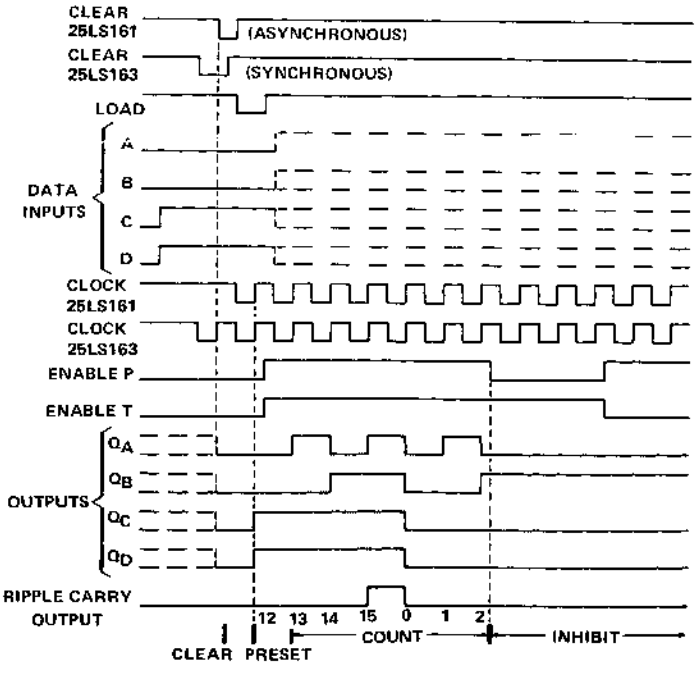
1. Measured from clear input on 25LS160 and 25LS161. Measured from clock input on 25LS162 and 25LS163.
2. Applies to 25LS162 and 25LS163 only.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES



25LS160, 25LS162

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



25LS161, 25LS163

Illustrated below is the following sequence:
1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen; fourteen fifteen, zero, one, and two
4. Inhibit

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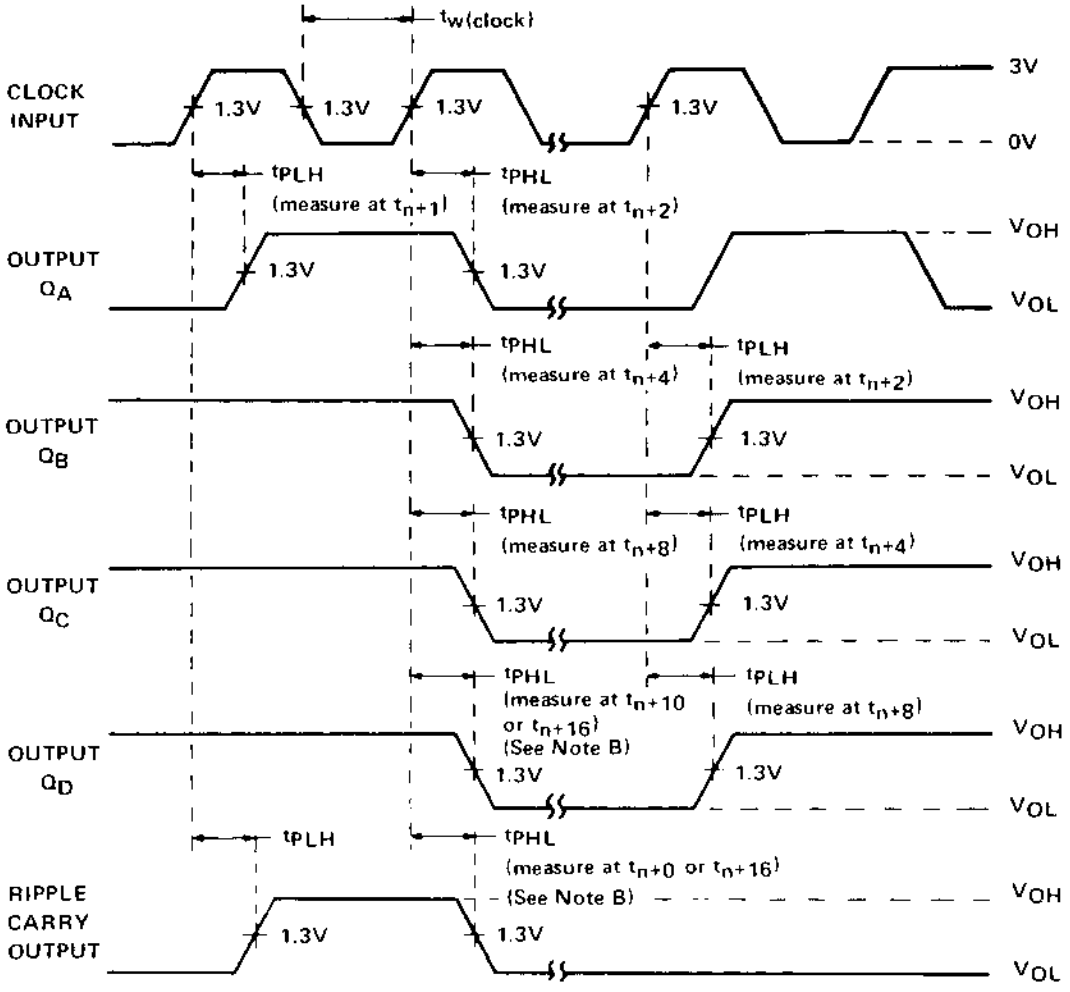
FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

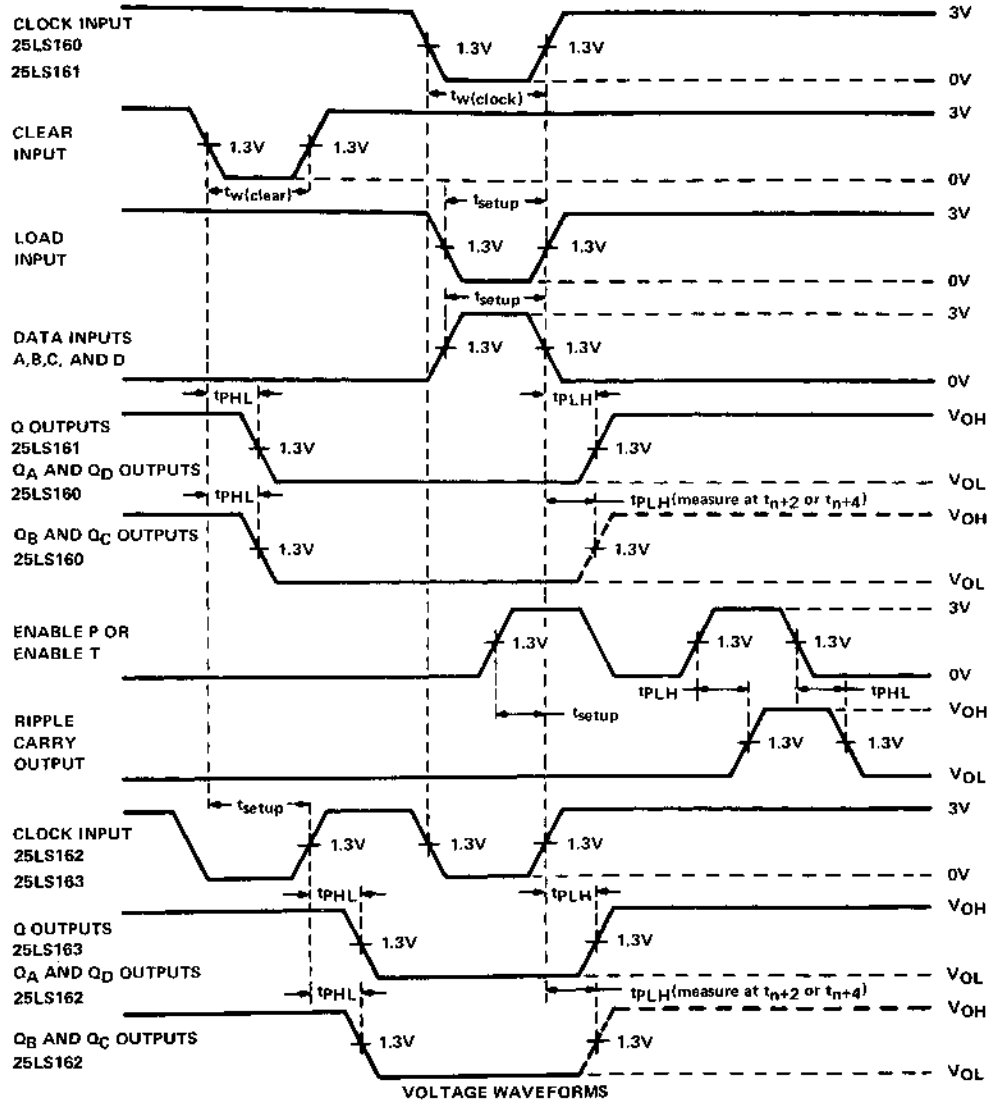
NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$: $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} 25LS162, and at t_n+16 for 25LS 163 where t_n is the bit time when all outputs are low.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

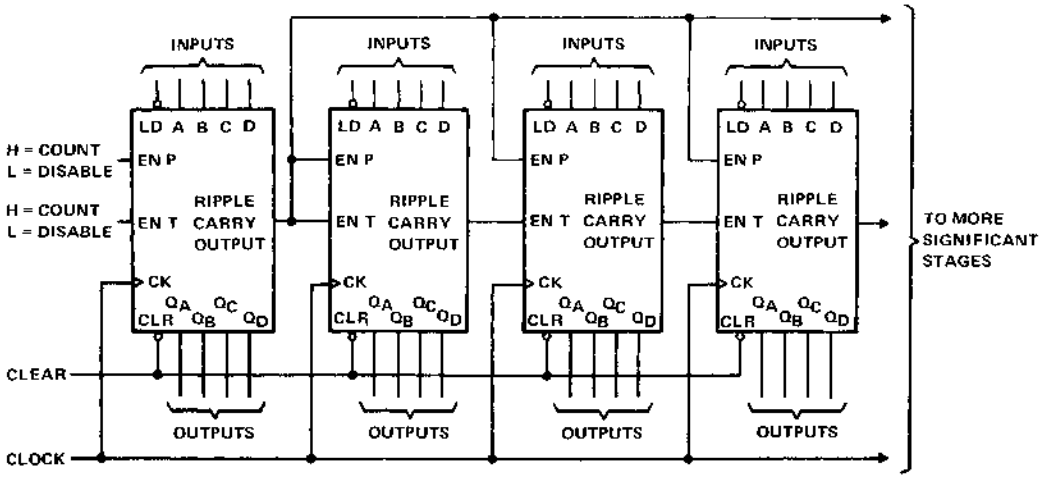
A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\,\Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at $t_n = 0$.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 25LS160 or 25LS162 will count in BCD and the 25LS163 will count in binary. Virtually any count mode (modulo-N, N_1-to N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



4-By-4 Register Files with Open-Collector Outputs

FEATURES

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
  - Scratch-Pad Memory
  - Buffer Storage between Processors
  - Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current: 20 μA

DESCRIPTION

The 25LS170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $\overline{G}_W$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $\overline{G}_R$, is high, the data outputs are inhibited and remain high.

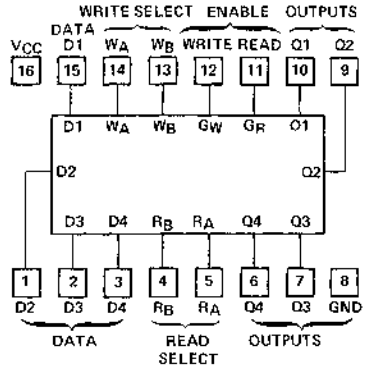
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

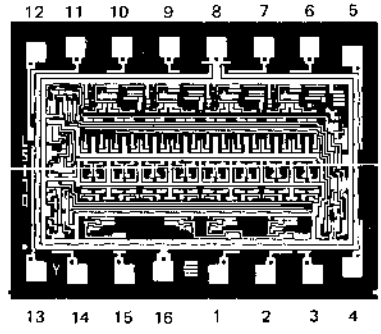
This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable of the 25LS170 are buffered to lower the drive requirements to one Series 54LS/74LS standard load, respectively, input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

PIN-OUT DIAGRAM

25LS170





Die Size: .090 x .068

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LOGIC

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C).

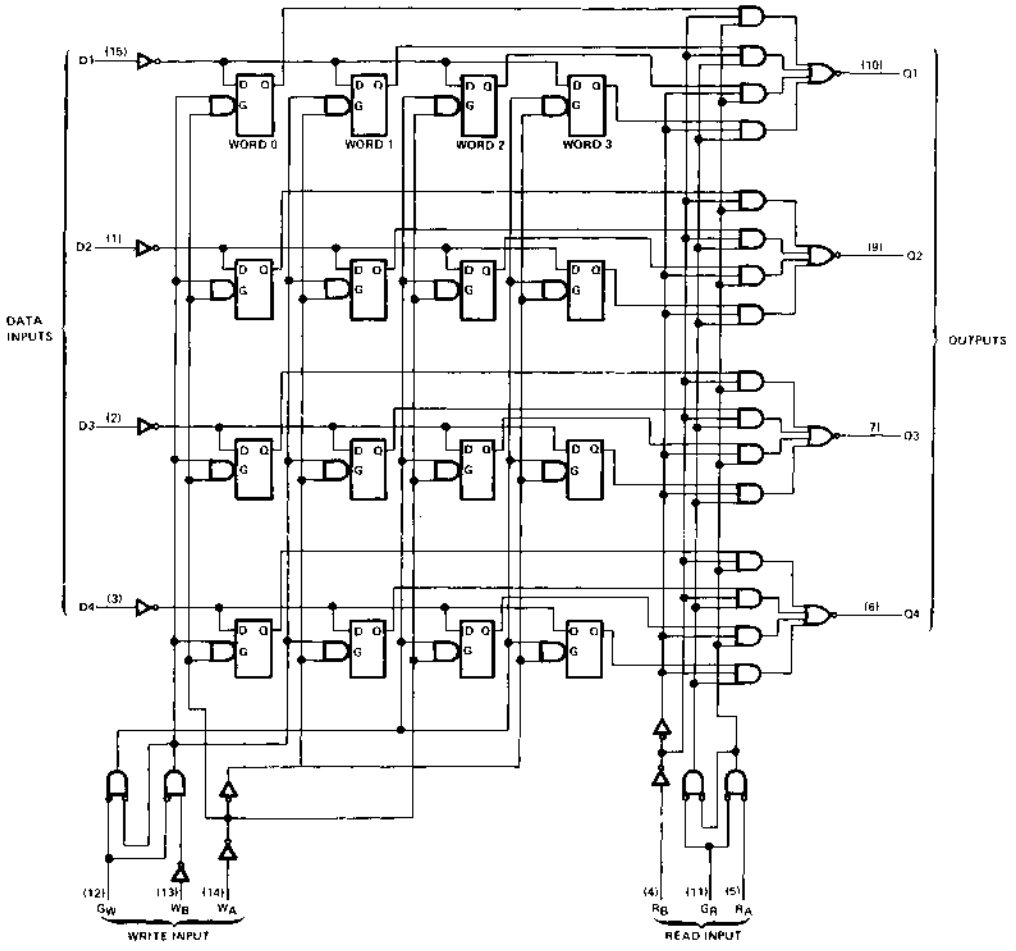
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}		4		8	4		8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

Electrical Characteristics Over Recommended Operating Free-Air Temp. Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Military			Commercial			Unit
				Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH} High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{OH} = 5.5V, V_{IH} = 2V			20			20	mA
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	Any D, R, or W	V_{CC} = MAX,	V_I = 7V			0.1			0.1	mA
	G_R or G_W					0.2			0.2	
I_{IH} High-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 2.7V			20			20	mA
	G_R or G_W					40			40	
I_{IL} Low-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 0.4V			−0.4			−0.4	mA
	G_R or G_W					−0.8			−0.8	
I_{CC} Supply current		V_{CC} = MAX,	See Note 6		25	40		25	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C.

NOTE 4. I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1, page 3-41 and Fig. B, page 2-174)						
t_{PLH}	Read enable	Any Q		20	30	ns
t_{PHL}				20	30	
t_{PLH}	Read select	Any Q	25	40		ns
t_{PHL}				24	40	
t_{PLH}	Write enable	Any Q		30	45	ns
t_{PHL}				26	40	
t_{PLH}	Data	Any Q		30	45	ns
t_{PHL}				22	35	

PARAMETER MEASUREMENT INFORMATION

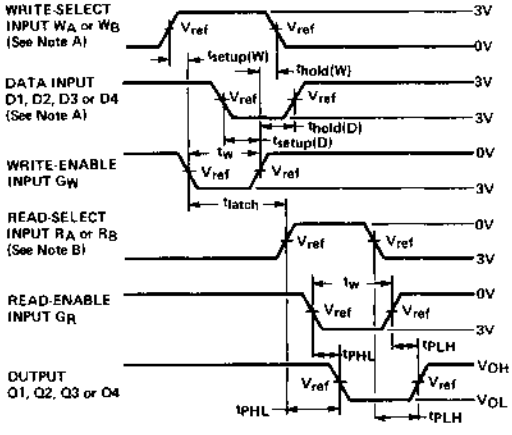


FIGURE 1

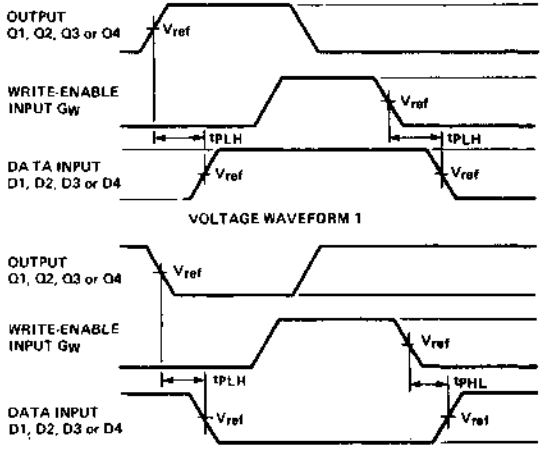


FIGURE 2

NOTES: A. High-level input pulses at the select and data inputs are illustrated in Figure 1; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

D. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ≤ 50% $t_r \leq 15$ ns and $t_f \leq 6$ ns for .

D. V_{ref} = 1.3 V.

FEATURES

- Positive edge-triggered common clock
- Asynchronous common reset
- Clock-to-output delays of 14 ns
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

DESCRIPTION

The 25LS174 is a six-bit register with single-rail outputs and the 25LS175 is a four-bit register with complementary outputs. Both consist of D-type flip-flops with a buffered common clock and an asynchronous, active-Low buffered clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

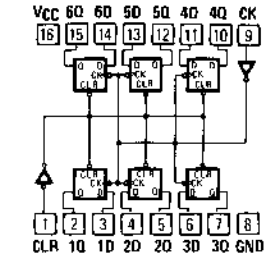
FUNCTION TABLE (EACH FLIP-FLOP)

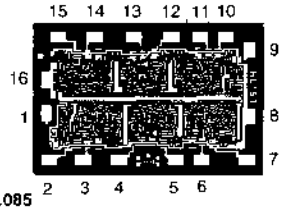
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.
† = 25LS175 only

PIN-OUT DIAGRAMS

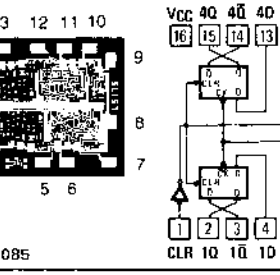
25LS174

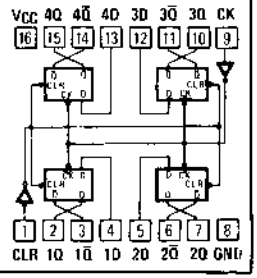




Die Size .056 x .085

25LS175

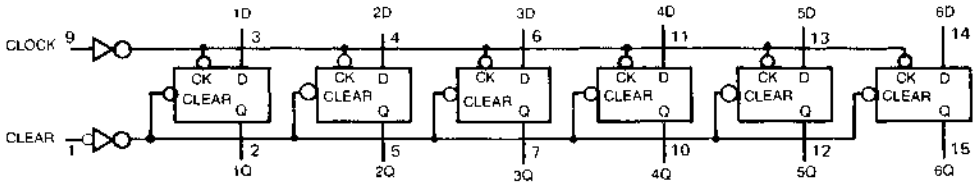




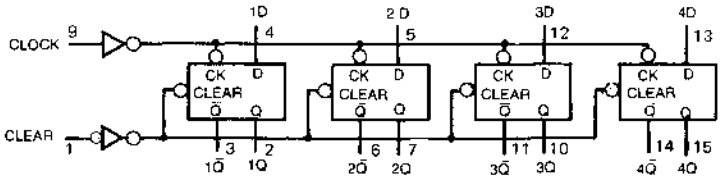
Die Size .056 x .085

LOGIC DIAGRAMS

25LS174



25LS175



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Recommended Operating Conditions

		Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-440			-440	μA
Low-level output current, I_{OL}		4		8	4		8	mA
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock pulse, t_w (Low)		15			15			ns
Width of clear pulse, t_w (Low)		20			20			ns
Setup time	Data input t_{setup}	10			10			ns
	Clear recovery, t_{rec}	12			12			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

t_{setup} is the minimum time required for the correct logic level to be present at the data input prior to the rising edge of the clock in order to be recognized and transferred to the output.

t_{hold} is the minimum time required for the logic level to be maintained at the data input after the rising edge of the clock in order to insure recognition.

t_{rec} is the minimum time required between the end of the clear pulse and the rising edge of the clock in order to transfer High data to the Q output.

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_I=V_{IH} or V_{IL} V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V,	I_{OL}=4mA		0.25	0.40			0.40	V
	V_{IL}=V_{IL}max V_I=V_{IH} or V_{IL}	I_{OL}=8mA		0.35	0.45			0.45	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.36			-0.36	mA
I_{OS}†	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††	V_{CC}=MAX	25LS174		16	26		16	26	mA
		25LS175		11	18		11	18	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured, after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
f_{max}			35	45		MHz
t_{PLH} (LS175 only)	Clear	Q		19	25	ns
t_{PHL}	Clear	Q		20	35	ns
t_{PLH}	Clock	Q		14	23	ns
t_{PHL}	Clock	Q		13	20	ns

FEATURES

- **Provides 16 arithmetic operations**
- **Provides 16 logic operations**
- **Full look-ahead for high-speed arithmetic operation on long words**
- **Higher speed compared to 9LS/54LS and 9LS/74LS**
- **8mA sink current over full military temperature range**
- **50mV improved V_{OL} compared to 9LS/74LS**
- **440μA source current**
- **100% reliability assurance testing in compliance with MIL-STD-883.**

DESCRIPTION

The 25LS181 is an arithmetic logic unit (ALU)/function generator which has a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182, full carry ahead look-ahead circuits, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 25LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1 which requires an end-around or forced carry to provide A-B.

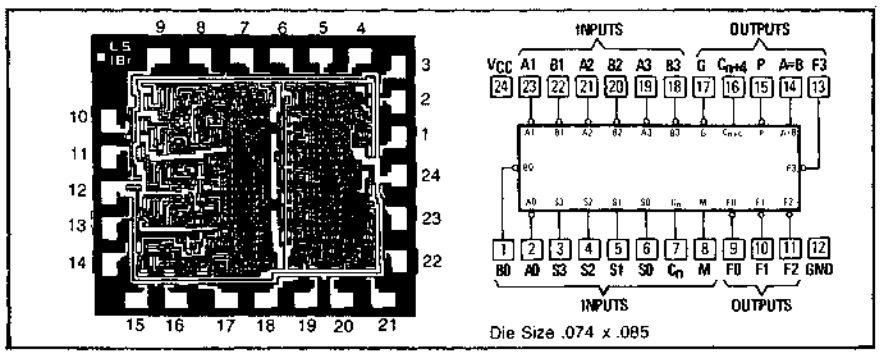
The 25LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs, S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT $\overline{C}_n$	OUTPUT $\overline{C}_{n+4}$	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A = B	A = B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≠ B	A ≠ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

PIN-OUT DIAGRAM



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ALU SIGNAL DESIGNATIONS

The 25LS181 can be used with the signal designations of either Figure 1 or Figure 2

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

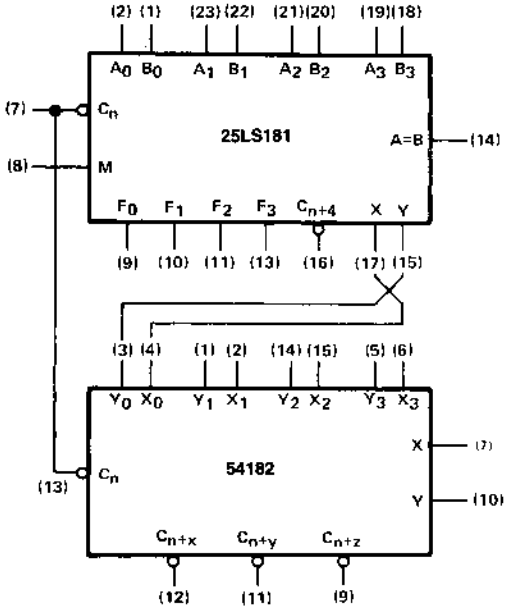


FIGURE 1
(FOR TABLE 1)

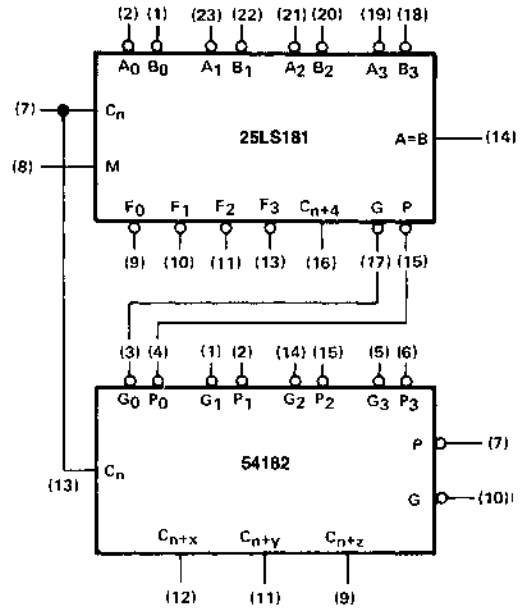


FIGURE 2
(FOR TABLE 2)

TABLE 1

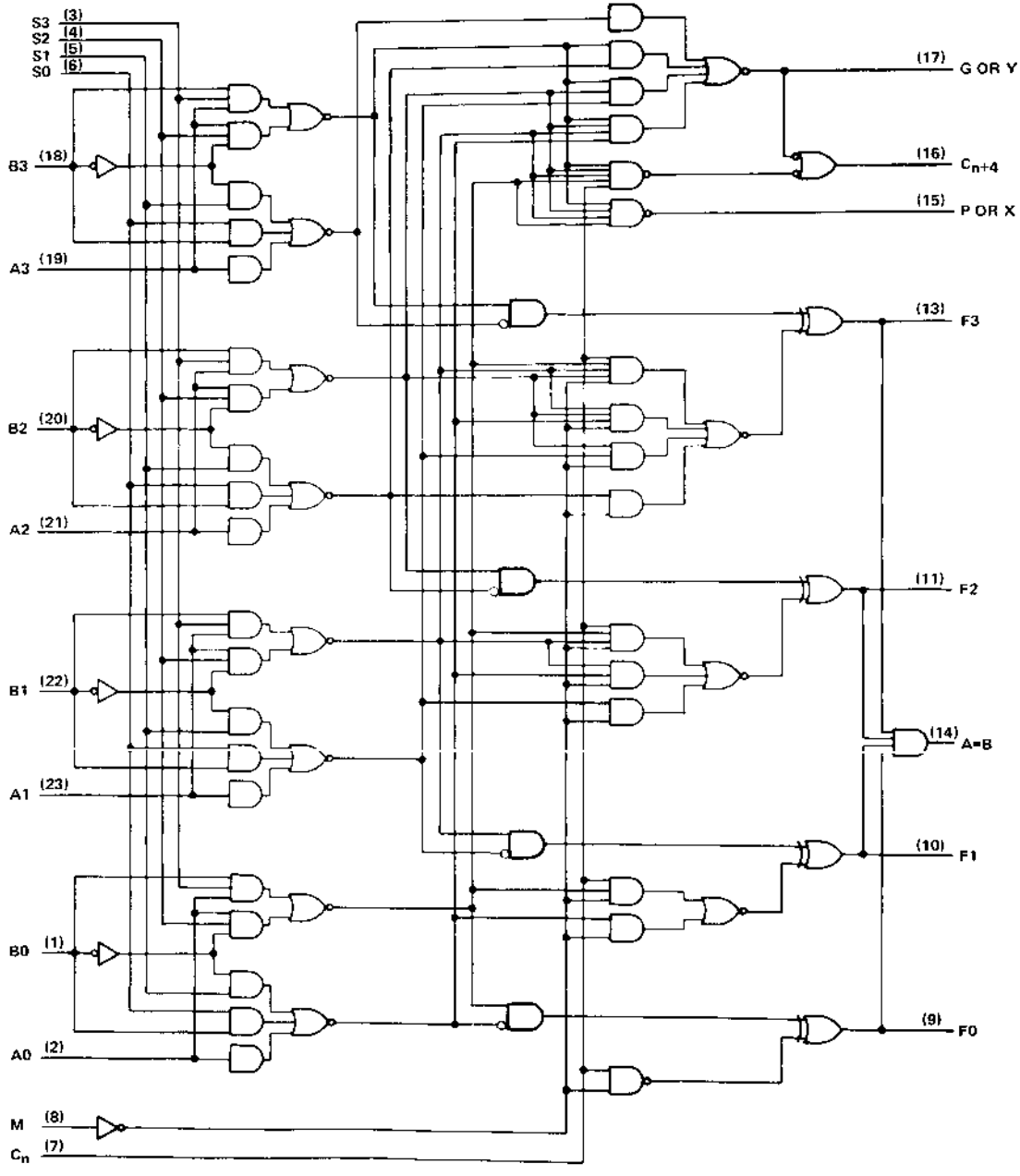
SELECTION S_3 S_2 S_1 S_0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	ACTIVE-HIGH DATA: M = L; ARITHMETIC OPERATIONS: C_n = H (no carry)	ACTIVE-HIGH DATA: M = L; ARITHMETIC OPERATIONS: C_n = L (no carry)
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE 2

SELECTION S_3 S_2 S_1 S_0	ACTIVE LOW DATA: M = H LOGIC FUNCTIONS	ACTIVE LOW DATA: M = L; ARITHMETIC OPERATIONS: C_n = L (with carry)	ACTIVE LOW DATA: M = L; ARITHMETIC OPERATIONS: C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS (A + B)	F = (A + $\overline{B}$) PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



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Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	Any Output except A = B	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
I_{OH}	A = B Output only	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, V_I=V_{IH} or V_{IL}				100			100	μA
V_{OL}	All outputs	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, V_I=V_{IH} or V_{IL}	I_{OL}=4mA			0.40			0.40	V
			I_{OL}=8mA			0.45			0.45	
	Output G		I_{OL}=16mA(G)			0.55			0.55	
I_I	Mode input	V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
	Any $\overline{A}$ or $\overline{B}$ input					0.3			0.3	
	Any S input					0.4			0.4	
	Carry input					0.5			0.5	
I_{IH}	Mode input	V_{CC}=MAX, V_I=2.7V				20			20	μA
	Any $\overline{A}$ or $\overline{B}$					60			60	
	Any S input					80			80	
	Carry input					100			100	
I_{IL}	Mode input	V_{CC}=MAX, V_I=0.5V				-0.36			-0.36	mA
	Any $\overline{A}$ or $\overline{B}$ input					-1.08			-1.08	
	Any S input					-1.44			-1.44	
	Carry input					-2			-2	
I_{OS}†	Any Output except A-B	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††		V_{CC}=MAX	Condition A		20	32		20	34	mA
			Condition B		21	35		21	37	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††With outputs open, I_{CC} is measured for the following conditions:

A. S0 through S3, M and A inputs are at 4.5V, all other inputs are grounded.

B. S0 through S3 and M are at 4.5V, all other inputs are grounded.

Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter¶	From (Input)	To (Output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	C_n	C_{n+4}		14	25	ns
t_{PHL}				13	14	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	Any A or B	C_{n+4}		24	33	ns
t_{PHL}				17	31	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	C_{n+4}		24	35	ns
t_{PHL}				29	35	
M = 0V, (SUM or DIFF mode)						
t_{PLH}	C_n	Any F		12	19	ns
t_{PHL}				12	18	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	Any A or B	G		12	25	ns
t_{PHL}				15	23	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	G		20	25	ns
t_{PHL}				17	25	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 4.5V (SUM mode)						
t_{PLH}	Any A or B	P		14	26	ns
t_{PHL}				20	26	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	P		24	30	ns
t_{PHL}				22	26	
M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V (SUM mode)						
t_{PLH}	A_i or B_i	F_i		15	28	ns
t_{PHL}				13	19	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	A_i or B_i	F_i		24	30	ns
t_{PHL}				15	19	
M = 4.5V (logic mode)						
t_{PLH}	A_i or B_i	F_i		17	31	ns
t_{PHL}				15	25	
M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V (DIFF mode)						
t_{PLH}	Any A or B	A = B		33	50	ns
t_{PHL}				29	45	

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All B	All B	Any F or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

FEATURES

- **Single up/down count mode control line**
- **Asynchronous parallel load**
- **Count enable, parallel load control inputs**
- **Cascadable**
- **Higher speed compared to 9LS/54LS and 9LS/74LS**
- **8mA sink current over full military temperature range**
- **50mV improved V_{OL} compared to 9LS/74LS**
- **440μA source current**
- **100% reliability assurance testing in compliance with MIL-STD-883**

DESCRIPTION

The 25LS190 and 25LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The 25LS191 is a 4-bit binary counter and the 25LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

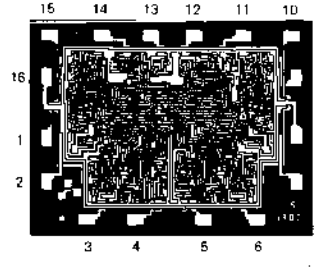
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable and down/up inputs should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

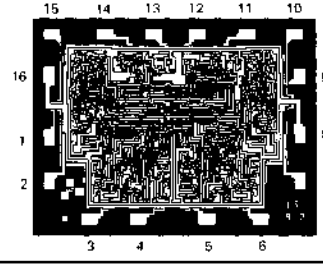
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN-OUT DIAGRAM

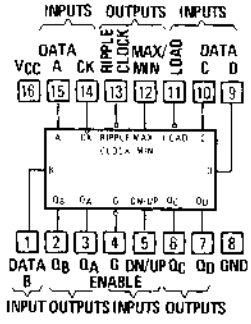


25LS190



25LS191

Die Size .100 x .077



LOW INPUT TO LOAD SETS Q_A = A, Q_B = B, Q_C = C, Q_D = D

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Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	25			25			ns
Data setup time, t_{setup} (see Figures 1 and 2)	12			12			ns
Enable to clock setup time, t_{setup}	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA		0.30	0.45		0.30	0.45	
I_I	Enable	V_{CC}=MAX, V_I=7V				0.3			0.3	mA
	Others					0.1			0.1	
I_{IH}	Enable	V_{CC}=MAX, V_I=2.7V				60			60	μA
	Others					20			20	
I_{IL}	Enable	V_{CC}=MAX, V_I=0.4V				-1.08			-1.08	mA
	Others					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††		V_{CC}=MAX			20	35		20	35	mA

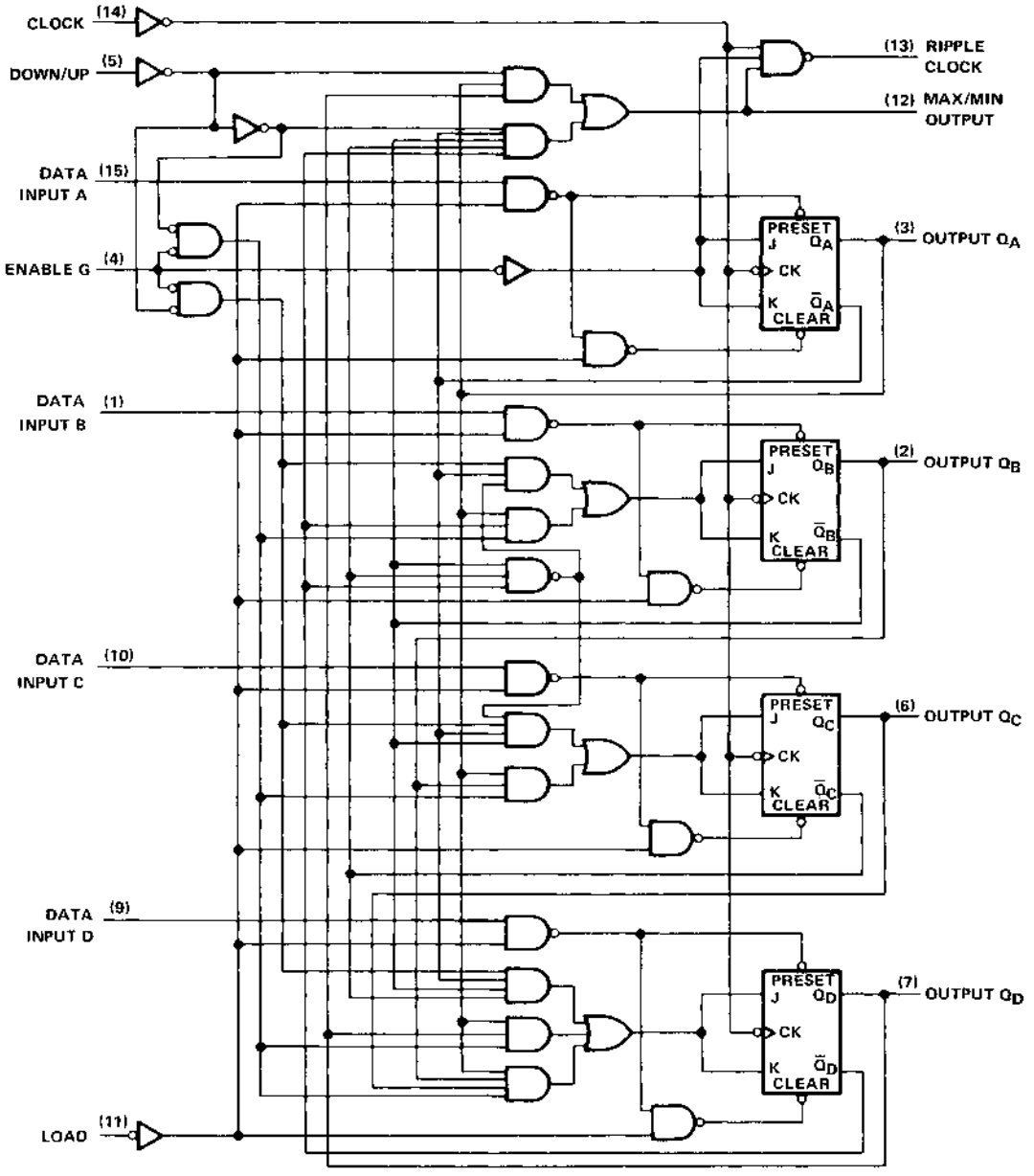
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, $V_{CC} = T_A = +25°C$

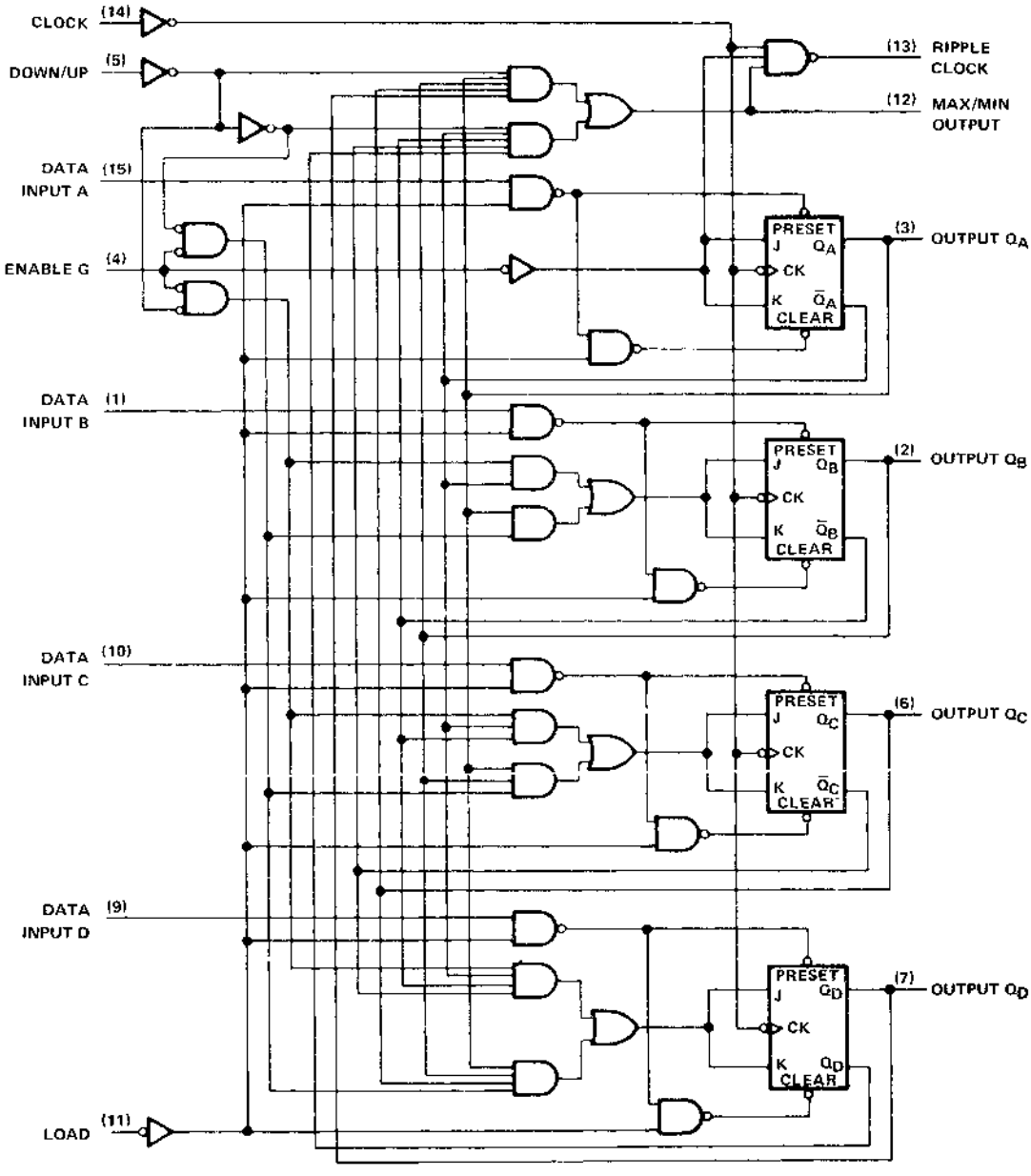
Parameter	From (input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (see Fig. 1 and 3 thru 7 on pages 3-56 and 3-57 and Fig. A on page 2-174)						
f_{max}			25	35		MHz
t_{PLH}	Load	Q_A,Q_B,Q_C,Q_D		22	33	ns
t_{PHL}				30	39	
t_{PLH}	Data A,B,C,D	Q_A,Q_B,Q_C,Q_D		13	22	ns
t_{PHL}				29	39	
t_{PLH}	Clock	Ripple Clock		11	18	ns
t_{PHL}				14	21	
t_{PLH}	Clock	Q_A,Q_B,Q_C,Q_D		15	21	ns
t_{PHL}				16	30	
t_{PLH}	Clock	Max/Min		23	39	ns
t_{PHL}				22	39	
t_{PLH}	Down/Up	Ripple Clock		16	45	ns
t_{PHL}				25	45	
t_{PLH}	Down/Up	Max/Min		17	33	ns
t_{PHL}				12	33	
t_{PLH}	Enable	Ripple Clock		10	19	ns
t_{PHL}				14	27	

LOGIC DIAGRAM

25LS190



LOGIC DIAGRAM
25LS191



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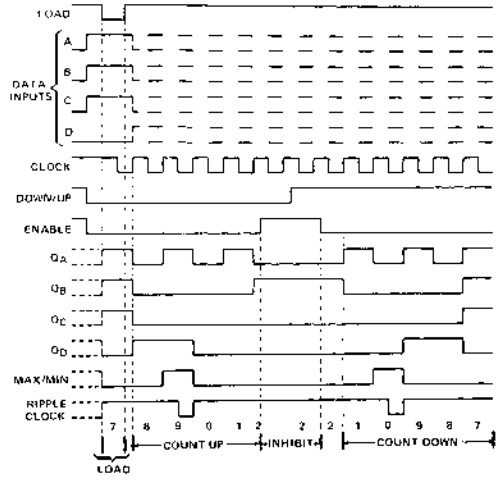
25LS190 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence.

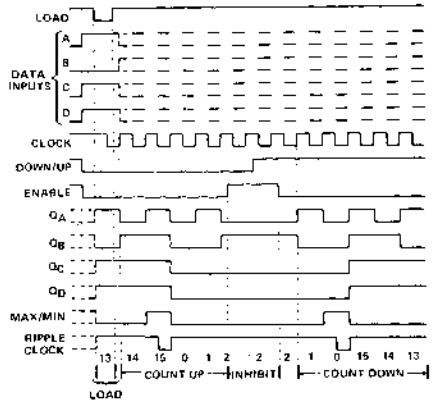
1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



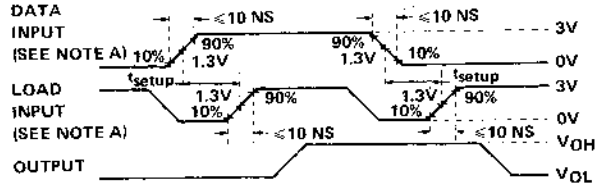
25LS191 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

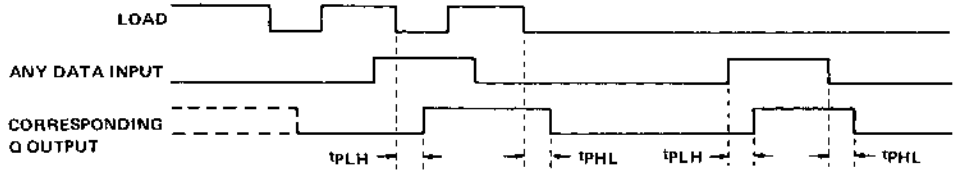


PARAMETER MEASUREMENT INFORMATION



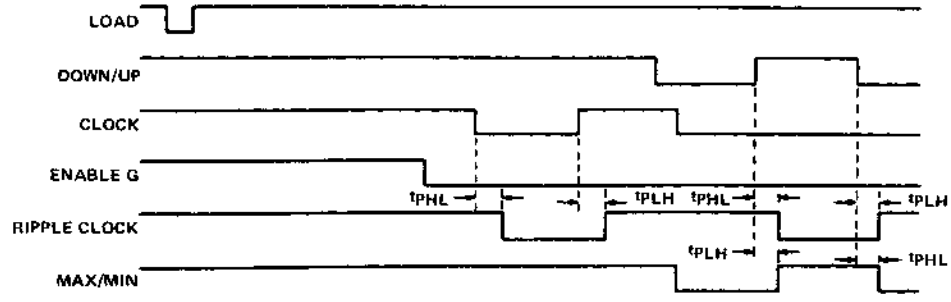
NOTE:
A. The inputs pulses are supplied by generators having the following characteristics: Z_{out} = 50Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.

FIGURE 1–DATA SETUP TIME VOLTAGE WAVEFORMS



NOTE: Conditions on other inputs are irrelevant.

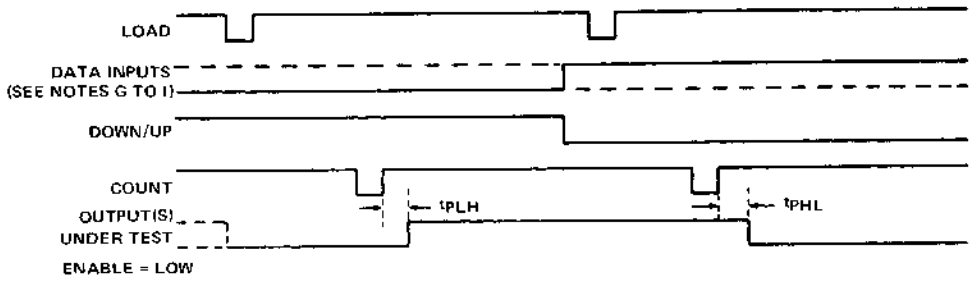
FIGURE 2–LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE: All data inputs are low.

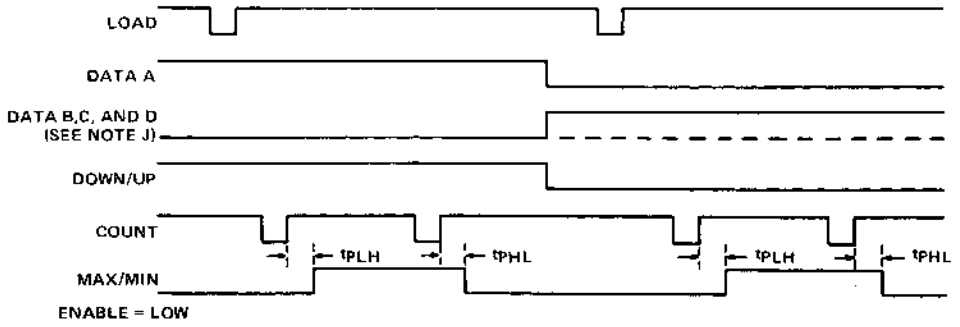
FIGURE 3–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO MAX/MIN

PARAMETER MEASUREMENT INFORMATION (Continued)



NOTES:
F. To test Q_A, Q_B, and Q_C outputs of 25LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
G. To test Q_D output of 25LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
H. To test Q_A, Q_B, Q_C, and Q_D outputs of 54LS191: All four data inputs are shown by the solid line.

FIGURE 4–CLOCK TO OUTPUT



NOTE I:
Data inputs B and C are shown by the dashed line for the 25LS190 and the solid line for the 25LS191: Data input D is shown by the solid line for both devices.

FIGURE 5–CLOCK TO MAX/MIN

FEATURES

- Separate clock inputs for count-up, count-down
- Asynchronous parallel load and clear
- Cascadable
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

DESCRIPTION

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The 25LS192 is a BCD counter and the 25LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

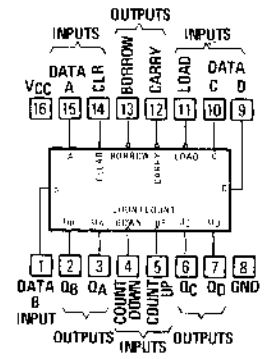
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

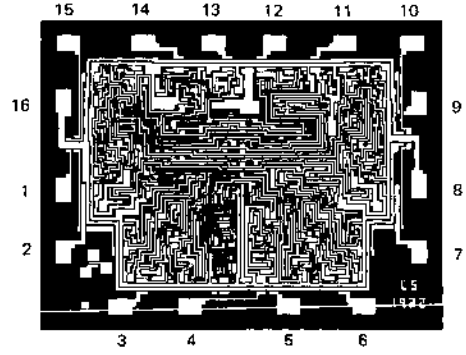
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN-OUT DIAGRAM

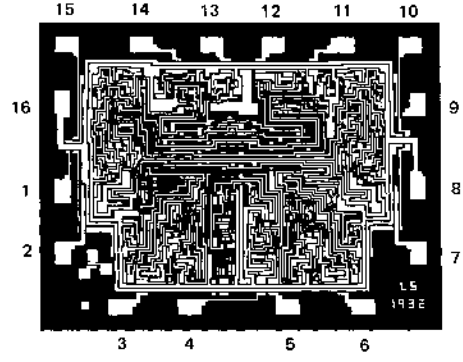


Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

25LS192



25LS193



Die Size: .100 x .077 (both types)

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Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-440			-440	μA
Low-level output current, I_{OL}	4		8	4		8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature range, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA		0.30	0.45		0.30	0.45	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††	V_{CC}=MAX			19	34		19	34	mA

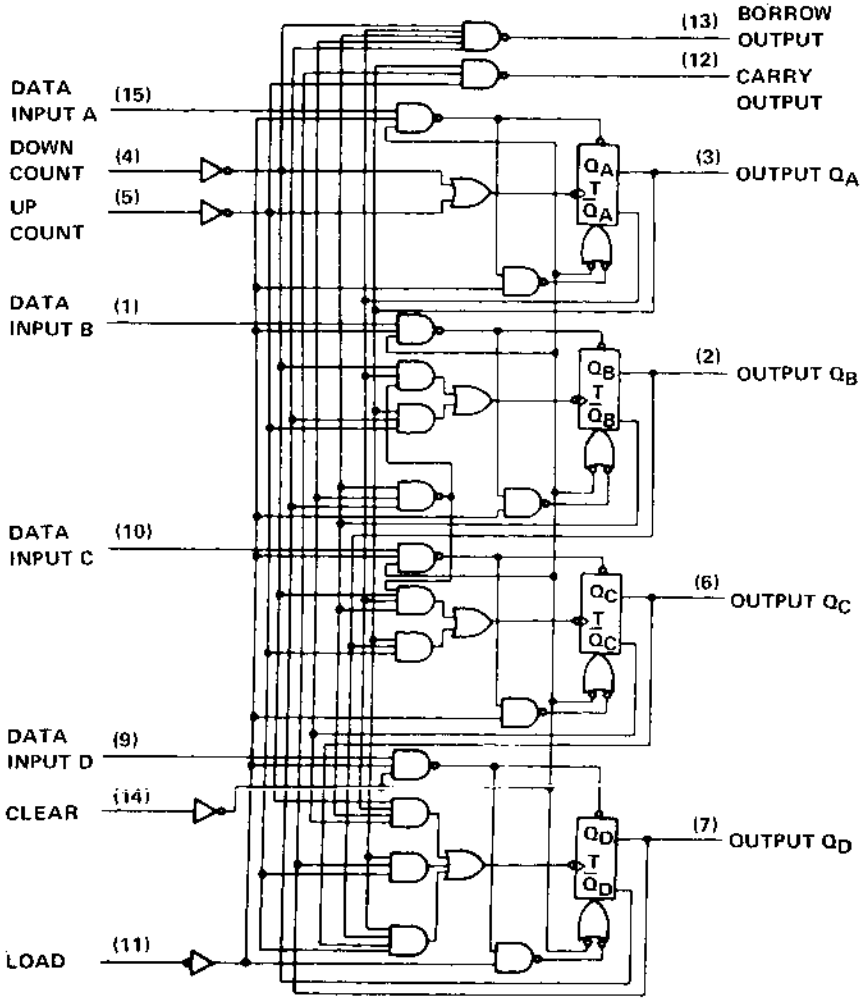
*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time
††I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

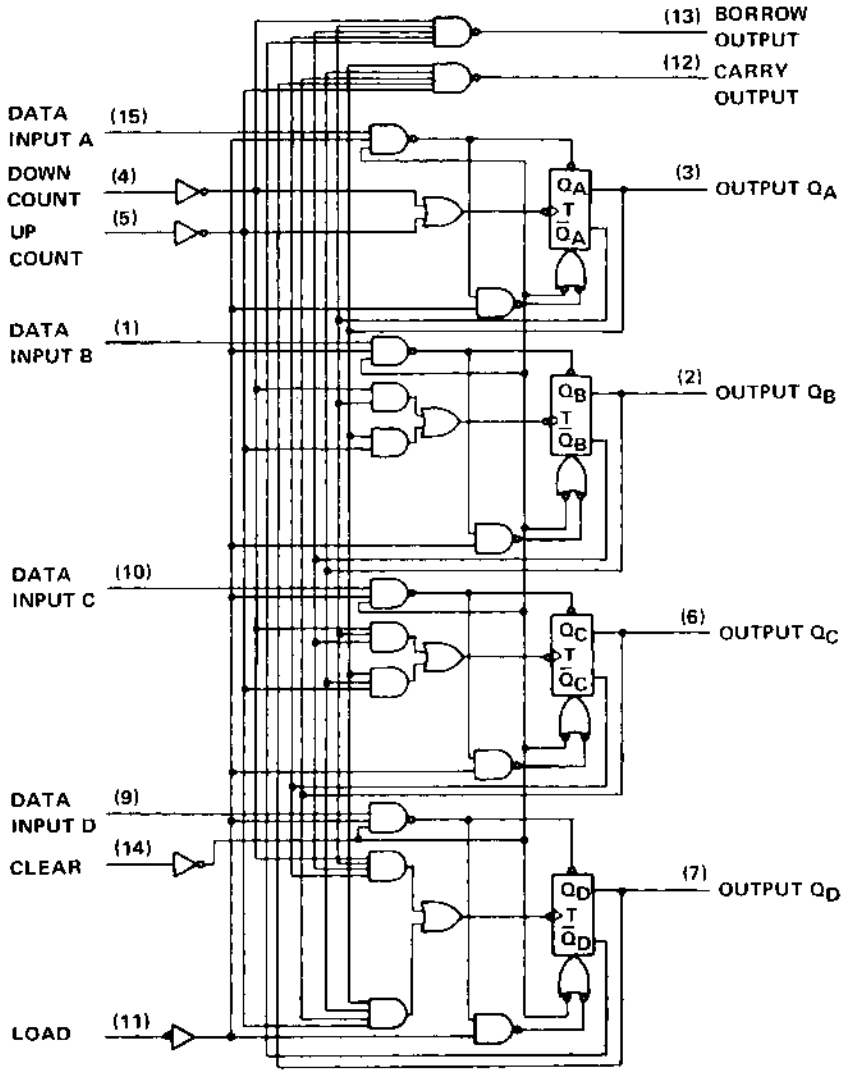
Parameters	From (input)	To (output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1 & 2 on page 3-62 and 3-63 and Fig. A, page 2-174)						
f_{max}			25	35		MHz
t_{PLH}	Count-up	Carry		9	18	ns
t_{PHL}				17	24	
t_{PLH}	Count-down	Borrow		9	18	ns
t_{PHL}				17	24	
t_{PLH}	Either Count	Q		19	30	ns
t_{PHL}				20	32	
t_{PLH}	Load	Q		22	33	ns
t_{PHL}				29	40	
t_{PHL}	Clear	Q		23	33	ns

LOGIC DIAGRAM

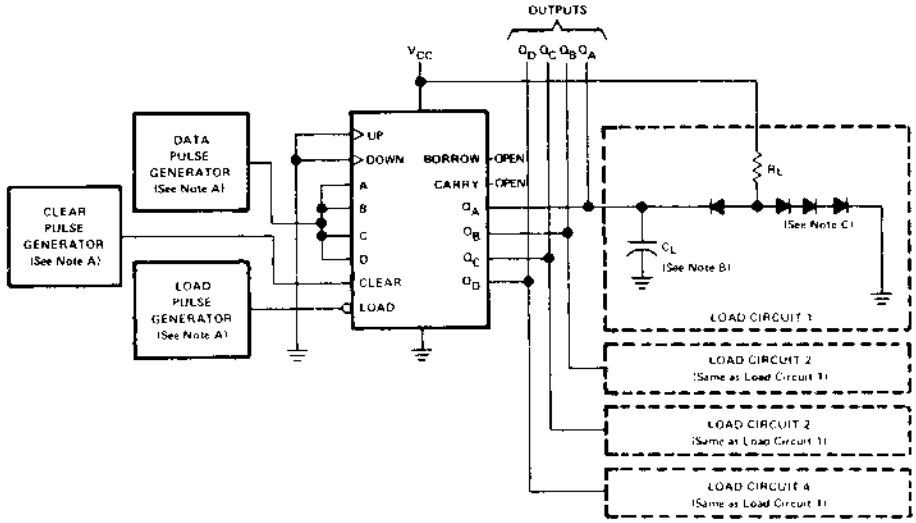
25LS192



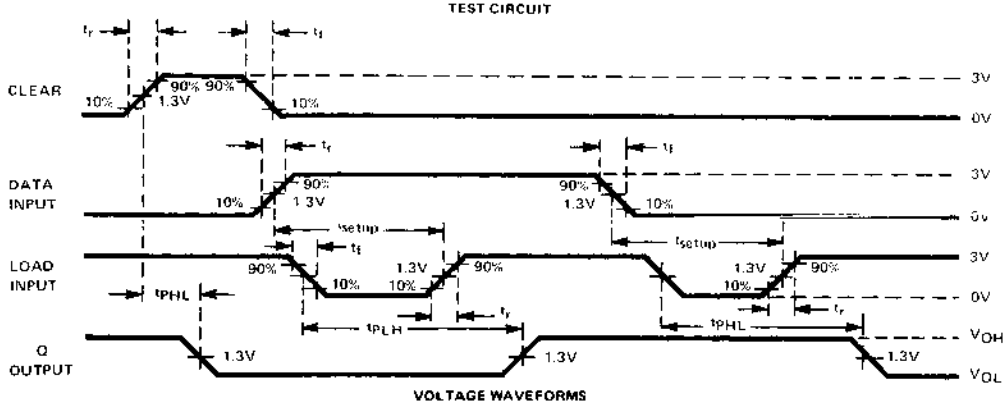
LOGIC DIAGRAM
25LS193



PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

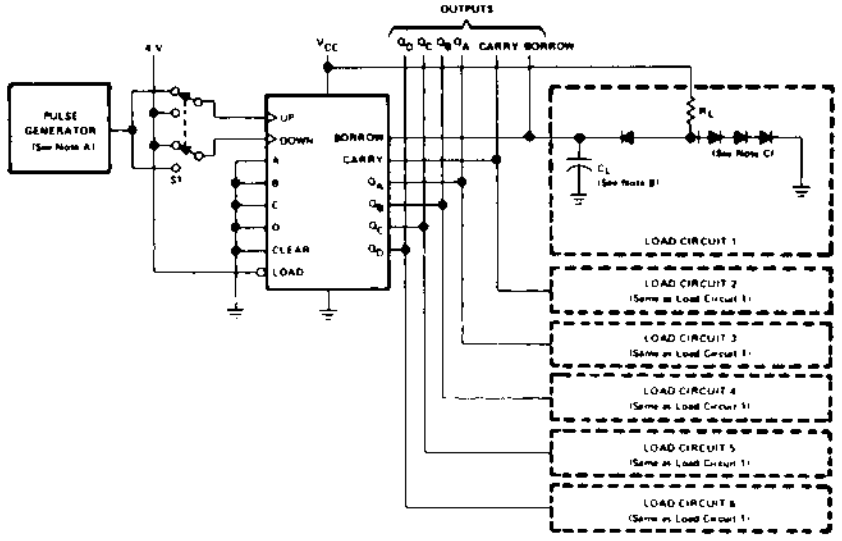


VOLTAGE WAVEFORMS

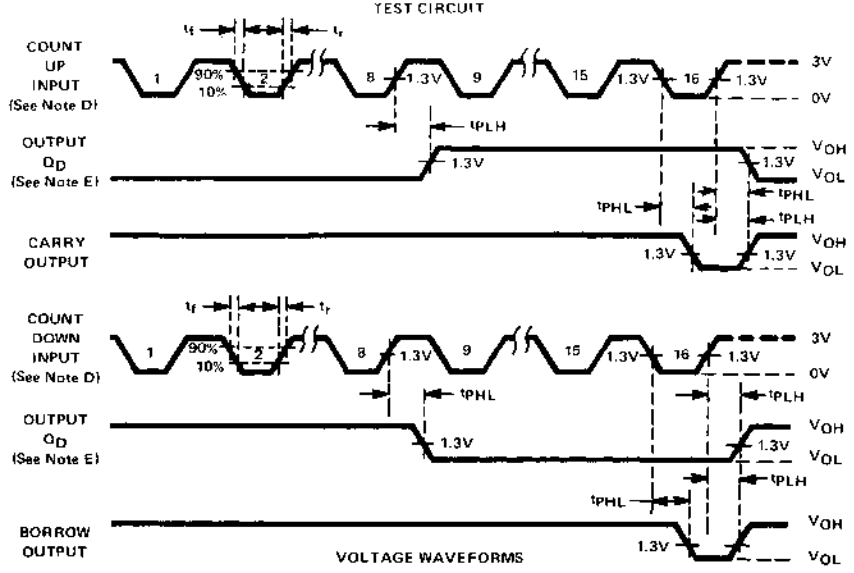
NOTES:
A. The pulse generators have the following characteristics: Z_{out} = 50Ω and for the data pulse generator PRR < 500KHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. t_r and t_f ≤ 7 ns.

FIGURE 1 — CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION (Continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

A. The pulse generator has the following characteristics: PRR ≤ 1MHz, Z_{out} = 50Ω, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064.
D. Count-up and count-down pulse shown is for the 25LS193 binary counter. Count cycle for 25LS192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and t_f ≤ 7ns.

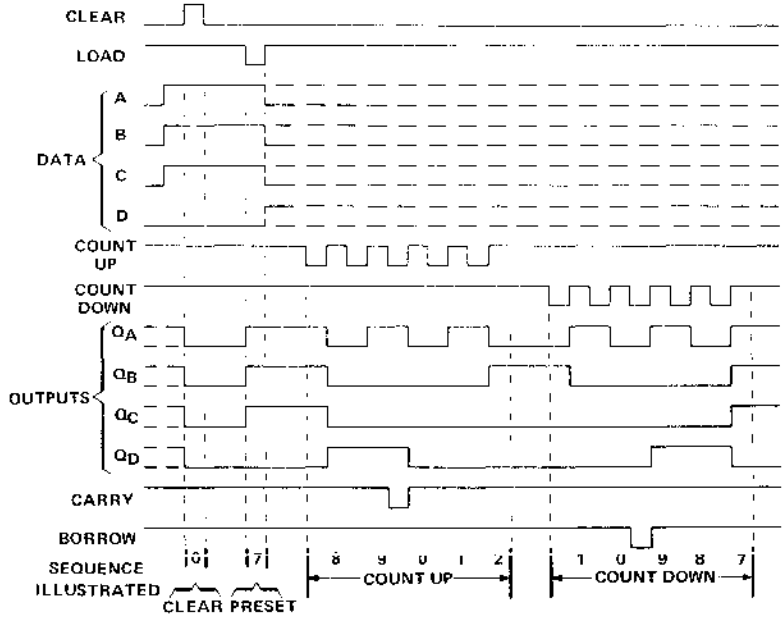
FIGURE 2–PROPAGATION DELAY TIMES

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

25LS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

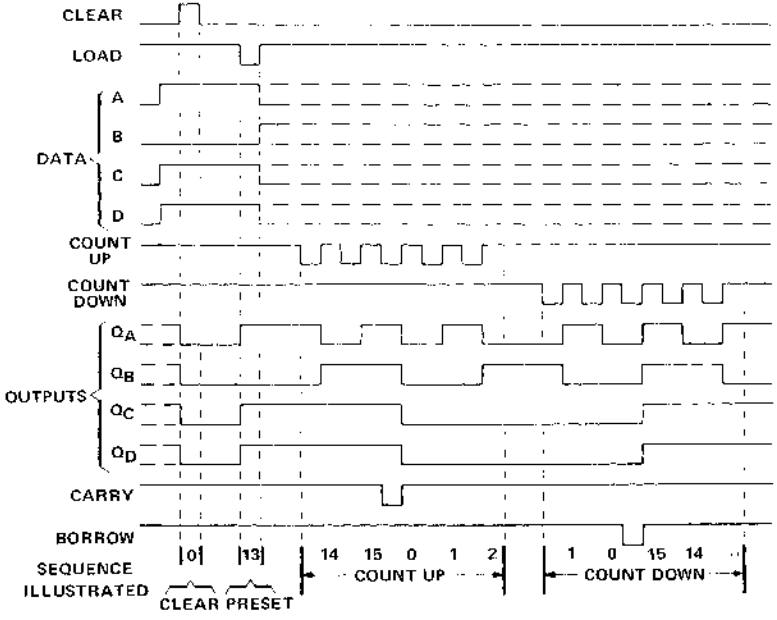


NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES
25LS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



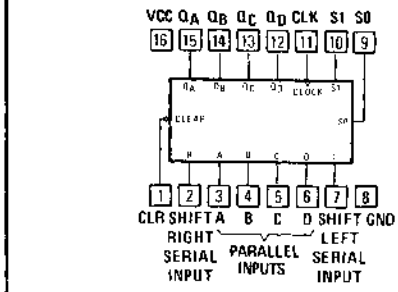
NOTES:
A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

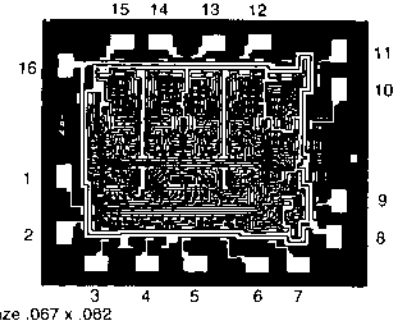
FEATURES

- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

PIN-OUT DIAGRAM

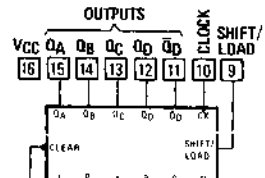
25LS194A

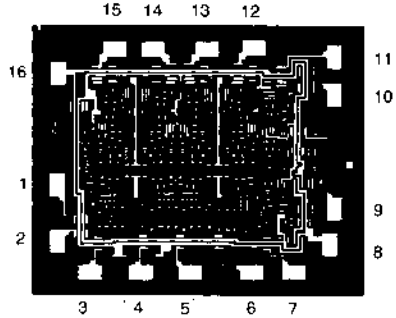




Die Size .067 x .082

25LS195A





Die Size .067 x .082

DESCRIPTION

The 25LS194A and 25LS195A are 4-bit registers that exhibit fully synchronous operation in all operating modes. The 25LS195A can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, Q_A, is loaded via the J and K inputs in the shift mode.

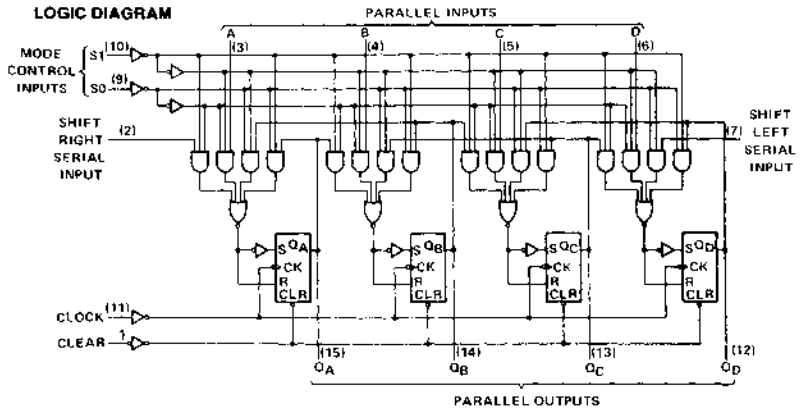
The 25LS194A operates in four modes under control of the two select inputs, S_0 and S_1. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the Q_A bit input from R), shift left (data comes from the flip-flop to the right, with the Q_D input from L), and hold or do nothing (each flip-flop receives data from its own output).

For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW synchronous clear (CLR) which forces all outputs to the LOW state (Q_D HIGH) independent of any other inputs.

Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

RAYTHEON

25LS194A
LOGIC DIAGRAM



25LS194A
FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE S1	MODE S0	CLOCK	SERIAL LEFT	SERIAL RIGHT	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

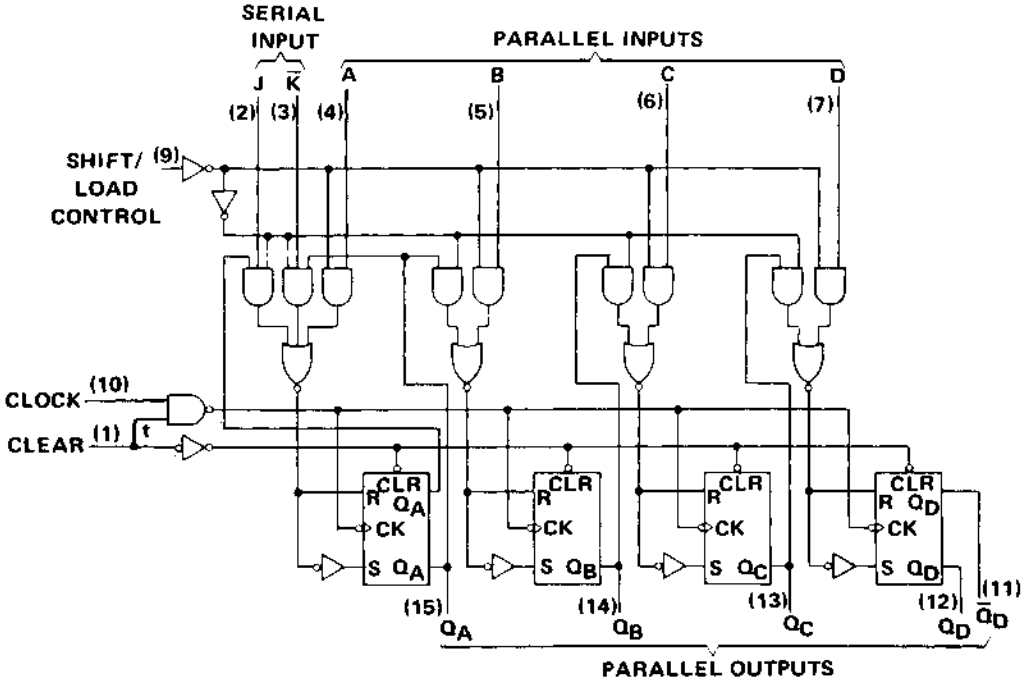
↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, $2Q_{D0}$ = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

25LS195A
LOGIC DIAGRAM



25LS195A
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock.

Recommended Operating Conditions

		Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-440			-440	μA
Low-level output current, I_{OL}		4		8	4		8	mA
Clock frequency, f_{clock}		0		35	0		35	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Mode control	30			30			ns
	Serial and parallel data	16			16			ns
	Clear inactive-state	18			18			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		Military			Commercial			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-440μA		2.5	3.5		2.7	3.4		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA		0.30	0.45		0.30	0.45	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.36	mA
I_{OS}†	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††	V_{CC}=MAX	25LS194A		15	23		15	23	mA
		25LS195A		14	21		14	21	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

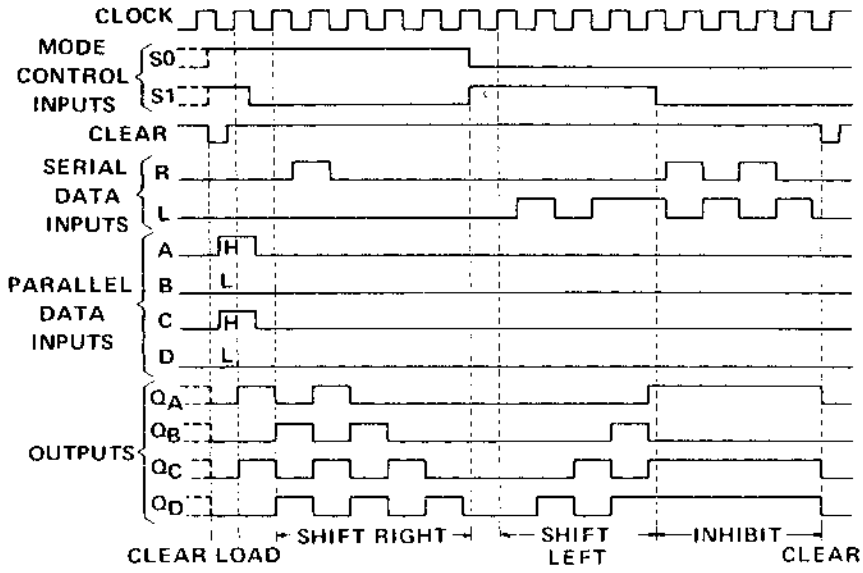
†Not more than one output should be shorted at a time.

††With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5V, applied to clock.

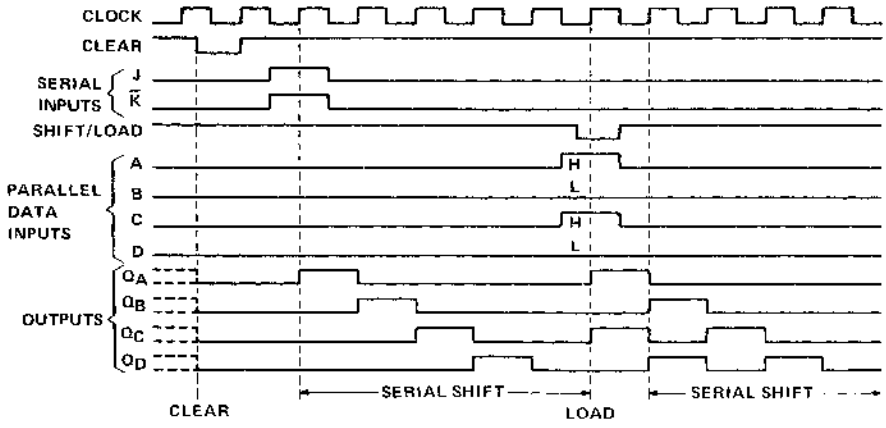
Switching Characteristics, V_{cc} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	25LS194A			25LS195A			Unit
			Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2.0kΩ (See Fig. 1 & 2 on page 3-71 and Fig. A on page 2-174)									
t_{PLH}	Clock	Q_i		13	21		13	21	ns
t_{PHL}				12	18		12	18	ns
t_{PHL}	Clear	Q_i		17	26		17	26	ns
t_{pw}	Pulse Width	Clock	17			16			ns
t_{pw}		Clear	17			12			ns
t_s	Set up time	Mode Control	25			25			ns
t_s		Data Input	16			15			ns
t_s	Clear recovery	Clock	20			20			ns
t_h	Hold time	Data	0			0			ns
t_R	Shift/Release Time (25LS195A only)				–			10	ns
f_{MAX}	Maximum clock frequency		35	55		35	55		MHz

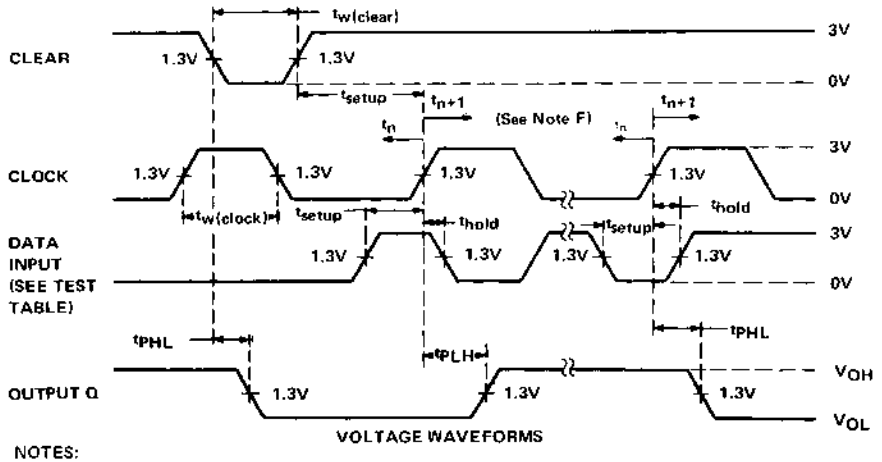
25LS194A
TYPICAL TIMING SEQUENCES



25LS195A
TYPICAL TIMING SEQUENCES



25LS194A



VOLTAGE WAVEFORMS

NOTES:

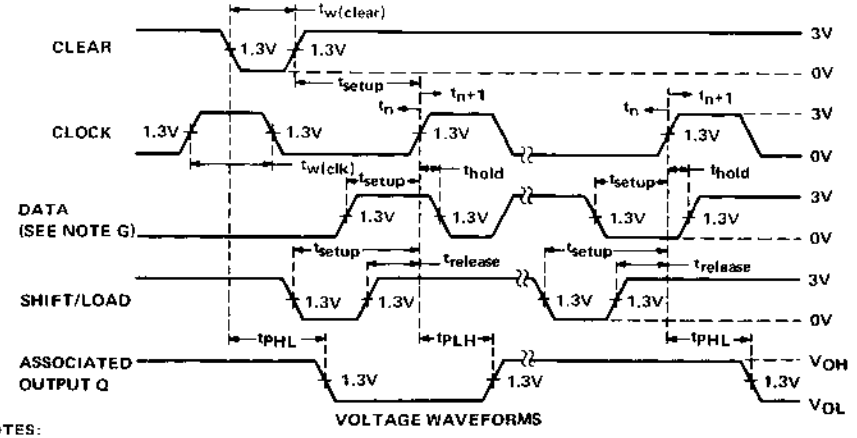
A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz, $t_r \leq$ 15ns and $t_f \leq 6$ ns. When testing f_{max}, vary PRR.

B. A clear pulse is applied prior to each test.

C. V_{ref} = 1.3V.
Proplagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1

25LS195A
LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ MHz, $t_r \leq 15$ ns, and $t_f \leq 6$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

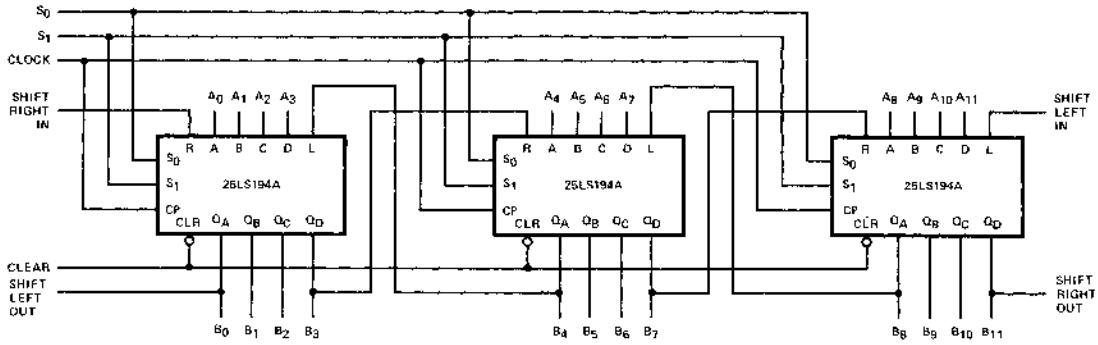
F. J and $\overline{K}$ are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 2

APPLICATION

12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL LOAD REGISTER



8-Line-To-1-Line Multiplexer With Three-State Outputs

25LS251

FEATURES

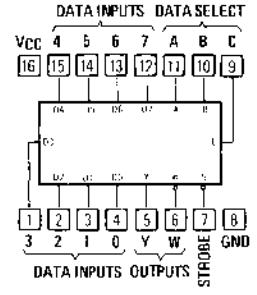
- Selects one of eight data sources
- Performs parallel-to-serial conversion
- Complementary 3-state outputs
- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

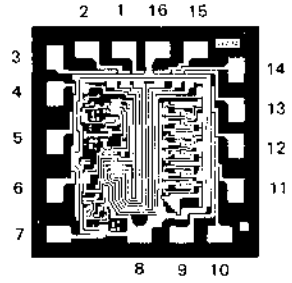
DESCRIPTION

This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources and features a strobe-controlled three-state output. The strobe must be at a low logic level to enable this device. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

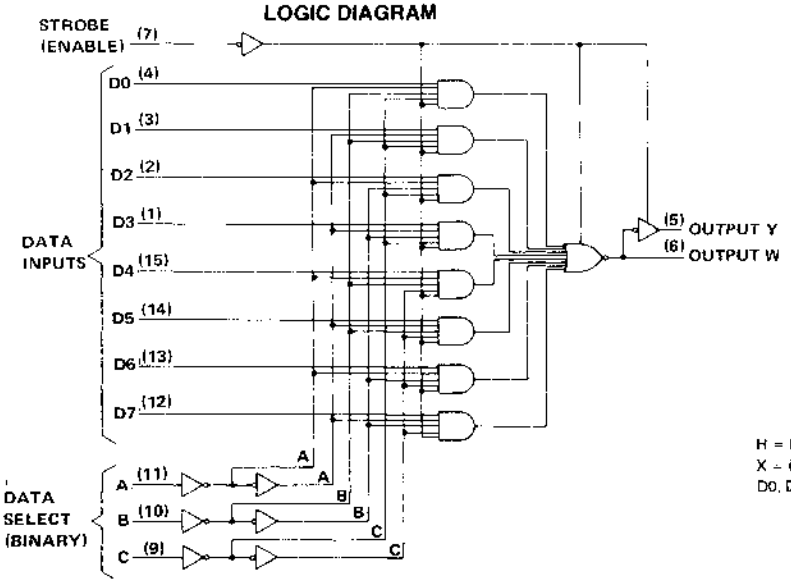
PIN-OUT DIAGRAM





Die Size: .056 x .057

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX, I_{OH}=MAX		2.4	3.4		2.4	3.2		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=MAX,	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
		I_{OL}=8mA		0.30	0.45		0.30	0.45	
$I_{O(off)}$	V_{CC}=MAX, V_{IH}=2V	V_O=2.7V			20			20	μA
		V_O=0.4V			-20			-20	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-85	-15		-85	mA
I_{CC}††	V_{CC}=MAX	Condition A		6.1	10		6.1	10	mA
		Condition B		7.1	12		7.1	12	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
A. Strobe grounded.
B. Strobe at 4.5V

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	From (Input)	To (Output)	+25°C			Unit
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	A, B, or C (4 levels)	Y		29	44	ns
t_{PHL}				20	30	
t_{PLH}	A, B, or C (3 levels)	W		16	24	ns
t_{PHL}				21	32	
t_{PLH}	Any D	Y		14	24	ns
t_{PHL}				11	17	
t_{PLH}	Any D	W		8	12	ns
t_{PHL}				9	14	
t_{ZH}	Strobe	Y		9	12	ns
t_{ZL}				13	19	
t_{ZH}	Strobe	W		4	15	ns
t_{ZL}				13	18	
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C, page 2-174)						
t_{HZ}	Strobe	Y		9	27	ns
t_{LZ}				10	18	
t_{HZ}	Strobe	W		17	29	ns
t_{LZ}				10	18	

Dual 4-Line to 1-Line Data Selectors/Multiplexers

25LS253

DISTINCTIVE CHARACTERISTICS

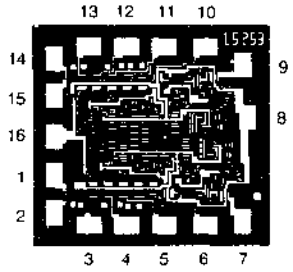
- **Permits multiplexing from N lines to 1 line**
- **Performs parallel-to-serial conversion**
- **Provides three-state outputs for data bus organization data bus organization**
- **100% reliability assurance testing in compliance with MIL-STD-883**

DESCRIPTION

This dual four-input multiplexer provides the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the 25LS153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

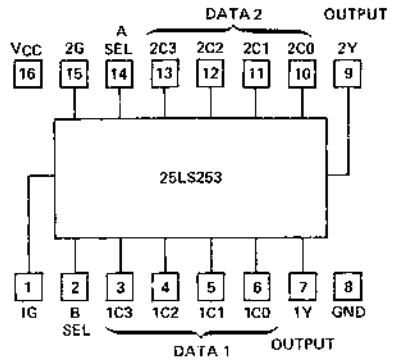
The 25LS253 features a three-state output to interface with bus organized systems. Each section of the 25LS253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

PIN-OUT DIAGRAM

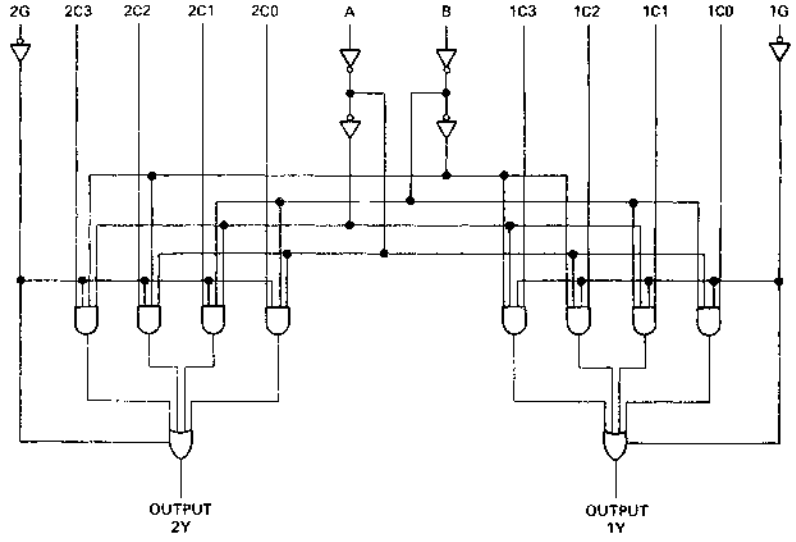


Die Size: .057 x .061

LOGIC SYMBOL



LOGIC DIAGRAM



G = Output Enable

Recommended Operating Conditions

	Military			Commercial			Units
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level Output Current, I_{OH}			1.0			1.0	mA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Operating Temperature Range (Unless Otherwise Noted)

Parameters	Test Conditions (Note 1)		Military			Commercial			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2			2			V
V_{IL}	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	V
V_I	V_{CC} = MIN., I_{IN} = −18mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA	2.4	3.4					V
		I_{OH} = −2.6mA				2.4	3.2		
V_{OL}	V_{CC} = MIN., V_{IH} = 2.0V, V_{IL} = V_{IL} MAX	I_{OL} = 4mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8mA		0.30	0.45		0.30	0.45	
I_{IL} (3)	V_{CC} = MAX., V_{IN} = 0.4V				−0.36			−0.36	mA
I_{IH} (3)	V_{CC} = MAX., V_{IN} = 2.7V				20			20	µA
I_I	V_{CC} = MAX., V_{IN} = 7.0V				0.1			0.1	mA
I_O	V_{CC} = MAX.	V_O = 2.4V			20			20	µA
		V_O = 0.4V			−20			−20	
I_{SC}	V_{CC} = MAX.		−15		−85	−15		−85	mA
I_{CC}	V_{CC} = MAX (Note 5)			7	12		7	12	mA

Switching Characteristics V_{cc} = 5V, T_A = 125°C

Parameters	From (Input)	To (Output)	+25°C			Units
			Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	C_i	Y_i		10	15	ns
t_{PHL}				7	12	
t_{PLH}	Select (A or B)	Y_i		20	30	ns
t_{PHL}				15	23	
t_{ZH}	G_i	Y_i		11	23	ns
t_{ZL}				15	23	
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C, page 2-174)						
t_{HZ}				12	18	ns
t_{LZ}				12	18	

FUNCTION TABLE

INPUTS			OUTPUTS	
Select		Data	LS253 Output Control	LS253 Output
B	A	C_0 C_1 C_2 C_3	G	Y
X	X	X X X X	H	Z
L	L	L X X X	L	L
L	L	H X X X	L	H
L	H	X L X X	L	L
L	H	X H X X	L	H
H	L	X X L X	L	L
H	L	X X H X	L	H
H	H	X X X L	L	L
H	H	X X X H	L	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance

NOTE: A & B are common to both 4-input multiplexers.

DEFINITION OF FUNCTIONAL TERMS:

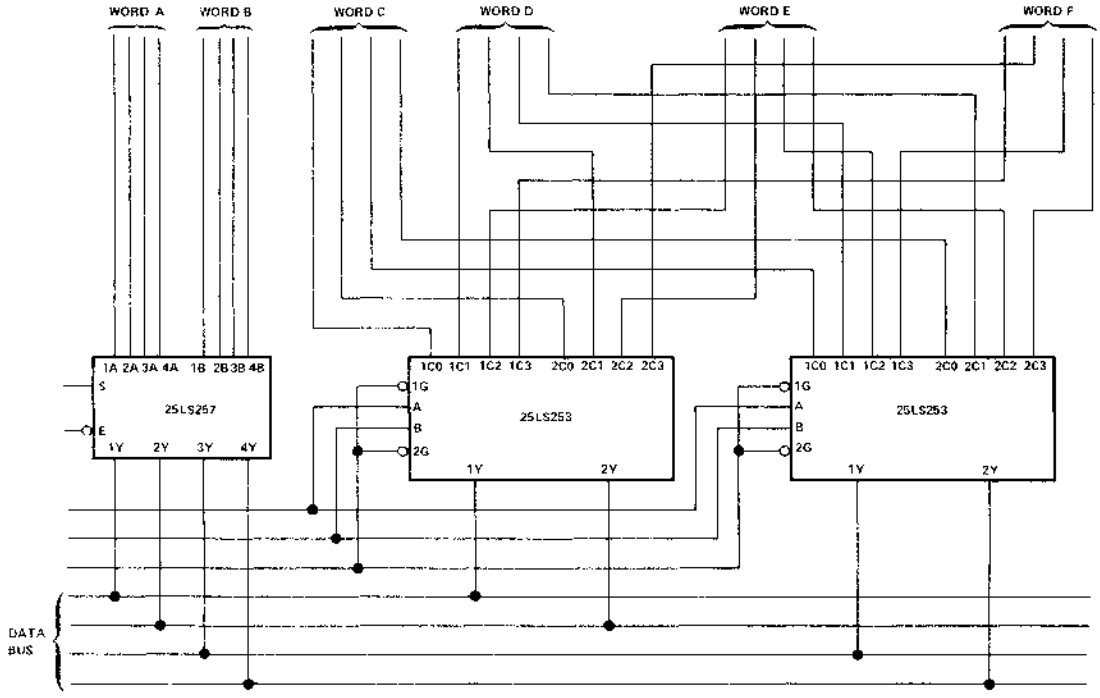
$1C_i$, $2C_i$ Data Inputs. The four data inputs to each multiplexer; i = 0, 1, 2, and 3.

1Y, 2Y Multiplexer Outputs. The output of each four-input multiplexer.

A, B Select Inputs. The inputs used to determine which of the four data inputs are selected for the output.

G Output Control. An active-LOW three-state control used to enable the output. A HIGH level input forces the output to the high-impedance (off) state.

APPLICATIONS



RAYTHEON

Quadruple 2-Line-To-1-Line Multiplexers With Three-State Outputs

25LS257 25LS258

FEATURES

- Higher speed compared to 9LS/54LS and 9LS/74LS
- 8mA sink current over full military temperature range
- 50mV improved V_{OL} compared to 9LS/74LS
- 440μA source current
- 100% reliability assurance testing in compliance with MIL-STD-883.

DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The 25LS257 presents true data; the 25LS258 presents inverted data. With Output Control HIGH, the outputs are forced to a high impedance state.

FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	LS257	LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

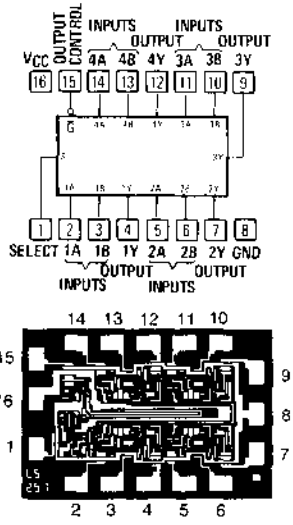
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Low level at S selects A inputs

High level at S selects B inputs.

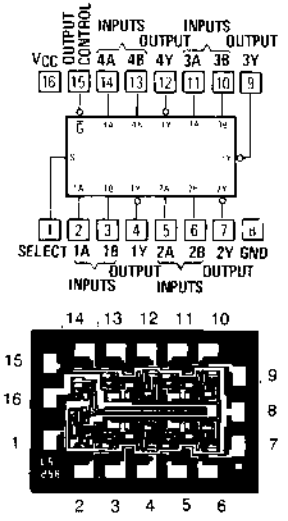
PIN-OUT DIAGRAMS

25LS257



Die Size .047 x .066

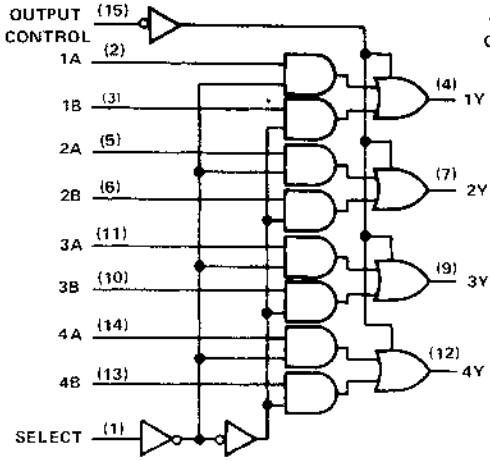
25LS258



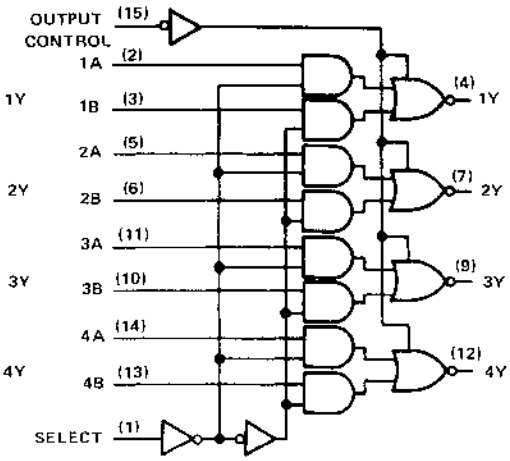
Die Size .047 x .066

LOGIC DIAGRAMS

25LS257



25LS258



Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-1			-2.6	mA
Low-level output current, I_{OL}	4		8	4		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*		Military			Commercial			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}		Guaranteed input logical high voltage for all inputs		2			2			V
V_{IL}		Guaranteed input logical low voltage for all inputs				0.7			0.8	V
V_I		V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max, I_{OH}=MAX	I_{OH} = -1.0mA	2.4	3.4					V
			I_{OH} = -2.6mA				2.4	3.1		
V_{OL}		V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL} max	I_{OL}=4mA		0.25	0.40		0.25	0.40	V
			I_{OL}=8mA		0.30	0.45		0.30	0.45	
I_{OZH}		V_{CC}=MAX, V_{IH}=2V V_O=2.4V				20			20	μA
I_{OZL}		V_{CC}=MAX, V_{IH}=2V, V_O=0.4V				-20			-20	μA
I_I	S input	V_{CC}=MAX, V_I=7V				0.2			0.2	mA
	Any other					0.1			0.1	
I_{IH}	S input	V_{CC}=MAX, V_I=2.7V				40			40	μA
	Any other					20			20	
I_{IL}	S input	V_{CC}=MAX, V_I=0.4V				-0.8			-0.8	mA
	Any other					-0.4			-0.4	
I_{OS}†		V_{CC}=MAX		-15		-85	-15	-15	-85	mA
I_{CC}††	All outputs high	V_{CC}=MAX	25LS257		5.9	10.0		5.9	10.0	mA
	All outputs low				8.2	13.5		9.2	13.5	
	All outputs off				10	15.3		10	15.3	
	All outputs high		25LS258		4.1	8.0		4.1	8.0	
	All outputs low				6.2	11.0		6.2	11.0	
	All outputs off				7.0	11.2		7.0	11.2	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics, V_{CC} = 5V, T_A = 25°C

Parameter ¶		From (input)	To (output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{PLH}	25LS257	Data	Any		6	12	ns
t_{PHL}					7	12	
t_{PLH}	25LS258	Data	Any		8	12	ns
t_{PHL}					5	12	
t_{PLH}	25LS257	Select	Any		12	18	ns
t_{PHL}					12	18	
t_{PLH}	25LS258	Select	Any		12	18	ns
t_{PHL}					10	18	
t_{ZH}	25LS257	Output Control	Any		10	18	ns
t_{ZL}					10	16	
t_{ZH}	25LS258	Output Control	Any		10	18	ns
t_{ZL}					11	18	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)							
t_{HZ}	25LS257	Output Control	Any		10	15	ns
t_{LZ}					10	18	
t_{HZ}	25LS258	Output Control	Any		9	15	ns
t_{LZ}					8	15	

8-Bit Universal Shift/Storage Register

25LS299

FEATURES

- Four operational modes
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

DESCRIPTION

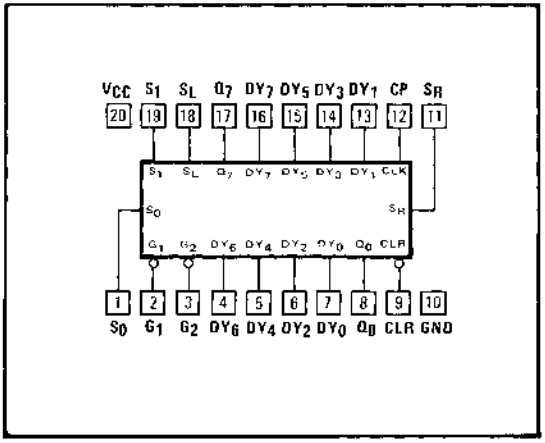
The 25LS299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible—Hold (store), shift left, shift right and load data.

Parallel load inputs and register outputs are multiplexed to reduce the number of package pins. Separate continuous outputs are also provided for flip-flop Q_0 and Q_7. These devices can be cascaded to N-Bit words.

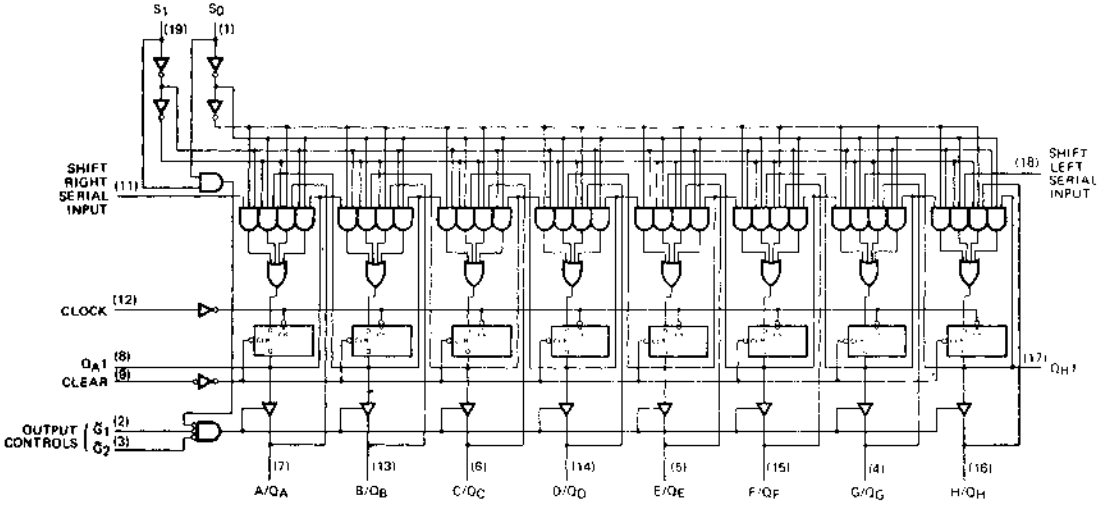
The 25LS299 has a typical shift frequency of 50 MHz; and is packaged in the standard 20-pin DIP package.

A separate active-LOW asynchronous clear input forces all flip-flops to the LOW state whenever this clear input is LOW.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



Recommended Operating Conditions

	Military			Commercial			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-Level Output Current, I_{OH}		-0.44	-1.0		-0.44	-2.6	mA
Low-Level Output Current, I_{OL}	4		8	4		8	mA
Operating Free-Air Temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions*			Military			Commercial			Unit
					Min	Typ**	Max	Min	Typ**	Max	
V_{IH}		Guaranteed input logical HIGH voltage for all inputs			2			2			V
V_{IL}		Guaranteed input logical LOW voltage for all inputs					0.7			0.8	V
V_I		V_{CC}=MIN., I_{IN}= -18mA					-1.5			-1.5	V
V_{OH}		V_{CC}=MIN.	Q_0,Q_7	I_{OH}=-0.44mA	2.5			2.7			V
		V_{IN}=V_{IH} or V_{IL}	DY_0,DY_7	I_{OH}=-1.0mA	2.4						V
				I_{OH}=-2.6mA				2.4			
V_{OL}		V_{CC}=MIN.		I_{OL} = 4.0mA		0.25	0.40		0.25	0.40	V
		V_{IN}=V_{IH} or V_{IL}		I_{OL} = 8.0mA		0.30	0.45		0.30	0.45	
I_I	S_0, S_1	V_{CC}=MAX., V_{IN} = 5.5V					0.2			0.2	mA
	All others						0.1			0.1	
I_H	S_0, S_1	V_{CC}=MAX., V_{IN} = 2.7V					40			40	µA
	All others						20			20	
I_{IL}	S_0, S_1	V_{CC}=MAX., V_{IN} = 0.4V					-0.8			-0.8	mA
	All others						-0.4			-0.4	
I_O		V_{CC} = MAX.		V_O= 0.4V			-100			-100	µA
				V_O= 2.7V			40			40	
I_{OS}		V_{CC} = MAX., See Note 3			-30		-85	-30		-85	mA
I_{CC}		V_{CC} = MAX., See Note 4				38	57		38	57	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. I_{CC} — measured with clock input HIGH and output controls HIGH.

Switching Characteristics, V_{CC} = 5V, T_A = +25°C

Parameter	From (input)	To (output)	+25°C Min	+25°C Typ	+25°C Max	Unit
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. A, page 2-174)						
t_{PLH}	Clock	Q_i		19		ns
t_{PHL}				23		
t_{PLH}	Clock	DY_i		18		ns
t_{PHL}				21		
t_{PHL}	Clear	DY_0-DY_7		25		ns
t_{PHL}	Clear	Q_0 or Q_7		27		ns
t_{ZH}	S_1, S_0	DY_i		20		ns
t_{ZL}				19		
t_{ZH}	$\overline{G}_1$, $\overline{G}_2$	DY_i		20		ns
t_{ZL}				18		
t_s	S_1, S_0 Set-up Prior to Clock		20			ns
t_s	S_R, S_L Set-up Prior to Clock		20			ns
t_{pw}	Pulse Width (Clock)		25			ns
t_n	Hold Time		3			ns
f_{max}				50		MHz
Test Conditions: C_L = 5pF, R_L = 2kΩ (See Fig. C, page 2-174)						
t_{LZ}	S_1, S_0	DY_i		22		ns
t_{HZ}				20		
t_{LZ}	$\overline{G}_1$, $\overline{G}_2$	DY_i		20		ns
t_{HZ}				16		

TRUTH TABLE

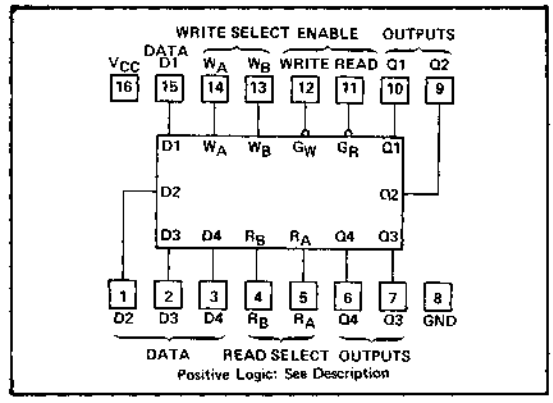
FUNCTION	INPUTS							OUTPUTS		INPUTS/OUTPUTS							
	S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$ $\overline{G}_2$	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear	X	X	L	X	(Note 1)		L L	L	L	L	L	L	L	L	L	L	L
Output Control	X	X	X	X	X	X	H L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	X	X	X	X	X	X	L H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	X	X	X	X	X	X	H H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
Hold	X	X	H	X	L	L	L L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
M Load (Note 2)	X	X	H	↑	H	H	L L	A	A	A	B	C	D	E	F	G	H
O Shift Right	L	X	H	↑	H	L	L L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
D Shift Right	H	X	H	↑	H	L	L L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
E Shift Left	X	L	H	↑	L	H	L L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
Shift Left	X	H	H	↑	L	H	L L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedence ↑ = Transition LOW-to-HIGH
H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_i are inputs.

FEATURES

- **Separate Read/Write Addressing Permits Simultaneous Reading and Writing**
- **Fast Access Times . . . Typically 20 ns**
- **Organized as 4 Words of 4 Bits**
- **Expandable to 512 Words of n-Bits**
- **For Use as:**
  - **Scratch-Pad Memory**
  - **Buffer Storage Between Processors**
  - **Bit Storage in Fast Multiplication Designs**
- **3-State Outputs**
- **The 25LS170 is Similar But Has Open-Collector Outputs**



DESCRIPTION

The 25LS670 MSI 16-bit TTL register file incorporates the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gates inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 25LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current three-state outputs. Up to 120 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

LOGIC

READ FUNCTION TABLE (SEE NOTES A AND D)

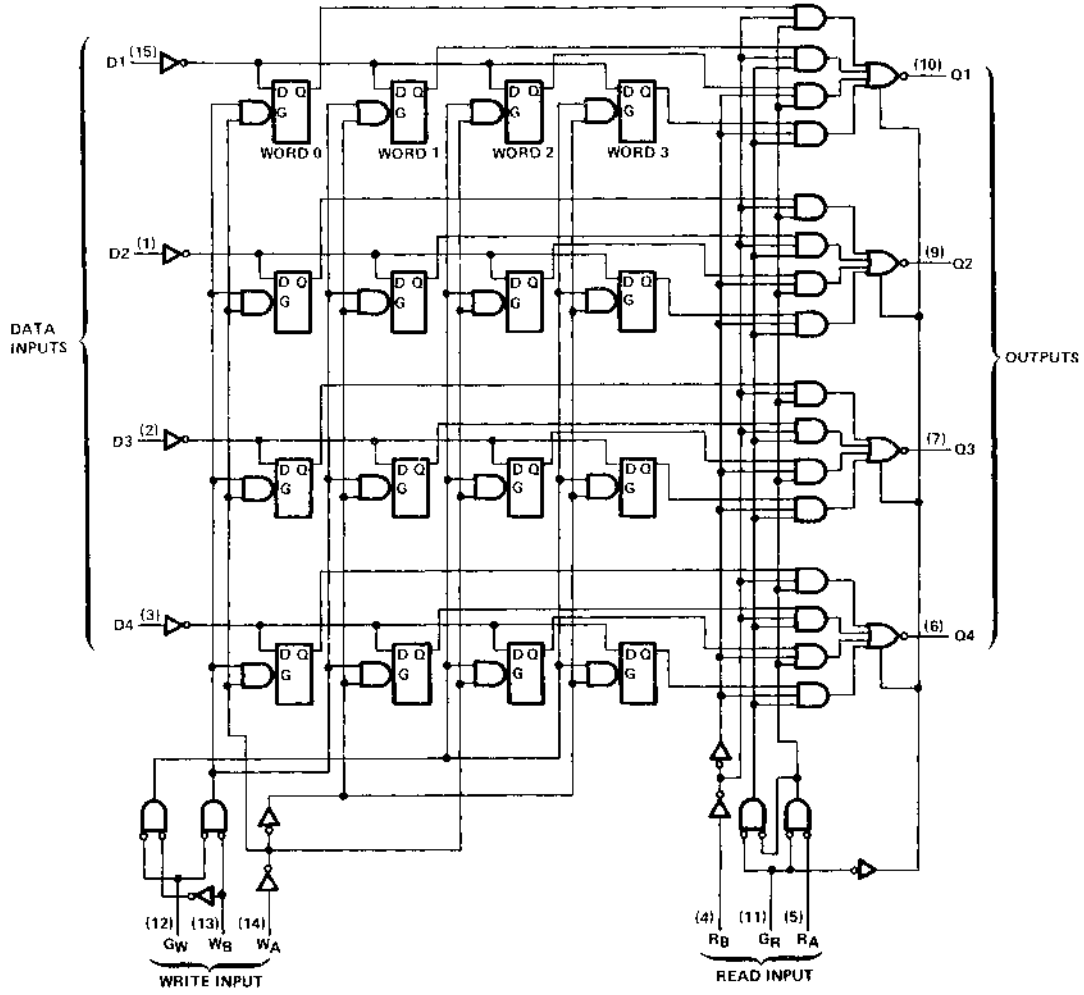
READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

FUNCTIONAL BLOCK DIAGRAM



Recommended Operating Conditions

		Military			Commercial			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}		4		8	4		8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	Write select with respect to write enable, $t_{setup(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_{hold(D)}$	15			15			ns
	Write select with respect to write enable, $t_{hold(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES 1. Voltage values are with respect to network ground terminal.

2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

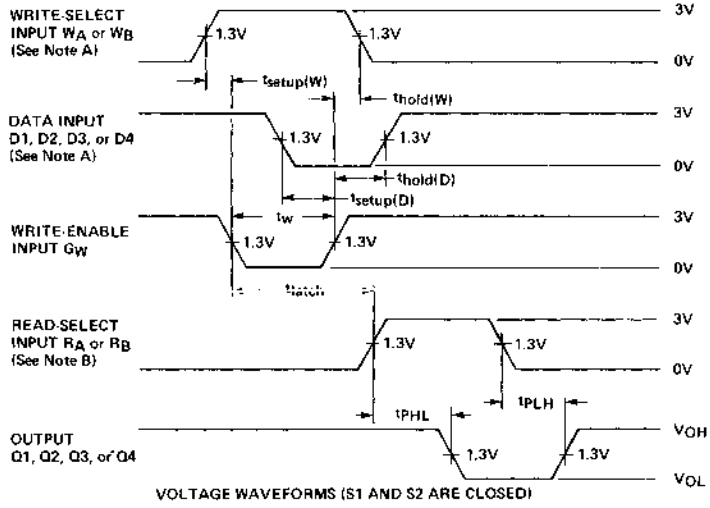
Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless otherwise Noted)

Parameter		Test Conditions†			Military			Commercial			Unit
					Min.	Typ‡	Max.	Min.	Typ‡	Max.	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V,	I_{OH} = −1mA	2.4	3.4					V
				I_{OH} = −2.6mA				2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V,	I_{OL} = 4mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.45		0.35	0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2V,	V_O = 2.7V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2V,	V_O = 0.4V			−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7V	Any, D, R, or W				0.1			0.1	mA
			G_W				0.2			0.2	
			G_R				0.3			0.3	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V	Any D, R, or W				20			20	μA
			G_W				40			40	
			G_R				60			60	
I_{IL}	Low-level input current	V_{CC} = MAX	Any D, R, or W				−0.4			−0.4	mA
			G_W				−0.8			−0.8	
			G_R				−1.2			−1.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−15		−85	−15		−85	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4			30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

Switching Characteristics, V_{CC} = 5V, Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	+25°C Min.	+25°C Typ.	+25°C Max.	Unit
Test Conditions: C_L = 15pF, R_L = 2.0kΩ (See Fig. 1 & 2 on page 3-90 & 3-91 and Fig. A on page 2-174)						
t_{PLH}	Read	Any Q		23	40	ns
t_{PHL}	Select			25	45	
t_{PLH}	Write	Any Q		26	45	ns
t_{PHL}	enable			28	50	
t_{PLH}	Data	Any Q		25	45	ns
t_{PHL}				23	40	
Test Conditions: C_L = 5pF, R_L = 2.0kΩ (See Fig. C, page 2-174)						
t_{ZH}	Read	Any Q		15	35	ns
t_{ZL}	enable			22	40	
t_{HZ}				30	50	ns
t_{LZ}				16	35	



VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

FIGURE 1

NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read select input, the read-enable input is low.

C. Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 15 ns, t_f ≤ 6 ns.

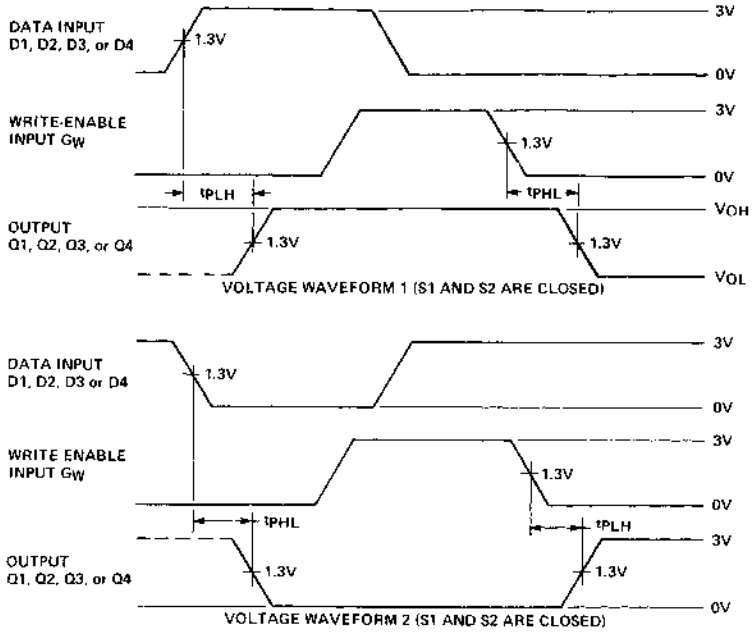


FIGURE 2

NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

B. Input waveforms are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle $\leq$ 50%, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

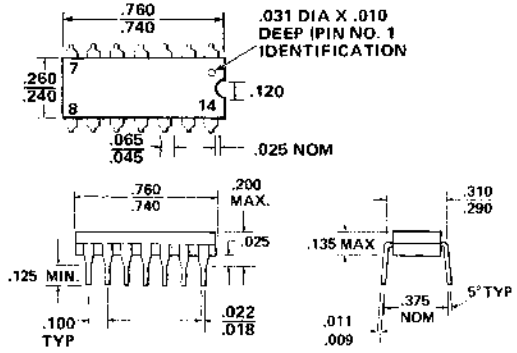
SECTION 4
Packaging Information

CONTENTS PAGE

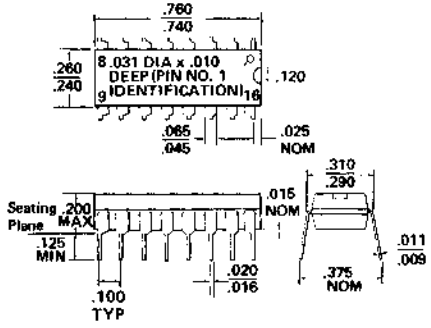
Packaging Information

Plastic Packages

14-PIN PLASTIC DIP
DB/BD

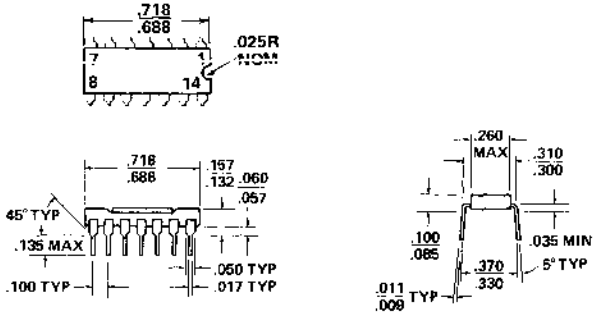


16-LEAD PLASTIC DIP
BM/MB



Metal Package

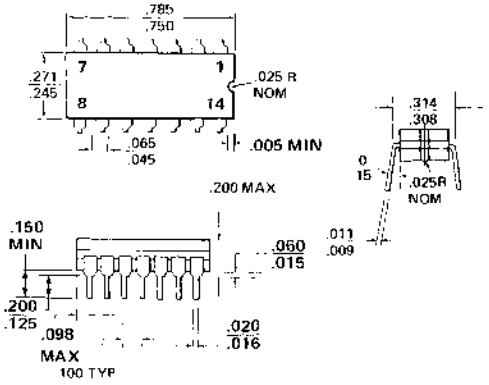
14-LEAD METAL DIP
D



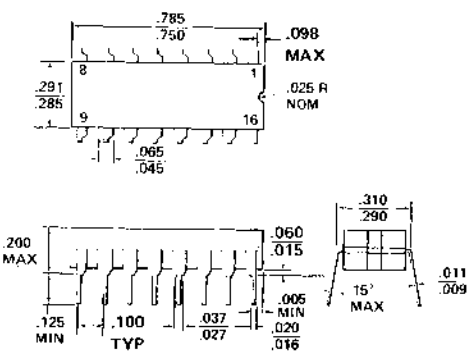
RAYTHEON

Ceramic Packages

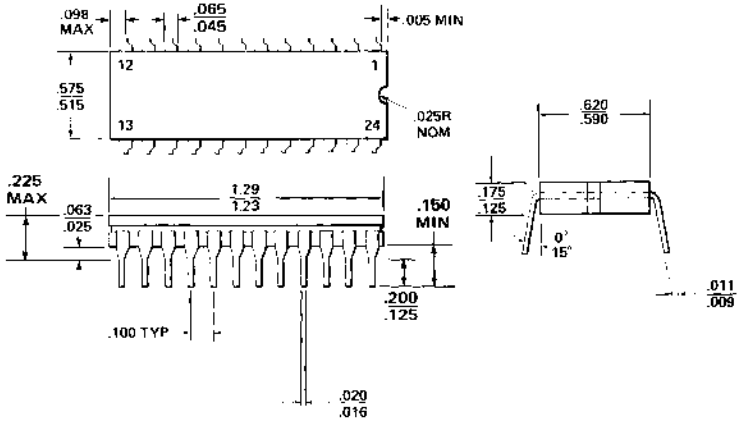
14-LEAD CERAMIC DIP
DC/J



16-LEAD
CERAMIC PACKAGE
DM

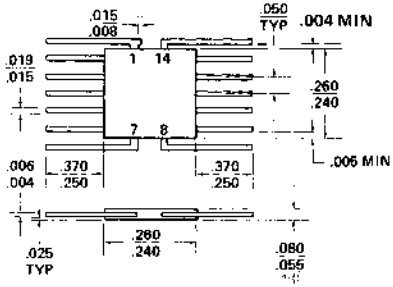


24-LEAD
CERAMIC PACKAGE
R/J

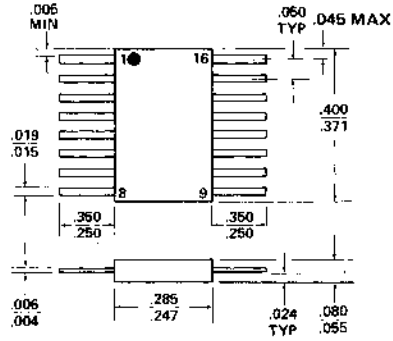


Ceramic

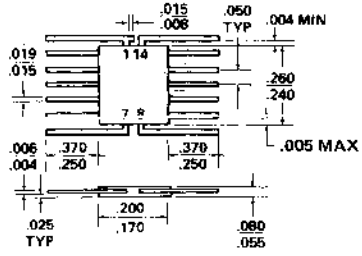
14-LEAD CERAMIC FLAT PACKAGE CJ/W



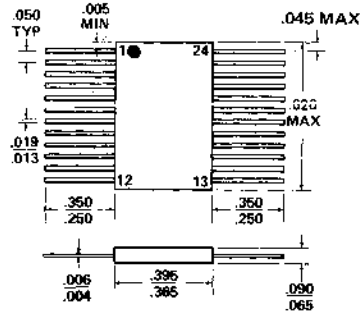
16-LEAD CERAMIC FLAT PACKAGE CL/W



14-LEAD CERAMIC FLAT PACKAGE CK



24-LEAD CERAMIC FLAT PACKAGE CN/W



Metal

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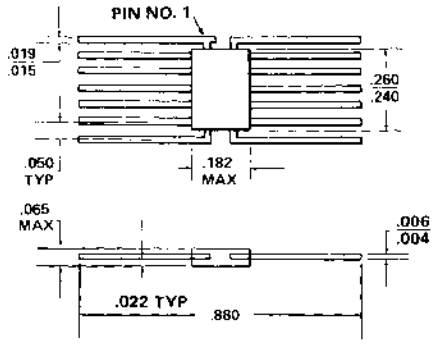
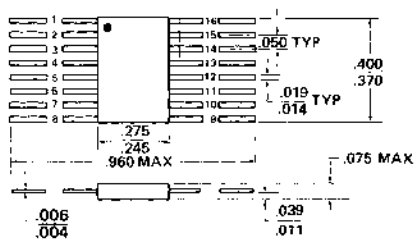
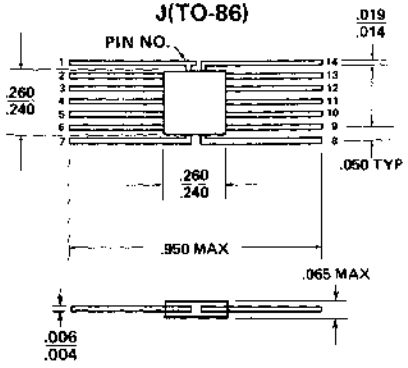


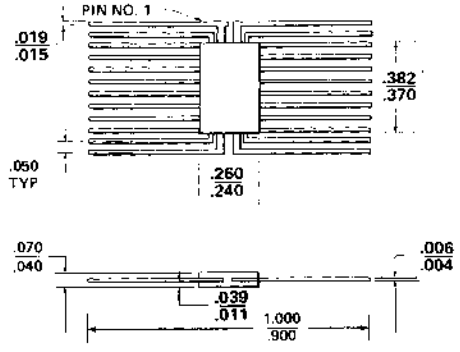
16-LEAD METAL FLAT PACKAGE L

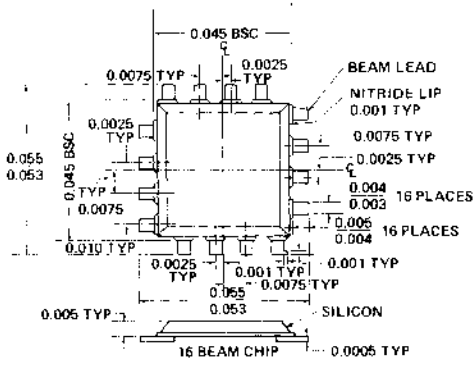


14-LEAD METAL FLAT PACKAGE J(TO-86)



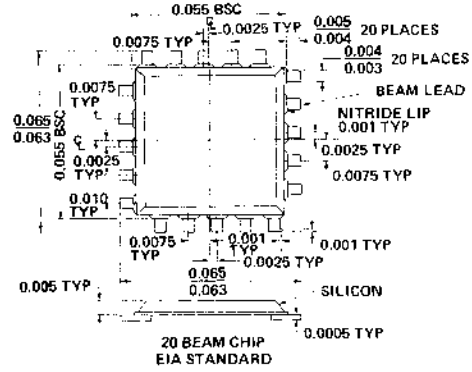
24-LEAD METAL FLAT PACKAGE N





NOTE: 1. METALIZATION DOWN
2. COUNTER CLOCKWISE BEAM ORDER

MECHANICAL OUTLINE 9



NOTE: 1. METALIZATION DOWN
2. COUNTER CLOCKWISE BEAM ORDER

MECHANICAL OUTLINE 12

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