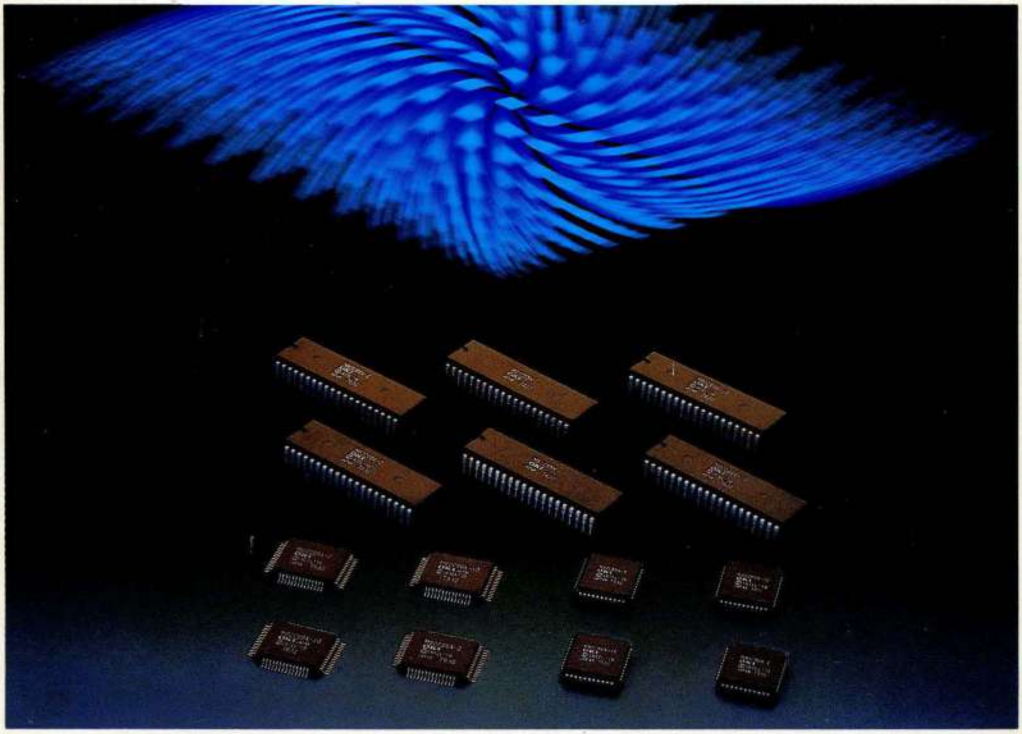
DATA BOOK

OKI

MICROPROCESSOR



THIRD EDITION
ISSUE DATE: MAR., 1988

MICROPROCESSOR DATA BOOK 1988

CONTENTS

CMOS MICROPROCESSOR LINE - UP

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PRODUCTS	PART NAME	POWER SUPPLY VOLTAGE	POWER SUPPLY CURRENT (MAX)	PACKAGE	REMARKS	COMPATIBILITY SUPPLIER	COMPATIBILITY TYPE
8 BIT CPU	MSM80C85A	5V	22mA	40 DIP 44 FLAT 44 PLCC	8 BIT MICROPROCESSOR 3 MHz	Intel	8085A
	MSM80C85A-2	5V	20mA	40 DIP 44 FLAT 44 PLCC	8 BIT MICROPROCESSOR 5 MHz	Intel	8085A-2
16 BIT CPU	MSM80C86A	5V	55mA	40 DIP 56 FLAT 44 PLCC	16 BIT MICROPROCESSOR 5 MHz	Intel	8086
	MSM80C86A-2		80mA		8 MHz	Intel	8086-2
	MSM80C86A-10		100mA		10 MHz		
8 BIT CPU	MSM80C88A	5V	55mA	40 DIP 56 FLAT 40 PLCC	8 BIT MICROPROCESSOR 5 MHz	Intel	8088
	MSM80C88A-2		80mA		8 MHz	Intel	8088-2
	MSM80C88A 10		100mA		10 MHz		
I/O	MSM81C55-5	5V	5mA	40 DIP 44 FLAT 44 PLCC	2048 BIT STRAM with I/O and TIMER	Intel	8355
	MSM82C12	5V	1mA	24 DIP 24 FLAT	8 BIT INPUT/OUTPUT PORT	Intel	8212
	MSM82C37A-5	5V	10mA	40 DIP 44 FLAT 44 PLCC	PROGRAMMABLE DMA CONTROLLER	Intel	8237A
	MSM82C43	5V	1mA	24 DIP 24 FLAT	INPUT/OUTPUT PORT EXPANDER		
	MSM82C51A MSM82C51A-2	5V	5mA	28 DIP 32 FLAT 28 PLCC	PROGRAMMABLE COMMUNICA–TIONS INTERFACE	Intel	8251A
	MSM82C53-5	5V	5mA	24 DIP 32 FLAT 28 PLCC	PROGRAMMABLE INTERVAL TIMER	Intel	8253
	MSM82C53-2		8mA				
	MSM82C54-2	5V	10mA	24 DIP 32 FLAT 28 PLCC	PROGRAMMABLE COUNTER	Intel	8254
	MSM82C55A-5	5V	5mA	40 DIP 44 FLAT 44 PLCC *1	PROGRAMMABLE PERIPHERAL INTERFACE	Intel	8255
	MSM82C55A-2		8mA				
	MSM82C59A-2	5V	5mA	28 DIP 32 FLAT 28 PLCC	PROGRAMMABLE INTERRUPT CONTROLLER	Intel	8259A-2
	MSM82C84A	5V	10mA	18 DIP 24 FLAT	CLOCK GENERATOR and DRIVER	Intel	8284A
	MSM82C84A-5	5V	10mA	18 DIP 24 FLAT	CLOCK GENERATOR and DRIVER (5 MHz)	Intel	8284A
	MSM82C84A-2		16mA		CLOCK GENERATOR and DRIVER (8 MHz)		
	MSM82C88 MSM82C88-2	5V	10mA	20 DIP 24 FLAT	BUS CONTROLLER	Intel	8288
	MSM83C55	5V	5mA	40 DIP 44 FLAT 44 PLCC	16384 BIT ROM with I/O	Intel	8355
PERI-PHERALS	MSM5832	5V	0.1mA	18 DIP	REAL TIME CLOCK		
	MSM58321	5V	0.1mA	16 DIP	REAL TIME CLOCK		
	MSM6242	5V	10μA	18 DIP 24 FLAT	REAL TIME CLOCK DIRECT BUS CONNECTED		

*1 44PLCC is only available for 82C55A-2.

SYSTEM CONFIGURATION

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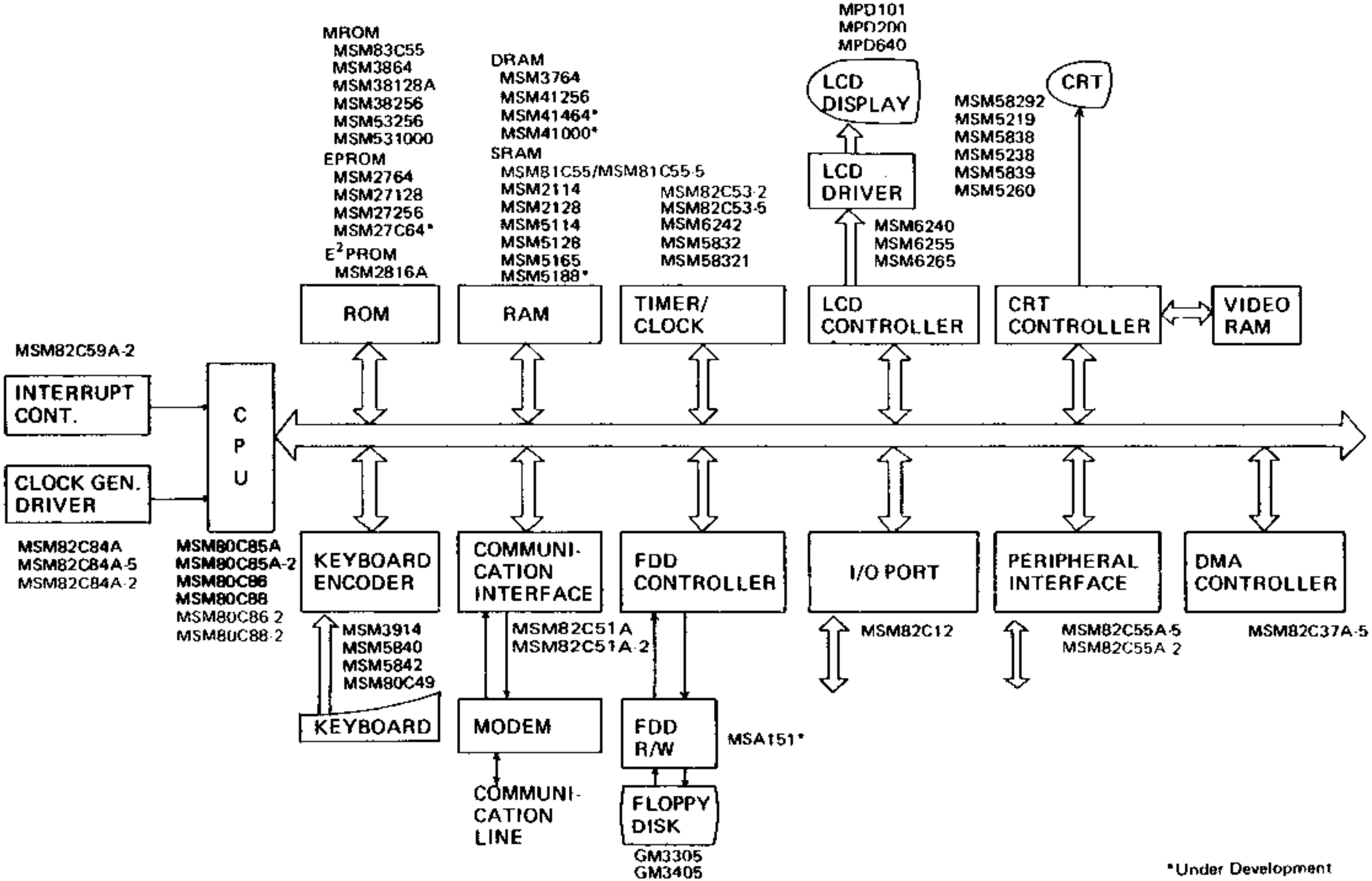
PERSONAL COMPUTER/WORD PROCESSOR SYSTEM CONFIGURATION



*Under Development

2

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PACKAGING

PACKAGING

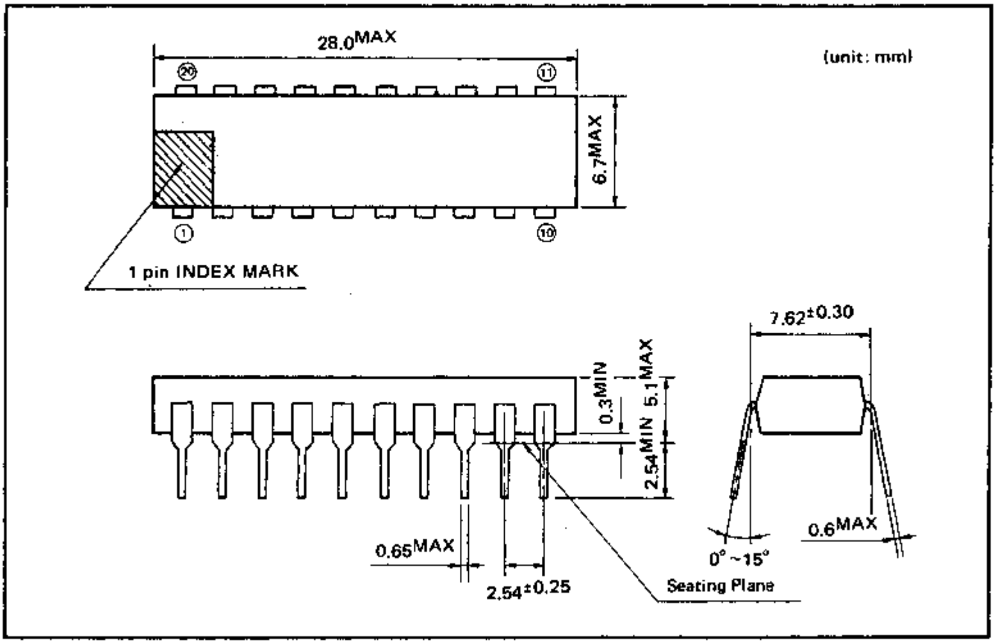
PRO-DUCTS	PART NAME	PACKAGE/PIN COUNT		
		DIP	FLAT	PLCC
MPU	M80C85A (Note: 1)	40	44	44
	M80C85A-2	40	44	44
	M80C86A	40	56	44
	M80C86A-2/80C86A-10	40	56	44
	M80C88A	40	56	44
	M80C88A-2/80C88A-10	40	56	44
I/O	M81C55/81C55-5	40	44	44
	M82C12	24	24	–
	M82C37A-5	40	44	44
	M82C43	24	24	–
	M82C51A	28	32	–
	M82C51A-2	28	32	28
	M82C53-5/82C53-2	24	32	28
	M82C54-2	24	32	28
	M82C55A-5/82C55A-2	40	44	44(Note:2)
	M82C59A-2	28	32	28
	M82C84A	18	24	–
	M82C84A-5/84A-2	18	24	20(Note:3)
	M82C88	20	24	–
	M82C88-2	20	24	20
	M83C55	40	44	44
PERI-PHER-ALS	M5832	18	–	–
	M58321	16	–	–
	M6242	18	24	–

Note: 1. Model numbers suffixed by RS denote plastic DIP, while GS denotes plastic FLAT.
Ex. MSM80C85ARS . . . . plastic DIP
MSM80C85AGS . . . . plastic FLAT

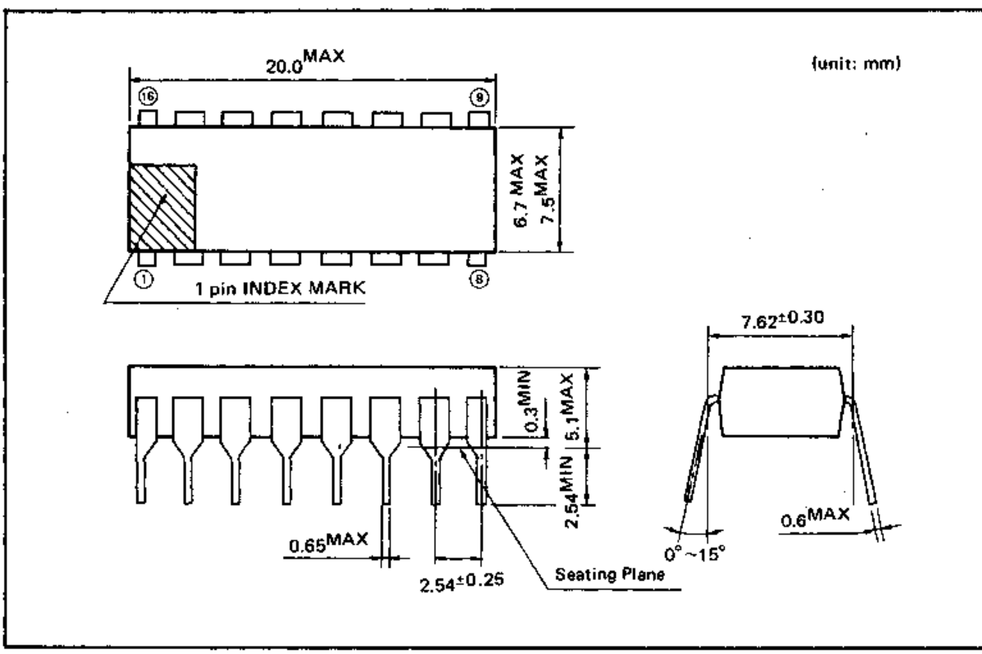
Note: 2. M82C55A-5 has no PLCC Package.
Note: 3. M82C84A-5 has no PLCC Package.

3

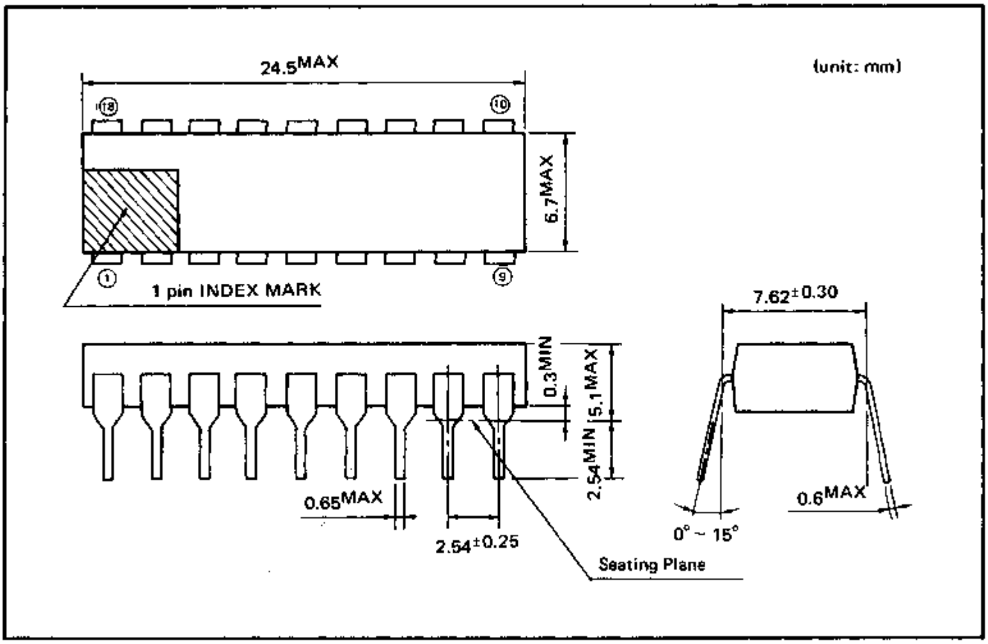
● 20 PIN PLASTIC SKINNY DIP



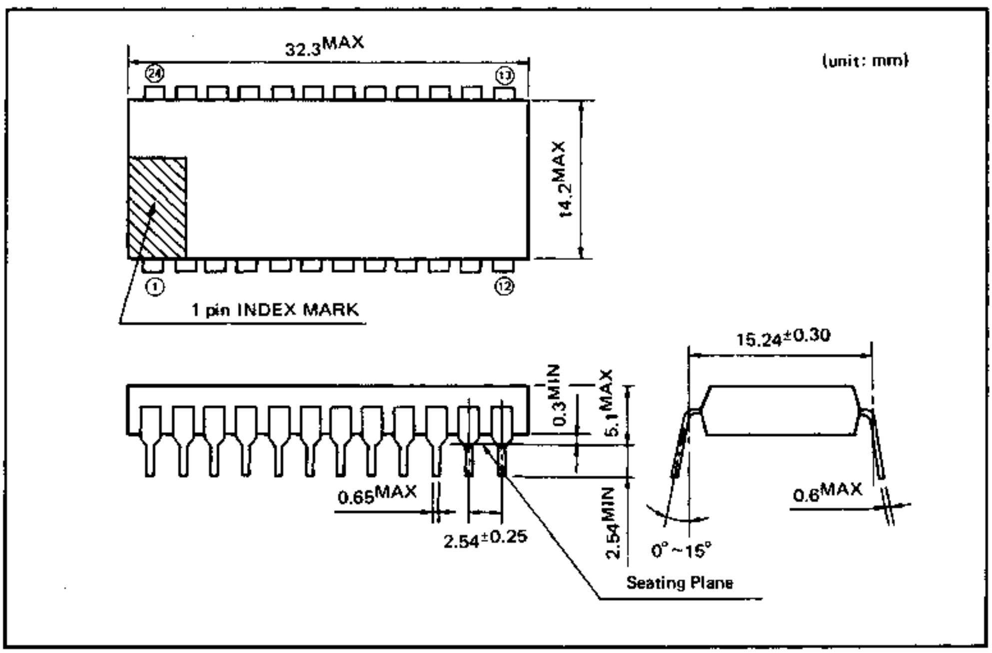
● 16 PIN PLASTIC DIP



● **18 PIN PLASTIC DIP**



● **24 PIN PLASTIC DIP**



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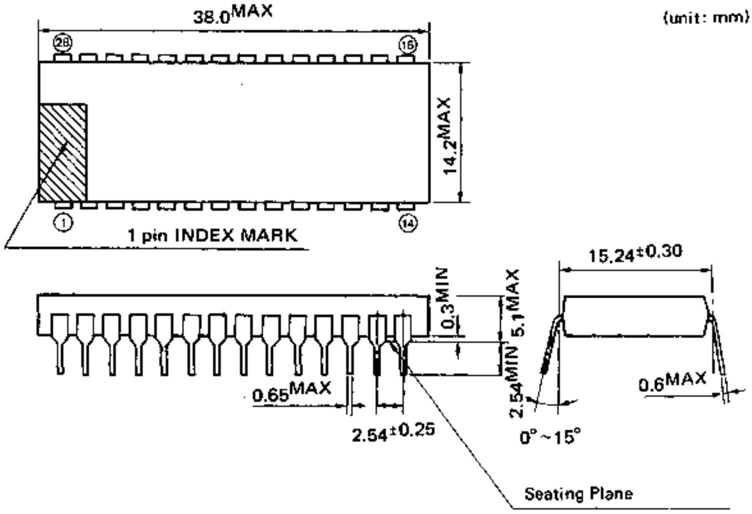
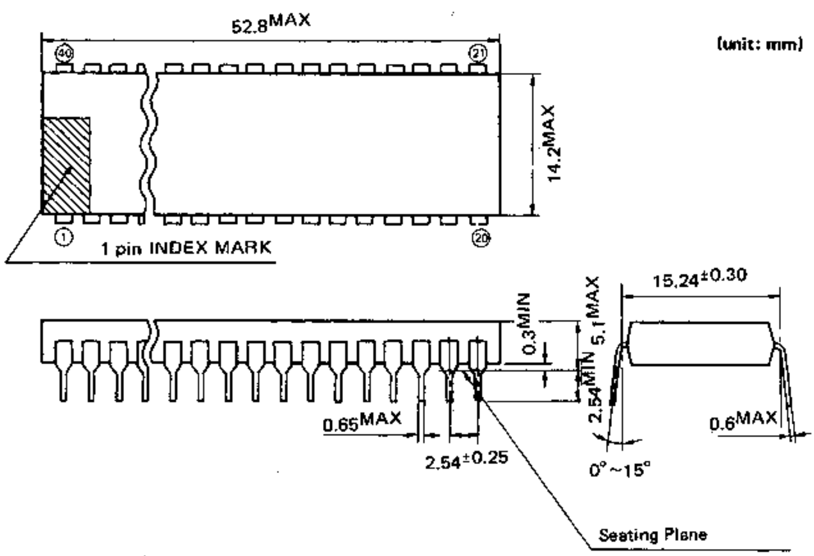
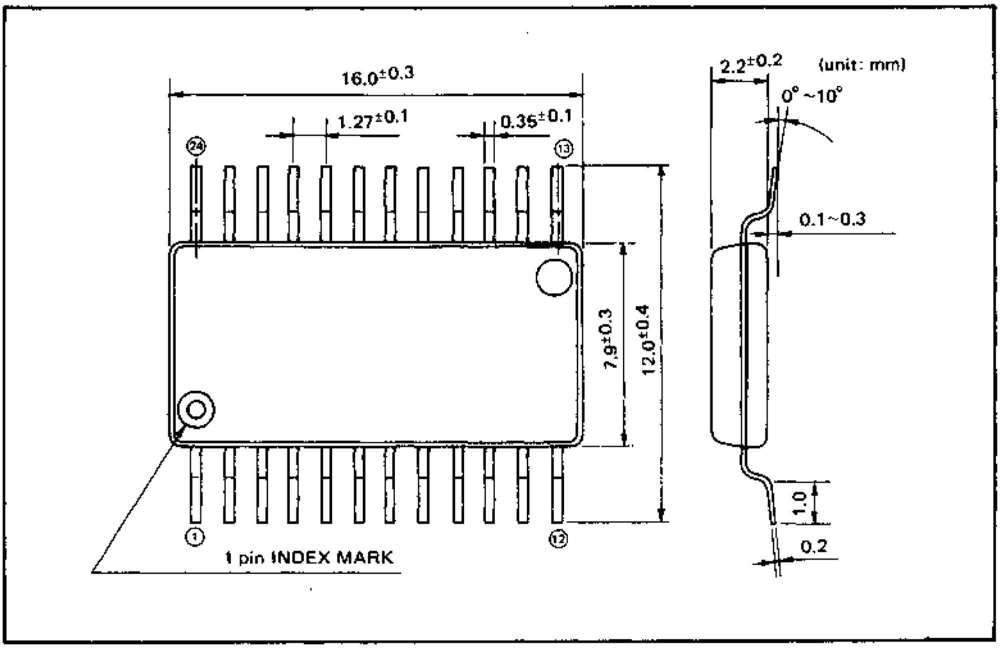
● 28 PIN PLASTIC DIP



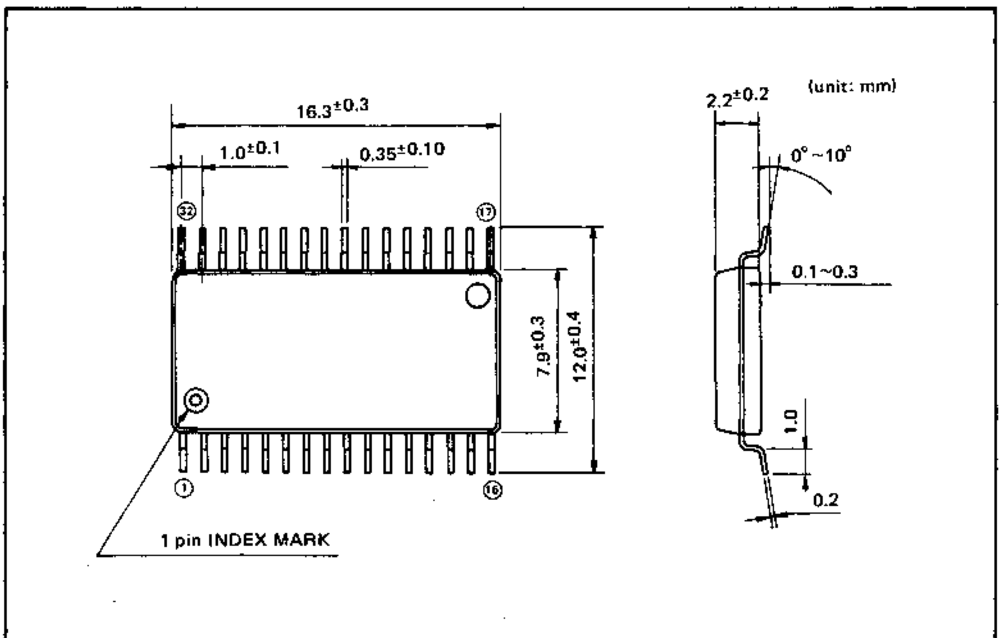
● 40 PIN PLASTIC DIP



● 24 PIN PLASTIC FLAT



● 32 PIN PLASTIC FLAT



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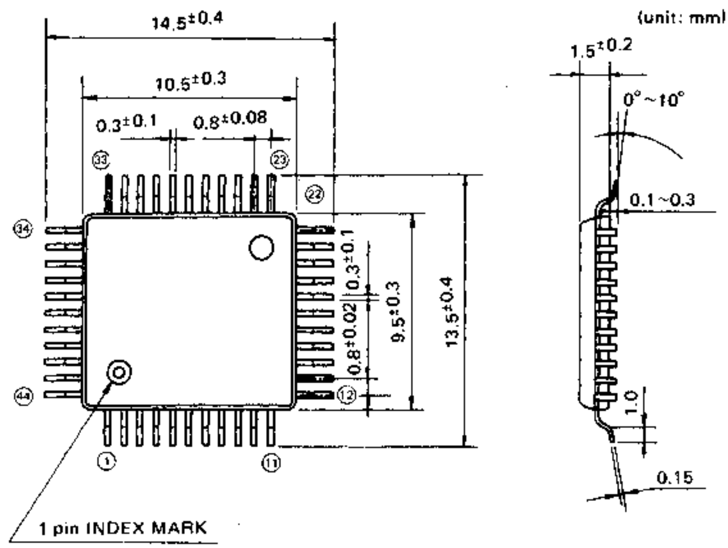
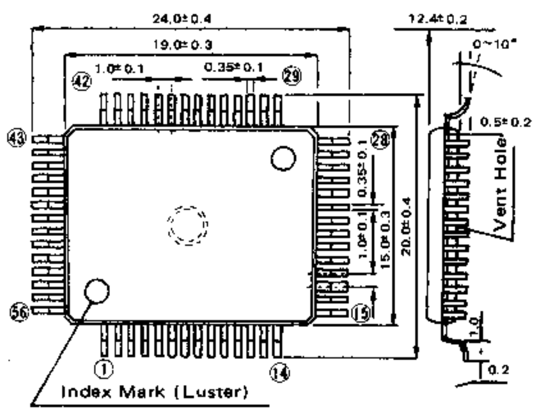
● 44 PIN PLASTIC FLAT

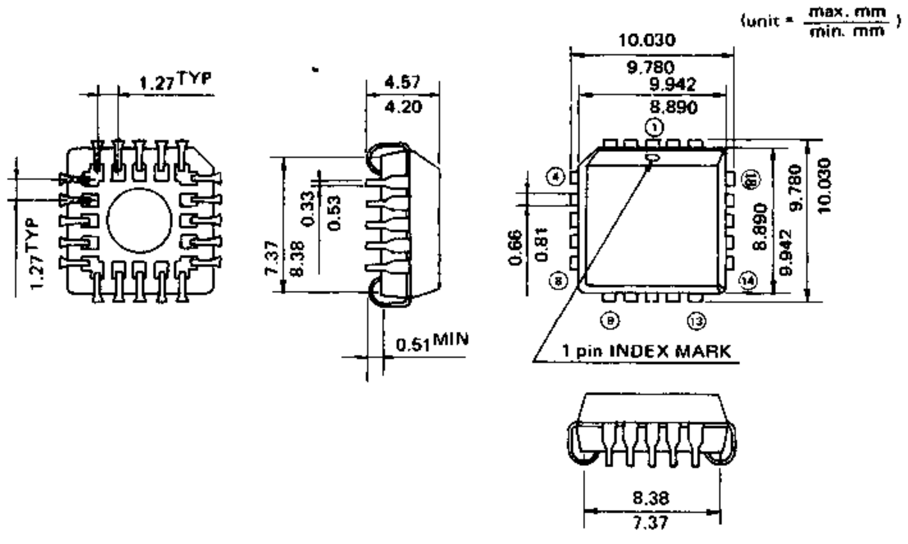


● 56 PIN PLASTIC FLAT



(LARGE TYPE)

● **20 PIN SQUARE PLCC**



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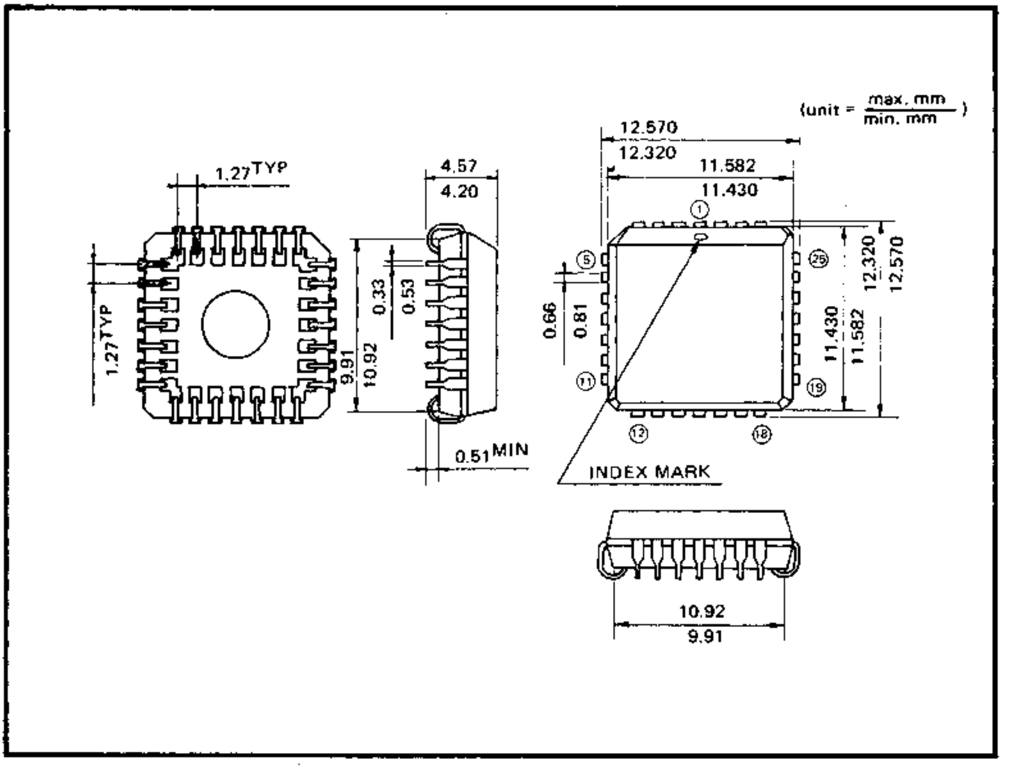
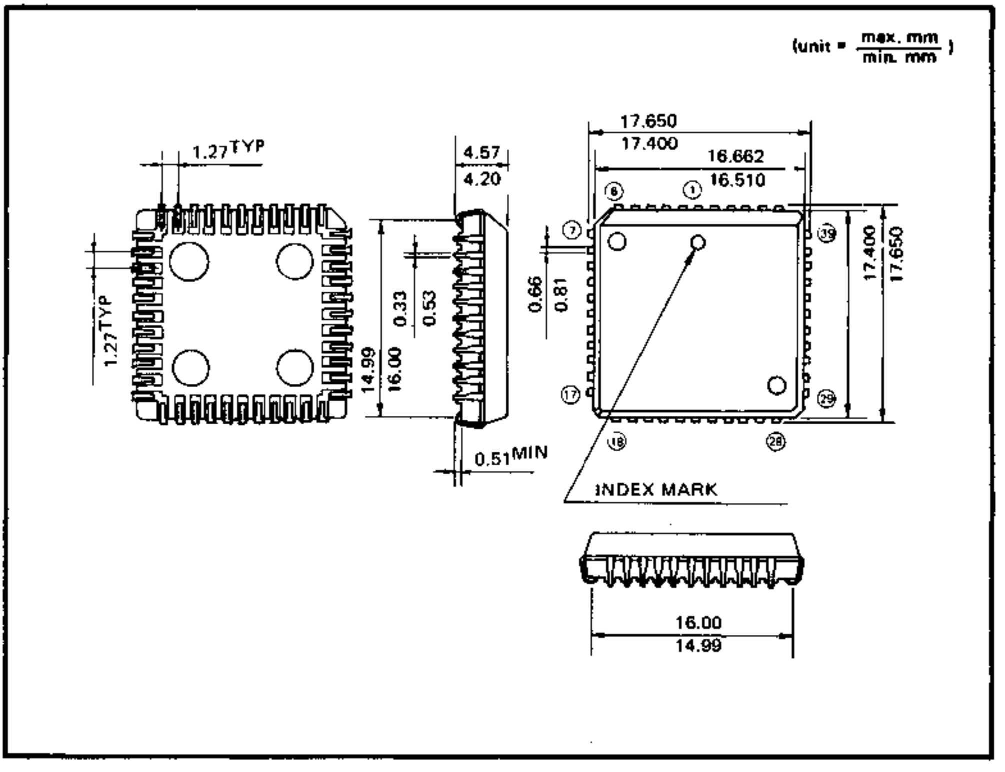
● **28 PIN SQUARE PLCC**



• **44 PIN QUAD PLCC**



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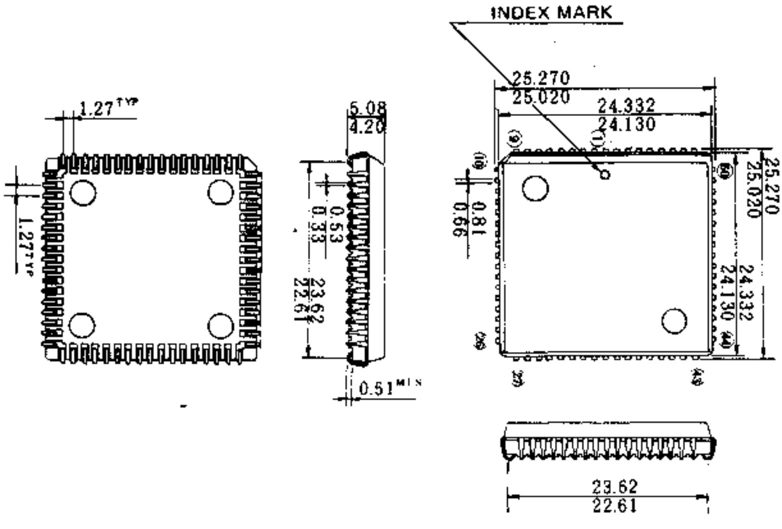
● 68 PIN SQUARE PLCC

(unit = max. mm / min. mm)



RELIABILITY INFORMATION

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RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.
Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection
(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics
(3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

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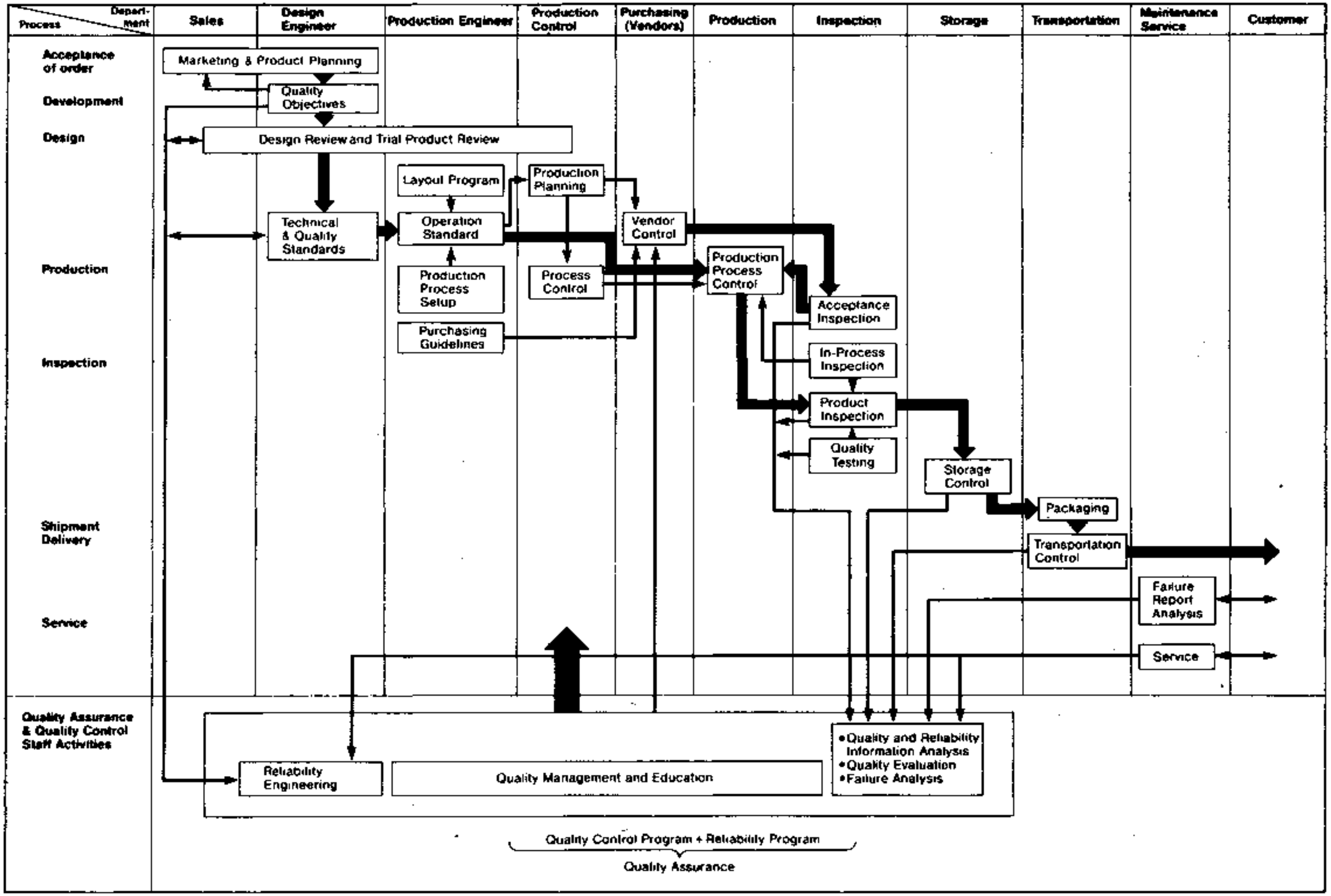

Figure 1 Quality Assurance System

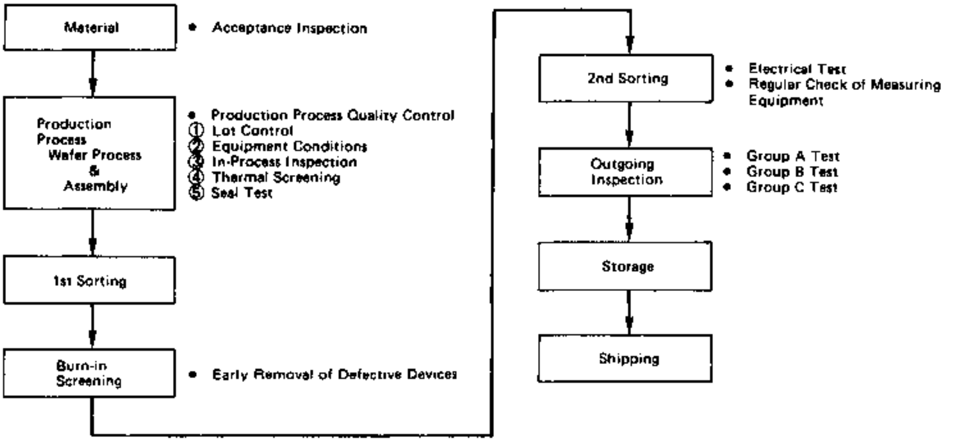

Figure 2 Manufacturing Process

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Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

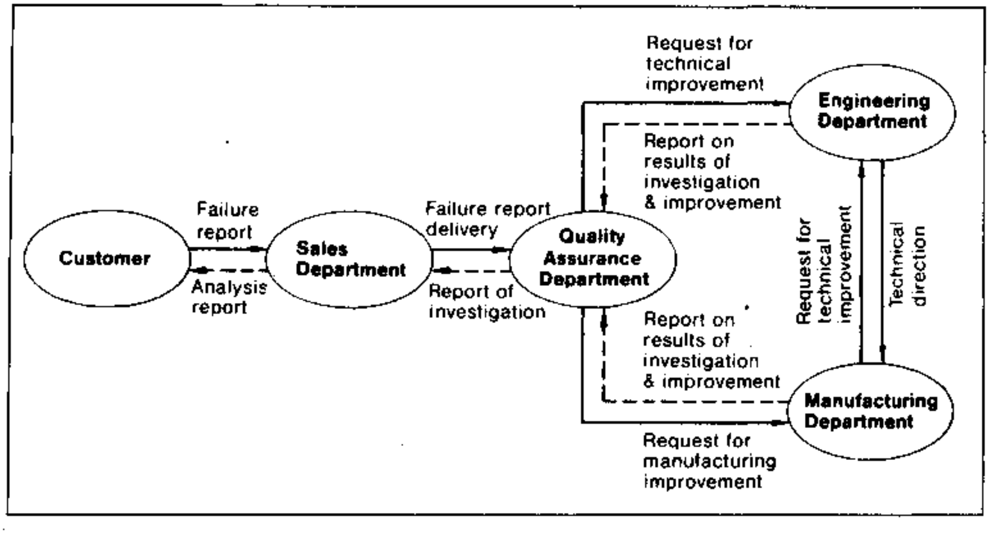
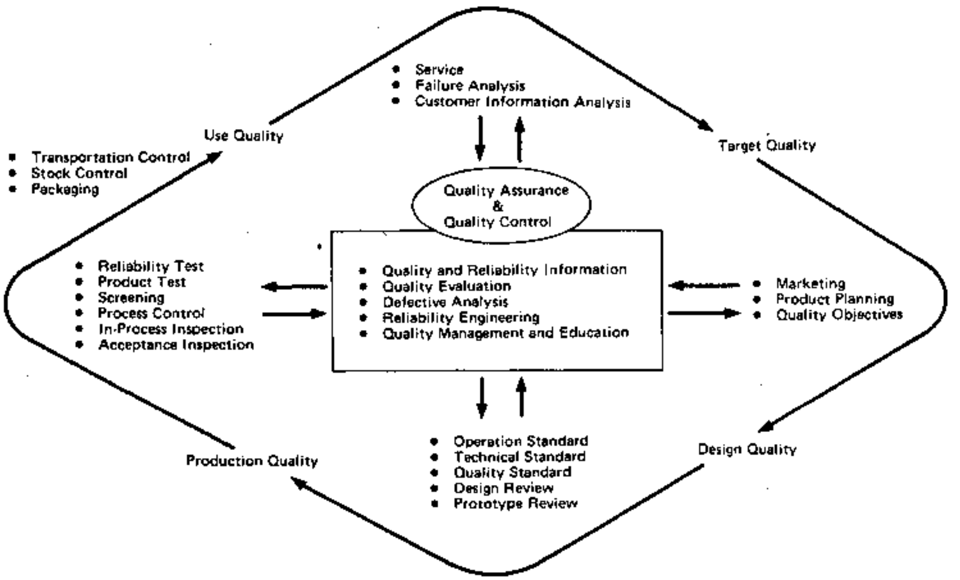


Figure 3 Failure report process



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3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.
By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in LSI elements and their analysis are described on next page.

MICROPROCESSOR LIFE TEST RESULTS

Part name		MSM80C85A-2RS			MSM81C55RS			MSM82C59A-2RS			Referred standard
Function		8 BIT MICROPROCESSOR			2048 BIT CMOS STATIC RAM WITH I/O PORTS & TIMER			PROGRAMMABLE INTERRUPT CONTROLLER			
Test item	Test condition	Sample size (pcs)	Test hours or cycles	Failures	Sample size (pcs)	Test hours & cycles	Failures	Sample size (pcs)	Test hours & cycles	Failures	
Operating life test	Ta = 125°C Vcc = 6V	88	2000 (H)	0	22	2000 (H)	0	88	2000 (H)	0	MIL-STD-883C METHOD 1005
Temperature humidity test	Ta = 85°C RH = 85% Vcc = 6V	100	2000 (H)	0	25	2000 (H)	0	100	2000 (H)	0	
Temperature cycling test	−55°C ⇄ RT ⇄ 150°C (30 min) ↑ (30 min) (5 min)	100	500 (cy)	0	50	300 (cy)	0	100	500 (cy)	0	MIL-STD-883C METHOD 1010
Pressure cooker test	Ta = 121°C RH = 100% 2 atm	50	200 (H)	0	50	200 (H)	0	50	200 (H)	0	

Part name		MSM80C86/88JS			MSM80C86/88AJS			Referred standard
Function		16 BIT MICROPROCESSOR (DYNAMIC VERSION)			16 BIT MICROPROCESSOR (STATIC VERSION)			
Test item	Test condition	Sample size (pcs)	Test hours & cycles	Failures	Sample size (pcs)	Test hours & cycles	Failures	
Operating life test	Ta = 125°C Vcc = 6V	88	2000 (H)	0	88	1000 (H)	0	MIL-STD-883C METHOD 1005
Temperature humidity test	Ta = 85°C RH = 85% Vcc = 6V	100	2000 (H)	0	100	1000 (H)	0	
Temperature cycling test	−55°C ⇄ RT ⇄ 150°C (30 min) ↑ (30 min) (5 min)	100	500 (cy)	0	100	500 (cy)	0	MIL-STD-883C METHOD 1010
Pressure cooker test	Ta = 121°C RH = 100% 2 atm	50	200 (H)	0	50	200 (H)	0	

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MICROPROCESSOR ENVIRONMENTAL TEST RESULTS

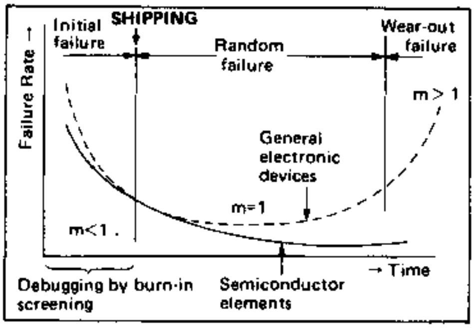
Part name		MSM80C85A-2RS		MSM81C55RS		MSM82C59A-2RS		Referred standard
Function		8 BIT MICROPROCESSOR		2048 BIT CMOS STATIC RAM WITH I/O PORTS & TIMER		PROGRAMMABLE INTERRUPT CONTROLLER		
Test item	Test condition	Sample size (pcs)	Failures	Sample size (pcs)	Failures	Sample size (pcs)	Failures	
PRE-Bake	Bake (125°C, 6 hrs)	22	0	22	0	22	0	—
↓ Soldering Heat Test	260°C 10 SEC	22	0	22	0	22	0	MIL-STD-883C METHOD 2003
↓ Temperature Cycling Test	−55°C⇄RT⇄150°C (30min) (5min) (30min) 20 cycles	22	0	22	0	22	0	MIL-STD-883C METHOD 1010
↓ Thermal Shock Test	100°C⇄0°C (5min) (5min) 10 cycles	22	0	22	0	22	0	MIL-STD-883C METHOD 1011
Lead Integrity: Tensile	500 g 10SEC	11	0	11	0	11	0	MIL-STD883C METHOD 2004
Lead Integrity: Bending	250 g 90° BEND 3 TIMES							
Solderability	230°C 5 SEC	22	0	22	0	22	0	MIL STD883C METHOD 2003

	Part name		MSM80C86/88JS		MSM80C86A/88AJS		Referred standard
	Function		16 BIT MICROPROCESSOR (DYNAMIC VERSION)		16 BIT MICROPROCESSOR (STATIC VERSION)		
	Test item	Test condition	Sample size (pcs)	Failures	Sample size (pcs)	Failures	
Thermal Environmental Test	PRE-Bake	Bake (125°C, 6 hrs)	22	0	22	0	—
	↓ Soldering Heat Test	Vapor Phase Reflow (215±2°C, 90+10, −0sec) 2 times					
	↓ Temperature Cycling Test	−55°C⇄RT⇄150°C (30min) (5min) (30min) 20 cycles					MIL-STD-883C METHOD 1010
	↓ Thermal Shock Test	100°C⇄0°C (5min) (5min) 10 cycles					MIL-STD-883C METHOD 1011
Other Test	Solderability	Bake (125°C, 24hrs) → Immerse into Flux → Immerse into Solder (215±2°C 10±1sec)	22	0	22	0	

4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

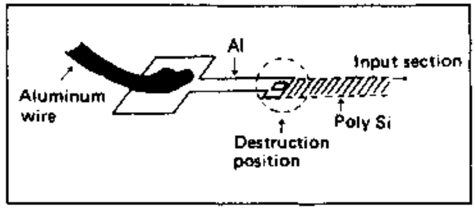
Semiconductor Element Failure Rate Curve



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

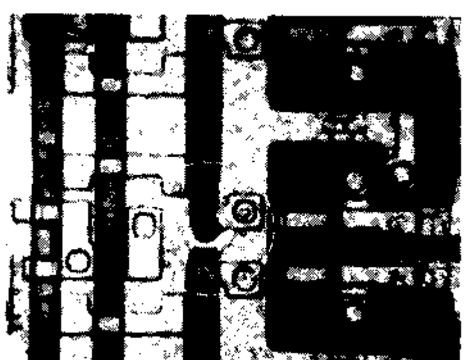
3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 cm through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.

Example of surge destruction



Photolithographic Defect

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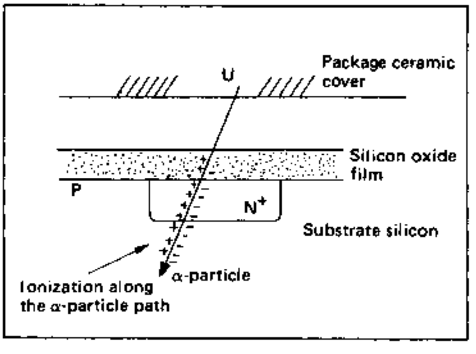
5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

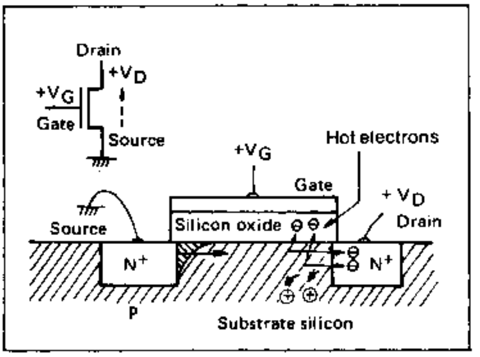
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

DATA SHEETS

CPUs

5

OKI semiconductor

MSM80C85A RS/GS/JS

8-BIT CMOS MICROPROCESSOR

GENERAL DESCRIPTION

The MSM80C85A is a complete 8-bit parallel central processor implemented in silicon gate C-MOS technology.

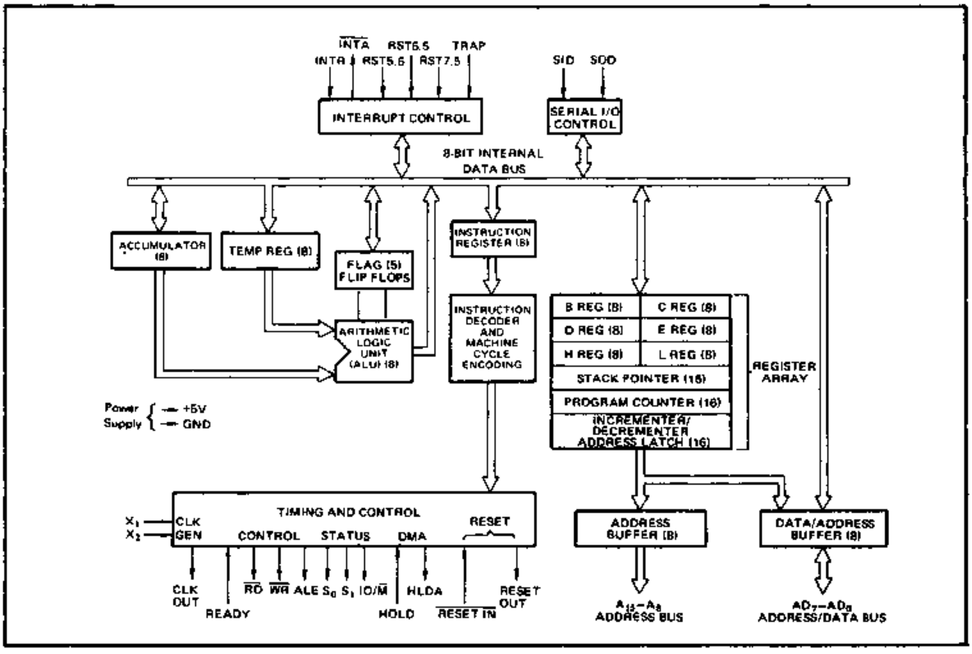
It is designed with the same processing speed and lower power consumption compared with MSM8085A, thereby offering a high level of system integration.

The MSM80C85A uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of MSM81C55/MSM83C55 memory products allow a direct interface with the MSM80C85A.

FEATURES

- Low Power Dissipation: 50 mW Typ
- Single +4 to +6 V Power Supply
- −40 to +85°C, Operating Temperature
- 1.3µ Instruction Cycle
- On-Chip Clock Generator (with External Crystal)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- TTL Compatible
- Four Vectored Interrupt Inputs (One is non-maskable) Plus the 8080A-compatible interrupt.
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Addressing Capability to 64K Bytes of Memory
- 40-pin Plastic DIP (MSM80C85ARS)
- 44-pin Plastic Flat Package (MSM80C85AGS)
- 44-pin PLCC Package (MSM80C85AJS)

FUNCTIONAL BLOCK DIAGRAM



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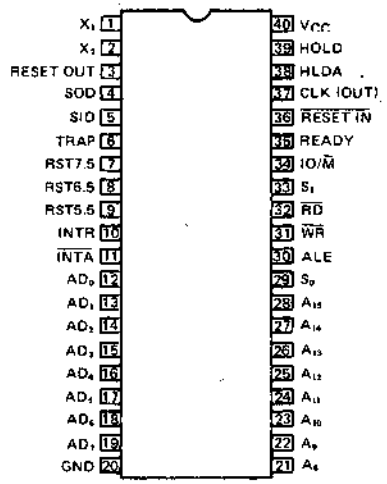
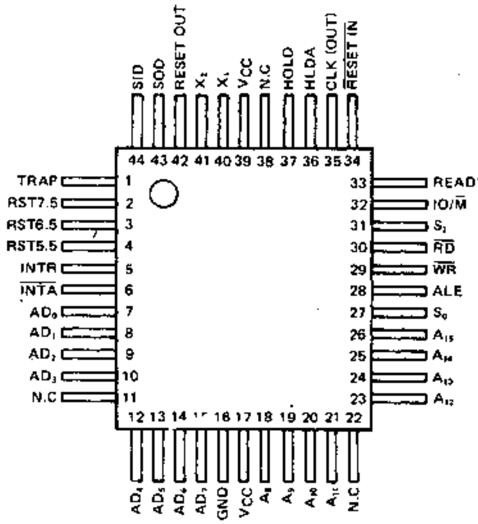
PIN CONFIGURATION

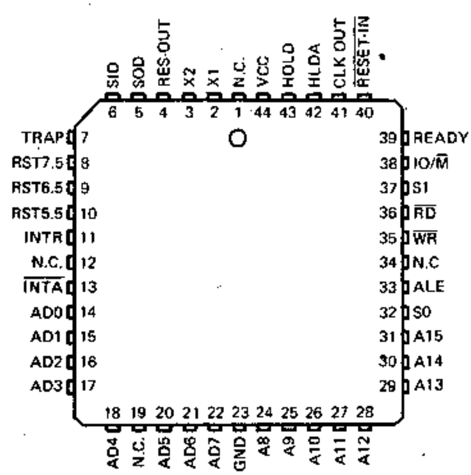
MSM80C85ARS (Top View)
40 Lead Plastic DIP





MSM80C85AGS (Top View)
44 Lead Plastic Flat Package

MSM80C85AJS (Top View)
44 Plastic Leaded Chip Carrier



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MSM80C85A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8-A_{15} (Output, 3-state)	Address Bus: The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_0-AD_7 (Input/Output) 3-state	Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 — States 0 0 1 — Memory write 0 1 0 — Memory read 1 0 1 — I/O write 1 1 0 — I/O read 0 1 1 — Opcode fetch 1 1 1 — Interrupt Acknowledge · 0 0 — Halt · = 3-state · x x — Hold (high impedance) · x x — Reset x = unspecified S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR, 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Input)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5–7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table 1.)

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Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
GND	Ground Reference.

Table 1 Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

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FUNCTIONAL DESCRIPTION

The MSM80C85A is a complete 8-bit parallel central processor. It is designed with silicon gate C-MOS technology and requires a single +5 volt supply. Its basic clock speed is 3MHz, thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (MSM80C85A), a RAM/IO (MSM81C55), and a ROM/IO chip (MSM83C55).

The MSM80C85A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pairs. The MSM-80C85A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-bit x 6 or 16-bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The MSM80C85A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The MSM80C85A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The MSM80C85A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, the MSM80C85A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The MSM80C85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP, INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the MSM80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the MSM80C85A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5–7.5 will provide current interrupt Enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

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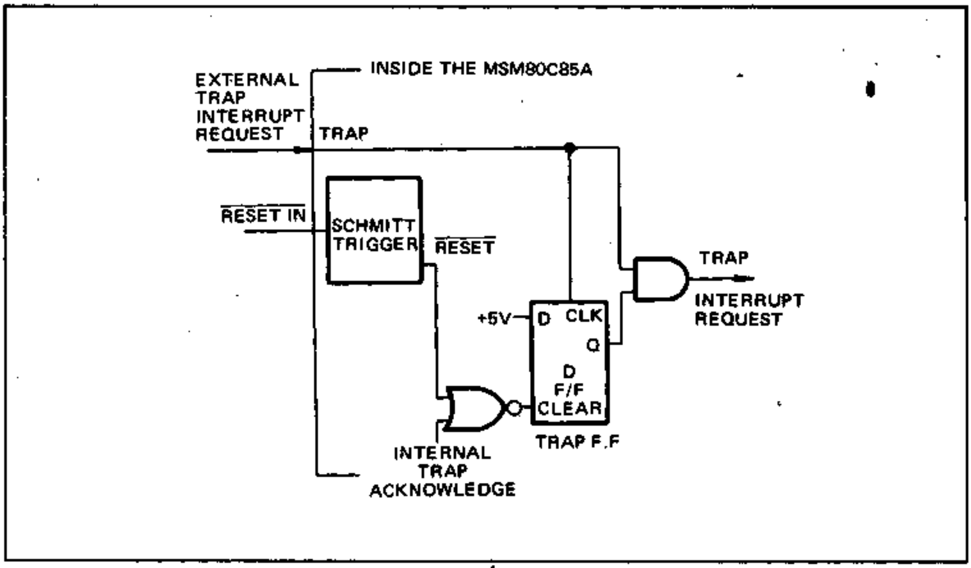

Figure 3 Trap and $\overline{\text{RESET IN}}$ Circuit

DRIVING THE X_1 and X_2 INPUTS

You may drive the clock inputs of the MSM80C85A with a crystal, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the MSM80C85A is operated with a 6 MHz cyrstal (for 3 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

C_L (load capacitance) $\leq$ 30 pF

C_S (shunt capacitance) $\leq$ 7 pF

R_S (equivalent shunt resistance) $\leq$ 75 ohms

Drive level: 10 mW

Frequency tolerance: ±.005% (suggested)

Note the use of the capacitors between X_1, X_2 and ground. These capacitors are required to assure oscillator startup at the correct frequency.

Figure 4 shows the recommended clock driver circuits. Note in B that a pullup resistor is required to assure that the high level voltage of the input is at least 4V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 4B). To prevent self-oscillation of the MSM80C85A, be sure that X_2 is not coupled back to X_1 through the driving circuit.

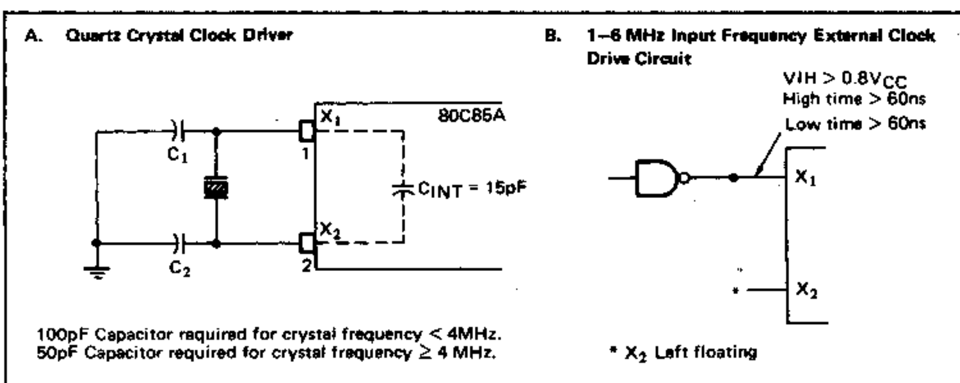

Figure 4 Clock Driver Circuits

BASIC SYSTEM TIMING

The MSM80C85A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 5 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

Table 2 MSM80C85A Machine Cycle Chart

Machine Cycle		Status			Control		
		$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	0	1	1	0	1	1
Memory Read	(MR)	0	1	0	0	1	1
Memory Write	(MW)	0	0	1	1	0	1
I/O Read	(IOR)	1	1	0	0	1	1
I/O Write	(IOW)	1	0	1	1	0	1
Acknowledge of INTR	(INA)	1	1	1	1	1	0
Bus Idle	(BI): DAD	0	1	0	1	1	1
	RST, TRAP						
	HALT	1	1	1	1	1	1
		TS	0	0	TS	TS	1

Table 3 MSM80C85A Machine State Chart

Machine State	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 (1)
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 (2)	X	TS	1	1	0
T_5	1	0 (2)	X	TS	1	1	0
T_6	1	0 (2)	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

Notes: (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) $IO/\overline{M}$ = 1 during $T_4 \sim T_6$ of INA machine cycle.

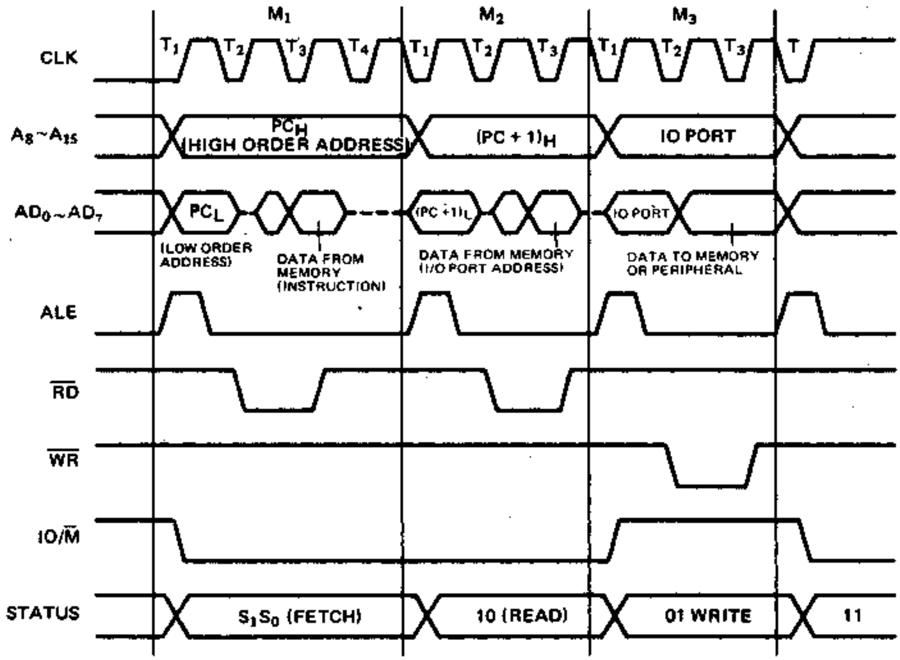

Figure 5· MSM80C85A Basic System Timing

Table 4 Absolute Maximum Ratings

Ambient Temperature under Bias	−40°C to + 85°C
Storage Temperature	−55°C to + 150°C
Supply Voltage Respect to Ground	−0.3V to + 7.0V
Input Voltage Respect to Ground	−0.3V to V_{CC} + 0.3V
Power Dissipation	1.0 Watt (DIP)
	0.7 Watt (FLAT)
	1.0 Watt (PLCC)

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(T_A = −40°C to + 85°C; V_{CC} = 5V ±10%; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	
Input Low Voltage	V_{IL}	−0.3		+0.8	V		
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V		
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2mA	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA	
		4.2			V	I_{OH} = −40μA	
Input Leak	I_{LI}	−10		10	μA	0V ≤ V_{IN} ≤ V_{CC}	
Output Leak	I_{LO}	−10		10	μA	0V ≤ V_{OUT} ≤ V_{CC}	
Input Low Level, RESET	V_{ILR}	−0.3		+0.8	V		
Input High Level, RESET	V_{IHR}	3.0		V_{CC} + 0.3	V		
Hysteresis, RESET	V_{HY}	0.25			V		
Power Supply Current	I_{CC}		10	22	mA	V_{CC} = 4.5V to 5.5V T_A = −40°C to +85°C	t_{CYC} = 320ns Reset Active CL=0pF
			10	17	mA	V_{CC} = 4.75V to 5.25V T_A = 0°C to +85°C	
Power Supply Voltage	V_{CC}	4	5	6	V		

A.C. CHARACTERISTICS

(T_A = −40°C to 85°C; V_{CC} = 5V ±10%)

Parameter	Symbol	80C85A		Units
		Min.	Max.	
CLK Cycle Period	t_{CYC}	320	2000	ns
CLK Low Time	t_1	80		ns
CLK High Time	t_2	120		ns
CLK Rise and Fall Time	t_r, t_f		30	ns
X_1 Rising to CLK Rising	t_{XKR}	30	120	ns
X_1 Rising to CLK Falling	t_{XKF}	30	150	ns
$A_{8\sim15}$ Valid to Leading Edge of Control (1)	t_{AC}	270		ns
$A_{0\sim7}$ Valid to Leading Edge of Control	t_{ACL}	240		ns
$A_{0\sim15}$ Valid to Valid Data In	t_{AD}		575	ns
Address Float After Leading Edge of $\overline{RD}$ ($\overline{INTA}$)	t_{AFR}		0	ns
$A_{8\sim15}$ Valid Before Trailing Edge of ALE(1)	t_{AL}	115		ns
$A_{0\sim7}$ Valid Before Trailing Edge of ALE	t_{ALL}	90		ns
READY Valid from Address Valid	t_{ARY}		220	ns
Address (A_8–A_{15}) Valid After Control	t_{CA}	120		ns
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		ns
Trailing Edge of Control to Leading Edge of ALE	t_{CL}	50		ns
Data Valid to Trailing Edge of $\overline{WR}$	t_{DW}	420		ns
HLDA to Bus Enable	t_{HABE}		210	ns
Bus Float After HLDA	t_{HABF}		210	ns

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A.C. CHARACTERISTICS (cont'd)

Parameter	Symbol	80C85A		Units
		Min.	Max.	
HLDA Valid to Trailing Edge of CLK	t_{HACK}	110		ns
HOLD Hold Time	t_{HDH}	0		ns
HOLD Setup Time to Trailing Edge of CLK	t_{HDS}	170		ns
INTR Hold Time	t_{INH}	0		ns
INTR, RST, and TRAP Setup Time to Falling Edge of CLK	t_{INS}	160		ns
Address Hold Time After ALE	t_{LA}	100		ns
Trailing Edge of ALE to Leading Edge of Control	t_{LC}	130		ns
ALE Low During CLK High	t_{LCK}	100		ns
ALE to Valid Data During Read	t_{LDR}		460	ns
ALE to Valid Data During Write	t_{LDW}		200	ns
ALE Width	t_{LL}	140		ns
ALE to READY Stable	t_{LRY}		110	ns
Trailing Edge of $\overline{RD}$ to Re-Enabling of Address	t_{RAE}	150		ns
$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300	ns
Control Trailing Edge to Leading Edge of Next Control	t_{RV}	400		ns
Data Hold Time After $\overline{RD}$ $\overline{INTA}$ (7)	t_{RDH}	0		ns
READY Hold Time	t_{RYH}	0		ns
READY Setup Time to Leading Edge of CLK	t_{RYS}	110		ns
Data Valid After Trailing Edge of $\overline{WR}$	t_{WD}	100		ns
LEADING Edge of $\overline{WR}$ to Data Valid	t_{WDL}		40	ns

Notes:
(1) A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
(2) Test conditions: t_{CYC} = 320ns C_L = 150pF
(3) For all output timing where C_L = 150pF use the following correction factors:
$25pF \leq C_L < 150pF$: −0.10ns/pF
$150pF < C_L \leq 300pF$: +0.30ns/pF
(4) Output timings are measured with purely capacitive load.
(5) All timings are measured at output voltage V_L = 0.8V, V_H = 2.2V, and 1.5V with 10ns rise and fall time on inputs.
(6) To calculate timing specifications at other values of t_{CYC} use Table 7.
(7) Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

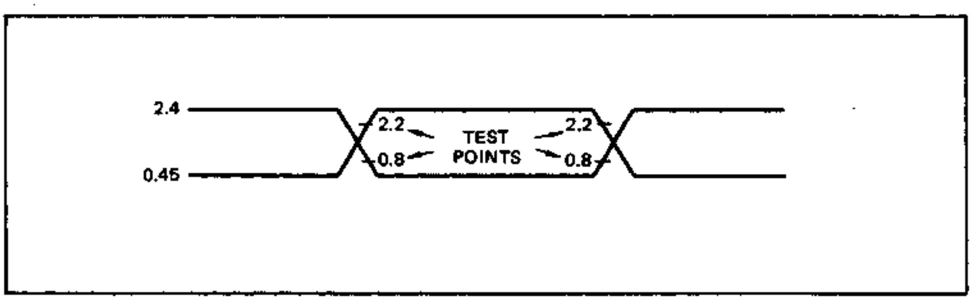


Table 7 Bus Timing Specification as a T_{CYC} Dependent

MSM80C85A			
t_{AL}	–	(1/2)T – 45	MIN
t_{LA}	–	(1/2)T – 60	MIN
t_{LL}	–	(1/2)T – 20	MIN
t_{LCK}	–	(1/2)T – 60	MIN
t_{LC}	–	(1/2)T – 30	MIN
t_{AD}	–	(5/2 + N)T – 225	MAX
t_{RD}	–	(3/2 + N)T – 180	MAX
t_{RAE}	–	(1/2)T – 10	MIN
t_{CA}	–	(1/2)T – 40	MIN
t_{DW}	–	(3/2 + N)T – 60	MIN
t_{WD}	–	(1/2)T – 60	MIN
t_{CC}	–	(3/2 + N)T – 80	MIN
t_{CL}	–	(1/2)T – 110	MIN
t_{ARY}	–	(3/2)T – 260	MAX
t_{HACK}	–	(1/2)T – 50	MIN
t_{HABF}	–	(1/2)T + 50	MAX
t_{HABE}	–	(1/2)T + 50	MAX
t_{AC}	–	(2/2)T – 50	MIN
t_1	–	(1/2)T – 80	MIN
t_2	–	(1/2)T – 40	MIN
t_{RV}	–	(3/2)T – 80	MIN
t_{LDR}	–	(2+N)T – 180	MAX

Note: N is equal to the total WAIT states.
T = t_{CYC}

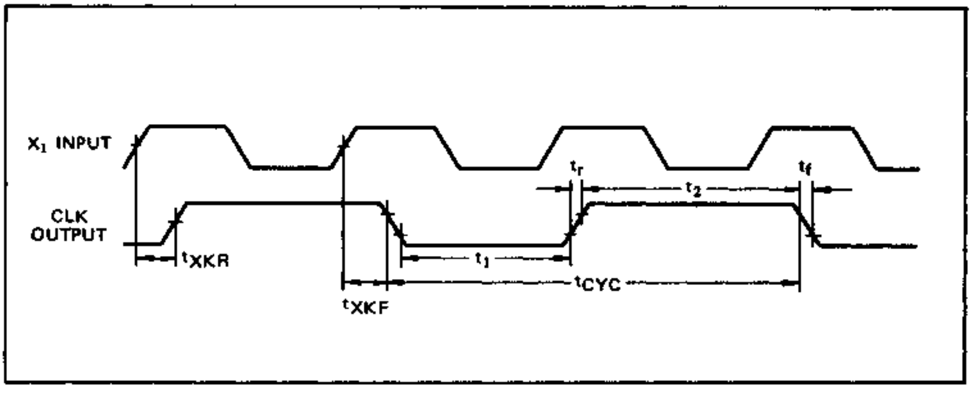
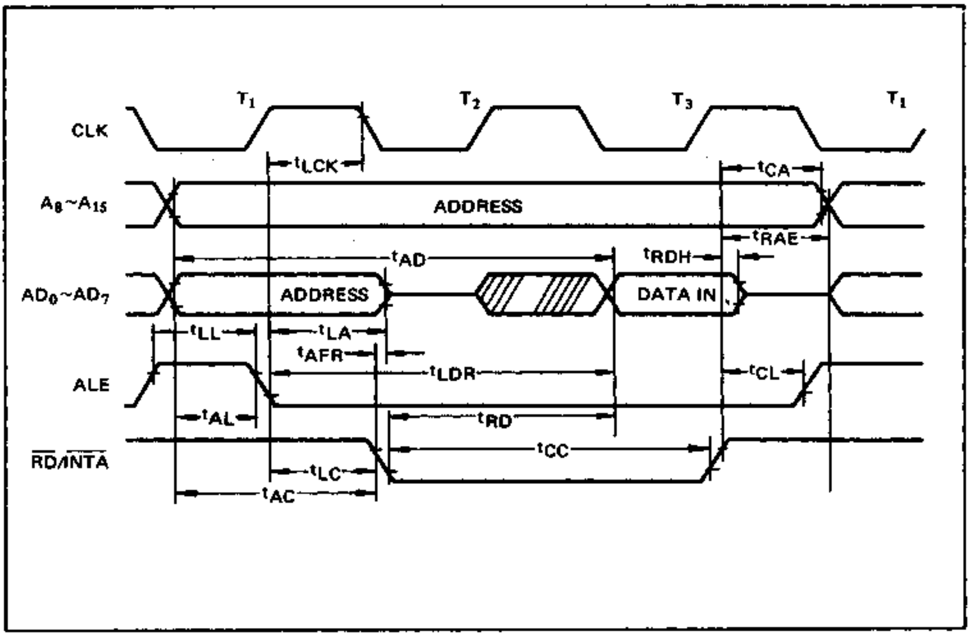


Figure 6 Clock Timing Waveform

READ OPERATION



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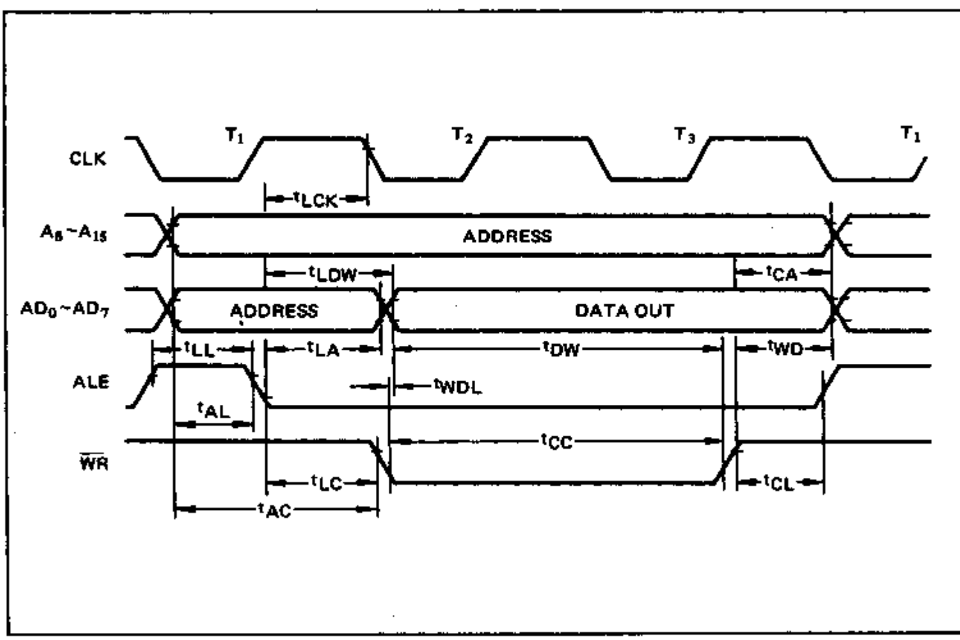
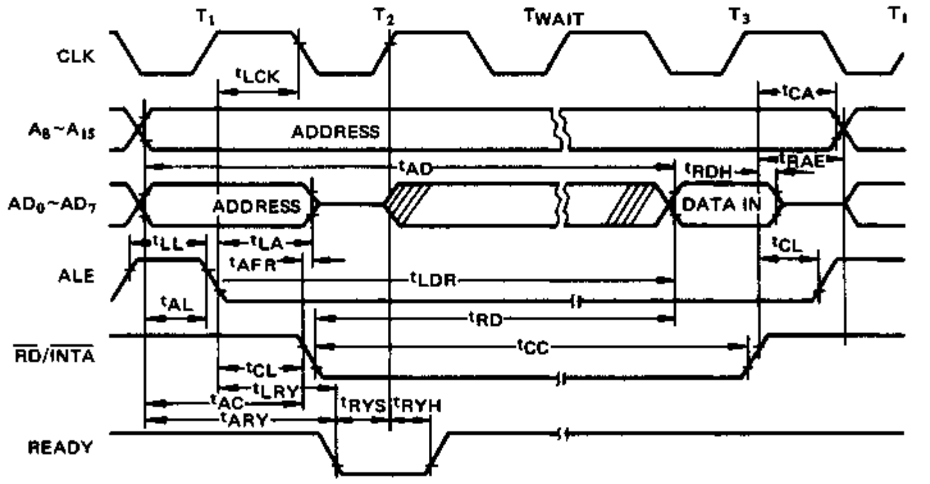
WRITE OPERATION



Read operation with Wait Cycle (Typical)–
same READY timing applies to WRITE operation



Note: READY must remain stable during setup and hold times.

Figure 7 MSM80C85A Bus Timing, With and Without Wait

HOLD OPERATION

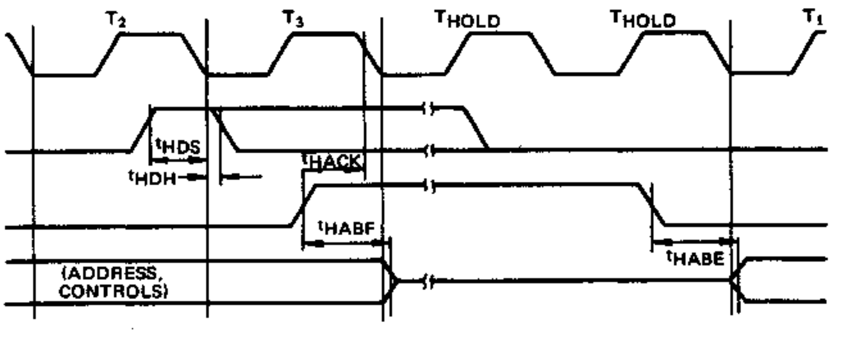


Figure 8 MSM80C85A Hold Timing

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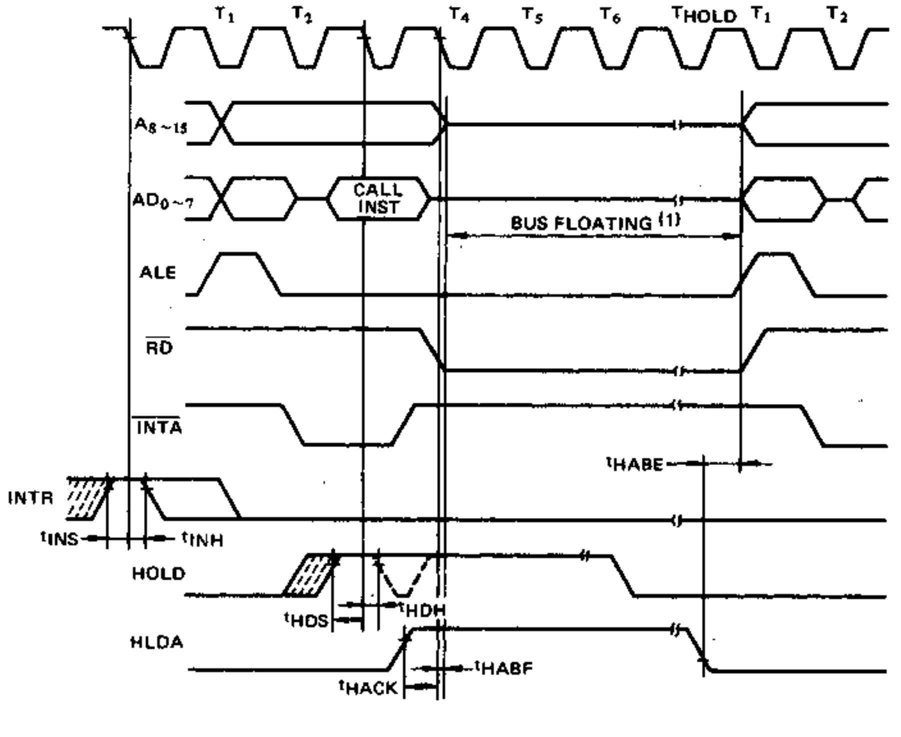

Note: (1) IO/$\overline{M}$ is also floating during this time.

Figure 9 MSM80C85A Interrupt and Hold Timing

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Table 8 Instruction Set Summary

Mnemonic	Description	Instruction Code (1)								Clock (2) Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code(1)								Clock(2) Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code (1)								Clock(2) Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

Notes: (1) DDD or SSS. B 000. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111.
(2) Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

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OKI semiconductor

MSM80C85A-2RS/GS/JS

8-BIT CMOS MICROPROCESSOR

GENERAL DESCRIPTION

The MSM80C85A-2 is a complete 8-bit parallel central processor implemented in silicon gate C-MOS technology and compatible with MSM80C85A.

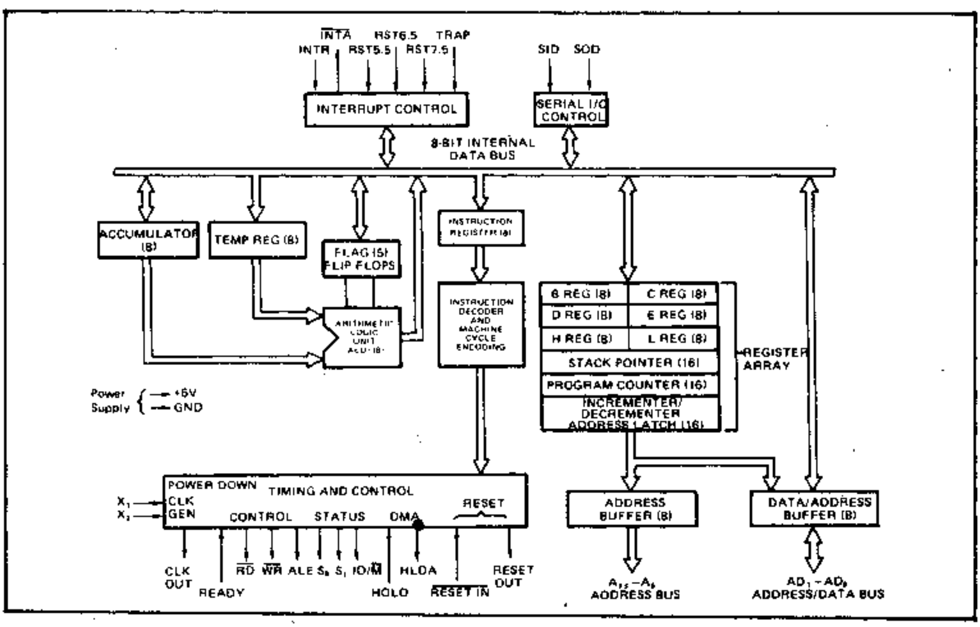
It is designed with higher processing speed (max. 5 MHz) and lower power consumption compared with MSM80C85A and power down mode is provided, thereby offering a high level of system integration.

The MSM80C85A-2 uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latche of a MSM81C55-5 memory product allows a direct interface with the MSM80C85A-2.

FEATURES

- Power down mode (HALT·HOLD)
- Low Power Dissipation: 50mW Typ
- Single +3 to +6 V Power Supply
- −40 to +85°C, Operating Temperature
- Compatible with MSM80C85A
- 0.8μ Instruction Cycle (V_{CC} = 5V)
- On-Chip Clock Generator (with External Crystal)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-maskable) Plus the 8080A-compatible interrupt.
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Addressing Capability to 64K Bytes of Memory
- TTL Compatible
- 40 pin Plastic DIP (MSM80C85A-2RS)
- 44 pin Plastic Flat Package (MSM80C85A-2GS)
- 44 pin PLCC Package (MSM80C85A-2JS)

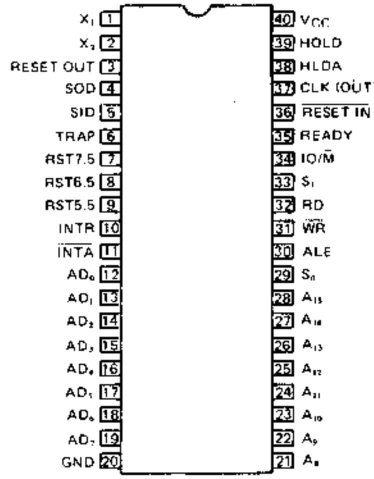
FUNCTIONAL BLOCK DIAGRAM

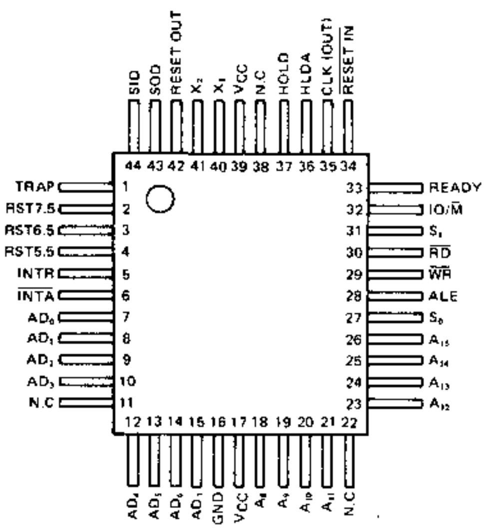


PIN CONFIGURATION

MSM80C85A-2RS (Top View)

40 Lead Plastic DIP



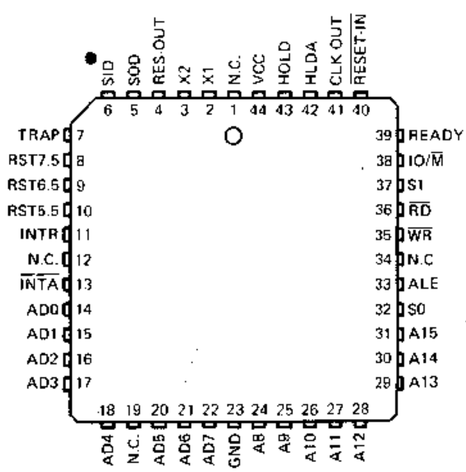


MSM80C85A-2GS (Top View)

44 Lead Plastic Flat Package

MSM80C85A-2JS (Top View)

44 Plastic Leaded Chip Carrier



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MSM80C85A-2 FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8-A_{15} (Output, 3-state)	Address Bus: The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_0-AD_7 (Input/Output) 3-state	Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information ALE is never 3-stated.
S_0, S_1, IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 — States 0 0 1 — Memory write 0 1 0 — Memory read 1 0 1 — I/O write 1 1 0 — I/O read 0 1 1 — Opcode fetch 1 1 1 — Interrupt Acknowledge . 0 0 — Halt = 3-state . x x — Hold (high impedance) . x x — Reset x = unspecified S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$, 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle READY must conform to specified setup and hold times.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated. And status of power down is controlled by HOLD.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled on during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted. Power down mode is reset by INTR.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Input)	RESTART INTERRUPTS. These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction. Power down mode is reset by these interrupts.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5—7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table 1.) Power down mode is reset by input of TRAP.

Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops and release power down mode. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of $\overline{\text{RESET}}$, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicated cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
GND	Ground Reference.

Table 1 Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

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FUNCTIONAL DESCRIPTION

The MSM80C85A-2 is a complete 8-bit parallel central processor. It is designed with silicon gate C-MOS technology and requires a single +5 volt supply. Its basic clock speed is 5MHz, thus improving on the present MSM80C85A's performance with higher system speed and power down mode. Also it is designed to fit into a minimum system of three IC's: The cpu (MSM80C85A-2), and a RAM/IO (MSM81C55-5)

The MSM80C85A-2 has twelve addressable 8-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pairs. The MSM-80C85A-2 register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-bit x 6 or 16-bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The MSM80C85A-2 uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The MSM80C85A-2 provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The MSM80C85A-2 also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, the MSM80C85A-2 has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt and power down mode with HALT and HOLD.

INTERRUPT AND SERIAL I/O

The MSM80C85A-2 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the MSM80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a flixed priority that determines which interrupt is to be recognized if more than one is pending, as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the MSM80C85A-2. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

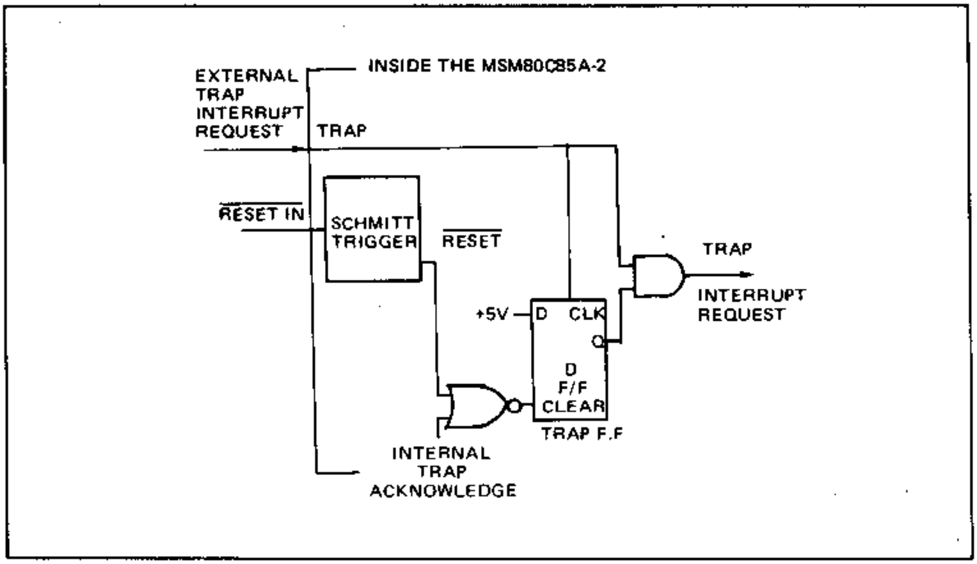

Figure 3 Trap and RESET IN Circuit

DRIVING THE X_1 and X_2 INPUTS

You may drive the clock inputs of the MSM80C85A-2 with a crystal, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the MSM80C85A-2 is operated with a 6 MHz crystal (for 3 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

C_L (load capacitance) ≤ 30 pF

C_S (shunt capacitance) ≤ 7 pF

R_S (equivalent shunt resistance) ≤ 75 ohms

Drive level: 10 mW

Frequency tolerance: ±.005% (suggested)

Note the use of the capacitors between X_1, X_2 and ground. These capacitors are required to assure oscillator startup at the correct frequency.

Figure 4 shows the recommended clock driver circuits. Note in B that a pullup resistor is required to assure that the high level voltage of the input is at least 4V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 4B). To prevent self-oscillation of the MSM80C85A-2, be sure that X_2 is not coupled back to X_1 through the driving circuit.

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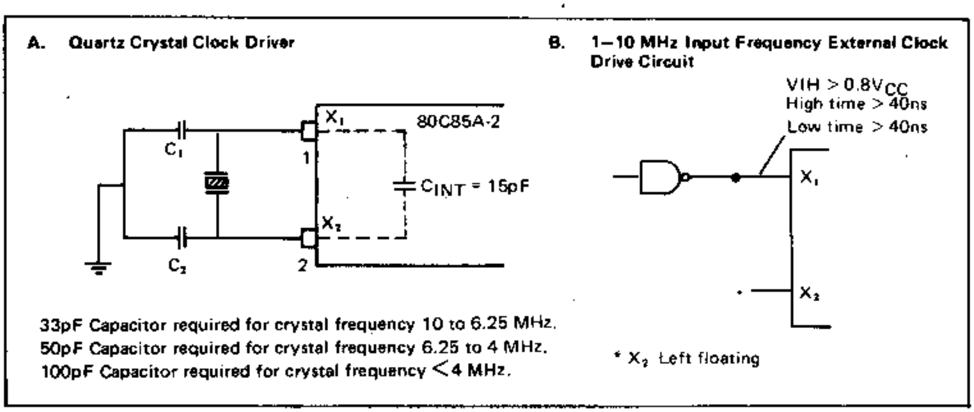

Figure 4 Clock Driver Circuits

BASIC SYSTEM TIMING

The MSM80C85A-2 has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 5 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

Table 2 MSM80C85A-2 Machine Cycle Chart

Machine Cycle		Status			Control		
		IO/$\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	0	1	1	0	1	1
Memory Read	(MR)	0	1	0	0	1	1
Memory Write	(MW)	0	0	1	1	0	1
I/O Read	(IOR)	1	1	0	0	1	1
I/O Write	(IOW)	1	0	1	1	0	1
Acknowledge of INTR	(INA)	1	1	1	1	1	0
Bus Idle	(BI): DAD ACK. OF RST, TRAP	0	1	0	1	1	1
	RST, TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

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Table 3 MSM80C85A-2 Machine State Chart

Machine State	Status & Buses				Control		
	S_1,S_0	IO/$\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1(1)
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 (2)	X	TS	1	1	0
T_5	1	0 (2)	X	TS	1	1	0
T_6	1	0 (2)	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS= High Impedance
X = Unspecified

Notes: (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) IO/$\overline{M}$ = 1 during $T_4 \sim T_6$ of INA machine cycle.

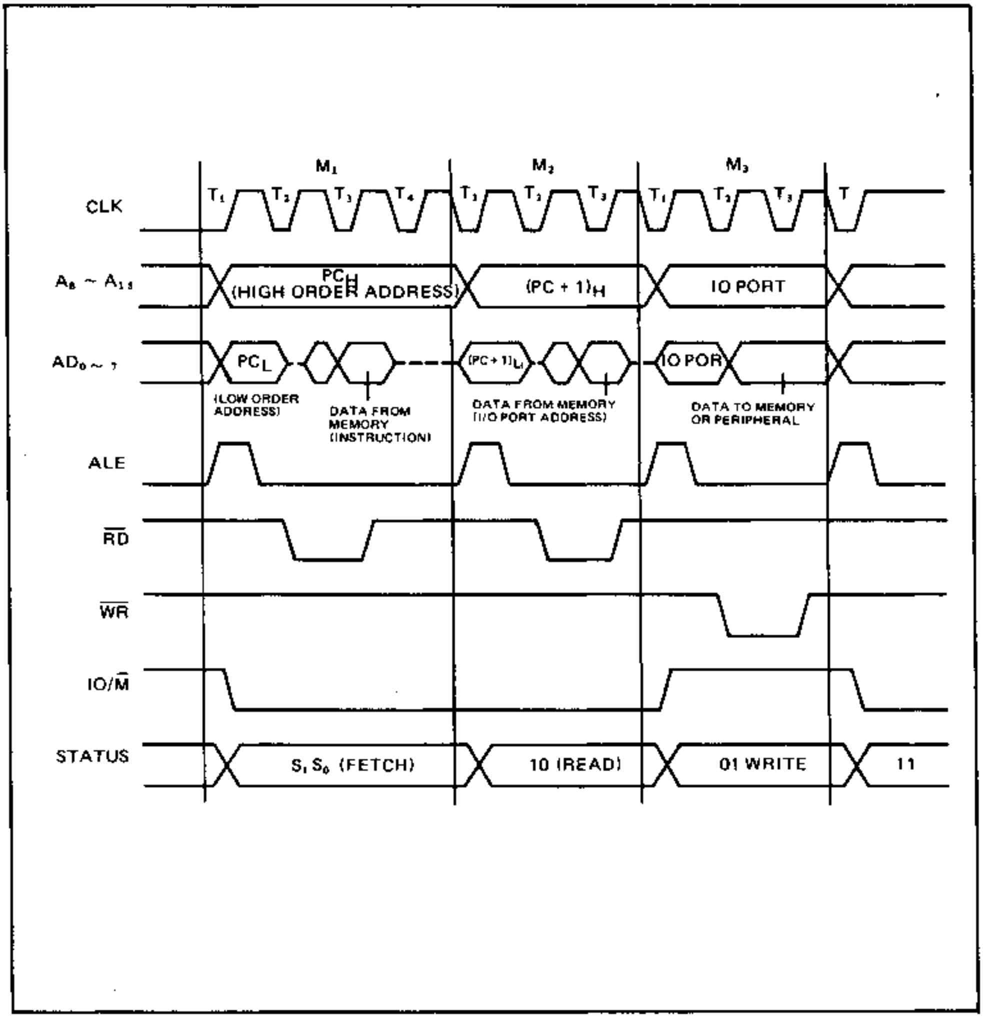

Figure 5. MSM80C85A-2 Basic System Timing

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POWER DOWN Mode (a newly added function)

The MSM80C85A-2 is compatible with the MSM80C85A in function and POWER DOWN mode. This reduces power consumption further.

There are two methods available for starting this POWER DOWN mode. One is through software control by using the HALT command and the other is under hardware control by using the pin HOLD. This mode is released by the HOLD, RESET, and interrupt pins (TRAP, RST7.5, RST6.5, RST5.5, or INTR). (See Table 4.)

Since the sequence of HALT, HOLD, RESET, and INTERRUPT is compatible with MSM80C85A, every the POWER DOWN mode can be used with no special attention.

Table 4 POWER DOWN Mode Releasing Method

Start by means of HALT command	Released by using pins RESET and INTERRUPT (not by pin HOLD)
Start by means of HOLD pin	Released by using RESET and HOLD pins (not by interrupt pins)

(1) Start by means of HALT command
(See Figures 6 and 7.)
The POWER DOWN mode can be started by executing the HALT command.
At this time, the system is put into the HOLD status and therefore the POWER DOWN mode cannot be released even when the HOLD is released later.
In this case, the POWER DOWN mode can be released by means of the RESET or interrupt.

(2) Start by means of HOLD pin (See Figure 8.)
During the execution of commands other than the HALT, the POWER DOWN mode is started when the system is put into HOLD status by means of the HOLD pin.
Since no interrupt works during the execution of the HOLD, the POWER DOWN mode cannot be released by means of interrupt pins.
In this case, the POWER DOWN mode can be released either by means of the RESET pin or by releasing the HOLD status by means of HOLD pin.

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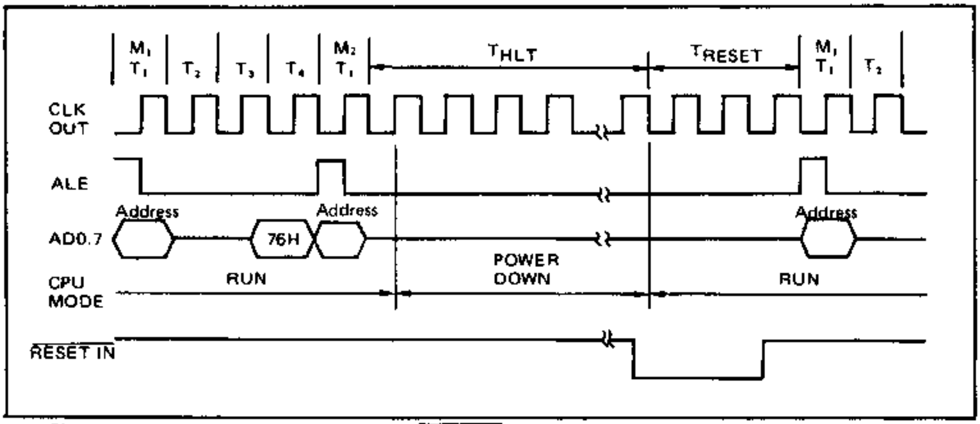

Figure 6. Started by HALT and Released by $\overline{\text{RESET IN}}$

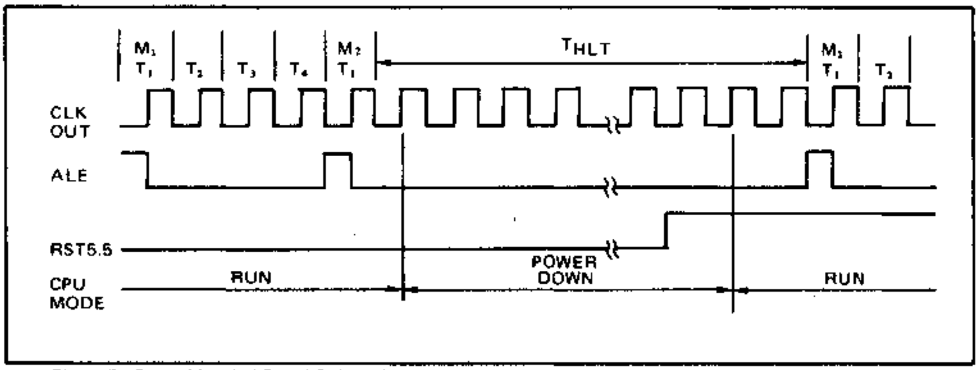

Figure 7. Started by HALT and Released by RST5.5

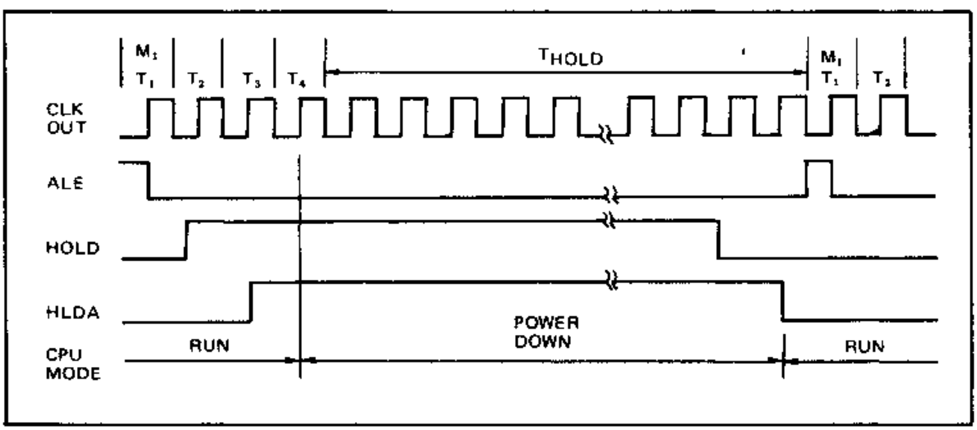

Figure 8. Started and Released by HOLD

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits			Unit
			MSM80C85A-2RS	MSM80C85A-2GS	MSM80C85A-2JS	
Power Supply Voltage	V_{CC}	With respect to GND	$-0.5 \sim +7$			V
Input Voltage	V_{IN}	With respect to GND	$-0.5 \sim V_{CC} +0.5$			V
Output Voltage	V_{OUT}	With respect to GND	$-0.5 \sim V_{CC} +0.5$			V
Storage Temperature	Tstg		$-55 \sim +150$			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	$3 \sim 6$	V
Operating Temperature	Top	$-40 \sim +85$	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Output Voltage	V_{IH}	2.2		V_{CC} + 0.3	V
"L" RESET IN Input Voltage	V_{ILR}	−0.3		+0.8	V
"H" RESET IN Input Voltage	V_{IHR}	3.0		V_{CC} + 0.3	V

D.C. CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 2mA				0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −400μA	V_{CC} = 4.5V ~ 5.5V Ta = −40°C ~ +85°C	2.4			V
		I_{OH} = −40μA		4.2			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Operating Supply Current	I_{CC}	Tcyc = 200ns C_L = 0pF at reset			10	20	mA
		Tcyc = 200ns C_L = 0pF at power down mode			3	7	mA

A.C. CHARACTERISTICS

($Ta = -40°C \sim 85°C$, $V_{CC} = 4.5V \sim 5.5V$)

Parameter	Symbol	Condition	Min.	Max.	Unit
CLK Cycle Period	t_{CYC}	—	200	2000	ns
CLK Low Time	t_1		40		ns
CLK High Time	t_2		70		ns
CLK Rise and Fall Time	t_r, t_f			30	ns
X_1 Rising to CLK Rising	t_{XKR}		25	120	ns
X_1 Rising to CKK Falling	t_{XKF}		30	150	ns
$A_8 \sim_{15}$ Valid to Leading Edge of Control (1)	t_{AC}		115		ns
$A_0 \sim_7$ Valid to Leading Edge of Control	t_{ACL}		115		ns
$A_8 \sim_{15}$ Valid Data In	t_{AD}			330	ns
Address Float After Leading Edge of RD INTA	t_{AFR}			0	ns
$A_8 \sim_{15}$ Valid Before Trailing Edge of ALE (1)	t_{AL}		50		ns
$A_0 \sim_7$ Valid Before Trailing Edge of ALE	t_{ALL}		50		ns
READY Valid from Address Valid	t_{ARY}			100	ns
Address ($A_8 \sim_{15}$) Valid After Control	t_{CA}		60		ns
Width of Control Law (RD, WR, INTA)	t_{CC}		230		ns
Trailing Edge of Control to Leading Edge of ALE	t_{CL}		25		ns
Data Valid to Trailing Edge of WR	t_{DW}		230		ns
HLDA to Bus Enable	t_{HABE}			150	ns
Bus Float After HLDA	t_{HABF}	t_{CYC} = 200ns C_L = 150pF		150	ns
HLDA Valid to Trailing Edge of CLK	t_{HACK}		40		ns
HOLD Hold Time	t_{HDH}		0		ns
HOLD Step Up Time to Trailing Edge of CLK	t_{HDS}		120		ns
INTR Hold Time	t_{INH}		0		ns
INTR, RST and TRAP Setup Time to Falling Edge of CLK	t_{INS}		150		ns
Address Hold Time After ALE	t_{LA}		50		ns
Trailing Edge of ALE to Leading Edge of Control	t_{LC}		60		ns
ALE Low During CLK High	t_{LCK}		50		ns
ALE to Valid Data During Read	t_{LDR}			250	ns
ALE to Valid Data During Write	t_{LDW}			140	ns
ALE Width	t_{LL}		80		ns
ALE to READY Stable	t_{LRY}			30	ns
Trailing Edge of RD to Re-enabling of Address	t_{RAE}		90		ns
RD (or INTA) to Valid Data	t_{RD}			150	ns
Control Trailing Edge to Leading Edge of Next Control	t_{RV}		220		ns
Data Hold Time After RD INTA (7)	t_{RDH}		0		ns
READY Hold Time	t_{RYH}		0		ns
READY Setup Time to Leading Edge of CLK	t_{RYS}		100		ns
Data Valid After Trailing Edge of WR	t_{WD}		60		ns
LEADING Edge of WR to Data Valid	t_{WDL}			20	ns

Notes: (1) $A_8 \sim A_{15}$ address Specs apply to IO/M, S_0, and S_1 except $A_8 \sim A_{15}$ are undefined during $T_4 \sim T_6$ of OF cycle whereas IO/M, S_0, and S_1 are stable.
(2) Test conditions: t_{CYC} = 200ns C_L = 150pF
(3) For all output timing where C_L = 150pF use the following correction factors:
25pF $\le C_L <$ 150pF: −0.10ns/pF
150pF $< C_L \le$ 300pF: +0.30ns/pF
(4) Output timings are measured with purely capacitive load.
(5) All timings are measured at output voltage V_L = 0.8V, V_H = 2.2V, and 1.5V with 10ns rise and fall time on inputs.
(6) To calculate timing specifications at other values of t_{CYC} use Table 7.
(7) Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

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Table 7 Bus Timing Specification as a T_{CYC} Dependent

($Ta = -40°C \sim +85°C$, $V_{CC} = 4.5V \sim 5.5V$, $C_L = 150pF$)

	MSM80C85A-2		
t_{AL}	–	(1/2)T – 50	MIN
t_{LA}	–	(1/2)T – 50	MIN
t_{LL}	–	(1/2)T – 20	MIN
t_{LCK}	–	(1/2)T – 50	MIN
t_{LC}	–	(1/2)T – 40	MIN
t_{AD}	–	(5/2 + N)T – 170	MAX
t_{RD}	–	(3/2 + N)T – 150	MAX
t_{RAE}	–	(1/2)T – 10	MIN
t_{CA}	–	(1/2)T – 40	MIN
t_{DW}	–	(3/2 + N)T – 70	MIN
t_{WD}	–	(1/2)T – 40	MIN
t_{CC}	–	(3/2 + N)T – 70	MIN
t_{CL}	–	(1/2)T – 75	MIN
t_{ARY}	–	(3/2)T – 200	MAX
t_{HACK}	–	(1/2)T – 60	MIN
t_{HABF}	–	(1/2)T + 50	MAX
t_{HABE}	–	(1/2)T + 50	MAX
t_{AC}	–	(2/2)T – 85	MIN
t_1	–	(1/2)T – 60	MIN
t_2	–	(1/2)T – 30	MIN
t_{RV}	–	(3/2)T – 80	MIN
t_{LDR}	–	(2+N)T – 150	MAX

Note: N is equal to the total WAIT states.
$T = t_{CYC}$

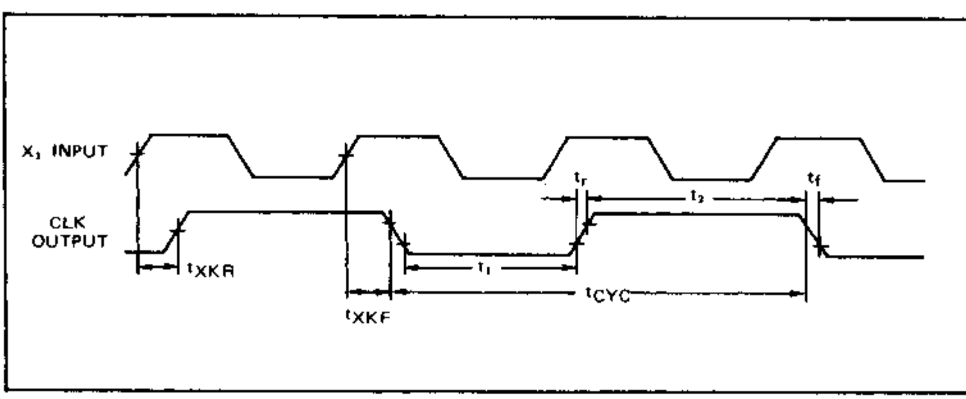
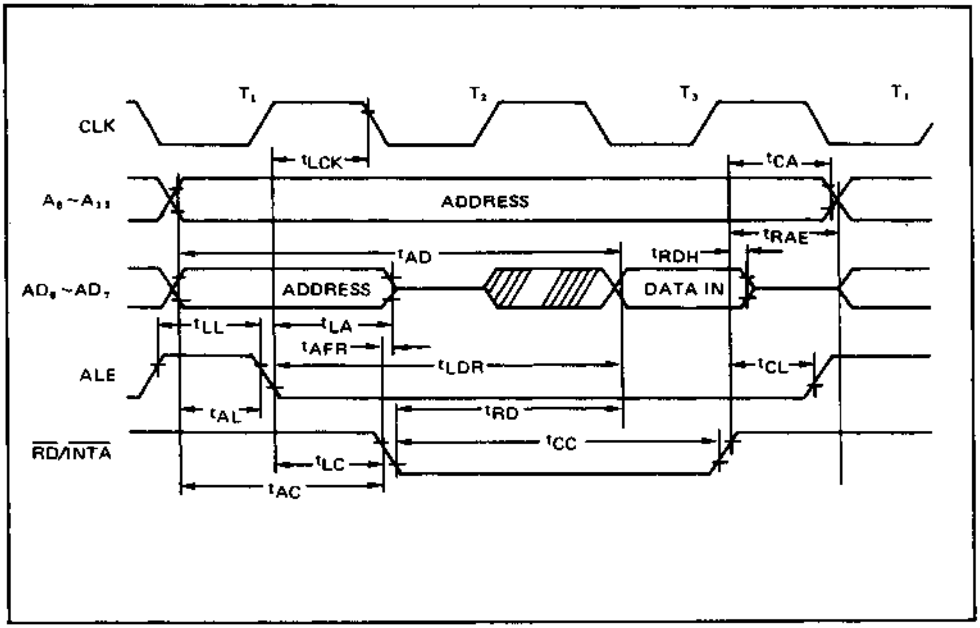
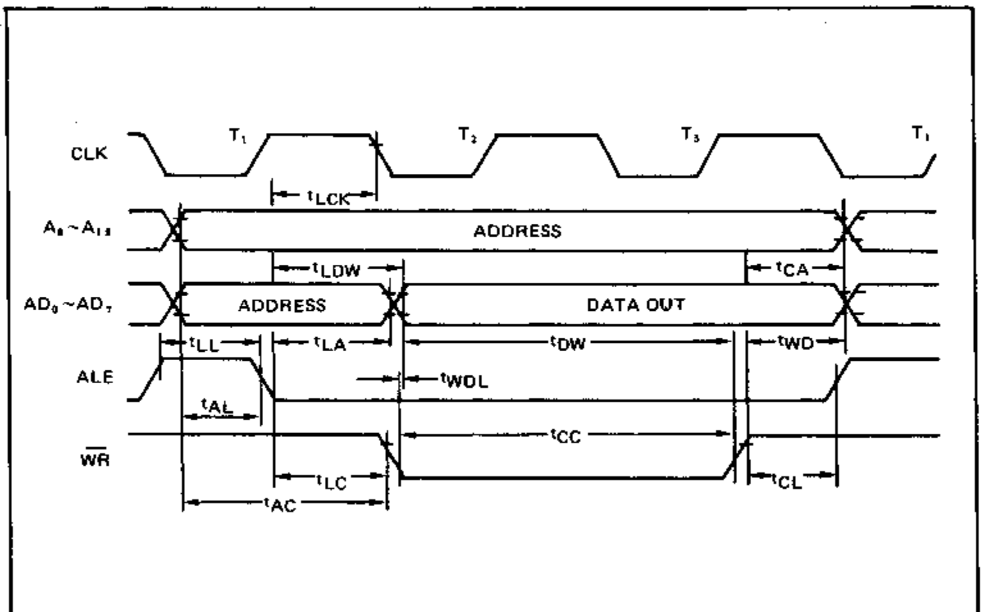


Figure 6 Clock Timing Waveform

READ OPERATION



WRITE OPERATION



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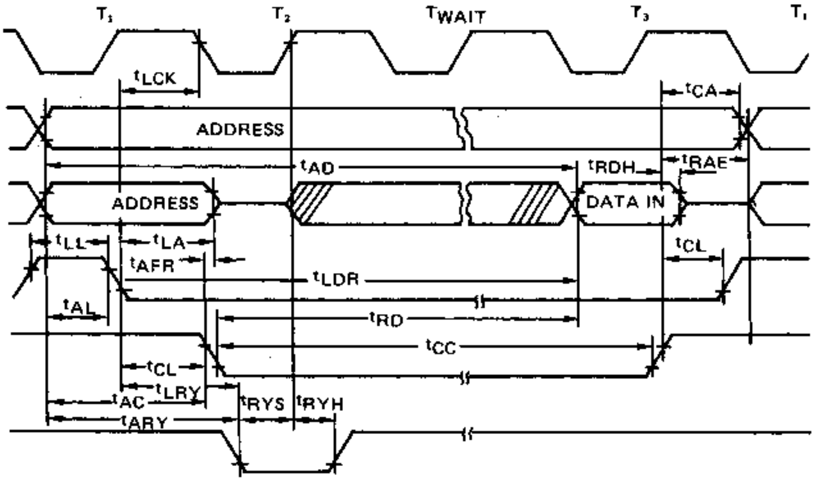
Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation



Note: READY must remain stable during setup and hold times.

Figure 7 MSM80C85A-2 Bus Timing, With and Without Wait

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HOLD OPERATION

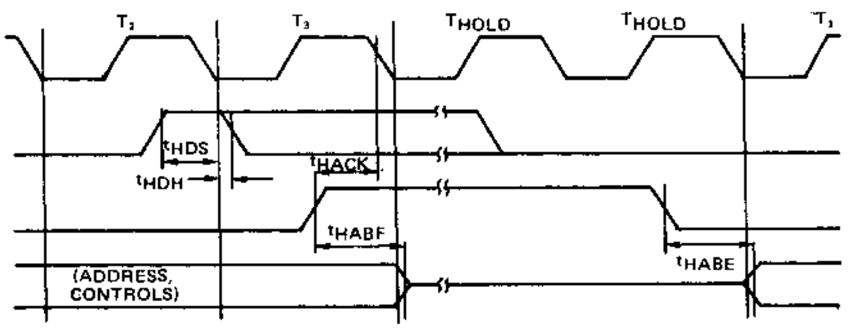
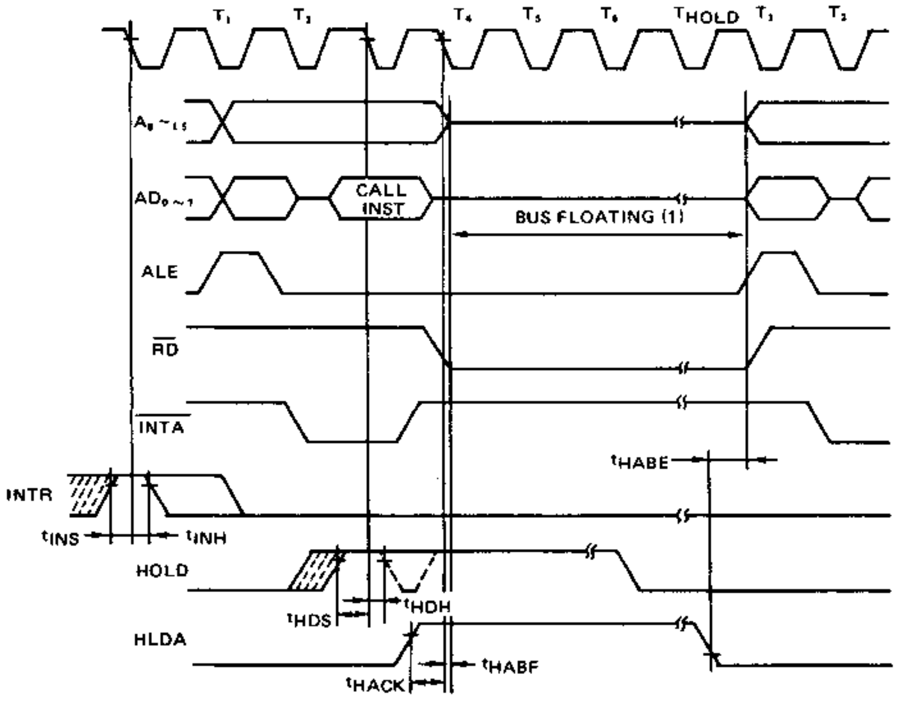


Figure 8 MSM80C85A-2 Hold Timing



Note: (1) IO/$\overline{M}$ is also floating during this time.

Figure 9 MSM80C85A-2 Interrupt and Hold Timing

Table 8 Instruction Set Summary

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock (2) Cycles
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code(1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock(2) Cycles
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

5

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code(1)								Clock(2) Cycles
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or Memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupts	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt (Power down)	0	1	1	1	0	1	1	0	5
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

Notes: (1) DDD or SSS. B 000. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111.
(2) Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.

5

OKI semiconductor

MSM80C86ARS/GS/JS
MSM80C86A-2RS/GS/JS

16-BIT CMOS MICROPROCESSOR

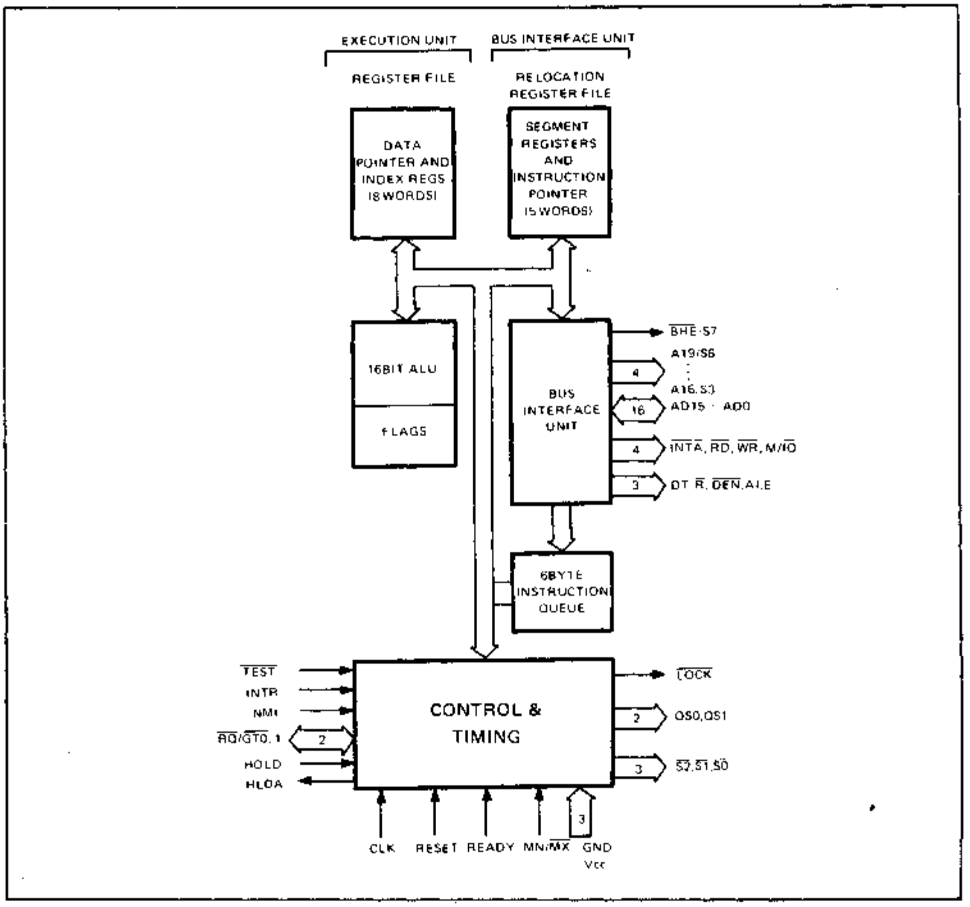
GENERAL DESCRIPTION

The MSM80C86A/MSM80C86A-2 are complete 16-bit CPUs implemented in Silicon Gate CMOS technology. They are designed with same processing speed as the NMOS 8086/8086-2 but have considerably less power consumption. They are directly compatible with MSM80C88A/MSM80C88A-2 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

FEATURES

- 1 Mbyte Direct Addressable Memory Space
- Internal 14 Word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 5 MHz Clock Rate (MSM80C86A)
- From DC to 8 MHz Clock Rate (MSM80C86A-2)
- Low Power Dissipation 10 mA/MHz
- Bus Hold Circuitry Eliminates Pull-Up Resistors

CIRCUIT CONFIGURATION



PIN CONFIGURATION

MSM80C86ARS (Top View)
MSM80C86A-2RS
40 Lead Plastic DIP

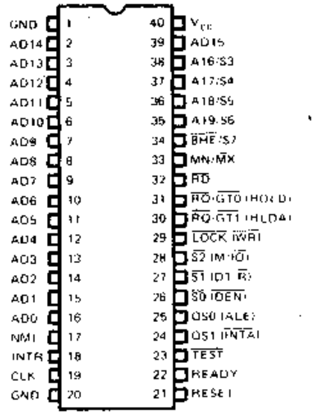


Fig. 2a MSM80C86ARS/MSM80C86A-2RS

MSM80C86AGS (Top View)
MSM80C86A-2GS
56 Lead Plastic Flat Package

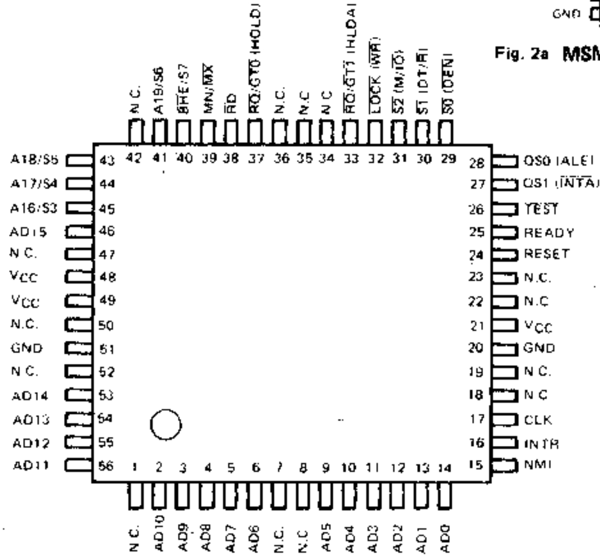
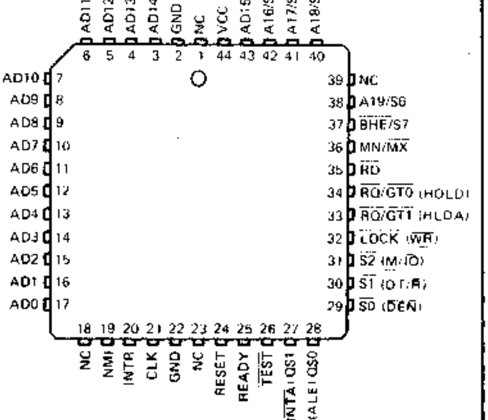


Fig. 2b MSM80C86AGS/MSM80C86A-2GS

MSM80C86AJS (Top View)
MSM80C86A-2JS
44-pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits			Unit	Conditions
		MSM80C86ARS MSM80C86A-2RS	MSM80C86AGS MSM80C86A-2GS	MSM80C86AJS MSM80C86A-2JS		
Power Supply Voltage	V_{CC}	-0.5 ~ +7			V	With respect to GND
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5			V	
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5			V	
Storage Temperature	Tstg	-65 ~ +150			°C	—
Power Dissipation	P_D	1.0	0.7		W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits		Unit
		MSM80C86A	MSM80C86A-2	
Power Supply Voltage	V_{CC}	3 ~ 6	4.75 ~ 5.25	V
Operating Temperature	T_{OP}	-40 ~ +85	0 ~ +70	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MSM80C86A			MSM80C86A-2			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	-40	+25	+85	0	+25	+70	°C
"L" Input Voltage	V_{IL}	-0.5		+0.8	-0.5		+0.8	V
"H" Input Voltage	V_{IH} (*1)	V_{CC}-0.8		V_{CC} +0.5	V_{CC}-0.8		V_{CC} +0.5	V
	V_{IH} (*2)	2.0		V_{CC} +0.5	2.0		V_{CC} +0.5	V

*1 Only CLK, *2 Except CLK.

DC CHARACTERISTICS

(MSM80C86A: V_{CC} = 4.5V to 5.5V, Ta = −40° to +85°C)
(MSM80C86A-2: V_{CC} = 4.75 to 5.25V, Ta = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
"L" Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.0			V	I_{OH} = −2.5 mA
		V_{CC}−0.4				I_{OH} = −100 μA
Input Leak Current	I_{LI}	−1.0		+1.0	μA	$0 < V_I < V_{CC}$
Output Leak Current	I_{LO}	−10		+10	μA	V_O = V_{CC} or GND
Input Leakage Current (Bus Hold Low)	I_{BHL}	50		400	μA	V_{IN} = 0.8V *3
Input Leakage Current (Bus Hold High)	I_{BHH}	−50		−400	μA	V_{IN} = 3.0V *4
Bus Hold Low Overdrive	I_{BHLO}			600	μA	*5
Bus Hold High Overdrive	I_{BHHO}			−600	μA	*6
Operating Power Supply Current	I_{CC}			10	mA/MHz	V_{IL} = GND V_{IH} = V_{CC}
Standby Power Supply Current	I_{CCS}			500	μA	V_{CC} = 5.5V Outputs Unloaded V_{IN} = V_{CC} or GND
Input Capacitance	C_{in}			5	pF	*7
Output Capacitance	C_{out}			15	pF	*7
I/O Capacitance	$C_{I/O}$			20	pF	*7

*3 Test condition is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2–16, and 35–39

*4 Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2–16, 26–32, and 34–39.

*5 An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.

*6 An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

*7 Test Conditions: a) Freq = 1 MHz.
b) Ummeasured Pins at GND.
c) V_{IN} at 5.0V or GND.

A.C. CHARACTERISTICS

(MSM80C86A: V_{CC} = 4.5V to 5.5V, Ta = –40°C to +85°C)
(MSM80C86A-2: V_{CC} = 4.75V to 5.25V, Ta = 0°C to 70°C)

Minimum Mode System

Timing Requirements

Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
CLK Cycle Period	TCLCL	200	DC	125	DC	ns
CLK Low Time	TCLCH	118		68		ns
CLK High Time	TCHCL	69		44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10		10	ns
Data in Setup Time	TDVCL	30		20		ns
Data in Hold Time	TCLDX	10		10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		0		ns
READY Setup Time into MSM80C86A	TRYHCH	118		68		ns
READY Hold Time into MSM80C86A-2	TCHRYX	30		20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		-8		ns
HOLD Setup Time	THVCH	35		20		ns
INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	TINVCH	30		15		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15		15	ns

Timing Responses

Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
Address Valid Delay	TCLAV	10	110	10	60	ns
Address Hold Time	TCLAX	10		10		ns
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns
ALE Width	TLHLL	TCLCH-20		TCLCH-10		ns
ALE Active Delay	TCLLH		80		50	ns
ALE Inactive Delay	TCHLL		85		55	ns
Address Hold Time to ALE Inactive	TLLAX	TCHCL-10		TCHCL-10		ns
Data Valid Delay	TCLDV	10	110	10	60	ns
Data Hold Time	TCHDX	10		10		ns
Data Hold Time after $\overline{\text{WR}}$	TWHDX	TCLCH-30		TCLCH-30		ns
Control Active Delay 1	TCVCTV	10	110	10	70	ns
Control Active Delay 2	TCHCTV	10	110	10	60	ns
Control Inactive Delay	TCVCTX	10	110	10	70	ns
Address Float to $\overline{\text{RD}}$ Active	TAZRL	0		0		ns
$\overline{\text{RD}}$ Active Delay	TCLRL	10	165	10	100	ns

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Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns
HLDA Valid Delay	TCLHAV	10	160	10	100	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-75		2TCLCL-50		ns
$\overline{WR}$ Width	TWLWH	2TCLCL-60		2TCLCL-40		ns
Address Valid to ALE Low	TAVAL	TCLCH-60		TCLCH-40		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15		15	ns

Notes: 1. Signal at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3)

5

Maximum Mode System (Using MSM 82C88 Bus Controller)
Timing Requirements

Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
CLK Cycle Period	TCLCL	200	DC	125	DC	ns
CLK Low Time	TCLCH	118		68		ns
CLK High Time	TCHCL	69		44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10		10	ns
Data in Setup Time	TDVCL	30		20		ns
Data in Hold Time	TCLDX	10		10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		0		ns
READY Setup Time into MSM 80C86A	TRYHCH	118		68		ns
READY Hold Time into MSM 80C86A	TCHRYX	30		20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		-8		ns
Set up Time for Recognition (NMI, INTR, $\overline{\text{TEST}}$) (See Note 2)	TINVCH	30		15		ns
$\overline{\text{RQ}}/\overline{\text{GT}}$ Setup Time	TGVCH	30		15		ns
$\overline{\text{RQ}}$ Hold Time into MSM 80C86A	TCHGX	40		30		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15		15	ns
Input Fall Time (Except CLK) (From 2.0 to 0.8V)	TIHIL		15		15	ns

Timing Responses

Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
Command Active Delay (See Note 1)	TCLML	5	45	5	35	ns
Command Inactive Delay (See Note 1)	TCLMH	5	45	5	45	ns
READY Active to Status Passive (See Note 4)	TRYHSH		110		65	ns
Status Active Delay	TCHSV	10	110	10	60	ns
Status Inactive Delay	TCLSH	10	130	10	70	ns
Address Valid Delay	TCLAV	10	110	10	60	ns
Address Hold Time	TCLAX	10		10		ns
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns
Status Valid to ALE High (See Note 1)	TSVLH		35		25	ns
Status Valid to MCE High (See Note 1)	TSVMCH		35		30	ns
CLK low to ALE Valid (See Note 1)	TCLLH		35		25	ns
CLK Low to MCE High (See Note 1)	TCLMCH		35		25	ns
ALE Inactive Delay (See Note 1)	TCHLL	4	35	4	25	ns
Data Valid Delay	TCLDV	10	110	10	60	ns
Data Hold Time	TCHDX	10		10		ns

5

Parameter	Symbol	MSM80C86A		MSM80C86A-2		Unit
		Min.	Max.	Min.	Max.	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns
Control Inactive Delay (See Note 1)	TCVNX	5	45	10	45	ns
Address Float to $\overline{RD}$ Active	TAZRL	0		0		ns
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns
Direction Control Inactive Delay (See Note 1)	TCHDTH		35		30	ns
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-75		2TCLCL-50		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15		15	ns

Notes: 1. Signal at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3)
4. Applies only to T3 and wait states.

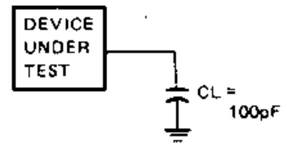
5

TIMING CHART

Input/Output

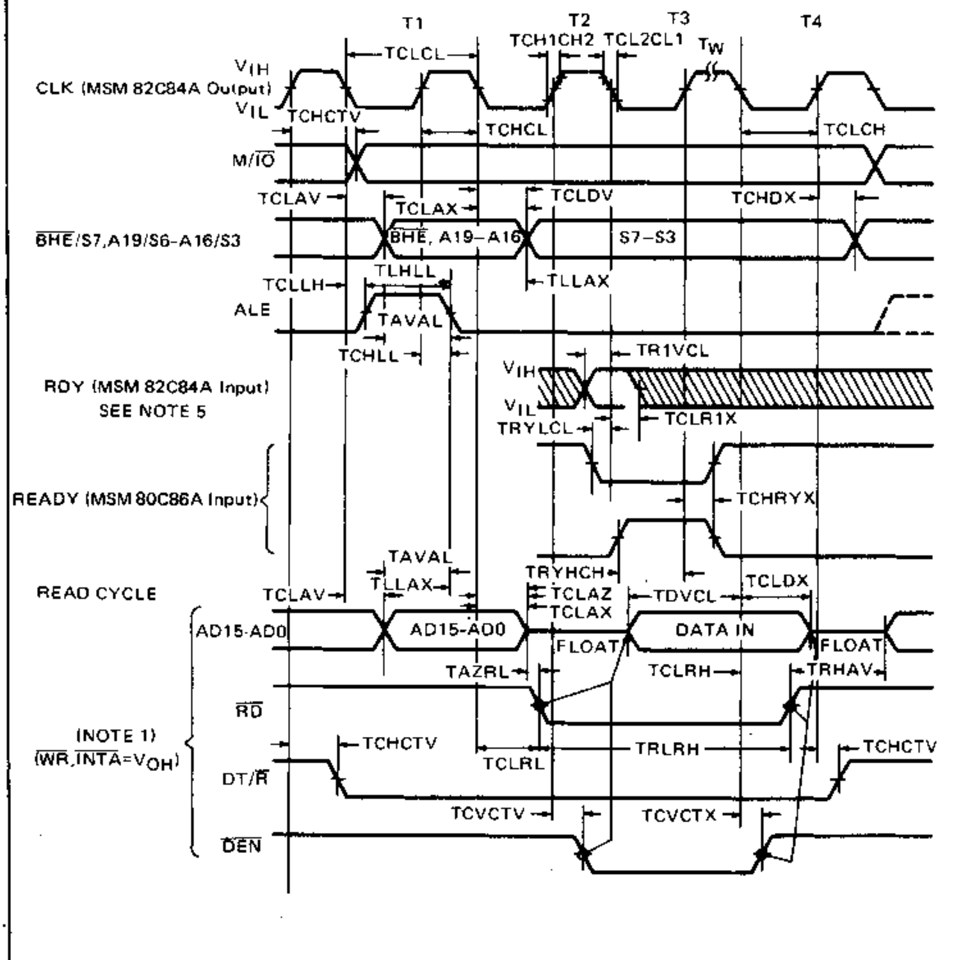
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE 1.5V FOR BOTH A LOGIC "1" AND "0"

A.C. Testing Load Circuit

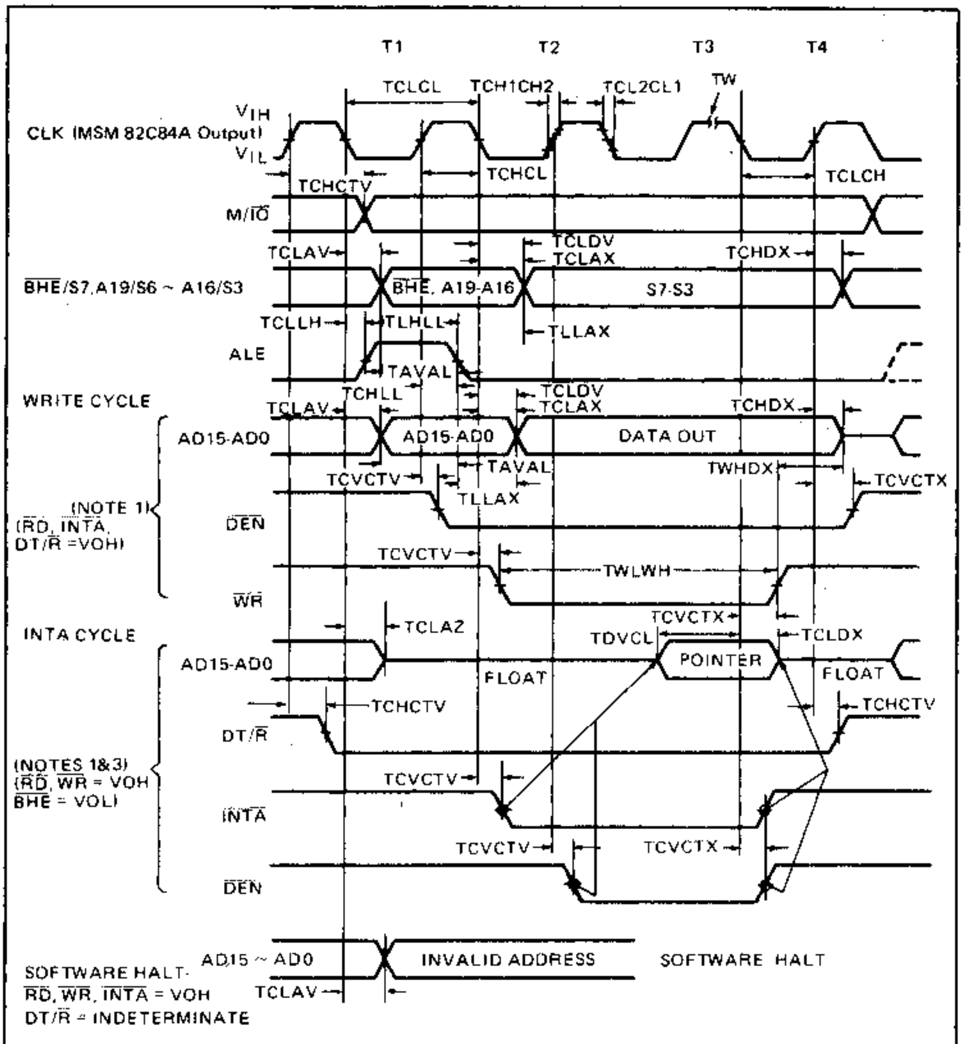


CL INCLUDES JIG CAPACITANCE

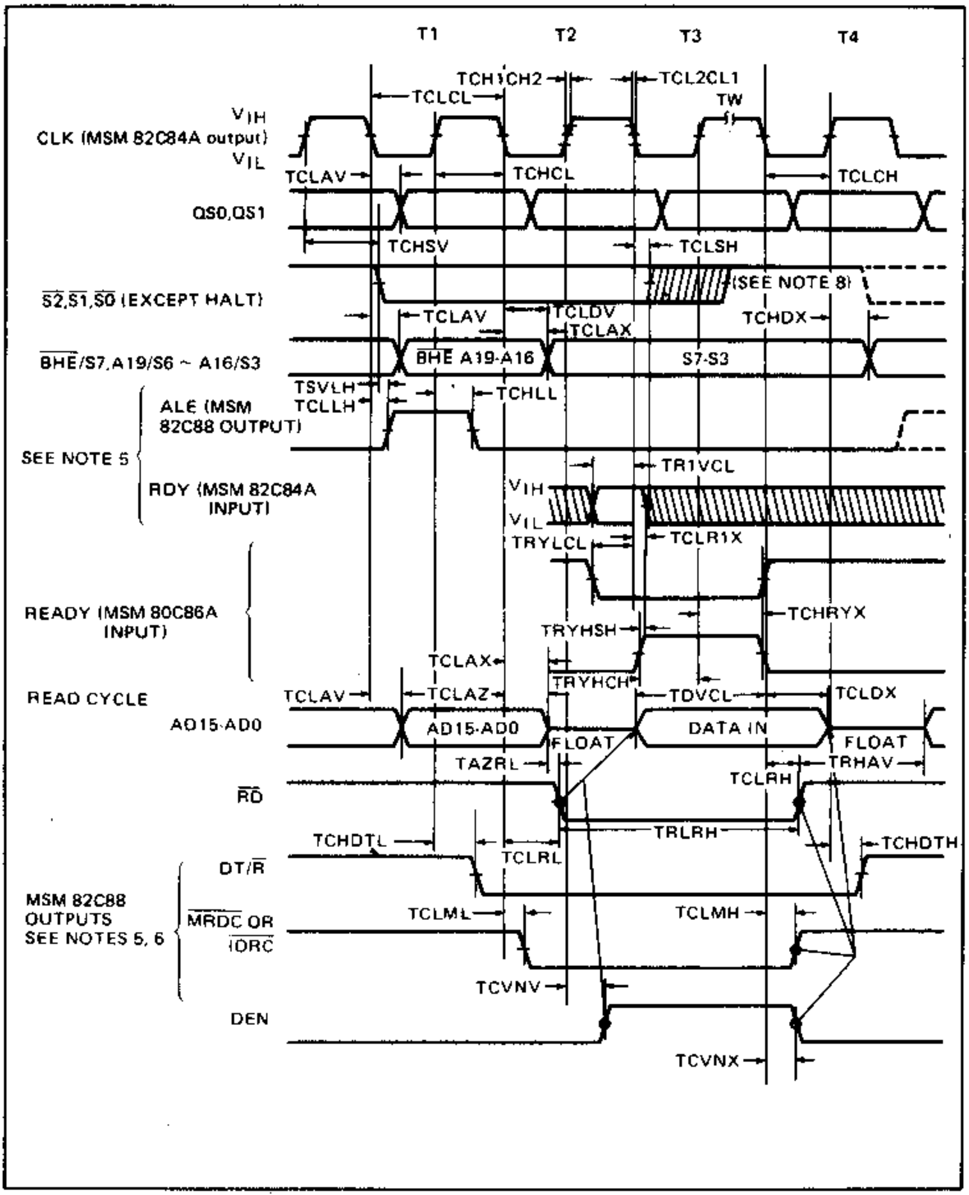
Minimum Mode



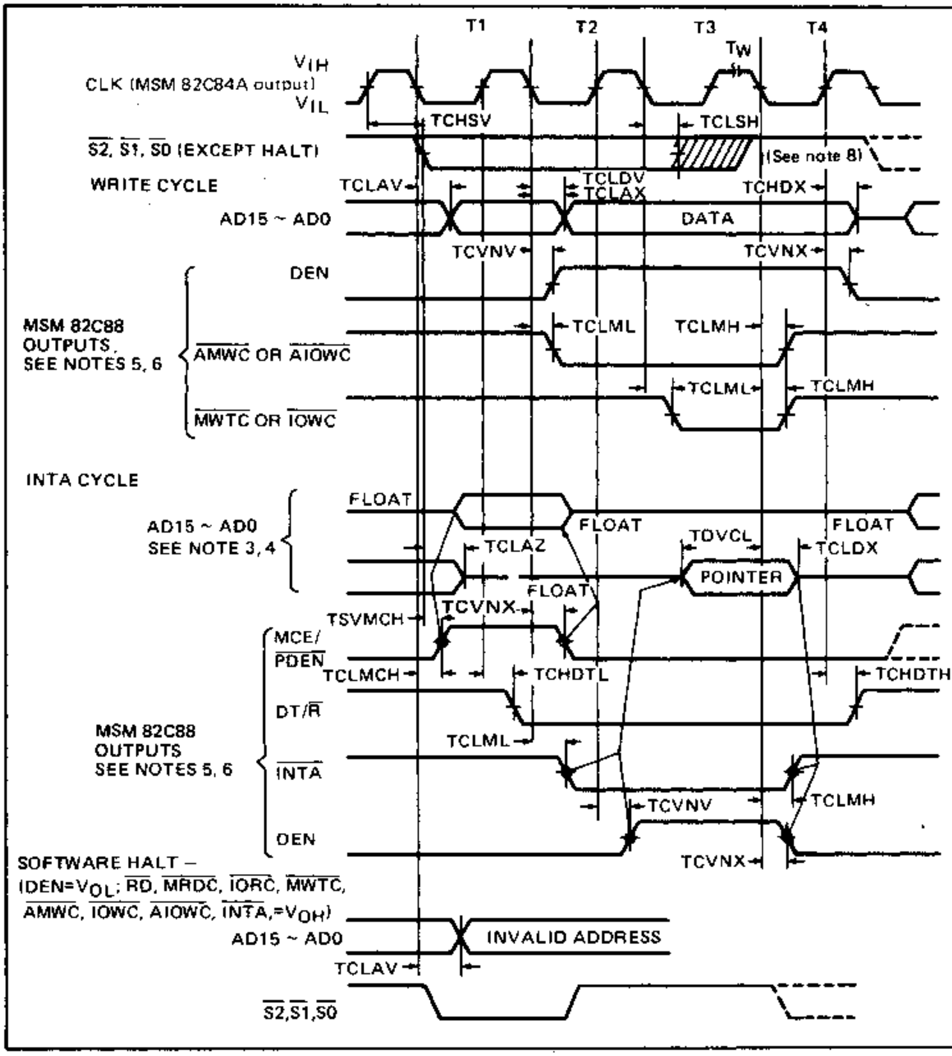
Minimum Mode (Continued)



Maximum Mode

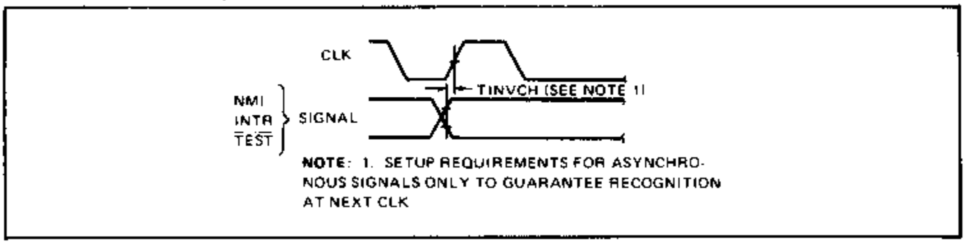


Maximum Mode (Continued)

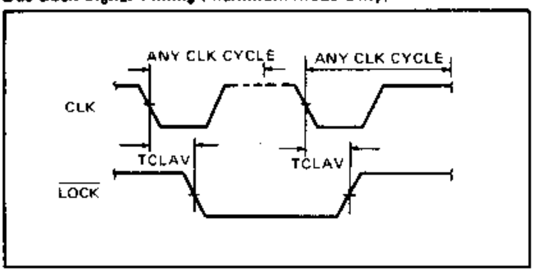


Notes:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2,T3,T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The MSM 80C86A LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at MSM 82C84A or MSM 82C88 are shown for reference only.
6. The issuance of the MSM 82C88 command and control signals (MRDC,MWTC,AMWC,IORC,IOWC,AIOWC, INTA and DEN) lags the active high MSM 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4.

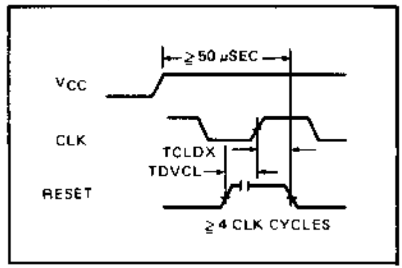
Asynchronous Signal Recognition



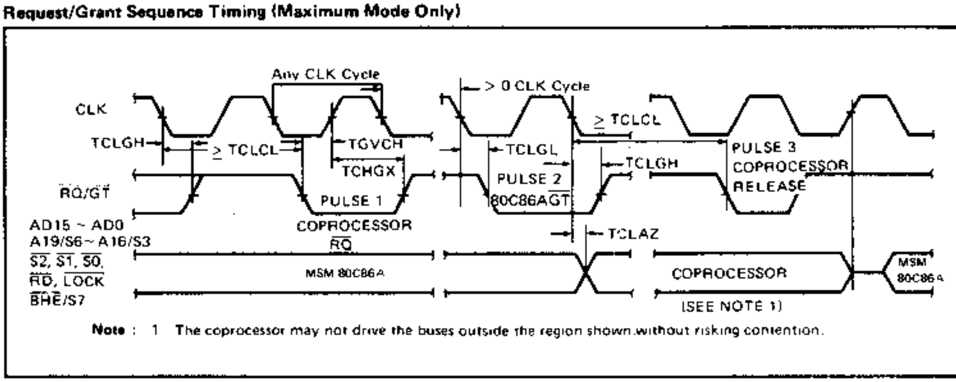
Bus Lock Signal Timing (Maximum Mode Only)



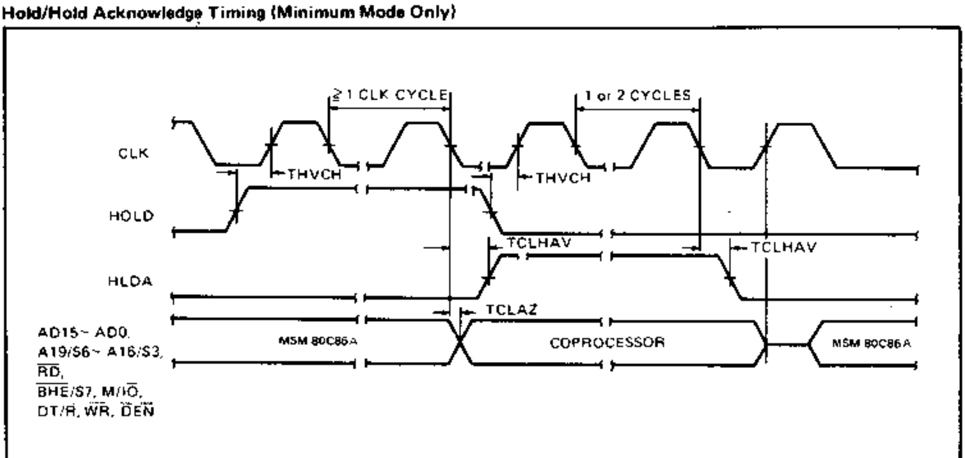
Reset Timing



Request/Grant Sequence Timing (Maximum Mode Only)



Hold/Hold Acknowledge Timing (Minimum Mode Only)



PIN DESCRIPTION

AD0 – AD15

ADDRESS DATA BUS: Input/Output

These lines are the multiplexed address and data bus.

These are the address bus at the T1 cycle and the data bus at the T2, T3, TW and T4 cycles.

At the T1 cycle, AD0 low indicates Data Bus Low (D0 – D7) Enable. These lines are high impedance during interrupt acknowledge and hold acknowledge.

A16/S3, A17/S4, A18/S5, A19/S6

ADDRESS/STATUS: Output

Tses are the four most significant addresses, at the T1 cycle. Accessing I/O port address, these are low at T1 cycles. These lines are Status lines at T2, T3, TW and T4 cycles. S3 and S4 are encoded as shown.

S3	S4	Characteristics
0	0	Alternate Data
1	0	Stack
0	1	Code or None
1	1	Data

These lines are high impedance during hold acknowledge.

$\overline{BHE}$/S7

BUS HIGH ENABLE/STATUS: Output

This line indicates Data Bus High Enable (BHE) at the T1 cycle.

This line indicates Data Bus High Enable (BHE) at the T1 cycles.

This line is status line at T2, T3, TW and T4 cycles.

$\overline{RD}$

READ: Output

This line indicates that CPU is in the memory or I/O read cycle.

This line is the read strobe signal when CPU read data from memory or I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

READY

READY: Input

This line indicates to the CPU that the addressed memory or I/O device is ready to read or write.

This line is active high.

If the setup and hold time is out of specification, illegal operation will occur.

INTR

INTERRUPT REQUEST: Input

This line is the level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulation.

It can be internally masked by software.

This signal is active high and internally synchronized.

$\overline{TEST}$

TEST: Input

This line is examined by the WAIT instruction.

When $\overline{TEST}$ is high, the CPU enters idle cycle.

When $\overline{TEST}$ is low, the CPU exits the idle cycle.

NMI

NON MASKABLE INTERRUPT: Input

This line causes a type 2 interrupt.

NMI is not maskable.

This signal is internally synchronized and needs 2 clock cycles of pulse width.

RESET

RESET: Input

This signal causes the CPU to initialize immediately.

This signal is active high and must be at least four clock cycles.

CLK

CLOCK: Input

This signal provides the basic timing for the internal circuit.

MN/$\overline{MX}$

MINIMUM/MAXIMUM: Input

This signal selects the CPU's operating mode.

When V_{CC} is connected, the CPU operates in Minimum mode.

Whin GND is connected, the CPU orerates Maximum mode.

V_{CC}

V_{CC}: +3 — +6V supplied.

GND

GROUND

The following pin function descriptions are maximum mode only.

Other pin functions are already described.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

STATUS: Output

These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals.

These lines are high impedance during hold acknowledge.

These status lines are encoded as shown.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

$\overline{RQ}/\overline{GT0}$
$\overline{RQ}/\overline{GT1}$
REQUEST/GRANT: Input/Output

These lines are used for Bus Request from other devices and Bus GRANT to other deivces.

These lines are bidirectional and active low.

$\overline{LOCK}$
LOCK: Output

This line is active low.

When this line is low, other devices can not gain control of the bus.

This line is high impedance during hold acknowledge.

QS0/QS1
QUEUE STATUS: Output

These lines are Queue Status, and indicate internal instrucion queue status.

QS1	QS0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are minimum mode only. Other pin functions are already described.

M/$\overline{IO}$
STATUS: Output

This line selects memory address space or I/O address space.

When this line is high, the CPU selects memory address space and when it is low, the CPU selects I/O address space.

This line is high impedance during hold acknowledge.

$\overline{WR}$
WRITE: Output

This line indicates that the CPU is in the memory or I/O write cycle.

This line is a write strobe signal when the CPU writes data to memory or I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

$\overline{INTA}$
INTERRUPT ACKNOWLEDGE: Output

This line is a read strobe signal for the interrupt acknowledge cycle.

This line is active low.

ALE
ADDRESS LATCH ENABLE: Output

This line is used for latching the address into the MSM82C12 address latch, It is a possitive pulse and its trailing edge is used to strobe the address, This line is never floated.

DT/$\overline{R}$
DATA TRANSMIT/RECEIVE: Output

This line is used to control the output enable of the bus transceiver.

When this line is high, the CPU transmits data, and when it is low, the CPU receives data.

This line is high impedance during hold acknowledge.

$\overline{DEN}$
DATA ENABLE: Output

This line is used to control the output enable of the bus transceiver.

This line is active low. This line is high impedance during hold acknowledge.

HOLD
HOLD REQUEST: Input

This line is used for Bus Request from other devices.
This line is active high.

HLDA
HOLD ACKNOWLEDGE: Output

This line is used for Bus Grant to other devices.

This line is active high.

FUNCTIONAL DESCRIPTION

STATIC OPERATION

All MSM80C86A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C86A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C86A can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Sigle step clock operation allows simple interface circuitry to provice critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since MSM80C86A power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, MSM80C86A power requirement is the standby current (500 μA maximum).

GENERAL OPERATION

The internal function of the MSM80C86 consists of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. Instruction pre-fetch is perfomed while waiting for decording and execution of instructions. Thus, the CPU's performance is increased. Up to 6-bytes of instruction stream can be queued.

The EU receives pre-fetched instructions from the BIU queue, decodes and executes the instructions, and provides the un-relocated operand address to BIU.

MEMORY ORGANIZATION

The MSM80C86A has a 20-bit address to memory. Each address has an 8-bit data width. Memory is organized 00000H to FFFFFH and is logicaly divided into four segments: code, data, extra data and stack segment. Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)

All memory references are made relative to the segment register which functions in accordance with a select rule. Word operands can be located on even or odd address boundary.

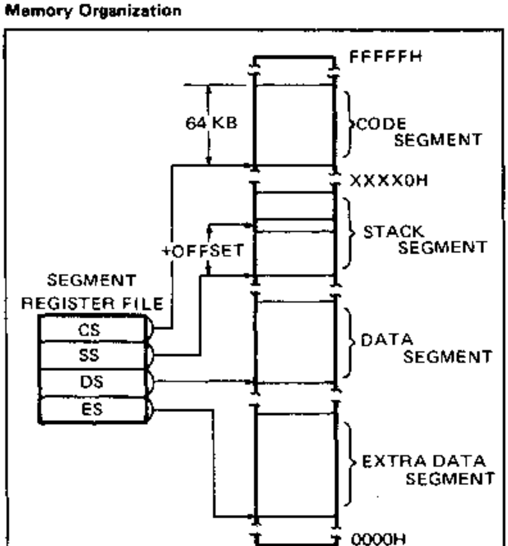
The BIU automatically performs the proper number of memory accesses. Memory consists of an even address and an odd address. Byte data of even address is transfered on the D0 – D7 and byte data of odd address is transfered on the D8 – D15.

The CPU prevides two enable signals $\overline{BHE}$ and A0 to access either an odd address, even address or both:

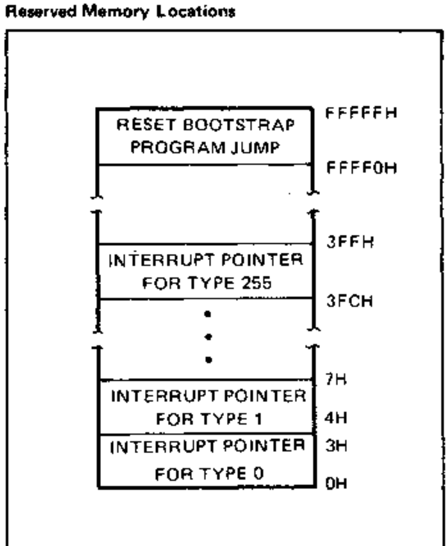
Memory location FFFF0H is the start address after reset, and 00000H through 003FFH are reserved as an interrupt pointer, where there are 256 types of interrupt pointers.

Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

Memory Organization



Reserved Memory Locations



Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment overriden.

MINIMUM AND MAXIMUM MODES

The MSM80C86A has two system modes: minimum and maximum. When using maximum mode, it is easy to organize a multi-CPU system with a 82C88 Bus Controller which generate the bus control signal.

When using minimum mode, it is easy to organize a simple system by generating bus control signal by itself.

MN/$\overline{MX}$ is the mode select pin. Definition of 24-31 pin changes depend on the MN/$\overline{MX}$ pin.

BUS OPERATION

The MSM80C86A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for a system, it is only to add the address latch.

A CPU bus cycle consists of at least four clock cycles: T1, T2 T3 and T4. (Fig. 4)

The address output occurs during T1 and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus at the read operation. When the device which is accessed by the CPU is not ready for The data transfer and the CPU "NOT READY", TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution. During the T1 cycle, the ALE signal is output from the CPU or the MSM82C88 depending on MN/$\overline{MX}$. At the trailing edge of ALE, a valid address may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used in the maximum mode by the bus controller to recognize the type of bus operation according to the following table.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are multiplexed with A16 ~ A19, and $\overline{BHE}$; therefore, they are valid during T2 through T4.

S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table.

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

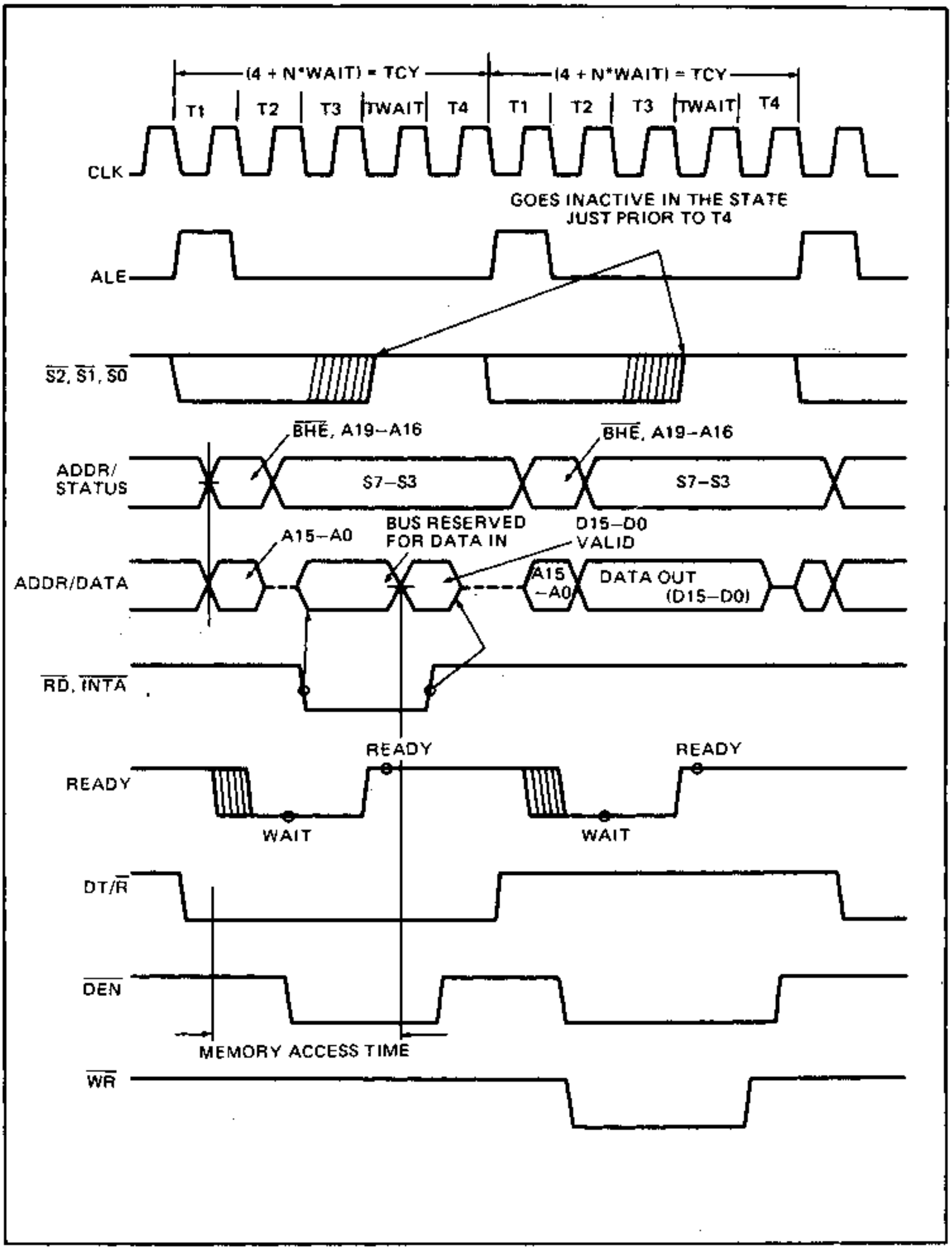
S5 indicates interrupt enable Flag.

I/O ADDRESSING

The MSM80C86A has 64 Kbyte of I/O or as 32 Kwords I/O. When the CPU accesses an I/O device, addresses A0 ~ A15 are in the same format as a memory address, and A16 ~ A19 are low.

The I/O ports addresses are same as memory, so it is necessary to be careful when using 8-bit peripherals.

Basic System Timing



EXTERNAL INTERFACE

RESET

CPU Initalization is executed by the RESET pin. The MSM80C86A's RESET High signal is required for greater than 4 clock cycles.

The Rising edge of RESET terminates present operation immediately. The Falling edge of RESET triggers an internal reset sequence for approximately 10 clock cycles. Afer the internal reset sequence is finished normal operation occurs from absolute location FFFF0H.

INTERRUPT OPERATIONS

Interrupt operation is classified as software or hardware, and hardware interrupt is classified as non-maskable or maskable.

An interrupt causes a new program location defined on the interrupt pointer table, according to the interrupt type. Absolute locations 00000H through 003FFH are reserved for the interrupt pointer table. The interrupt pointer table consists of 256-elements. Each element is 4 bytes in size and corresponds to an 8 bit type number which is sent from an interrupt interrupt request device during the interrupt acknowledge cycle.

NON-MASKABLE INTERRUPT (NMI)

The MSM80C86A has a Non-maskable Interrupt (NMI) which is of higher priority than the maskable interrupt request (INTR).

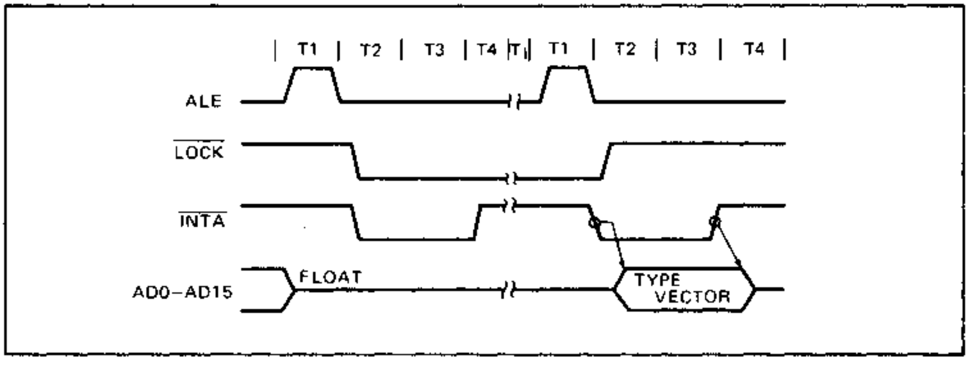
The NMI request pulse width needs a minimum of 2 clock cycles. The NMI will be serviced at the end of the current instruction or between string manipulations.

MASKABLE INTERRUPT (INTR)

The MSM80C86A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until the interrupt request is acknowledged.

INTR will be serviced at the end of the aurrent instruction or between string manipulations.

Interrupt Acknowledge Sequence



INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt, after which the Flag register is automatically pushed onto the stack. During the acknowledge sequence, the CPU emits the lock signal from T2 of the first bus cycle to T2 of the second bus cycle. At second bus cyclees, byte is fetched from the external device as a vector which identified the type of interrupt. This vector is multiplied by four and used as a interrupt pointer address. (INTR only)

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

HALT

When a Halt instruction is executed, the CPU enters the Halt state. An interrupt request or RESET will force the MSM80C86A out of the Halt state.

SYSTEM TIMING – MINIMUM MODE

A bus cycle begins T1 with an ALE signal. The trailing edge of ALE is used to latch the address. From T1 to T4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to data bus.

The read ($\overline{RD}$), write ($\overline{WR}$) and interrupt acknowledge ($\overline{INTA}$) signals causes the addressed device to enable data bus. These signal becomes active at the beginning of T2 and inactive at the beginning of T4.

SYSTEM TIMING – MAXIMUM MODE

At maximum mode, the MSM82C88 Bus Controller is added to system. The CPU sends status information to the Bus Controller. Bus timing signals are generated by Bus Controller. Bus timing is almost the same as in the minimum mode.

5

BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on MSM80C86A pins 2–16, 26–32, and 34–39 (Figures 6a, 6b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 600 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

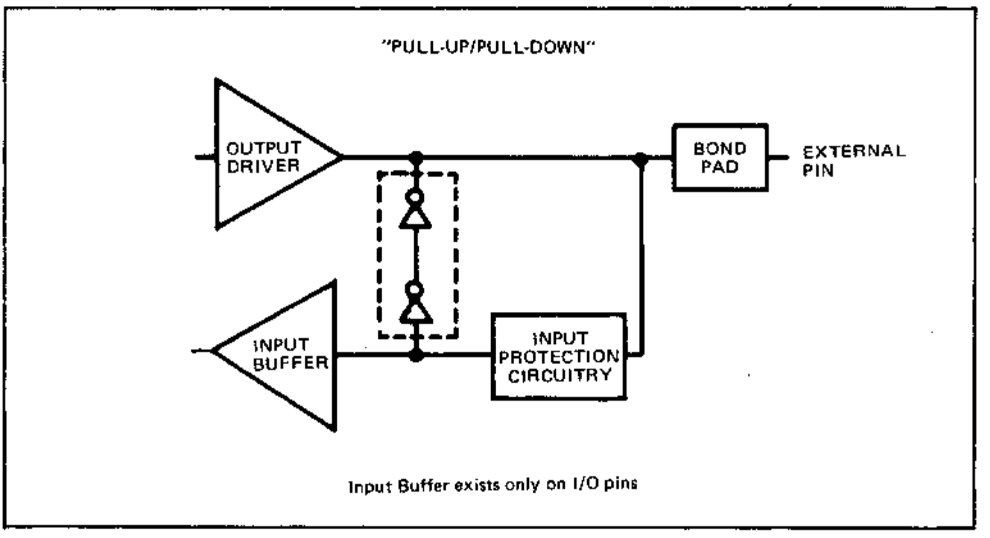


Figure 6a. Bus hold circuitry pin 2-16, 35-39.

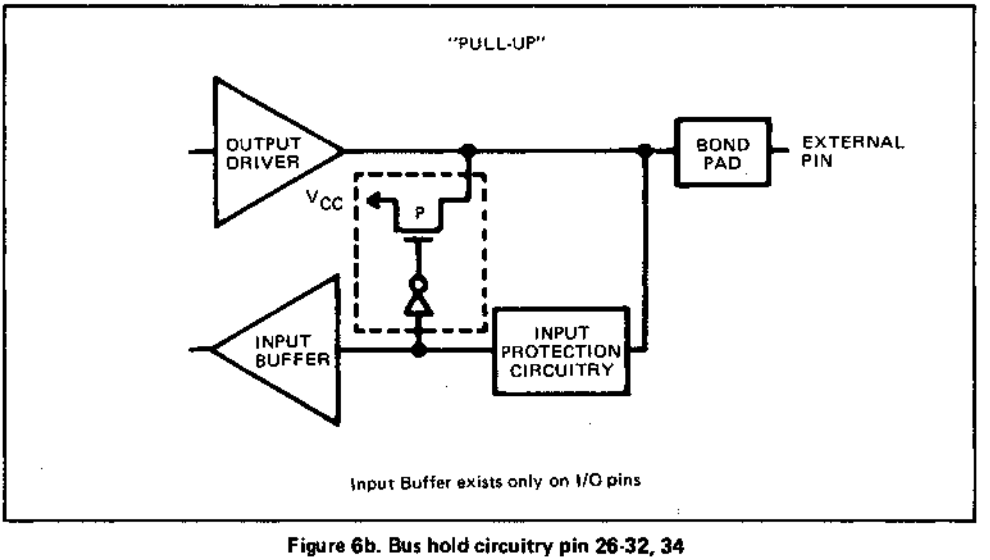


Figure 6b. Bus hold circuitry pin 26-32, 34

DATA TRANSFER

MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate to register	1 0 1 1 w reg	data	data if w = 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with borrow:				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1			

DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD = Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate left through carry	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate right through carry	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w			

CJMP = Conditional JMP				
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp		
JZ/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp		
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp		
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp		
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp		
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp		
JO = Jump on over flow	0 1 1 1 0 0 0 0	disp		
JS = Jump on sign	0 1 1 1 1 0 0 0	disp		
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp		
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp		
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp		
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp		
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp		
JNP/JPO = Jump on not parity/parity odd	0 1 1 1 1 0 1 1	disp		
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp		
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp		
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp		
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp		
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp		
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp		
INT = Interrupt:				
Type specified	1 1 0 0 1 1 0 1	type		
Type 3	1 1 0 0 1 1 0 0			
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0			
IRET = Interrupt return	1 1 0 0 1 1 1 1			

PROCESSOR CONTROL

CLC = Clear carry	1 1 1 1 1 0 0 0			
CMC = Complement carry	1 1 1 1 0 1 0 1			
STC = Set carry	1 1 1 1 1 0 0 1			
CLD = Clear direction	1 1 1 1 1 1 0 0			
STD = Set direction	1 1 1 1 1 1 0 1			
CLI = Clear interrupt	1 1 1 1 1 0 1 0			
STI = Set interrupt	1 1 1 1 1 0 1 1			
HLT = Halt	1 1 1 1 0 1 0 0			
WAIT = Wait	1 0 0 1 1 0 1 1			
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m		
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0			

CONTROL TRANSFER

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CALL = Call:				
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct within segment-short	1 1 1 0 1 0 1 1	disp		
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within segment	1 1 0 0 0 0 1 1			
Within seg. adding immediate to SP	1 1 0 0 0 0 1 0	data-low	data-high	
Intersegment	1 1 0 0 1 0 1 1			
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	

Footnotes:

AL = 8-bit accumulator
AX = 18-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed value
If d = 1 then "to" reg: If d = 0 then "from" reg.
If w = 1 then word instruction: If w = 0 then byte instruction

If mod = 11 then r/m is treated as a REG field
If mod = 00 then DISP = 0*, disp-low and disp-high are absent
If mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
If mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
If r/m = 001 then EA = (BX) + (DI) + DISP
If r/m = 010 then EA = (BP) + (SI) + DISP
If r/m = 011 then EA = (BP) + (DI) + DISP
If r/m = 100 then EA = (SI) + DISP
If r/m = 101 then EA = (DI) + DISP
If r/m = 110 then EA = (BP) + DISP*
If r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
* except if mod = 00 and r/m = 110 then EA-disp-high: disp-low

If s:w = 01 then 16 bits of immediate data form the operand
If s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
If v = 0 then "count" = 1: If v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit	(w = 1)	8-Bit	(w = 0)	Segment	
000	AX	000	AL	00	ES
001	CX	001	CL	01	CS
010	DX	010	DL	10	SS
011	BX	011	BL	11	DS
100	SP	100	AH		
101	BP	101	CH		
110	SI	110	DH		
111	DI	111	BH		

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = x:x:x:x:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Preliminary

MSM80C86A-10RS/GS/JS

16-BIT CMOS MICROPROCESSOR

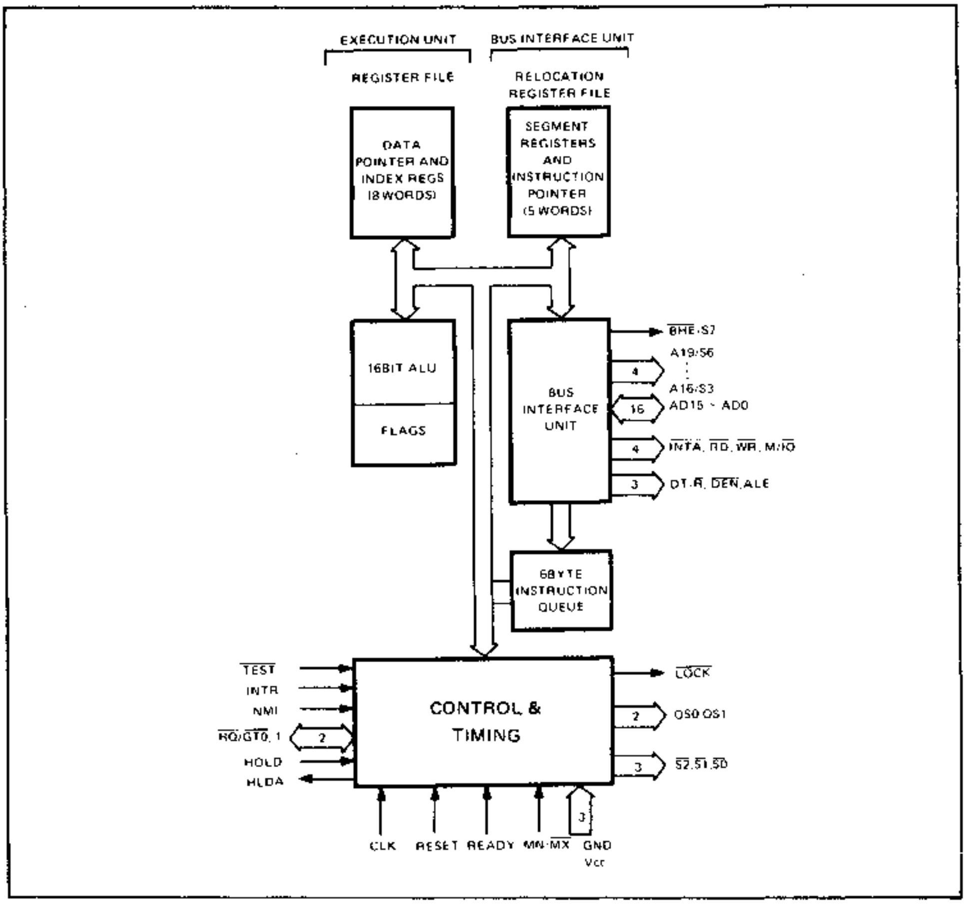
GENERAL DESCRIPTION

The MSM80C86A-10 are complete 16-bit CPUs implemented in Silicon Gate CMOS technology. They are designed with same processing speed as the NMOS 8086-1 but have considerably less power consumption. They are directly compatible with MSM80C88A-10 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

FEATURES

- 1 Mbyte Direct Addressable Memory Space
- Internal 14 Word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 10 MHz Clock Rate
- Low Power Dissipation 10 mA/MHz
- Bus Hold Circuitry Eliminates Pull-Up Resistors

CIRCUIT CONFIGURATION



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PIN CONFIGURATION

MSM80C86A-10RS (Top View)
40 Lead Plastic DIP

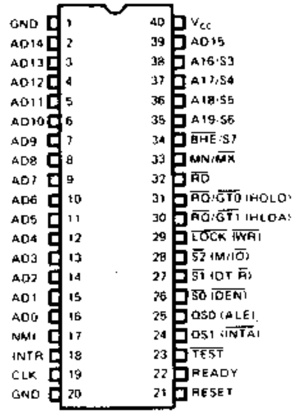


Fig. 2a MSM80C86A-10RS

MSM80C86A-10GS (Top View)
56 Lead Plastic Flat Package

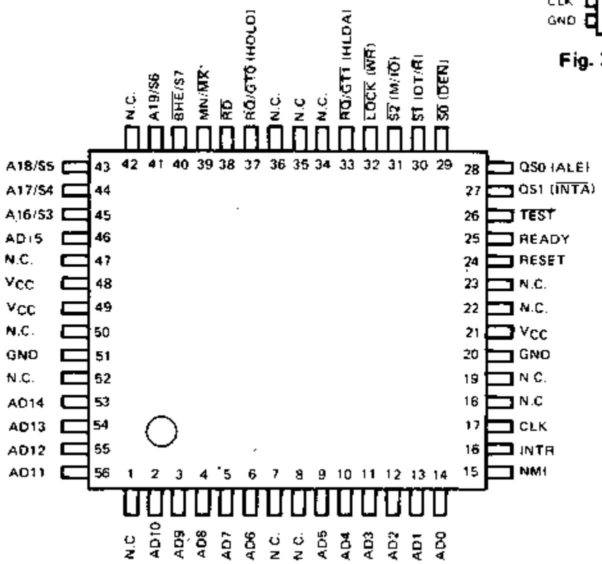
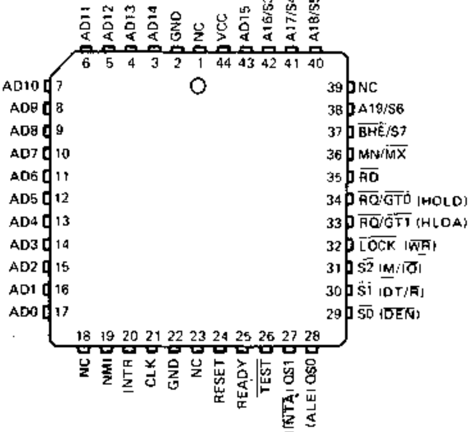


Fig. 2b MSM80C86A-10GS

MSM80C86A-10JS (Top View)
44-pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits			Unit	Conditions
		MSM80C86A-10RS	MSM80C86A-10GS	MSM80C86A-10JS		
Power Supply Voltage	V_{CC}	-0.5 ~ +7			V	With respect to GND
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5			V	
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5			V	
Storage Temperature	Tstg	-65 ~ +150			°C	–
Power Dissipation	P_D	1.0	0.7		W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits	Unit
		MSM80C86A-10	
Power Supply Voltage	V_{CC}	4.75 ~ 5.25	V
Operating Temperature	T_{OP}	0 ~ +70	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MSM80C86A-10			Unit
		MIN	TYP	MAX	
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	0	+25	+70	°C
"L" Input Voltage	V_{IL}	-0.5		+0.8	V
"H" Input Voltage	V_{IH} (*1)	V_{CC}-0.8		V_{CC} +0.5	V
	V_{IH} (*2)	2.0		V_{CC} +0.5	V

*1 Only CLK, *2 Except CLK.

5

DC CHARACTERISTICS

(MSM80C86A-10: V_{CC} = 4.75 to 5.25V, Ta = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
"L" Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.0			V	I_{OH} = −2.5 mA
		V_{CC}−0.4				I_{OH} = −100 μA
Input Leak Current	I_{LI}	−1.0		+1.0	μA	$0 < V_I < V_{CC}$
Output Leak Current	I_{LO}	−10		+10	μA	V_O = V_{CC} or GND
Input Leakage Current (Bus Hold Low)	I_{BHL}	50		400	μA	V_{IN} = 0.8V *3
Input Leakage Current (Bus Hold High)	I_{BHH}	−50		−400	μA	V_{IN} = 3.0V *4
Bus Hold Low Overdrive	I_{BHLO}			600	μA	*5
Bus Hold High Overdrive	I_{BHHO}			−600	μA	*6
Operating Power Supply Current	I_{CC}			10	mA/MHz	V_{IL} = GND, V_{IH} = V_{CC}
Standby Power Supply Current	I_{CCS}			500	μA	V_{CC} = 5.5V, Outputs Unloaded, V_{IN} = V_{CC} or GND
Input Capacitance	C_{in}			5	pF	*7
Output Capacitance	C_{out}			15	pF	*7
I/O Capacitance	$C_{I/O}$			20	pF	*7

*3 Test condition is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2–16, and 35–39

*4 Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2–16, 26–32, and 34–39.

*5 An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.

*6 An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.

*7 Test Conditions: a) Freq = 1 MHz.
b) Ummeasured Pins at GND.
c) V_{IN} at 5.0V or GND.

5

A.C. CHARACTERISTICS

(MSM80C86A-10: V_{CC} = 4.75V to 5.25V, Ta = 0°C to 70°C)

Minimum Mode System

Timing Requirements

Parameter	Symbol	MSM80C86A-10		Unit
		Min.	Max.	
CLK Cycle Period	TCLCL	100	DC	ns
CLK Low Time	TCLCH	46		ns
CLK High Time	TCHCL	44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10	ns
Data in Setup Time	TDVCL	20		ns
Data in Hold Time	TCLDX	10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		ns
READY Setup Time into MSM80C86A	TRYHCH	46		ns
READY Hold Time into MSM80C86A-2	TCHRYX	20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		ns
HOLD Setup Time	THVCH	20		ns
INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	TINVCH	15		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15	ns

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Timing Responses

Parameter	Symbol	MSM80C86A-10		Unit
		Min.	Max.	
Address Valid Delay	TCLAV	10	60	ns
Address Hold Time	TCLAX	10		ns
Address Float Delay	TCLAZ	TCLAX	50	ns
ALE Width	TLHLL	TCLCH-10		ns
ALE Active Delay	TCLLH		40	ns
ALE Inactive Delay	TCHLL		45	ns
Address Hold Time to ALE Inactive	TLLAX	TCHCL-10		ns
Data Valid Delay	TCLDV	10	60	ns
Data Hold Time	TCHDX	10		ns
Data Hold Time after $\overline{\text{WR}}$	TWHDX	TCLCH-25		ns
Control Active Delay 1	TCVCTV	10	55	ns
Control Active Delay 2	TCHCTV	10	50	ns
Control Inactive Delay	TCVCTX	10	55	ns
Address Float to $\overline{\text{RD}}$ Active	TAZRL	0		ns
$\overline{\text{RD}}$ Active Delay	TCLRL	10	70	ns

Parameter	Symbol	MSM80C86A-10		Unit
		Min.	Max.	
$\overline{RD}$ Inactive Delay	TCLRH	10	60	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-35		ns
HLDA Valid Delay	TCLHAV	10	60	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-40		ns
$\overline{WR}$ Width	TWLWH	2TCLCL-35		ns
Address Valid to ALE Low	TAVAL	TCLCH-35		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15	ns

Notes: 1. Signal at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3)

5

Maximum Mode System (Using MSM 82C88 Bus Controller)
Timing Requirements

Parameter	Symbol	MSM80C86A-10 Min.	MSM80C86A-10 Max.	Unit
CLK Cycle Period	TCLCL	100	DC	ns
CLK Low Time	TCLCH	46		ns
CLK High Time	TCHCL	44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10	ns
Data in Setup Time	TDVCL	15		ns
Data in Hold Time	TCLDX	10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		ns
READY Setup Time into MSM 80C86A	TRYHCH	46		ns
READY Hold Time into MSM 80C86A	TCHRYX	20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		ns
Set up Time for Recognition (NMI, INTR, $\overline{TEST}$) (See Note 2)	TINVCH	15		ns
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	15		ns
$\overline{RQ}$ Hold Time into MSM 80C86A	TCHGX	20		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15	ns
Input Fall Time (Except CLK) (From 2.0 to 0.8V)	TIHIL		15	ns

5

Timing Responses

Parameter	Symbol	MSM80C86A-10 Min.	MSM80C86A-10 Max.	Unit
Command Active Delay (See Note 1)	TCLML	5	35	ns
Command Inactive Delay (See Note 1)	TCLMH	5	45	ns
READY Active to Status Passive (See Note 4)	TRYHSH		45	ns
Status Active Delay	TCHSV	10	45	ns
Status Inactive Delay	TCLSH	10	60	ns
Address Valid Delay	TCLAV	10	60	ns
Address Hold Time	TCLAX	10		ns
Address Float Delay	TCLAZ	TCLAX	50	ns
Status Valid to ALE High (See Note 1)	TSVLH		25	ns
Status Valid to MCE High (See Note 1)	TSVMCH		30	ns
CLK low to ALE Valid (See Note 1)	TCLLH		25	ns
CLK Low to MCE High (See Note 1)	TCLMCH		25	ns
ALE Inactive Delay (See Note 1)	TCHLL	4	25	ns
Data Valid Delay	TCLDV	10	60	ns
Data Hold Time	TCHDX	10		ns

Parameter	Symbol	MSM80C86A-10		Unit
		Min.	Max.	
Control Active Delay (See Note 1)	TCVNV	5	45	ns
Control Inactive Delay (See Note 1)	TCVNX	10	45	ns
Address Float to $\overline{RD}$ Active	TAZRL	0		ns
$\overline{RD}$ Active Delay	TCLRL	10	70	ns
$\overline{RD}$ Inactive Delay	TCLRH	10	60	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-35		ns
Direction Control Active Delay (See Note 1)	TCHDTL		50	ns
Direction Control Inactive Delay (See Note 1)	TCHDTH		30	ns
$\overline{GT}$ Active Delay	TCLGL	0	45	ns
$\overline{GT}$ Inactive Delay	TCLGH	0	45	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-40		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15	ns

Notes: 1. Signal at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3)
4. Applies only to T3 and wait states.

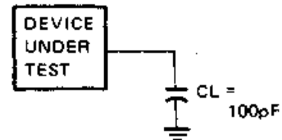
5

TIMING CHART

Input/Output

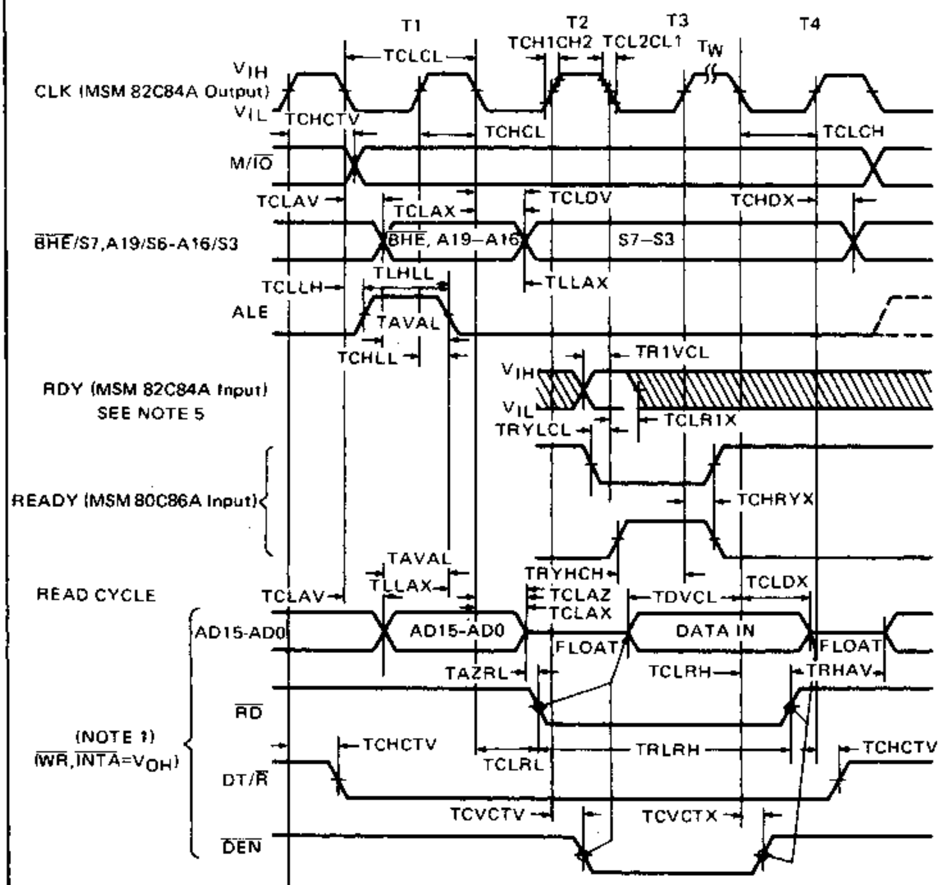
A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE 1.5V FOR BOTH A LOGIC "1" AND "0"

A.C. Testing Load Circuit

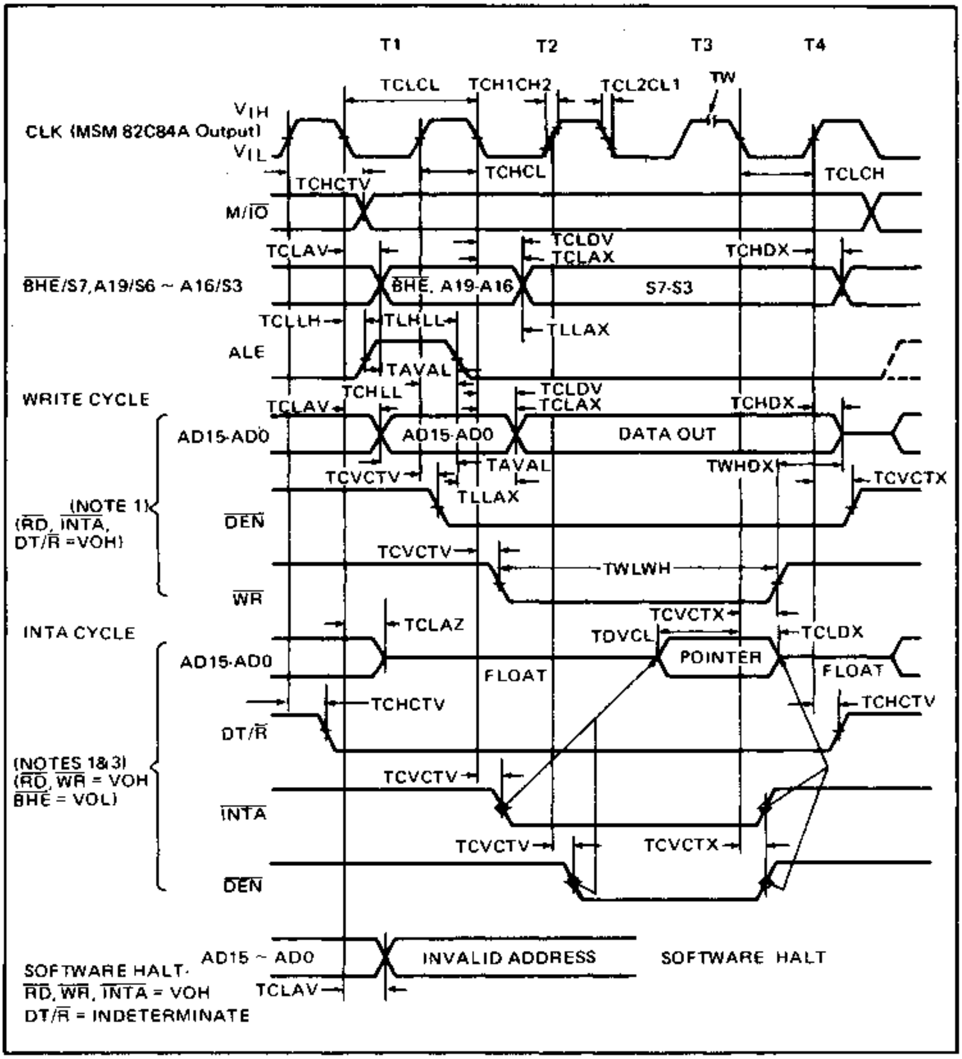


CL INCLUDES JIG CAPACITANCE

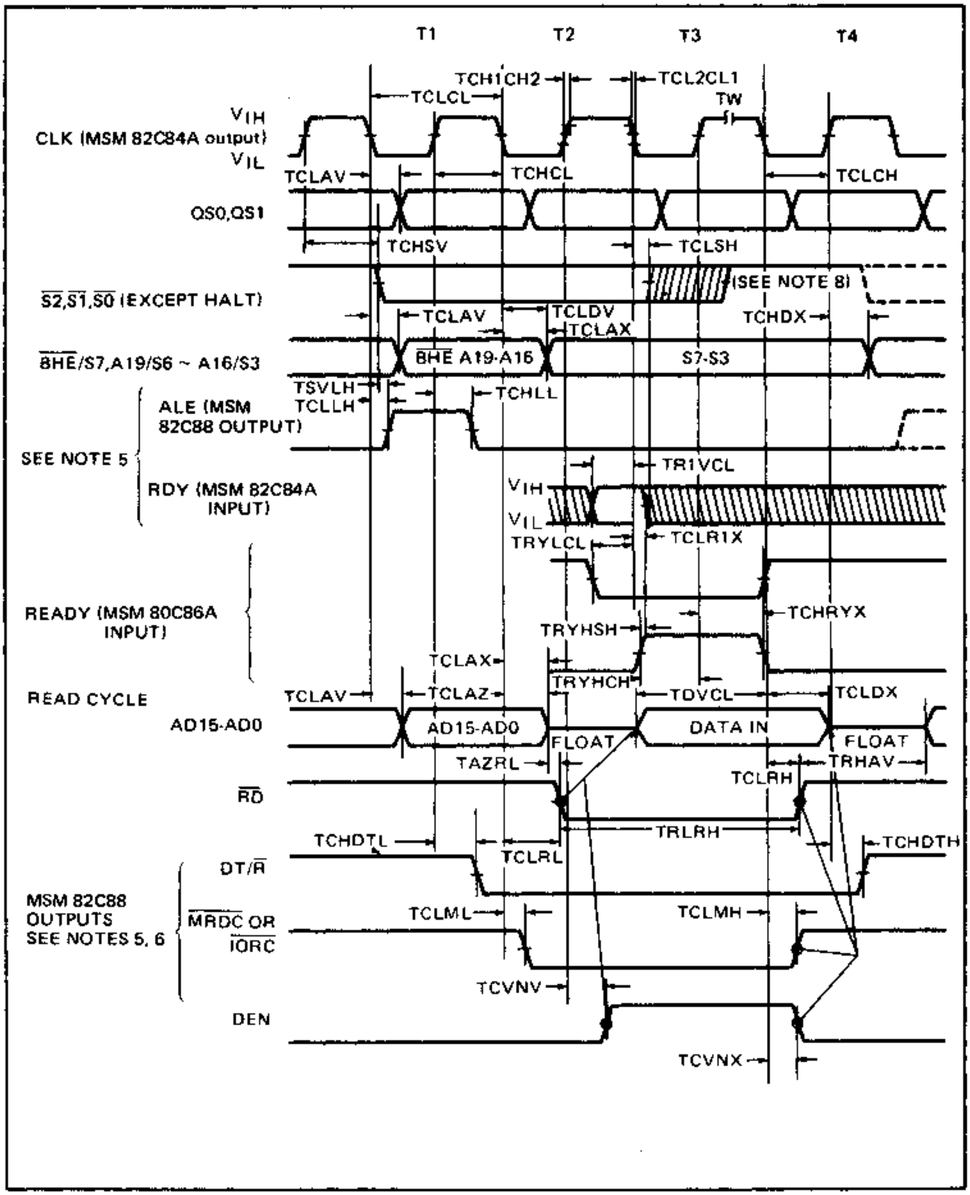
Minimum Mode



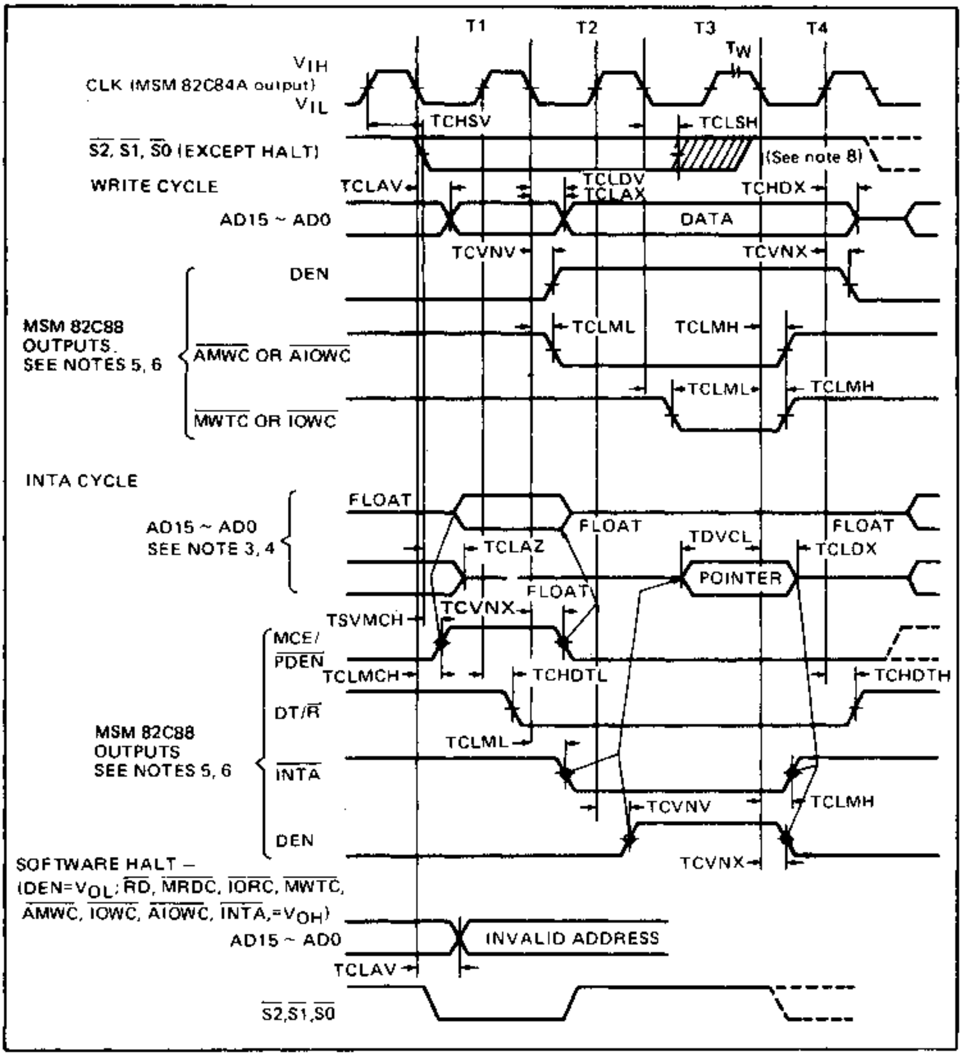
Minimum Mode (Continued)



Maximum Mode



Maximum Mode (Continued)



Notes:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2,T3,T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second INTA cycle.
4. Two INTA cycles run back-to-back. The MSM 80C86A LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at MSM 82C84A or MSM 82C88 are shown for reference only.
6. The issuance of the MSM 82C88 command and control signals (MRDC,MWTC,AMWC,IORC,IOWC,AIOWC, INTA and DEN) lags the active high MSM 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T4

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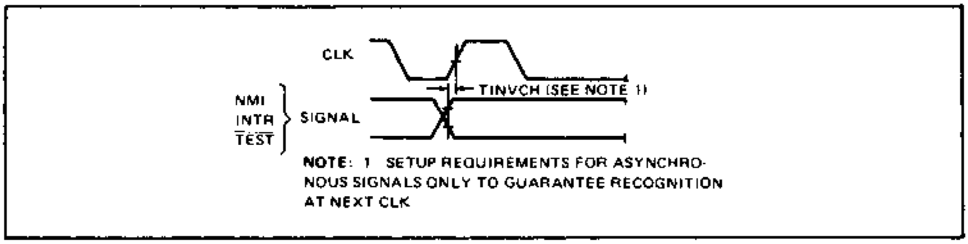
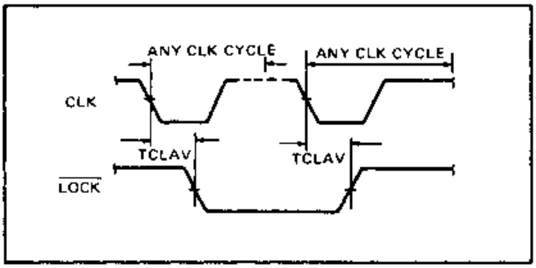
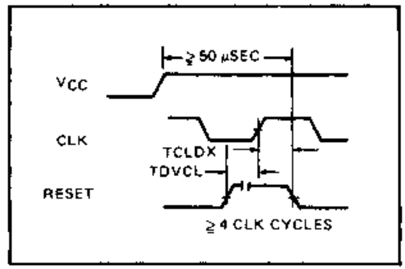
Asynchronous Signal Recognition



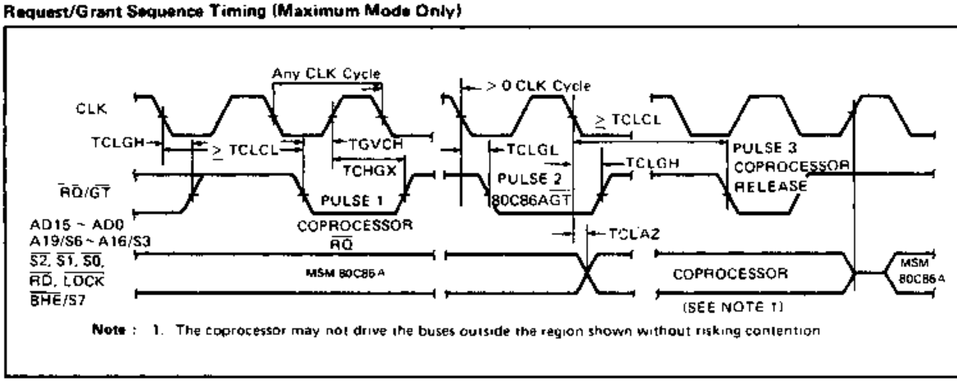
Bus Lock Signal Timing (Maximum Mode Only)



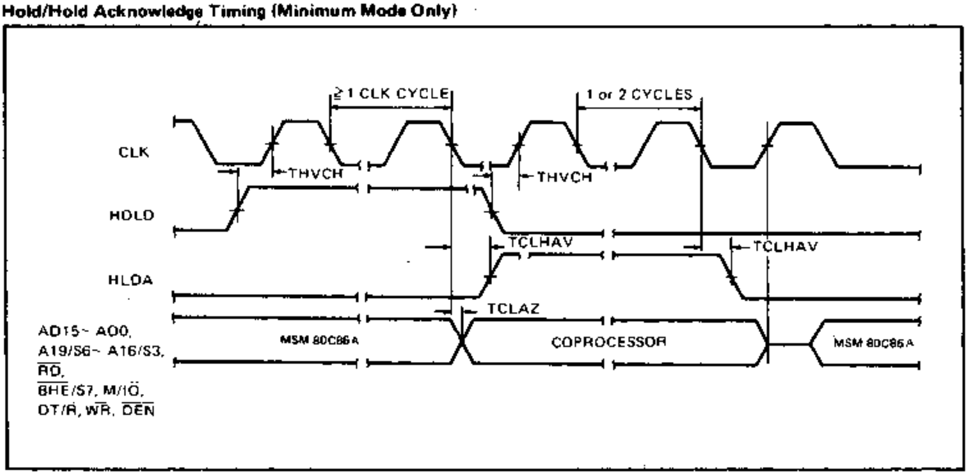
Reset Timing



Request/Grant Sequence Timing (Maximum Mode Only)



Hold/Hold Acknowledge Timing (Minimum Mode Only)



PIN DESCRIPTION

AD0 – AD15

ADDRESS DATA BUS: Input/Output

These lines are the multiplexed address and data bus.

These are the address bus at the T1 cycle and the data bus at the T2, T3, TW and T4 cycles.

At the T1 cycle, AD0 low indicates Data Bus Low (D0 – D7) Enable. These lines are high impedance during interrupt acknowledge and hold acknowledge.

A16/S3, A17/S4, A18/S5, A19/S6

ADDRESS/STATUS: Output

Tses are the four most significant addresses, at the T1 cycle. Accessing I/O port address, these are low at T1 cycles. These lines are Status lines at T2, T3, TW and T4 cycles. S3 and S4 are encoded as shown.

S3	S4	Characteristics
0	0	Alternate Data
1	0	Stack
0	1	Code or None
1	1	Data

These lines are high impedance during hold acknowledge.

$\overline{BHE}$/S7

BUS HIGH ENABLE/STATUS: Output

This line indicates Data Bus High Enable (BHE) at the T1 cycle.

This line indicates Data Bus High Enable (BHE) at the T1 cycles.

This line is status line at T2, T3, TW and T4 cycles.

$\overline{RD}$

READ: Output

This line indicates that CPU is in the memory or I/O read cycle.

This line is the read strobe signal when CPU read data from memory or I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

READY

READY: Input

This line indicates to the CPU that the addressed memory or I/O device is ready to read or write.

This line is active high.

If the setup and hold time is out of specification, illegal operation will occur.

INTR

INTERRUPT REQUEST: Input

This line is the level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulation.

It can be internally masked by software.

This signal is active high and internally synchronized.

$\overline{TEST}$

TEST: Input

This line is examined by the WAIT instruction.

When $\overline{TEST}$ is high, the CPU enters idle cycle.

When $\overline{TEST}$ is low, the CPU exits the idle cycle.

NMI

NON MASKABLE INTERRUPT: Input

This line causes a type 2 interrupt.

NMI is not maskable.

This signal is internally synchronized and needs 2 clock cycles of pulse width.

RESET

RESET: Input

This signal causes the CPU to initialize immediately.

This signal is active high and must be at least four clock cycles.

CLK

CLOCK: Input

This signal provides the basic timing for the internal circuit.

MN/$\overline{MX}$

MINIMUM/MAXIMUM: Input

This signal selects the CPU's operating mode.

When V_{CC} is connected, the CPU operates in Minimum mode.

Whin GND is connected, the CPU orerates Maximum mode.

V_{CC}

V_{CC}: +5V supplied.

GND

GROUND

The following pin function descriptions are maximum mode only.

Other pin functions are already described.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

STATUS: Output

These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals.

These lines are high impedance during hold acknowledge.

These status lines are encoded as shown.

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$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

$\overline{RQ}/\overline{GT0}$
$\overline{RQ}/\overline{GT1}$

REQUEST/GRANT: Input/Output

These lines are used for Bus Request from other devices and Bus GRANT to other deivces.

These lines are bidirectional and active low.

$\overline{LOCK}$

LOCK: Output

This line is active low.

When this line is low, other devices can not gain control of the bus.

This line is high impedance during hold acknowledge.

QS0/QS1

QUEUE STATUS: Output

These lines are Queue Status, and indicate internal instrucion queue status.

QS1	QS0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are minimum mode only. Other pin functions are already described.

M/$\overline{IO}$

STATUS: Output

This line selects memory address space or I/O address space.

When this line is high, the CPU selects memory address space and when it is low, the CPU selects I/O address space.

This line is high impedance during hold acknowledge.

$\overline{WR}$

WRITE: Output

This line indicates that the CPU is in the memory or I/O write cycle.

This line is a write strobe signal when the CPU writes data to memory or I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

$\overline{INTA}$

INTERRUPT ACKNOWLEDGE: Output

This line is a read strobe signal for the interrupt acknowledge cycle.

This line is active low.

ALE

ADDRESS LATCH ENABLE: Output

This line is used for latching the address into the MSM82C12 address latch, It is a possitive pulse and its trailing edge is used to strobe the address, This line is never floated.

DT/$\overline{R}$

DATA TRANSMIT/RECEIVE: Output

This line is used to control the output enable of the bus transceiver.

When this line is high, the CPU transmits data, and when it is low, the CPU receives data.

This line is high impedance during hold acknowledge.

$\overline{DEN}$

DATA ENABLE: Output

This line is used to control the output enable of the bus transceiver.

This line is active low. This line is high impedance during hold acknowledge.

HOLD

HOLD REQUEST: Input

This line is used for Bus Request from other devices.

This line is active high.

HLDA

HOLD ACKNOWLEDGE: Output

This line is used for Bus Grant to other devices.

This line is active high.

FUNCTIONAL DESCRIPTION

STATIC OPERATION

All MSM80C86A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C86A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C86A can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Sigle step clock operation allows simple interface circuitry to provice critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since MSM80C86A power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, MSM80C86A power requirement is the standby current (500 μA maximum).

GENERAL OPERATION

The internal function of the MSM80C86 consists of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. Instruction pre-fetch is perfomed while waiting for decording and execution of instructions. Thus, the CPU's performance is increased. Up to 6-bytes of instruction stream can be queued.

The EU receives pre-fetched instructions from the BIU queue, decodes and executes the instructions, and provides the un-relocated operand address to BIU.

MEMORY ORGANIZATION

The MSM80C86A has a 20-bit address to memory. Each address has an 8-bit data width. Memory is organized 00000H to FFFFFH and is logicaly divided into four segments: code, data, extra data and stack segment. Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)

All memory references are made relative to the segment register which functions in accordance with a select rule. Word operands can be located on even or odd address boundary.

The BIU automatically performs the proper number of memory accesses. Memory consists of an even address and an odd address. Byte data of even address is transfered on the D0 — D7 and byte data of odd address is transfered on the D8 — D15.

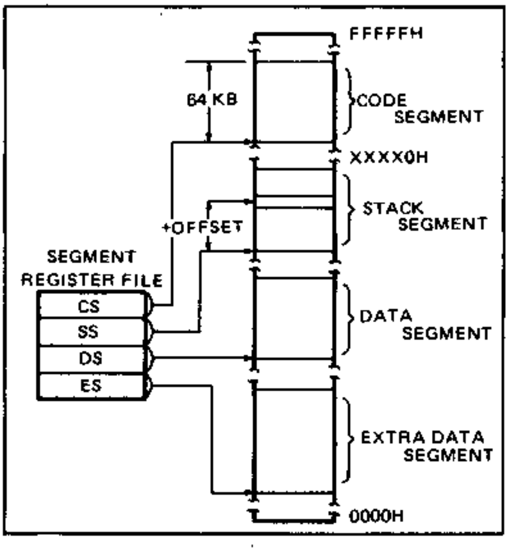
The CPU prevides two enable signals $\overline{BHE}$ and A0 to access either an odd address, even address or both:

Memory location FFFF0H is the start address after reset, and 00000H through 003FFH are reserved as an interrupt pointer, where there are 256 types of interrupt pointers.

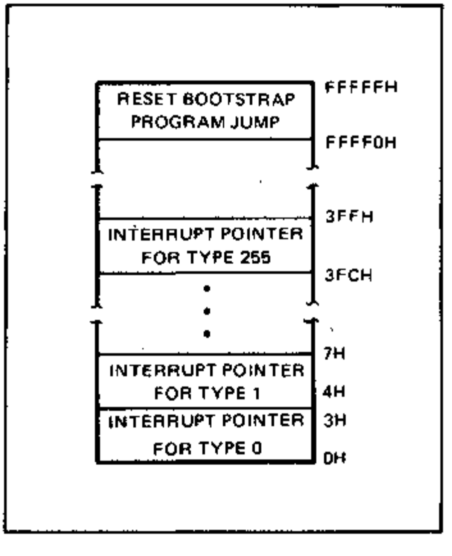
Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

5

Memory Organization



Reserved Memory Locations



Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment overriden.

MINIMUM AND MAXIMUM MODES

The MSM80C86A has two system modes: minimum and maximum. When using maximum mode, it is easy to organize a multi-CPU system with a 82C88 Bus Controller which generate the bus control signal.

When using minimum mode, it is easy to organize a simple system by generating bus control signal by itself.

MN/$\overline{MX}$ is the mode select pin. Definition of 24-31 pin changes depend on the MN/$\overline{MX}$ pin.

BUS OPERATION

The MSM80C86A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for a system, it is only to add the address latch.

A CPU bus cycle consists of at least four clock cycles: T1, T2 T3 and T4. (Fig. 4)

The address output occurs during T1 and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus at the read operation. When the device which is accessed by the CPU is not ready for The data transfer and the CPU "NOT READY", TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution. During the T1 cycle, the ALE signal is output from the CPU or the MSM82C88 depending on MN/$\overline{MX}$. At the trailing edge of ALE, a valid address may be latched.

Status bits $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ are used in the maximum mode by the bus controller to recognize the type of bus operation according to the following table.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are multiplexed with A16 ~ A19, and $\overline{BHE}$: therefore, they are valid during T2 through T4.

S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table.

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

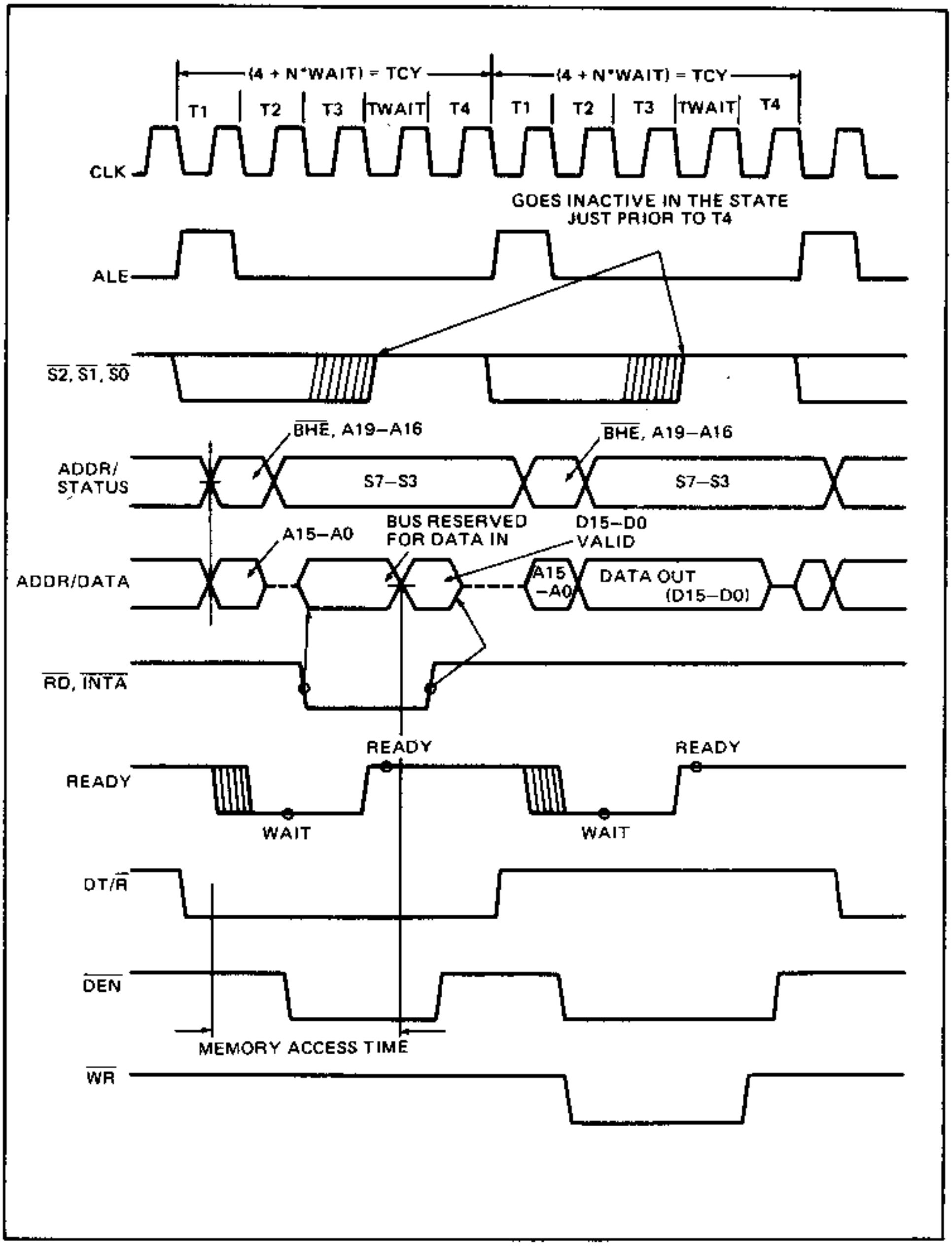
S5 indicates interrupt enable Flag.

I/O ADDRESSING

The MSM80C86A has 64 Kbyte of I/O or as 32 Kwords I/O. When the CPU accesses an I/O device, addresses AO ~ A15 are in the same format as a memory address, and A16 ~ A19 are low.

The I/O ports addresses are same as memory, so it is necessary to be careful when using 8-bit peripherals.

Basic System Timing



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EXTERNAL INTERFACE

RESET

CPU Initalization is executed by the RESET pin. The MSM80C86A's RESET High signal is required for greater than 4 clock cycles.

The Rising edge of RESET terminates present operation immediately. The Falling edge of RESET triggers an internal reset sequence for approximately 10 clock cycles. Afer the internal reset sequence is finished normal operation occurs from absolute location FFFF0H.

INTERRUPT OPERATIONS

Interrupt operation is classified as software or hardware, and hardware interrupt is classified as non-maskable or maskable.

An interrupt causes a new program location defined on the interrupt pointer table, according to the interrupt type. Absolute locations 00000H through 003FFH are reserved for the interrupt pointer table. The interrupt pointer table consists of 256-elements. Each element is 4 bytes in size and corresponds to an 8 bit type number which is sent from an interrupt interrupt request device during the interrupt acknowledge cycle.

NON-MASKABLE INTERRUPT (NMI)

The MSM80C86A has a Non-maskable Interrupt (NMI) which is of higher priority than the maskable interrupt request (INTR).

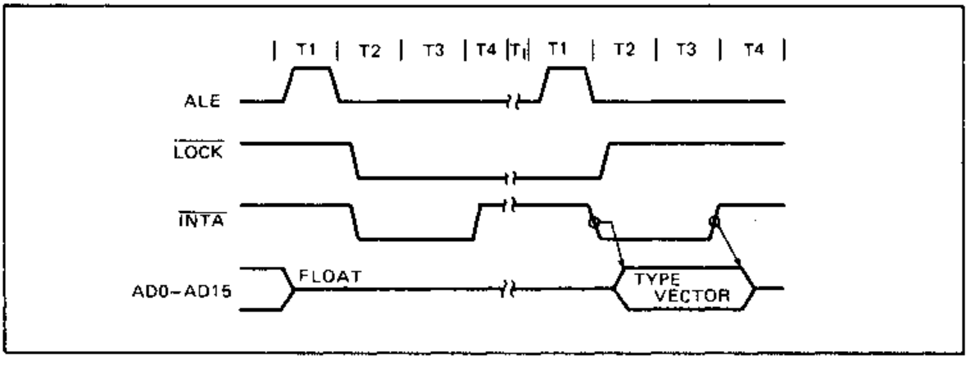
The NMI request pulse width needs a minimum of 2 clock cycles. The NMI will be serviced at the end of the current instruction or between string manipulations.

MASKABLE INTERRUPT (INTR)

The MSM80C86A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until the interrupt request is acknowledged.

INTR will be serviced at the end of the aurrent instruction or between string manipulations.

Interrupt Acknowledge Sequence



INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt, after which the Flag register is automatically pushed onto the stack. During the acknowledge sequence, the CPU emits the lock signal from T2 of the first bus cycle to T2 of the second bus cycle. At second bus cyclees, byte is fetched from the external device as a vector which identified the type of interrupt. This vector is multiplied by four and used as a interrupt pointer address. (INTR only)

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

HALT

When a Halt instruction is executed, the CPU enters the Halt state. An interrupt request or RESET will force the MSM80C86A out of the Halt state.

SYSTEM TIMING — MINIMUM MODE

A bus cycle begins T1 with an ALE signal. The trailing edge of ALE is used to latch the address. From T1 to T4 the M/$\overline{IO}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to data bus.

The read ($\overline{RD}$), write ($\overline{WR}$) and interrupt acknowledge ($\overline{INTA}$) signals causes the addressed device to enable data bus. These signal becomes active at the beginning of T2 and inactive at the beginning of T4.

SYSTEM TIMING — MAXIMUM MODE

At maximum mode, the MSM82C88 Bus Controller is added to system. The CPU sends status information to the Bus Controller. Bus timing signals are generated by Bus Controller. Bus timing is almost the same as in the minimum mode.

BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on MSM80C86A pins 2—16, 26—32, and 34—39 (Figures 6a, 6b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 600 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

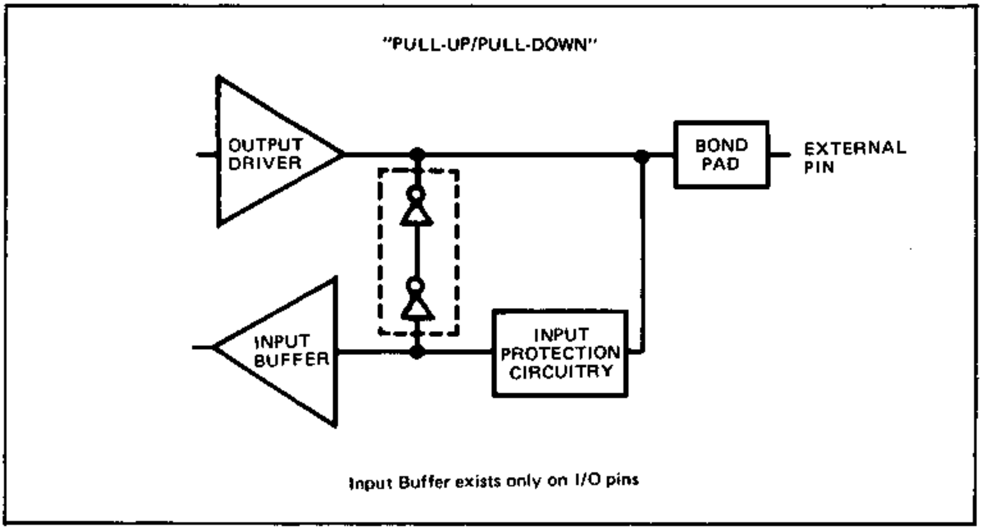


Figure 6a. Bus hold circuitry pin 2-16, 35-39.

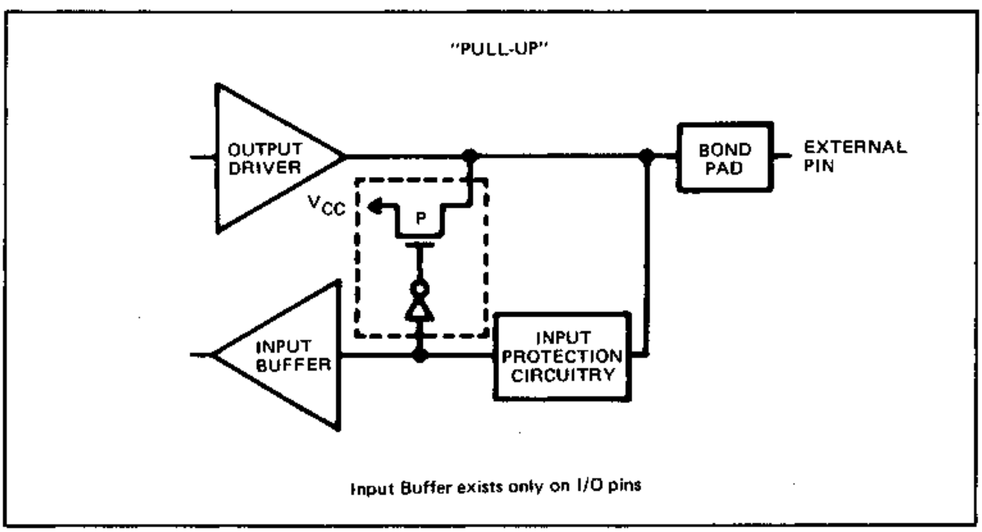


Figure 6b. Bus hold circuitry pin 26-32, 34

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DATA TRANSFER

MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate to register	1 0 1 1 w reg	data	data if w = 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with borrow:				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1			

DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD = Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate left through carry	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate right through carry	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w			

CJMP = Conditional JMP				
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp		
JZ/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp		
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp		
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp		
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp		
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp		
JO = Jump on over flow	0 1 1 1 0 0 0 0	disp		
JS = Jump on sign	0 1 1 1 1 0 0 0	disp		
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp		
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp		
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp		
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp		
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp		
JNP/JPO = Jump on not parity/parity odd	0 1 1 1 1 0 1 1	disp		
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp		
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp		
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp		
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp		
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp		
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp		
INT = Interrupt:				
Type specified	1 1 0 0 1 1 0 1	type		
Type 3	1 1 0 0 1 1 0 0			
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0			
IRET = Interrupt return	1 1 0 0 1 1 1 1			

PROCESSOR CONTROL

CLC = Clear carry	1 1 1 1 1 0 0 0			
CMC = Complement carry	1 1 1 1 0 1 0 1			
STC = Set carry	1 1 1 1 1 0 0 1			
CLD = Clear direction	1 1 1 1 1 1 0 0			
STD = Set direction	1 1 1 1 1 1 0 1			
CLI = Clear interrupt	1 1 1 1 1 0 1 0			
STI = Set interrupt	1 1 1 1 1 0 1 1			
HLT = Halt	1 1 1 1 0 1 0 0			
WAIT = Wait	1 0 0 1 1 0 1 1			
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m		
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0			

CONTROL TRANSFER

CALL = Call:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct within segment-short	1 1 1 0 1 0 1 1	disp		
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within segment	1 1 0 0 0 0 1 1			
Within seg. adding immediate to SP	1 1 0 0 0 0 1 0	data-low	data-high	
Intersegment	1 1 0 0 1 0 1 1			
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	

Footnotes:

AL = 8-bit accumulator
AX = 18-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed value
If d = 1 then "to" reg: If d = 0 then "from" reg.
If w = 1 then word instruction: If w = 0 then byte instruction

If mod = 11 then r/m is treated as a REG field
If mod = 00 then DISP = 0*, disp-low and disp-high are absent
If mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
If mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
If r/m = 001 then EA = (BX) + (DI) + DISP
If r/m = 010 then EA = (BP) + (SI) + DISP
If r/m = 011 then EA = (BP) + (DI) + DISP
If r/m = 100 then EA = (SI) + DISP
If r/m = 101 then EA = (DI) + DISP
If r/m = 110 then EA = (BP) + DISP*
If r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
* except if mod = 00 and r/m = 110 then EA-disp-high: disp-low

If s:w = 01 then 16 bits of immediate data form the operand
If s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
If v = 0 then "count" = 1: If v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit	(w = 1)	8-Bit	(w = 0)	Segment
000	AX	000	AL	00 ES
001	CX	001	CL	01 CS
010	DX	010	DL	10 SS
011	BX	011	BL	11 DS
100	SP	100	AH	
101	BP	101	CH	
110	SI	110	DH	
111	DI	111	BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = x:x:x:x:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

OKI semiconductor

MSM80C88ARS/GS/JS
MSM80C88A-2RS/GS/JS

8-BIT CMOS MICROPROCESSOR

GENERAL DESCRIPTION

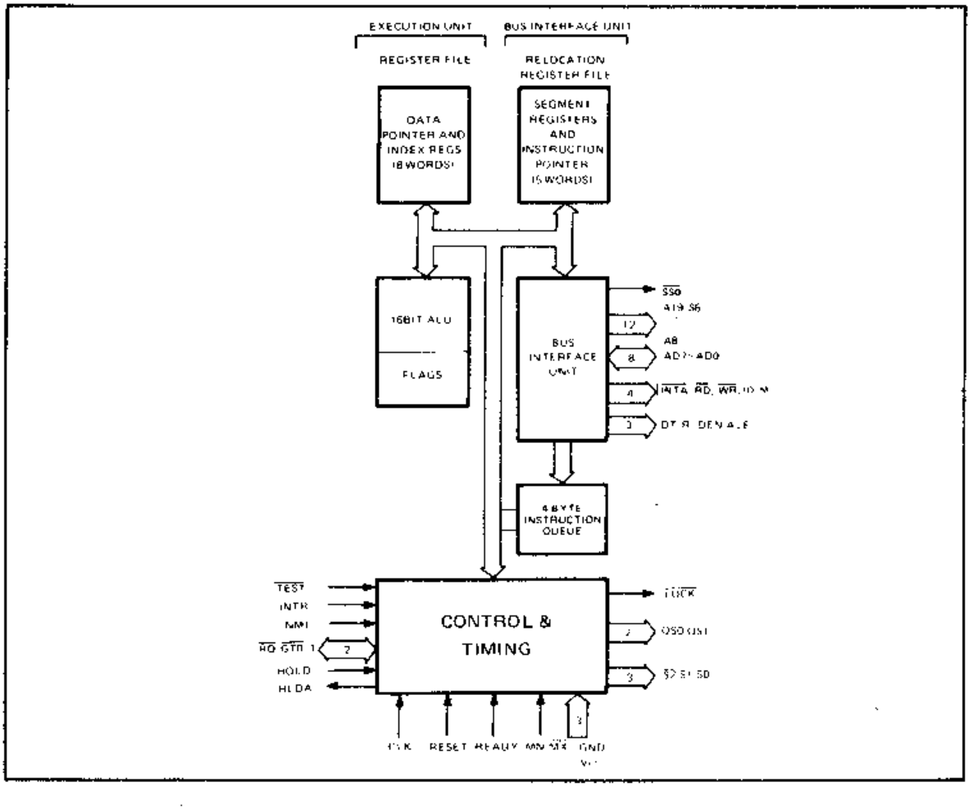
The MSM80C88A/MSM80C88A-2 are internal 16-bit CPUs with 8-bit interface implemented in Silicon Gate CMOS technology. They are designed with the same processing speed as the NMOS 8088/8088-2, but with considerably less power consumption.

The processor has attributes of both 8 and 16-bit microprocessor. It is directly compatible with MSM80C86A/MSM80C86A-2 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

FEATURES

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- 1 Mbyte Direct Addressable Memory Space
- Software Compatible with MSM80C86A
- Internal 14 Word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 5 MHz Clock Rate (MSM80C88A)
- From DC to 8 MHz Clock Rate (MSM 80C88A-2)
- Low Power Dissipation (10 mA/MHz)
- Bus Hold Circuitry Eliminates Pull-Up Resistors

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION

MSM80C88ARS (Top View)
MSM80C88A-2RS
40 Lead Plastic DIP

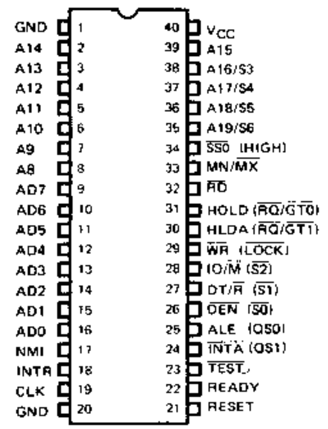


Fig. 2a MSM80C88AGS/MSM80C88A-2GS

MSM80C88AGS (Top View)
MSM80C88A-2GS
56-Lead Plastic Flat Package

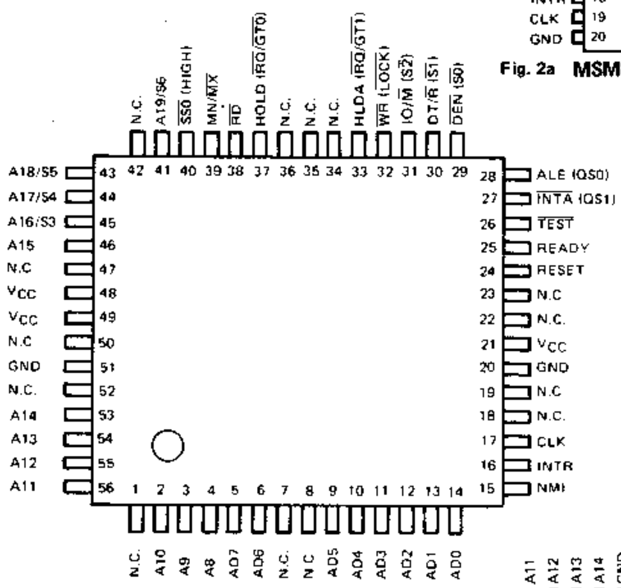
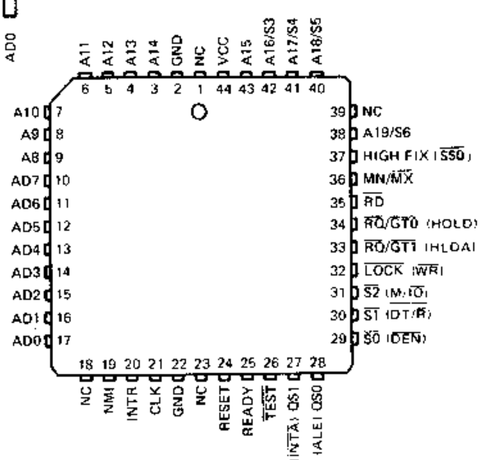


Fig. 2b MSM80C88AGS/MSM80C88A-2GS

MSM80C88AJS (Top View)
MSM80C88A-2JS
44 Pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits			Unit	Conditions
		MSM80C88ARS MSM80C88A-2RS	MSM80C88AGS MSM80C88A-2GS	MSM80C88AJS MSM80C88A-2JS		
Power Supply Voltage	V_{CC}	-0.5 ~ +7			V	With respect to GND
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5			V	
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5			V	
Storage Temperature	Tstg	-65 ~ +150			°C	–
Power Dissipation	P_D	1.0	0.7		W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits		Unit
		MSM80C88A	MSM80C88A-2	
Power Supply Voltage	V_{CC}	3 ~ 6	4.75 ~ 5.25	V
Operating Temperature	T_{OP}	-40 ~ +85	0 ~ +70	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MSM80C88A			MSM80C88A-2			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	-40	+25	+85	0	+25	+70	°C
"L" Input Voltage	V_{IL}	-0.5		+0.8	-0.5		+0.8	V
"H" Input Voltage	V_{IH} (*1)	V_{CC}-0.8		V_{CC} +0.5	V_{CC}-0.8		V_{CC} +0.5	V
	V_{IH} (*2)	2.0		V_{CC} +0.5	2.0		V_{CC} +0.5	V

*1 Only CLK, *2 Except CLK,

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DC CHARACTERISTICS

(MSM80C86A: V_{CC} = 4.5V to 5.5V, Ta = −40° to +85°C)
(MSM80C88A-2: V_{CC} = 4.75 to 5.25V, Ta = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
"L" Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.0			V	I_{OH} = −2.5 mA
		V_{CC}−0.4				I_{OH} = −100μA
Input Leak Current	I_{LI}	−1.0		+1.0	μA	$0 < V_I < V_{CC}$
Output Leak Current	I_{LO}	−10		+10	μA	$V_O = V_{CC}$ or GND
Input Leakage Current (Bus Hold Low)	I_{BHL}	50		400	μA	V_{IN} = 0.8V *3
Input Leakage Current (Bus Hold High)	I_{BHH}	−50		−400	μA	V_{IN} = 3.0V *4
Bus Hold Low Overdrive	I_{BHLO}			600	μA	*5
Bus Hold High Overdrive	I_{BHHO}			−600	μA	*6
Operating Power Supply Current	I_{CC}			10	mA/MHz	V_{IL}=GND V_{IH}=V_{CC}
StandbySupply Current	I_{CCS}			500	μA	V_{IN}=V_{CC} or GND Outputs Unloaded CLK=GND or V_{CC}
Input Capacitance	C_{in}			5	pF	*7
Output Capacitance	C_{out}			15	pF	*7
I/O Capacitance	$C_{I/O}$			20	pF	*7

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*3. Test conditions is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2–16 and 35–39.
*4. Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2–16, 26–32, and 34–39.
*5. An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
*6. An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.
*7. Test Conditions: a) Freq = 1 MHz.
b) Unmeasured Pins at GND.
c) V_{IN} at 5.0V or GND.

A.C. CHARACTERISTICS

(MSM80C88A: V_{CC} = 4.5V to 5.5V, Ta = –40°C to +85°C)
(MSM80C88A-2: V_{CC} = 4.75V to 5.25V, Ta = 0°C to 70°C)

Minimum Mode System

Timing Requirements

Parameter	Symbol	MSM80C88A		MSM80C88A-2		Unit
		Min.	Max.	Min.	Max.	
CLK Cycle Period	TCLCL	200	DC	125	DC	ns
CLK Low Time	TCLCH	118		68		ns
CLK High Time	TCHCL	69		44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10		10	ns
Data in Setup Time	TDVCL	30		20		ns
Data in Hold Time	TCLDX	10		10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		0		ns
READY Setup Time into MSM 80C88A	TRYHCH	118		68		ns
READY Hold Time into MSM 80C88A	TCHRYX	30		20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		-8		ns
HOLD Setup Time	THVCH	35		20		ns
INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	TINVCH	30		15		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15		15	ns

5

Timing Responses

Parameter	Symbol	MSM80C88A		MSM80C88A-2		Unit
		Min.	Max.	Min.	Max.	
Address Valid Delay	TCLAV	10	110	10	60	ns
Address Hold Time	TCLAX	10		10		ns
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns
ALE Width	TLHLL	TCLCH-20		TCLCH-10		ns
ALE Active Delay	TCLLH		80		50	ns
ALE Inactive Delay	TCHLL		85		55	ns
Address Hold Time to ALE Inactive	TLLAX	TCHCL-10		TCHCL-10		ns
Data Valid Delay	TCLDV	10	110	10	60	ns
Data Hold Time	TCHDX	10		10		ns
Data Hold Time after $\overline{\text{WR}}$	TWHDX	TCLCH-30		TCLCH-30		ns
Control Active Delay 1	TCVCTV	10	110	10	70	ns
Control Active Delay 2	TCHCTV	10	110	10	60	ns
Control Inactive Delay	TCVCTX	10	110	10	70	ns
Address Float to $\overline{\text{RD}}$ Active	TAZRL	0		0		ns
$\overline{\text{RD}}$ Acrive Delay	TCLRL	10	165	10	100	ns

Parameter	Symbol	MSM80C88A		MSM80C88A-2		Unit
		Min.	Max.	Min.	Max.	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns
HLDA Valid Delay	TCLHAV	10	160	10	100	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-75		2TCLCL-50		ns
$\overline{WR}$ Width	TWLWH	2TCLCL-60		2TCLCL-40		ns
Address Valid to ALE Low	TAVAL	TCLCH-60		TCLCH-40		ns
Output Rise Time (From 0.8V to 2.0)	TOLOH		15		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15		15	ns

Notes: 1. Signals at MSM82C84A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3)

Maximum Mode System (Using MSM 82C88 Bus Controller)
Timing Requirements

Parameter	Symbol	MSM80C88A		MSM80C88A-2		Unit
		Min.	Max.	Min.	Max.	
CLK Cycle Period	TCLCL	200	DC	125	DC	ns
CLK Low Time	TCLCH	118		68		ns
CLK High Time	TCHCL	69		44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10		10	ns
Data in Setup Time	TDVCL	30		20		ns
Data in Hold Time	TCLDX	10		10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		0		ns
READY Setup Time into MSM 80C88A	TRYHCH	118		68		ns
READY Hold Time into MSM 80C88A	TCHRYX	30		20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		-8		ns
Set up Time for Recognition (NMI, INTR, $\overline{TEST}$) (See Note 2)	TINVCH	30		15		ns
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	30		15		ns
$\overline{RQ}$ Hold Time into MSM 80C88A	TCHGX	40		30		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15		15	ns

5

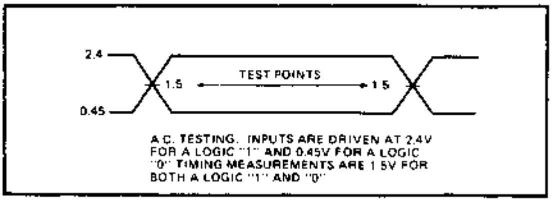
Timing Responses

Parameter	Symbol	MSM80C88A		MSM80C88A-2		Unit
		Min.	Max.	Min.	Max.	
Command Active Delay (See Note 1)	TCLML	5	45	5	35	ns
Command Inactive Delay (See Note 1)	TCLMH	5	45	5	45	ns
READY Active to Status Passive (See Note 4)	TRYHSH		110		65	ns
Status Active Delay	TCHSV	10	110	10	60	ns
Status Inactive Delay	TCLSH	10	130	10	70	ns
Address Valid Delay	TCLAV	10	110	10	60	ns
Address Hold Time'	TCLAX	10		10		ns
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns
Status Valid to ALE High (See Note 1)	TSVLH		35		25	ns
Status Valid to MCE High (See Note 1)	TSVMCH		35		30	ns
CLK low to ALE Valid (See Note 1)	TCLLH		35		25	ns
CLK Low to MCE High (See Note 1)	TCLMCH		35		25	ns
ALE Inactive Delay (See Note 1)	TCHLL	4	35	4	25	ns
Data Valid Delay	TCLDV	10	110	10	60	ns
Data Hold Time	TCHDX	10		10		ns
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns
Control Inactive Delay (See Note 1)	TCVNX	5	45	5	45	ns
Address Float to $\overline{RD}$ Active	TAZRL	0		0		ns
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns
Direction Control Inactive Delay (See Note 1)	TCHDTH		35		30	ns
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-75		2TCLCL-50		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15		15	ns

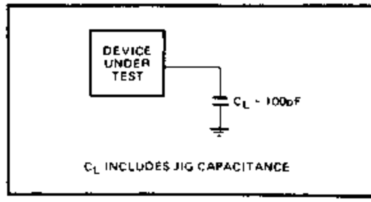
Notes:
1. Signals at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3)
4. Applies only to T3 and wait states.

5

A.C. TESTING INPUT, OUTPUT WAVEFORM

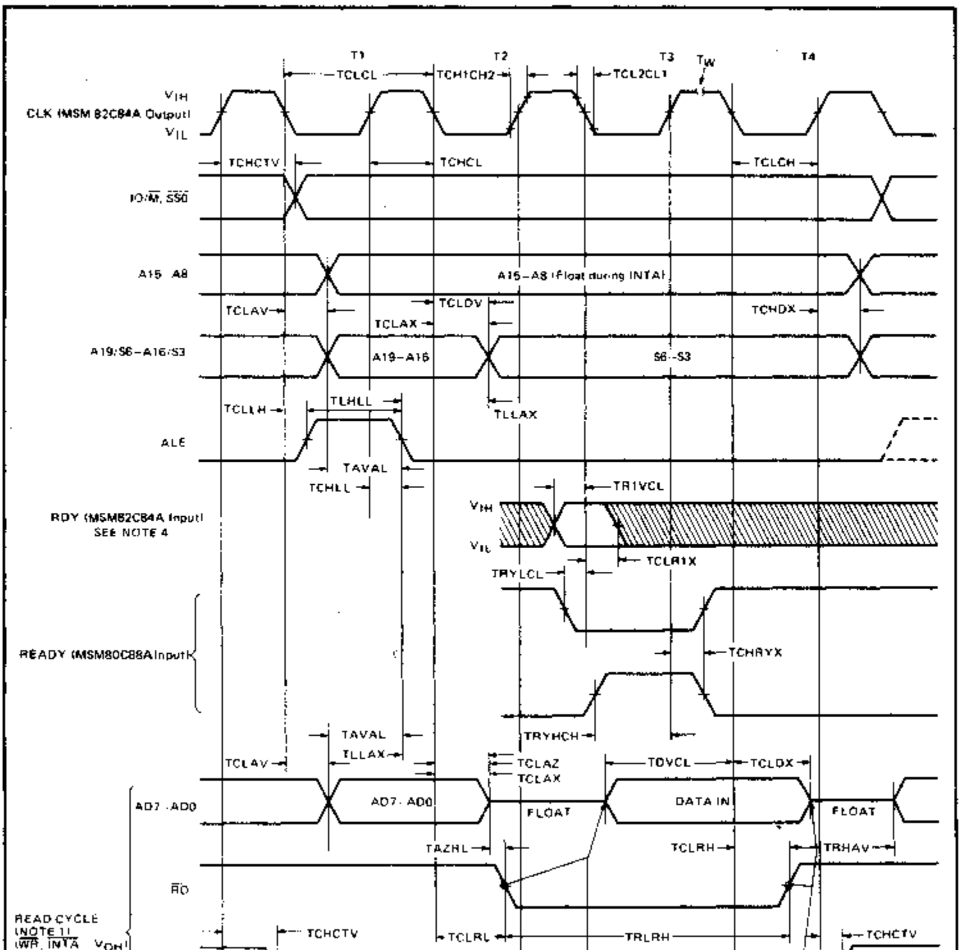


A.C. TESTING LOAD CIRCUIT



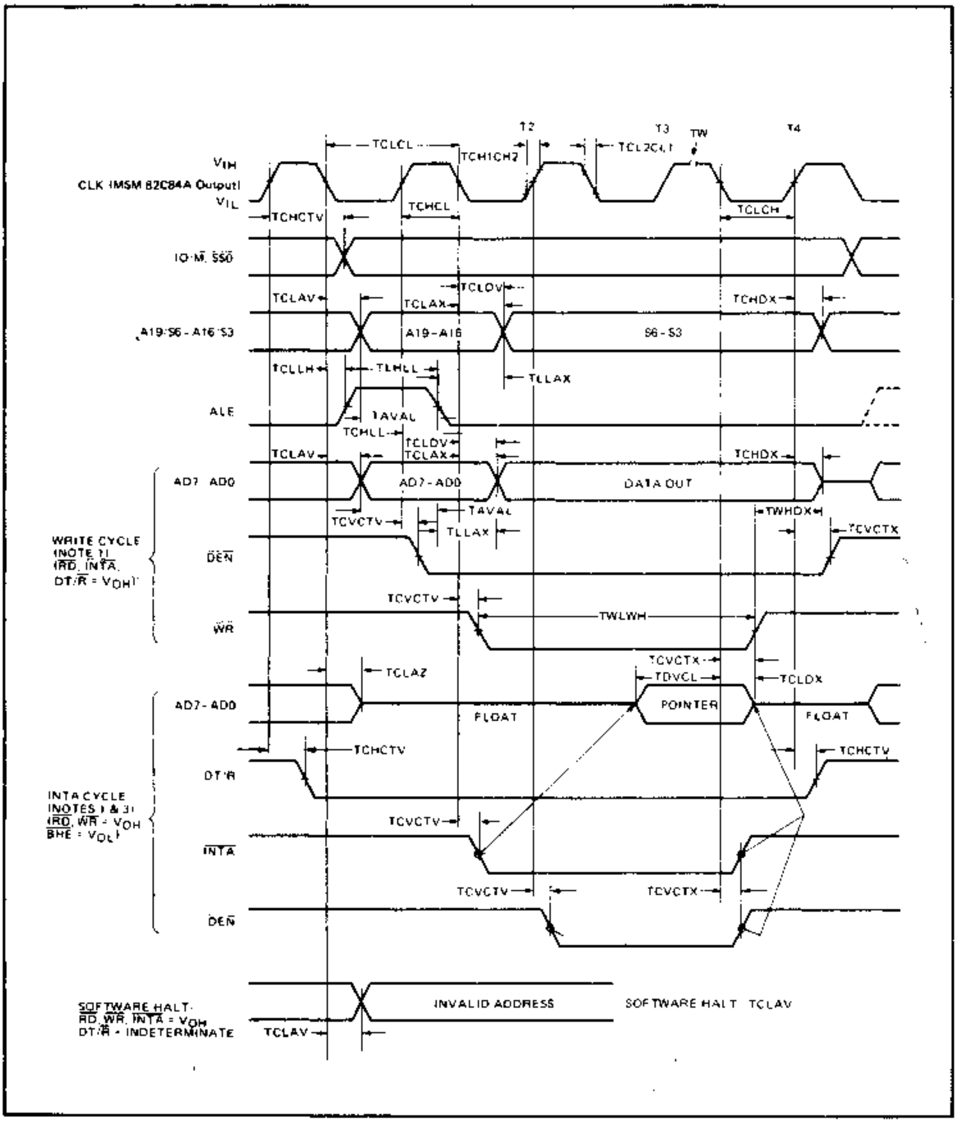
TIMING CHART

Minimum Mode



5

Minimum Mode (Continued)

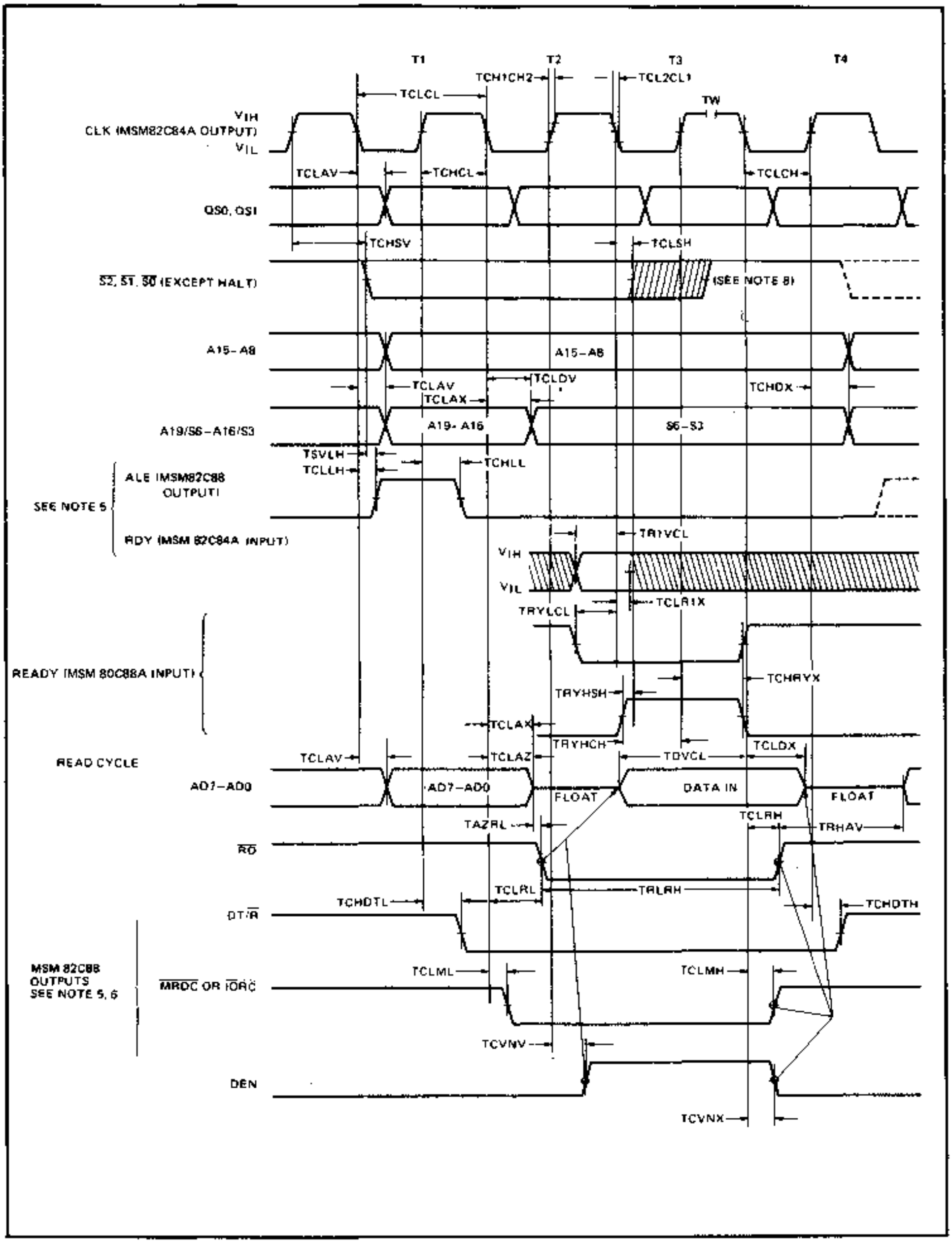


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two INTA cycles run back-to-back. The MSM80C88A LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at MSM 82C84A shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

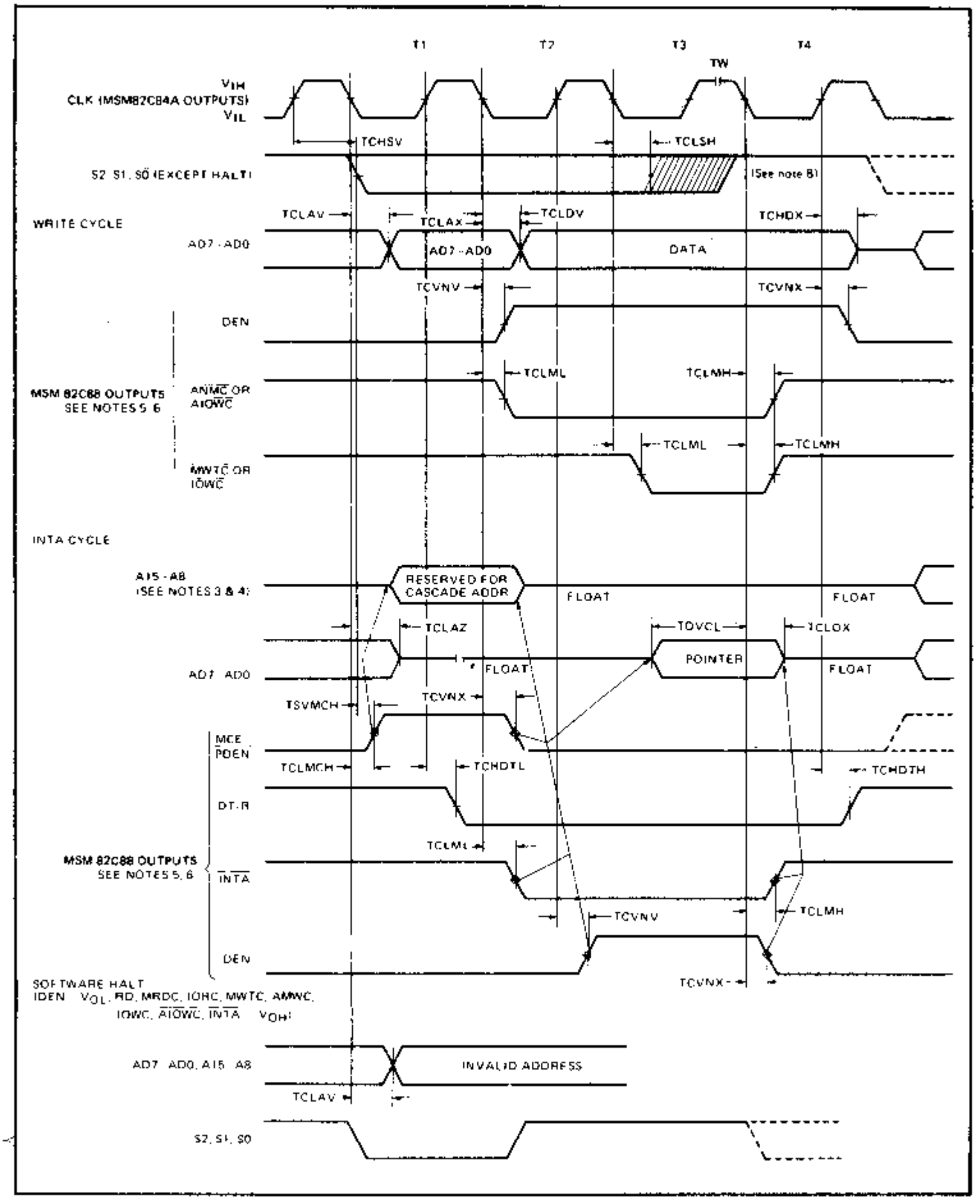
5

Maximum Mode



5

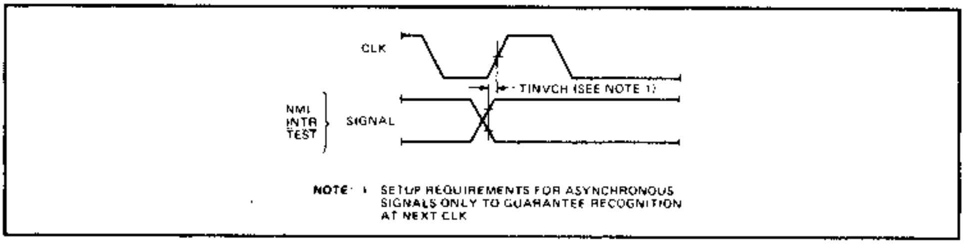
Maximum Mode (Continued)



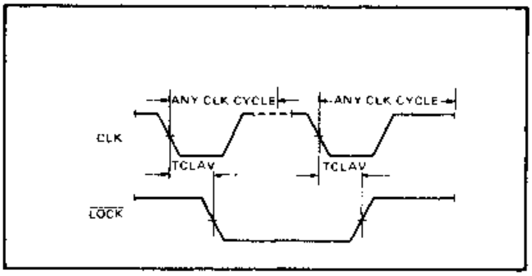
NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted
3. Cascade address is valid between first and second INTA cycle
4. Two INTA cycles run back to-back. The MSM 80C88A LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle
5. Signal at MSM 82C84A and MSM82C88 shown for reference only
6. The issuance of the MSM 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high MSM 82C88 CEN
7. All timing measurements are made at 1.5V unless otherwise noted
8. Status inactive in state just prior to T4

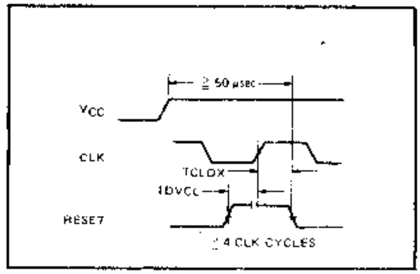
Asynchronous Signal Recognition



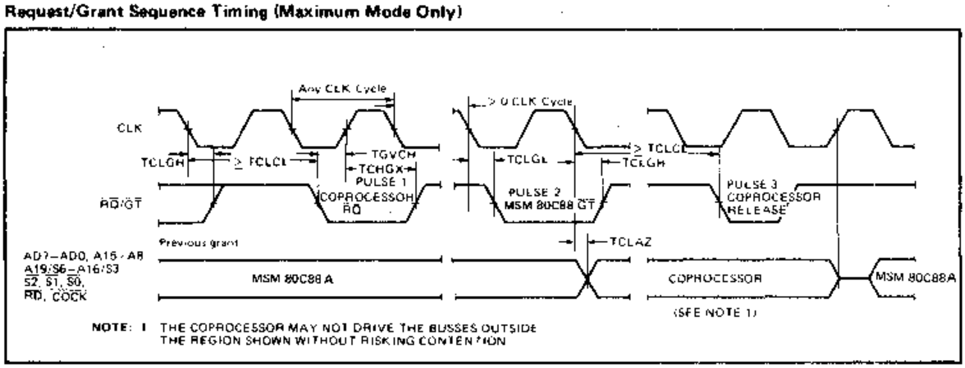
Bus Lock Signal Timing (Maximum Mode Only)



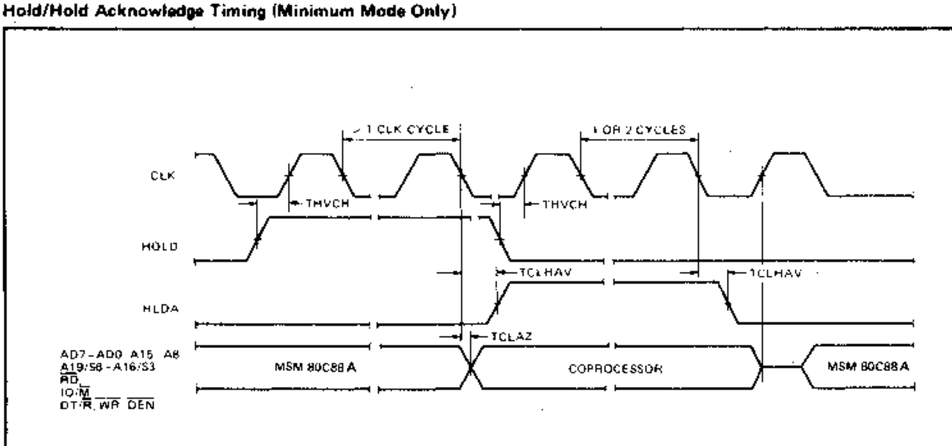
Reset Timing



Request/Grant Sequence Timing (Maximum Mode Only)



Hold/Hold Acknowledge Timing (Minimum Mode Only)



PIN DESCRIPTION

AD0–AD7

ADDRESS DATA BUS: Input/Output

These lines are the multiplexed address and data bus.
These are the address bus at T,1 cycle and the data bus at T2, T3, TW and T4 cycle.
T2, T3, TW and T4 cycle.
These lines are high impedance during interrupt acknowledge and hold acknowledge.

A8–A15

ADDRESS BUS: Output

These lines are the address bus bits 8 thru 15 at all cycles.
These lines do not have to be latched by an ALE signal.
These lines are high impedance during interrupt acknowledge and hold acknowledge.

A16/S3, A17/S4, A18/S5, A19/S6

ADDRESS/STATUS: Output

These are the four most significant address as at the T1, cycle.
Accessing I/O port address, these are low at T1 Cycles.
These lines are Status lines at the T2, T3, TW and T4 Cycle.
S5 indicate interrupt enable Flag.
S3 and S4 are encoded as shown.

S3	S4	Characteristics
0	0	Alternate Data
1	0	Stack
0	1	Code or None
1	1	Data

These lines are high impedance during hold acknowledge.

$\overline{RD}$

READ: Output

This lines indicates that the CPU is in a memory or I/O read cycle.
This line is the read strobe signal when the CPU reads data from a memory or I/O device.
This line is active low.
This line is high impedance during hold acknowledge.

READY

READY: Input

This line indicates to the CPU that an addressed memory or I/O device is ready to read or write.
This line is active high.
IF the setup and hold time are outof specification, an illegal operation will occur.

INTR

INTERRUPT REQUEST: Input

This line is a level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulations.
It can be internally masked by software.
This signal is active high and internally synchronized.

$\overline{TEST}$

TEST: Input

This line is examined by a "WAIT" instruction.
When $\overline{TEST}$ is high, the CPU enters an idle cycle.
When $\overline{TEST}$ is low, the CPU exits an idle cycle.

NMI

NON MASKABLE INTERRUPT: Input

This line causes a type 2 interrupt.
NMI is not maskable.
This signal is internally synchronized and needs a 2 clock cycle pulse width.

RESET

RESET: Input

This signal causes the CPU to initialize immediately.
This signal is active high and must be at least four clock cycles.

CLK

CLOCK: Input

This signal provide the basic timing for an internal circuit.

MN/$\overline{MX}$

MINIMUM/MAXIMUM: Input

This signal selects the CPU's operate mode.
When V_{CC} is connected, the CPU operates in minimum mode.
When GND is connected, the CPU operates in maximum mode.

V_{CC}

V_{CC} +3 – +6 V supplied.

GND

GROUND

The following pin function descriptions are for maximum mode only.
Other pin functions are already described.

5

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

STATUS: Output

These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals.

These lines are high impedance during hold acknowledge.

These status lines are encoded as shown.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

$\overline{RQ}/\overline{GT0}$
$\overline{RQ}/\overline{GT1}$

REQUEST/GRANT: Input/Output

These lines are used for Bus Request from other devices and Bus GRANT to other devices.

These lines are bidirectional and active low.

$\overline{LOCK}$

LOCK: Output

This line is active low.

When this line is low, other devices can not gain control of the bus.

This line is high impedance during hold acknowledge.

QS0/QS1

QUEUE STATUS: Output

These are Queue Status Lines that indicate internal instruction queue status.

QS1	QS0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are minimum mode only. Other pin functions are already described.

IO/$\overline{M}$

STATUS: Output

This line selects memory address space or I/O address space.

When this line is low, the CPU selects memory address space and when it is high, the CPU selects I/O address space.

This line is high impedance during hold acknowledge.

$\overline{WR}$

WRITE: Output

This line indicates that the CPU is in a memory or I/O write cycle.

This line is a write strobe signal when the CPU writes data to memory or an I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

$\overline{INTA}$

INTERRUPT ACKNOWLEDGE: Output

This line is a read strobe signal for the interrupt accknowledge cycle.

This line is active low.

ALE

ADDRESS LATCH ENABLE: Output

This line is used for latching an address into the MSM82C12 address latch it is a positive pulse and the trailing edge is used to strobe the address. This line in never floated.

DT/$\overline{R}$

DATA TRANSMIT/RECEIVE: Output

This line is used to control the direction of the bus transceiver.

When this line is high, the CPU transmits data, and when it is low, the CPU receive data.

This line is high impedance during hold acknowledge.

$\overline{DEN}$

DATA ENABLE: Output

This line is used to control the output enable of the bus transceiver.

This line is active low. This line is high impedance during hold acknowledge.

HOLD

HOLD REQUEST: Input

This line is used for a Bus Request from an other device.

This line is active high.

HLDA

HOLD ACKNOWLEDGE: Output

This line is used for a Bus Grant to an other device.

This line is active high.

$\overline{SS0}$

STATUS: Output

This line is logically equivalent to $\overline{S0}$ in the maximum mode.

STATIC OPERATION

All MSM80C88A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C88A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C88A can be signal stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C88A power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the MSM80C88A power requirement is the standby current (500 μA maximum).

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal function of the MSM80C88A consist of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

The BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. By performing instruction prefetch while waiting for decoding and execution of instruction, the CPU's performance is increased. Up to 4-bytes fo instruction stream can be queued.

EU receives pre-fetched instructions from the BIU queue, decodes and executes instructions and provides an un-relocated operand address to the BIU.

MEMORY ORGANIZATION

The MSM80C88A has a 20-bit address to memory. Each address has 8-bit data width. Memory is organized 00000H to FFFFFH and is logically divided into four segments: code, data, extra data and stack segment. Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)

All memory references are made relative to a segment register according to a select rule. Memory location FFFF0H is the start address after reset, and 00000H through 003FFH are reserved as an interrupt pointer. There are 256 types of interrupt pointer;

Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

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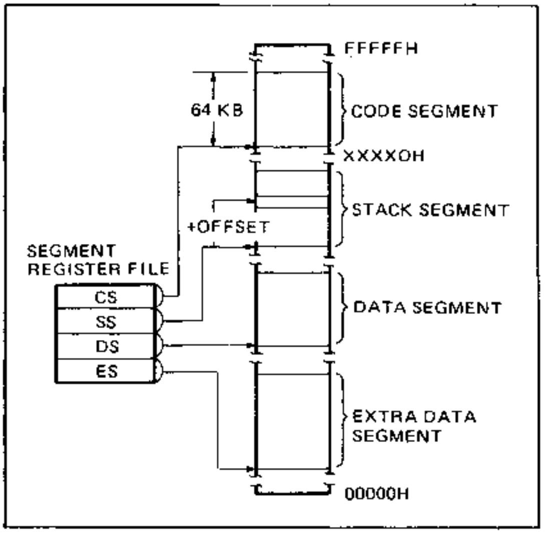
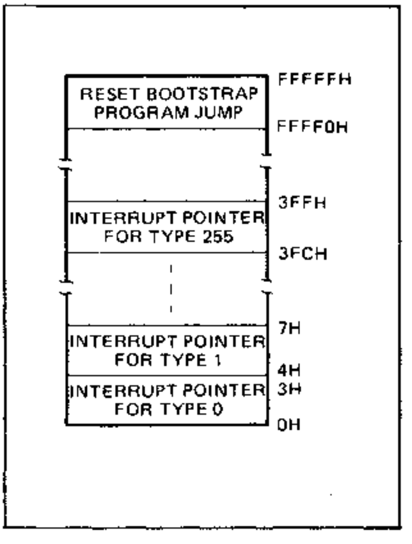
Memory Organization



Reserved Memory Locations



Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

MINIMUM AND MAXIMUM MODES

The MSM80C88A has two system modes: minimum and maximum. When using the maximum mode, it is easy to organize a multiple-CPU system with the MSM 82C88 Bus Controller which generates the bus control signal.

When using the minimum mode, it is easy to organize a simple system by generating the bus control signal itself. MN/$\overline{MX}$ is the mode select pin. Definition of 24–31, 34 pin changes depends on the MN/MX pin.

BUS OPERATION

The MSM80C88A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for the system, it is only needed to add the address latch.

A CPU bus cycle consists of at least four clock cycles: T1, T2, T3 and T4. (Fig. 4)

The address output occurs during T1, and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus during read operation. When the device which is accessed by the CPU is not ready to data transfer and send to the CPU "NOT READY" is indicated TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution. At the T1 cycle an ALE signal is output from the CPU or the MSM82C88 depending in MN/$\overline{MX}$. at the trailing edge of an ALE, a valid address may be latched. Status bits S0, S1 and S2 are uased, in maximum mode, by the bus controller to recognize the type of bus operation according to the following table.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bit S3 through S6 are multiplexed with A16–A19, and therefore they are valid during T2 through T4. S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table.

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra Segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

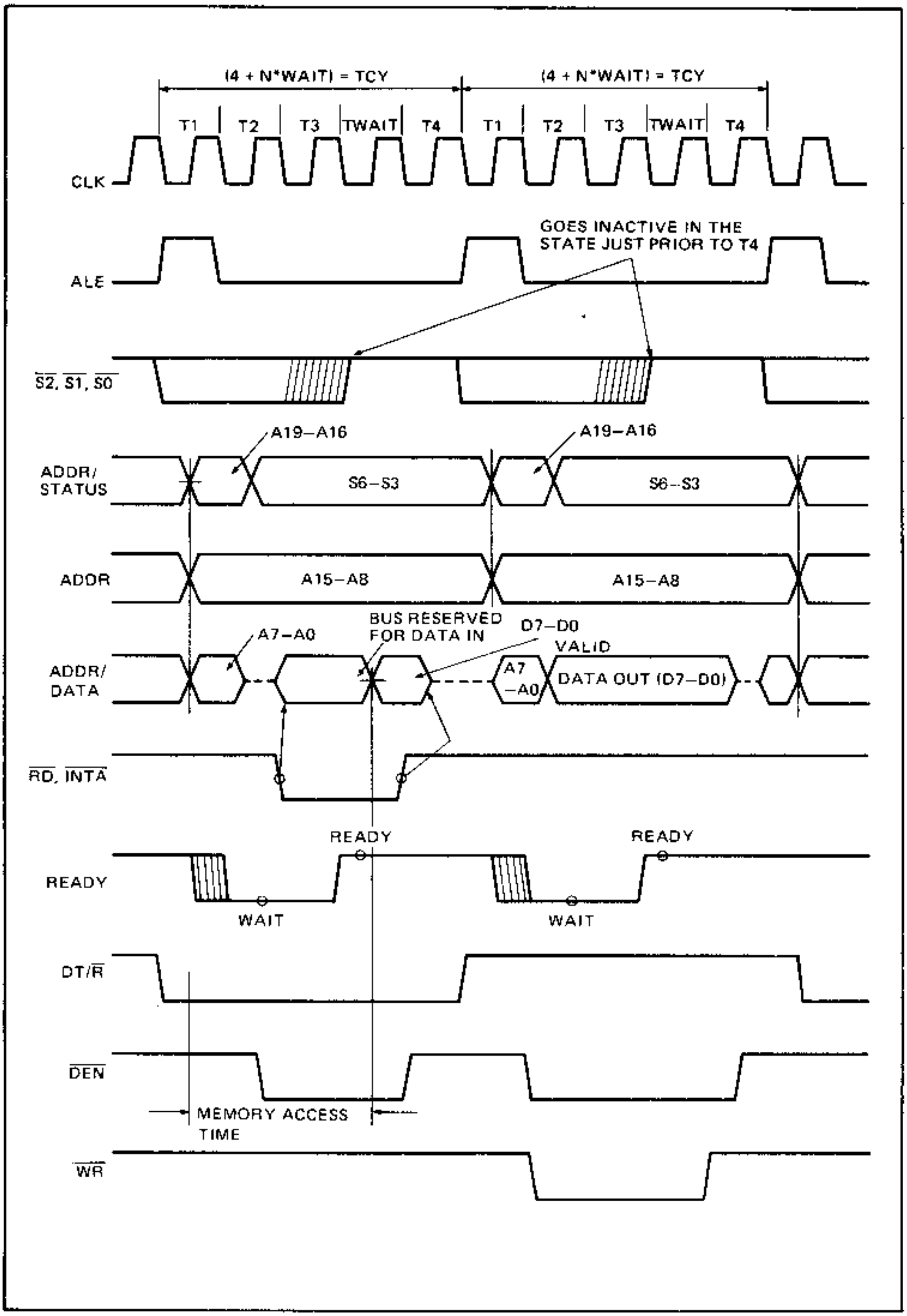
S5 indicates interrupt enable Flag.

I/O ADDRESSING

The MSM80C88A has a 64 Kbyte I/O. When the CPU accesses an I/O device, address A0–A15 are in same format as a memory access, and A16–A19 are low.

I/O ports address are same as four memory.

Basic System Timing



EXTERNAL INTERFACE

RESET

CPU initialization is executed by the RESET pin. The MSM80C88A's RESET High signal is required for greater than 4 clock cycles.

The rising edge of RESET terminates the present operation immediately. The falling edge of RESET triggers an internal reset requence for approximately 10 clock cycles. After internal reset sequence is finished, normal operation begins from absolute location FFFF0H.

INTERRUPT OPERATIONS

The interrupt operation is classified as software or hardware, and hardware interrupt is classified as non-markable or maskable.

An interrupt causes a new program location which is defined by the interrupt pointer table, according to the interrupt type. Absolute location 00000H through 003FFH is reserved for the interrupt pointer table. The interrupt pointer table consists of 256-elements. Each element is 4 bytes in size and corresponds to an 8-bit type number which is sent from an interrupt request device during the interrupt acknowledge cycle.

NON-MASKABLE INTERRUPT (NMI)

The MSM80C88A has a non-maskable Interrupt (NM1) which is of higher priority than a maskable interrupt request (INTR).

An NM1 request pulse width needs minimum of 2 clock cycles. The NM1 will be serviced at the end of the current instruction or between string manipulations.

MASKABLE INTERRUPT (INTR)

The MSM80C88A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until interrupt request is acknowledged.

The INTR will be serviced at the end of the current instruction or between string manipulations.

INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt, after which the Flag register is automatically pushed onto the stack. During an acknowledge sequence, the CPU emits the lock signal from T2 of first bus cycle to T2 of second bus cycle. At the second bus cycle, a byte is fetched from the external device as a vector which identifies the type of interrupt. This vector is multiplied by four and used as an interrupt pointer address (INTR only).

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

HALT

When a Halt instruction is executed, the CPU enter Halt state. An interrupt request or RESET will force the MSM80C88A out of the Halt state.

SYSTEM TIMING—MINIMUM MODE

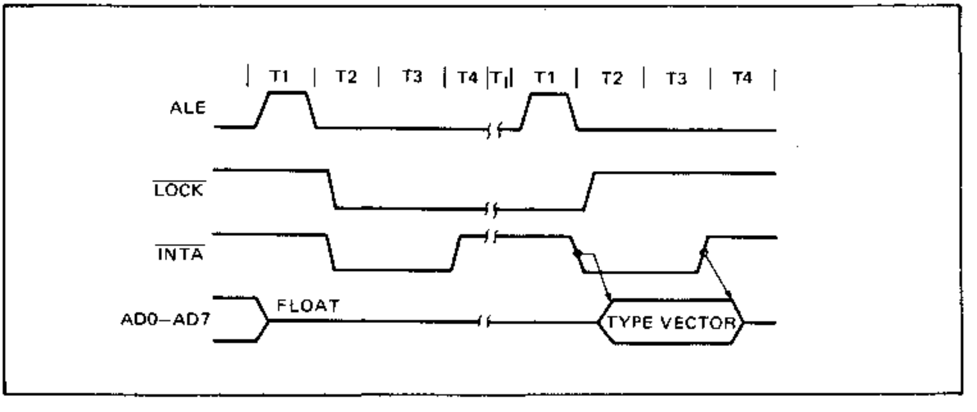
A bus cycle begins at T1 with an ALE signal. The trailing edge of ALE is used to latch the address. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to the data bus.

The read ($\overline{RD}$), write ($\overline{WR}$), and interrupt acknowledge ($\overline{INTA}$) signals caused the addressed device to enable the data bus. These signals become active at the beginning of T2 and inactive at the beginning of T4.

SYSTEM TIMING—MAXIMUM MODE

In maximum mode, the MSM82C88 Bus Controller is added to system. The CPU sends status information to the Bus Controller. Bus timing signals are generated by the Bus Controller. Bus timing is almost the same as in minimum mode.

Interrupt Acknowledge Sequence



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BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices, and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on 80C86 pins 2–16, 26–32, and 34–39 (Figures 6a, 6b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

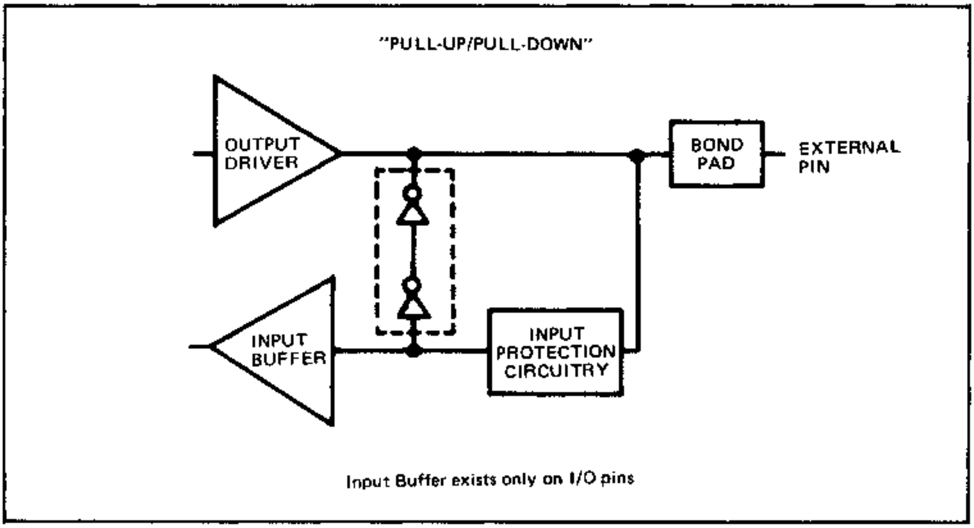

Figure 6a. Bus hold circuitry pin 2-16, 35-39.

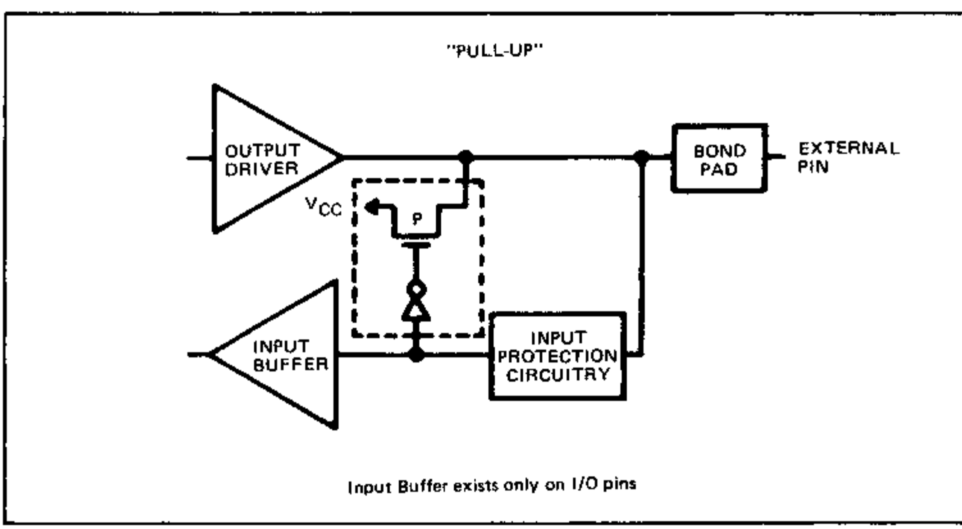

Figure 6b. Bus hold circuitry pin 26-32, 34

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DATA TRANSFER

MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate to register	1 0 1 1 w reg	data	data if w = 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

Instruction	Byte 1	Byte 2	Byte 3	Byte 4
ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with borrow:				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1			

DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD = Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate left through carry	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate right through carry	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w			

CJMP = Conditional JMP				
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp		
JZ/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp		
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp		
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp		
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp		
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp		
JO = Jump on over flow	0 1 1 1 0 0 0 0	disp		
JS = Jump on sign	0 1 1 1 1 0 0 0	disp		
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp		
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp		
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp		
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp		
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp		
JNP/JPO = Jump on not parity/parity odd	0 1 1 1 1 0 1 1	disp		
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp		
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp		
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp		
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp		
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp		
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp		
INT = Interrupt:				
Type specified	1 1 0 0 1 1 0 1	type		
Type 3	1 1 0 0 1 1 0 0			
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0			
IRET = Interrupt return	1 1 0 0 1 1 1 1			

PROCESSOR CONTROL

CLC = Clear carry	1 1 1 1 1 0 0 0			
CMC = Complement carry	1 1 1 1 0 1 0 1			
STC = Set carry	1 1 1 1 1 0 0 1			
CLD = Clear direction	1 1 1 1 1 1 0 0			
STD = Set direction	1 1 1 1 1 1 0 1			
CLI = Clear interrupt	1 1 1 1 1 0 1 0			
STI = Set interrupt	1 1 1 1 1 0 1 1			
HLT = Halt	1 1 1 1 0 1 0 0			
WAIT = Wait	1 0 0 1 1 0 1 1			
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m		
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0			

CONTROL TRANSFER

CALL = Call:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct within segment-short	1 1 1 0 1 0 1 1	disp		
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within segment	1 1 0 0 0 0 1 1			
Within seg. adding immediate to SP	1 1 0 0 0 0 1 0	data-low	data-high	
Intersegment	1 1 0 0 1 0 1 1			
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed value
If d = 1 then "to" reg; If d = 0 then "from" reg.
If w = 1 then word instruction; If w = 0 then byte instruction

If mod = 11 then r/m is treated as a REG field
If mod = 00 then DISP = 0*, disp-low and disp-high are absent
If mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
If mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
If r/m = 001 then EA = (BX) + (DI) + DISP
If r/m = 010 then EA = (BP) + (SI) + DISP
If r/m = 011 then EA = (BP) + (DI) + DISP
If r/m = 100 then EA = (SI) + DISP
If r/m = 101 then EA = (DI) + DISP
If r/m = 110 then EA = (BP) + DISP*
If r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
* except if mod = 00 and r/m = 110 then EA-disp-high: disp-low

If s:w = 01 then 16 bits of immediate data form the operand
If s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
If v = 0 then "count" = 1; If v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit	(w = 1)	8-Bit	(w = 0)	Segment	
000	AX	000	AL	00	ES
001	CX	001	CL	01	CS
010	DX	010	DL	10	SS
011	BX	011	BL	11	DS
100	SP	100	AH		
101	BP	101	CH		
110	SI	110	DH		
111	DI	111	BH		

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = x:x:x:x:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Preliminary

OKI semiconductor

MSM80C88A-10RS/GS/JS

8-BIT CMOS MICROPROCESSOR

GENERAL DESCRIPTION

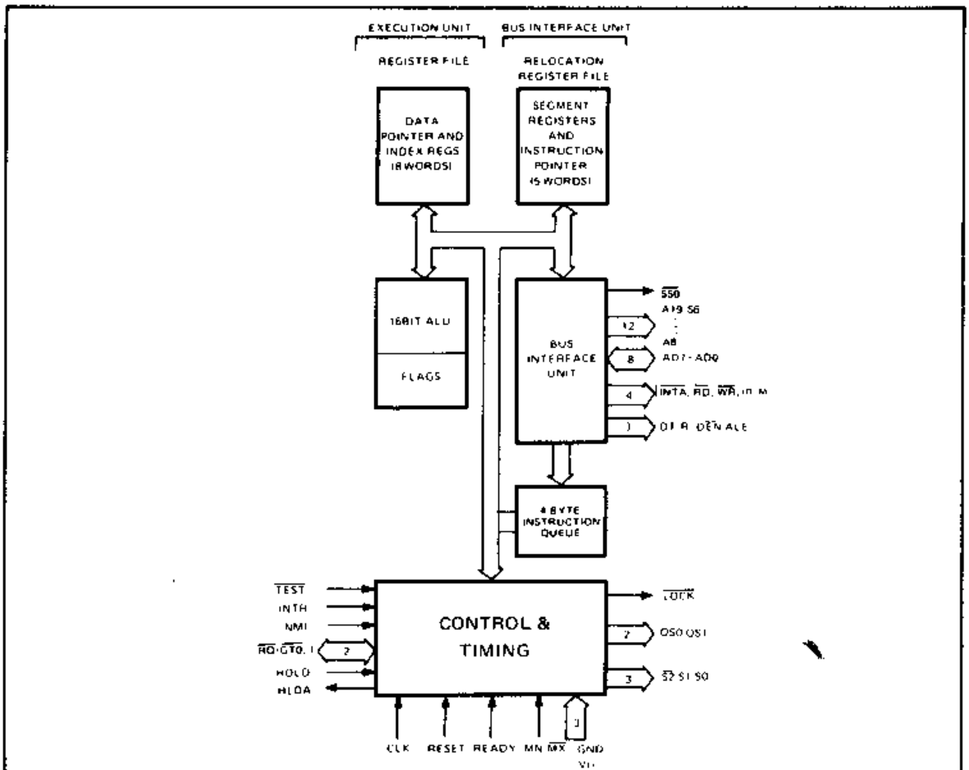
The MSM80C88A-10 are internal 16-bit CPUs with 8-bit interface implemented in Silicon Gate CMOS technology. They are designed with the same processing speed as the NMOS8088-1, but with considerably less power consumption.

The processor has attributes of both 8 and 16-bit microprocessor. It is directly compatible with MSM80C86A-10 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

FEATURES

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- 1 Mbyte Direct Addressable Memory Space
- Software Compatible with MSM80C86A
- Internal 14 Word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 10 MHz Clock Rate
- Low Power Dissipation (10 mA/MHz)
- Bus Hold Circuitry Eliminates Pull-Up Resistors

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION

MSM80C88A-10RS (Top View)
40 Lead Plastic DIP

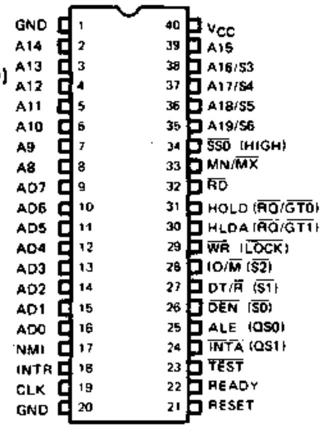


Fig. 2a MSM80C88A-10GS

MSM80C88A-10GS (Top View)
56-Lead Plastic Flat Package

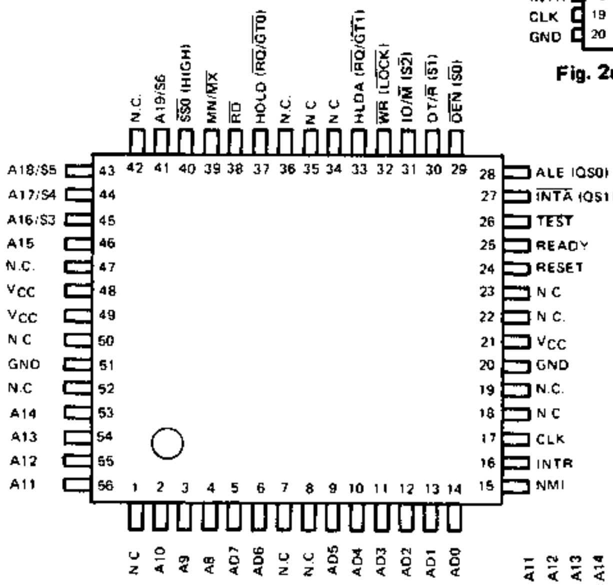
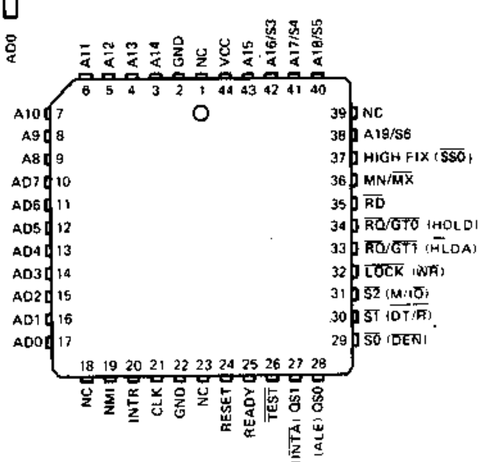


Fig. 2b MSM80C88A-10GS

MSM80C88A-10JS (Top View)
44 Pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits			Unit	Conditions
		MSM80C88A-10RS	MSM80C88A-10GS	MSM80C88A-10JS		
Power Supply Voltage	V_{CC}	-0.5 ~ +7			V	With respect to GND
Input Voltage	V_{IN}	-0.5 ~ V_{CC} +0.5			V	
Output Voltage	V_{OUT}	-0.5 ~ V_{CC} +0.5			V	
Storage Temperature	Tstg	-65 ~ +150			°C	–
Power Dissipation	P_D	1.0	0.7		W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits	Unit
		MSM80C88A-10	
Power Supply Voltage	V_{CC}	4.75 ~ 5.25	V
Operating Temperature	T_{OP}	0 ~ +70	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MSM80C88A-10			Unit
		MIN	TYP	MAX	
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	0	+25	+70	°C
"L" Input Voltage	V_{IL}	-0.5		+0.8	V
"H" Input Voltage	V_{IH} (*1)	V_{CC} -0.8		V_{CC} +0.5	V
	V_{IH} (*2)	2.0		V_{CC} +0.5	V

*1 Only CLK, *2 Except CLK

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DC CHARACTERISTICS

(MSM80C88A-10: V_{CC} = 4.75 to 5.25V, Ta = 0°C to +70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
"L" Output Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.0			V	I_{OH} = −2.5 mA
		V_{CC}−0.4				I_{OH} = −100μA
Input Leak Current	I_{LI}	−1.0		+1.0	μA	$0 < V_I < V_{CC}$
Output Leak Current	I_{LO}	−10		+10	μA	V_O = V_{CC} or GND
Input Leakage Current (Bus Hold Low)	I_{BHL}	50		400	μA	V_{IN} = 0.8V *3
Input Leakage Current (Bus Hold High)	I_{BHH}	−50		−400	μA	V_{IN} = 3.0V *4
Bus Hold Low Overdrive	I_{BHLO}			600	μA	*5
Bus Hold High Overdrive	I_{BHHO}			−600	μA	*6
Operating Power Supply Current	I_{CC}			10	mA/MHz	V_{IL}=GND V_{IH}=V_{CC}
StandbySupply Current	I_{CCS}			500	μA	V_{IN}=V_{CC} or GND Outputs Unloaded CLK=GND or V_{CC}
Input Capacitance	C_{in}			5	pF	*7
Output Capacitance	C_{out}			15	pF	*7
I/O Capacitance	$C_{I/O}$			20	pF	*7

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*3. Test conditions is to lower V_{IN} to GND and then raise V_{IN} to 0.8V on pins 2–16 and 35–39.
*4. Test condition is to raise V_{IN} to V_{CC} and then lower V_{IN} to 3.0V on pins 2–16, 26–32, and 34–39.
*5. An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
*6. An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.
*7. Test Conditions: a) Freq = 1 MHz.
b) Ummeasured Pins at GND.
c) V_{IN} at 5.0V or GND.

A.C. CHARACTERISTICS

(MSM80C88A-10: V_{CC} = 4.75V to 5.25V, Ta = 0°C to 70°C)

Minimum Mode System

Timing Requirements

Parameter	Symbol	MSM80C88A-10		Unit
		Min.	Max.	
CLK Cycle Period	TCLCL	100	DC	ns
CLK Low Time	TCLCH	46		ns
CLK High Time	TCHCL	44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10	ns
Data in Setup Time	TDVCL	20		ns
Data in Hold Time	TCLDX	10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		ns
READY Setup Time into MSM 80C88A	TRYHCH	46		ns
READY Hold Time into MSM 80C88A	TCHRYX	20		ns
READY inactive to CLK (See Note 3)	TRYLCL	−8		ns
HOLD Setup Time	THVCH	20		ns
INTR, NMI, $\overline{TEST}$ Setup Time (See Note 2)	TINVCH	15		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15	ns

Timing Responses

Parameter	Symbol	MSM80C88A-10		Unit
		Min.	Max.	
Address Valid Delay	TCLAV	10	60	ns
Address Hold Time	TCLAX	10		ns
Address Float Delay	TCLAZ	TCLAX	50	ns
ALE Width	TLHLL	TCLCH-10		ns
ALE Active Delay	TCLLH		40	ns
ALE Inactive Delay	TCHLL		45	ns
Address Hold Time to ALE Inactive	TLLAX	TCHCL-10		ns
Data Valid Delay	TCLDV	10	60	ns
Data Hold Time	TCHDX	10		ns
Data Hold Time after $\overline{WR}$	TWHDX	TCLCH-25		ns
Control Active Delay 1	TCVCTV	10	55	ns
Control Active Delay 2	TCHCTV	10	50	ns
Control Inactive Delay	TCVCTX	10	55	ns
Address Float to $\overline{RD}$ Active	TAZRL	0		ns
$\overline{RD}$ Acrive Delay	TCLRL	10	70	ns

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Parameter	Symbol	MSM80C88A-10		Unit
		Min.	Max.	
$\overline{RD}$ Inactive Delay	TCLRH	10	60	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-35		ns
HLDA Valid Delay	TCLHAV	10	60	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-40		ns
$\overline{WR}$ Width	TWLWH	2TCLCL-35		ns
Address Valid to ALE Low	TAVAL	TCLCH-35		ns
Output Rise Time (From 0.8V to 2.0)	TOLOH		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15	ns

Notes: 1. Signals at MSM82C84A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state. (8 ns into T3)

Maximum Mode System (Using MSM 82C88 Bus Controller)
Timing Requirements

Parameter	Symbol	MSM80C88A-10		Unit
		Min.	Max.	
CLK Cycle Period	TCLCL	100	DC	ns
CLK Low Time	TCLCH	46		ns
CLK High Time	TCHCL	44		ns
CLK Rise Time (From 1.0V to 3.5V)	TCH1CH2		10	ns
CLK Fall Time (From 3.5V to 1.0V)	TCL2CL1		10	ns
Data in Setup Time	TDVCL	15		ns
Data in Hold Time	TCLDX	10		ns
RDY Setup Time into MSM 82C84A (See Notes 1, 2)	TR1VCL	35		ns
RDY Hold Time into MSM 82C84A (See Notes 1, 2)	TCLR1X	0		ns
READY Setup Time into MSM 80C88A	TRYHCH	46		ns
READY Hold Time into MSM 80C88A	TCHRYX	20		ns
READY inactive to CLK (See Note 3)	TRYLCL	-8		ns
Set up Time for Recognition (NMI, INTR, $\overline{TEST}$) (See Note 2)	TINVCH	15		ns
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	15		ns
$\overline{RQ}$ Hold Time into MSM 80C88A	TCHGX	20		ns
Input Rise Time (Except CLK) (From 0.8V to 2.0V)	TILIH		15	ns
Input Fall Time (Except CLK) (From 2.0V to 0.8V)	TIHIL		15	ns

5

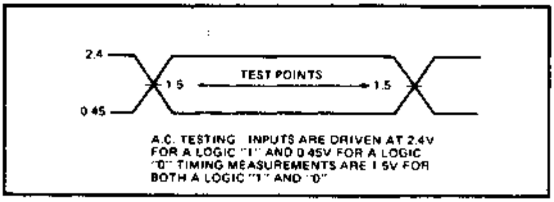
Timing Responses

Parameter	Symbol	MSM80C88A-10		Unit
		Min.	Max.	
Command Active Delay (See Note 1)	TCLML	5	35	ns
Command Inactive Delay (See Note 1)	TCLMH	5	45	ns
READY Active to Status Passive (See Note 4)	TRYHSH		45	ns
Status Active Delay	TCHSV	10	45	ns
Status Inactive Delay	TCLSH	10	60	ns
Address Valid Delay	TCLAV	10	60	ns
Address Hold Time	TCLAX	10		ns
Address Float Delay	TCLAZ	TCLAX	50	ns
Status Valid to ALE High (See Note 1)	TSVLH		25	ns
Status Valid to MCE High (See Note 1)	TSVMCH		30	ns
CLK low to ALE Valid (See Note 1)	TCLLH		25	ns
CLK Low to MCE High (See Note 1)	TCLMCH		25	ns
ALE Inactive Delay (See Note 1)	TCHLL	4	25	ns
Data Valid Delay	TCLDV	10	60	ns
Data Hold Time	TCHDX	10		ns
Control Active Delay (See Note 1)	TCVNV	5	45	ns
Control Inactive Delay (See Note 1)	TCVNX	5	45	ns
Address Float to $\overline{RD}$ Active	TAZRL	0		ns
$\overline{RD}$ Active Delay	TCLRL	10	70	ns
$\overline{RD}$ Inactive Delay	TCLRH	10	60	ns
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL-35		ns
Direction Control Active Delay (See Note 1)	TCHDTL		50	ns
Direction Control Inactive Delay (See Note 1)	TCHDTH		30	ns
$\overline{GT}$ Active Delay	TCLGL	0	45	ns
$\overline{GT}$ Inactive Delay	TCLGH	0	45	ns
$\overline{RD}$ Width	TRLRH	2TCLCL-40		ns
Output Rise Time (From 0.8V to 2.0V)	TOLOH		15	ns
Output Fall Time (From 2.0V to 0.8V)	TOHOL		15	ns

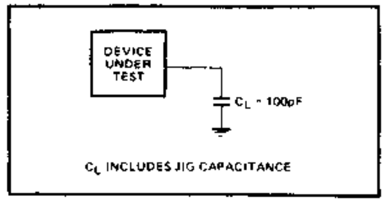
Notes:
1. Signals at MSM 82C84A or MSM 82C88 are shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3)
4. Applies only to T3 and wait states.

5

A.C. TESTING INPUT, OUTPUT WAVEFORM

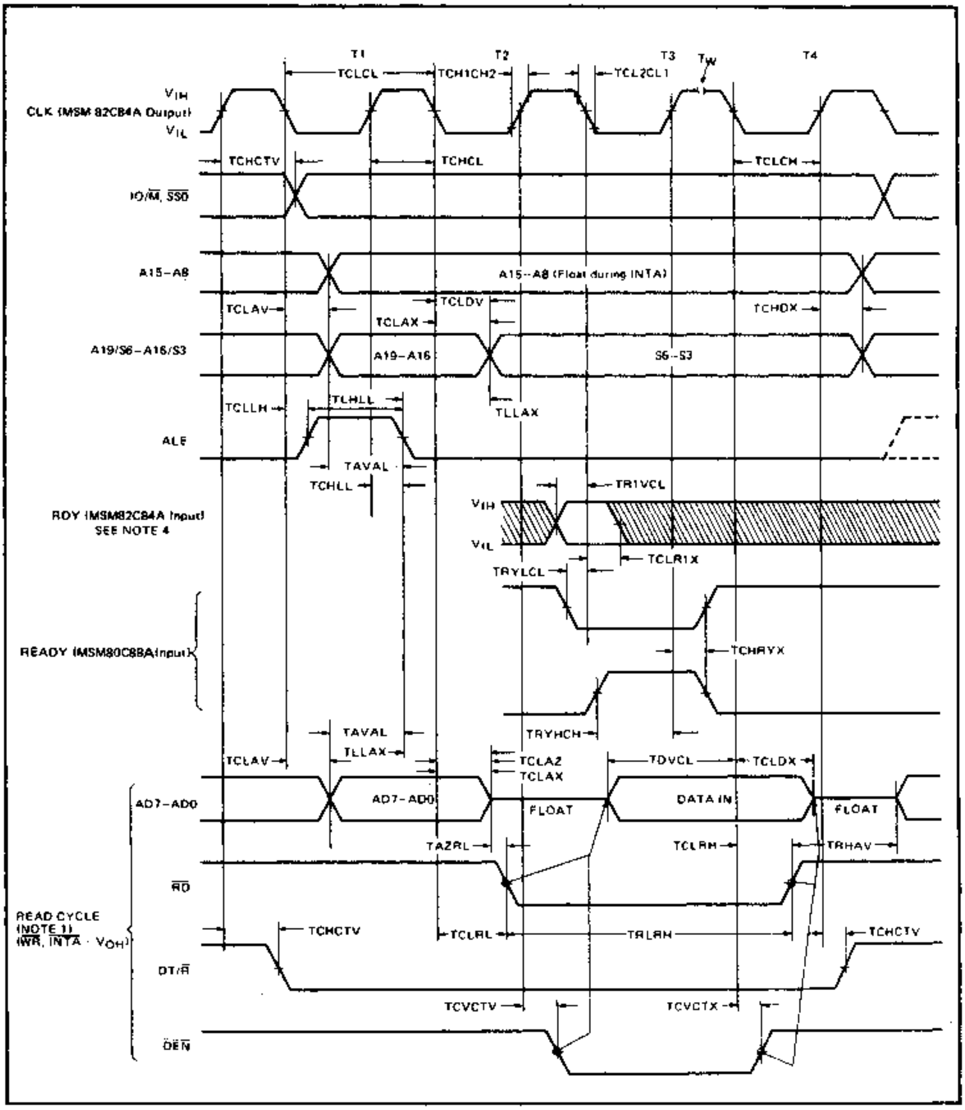


A.C. TESTING LOAD CIRCUIT



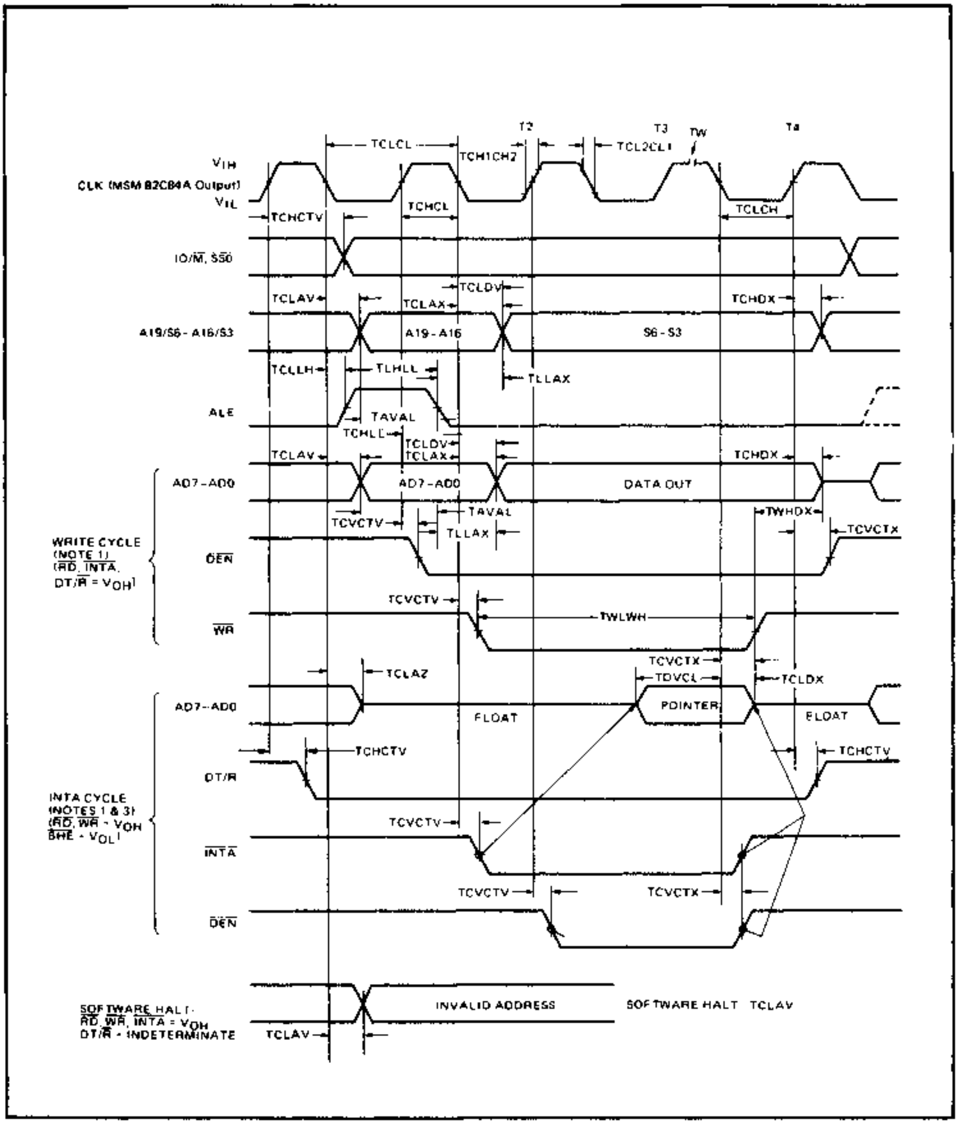
TIMING CHART

Minimum Mode



5

Minimum Mode (Continued)

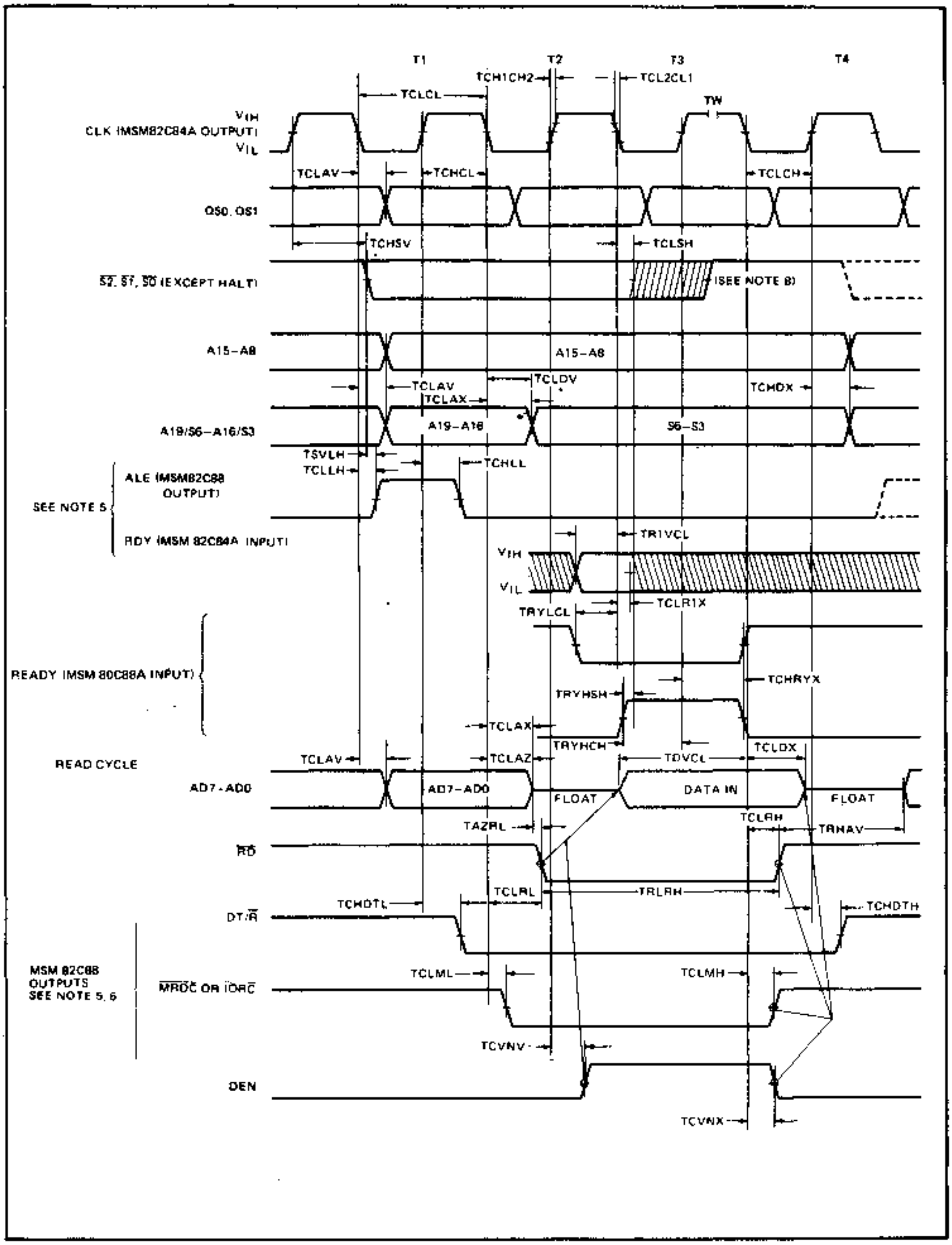


NOTES:

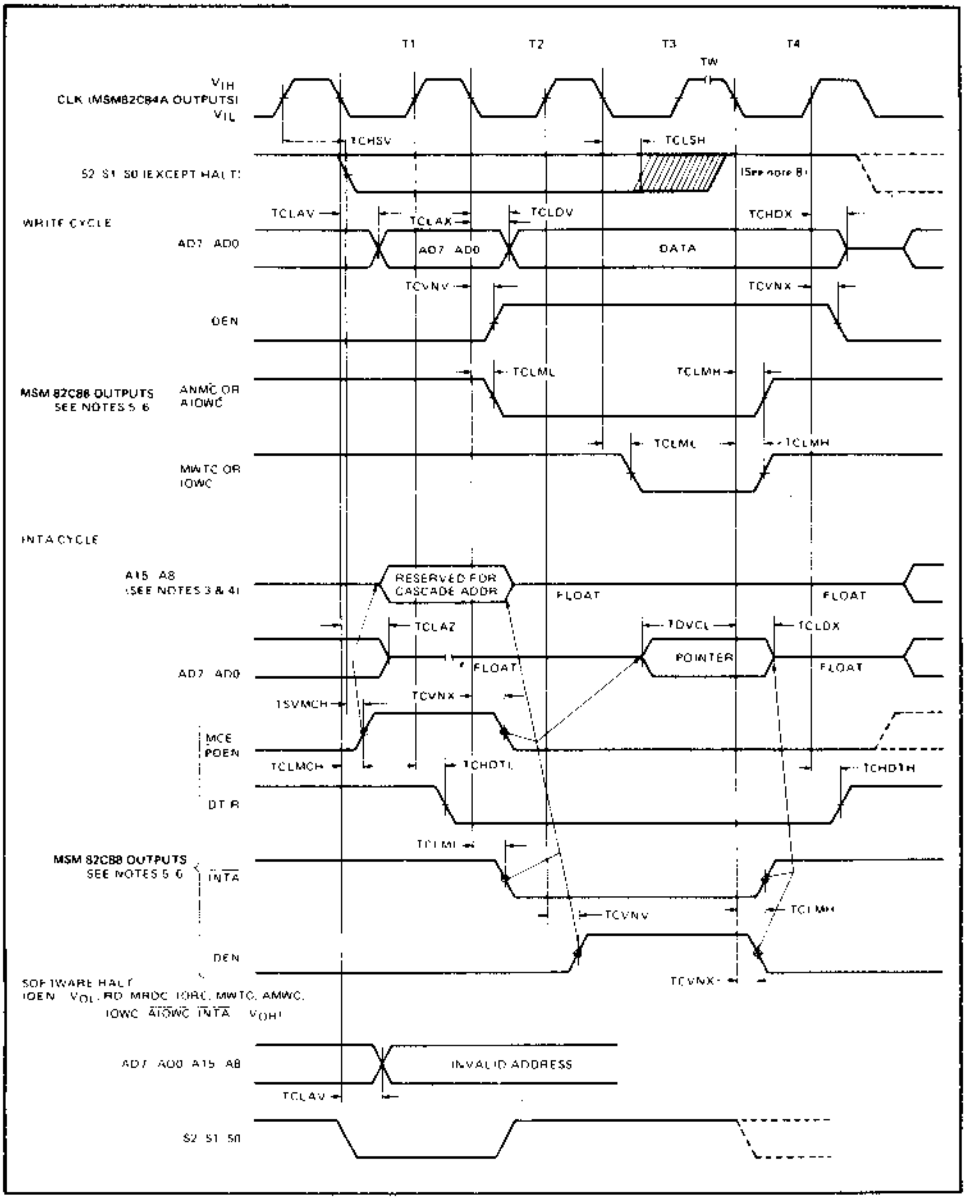
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3. Two INTA cycles run back-to-back. The MSM80C88A LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control signals shown for second INTA cycle.
4. Signals at MSM 82C84A shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

5

Maximum Mode



Maximum Mode (Continued)



NOTES.

1 All signals switch between V_{OH} and V_{OL} unless otherwise specified

2 RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted

3 Cascade address is valid between first and second INTA cycle

4 Two INTA cycles run back to back The MSM 80C88A LOCAL ADDR/DATA BUS is floating during both INTA cycles Control for pointer address is shown for second INTA cycle

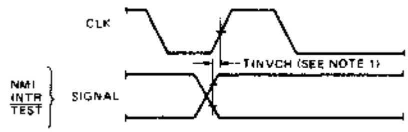
5 **Signal at MSM 82C84A and MSM82C88 shown for reference only.**

6 The issuance of the MSM 82C88 command and control signals $\overline{IMRDC}$ $\overline{MWTC}$ $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$ $\overline{INTA}$ and DEN) lags the active high MSM 82C88 CEN

7 All timing measurements are made at 1.5V unless otherwise noted

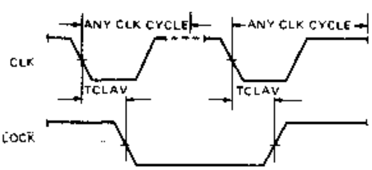
8 Status inactive in state just prior to T4

Asynchronous Signal Recognition

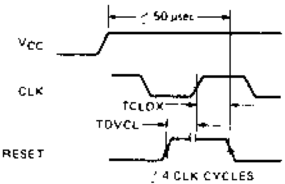


NOTE: 1 SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK

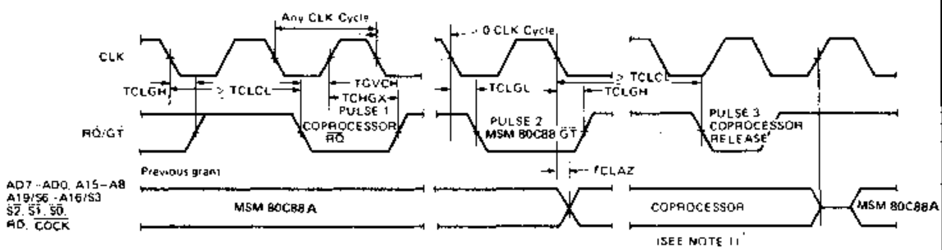
Bus Lock Signal Timing (Maximum Mode Only)



Reset Timing

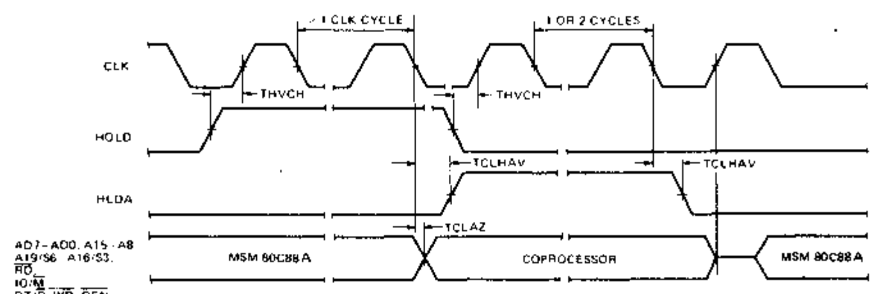


Request/Grant Sequence Timing (Maximum Mode Only)



NOTE: 1 THE COPROCESSOR MAY NOT DRIVE THE BUSSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION

Hold/Hold Acknowledge Timing (Minimum Mode Only)



PIN DESCRIPTION

AD0–AD7

ADDRESS DATA BUS: Input/Output

These lines are the multiplexed address and data bus.

These are the address bus at T1 cycle and the data bus at T2, T3, TW and T4 cycle.

T2, T3, TW and T4 cycle.

These lines are high impedance during interrupt acknowledge and hold acknowledge.

A8–A15

ADDRESS BUS: Output

These lines are the address bus bits 8 thru 15 at all cycles.

These lines do not have to be latched by an ALE signal.

These lines are high impedance during interrupt acknowledge and hold acknowledge.

A16/S3, A17/S4, A18/S5, A19/S6

ADDRESS/STATUS: Output

These are the four most significant address as at the T1, cycle.

Accessing I/O port address, these are low at T1 Cycles.

These lines are Status lines at the T2, T3, TW and T4 Cycle.

S5 indicate interrupt enable Flag.

S3 and S4 are encoded as shown.

S3	S4	Characteristics
0	0	Alternate Data
1	0	Stack
0	1	Code or None
1	1	Data

These lines are high impedance during hold acknowledge.

$\overline{RD}$

READ: Output

This lines indicates that the CPU is in a memory or I/O read cycle.

This line is the read strobe signal when the CPU reads data from a memory or I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

READY

READY: Input

This line indicates to the CPU that an addressed memory or I/O device is ready to read or write.

This line is active high.

IF the setup and hold time are outof specification, an illegal operation will occur.

INTR

INTERRUPT REQUEST: Input

This line is a level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulations.

It can be internally masked by software.

This signal is active high and internally synchronized.

$\overline{TEST}$

TEST: Input

This line is examined by a "WAIT" instruction.

When $\overline{TEST}$ is high, the CPU enters an idle cycle.

When $\overline{TEST}$ is low, the CPU exits an idle cycle.

NMI

NON MASKABLE INTERRUPT: Input

This line causes a type 2 interrupt.

NMI is not maskable.

This signal is internally synchronized and needs a 2 clock cycle pulse width.

RESET

RESET: Input

This signal causes the CPU to initialize immediately.

This signal is active high and must be at least four clock cycles.

CLK

CLOCK: Input

This signal provide the basic timing for an internal circuit.

MN/$\overline{MX}$

MINIMUM/MAXIMUM: Input

This signal selects the CPU's operate mode.

When V_{CC} is connected, the CPU operates in minimum mode.

When GND is connected, the CPU operates in maximum mode.

V_{CC}

V_{CC} +5V supplied.

GND

GROUND

The following pin function descriptions are for maximum mode only.

Other pin functions are already described.

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

STATUS: Output

These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals.

These lines are high impedance during hold acknowledge.

These status lines are encoded as shown.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

$\overline{RQ}/\overline{GT0}$
$\overline{RQ}/\overline{GT1}$

REQUEST/GRANT: Input/Output

These lines are used for Bus Request from other devices and Bus GRANT to other devices.

These lines are bidirectional and active low.

$\overline{LOCK}$

LOCK: Output

This line is active low.

When this line is low, other devices can not gain control of the bus.

This line is high impedance during hold acknowledge.

QS0/QS1

QUEUE STATUS: Output

These are Queue Status Lines that indicate internal instruction queue status.

QS1	QS0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are minimum mode only. Other pin functions are already described.

IO/$\overline{M}$

STATUS: Output

This line selects memory address space or I/O address space.

When this line is low, the CPU selects memory address space and when it is high, the CPU selects I/O address space.

This line is high impedance during hold acknowledge.

$\overline{WR}$

WRITE: Output

This line indicates that the CPU is in a memory or I/O write cycle.

This line is a write strobe signal when the CPU writes data to memory or an I/O device.

This line is active low.

This line is high impedance during hold acknowledge.

$\overline{INTA}$

INTERRUPT ACKNOWLEDGE: Output

This line is a read strobe signal for the interrupt accknowledge cycle.

This line is active low.

ALE

ADDRESS LATCH ENABLE: Output

This line is used for latching an address into the MSM82C12 address latch it is a positive pulse and the trailing edge is used to strobe the address. This line in never floated.

DT/$\overline{R}$

DATA TRANSMIT/RECEIVE: Output

This line is used to control the direction of the bus transceiver.

When this line is high, the CPU transmits data, and when it is low, the CPU receive data.

This line is high impedance during hold acknowledge.

$\overline{DEN}$

DATA ENABLE: Output

This line is used to control the output enable of the bus transceiver.

This line is active low. This line is high impedance during hold acknowledge.

HOLD

HOLD REQUEST: Input

This line is used for a Bus Request from an other device.

This line is active high.

HLDA

HOLD ACKNOWLEDGE: Output

This line is used for a Bus Grant to an other device.

This line is active high.

$\overline{SS0}$

STATUS: Output

This line is logically equivalent to $\overline{S0}$ in the maximum mode.

STATIC OPERATION

All MSM80C88A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C88A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C88A can be signal stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C88A power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the MSM80C88A power requirement is the standby current (500 μA maximum).

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The internal function of the MSM80C88A consist of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

The BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. By performing instruction prefetch while waiting for decoding and execution of instruction, the CPU's performance is increased. Up to 4-bytes fo instruction stream can be queued.

EU receives pre-fetched instructions from the BIU queue, decodes and executes instructions and provides an un-relocated operand address to the BIU.

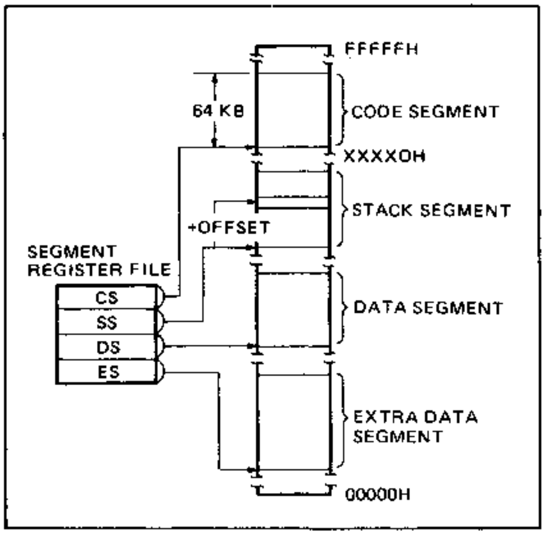
MEMORY ORGANIZATION

The MSM80C88A has a 20-bit address to memory. Each address has 8-bit data width. Memory is organized 00000H to FFFFFH and is logically divided into four segments: code, data, extra data and stack segment. Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)

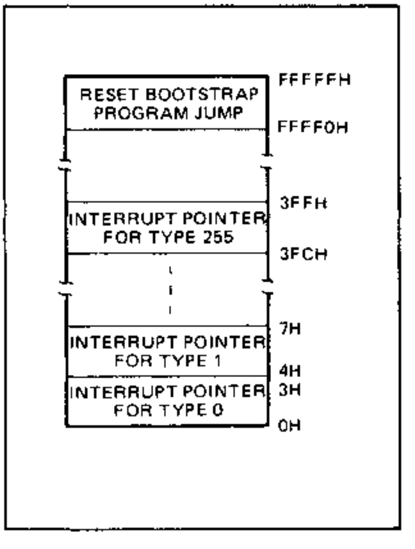
All memory references are made relative to a segment register according to a select rule. Memory location FFFF0H is the start address after reset, and 00000H through 003FFH are reserved as an interrupt pointer. There are 256 types of interrupt pointer;

Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

Memory Organization



Reserved Memory Locations



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Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

MINIMUM AND MAXIMUM MODES

The MSM80C88A has two system modes: minimum and maximum. When using the maximum mode, it is easy to organize a multiple-CPU system with the MSM 82C88 Bus Controller which generates the bus control signal.

When using the minimum mode, it is easy to organize a simple system by generating the bus control signal itself. MN/$\overline{MX}$ is the mode select pin. Definition of 24–31, 34 pin changes depends on the MN/MX pin.

BUS OPERATION

The MSM80C88A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for the system, it is only needed to add the address latch.

A CPU bus cycle consists of at least four clock cycles: T1, T2, T3 and T4. (Fig. 4)

The address output occurs during T1, and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus during read operation. When the device which is accessed by the CPU is not ready to data transfer and send to the CPU "NOT READY" is indicated TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution. At the T1 cycle an ALE signal is output from the CPU or the MSM82C88 depending in MN/$\overline{MX}$. at the trailing edge of an ALE, a valid address may be latched. Status bits S0, S1 and S2 are uased, in maximum mode, by the bus controller to recognize the type of bus operation according to the following table.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bit S3 through S6 are multiplexed with A16–A19, and therefore they are valid during T2 through T4. S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table.

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra Segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 indicates interrupt enable Flag.

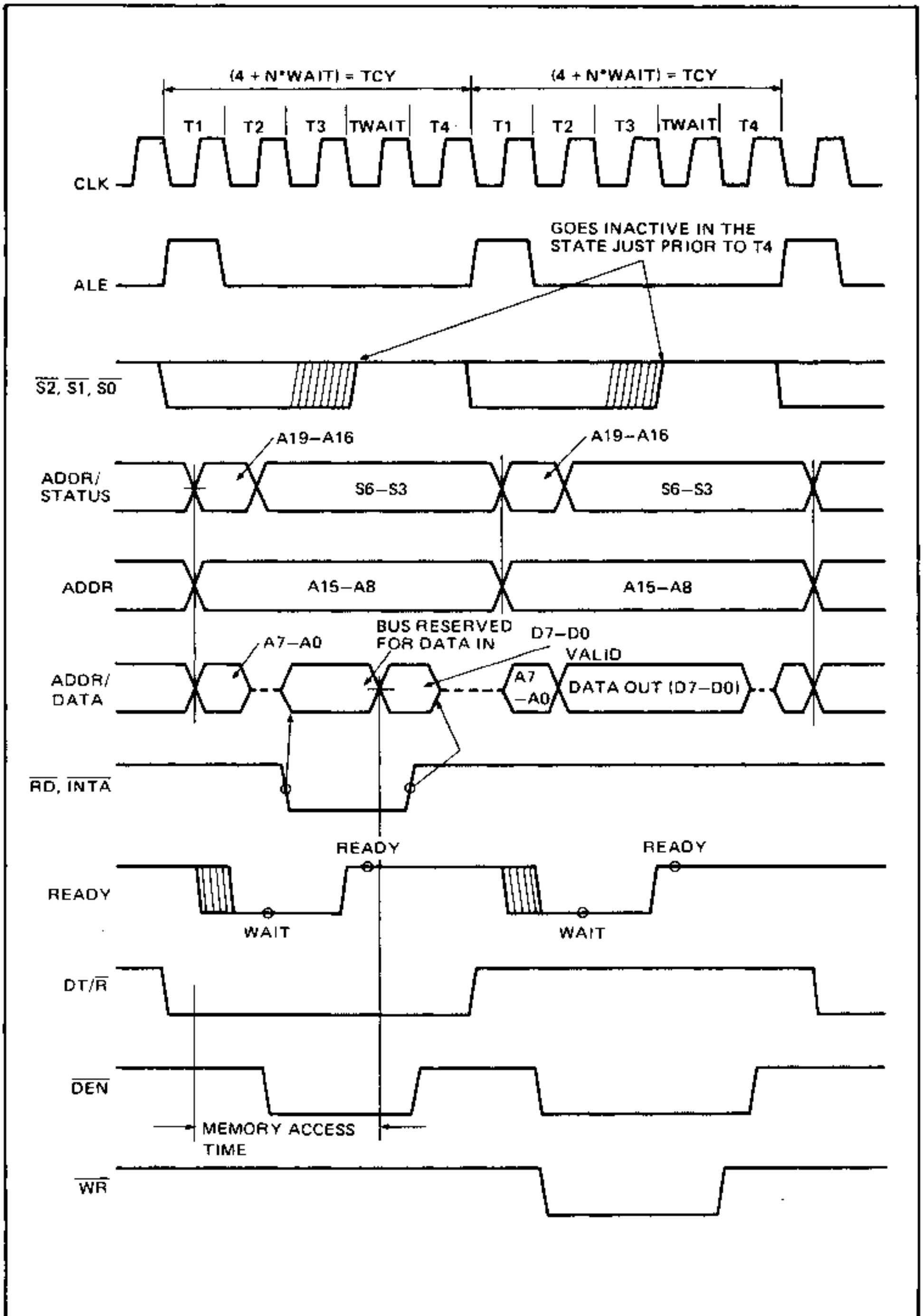
I/O ADDRESSING

The MSM80C88A has a 64 Kbyte I/O. When the CPU accesses an I/O device, address A0–A15 are in same format as a memory access, and A16–A19 are low.

I/O ports address are same as four memory.

5

Basic System Timing



EXTERNAL INTERFACE

RESET

CPU initialization is executed by the RESET pin. The MSM80C88A's RESET High signal is required for greater than 4 clock cycles.

The rising edge of RESET terminates the present operation immediately. The falling edge of RESET triggers an internal reset requence for approximately 10 clock cycles. After internal reset sequence is finished, normal operation begins from absolute location FFFF0H.

INTERRUPT OPERATIONS

The interrupt operation is classified as software or hardware, and hardware interrupt is classified as non-markable or maskable.

An interrupt causes a new program location which is defined by the interrupt pointer table, according to the interrupt type. Absolute location 00000H through 003FFH is reserved for the interrupt pointer table. The interrupt pointer table consists of 256-elements. Each element is 4 bytes in size and corresponds to an 8-bit type number which is sent from an interrupt request device during the interrupt acknowledge cycle.

NON-MASKABLE INTERRUPT (NMI)

The MSM80C88A has a non-maskable Interrupt (NM1) which is of higher priority than a maskable interrupt request (INTR).

An NM1 request pulse width needs minimum of 2 clock cycles. The NM1 will be serviced at the end of the current instruction or between string manipulations.

MASKABLE INTERRUPT (INTR)

The MSM80C88A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until interrupt request is acknowledged.

The INTR will be serviced at the end of the current instruction or between string manipulations.

INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt, after which the Flag register is automatically pushed onto the stack. During an acknowledge sequence, the CPU emits the lock signal from T2 of first bus cycle to T2 of second bus cycle. At the second bus cycle, a byte is fetched from the external device as a vector which identifies the type of interrupt. This vector is multiplied by four and used as an interrupt pointer address (INTR only).

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

HALT

When a Halt instruction is executed, the CPU enter Halt state. An interrupt request or RESET will force the MSM80C88A out of the Halt state.

SYSTEM TIMING—MINIMUM MODE

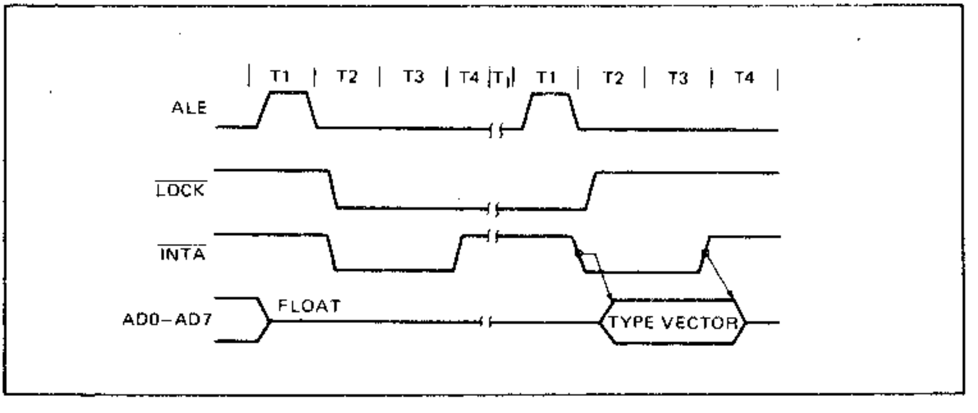
A bus cycle begins at T1 with an ALE signal. The trailing edge of ALE is used to latch the address. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to the data bus.

The read ($\overline{RD}$), write ($\overline{WR}$), and interrupt acknowledge ($\overline{INTA}$) signals caused the addressed device to enable the data bus. These signals become active at the beginning of T2 and inactive at the beginning of T4.

SYSTEM TIMING—MAXIMUM MODE

In maximum mode, the MSM82C88 Bus Controller is added to system. The CPU sends status information to the Bus Controller. Bus timing signals are generated by the Bus Controller. Bus timing is almost the same as in minimum mode.

Interrupt Acknowledge Sequence



BUS HOLD CIRCUITRY

To avoid high current conditions caused by floating inputs to CMOS devices, and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on 80C86 pins 2–16, 26–32, and 34–39 (Figures 6a, 6b). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400 μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

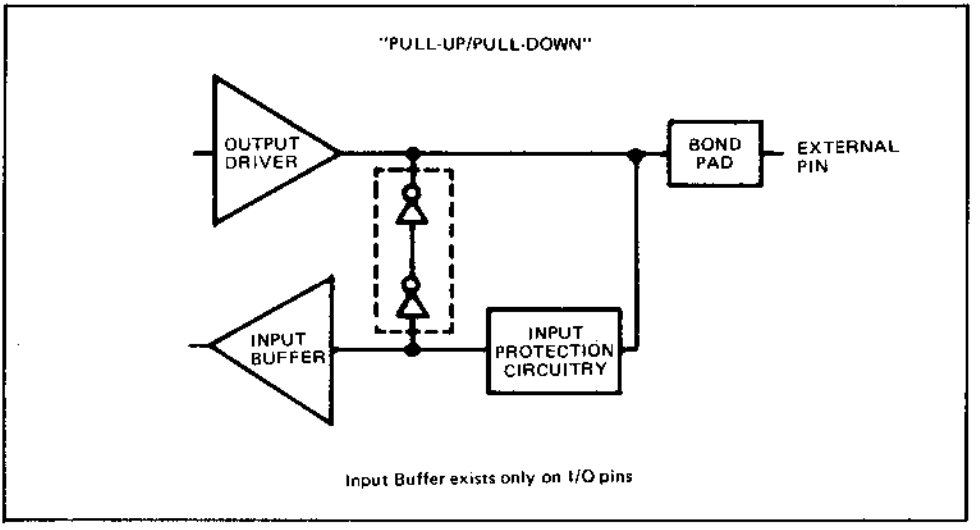


Figure 6a. Bus hold circuitry pin 2-16, 35-39.

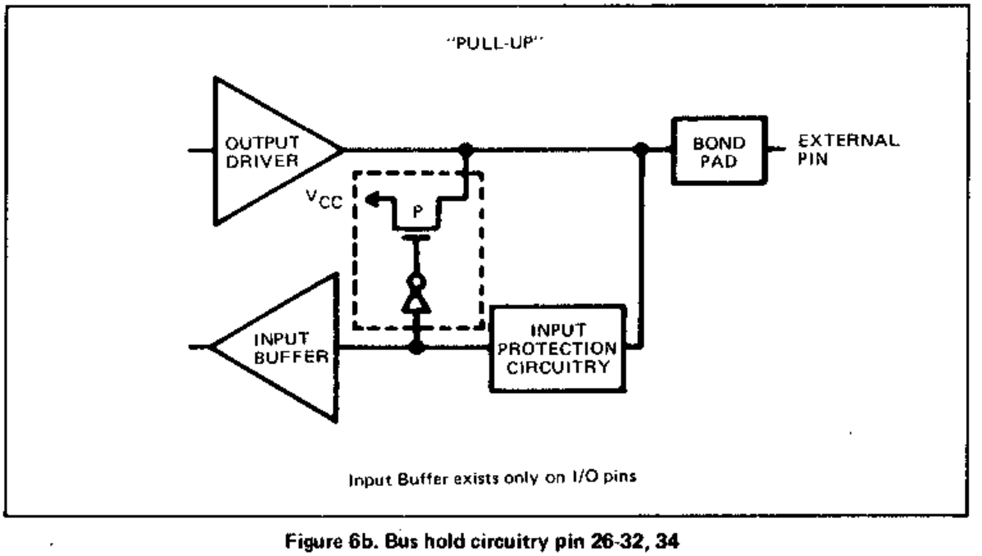


Figure 6b. Bus hold circuitry pin 26-32, 34

DATA TRANSFER

MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate to register	1 0 1 1 w reg	data	data if w = 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN = Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w = 1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s:w = 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w = 1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w = 1	
SBB = Subtract with borrow:				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s:w = 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w = 1	
DEC = Decrement:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG = Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP = Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s:w = 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w = 1	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1			

DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL = Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL = Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV = Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW = Convert byte to word	1 0 0 1 1 0 0 0			
CWD = Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate left through carry	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate right through carry	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1	
TEST = And function to flags, no result.				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1	
XOR = Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w			
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w			

CJMP = Conditional JMP				
JE/JZ = Jump on equal/zero	0 1 1 1 0 1 0 0	disp		
JZ/JNGE = Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp		
JLE/JNG = Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp		
JB/JNAE = Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp		
JBE/JNA = Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp		
JP/JPE = Jump on parity/parity even	0 1 1 1 1 0 1 0	disp		
JO = Jump on over flow	0 1 1 1 0 0 0 0	disp		
JS = Jump on sign	0 1 1 1 1 0 0 0	disp		
JNE/JNZ = Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp		
JNL/JGE = Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp		
JNLE/JG = Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp		
JNB/JAE = Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp		
JNBE/JA = Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp		
JNP/JPO = Jump on not parity/parity odd	0 1 1 1 1 0 1 1	disp		
JNO = Jump on not overflow	0 1 1 1 0 0 0 1	disp		
JNS = Jump on not sign	0 1 1 1 1 0 0 1	disp		
LOOP = Loop CX times	1 1 1 0 0 0 1 0	disp		
LOOPZ/LOOPE = Loop while zero/equal	1 1 1 0 0 0 0 1	disp		
LOOPNZ/LOOPNE = Loop while not zero/equal	1 1 1 0 0 0 0 0	disp		
JCXZ = Jump on CX zero	1 1 1 0 0 0 1 1	disp		
INT = Interrupt:				
Type specified	1 1 0 0 1 1 0 1	type		
Type 3	1 1 0 0 1 1 0 0			
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0			
IRET = Interrupt return	1 1 0 0 1 1 1 1			

PROCESSOR CONTROL

CLC = Clear carry	1 1 1 1 1 0 0 0			
CMC = Complement carry	1 1 1 1 0 1 0 1			
STC = Set carry	1 1 1 1 1 0 0 1			
CLD = Clear direction	1 1 1 1 1 1 0 0			
STD = Set direction	1 1 1 1 1 1 0 1			
CLI = Clear interrupt	1 1 1 1 1 0 1 0			
STI = Set interrupt	1 1 1 1 1 0 1 1			
HLT = Halt	1 1 1 1 0 1 0 0			
WAIT = Wait	1 0 0 1 1 0 1 1			
ESC = Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m		
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0			

CONTROL TRANSFER

CALL = Call:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high	
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m		
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m		
JMP = Unconditional Jump:				
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high	
Direct within segment-short	1 1 1 0 1 0 1 1	disp		
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m		
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high	
		seg-low	seg-high	
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m		
RET = Return from CALL:				
Within segment	1 1 0 0 0 0 1 1			
Within seg. adding immediate to SP	1 1 0 0 0 0 1 0	data-low	data-high	
Intersegment	1 1 0 0 1 0 1 1			
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive
Less = less positive (more negative) signed value
If d = 1 then "to" reg: If d = 0 then "from" reg.
If w = 1 then word instruction: If w = 0 then byte instruction

If mod = 11 then r/m is treated as a REG field
If mod = 00 then DISP = 0*, disp-low and disp-high are absent
If mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
If mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
If r/m = 001 then EA = (BX) + (DI) + DISP
If r/m = 010 then EA = (BP) + (SI) + DISP
If r/m = 011 then EA = (BP) + (DI) + DISP
If r/m = 100 then EA = (SI) + DISP
If r/m = 101 then EA = (DI) + DISP
If r/m = 110 then EA = (BP) + DISP*
If r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
* except if mod = 00 and r/m = 110 then EA-disp-high: disp-low

If s:w = 01 then 16 bits of immediate data form the operand
If s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
If v = 0 then "count" = 1: If v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)		8-Bit (w = 0)		Segment	
000	AX	000	AL	00	ES
001	CX	001	CL	01	CS
010	DX	010	DL	10	SS
011	BX	011	BL	11	DS
100	SP	100	AH		
101	BP	101	CH		
110	SI	110	DH		
111	DI	111	BH		

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = x:x:x:x:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

I/O

OKI semiconductor

MSM81C55RS/GS/JS
MSM81C55-5RS/GS/JS

2048 BIT CMOS STATIC RAM WITH I/O PORTS AND TIMER

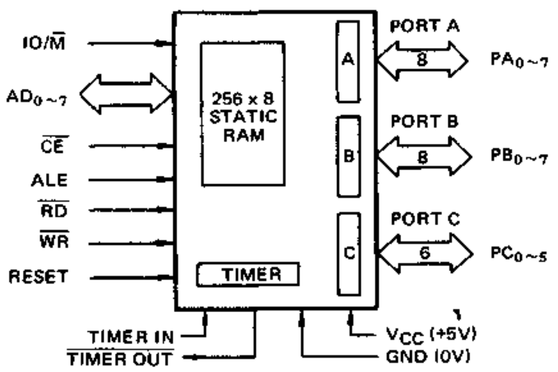
GENERAL DESCRIPTION

The MSM81C55/81C55-5 have 2k bits of static RAM (256 byte) with parallel I/O ports and a timer. It uses silicon gate CMOS technology and consumes a standby current of 100 micro ampere, maximum, while the chip is not selected. Featuring a maximum access time of 400 ns, the MSM81C55/81C55-5 can be used in an 80C85A/80C85A-2 system without using wait states. The parallel I/O consists of two 8-bit ports and one 6-bit port (both general purpose). The MSM81C55/81C55-5 also contains a 14-bit programmable counter/timer which may be used for sequence-wave generation or terminal count-pulsing.

FEATURES

- High speed and low power achieved with silicon gate CMOS technology.
- 256 words x 8 bits RAM
- Single power supply, 3 to 6V
- Completely static operation
- On-chip address latch
- 8-bit programmable I/O ports (port A and B)
- TTL Compatible
- RAM data hold characteristic at 2V
- 6-bit programmable I/O port (port C)
- 14-bit programmable binary counter/timer
- Multiplexed address/data bus
- 40 pin DIP package (MSM81C55RS/MSM81C55-5RS)
- 44 pin flat package (MSM81C55GS)/MSM81C55-5GS)
- 44 pin PLCC (MSM81C55JS/MSM81C55-5JS)
- Direct interface with MSM80C85A
- Direct interface with MSM80C85A-2 (MSM81C55-5)

FUNCTIONAL BLOCK DIAGRAM



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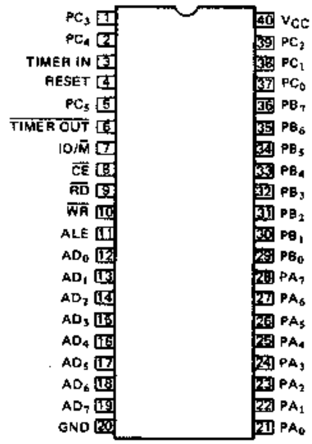
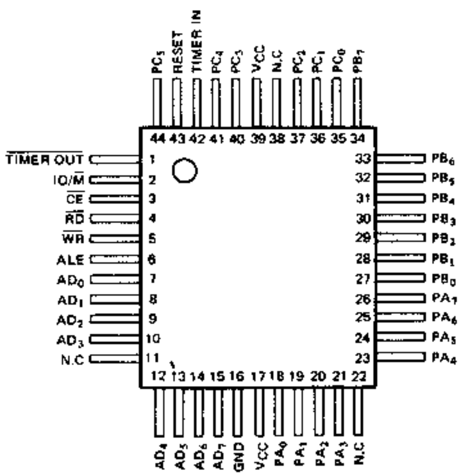
PIN CONFIGURATION

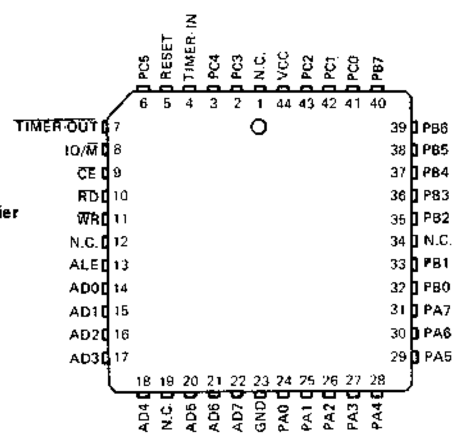
MSM81C55RS (Top View)
MSM81C55-5RS
40 Lead Plastic DIP





MSM81C55GS (Top View)
MSM81C55-5GS
44 Lead Plastic Flat Package

MSM81C55JS (Top View)
MSM81C55-5JS
44 Pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM81C55RS MSM81C55-5RS	MSM81C55GS MSM81C55-5GS	MSM81C55JS MSM81C55-5JS	
Supply Voltage	V_{CC}	Referenced to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to + 150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING CONDITION

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (81C55)	V_{CC}	4.5	5	5.5	V
Operating Temperature (81C55)	T_{OP}	−40	+25	+85	°C
"L" Level Input	V_{IL}	−0.3		+0.8	V
"H" Level Input	V_{IH}	2.2		V_{CC} + 0.3	V
Supply Voltage (81C55-5)	V_{CC}	4.75	5	5.25	V
Operating Temperature (81C55-5)	T_{OP}	−40	+25	+70	°C

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Level Output Voltage	V_{OL}	I_{OL} = 2mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to 85°C			0.45	V
"H" Level Output Voltage	V_{OH}	I_{OH} = −400μA		2.4			V
		I_{OH} = −40μA		4.2			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Standby Current	I_{CCS}	$\overline{CE} \geqq V_{CC}$−0.2V $V_{IH} \geqq V_{CC}$−0.2V $V_{IL} \leq$ 0.2V			0.1	100	μA
Mean Operating Current	I_{CC}	Memory cycle time: 1μs				5	mA

AC CHARACTERISTICS

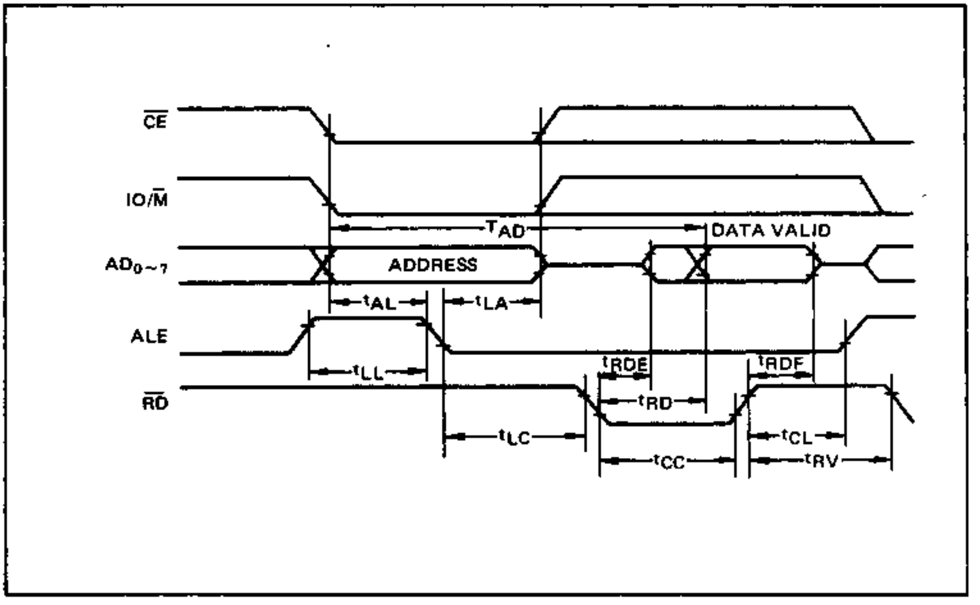
(V_{CC} = 4.5 to 5.5V, Ta = −40 to +80°C) MSM81C55
(V_{CC} = 4.75 to 5.25V, Ta = −40 to +70°C) MSM81C55-5

Parameter	Symbol	MSM81C55		MSM81C55-5		Unit	Remarks
		Min.	Max.	Min.	Max.		
Address/latch Set-up Time	t_{AL}	50		37		ns	Load capacitance: 150pF
Latch/address Holt Time	t_{LA}	30		30		ns	
Latch/read (write) Delay Time	t_{LC}	100		40		ns	
Read/output Delay Time	t_{RD}		170		140	ns	
Address/output Delay Time	t_{AD}		400		330	ns	
Latch Width	t_{LL}	100		70		ns	
Read/data Bus Floating Time	t_{RDF}	0	100	0	80	ns	
Read (write)/latch Delay Time	t_{CL}	20		20		ns	
Read (write) Width	t_{CC}	250		200		ns	
Data In/write Set-up Time	t_{DW}	150		100		ns	
Write/data-in Holt Time	t_{WD}	0		25		ns	
Recovery Time	t_{RV}	300		200		ns	
Write/port Output Delay Time	t_{WP}		400		300	ns	
Port Input/read Set-up Time	t_{PR}	70		50		ns	
Read/port Input Hold Time	t_{RP}	50		10		ns	
Strobe/buffer Full Delay Time	t_{SBF}		400		300	ns	
Strobe Width	t_{SS}	200		150		ns	
Strobe/buffer Empty Delay Time	t_{RBE}		400		300	ns	
Strobe/interrupt-on Delay Time	t_{SI}		400		300	ns	
Read/interrupt-off Delay Time	t_{RDI}		400		300	ns	
Port Input/strobe Set-up Time	t_{PSS}	50		20		ns	
Strobe/port-input Hold Time	t_{PHS}	120		100		ns	
Strobe/buffer-empty Delty Time	t_{SBE}		400		300	ns	
Write/buffer-full Delay Time	t_{WBF}		400		300	ns	
Write/interrupt-off Delay Time	t_{WI}		400		300	ns	
Time Output Delay Time Low	t_{TL}		400		300	ns	
Time Output Delay Time High	t_{TH}		400		300	ns	
Read/data Buse Enable Delay Time	t_{RDE}	10		10		ns	
Timer Cycle Time	t_{CYC}	320		320		ns	
Timer Input Rise and Fall Times	t_r, t_f		80		80	ns	
Timer Input Low Level Time	t_1	80		40		ns	
Timer Input High Level Time	t_2	120		70		ns	

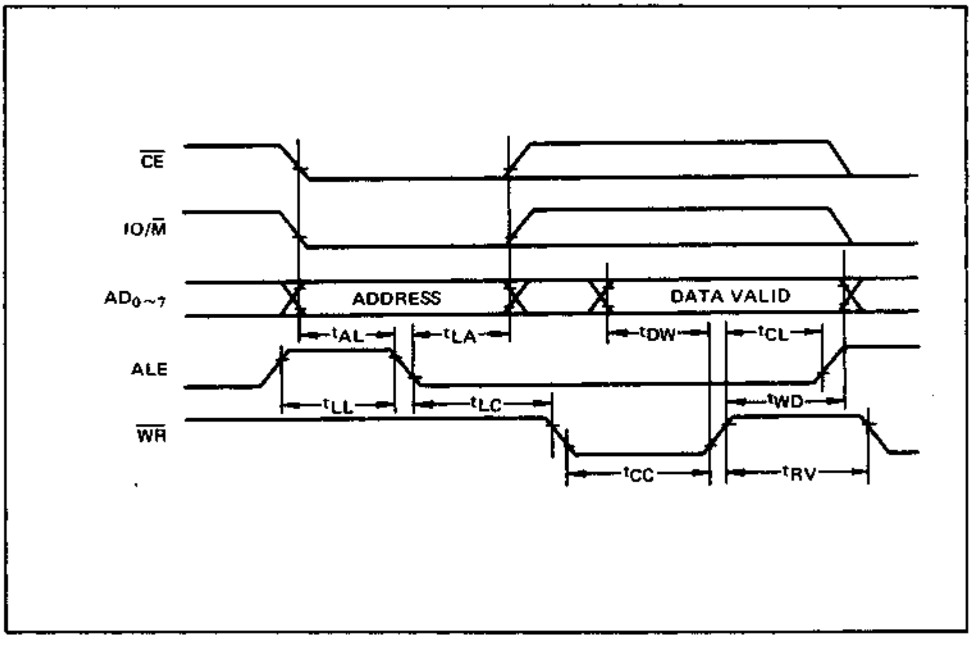
Note: Timing are measured with V_L = 0.8V and V_H = 2.2V for both input and output.

TIMING

Read Cycle



Write Cycle



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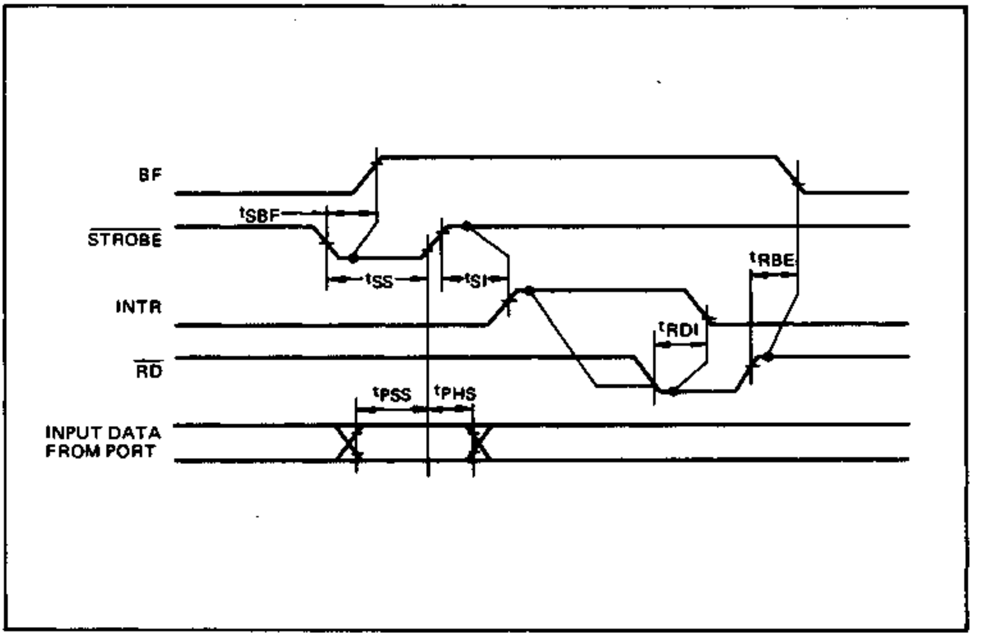
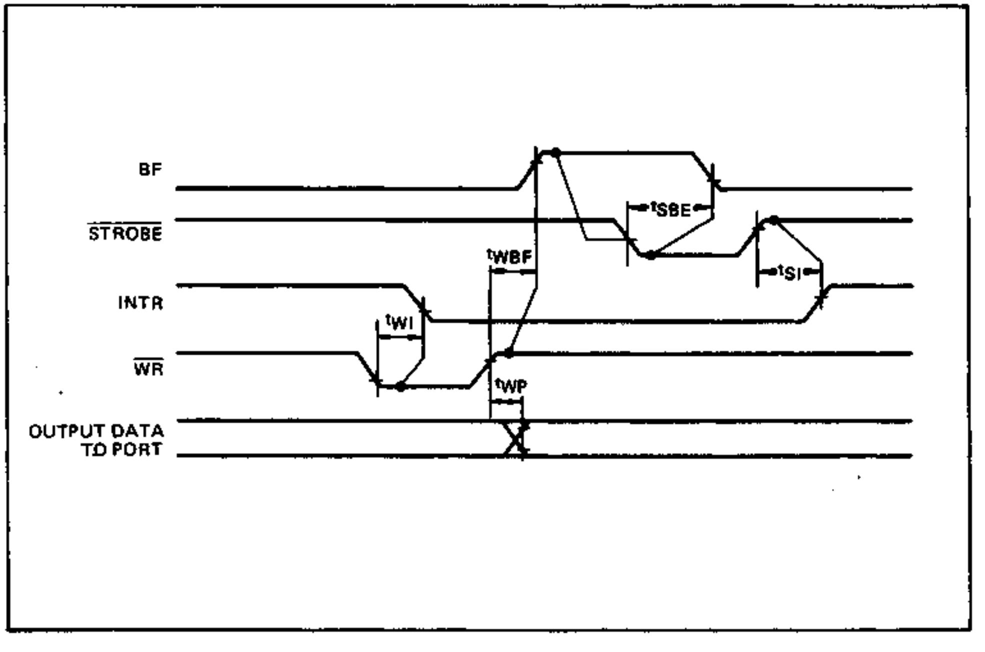
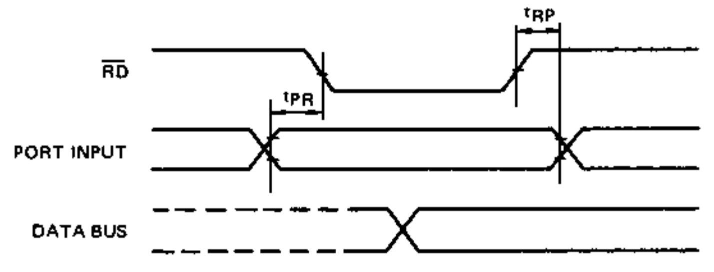
Strobe Input Mode



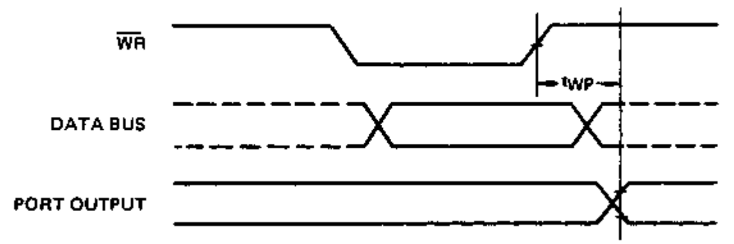
Strobe Output Mode



Basic Input Mode

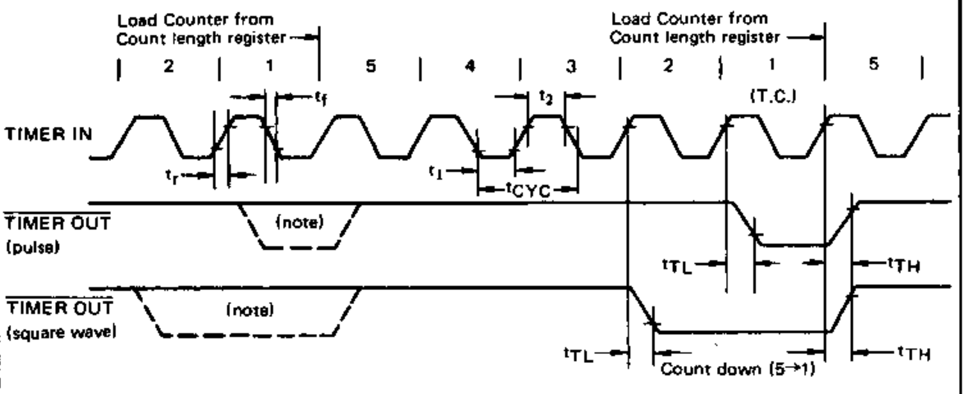


Basic Output Mode



Note: The DATA BUS timing is the same as the read and write cycles.

Timer Waveforms



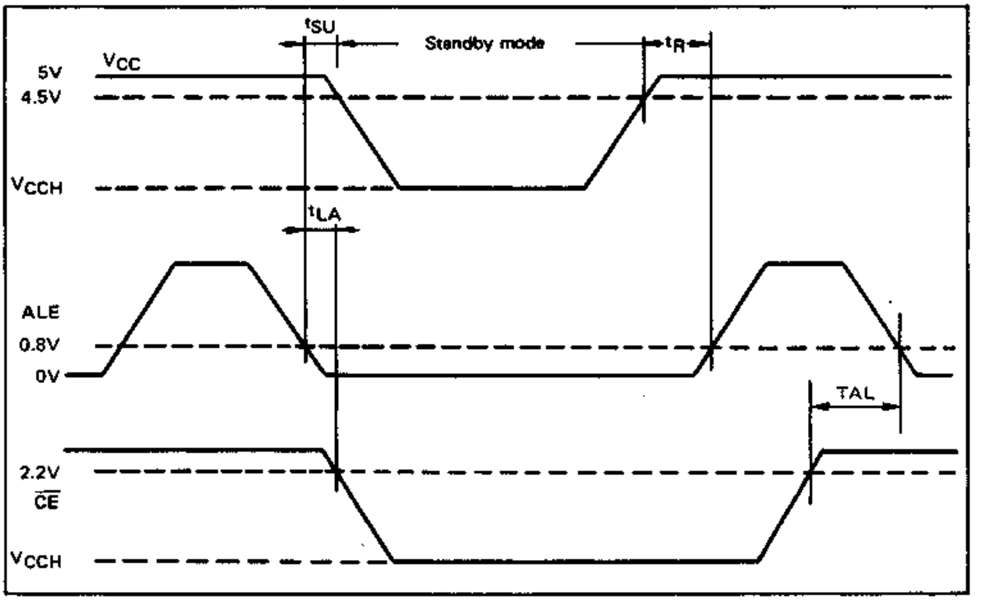
Note: Periodically output according to the output mode (m1=1) programming contents.

RAM DATA HOLD CHARACTERISTICS AT LOW SUPPLY VOLTAGE

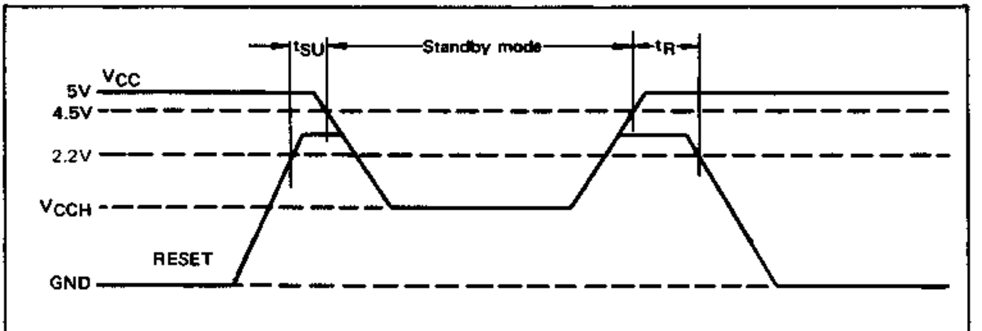
Item	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Data Holding Supply Voltage	V_{CCH}	V_{IN} = 0V or V_{CC}, ALE = 0V	2.0	–	–	V
Data Holding Supply Current	I_{CCH}	V_{CC} = V_{CCH}, ALE = 0 V_{IN} = 0V or V_{CC}	–	0.05	20	μ
Set-up Time	t_{SU}		30	–	–	ns
Hold Time	t_R		20	–	–	ns

Two ways to place device in standby mode:

(1) Method using $\overline{CE}$



(2) Method using RESET



Note: In this case, the C/S register is reset, the port is set into the input mode, and the timer stops.

PIN FUNCTIONS

Symbol	Function
RESET	A high level input to this pin resets the chip, places all three I/O ports in the input mode, resets all output latches and stops timer.
ALE	Negative going edge of the ALE (Address Latch Enable) input latches $AD_{0\sim7}$, $IO/\overline{M}$, and CE signals into the respective latches.
$AD_{0\sim7}$	Three-state, bi-directional address/data bus. Eight-bit address information on this bus is read into the internal address latch at the negative going edge of the ALE. Eight bits of data can be read from or written to the chip using this bus depending on the state of the WRITE or READ input.
$\overline{CE}$	When the CE input is high, both read and write operations to the chip are disabled.
$IO/\overline{M}$	A high level input to this pin selects the internal I/O functions, and a low level selects the memory.
$\overline{RD}$	If this pin is low, data from either the memory or ports is read onto the $AD_{0\sim7}$ lines depending on the state of the $IO/\overline{M}$ line.
$\overline{WR}$	If this pin is low, data on lines $AD_{0\sim7}$ is written into either the memory or into the selected port depending on the state of the $IO/\overline{M}$ line.
$PA_{0\sim7}$ ($PB_{0\sim7}$)	General-purpose I/O pins. Input/output directions can be determined by programming the command/status (C/S) register.
$PC_{0\sim5}$	Three pins are usable either as general-purpose I/O pins or control pins for the PA and PB ports. When used as control pins, they are assigned to the following functions: PC0: A INTR (port A interrupt) PC1: A BF (port A full) PC2: $\overline{\text{A STB}}$ (port A strobe) PC3: B INTR (port B interrupt) PC4: B BF (port B buffer full) PC5: $\overline{\text{B STB}}$ (port B strobe)
TIMER IN	Input to the counter/timer
$\overline{\text{TIMER OUT}}$	Timer output. When the present count is reached during timer operation, this pin provides a square-wave or pulse output depending on the programmed control status.
V_{CC}	3—6V power supply
GND	GND

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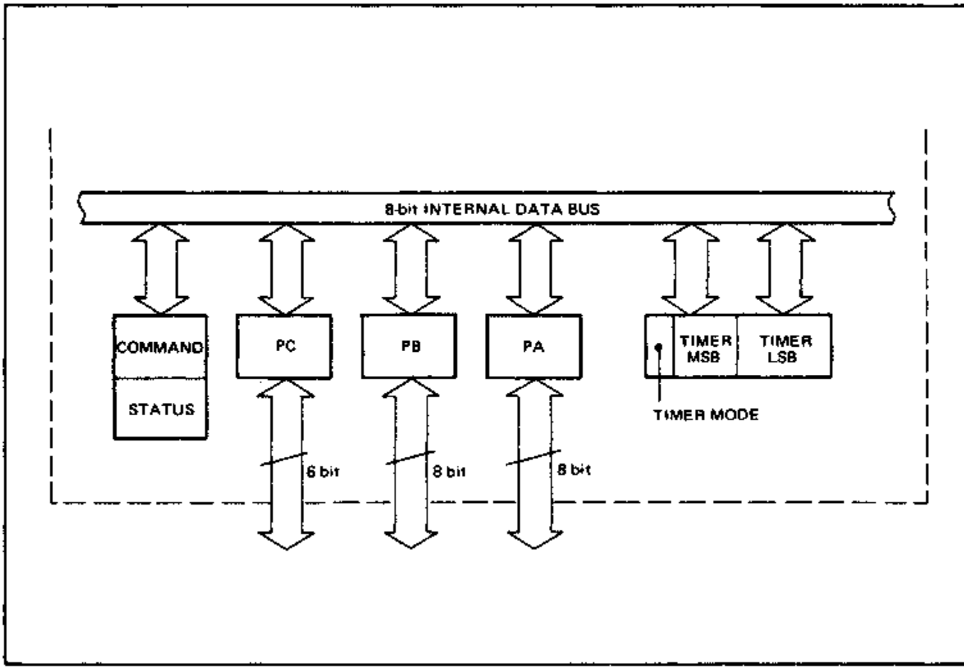
OPERATION

Description

The MSM81C55 has three functions as described below.

- 2K bit static RAM (256 words x 8 bits)
- Two 8-bit I/O ports (PA and PB) and a 6-bit I/O port (PC)
- 14-bit timer counter

The internal register is shown in the figure below, d the I/O addresses are described in the table below.



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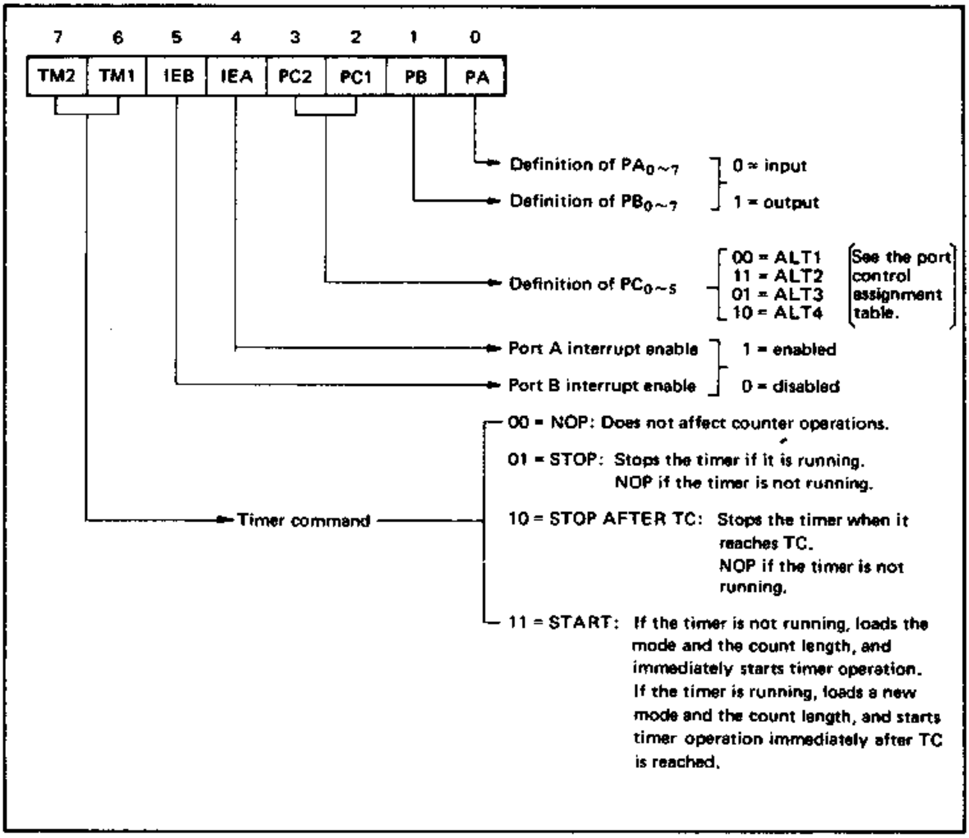
I/O Address								Selecting Register
A7	A6	A5	A4	A3	A2	A1	A0	
x	x	x	x	x	0	0	0	Internal command/status register
x	x	x	x	x	0	0	1	Universal I/O port A (PA)
x	x	x	x	x	0	1	0	Universal I/O port B (PB)
x	x	x	x	x	0	1	1	I/O port C (PC)
x	x	x	x	x	1	0	0	Timer count lower position 8 bits (LSB)
x	x	x	x	x	1	0	1	Timer count upper position 6 bits and timer mode 2 bits (MSB)

x: Don't care.

(1) Programming the Command/Status (C/S) Register

The contents of the command register can be written during an I/O cycle by addressing it with an I/O address of xxxxx000. Bit assignments for the register are shown below:



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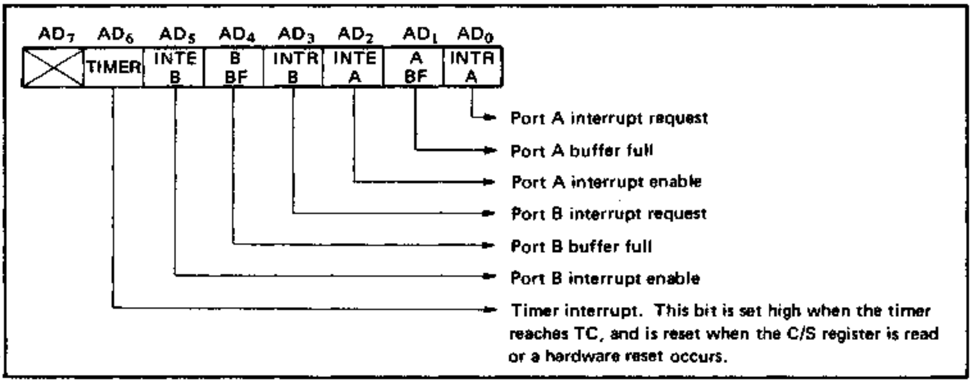
Port Control Assignment Table

Pin	ALT1	ALT2	ALT3	ALT4
PC_0	Input port	Output port	A INTR	A INTR
PC_1	Input port	Output port	A BF	A BF
PC_2	Input port	Output port	A STB	A STB
PC_3	Input port	Output port	Output port	B INTR
PC_4	Input port	Output port	Output port	B BF
PC_5	Input port	Output port	Output port	B STB

(2) Reading the C/S Register

The I/O and timer status can be accessed by reading the contents of the Status register located at I/O address xxxxx000. The status word format is shown below:



(3) PA and PB Registers

These registers may be used as either input or output ports depending on the programmed contents of the C/S register. They may also be used either in the basic mode or in the strobe mode.

I/O address of the PA register: xxxxx001

I/O address of the PB register: xxxxx010

(4) PC Register

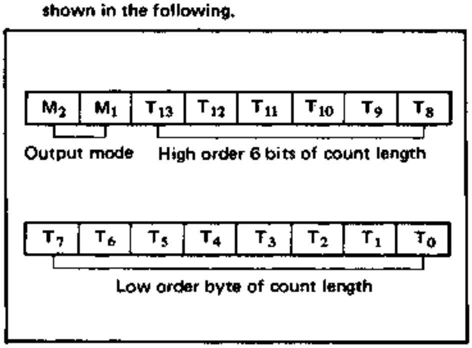
The PC register may be used as an input port, output port or control register depending on the programmed contents of the C/S register. The I/O address of the PC register is xxxxx011.

(5) Timer

The timer is a 14-bit down counter which counts TIMER IN pulses.

The low order byte of the timer register has an I/O address of xxxxx100, and the high order byte of the register has an I/O address of xxxxx101.

The count length register (CLR) may be preset with two bytes of data. Bits 0 through 13 are assigned to the count length and bits 14 and 15 specify the timer output mode. A read operation of the CLR reads the contents of the counter and the pertinent output mode. The initial value range which can initially be loaded into the counter is 2 through 3FFF hex. Bit assignments to the timer counter and possible output modes are shown in the following.



M_2	M_1	
0	0	Outputs a low-level signal in the latter half (Note 1) of a count period.
0	1	Outputs a low-level signal in the latter half of a count period, automatically loads the programmed count length, and restarts counting when the TC value is reached.
1	0	Outputs a pulse when the TC value is reached.
1	1	Outputs a pulse each time the preset TC value is reached, automatically loads the programmed count length, and restarts from the beginning.

Note 1: When counting an asymmetrical value such as (9), a high level is output during the first period of five, and a low level is output during the second period of four.

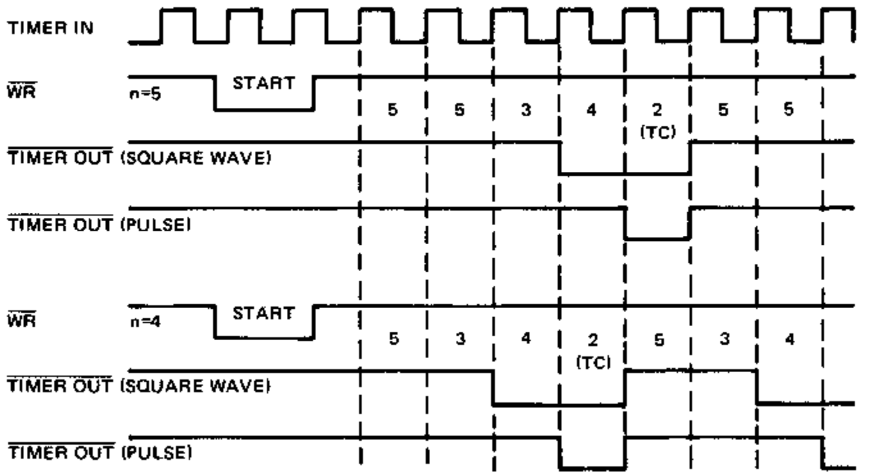
Note 2: If an internal counter of the MSM81C-55RS/GS receives a reset signal, count operation stops but the counter is not set to a specific initial value or output mode. When restarting count operation after reset, the START command must be executed again through the C/S register.

Note that while the counter is counting, you may load a new count and mode into the CLR. Before the new count and mode will be used by the counter, you must issue a START command to the counter.

Please note the timer circuit on the 81C55 is designed to be a square-wave timer, not a event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulse received. After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulse required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. STOP the counter
2. Read in the 16 bit value from the count registers.
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add ½ of the full original count (½ full count-1 if full count is odd).

Note: If you started with an odd count and you read the count registers before the third count pulse occurs, you will not be able to recognize whether one or two counts have occurred. Regardless of this, the 81C55 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.



Note: n is the value set in the CLR.
Figures in the diagram refer to counter value.

(6) Standby Mode (see page 7)

The MSM81C55 is placed in standby mode when the high level at the CE input is latched during the negative going edge of ALE. All input ports and the timer input should be pulled up or down to either V_{CC} or GND potential.

When using battery back-up, all ports should be set low or in input port mode. The timer output should be set low. Otherwise, a buffer should be added to the timer output and the battery should be connected to the power supply pins of the buffer.

By setting the reset input to a high level, the standby mode can be selected. In this case, the command register is reset, so the ports automatically set to the input mode and the timer stops.

5

OKI semiconductor

MSM82C12RS/GS

8-BIT INPUT/OUTPUT PORT

GENERAL DESCRIPTION

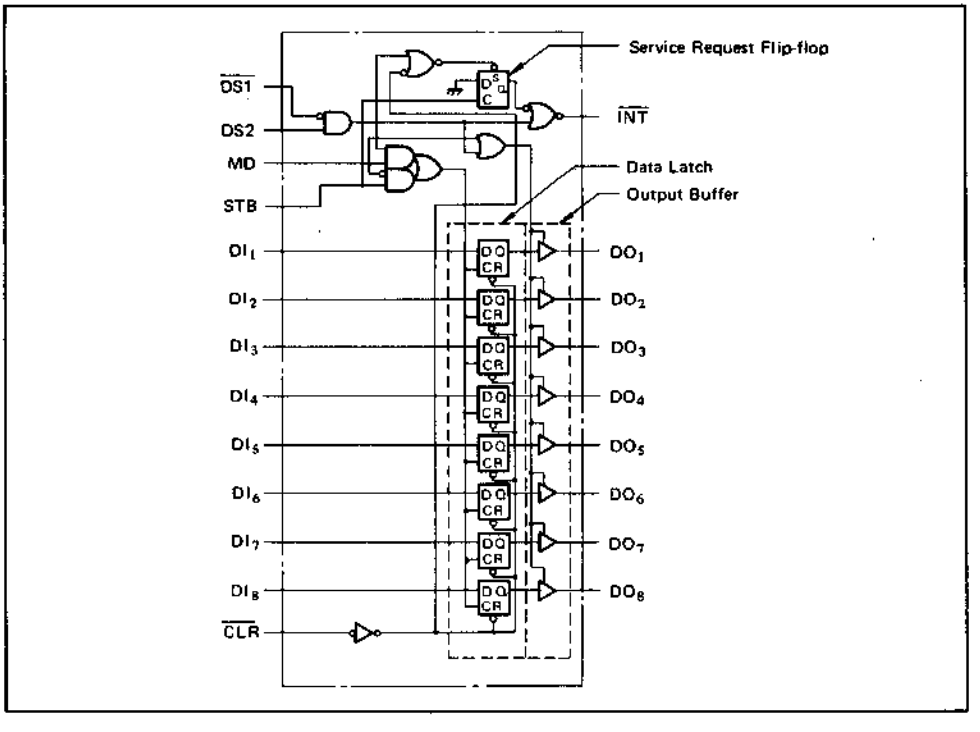
The MSM82C12 is an 8 bit input output port employing 3 μ silicon gate CMOS technology. It insures low operating power. This device incorporates a service request flip-flop for generation and control of interrupts for a CPU, in addition to an 8-bit latch circuit having a three-state output buffer.

It is effective when used as an address latch device to separate the time division bus line outputs in systems employing the MSM80C85A CPU or similar processors using multiplexed address/data bus line.

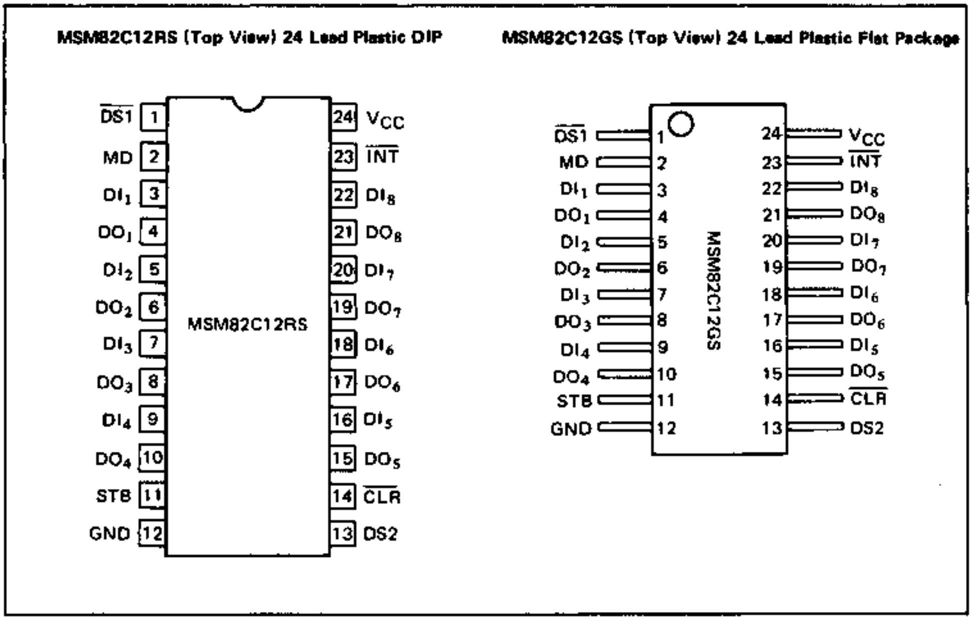
FEATURES

- Operated on low power consumption due to silicon gate CMOS.
- 3 V ~ 6 V single power supply
- Full static operation
- Parallel 8-bit data register and buffer
- Provided with an interrupt generating function through the adoption of a service request flip-flop
- Equipped with a clear terminal which operates asynchronously
- TTL compatible
- 24-pin DIP (MSM82C12RS)
- 24-pin flat package (MSM82C12GS)
- Functionally compatible with the 8212

CIRCUIT CONFIGURATION



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Item	Input/Output	Function
$DI_1 \sim DI_8$	Data input	Input	These pins are 8-bit data inputs. The data input is connected to the input D pins of the 8-bit data latch circuit built inot the device.
$DO_1 \sim DO_8$	Data output	Output	These pins are 8-bit data outputs. Each bit is composed of 3-state output buffers. These buffers can be made into enable or disable (high impedance status).
MD	Mode input	Input	This pin is a clock input for the data latch. It is also used to reset the internal service request flip-flop at the same time.
STB	Strobe input	Input	This pin is a clock input for the data latch. It is also used to reset the internal service request flip-flop at the same time.
$\overline{DS1}$, DS2	Device select input	Input	The AND of these two input functions make the status control of output buffers or becomes a clock input to the data latch. It also functions to perform set/reset of the internal service request flip-flop.
$\overline{CLR}$	Clear input	Input	This pin clears the internal data latch in low level. It also sets the internal service request flip-flop at this time. The clear is operated asynchronously to the clock.
$\overline{INT}$	Interrupt output	Output	This pin is the ouput of the internal service request flip-flop, but is inverted to ouptut it in low level operation.
V_{CC}			+5V power supply
GND			GND

5

FUNCTIONAL DESCRIPTION

Output Buffer Status Control and Data Latch Clock Input

When the input MD is at high level, the ouptut buffer is enabled and the device select input (DS1,DS2) becomes the clock input to the data latch. When the input MD is in low level, the status of the output buffer is determined by the device select input (DS1,DS2) (the output buffer is enabled when (DS1,DS2) is in high level). At this time, the input STB becomes the clock input to the data latch.

MD	($\overline{DS1}$ · DS2)	STB	$DO_1 \sim DO_8$
0	0	0	High impedance status
0	0	1	High impedance status
1	0	0	Data latch
1	0	1	Data latch
0	1	0	Data latch
0	1	1	Data in
1	1	0	Data in
1	1	1	Data in

Service Request Flip-flop

The service request flip-flop is used to generate and control the interrupt for the CPU when the MSM82C12 is used as an input/output port in a microcomputer system. The flip-flop is set asynchronously by input CLR. When the flip-flop is set, the system is in non-interrupt status.

$\overline{CLR}$	($\overline{DS1}$ · DS2)	STB	Q	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	1	0
1	1	0	1	0
1	0	0	1	1
1	0	↓	0	0

Clear

When the clear input becomes low level, the internal data latch is cleared irrespective of the clock and becomes low level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM82C12RS	MSM82C12GS	
Supply Voltage	V_{CC}	With respect to GND	−0.5 to +7		V
Input Voltage	V_{IN}		−0.5 to V_{CC}+0.5		V
Output Voltage	V_{OUT}		−0.5 to V_{CC}+0.5		V
Storage Temperature	T_{stg}		−55 to +150		°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to +85	°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA	V_{CC} = −4.5V to 5.5V, Ta = −40°C to +85°C			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −4mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (Standby)	I_{CCS}	$V_{IH} \geq V_{CC} - 0.2V$, $V_{IL} \leq 0.2V$			0.1	100	μA
Average Supply Current (active)	I_{CC}	f = 1 MHz				1	mA

AC CHARACTERISTICS

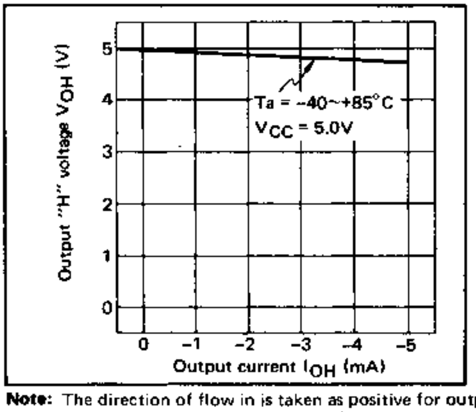
(V_{CC} = 4.5 ~ 5.5V, Ta = −40°C +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Pulse Width	t_{PW}	30			ns	Load 30pF
Data to Output Delay	t_{PD}		20	45	ns	
Write Enable to Output Delay	t_{WE}		31	60	ns	
Data Set Up Time	t_{SET}	15			ns	
Data Hold Time	t_H	30			ns	
Clear to Output Delay	t_C		19	40	ns	
Reset to Output Delay	t_R		21	45	ns	
Set to Output Delay	t_S		25	45	ns	
Output Enable Time	t_E		52	90	ns	Load 20pF + 1 kΩ
Output Disable Time	t_D		30	55	ns	

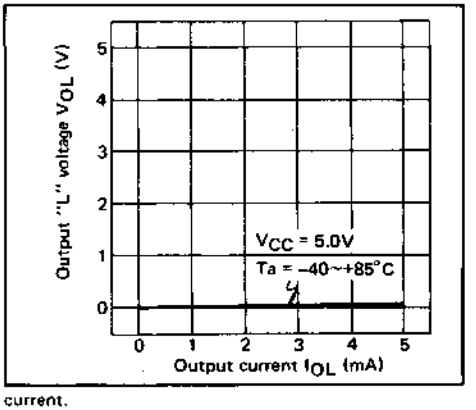
Note: TYP is measured where V_{CC} = 5 V and Ta = 25°C.
Timing is measured where VL = VH = 1.5V in both input and output.
t_E and t_D are measured at V_{OL} + 0.5V or V_{OH} − 0.5V when the two are made into high impedance status.

OUTPUT CHARACTERISTICS (DC Characteristics Reference Value)

(1) Output "H" voltage (V_{OH}) vs. output current (I_{OH})



(2) Output "L" voltage (V_{OL}) vs. output current (I_{OL})



Note: The direction of flow in is taken as positive for output current.

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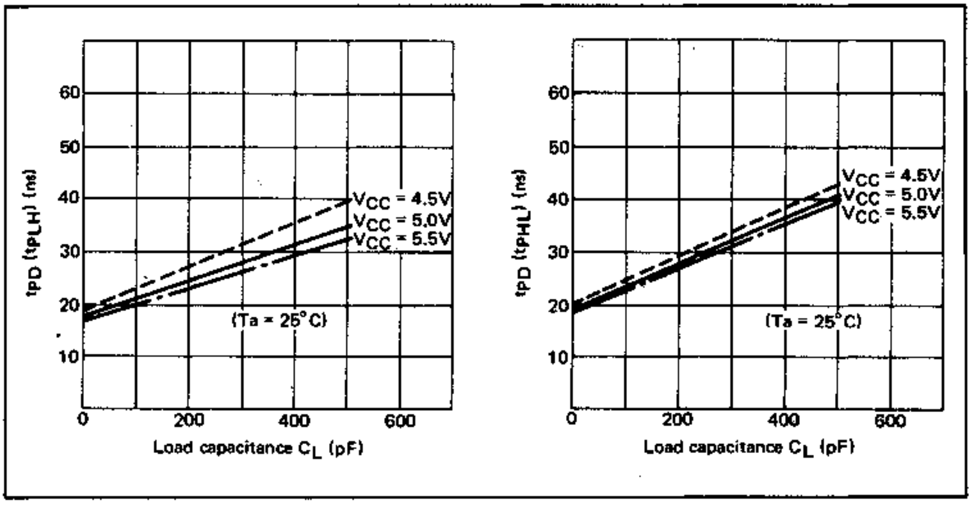
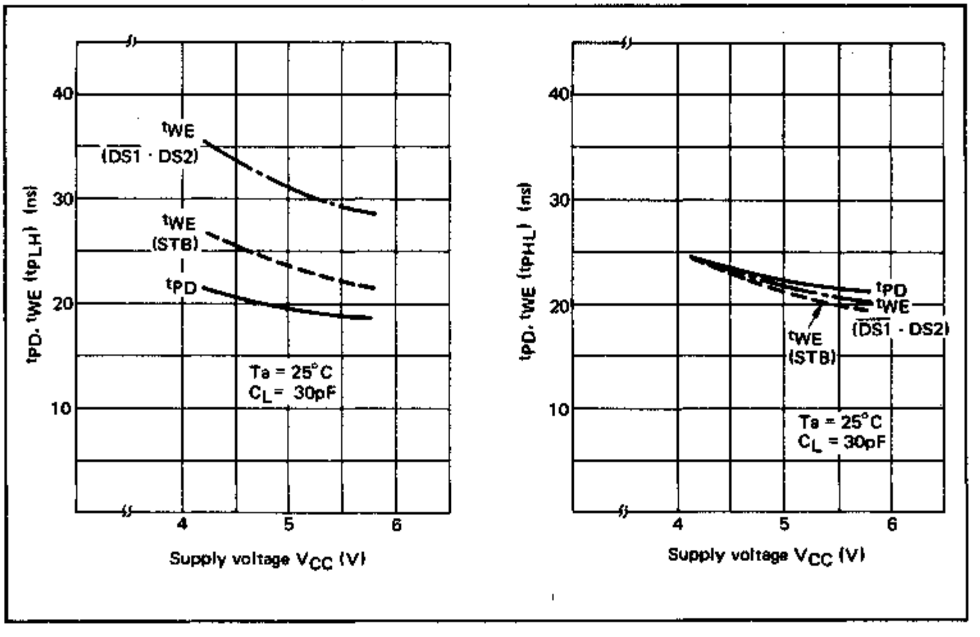
OUTPUT CHARACTERISTICS (AC Characteristics Reference Value)

(1) t_{PD} vs. load capacitance



(2) t_{PD} and t_{WE} vs. supply voltage



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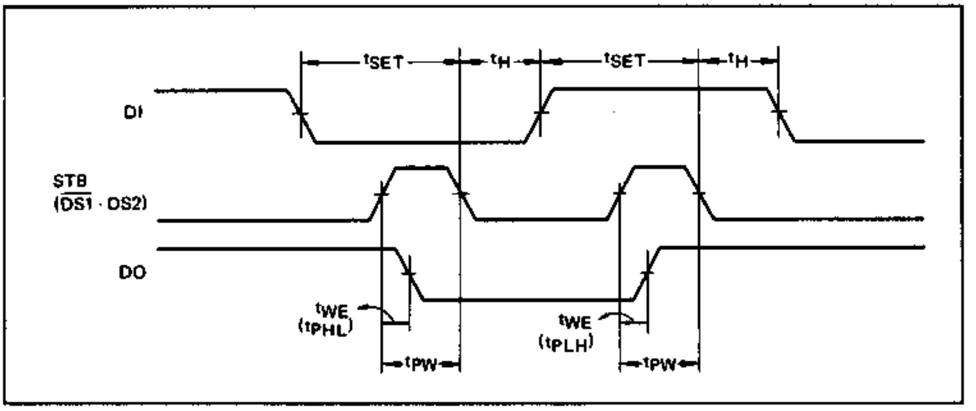
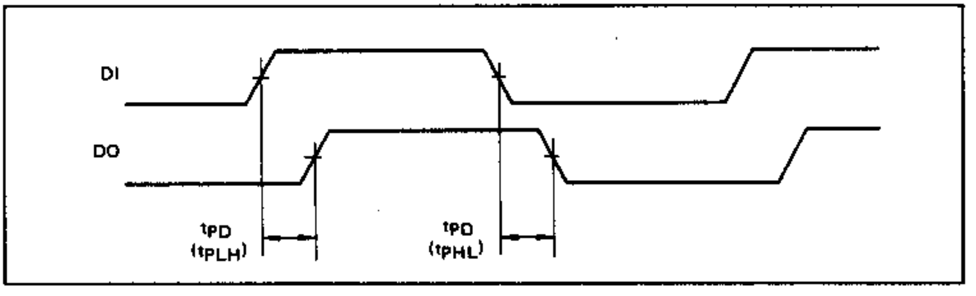
TIMING CHART

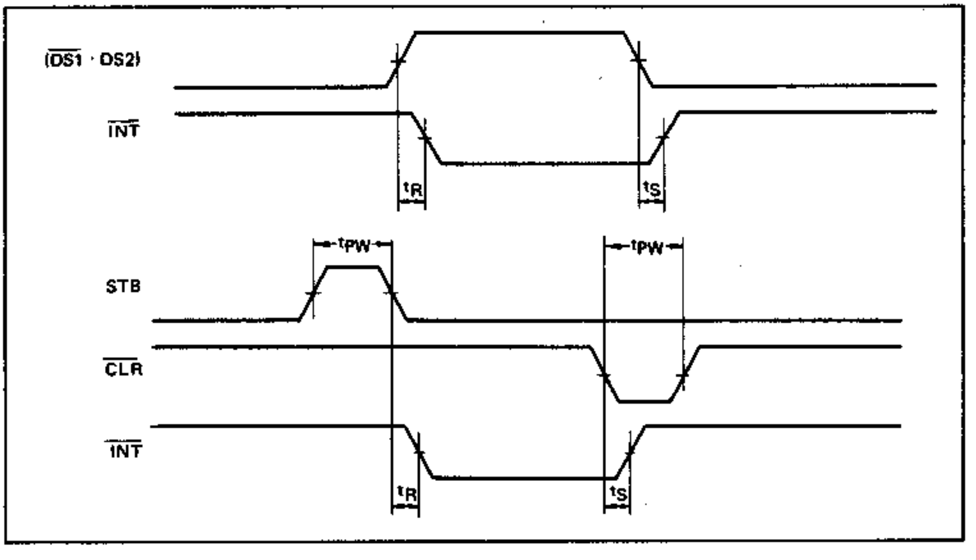
Data Latch Operation



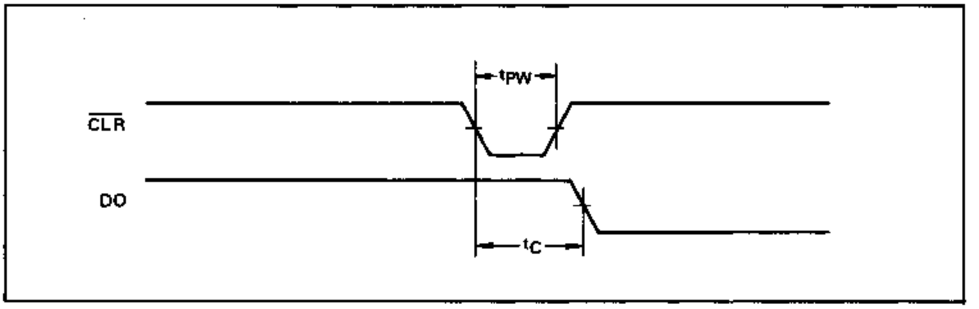
Gate Buffer Operation



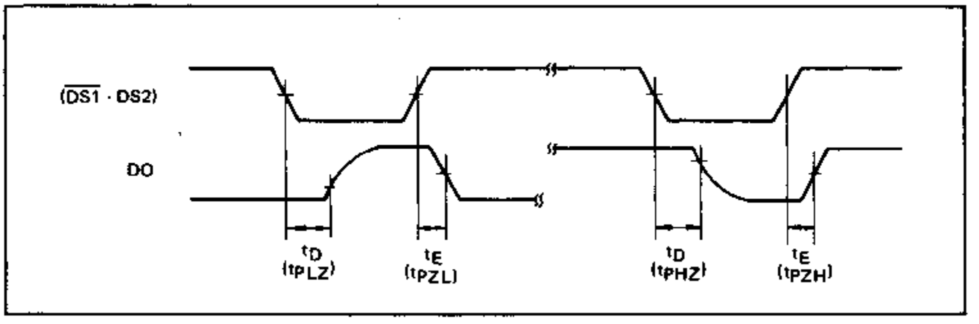
Interrupt Operation



Clear Operation



Output Buffer Enable/Disable (High Impedance Status) Operation



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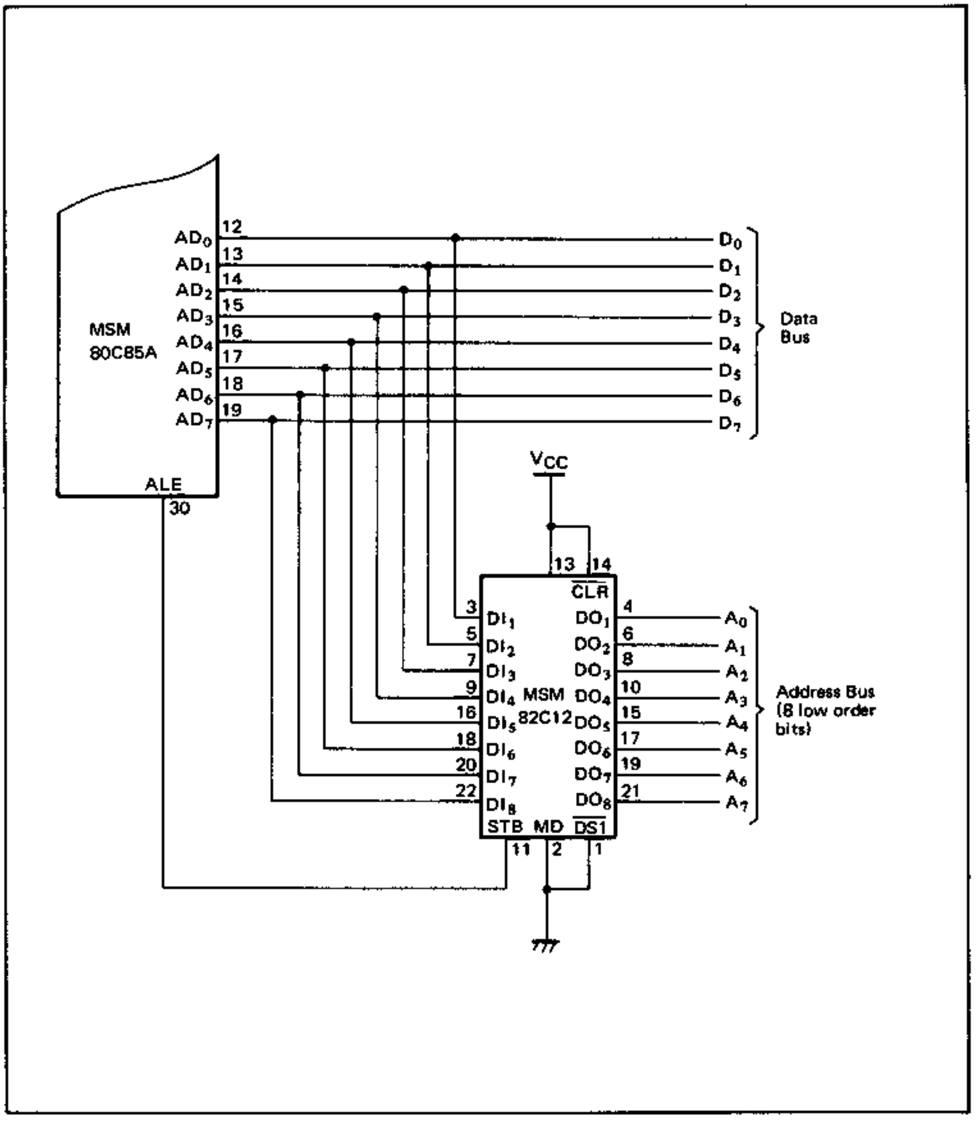
EXAMPLE OF APPLICATION OF MSM82C12

Address Latch of MSM80C85A

Used to separate the time division data bus (8 low order bits of the address bus and 8-bit data bus) into the address bus and data bus by means of the ALE (Address Latch Enable) signal.



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MSM82C37A-5RS/GS/JS

PROGRAMMABLE DMA CONTROLLER

GENERAL DESCRIPTION

The MSM82C37A-5RS/GS/JS, DMA (Direct Memory Access) controller is capable of high-speed data transfer without CPU intervention and is used as a peripheral device in microcomputer systems. The device features four independent programmable DMA channels.

Due to the use of silicon gate CMOS technology, standby current is 10 μA (max.), and power consumption is as low as 10 mA (max.) when a 5 MHz clock is generated.

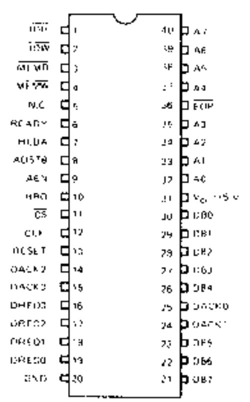
All items of AC characteristics are compatible with intel 8237A-5.

FEATURES

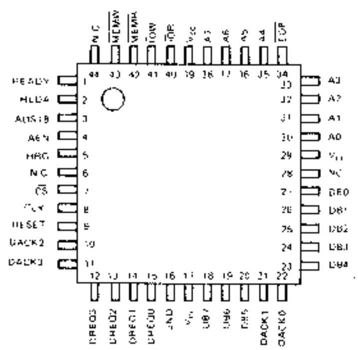
- Maximum operating frequency of 5 MHz(V_{CC}= 5 V ± 10%)
- High-speed operation at very low power consumption due to silicon gate CMOS technology
- Wide power supply voltage range of 3 to 6 V
- Wide operating temperature range from −40° to +85°C
- 4-channels independent DMA control
- DMA request masking and programming
- DMA request priority function
- DREQ and DACK input/output logic inversion
- DMA address increment/decrement selection
- Memory-to-Memory Transfers
- Channel extension by cascade connection
- DMA transfer termination by $\overline{EOP}$ input
- 40-pin DIP (MSM82C37A-5RS)
- 44-pin PLCC package (MSM82C37A-5JS)
- Intel 8237A-5 compatibility
- TTL Compatible

PIN CONNECTIONS

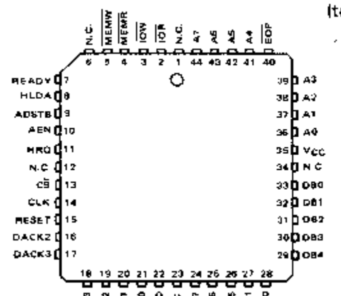
40-pin plastic DIP (top view)



44-pin plastic flat-package (top view)

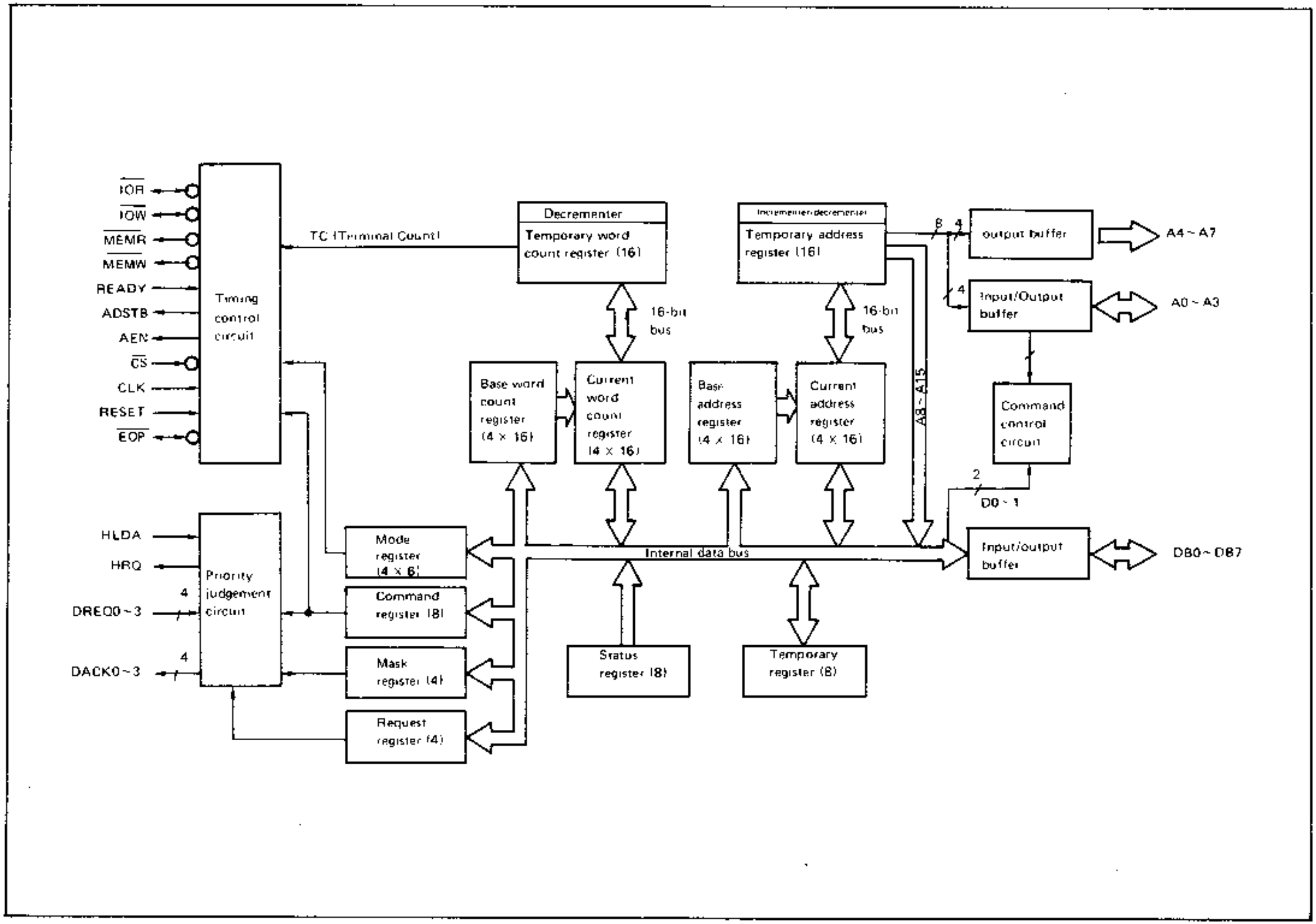


44-PIN PLCC PACKAGE (top view)



Note: N.C. (No Connection)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating			Unit
			MSM82C37A-5RS	MSM82C37A5GS	MSM82C37A-5JS	
Power supply voltage	V_{CC}	with respect to GND	−0.5 ~ +7			V
Input voltage	V_{IN}		−0.5 ~ V_{cc} + 0.5			V
Output voltage	V_{OUT}		−0.5 ~ V_{cc} + 0.5			V
Storage temperature	T_{stg}		−55 ~ +150			°C
Power dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGES

Parameter	Symbol	Range	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Maximum	Typical	Minimum	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature	T_{OP}	−40	+25	+85	°C
"L" input voltage	V_{IL}	−0.5	–	+0.8	V
"H" input voltage	V_{IH}	2.2	–	V_{CC} + 0.5	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Maximum	Typical	Minimum	Unit
"L" output voltage	V_{OL}	IOL = 3.2 mA	V_{CC} = 4.5 V ~ 5.5V Ta = −40°C ~ +85°C	—	—	0.4	V
"H" output voltage	V_{OH}	IOH = −1.0 mA		3.7	—	—	V
Input leak current	ILI	0 V ≦ V_{IN} ≦ V_{CC}		−10	—	10	μA
Output leak current	ILO	0 V ≦ V_{OUT} ≦ V_{CC}		−10	—	10	μA
Average power supply current during operations	ICC	Input frequency 5 MHz, whenRESET V_{IN} = 0 V/V_{CC}, C_L = 0 pF		—	—	10	mA
Power supply current in standby mode	ICCS	HLDA = 0 V, VIL = 0 V, VIH = VCC		—	—	10	μA

AC CHARACTERISTICS

DMA (MASTER) MODE

(Ta = -40 ~ +85°C, V_{CC} = 4.5 ~ 5.5V)

Symbol	Item	MIN	MAX	Unit	Comments
TAEL	Delay time from CLK falling edge up to AEN leading edge	—	200	ns	—
TAET	Delay time from CLK rising edge up to AEN trailing edge	—	130	ns	—
TAFAB	Delay time from CLK rising edge up to address floating status	—	90	ns	—
TAFC	Delay time from CLK rising edge up to read/write signal floating status	—	120	ns	—
TAFDB	Delay time from CLK rising edge up to data bus floating status	—	170	ns	—
TAHR	Address valid hold time to read signal trailing edge	TCY-100	—	ns	—
TAHS	Data valid hold time to ADSTB trailing edge	30	—	ns	—
TAHW	Address valid hold time to write signal trailing edge	TCY-50	—	ns	—
TAK	Delay time from CLK falling edge up to active DACK	—	170	ns	(Note 3)
	Delay time from CLK rising edge up to $\overline{EOP}$ leading edge	—	170	ns	(Note 5)
	Delay time from CLK rising edge up to $\overline{EOP}$ trailing edge	—	170	ns	—
TASM	Time from CLK rising edge up to address valid	—	170	ns	—
TASS	Data set-up time to ADSTB trailing edge	100	—	ns	—
TCH	Clock high-level time	68	—	ns	(Note 6)

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Symbol	Item	MIN	MAX	Unit	Comments
TCL	Clock low-level time	68	—	ns	(Note 6)
TCY	CLK cycle time	200	—	ns	
TDCL	Delay time from CLK rising edge to read/write signal leading edge	—	190	ns	(Note 2)
TDCTR	Delay time from CLK rising edge to read signal trailing edge	—	190	ns	(Note 2)
TDCTW	Delay time from CLK rising edge to write signal trailing edge	—	130	ns	(Note 2)
TDQ	Delay time from CLK rising edge to HRQ valid	—	120	ns	—
TEPS	$\overline{EOP}$ leading edge set-up time to CLK falling edge	40	—	ns	—
TEPW	$\overline{EOP}$ pulse width	220	—	ns	—
TFAAB	Delay time from CLK rising edge to address valid	—	170	ns	—
TFAC	Time from CLK rising edge up to active read/write signal	—	150	ns	—
TFADB	Delay time from CLK rising edge to data valid	—	200	ns	—
THS	HLDA valid set-up time to CLK rising edge	75	—	ns	—
TIDH	Input data hold time to $\overline{MEMR}$ trailing edge	0	—	ns	—
TIDS	Input data set-up time to $\overline{MEMR}$ trailing edge	170	—	ns	—
TODH	Output data hold time to $\overline{MENW}$ trailing edge	10	—	ns	—
TODV	Time from output data valid to $\overline{MEMW}$ trailing edge	125	—	ns	—
TQS	DREQ set-up time to CLK falling edge	0	—	ns	(Note 3)
TRH	READY hold time to CLK falling edge	20	—	ns	—
TRS	READY set-up time to CLK falling edge	60	—	ns	—
TSTL	Delay time from CLK rising edge to ADSTB leading edge	—	130	ns	—
TSTT	Delay time from CLK rising edge to ADSTB trailing edge	—	90	ns	—

SLAVE MODE

(Ta = -40 ~ +85°C, V_{CC} = 4.5 ~ 5.5V)

Symbol	Item	MIN	MAX	Unit	Comments
TAR	Time from address valid or $\overline{CS}$ leading edge to $\overline{IOR}$ leading edge	50	—	ns	—
TAW	Address valid set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TCW	$\overline{CS}$ leading edge set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TDW	Data valid set-up time to $\overline{IOW}$ trailing edge	130	—	ns	—
TRA	Address or $\overline{CS}$ hold time to $\overline{IOR}$ trailing edge	0	—	ns	—
TRDE	Data access time to $\overline{IOR}$ leading edge	—	140	ns	—
TRDF	Delay time to data floating status from $\overline{IOR}$ trailing edge	0	70	ns	—
TRSTD	Supply power leading edge set-up time to RESET trailing edge	500	—	ns	—
TRSTS	Time to first active $\overline{IOR}$ or $\overline{IOW}$ from RESET trailing edge	2TCY	—	ns	—
TRSTW	RESET pulse width	300	—	ns	—
TRW	$\overline{IOR}$ pulse width	200	—	ns	—
TWA	Address hold time to $\overline{IOW}$ trailing edge	20	—	ns	—
TWC	$\overline{CS}$ trailing edge hold time to $\overline{IOW}$ trailing edge	20	—	ns	—
TWD	Data hold time to $\overline{IOW}$ trailing edge	30	—	ns	—
TWWS	$\overline{IOW}$ pulse width	160	—	ns	—

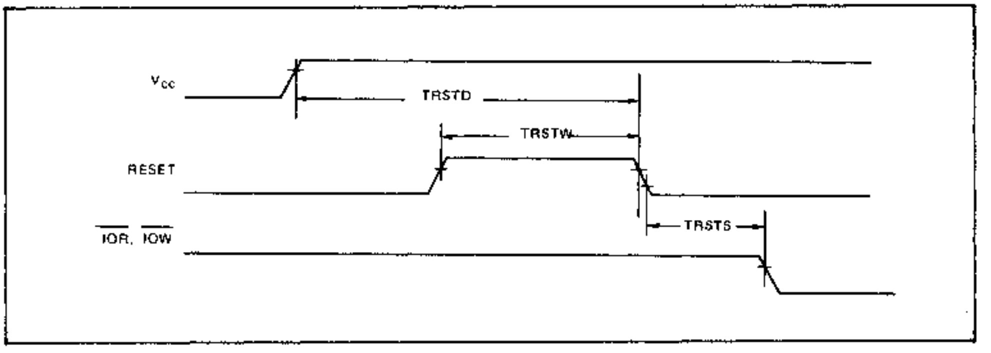
Note:

1. Output load capacitance of 150 (pF).
2. $\overline{IOW}$ and $\overline{MEMW}$ pulse widths of TCY-100 (ns) for normal writing, and 2TCY-100 (ns) for extended writing. $\overline{IOR}$ and $\overline{MEMR}$ pulse widths of 2TCY-50 (ns) for normal timing, and TCY-50 (ns) for compressed timing.
3. DREQ and DACK signal active level can be set to either low or high. In the timing chart, the DREQ signal has been set to active-high, and the DACK signal to active-low.
4. When the CPU executes continuous read or write in programming mode, the interval during which the read or write pulse becomes active must be set to at least 400 ns.
5. $\overline{EOP}$ is an open drain output. The value given is obtained when a 2.2 kohm pull-up resistance is connected to VCC.
6. Rise time and fall time is less than 10 ns.
7. Waveform measurement points for both input and output signals are 2.2 V for HIGH and 0.8 V for LOW, unless otherwise noted.

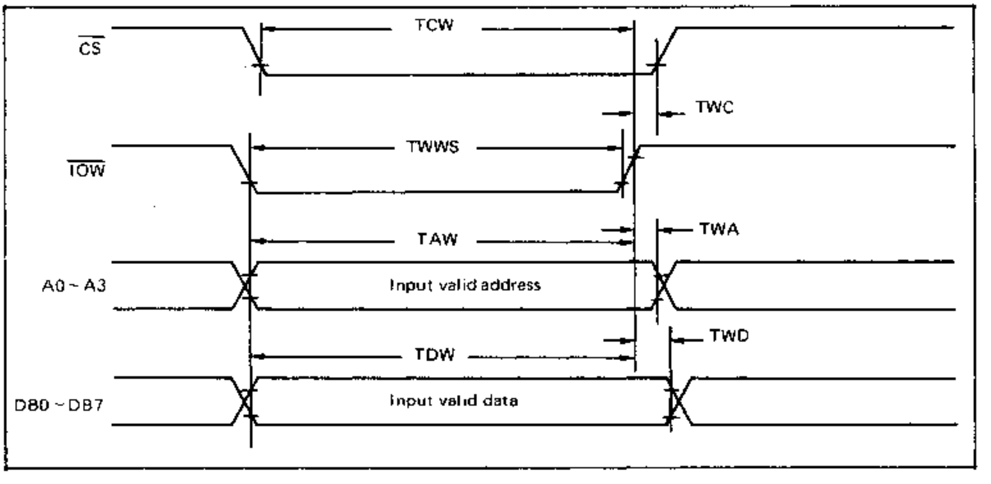
5

TIME CHART

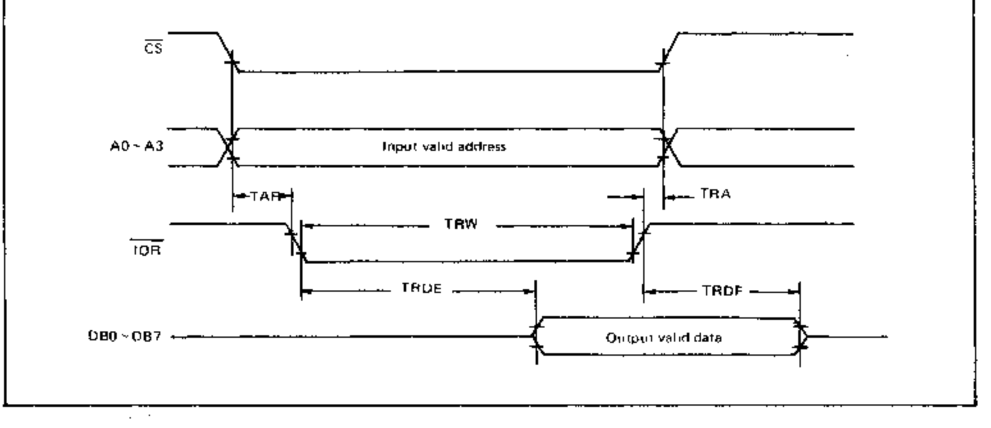
RESET TIMING



SLAVE MODE WRITE TIMING



SLAVE MODE READ TIMING



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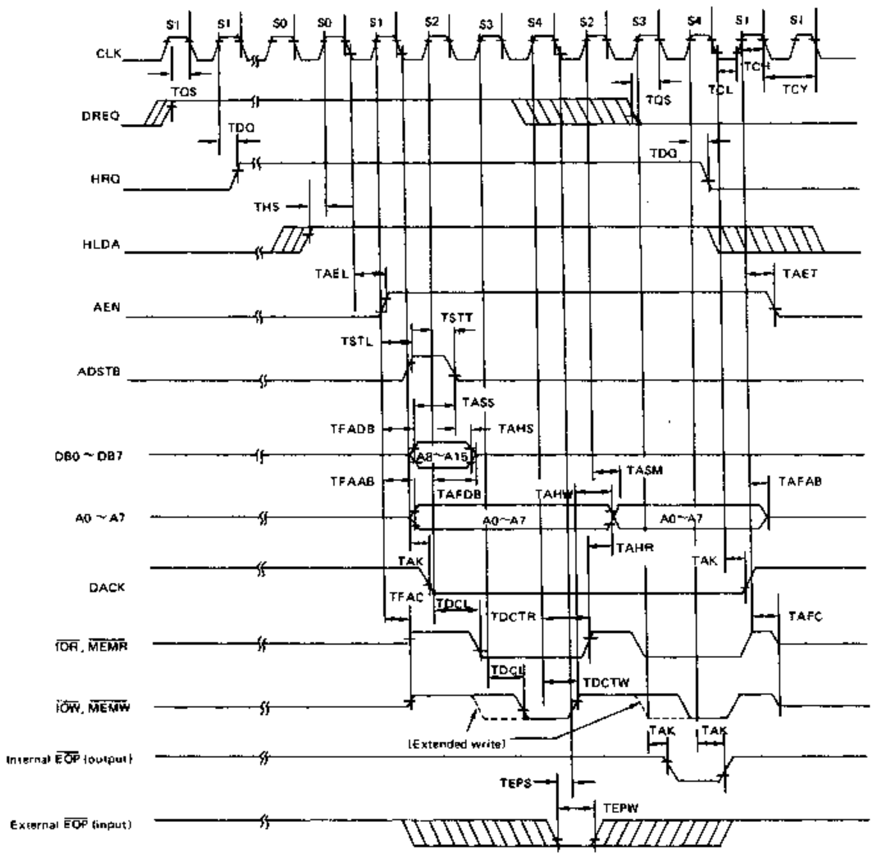
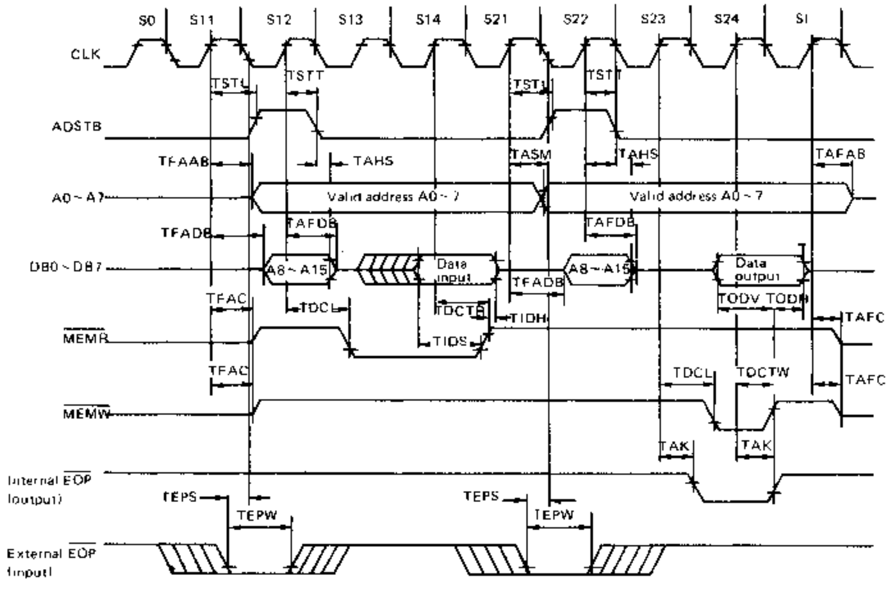
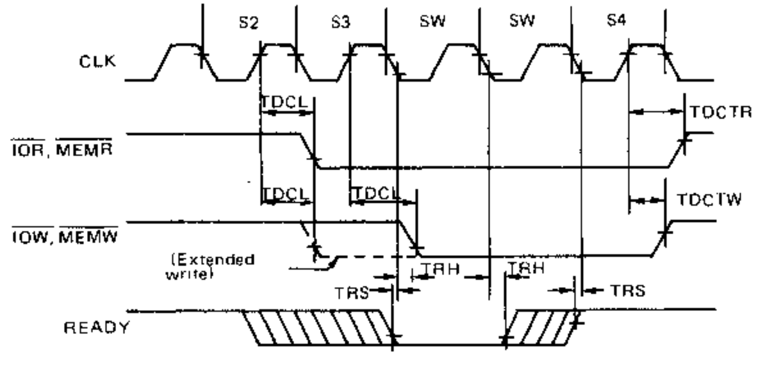
DMA TRANSFER TIMING



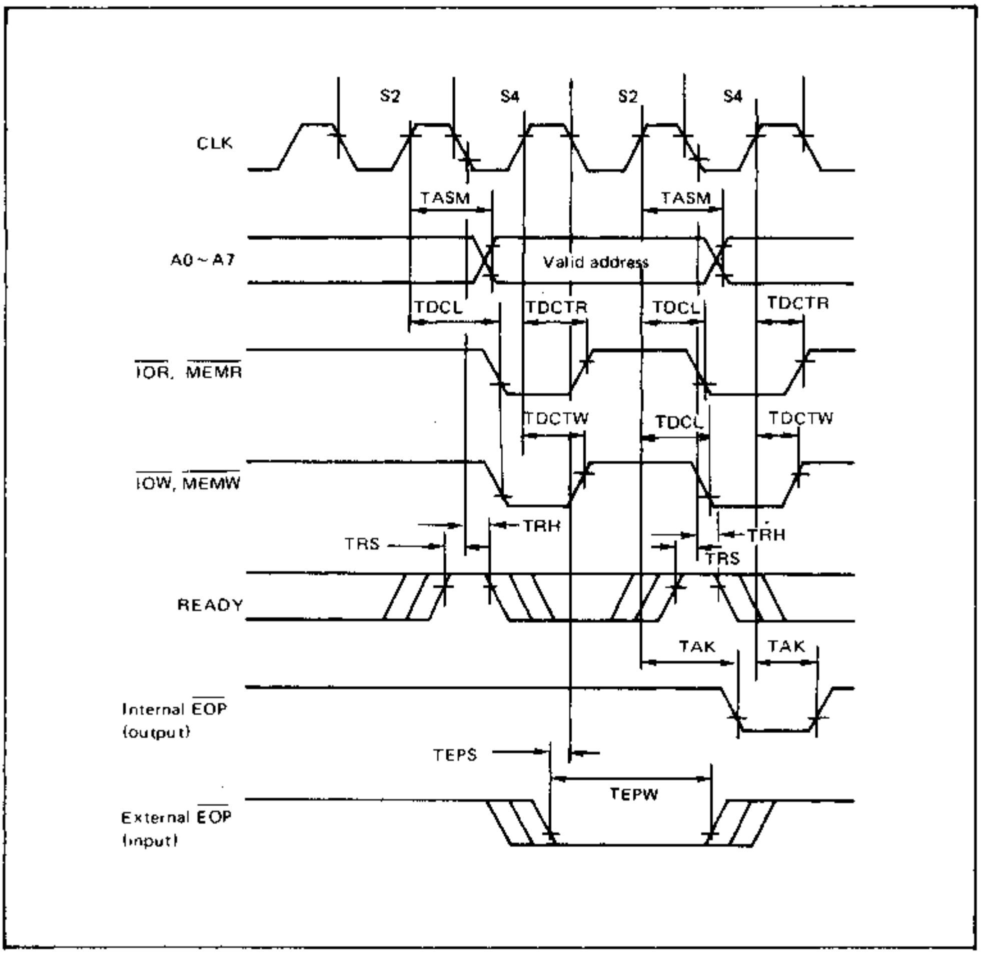
MEMORY TO MEMORY TRANSFER TIMING



READY TIMING



COMPRESSED TRANSFER TIMING



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PIN FUNCTIONS

Symbol	Pin name	Input/ output	Function
V_{CC}	Power		+5 V power supply.
GND	Ground		Ground (0 V) connection.
CLK	Clock	Input	Control of MSM82C37A-5 internal operations and data transfer speed.
$\overline{CS}$	Chip select	Input	$\overline{CS}$ is active-low input signal used for the CPU to select the MSM82C37A-5 as an I/O device in an idle cycle.
RESET	Reset	Input	RESET is active-high asynchronous input signal used to clear command, status, request, temporary registers, and first/last F/F, and to set mask register. The MSM82C37A-5 enters an idle cycle following a RESET.
READY	Ready	Input	The read or write pulse width can be extended to accomodate slow access memories and I/O devices when this input is switched to low level. Note this input must not change within the prescribed set-up/hold time.
HLDA	Hold acknowledge	Input	HLDA is active-high input signal used to indicate that system bus control has been released when a hold request is received by the CPU.
DREQ0 ~ DREQ3	DMA request 0 ~ 3 channels	Input	DREQ is asychronous DMA transfer request input signals. Although these pins are switched to active-high by reset, they can be programmed to become active-low. DMA requests are received in accordance with a prescribed order of priority. DREQ must be held until DACK becomes active.
DB0 ~ DB7	Data bus 0 ~ 7	Input/ output	DB is bidirectional three-state signals connected to the system data bus, and which is used as an input/output of MSM82C37A-5 internal registers during idle cycles, and as an output of the eight higher order bits of transfer addresses during active cycles. Also used as input and output of transfer data during memory-memory transfers.
$\overline{IOR}$	I/O read	Input/ output	$\overline{IOR}$ is active-low bidirectional three-state signal used as an input control signal for CPU reading of MSM82C37A-5 internal registers during idle cycles, and as an output control signal for reading I/O device transfer data in writing transfers during active cycles.
$\overline{IOW}$	I/O write	Input/ output	$\overline{IOW}$ is active-low bidirectional three-state signal used as an input control signal for CPU writing of MSM82C37A-5 internal registers during idle cycles, and as an output control signal for writing I/O device transfer data in writing transfers during active cycles.

Symbol	Pin name	Input/ output	Function
$\overline{EOP}$	End of process	Input/ output	$\overline{EOP}$ is active-low bidirectional three-state signal. Unlike other pins, this pin is an N-channel open drain. During DMA operations, a low-level output pulse is obtained from this pin if the channel word count changes from 0000H to FFFFH. And DMA transfers can be terminated by pulling the $\overline{EOP}$ input to low level. Both of these actions are called terminal count (TC). When an internal or external $\overline{EOP}$ is generated, the MSM82C37A-5 terminates the transfer and resets the DMA request. When the $\overline{EOP}$ pin is not used, it is necessary to hold the pin at high level by pull-up resistance to prevent the input of an $\overline{EOP}$ by error. Also note that the $\overline{EOP}$ function cannot be satisfied in cascade mode.
A0 ~ A3	Address 0 ~ 3	Input/ output	A0~A3 is bidirectional three-state signals used as input signals for specifying the MSM82C37A-5 internal register to be accessed by the CPU during idle cycles, and as an output the four lower order bits of the transfer address during active cycles.
A4 ~ A7	Address 4 ~ 7	Output	A4~A7 is three-state signals used as an output the four higher order bits of the transfer address during active cycles.
HRQ	Hold request	Output	HRQ is active-high signal used as an output of hold request to the CPU for system data bus control purposes. After HRQ has become active, at least one clock cycle is required before HLDA becomes active.
DACK0 ~ DACK3	DMA acknowledge 0 ~ 3 channels	Output	DACK is output signals used to indicate that DMA transfer to peripheral devices has been permitted. (Available in each channel.) Although these pins are switched to active-low when reset, they can be programmed to become active-high. Note that there is no DACK output signal during memory-memory transfers.
AEN	Address enable	Output	AEN is active-high output signal used to indicate that output signals sent from the MSM82C37A-5 to the system are valid. And in addition to enabling external latch to hold the eight higher order bits of the transfer address, this signal is also used to disable other system bus buffers.

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Symbol	Pin name	Input/ output	Function
ADSTB	Address strobe	Output	ADSTB is active-high signal used to strobe the eight higher order bits of the transfer address by external latch.
$\overline{MEMR}$	Memory read	Output	$\overline{MEMR}$ is active-low three-state output signal used as a control signal in reading data from memory during read transfers and memory-memory transfers.
$\overline{MEMW}$	Memory write	Output	$\overline{MEMW}$ is active-low three-state output signal used as a control signal in writing data into memory during write transfers and memory-memory transfers.

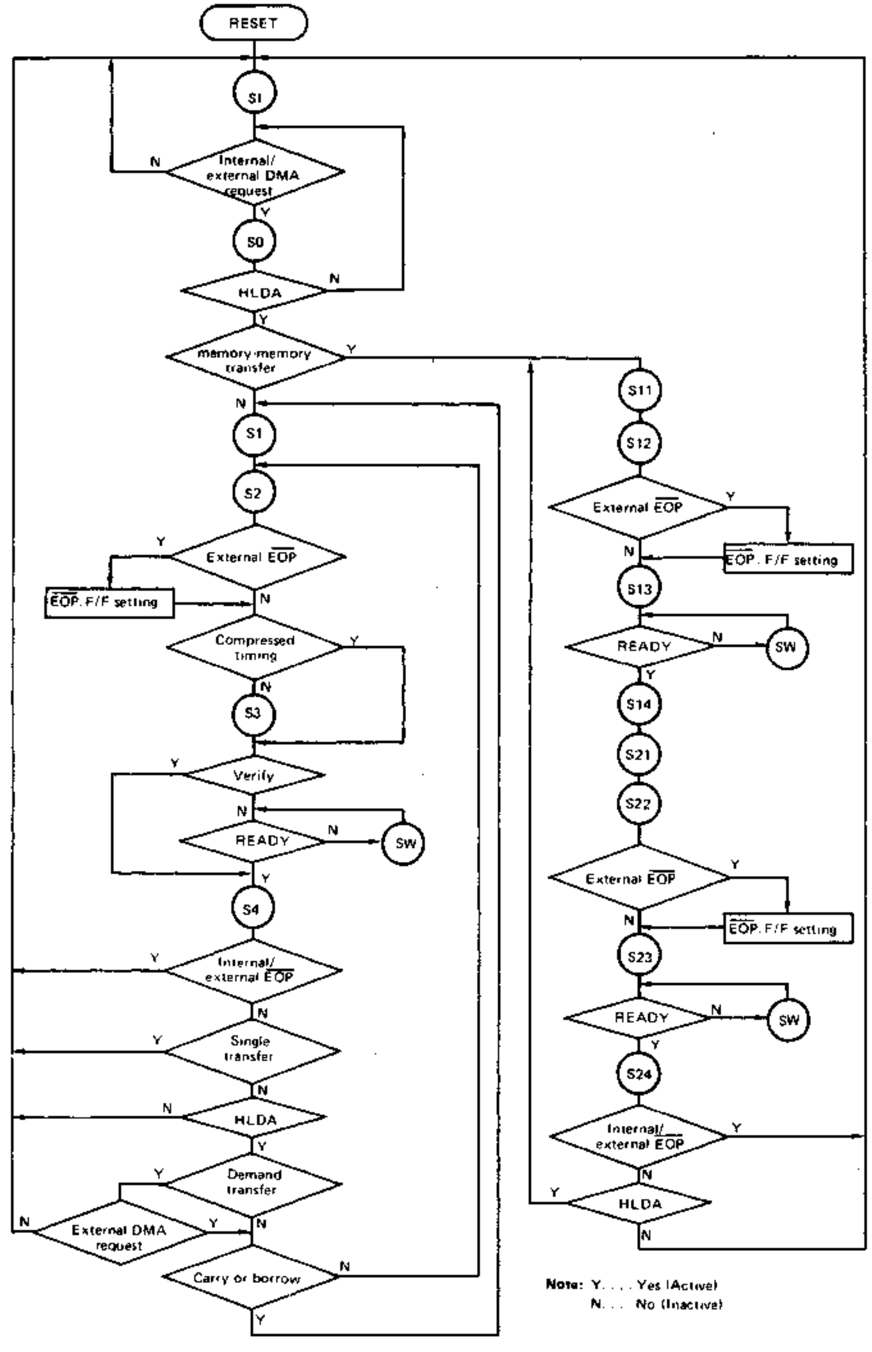

Fig. 1 DMA operation state transition diagram

OUTLINE OF FUNCTIONS

The MSM82C37A-5 consists of five blocks = three logic sections, an internal register section, and a counter section.

The logic sections include a timing control block where the internal timing and external control signals are generated, a command control block where each instruction from the CPU is decoded, and a priority decision block where the order of DMA channel priority is determined. The purpose of the internal register section is to hold internal states and instructions from the CPU, while the counter section computes addresses and word counts.

DESCRIPTION OF OPERATIONS

The MSM82C37A-5 operates in two cycles (called the idle and active cycles) which are divided into independent states. Each state is commenced by a clock falling edge and continues for a single clock cycle. The transition from one state to the next in DMA operations is outlined in Figure 1.

IDLE CYCLE

The idle cycle is entered from the SI state when there is no valid DMA request on any MSM82C37A-5 channel. During this cycle, DREQ and $\overline{CS}$ inputs are monitored during each cycle. When a valid DMA request is then received, an active cycle is commenced. And if the HLDA and $\overline{CS}$ inputs are at low level, a programming state is started with MSM82C37A-5 reading or writing executed by $\overline{IOR}$ or $\overline{IOW}$. Programming details are described later.

ACTIVE CYCLE

If a DMA request is received in an unmasked channel while the MSM82C37A-5 is in an idle cycle, or if a software DREQ is generated, the HRQ is changed to high level to commence an active cycle. The initial state of an active cycle is the S0 state which is repeated until the HLDA input from the CPU is changed to high level. (But because of internal operational reasons, a minimum of one clock cycle is required for the HLDA is be changed to high level by the CPU after the HRQ has become high level. That is, the S0 state must be repeated at least twice.)

After the HLDA has been changed to high level, the S0 state proceeds to operational states S1 thru S4 during I/O-memory transfers, or to operational states S11 thru S14 and S21 thru S24 during memory-memory transfers.

If the memory or I/O device cannot be accessed within the normal timing, an SW state (wait state) can be inserted by a READY input to extend the timing.

DESCRIPTION OF TRANSFER TYPES

MSM82C37A-5 transfers between an I/O and memory devices, or transfers between memory devices. The three types of transfers between I/O and memory devices are read, write, and verify.

I/O-MEMORY TRANSFERS

The operational states during an I/O-memory transfer are S1, S2, S3, and S4.

In the S1 state, an AEN output is changed to high level to indicate that the control signal from the MSM82C37A-5 is valid. The eight lower order bits of the transfer address are obtained from A0 thru A7, and the eight higher order bits are obtained from DB0 thru DB7. The ADSTB output is changed to high level at this time to set the eight higher order bits in an external address latch, and the DACK output is made active for the channel where the DMA request is acknowledged. Where there is no change in the eight higher bit transfer address during demand and block mode transfers, however, the S1 state is omitted.

In the S2 state, the $\overline{IOR}$ or $\overline{MEMR}$ output is changed to low level.

In the S3 state, $\overline{IOW}$ or $\overline{MEMW}$ is changed to low level. Where compressed timing is used, however, the S3 state is omitted.

The S2 and S3 states are I/O or memory input/output timing control states.

In the S4 state, $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, and $\overline{MEMW}$ are changed to high level, and the word count register is decremented by 1 while the address register is incremented (or decremented) by 1. This completes the DMA transfer of one word.

Note that in I/O-memory transfers, data is transferred directly without being taken in by the MSM82C37A-5. The differences in the three types of I/O-memory transfers are indicated below.

READ TRANSFER

Data is transferred from memory to the I/O device by changing $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ to low level. $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$ are kept at high level during this time.

WRITE TRANSFER

Data is transferred from the I/O device to memory by changing $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$ to low level. $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ are kept at high level during this time.

Note that writing and reading in these write and read transfers are with respect to the memory.

VERIFY TRANSFER

Although verify transfers involve the same operations as write and read transfers (such as transfer address generation and $\overline{\text{EOP}}$ input responses), they are in fact pseudo transfers where all I/O and memory reading/writing control signals are kept inactive. READY inputs are disregarded in verify transfers.

MEMORY-MEMORY TRANSFERS

Memory-memory transfers are used to transfer data blocks from one memory area to another.

Memory-memory transfers require a total of eight states to complete a single transfer four states (S11 thru S14) for reading from memory, and four states (S21 thru S24) for writing into memory. These states are similar to I/O-memory transfer states, and are distinguished by using two-digit numbers.

In memory-memory transfers, channel 0 is used for reading data from the source area, and channel 1 is used for writing data into the destination area. During the initial four states, data specified by the channel 0 address is read from the memory when MEMR is made active, and is taken in the MSM82C37A-5 temporary register. Then during the latter four states, the data in the temporary register is written in the address specified by channel 1. This completes the transfer of one byte of data. With channel 0 and channel 1 addresses subsequently incremented (or decremented) by 1, and channel 0, 1 word count decremented by 1, this operation is repeated. The transfer is terminated when the word count reaches FFFF(H) from 0000(H), or when an $\overline{\text{EOP}}$ input is applied from an external source. Note that there is no DACK output signal during this transfer.

The following preparations in programming are requiring to enable memory-memory transfers to be started.

COMMAND REGISTER SETTING

Memory-memory transfers are enabled by setting bit 0. Channel 0 address can be held for all transfers by setting bit 1. This setting can be used to enable 1-word contents of the source area to be written into the entire destination area.

MODE REGISTER SETTING

The transfer type destination is disregarded in channels 0 and 1. Memory-memory transfers are always executed in block transfer mode.

REQUEST REGISTER SETTING

Memory-memory transfers are started by setting the channel 0 request bit.

MASK REGISTER SETTING

Mask bits for all channels are set to prevent selection of any other channel apart from channel 0.

WORD COUNT REGISTER SETTING

The channel 1 word count is validated, while the channel 0 word count is disregarded.

In order to autoinitialize both channels, it is necessary to write the same values into both word count registers.

DESCRIPTION OF OPERATION MODES

SINGLE TRANSFER MODE

In single transfer mode, only one word is transferred, and the addresses are incremented (or decremented) by 1 while the word count is decremented by 1. The HRQ is then changed to low level to return the bus control to the CPU. If DREQ remains active after completion of a transfer, the HRQ is changed to low level. After the HLDA is changed to low level by the CPU, and then changes the HRQ back to high level to commence a fresh DMA cycle. For this reason, a machine cycle can be inserted between DMA cycles by the CPU.

BLOCK TRANSFER MODE

Once a DMA transfer is started in block mode, the transfer is continued until terminal count (TC) status is reached.

If DREQ remains active until DACK becomes active, the DMA transfer is continued even if DREQ becomes inactive.

DEMAND TRANSFER MODE

The DMA transfer is continued in demand transfer mode untiL DREQ is no longer active, or until TC status is reached.

During a DMA transfer, intermediate address and word count values are held in the current address and current word count registers. Consequently, if the DMA transfer is suspended as a result of DREQ becoming inactive before TC status is reached, and the DREQ for that channel is then made active again, the suspended DMA transfer is resumed.

CASCADE TRANSFER MODE

When DMA transfers involving more than four channels are required, connecting a multiple number of MSM82C37A-5 devices in a cascade connection (see Figure 2) enables a simple system extension. This mode is set by setting the first stage MSM82C37A-5 channel to cascade mode. The DREQ and DACK lines for the first stage MSM82C37A-5 channel set to cascade mode are connected to the HRQ and HLDA lines of the respective MSM82C37A-5 devices in the second stage. The first stage MSM82C37A-5 DACK signal must be set to active-high, and the DREQ signal to active-low.

Since the first stage MSM82C37A-5 is only used functionally in determining the order of priority of each channel when cascade mode is set, only DREQ and DACK are used – all other inputs are disregarded. And since the system may be hung up if the DMA transfer is activated by software DREQ, do not set a software DREQ for channels where cascade mode has been set.

In addition to the dual stage cascade connection shown in Figure 2, triple stage cascade connections are possible with the second stage also set to cascade mode.

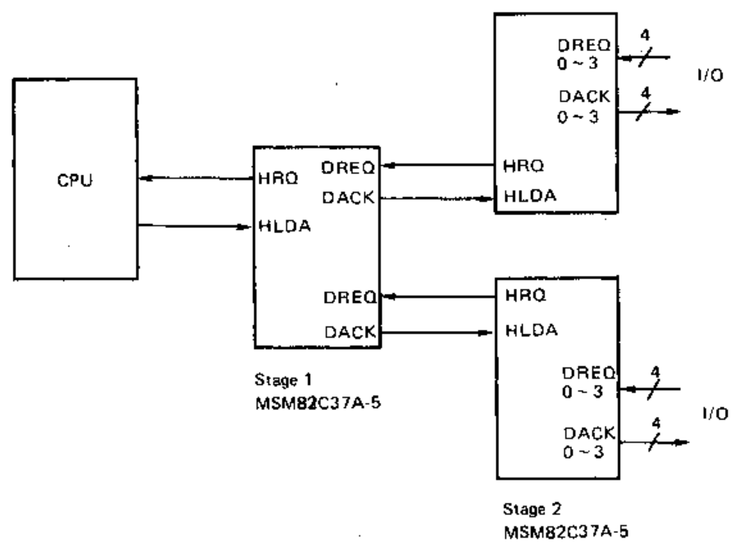

Fig. 2 MSM82C37A-5 cascade connection system

AUTOINITIALIZE MODE

Setting bit 4 of the mode register enables autoinitialization of that channel. Following TC generation, autoinitialize involves writing of the base address and the base word count register values in the respective current address and current word count registers. The same values as in the current registers are written in the base registers by the CPU, and are not changed during DMA transfers.

When a channel has been set to autoinitialize, that channel may be used in a second transfer without involving the CPU and without the mask bit being reset after the TC generation.

PRIORITY MODES

The MSM82C37A-5 makes use of two priority decision modes, and acknowledges the DMA channel of highest priority among the DMA requesting channels.

FIXED PRIORITY MODE

In fixed priority mode, channel 0 has the highest priority, followed by channel 1, 2, and 3 in that order.

ROTATING PRIORITY MODE

In rotating priority mode, the order of priority is changed so that the channel where the current DMA transfer has been completed is given lowest priority. This is to prevent any one channel from monopolizing the system. The fixed priority is regained immediately after resetting.

Table 1 MSM82C37A-5 priority decision modes

Priority mode		Fixed	Rotating			
Service terminated channel		–	CH0	CH1	CH2	CH3
Order of priority for next DMA	Highest	CH0	CH1	CH2	CH3	CH0
	↕	CH1	CH2	CH3	CH0	CH1
		CH2	CH3	CH0	CH1	CH2
	Lowest	CH3	CH0	CH1	CH2	CH3

COMPRESSED TIMING

Setting the MSM82C37A-5 to compressed timing mode enables the S3 state used in extension of the read pulse access time to be omitted (if permitted by system structure) for two or three clock cycle DMA transfers. If the S3 state is omitted, the read pulse width becomes the same as the write pulse width with the address updated in S2 and the read or write operation executed in S4. This mode is disregarded if the transfer is a memory-memory transfer. transfer.

EXTENDED WRITING

When this mode is set, the $\overline{IOW}$ or $\overline{MEMW}$ signal which normally appears during the S3 state is obtained during the S2 state, thereby extending the write pulse width. The purpose of this extended write pulse is to enable the system to accomodate memories and I/O devices where the access time is slower. Although the pulse width can also be extended by using READY, that involves the insertion of a SW state to increase the number of states.

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DESCRIPTION OF INTERNAL REGISTERS

CURRENT ADDRESS REGISTER

Each channel is equipped with a 16-bit long current address register where the transfer address is held during DMA transfers. The register value is incremented (or decremented) in each DMA cycle. Although this register is 16 bits long, the CPU is accessed by the MSM82C37A-5 eight bits at a time, therefore necessitating two successive 8-bit (lower and higher order bits) reading or writing operations using internal first/last flip-flops.

When autoinitialize has been set, the register is automatically initialized to the original value after TC.

CURRENT WORD COUNT REGISTER

Each channel is also equipped with a 16 bit-long current word count register where the transfer count is held during DMA transfers. The register value is decremented in each DMA cycle. When the word count value reaches FFFF(H) from OOOO(H), a TC is generated. Therefore, a word count vaue which is one less than the actual number of transfers must be set.

Since this register is also 16 bits long, it is accessed by first/last flip-flops control in the same way as the address register. And if autoinitialize has been set, the register is automatically initialized to the original value after TC.

BASE ADDRESS REGISTER AND BASE WORD COUNT REGISTER

Each channel is equipped with a 16-bit long base address register and base word count register where the initial value of each current register is held. The same values are written in each base register and the current register by the CPU. The contents of the current register can be made ready by the CPU, but the content of the base register cannot be read.

COMMAND REGISTER

This 8-bit write-only register prescribes DMA operations for all MSM82C37A-5 channels. An outline of all bits is given in Figure 3. When the controller is disabled by setting DB2, there is no HRQ output even if DMA request is active.

DREQ and DACK signals may be active high or active low by setting DB6 and DB7.

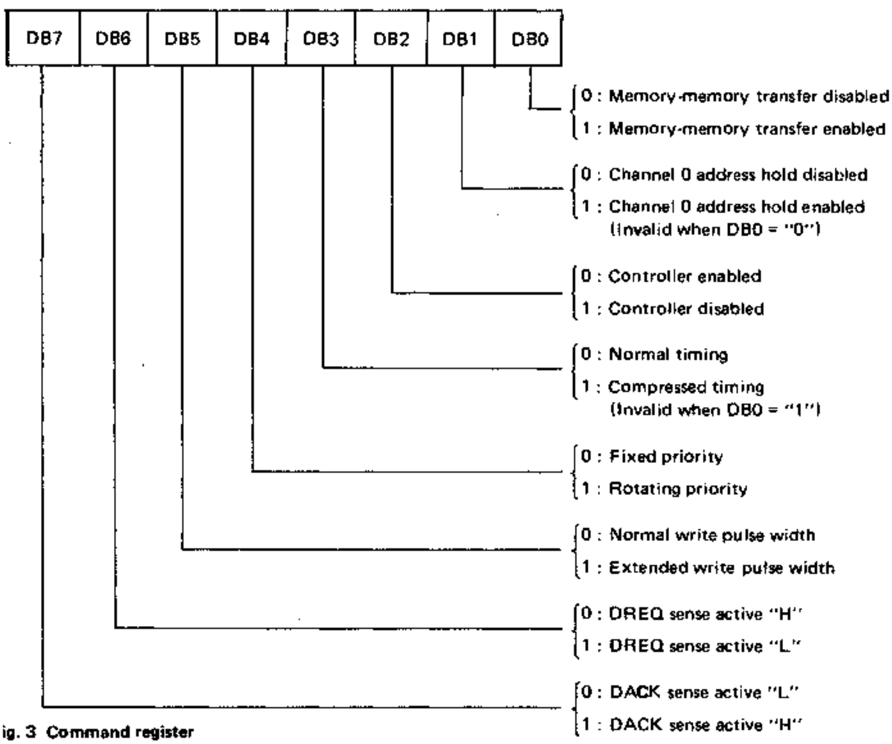


Fig. 3 Command register

MODE REGISTER

Each channel is equipped with a 6-bit write-only mode register, which is decided by setting DB0, DB1 which channel is to be written when writing from the CPU is programming status. The bit description is outlined in Figure 4.

This register is not cleared by Reset or Master Clear instruction.

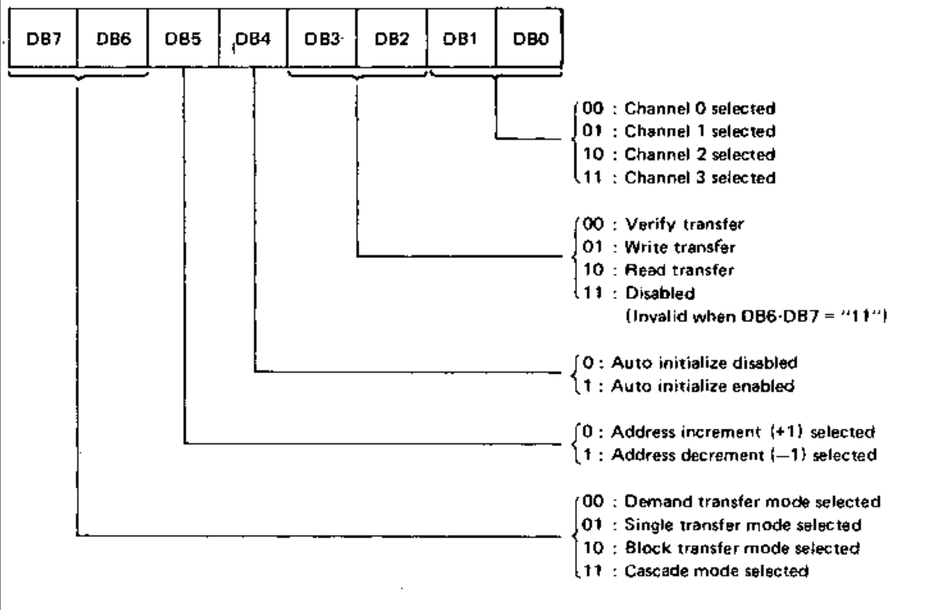


Fig. 4 Mode register

REQUEST REGISTER

In addition to using the DREQ signal, the MSM82C37A-5 can request DMA transfers by software means. This involves setting the request bit of request register. Each channel has a corresponding request bit in the request register, and the order of priority of these bits is determined by the priority decision circuit irrespective of the mask register. DMA transfers are acknowledged in accordance with the decided order of priority.

All request bits are reset when the TC is reached, and when the request bit of a certain channel has been received, all other request bits are cleared. When a memory-memory transfer is commenced, the channel 0 request bit is set. The bit description is outlined in Figure 5.

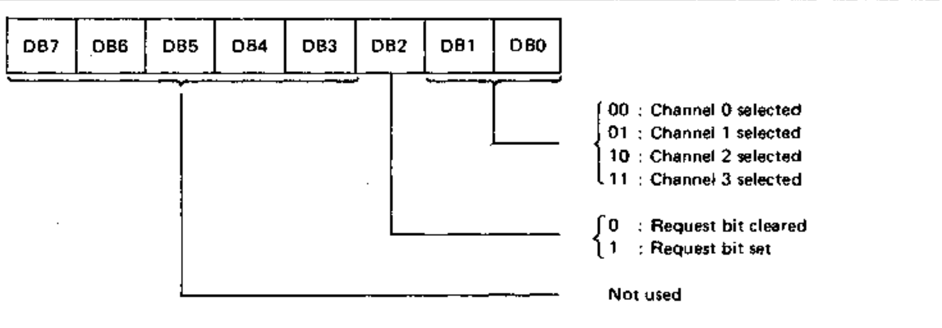
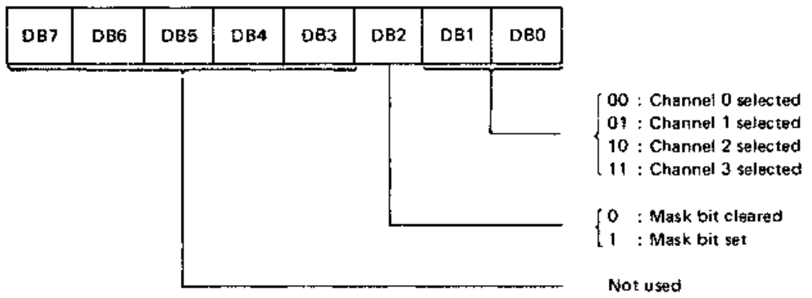


Fig. 5 Request register

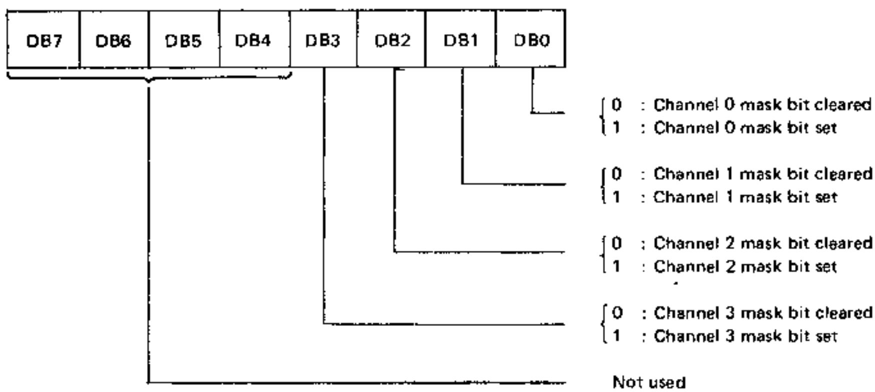
MASK REGISTER

This register is used in disabling and enabling of DMA transfers in each channel. Each channel includes a corresponding mask bit in the mask register, and each bit is set when the TC is reached if not in autoinitialize mode. This mask register can be set in two different ways.

The method for setting/resetting the register for each channel is outlined in Figure 6(a), while the method for setting/resetting the register for all channels at once is outlined in Figure 6(b).



(a) Single mask register (setting/resetting for each channel)



(b) All mask register (setting/resetting of all channels at once)

Fig. 6 Mask register

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STATUS REGISTER

This register is a read-only register used in CPU reading of the MSM82C37A-5 status. The four higher order bits indicate the DMA transfer request status for each channel, '1' being set when the DREQ input signal is active.

The four lower order bits indicate whether the corresponding channel has reached the TC or not, '1' being set when the TC status is reached. These four lower order bits are reset by status register reading, or RESET input and master clearing. A description of each bit is outlined in Figure 7.

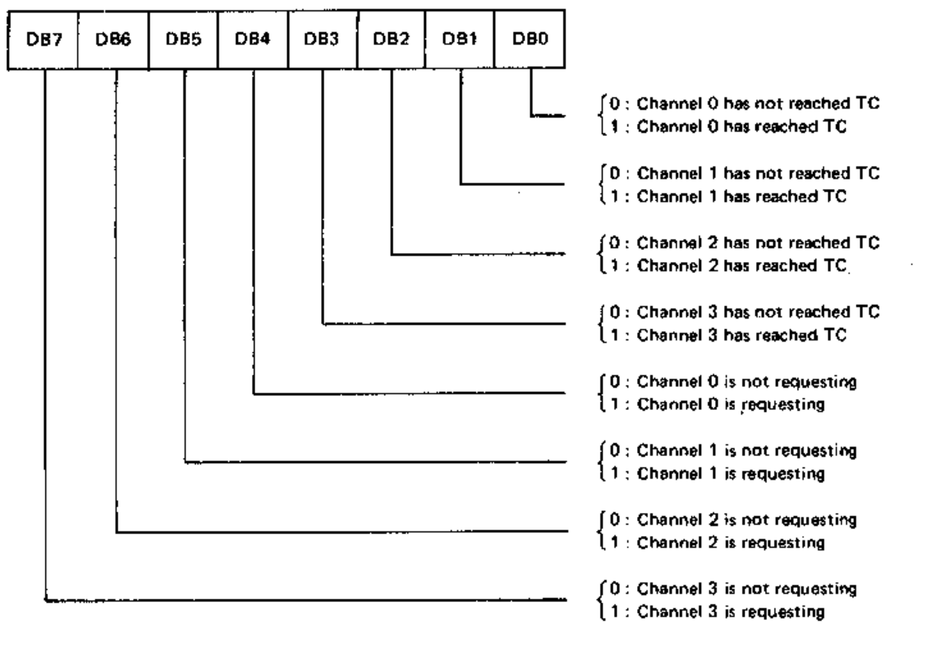

Fig. 7 Status register

TEMPORARY REGISTER

The temporary register is a register where transfer data is held temporarily during memory-memory transfers. Since the last item of data to be transferred is held after completion of the transfer, this item can be read by the CPU.

SOFTWARE COMMAND

The MSM82C37A-5 is equipped with software commands for executing special operations to ensure proper programming. Software command is irrespective of data bus contents.

CLEAR FIRST/LAST FLIP-FLOP

16-bit address and word count registers are read or written in two consecutive operations involving eight bits each (higher and lower order bits) under data bus port control. The fact that the lower order bits are accessed first by the MSM82C37A-5, followed by accessing of the higher order bits, is discerned by the internal first/last flip-flop. This command resets the first/last flip-flop with the eight lower order bits being accessed immediately after execution.

MASTER CLEAR

The same operation as when the hardware RESET input is applied. This command clears the contents of the command, status (for lower order bits), request, and temporary registers, also clears the first/last flip-flop, and sets the mask register. This command is followed by an idle cycle.

CLEAR MASK REGISTER

When this command is executed, the mask bits for all channels are cleared to enable reception of DMA transfers.

PROGRAMMING

The MSM82C37A-5 is switched to programming status when the HLDA input and $\overline{CS}$ are both at low level. In this state, $\overline{IOR}$ is changed to low level with $\overline{IOW}$ held at high level to enable reading by the CPU, or else $\overline{IOW}$ is changed to low level while $\overline{IOR}$ is held at high level to enable writing by the CPU.

A list of command codes for reading from the MSM82C37A-5 is given in Table 2, and a list of command codes for writing in the MSM82C37A-5 is given Table 3.

Note: If a DMA transfer request is received from an I/O device during MSM82C37A-5 programming, that DMA transfer may be commenced to prevent proper programming.
To prevent this interference, the DMA channel must be masked, or the controller disabled by the command register, or the system set so as to prevent DREQ becoming active during the programming.

Table 2 List of MSM82C37A-5 read commands

$\overline{CS}$	$\overline{IOR}$	A3	A2	A1	A0	Internal first/last flip/flop	Read out data		
0	0	0	0	0	0	0	Channel 0	Current address register	8 lower order bits
0	0	0	0	0	0	1			8 higher order bits
0	0	0	0	0	1	0		Current word count register	8 lower order bits
0	0	0	0	0	1	1			8 higher order bits
0	0	0	0	1	0	0	Channel 1	Current address register	8 lower order bits
0	0	0	0	1	0	1			8 higher order bits
0	0	0	0	1	1	0		Current word count register	8 lower order bits
0	0	0	0	1	1	1			8 higher order bits
0	0	0	1	0	0	0	Channel 2	Current address register	8 lower order bits
0	0	0	1	0	0	1			8 higher order bits
0	0	0	1	0	1	0		Current word count register	8 lower order bits
0	0	0	1	0	1	1			8 higher order bits
0	0	0	1	1	0	0	Channel 3	Current address register	8 lower order bits
0	0	0	1	1	0	1			8 higher order bits
0	0	0	1	1	1	0		Current word count register	8 lower order bits
0	0	0	1	1	1	1			8 higher order bits
0	0	1	0	0	0	X	Status register		
0	0	1	1	0	1	X	Temporary register		
0	0	Other combinations				X	Output data invalid		

Table 3 List of MSM82C37A-5 write commands

$\overline{CS}$	$\overline{IOW}$	A3	A2	A1	A0	Internal first/last flip-flop	Written data		
0	0	0	0	0	0	0	Channel 0	Current and base address registers	8 lower order bits
0	0	0	0	0	0	1			8 higher order bits
0	0	0	0	0	1	0		Current and base word count registers	8 lower order bits
0	0	0	0	0	1	1			8 higher order bits
0	0	0	0	1	0	0	Channel 1	Current and base address registers	8 lower order bits
0	0	0	0	1	0	1			8 higher order bits
0	0	0	0	1	1	0		Current and base word count registers	8 lower order bits
0	0	0	0	1	1	1			8 higher order bits
0	0	0	1	0	0	0	Channel 2	Current and base address registers	8 lower order bits
0	0	0	1	0	0	1			8 higher order bits
0	0	0	1	0	1	0		Current and base word count registers	8 lower order bits
0	0	0	1	0	1	1			8 higher order bits
0	0	0	1	1	0	0	Channel 3	Current and base address registers	8 lower order bits
0	0	0	1	1	0	1			8 higher order bits
0	0	0	1	1	1	0		Current and base word count registers	8 lower order bits
0	0	0	1	1	1	1			8 higher order bits
0	0	1	0	0	0	X	Command register		
0	0	1	0	0	1	X	Request register		
0	0	1	0	1	0	X	Single mask register		
0	0	1	0	1	1	X	Mode register		
0	0	1	1	0	0	X	Clear first/last flip-flop (software command)		
0	0	1	1	0	1	X	Master clear (software command)		
0	0	1	1	1	0	X	Clear mask register (software command)		
0	0	1	1	1	1	X	All mask register		

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OKI semiconductor

MSM82C43RS/GS

INPUT/OUTPUT PORT EXPANDER

GENERAL DESCRIPTION

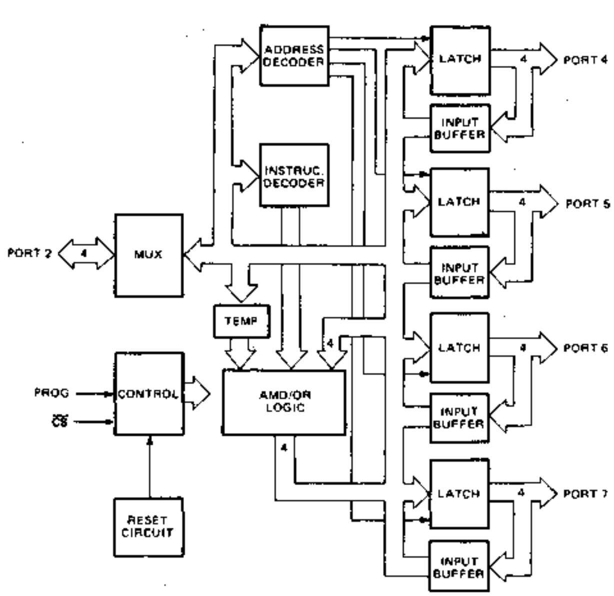
The MSM82C43 is an input/output port expander device based on 3μ silicon gate CMOS technology and designed to operate at low power consumption levels.

In systems employing the MSM80C48/49 8-bit 1-chip microcomputers, 4-bit data can be expanded by dividing between four I/O lines by executing the MOVDPp. A, MOVDA, Pp, ANLDPp, A and ORLDPp, A instrutbtions.

FEATURES

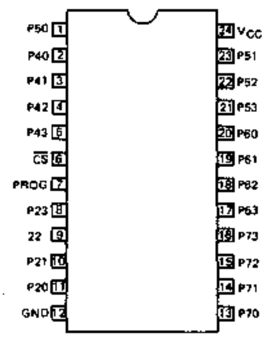
- 3μ silicon gate CMOS technology for low power consumption
- 2.5 to 6 V single power supply (dependent on MSM80C 48/49 operating frequency.)
- Fully static operation
- Bidirectional I/O ports
- TTL compatible (ports 4 thru 7)
- 24-pin DIP (MSM82C43RS)
- 24-pin flat package (MSM82C43GS)
- Functional compatibility with Intel i8243

FUNCTIONAL BLOCK DIAGRAM

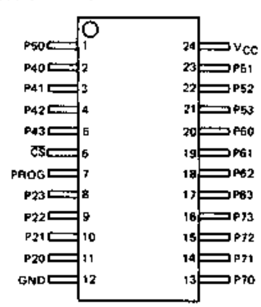


PIN CONFIGURATION

MSM82C43RS (Top View) 24 Lead Plastic DIP



MSM82C43GS (Top View) 24 Lead Plastic Flat Package



ELECTRIC CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	Ta = 25°C	–0.5 ~ 7	V
Input Voltage	V_I	Ta = 25°C	–0.3 ~ V_{CC}	V
Storage Temperature	Tstg	–	–65 ~ +150	°C

• Operating Conditions

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	–	2.5 ~ 6*1	V
Ambient Temperature	T_A	–	–40 ~ +85	°C
Fan-out	N	MOS load	10	–
		TTL load	3*2	–

• DC Characteristics (V_{CC} = 4.0V ~ 6.0V, Ta = –40°C ~ +85°C)

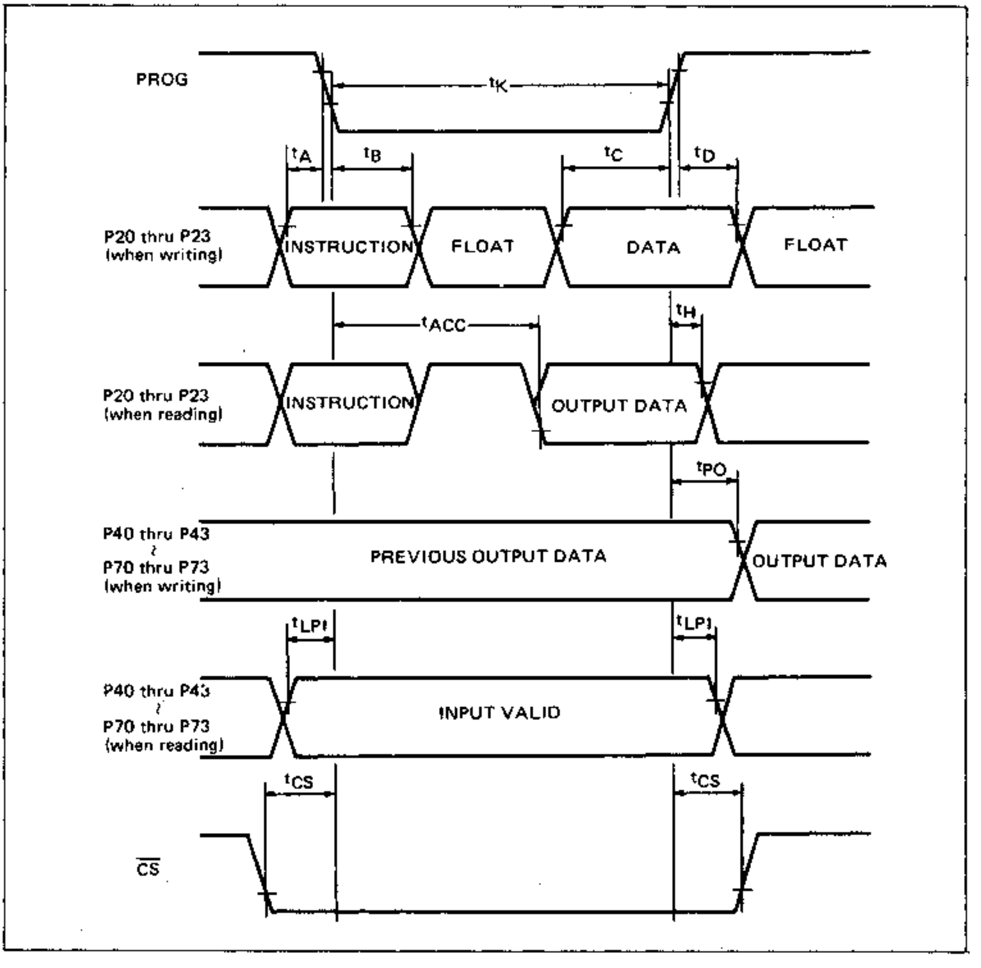
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
"L" Input Voltage	V_{IL}		–0.5	–	0.13Vcc	V
"H" Input Voltage	V_{IH}		0.4Vcc	–	V_{CC}	V
"L" Output Voltage Ports 4-7	V_{OL1}	I_{OL} = 5mA	–	–	0.45	V
"L" Output Voltage Port 7	V_{OL2}	I_{OL} = 20mA	–	–	1	V
"L" Output Voltage Port 2	V_{OL3}	I_{OL} = 0.9mA	–	–	0.45	V
"L" Total Output Current from Ports 4-7*3	I_{OL}	5mA/1PIN	–	–	80	mA
"H" Output Voltage Ports 4-7	V_{OH1}	I_{OH} = –240μA	0.75V_{CC}	–	–	V
"H" Output Voltage Port 2	V_{OH2}	I_{OH} = –100μA	0.75V_{CC}	–	–	V
"H" Output Voltage Ports 4-7	V_{OH1}	I_{OH} = –40μA	0.93V_{CC}	–	–	V
"H" Output Voltage Port 2	V_{OH2}	I_{OH} = –20μA	0.93V_{CC}	–	–	V
Input Leak Current*3	I_{IL1}	$0 \leqq V_{IN} \leqq V_{CC}$	–10	–	20	μA
Input Leak Current*6	I_{IL2}	$0 \leqq V_{IN} \leqq V_{CC}$	–10	–	10	μA
Power Supply Current	I_{CC}	Standby stop No accessing	–	5	100	μA
		For continuous MSM80C49 accessing at 11 MHz	–	1	2	mA

NOTE: *1 The supply voltage during operation is dependent on MSM80C49 operating frequency.
*2 Except P20 thru P23.
*3 P40 thru P43, P50 thru P53, P60 thru P63, P70 thru P73.
*4 P70 thru P73.
*5 P20 thru P23.
*6 P20 thru P23, CS, PROG.

• **AC Characteristics** (V_{CC} = 4.0V ~ 6.0V, Ta = −40°C ~ +85°C)

Parameter	Symbol	Conditions	MIN	MAX	Unit
Port Control Setting Time (up to PROG Falling Edge)	t_A	80pF LOAD	50	–	ns
Port Control Holding Time (From PROG Falling Edge)	t_B	20pF LOAD	60	–	ns
Output Data Setting Time	t_C	80pF LOAD	200	–	ns
Output Data Holding Time	t_D	20pF LOAD	20	–	ns
Input Data Holding Time	t_H	20pF LOAD	0	150	ns
PROG Pulse Width	t_K	–	700	–	ns
$\overline{CS}$ Valid Time (before and after PROG)	t_{CS}	–	50	–	ns
Output Data Valid Time (at Ports 4–7)	t_{PO}	100pF LOAD	–	700	ns
Input Data Holding Time (at Ports 4–7)	t_{LP1}	–	100	–	ns
Input Data Valid Time (from PROG Falling Edge)	t_{ACC}	80pF LOAD	–	650	ns

TIMING CHART



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PIN FUNCTIONS

Pin	Function
PROG	Clock input from MSM80C49. When PROG is changed from "H" to "L", MSM82C43 STARTS operating in accordance with an order from MSM80C49.
$\overline{CS}$	Input for chip select. Outputs and internal status cannot be changed when $\overline{CS}$ is "H".
P20 – P23	4-bit bidirectional I/O ports. When connected to P20 thru P23 of MSM80C49, direct data transfer from port to accumulator and from accumulator to port is possible.
P40 – P43 P50 – P53 P60 – P63 P70 – P73	4-bit bidirectional I/O ports. Data is latched statistically when output to ports, but is only valid while PROG is at "L" level when input.
V_{CC}	+5V power supply
GND	GROUND

FUNCTIONS

• **Write mode**

Execution of MOVDPp, A, ORLDPp, A, ANLDPp, and A by MSM80C49 enables direct output of accumulator contents to ports 4 thru 7, and output to the ports after ORing or ANDing with port data. The port data is latched statistically at this time and remains unchanged until execution of the next instruction.

• **Read mode**

Execution of MOVDA and Pp results in data of ports 4 thru 7 being accepted by the accumulator. Note that port data is valid only while PROG is at "L" level. When at "H" level, ports 4 thru 7 are switched to tristate and port 2 is switched to input mode.

• **Address and instruction code**

Instruction	P23	P22	Port	P21	P20
Read	0	0	Port 4	0	0
Write	0	1	Port 5	0	1
OR	1	0	Port 6	1	0
AND	1	1	Port 7	1	1

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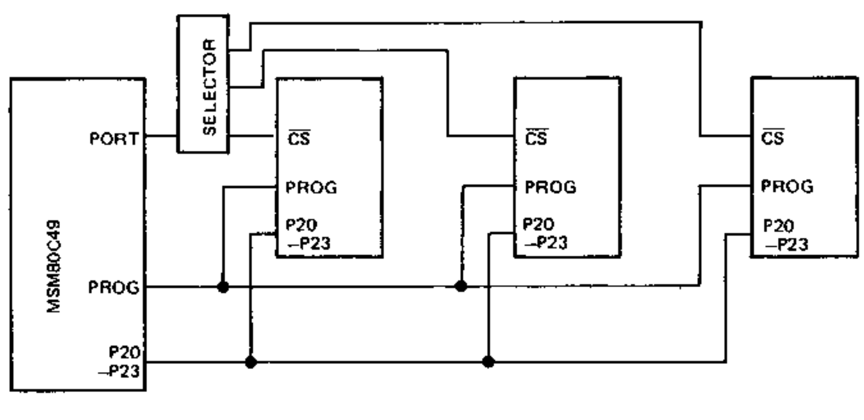
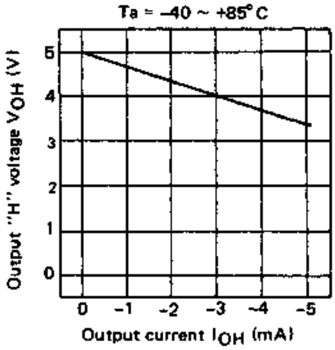
• **MSM82C43 Multiple connection example**



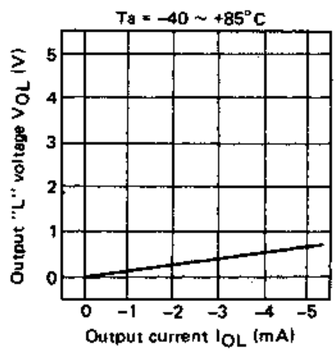
OUTPUT CHARACTERISTICS

• **Standard DC characteristics**

Output "H" voltage (V_{OH}) vs. output current (I_{OH})

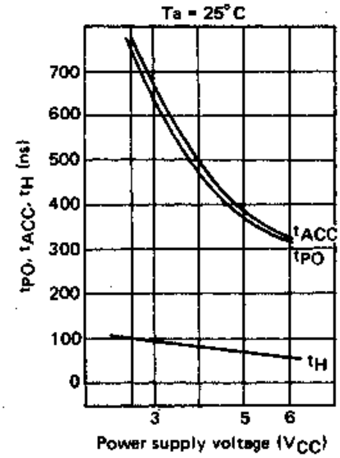


Output "L" voltage (V_{OL}) vs. output current (I_{OL})

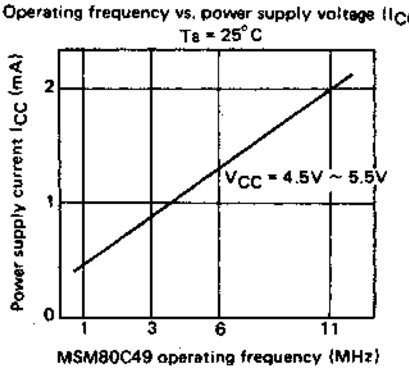


• **Standard AC characteristics**

t_{PO}, t_H, and t_{ACC} vs. power supply voltage (V_{CC})

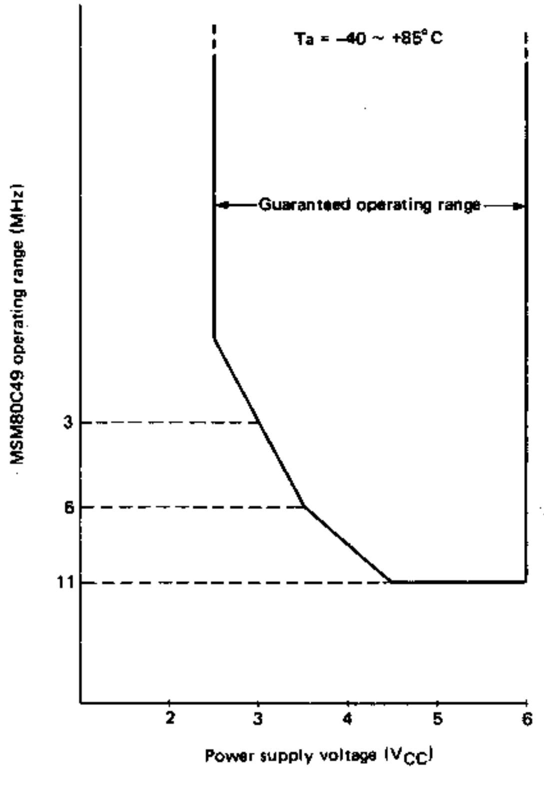


Operating frequency vs. power supply voltage (I_{CC})



Note: The direction which the output current flows through the device is taken as the positive direction.

GUARANTEED MSM82C43 OPERATING RANGE



OKI semiconductor

MSM82C51ARS/GS

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

GENERAL DESCRIPTION

The MSM82C51A is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.

As a peripheral device of a microcomputer system the MSM82C51A receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

The MSM82C51A configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on extremely low power at 100 μA (max) of standby current by suspending all operations.

FEATURES

- Wide power supply voltage range from 3 V to 6 V.
- Wide temperature range from −40° C to 85° C.
- Synchronous communication upto 64K baud.
- Asynchronous communication upto 38.4K baud.
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin DIP (MSM82C51ARS)
- 32-pin flat package (MSM82C51AGS)

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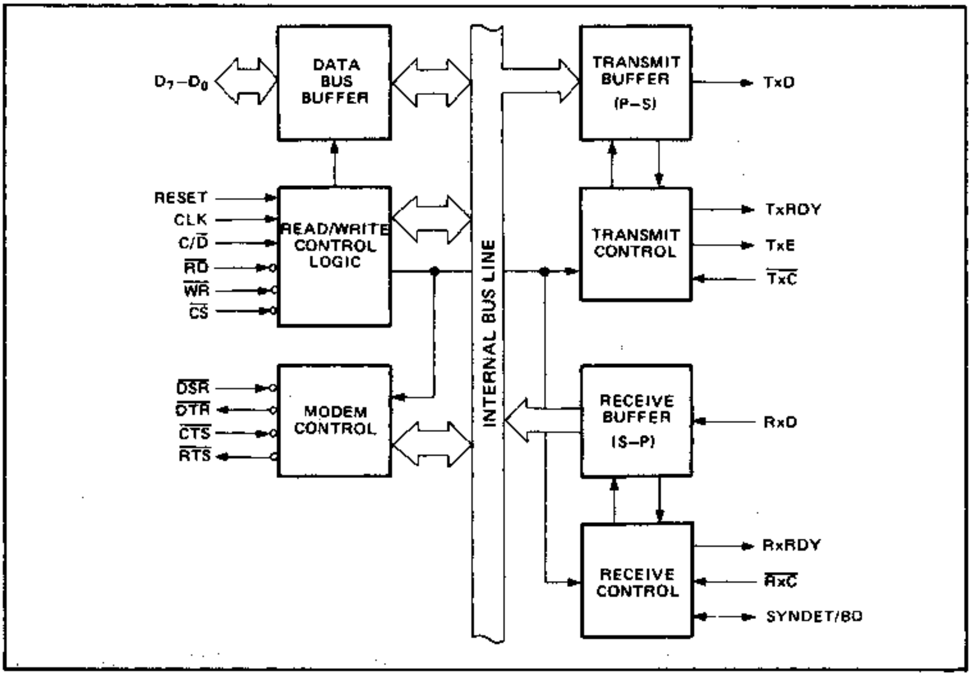
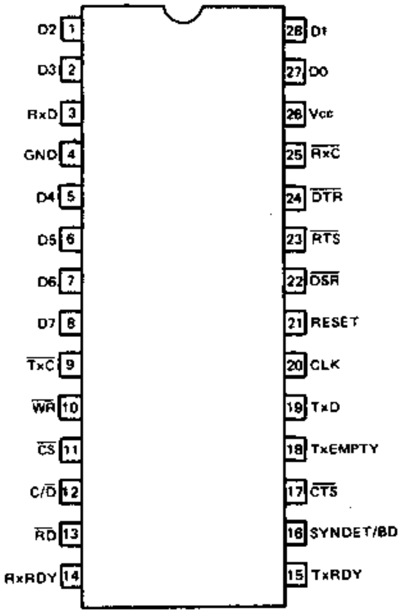
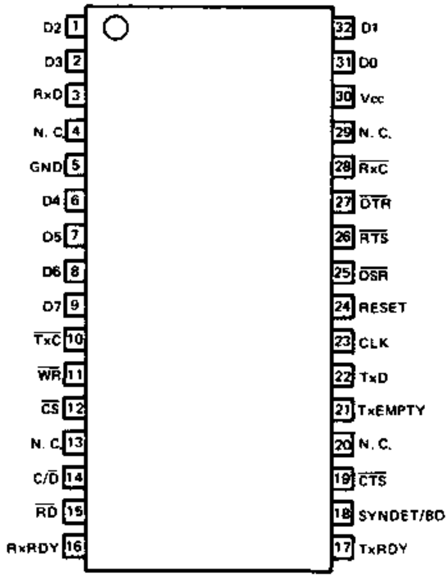
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



MSM82C51ARS (Top View)
28 Lead Plastic DIP



MSM82C51AGS (Top View)
32 Lead Plastic Flat Package

FUNCTION

Outline

The MSM82C51A's functional configuration is programed by software.

Operation between the MSM82C51A and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

Table 1 Operation between MSM82C51A and CPU

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	X	X	X	Data bus 3-state
0	X	1	1	Data bus 3-state
0	1	0	1	Status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting the MSM82C51A. Fig. 1 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

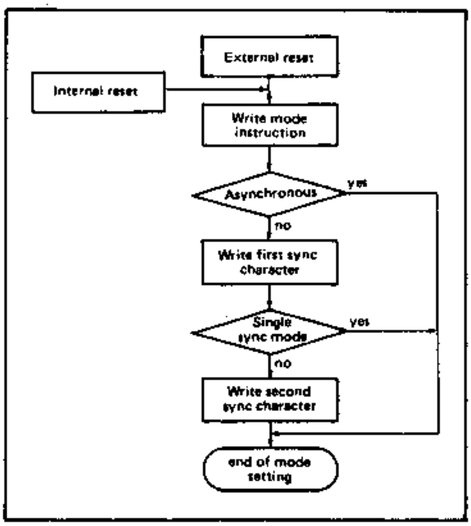


Fig. 1 Function-Setting Sequence (Mode Instruction Sequence)

Control Words

There are two types of control word.

1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the MSM82C51A. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- No. of synchronous characters (synchronous mode)

The bit configuration of mode instruction is shown in Fig.'s 2 and 3. In the case of synchronous mode, it is necessary to write one- or two-byte sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

Baud rate factor

0	1	0	1
0	0	1	1
Refer to Fig. 3 SYNC	1x	16x	64x

Character length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity check

0	1	0	1
0	0	1	1
Disable	Odd parity	Disable	Even parity

Stop bit length

0	1	0	1
0	0	1	1
Inhibit	1 bit	1.5 bits	2 bits

Fig. 2 Bit Configuration of Mode Instruction (Asynchrnous)

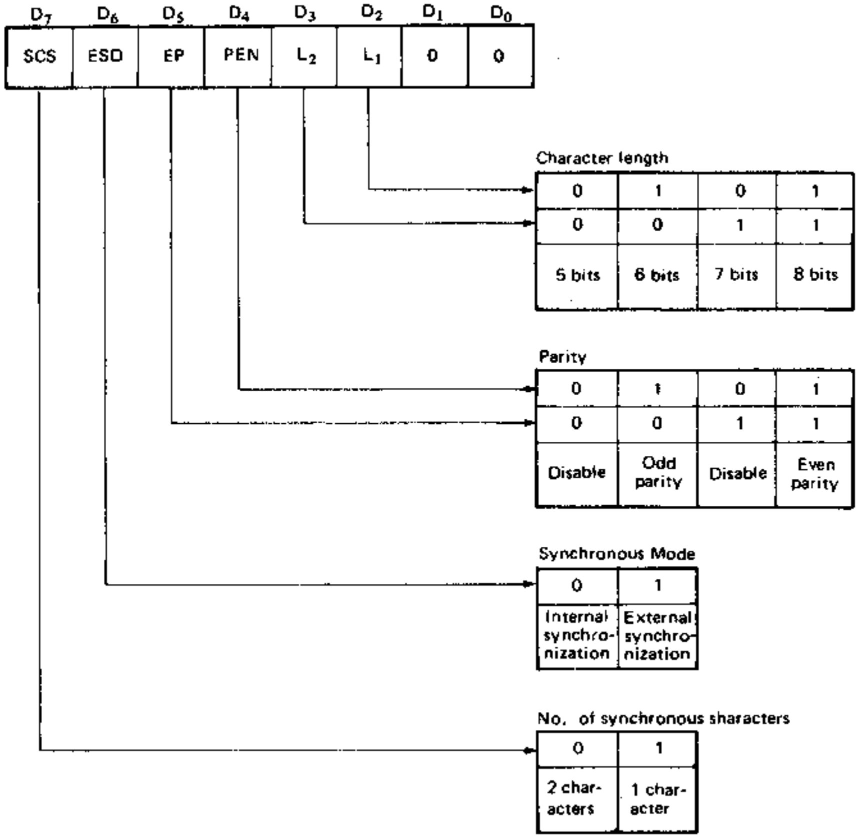


Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

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2) **Command**

Command is used for setting the operation of the MSM82C51A.

It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data.
- Resetting of error flag.
- Sending of break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.

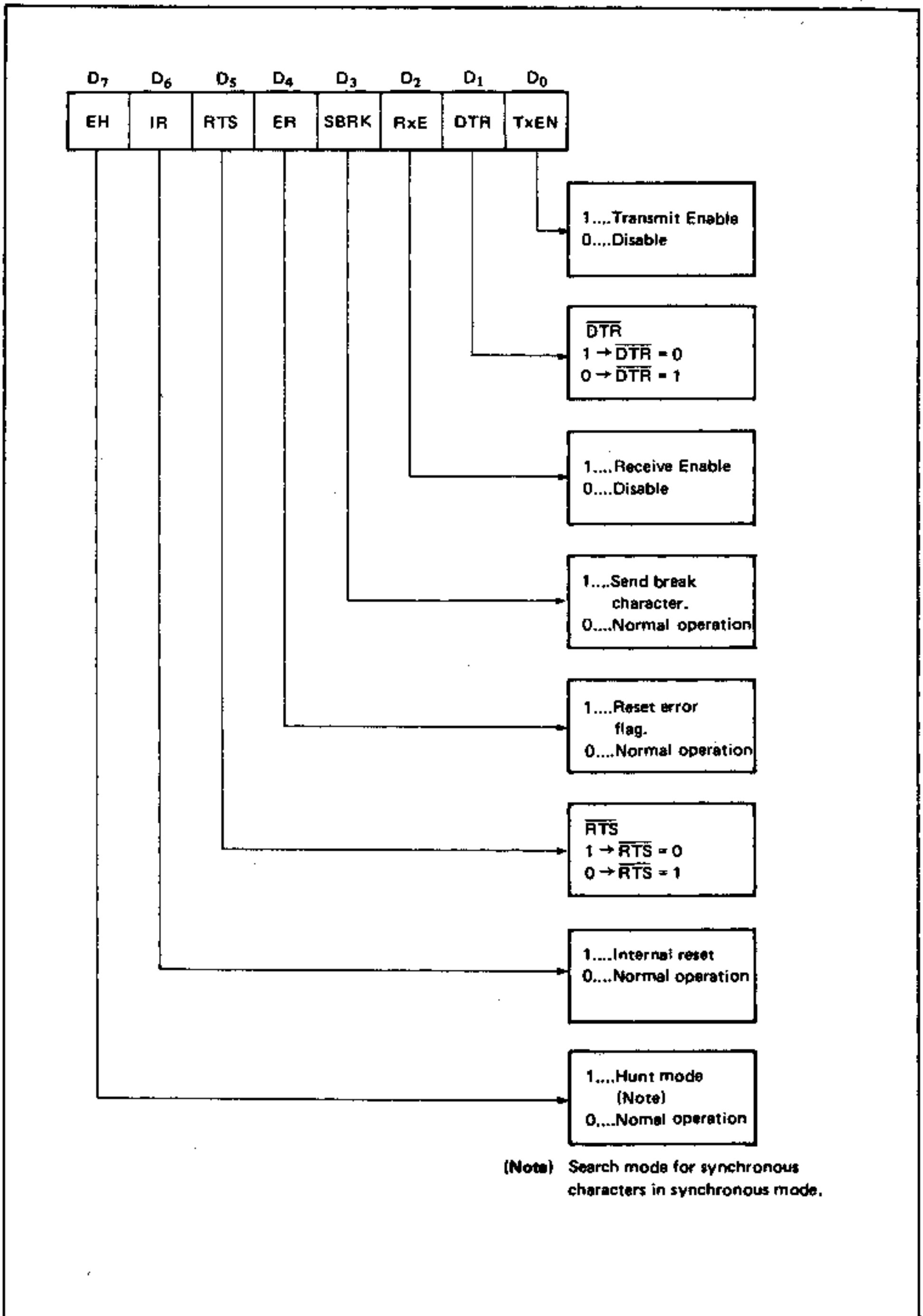

Fig. 4 Bit Configuration of Command

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Status Word

It is possible to see the internal status of MSM-82C51A by reading a status word.

The bit configuration of status word is shown in Fig. 5.

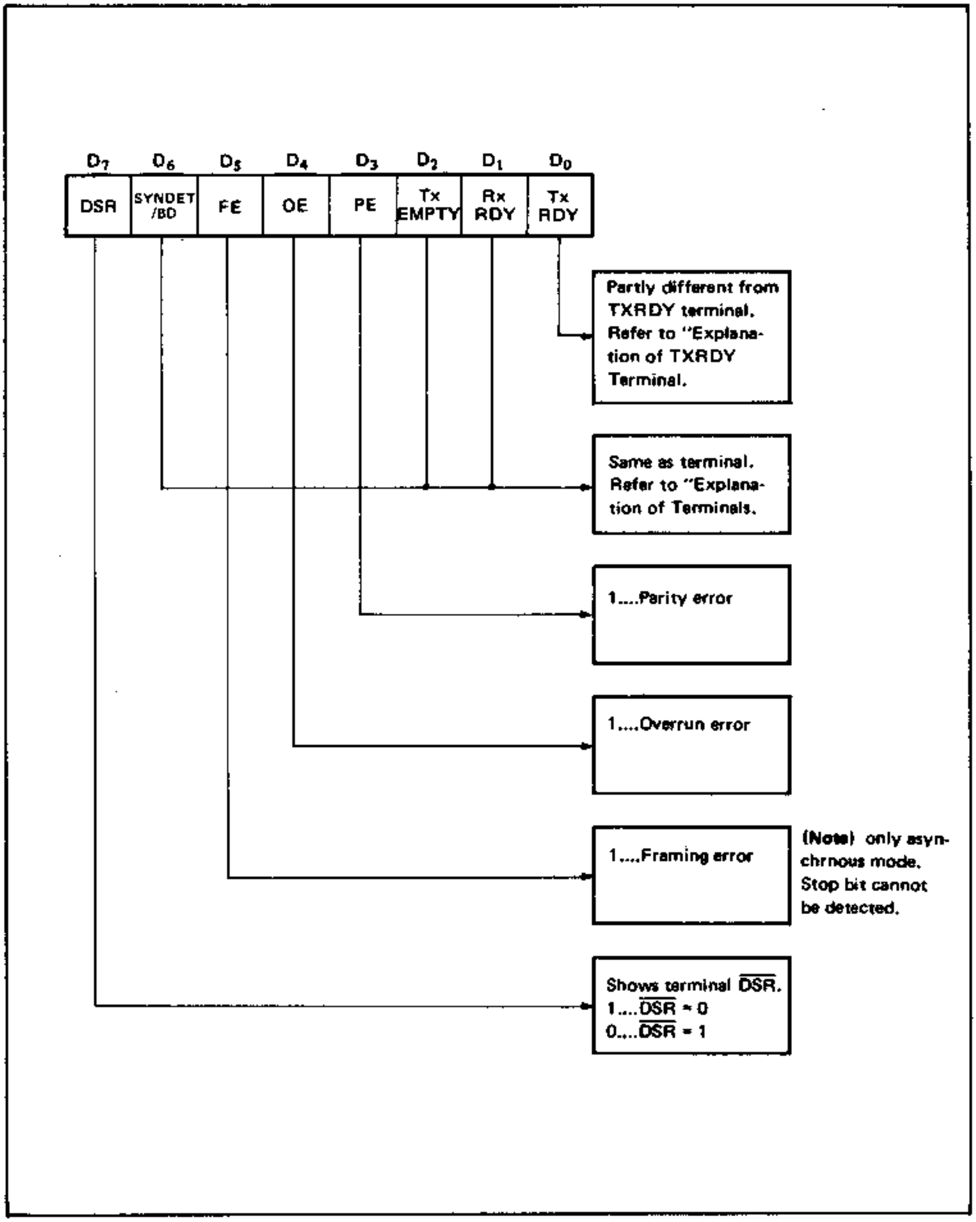

Fig. 5 Bit Configuration of Status Word

Standby Status

It is possible to put the MSM82C51A in "standby status".

When the following conditions have been satisfied the MSM82C51A is in "standby status."

(1) $\overline{CS}$ terminal is fixed at Vcc level.

(2) Input pins other than $\overline{CS}$, D_0 to D_7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are fixed at Vcc or GND level (including SYNDET in external synchronous mode).

Note When all output currents are 0, ICCS specification is applied.

Pin Descriptions

D_0 to D_7 (I/O terminal)

This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the MSM82C51A into "reset status."

The device waits for the writing of "mode instruction."

The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing.

CLK signal is independent of $\overline{RXC}$ or $\overline{TXC}$.

However, the frequency of CLK must be greater than 30 times the $\overline{RXC}$ and $\overline{TXC}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{WR}$ (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the MSM82C51A.

$\overline{RD}$ (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the MSM82C51A.

C/$\overline{D}$ (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the MSM82C51A is accessed by the CPU.

If C/$\overline{D}$ = low, data will be accessed.

If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input terminal)

This is the "active low" input terminal which selects the MSM82C51A at low level when the CPU accesses.

Note The device won't be in "standby status"; only setting $\overline{CS}$ = High.
Refer to "Explanation of Standby Status."

TXD (Output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out.

The device is in "mark status" (high level) after resetting or during a status when transmit is disabled.

It is also possible to set the device in "break status" (low level) by a command.

TXRDY (Output terminal)

This is an output terminal which indicates that the MSM82C51A is ready to accept a transmitted data character. But the terminal is always at low level if $\overline{CTS}$ high or the device was set in "TX disable status" by a command.

Note TXRDY status word indicates that transmit data character is receivable, regardless of $\overline{CTS}$ or command.

If the CPU writes a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the MSM82C51A has transmitted all the characters and had no data character.

In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted.

If the CPU writes a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

Note As the transmitter is disabled by setting $\overline{CTS}$ "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High".
Even if a data is written after disable, that data is not sent out and TXE will be "High". After the transmitter is enabled, it sent out.
(Refer to Timing Chart of Transmitter Control and Flag Timing)

$\overline{TXC}$ (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data.

In "synchronous mode," the baud rate will be the same as the frequency of $\overline{TXC}$.

In "asynchronous mode", it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16 or 1/64 the $\overline{TXC}$.

The falling edge of $\overline{TXC}$ sifts the serial data out of the MSM82C51A.

RXD (Input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the MSM82C51A contains a character that is ready to READ.

If the CPU reads a data character, RXRDY will be reset by the leading edge of $\overline{RD}$ signal.

Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

$\overline{RXC}$ (Input terminal)

This is a clock input signal which determines the transfer speed of received data.

In "synchronous mode," the baud rate is the same as the frequency of $\overline{RXC}$.

In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16, 1/64 the $\overline{RXC}$.

SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode.

In "internal synchronous mode," this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset.

In "external synchronous mode," this is an input terminal.

A "High" on this input forces the MSM82C51A to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level" output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

$\overline{DSR}$ (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

$\overline{DTR}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of $\overline{DTR}$ by a command.

$\overline{CTS}$ (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

$\overline{RTS}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of $\overline{RTS}$ by a command.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits		Unit	Conditions
		MSM82C51ARS	MSM82C51AGS		
Power supply voltage	V_{CC}	−0.5 ~ +7		V	With respect to GND
Input voltage	V_{IN}	−0.5 ~ V_{CC} + 0.5		V	
Output voltage	V_{OUT}	−0.5 ~ V_{CC} + 0.5		V	
Storage temperature	T_{stg}	−55 ~ 150		°C	—
Power dissipation	P_D	0.9	0.7	W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	T_{OP}	−40	+25	+85	°C
"L" input voltage	V_{IL}	−0.3		+0.8	V
"H" input voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

(Vcc = 4.5 ~ 5.5V Ta = −40°C ~ +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
"L" output voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
"H" output voltage	V_{OH}	3.7			V	I_{OH} = −400 μA
Input leak current	I_{LI}	−10		10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output leak current	I_{LO}	−10		10	μA	$0 \leq V_{OUT} \leq V_{CC}$
Operating supply current	I_{CCO}			5	mA	Asynchronous X64 during transmitting/receiving
Standby supply current	I_{CCS}			100	μA	All input voltage shall be fixed at V_{CC} or GND level.

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AC CHARACTERISTICS

(Vcc = 4.5 ~ 5.5V, Ta = −40 ~ 85°C)

CPU Bus Interface Part

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address stable before $\overline{RD}$	t_{AR}	20		NS	Note 2
Address hold time for $\overline{RD}$	t_{RA}	20		NS	Note 2
$\overline{RD}$ pulse width	t_{RR}	250		NS	
Data delay from $\overline{RD}$	t_{RD}		200	NS	
$\overline{RD}$ to data float	t_{DF}	10	100	NS	
Recovery time between $\overline{RD}$	t_{RVR}	6		T_{cy}	Note 5
Address stable before $\overline{WR}$	t_{AW}	20		NS	Note 2
Address hold time for $\overline{WR}$	t_{WA}	20		NS	Note 2
$\overline{WR}$ pulse width	t_{WW}	250		NS	
Data set-up time for $\overline{WR}$	t_{DW}	150		NS	
Data hold time for $\overline{WR}$	t_{WD}	20		NS	
Recovery time between $\overline{WR}$	t_{RVW}	6		T_{cy}	Note 4
RESET pulse width	t_{RESW}	6		T_{cy}	

Serial Interface Part

Parameter		Symbol	Min.	Max.	Unit	Remarks
Main clock period		t_{cy}	250		NS	Note 3
Clock low time		$t_{\overline{\phi}}$	90		NS	
Clock high time		t_{ϕ}	120	$t_{cy}-90$	NS	
Clock rise/fall time		t_R, t_F		20	NS	
TXD delay from falling edge of $\overline{TXC}$		t_{DTX}		1	μS	
Transmitter clock frequency	1X Baud	f_{TX}	DC	64	kHz	Note 3
	16X, Baud	f_{TX}	DC	615	kHz	
	64X, Baud	f_{TX}	DC	615	kHz	
Transmitter clock low time	1X Baud	t_{TPW}	13		T_{cy}	
	16X, 64X Baud	t_{TPW}	2		T_{cy}	
Transmitter clock high time	1X Baud	t_{TPD}	15		T_{cy}	
	16X, 64X Baud	t_{TPD}	3		T_{cy}	
Receiver clock frequency	1X Baud	f_{RX}	DC	64	kHz	Note 3
	16X Baud	f_{RX}	DC	615	kHz	
	64X Baud	f_{RX}	DC	615	kHz	
Receiver clock low time	1X Baud	t_{RPW}	13		T_{cy}	
	16X, 64X Baud	t_{RPW}	2		T_{cy}	
Receiver clock high time	1X Baud	t_{RPD}	15		T_{cy}	
	16X, 64X Baud	t_{RPD}	3		T_{cy}	
Time from the center of last bit to the rise of TXRDY		t_{TXRDY}		8	T_{cy}	
Time from the leading edge of $\overline{WR}$ to the fall of TXRDY		$t_{TXRDY\ CLEAR}$		400	NS	
Time from the center of last bit to the rise of RXRDY		t_{RXRDY}		26	T_{cy}	

5

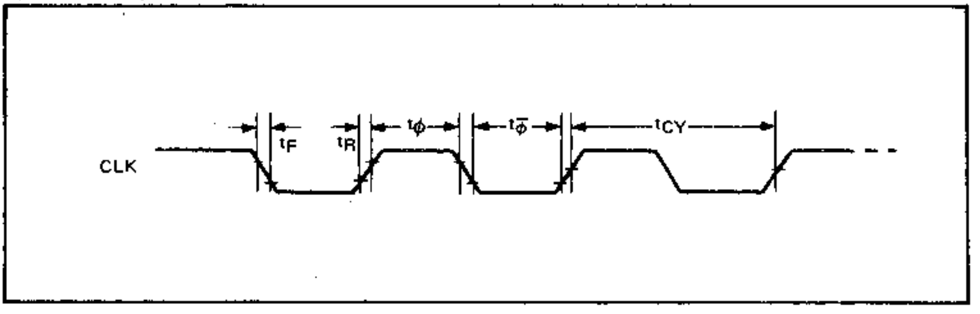
Parameter	Symbol	Min.	Max.	Unit	Remarks
Time from the leading edge of $\overline{RD}$ to the fall of RXRDY	$t_{RXRDY\ CLEAR}$		400	NS	
Internal SYNDET delay time from rising edge of $\overline{RXC}$	t_{IS}		26	T_{cy}	
SYNDET setup time for $\overline{RXC}$	t_{ES}	18		T_{cy}	
TXE delay time from the center of last bit	$t_{TXEMPTY}$	20		T_{cy}	
MODEM control signal delay time from rising edge of $\overline{WR}$	t_{WC}	8		T_{cy}	
MODEM control signal setup time for falling edge of $\overline{RD}$	t_{CR}	20		T_{cy}	
RXD setup time for rising edge of $\overline{RXC}$ (1X Baud)	t_{RXDS}	11		T_{cy}	
RXD hold time for falling edge of $\overline{RXC}$ (1X Baud)	t_{RXDH}	17		T_{cy}	

Caution 1) AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.
2) Addresses are $\overline{CS}$ and C/$\overline{D}$.
3) f_{TX} or $f_{RX} \leq 1/(30\ Tcy)$ 1 x baud
f_{TX} or $f_{RX} \leq 1/(5\ Tcy)$ 16 x, 64 x Baud
4) This recovery time is mode initialization only. Recovery time between command writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 18 t_{CY}.
Write Data is allowed only when TXRDY = 1.
5) This recovery time is Status read only.
Read Data is allowed only when RXRDY = 1.
6) Status update can have a maximum delay of 28 clock periods from event affecting the status.

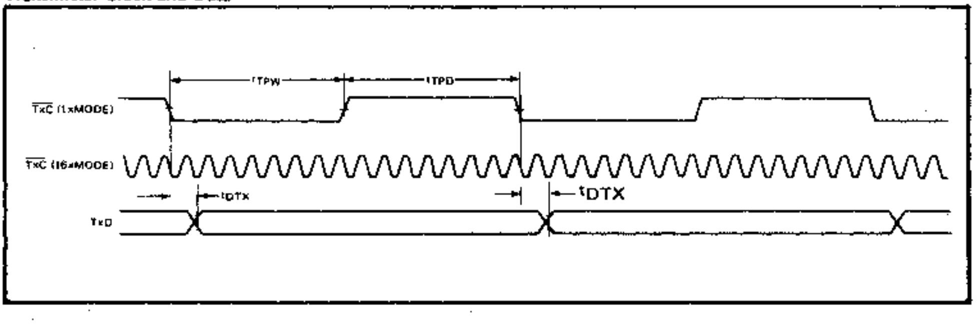
TIMING CHART

5

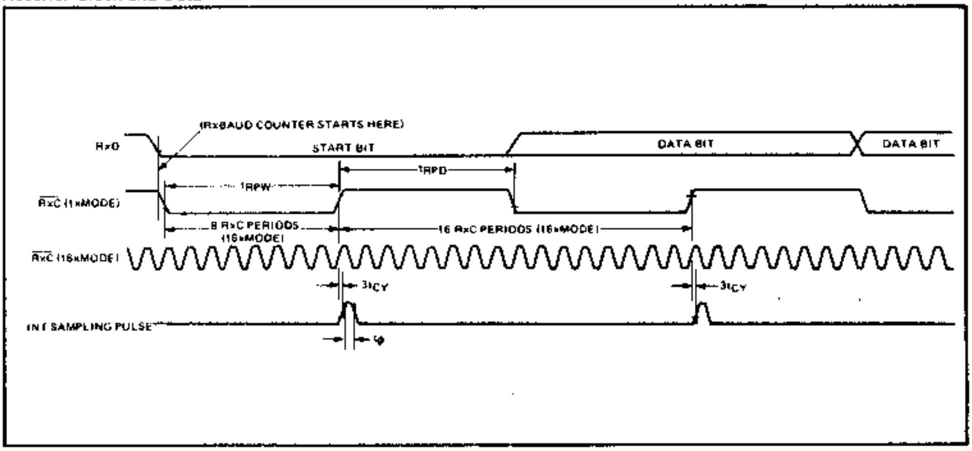
System Clock Input



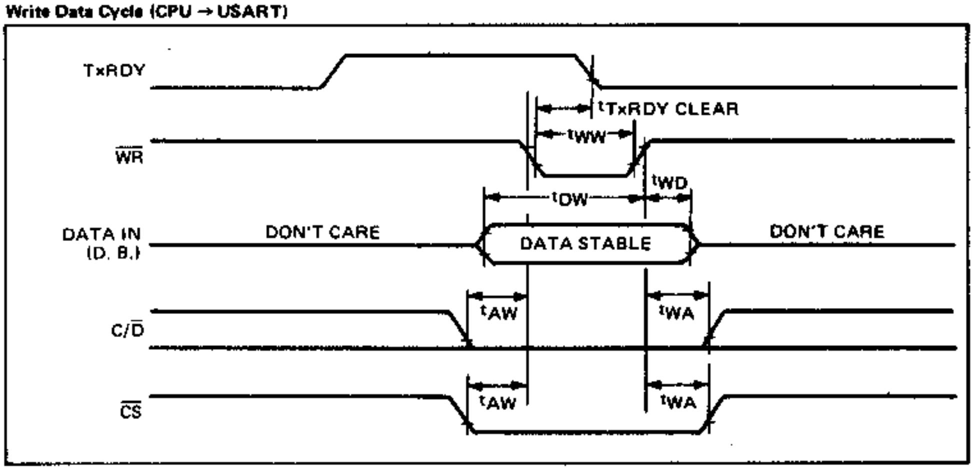
Transmitter Clock and Data



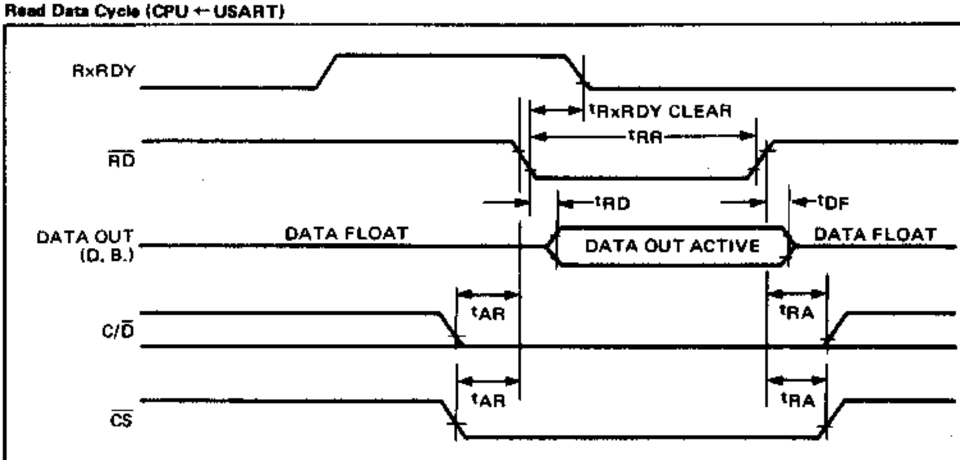
Receiver Clock and Data



Write Data Cycle (CPU → USART)

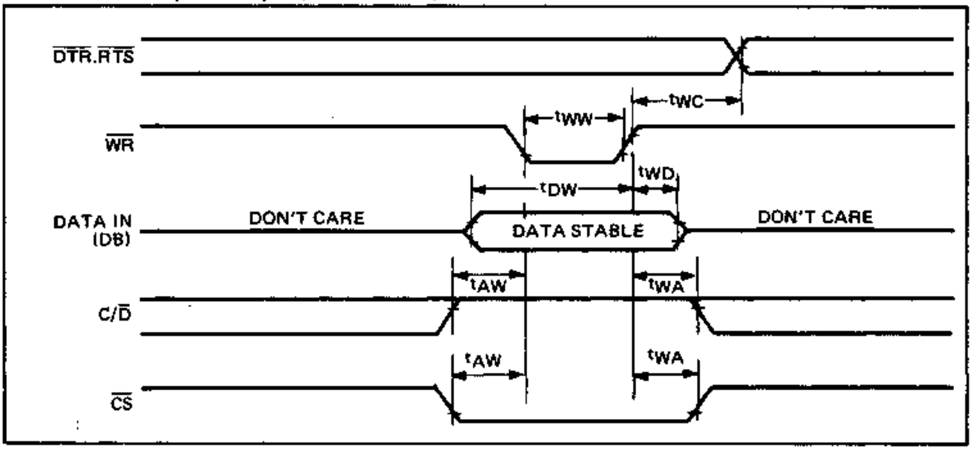


Read Data Cycle (CPU ← USART)

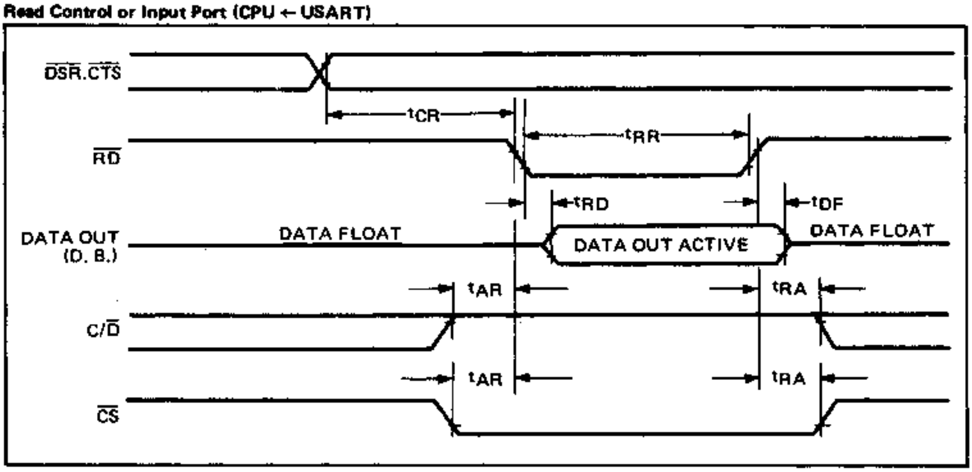


5

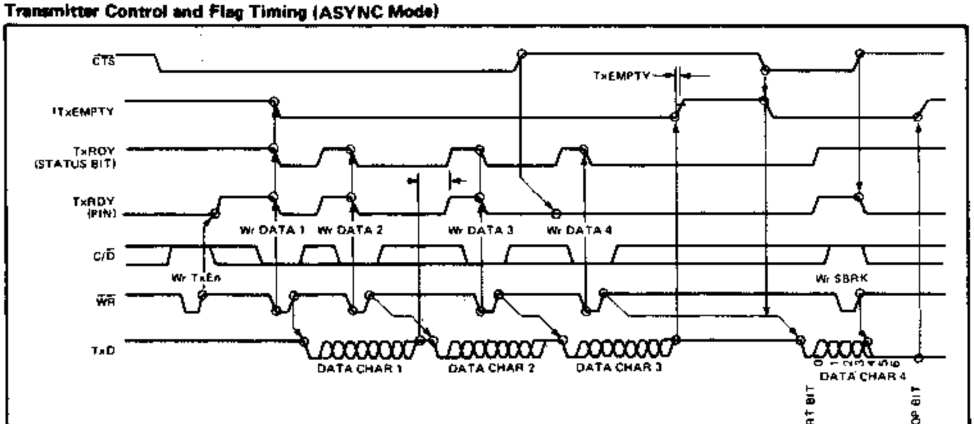
Write Control or Output Port Cycle (CPU → USART)



Read Control or Input Port (CPU ← USART)

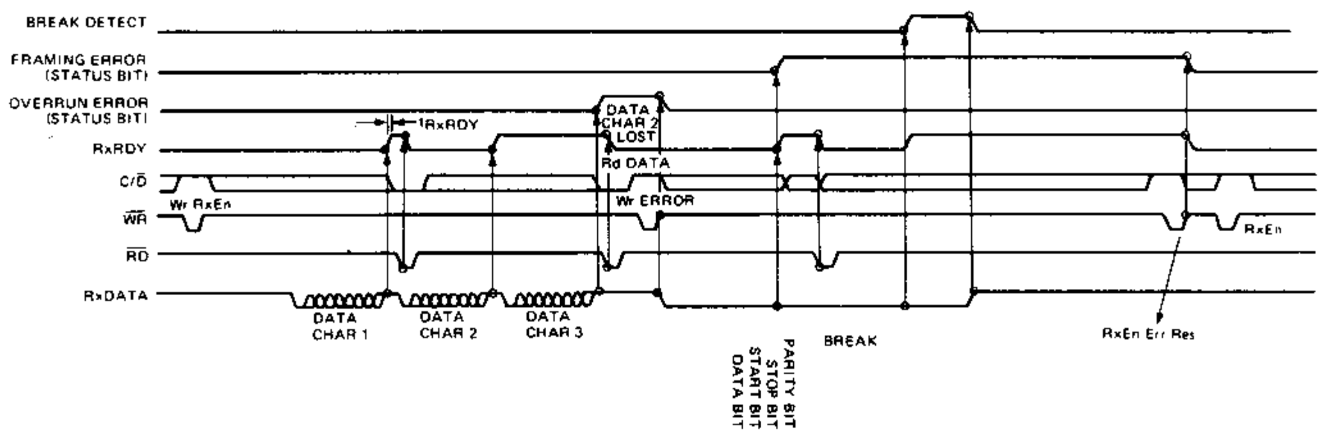


Transmitter Control and Flag Timing (ASYNC Mode)



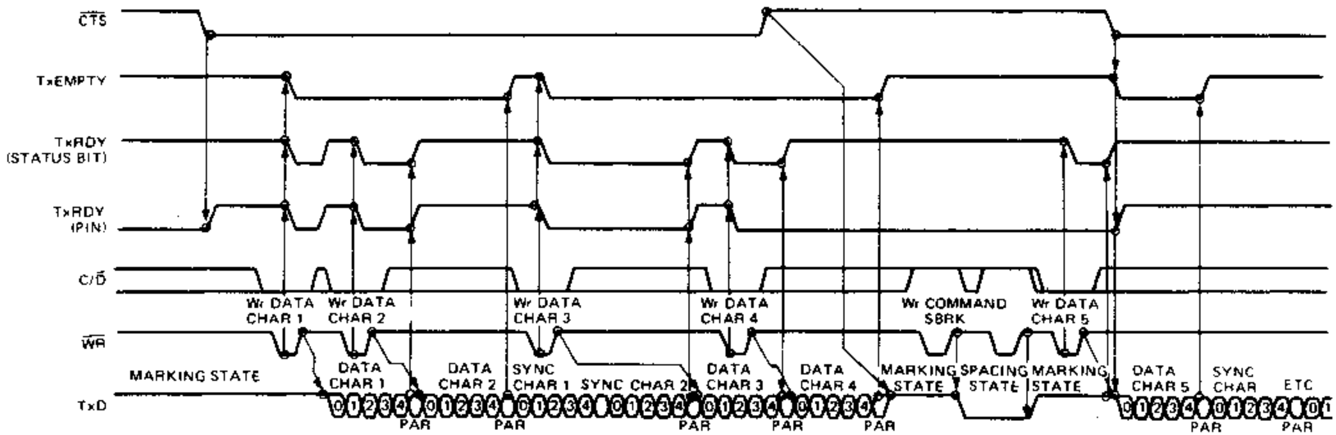
(Note) The wave-form chart is based on the case of 7 bit data length + parity bit + 2 stop bit.

Receiver Control and Flag Timing (ASYNC Mode)



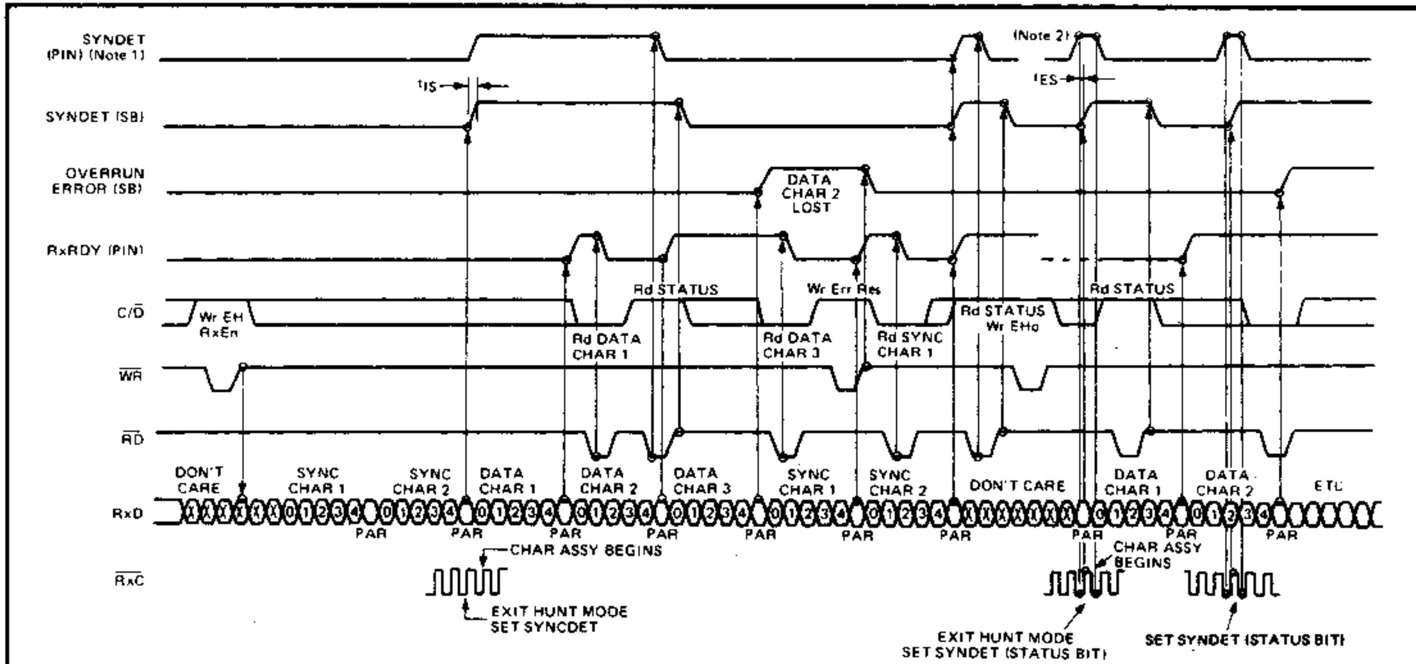
(Note) The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.

Transmitter Control and Flag Timing (SYNC Mode)



(Note) The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous characters.

Receiver Control and Flag Timing (SYNC Mode)



(Note 1) Internal synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous characters

(Note 2) External synchronization is based on the case of 5 data bit length + parity bit

OKI semiconductor

MSM82C51A-2RS/GS/JS

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

GENERAL DESCRIPTION

The MSM82C51A is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.

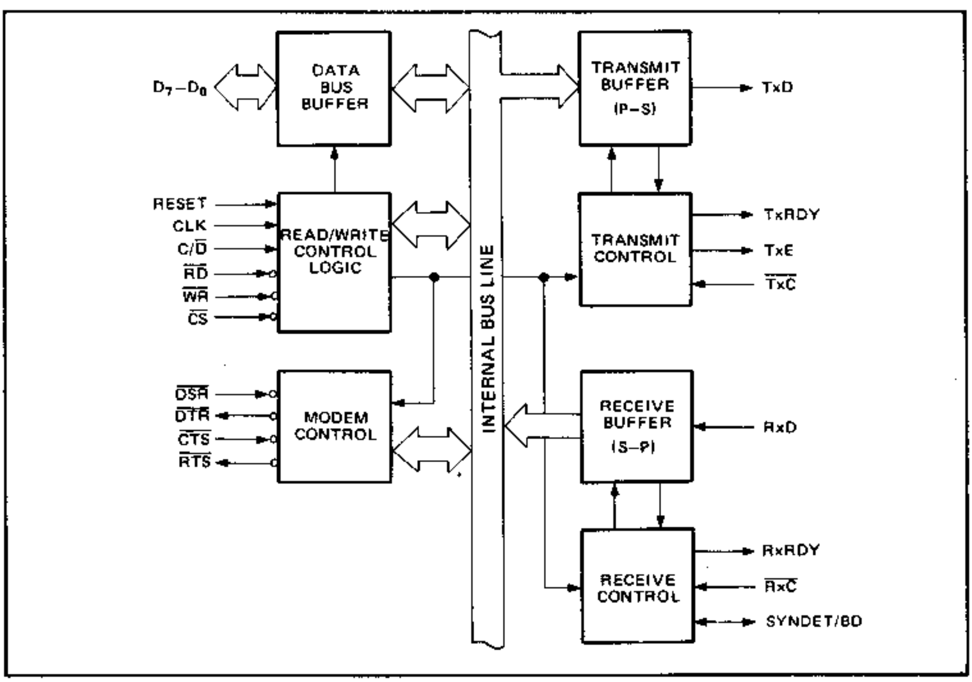
As a peripheral device of a microcomputer system, the MSM82C51A receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

The MSM82C51A configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on extremely low power at 100 μA (max) of standby current by suspending all operations.

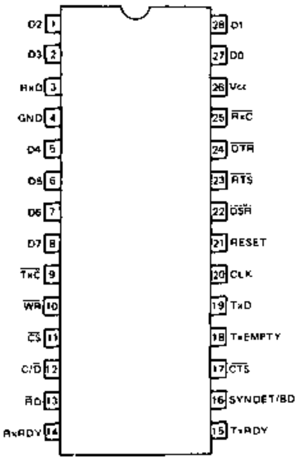
FEATURES

- Wide power supply voltage range from 3 V to 6 V.
- Wide temperature range from −40°C to 85°C.
- Synchronous communication upto 64K baud.
- Asynchronous communication upto 38.4K baud.
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin DIP (MSM82C51A-2RS)
- 32-pin flat package (MSM82C51A-2GS)
- 28-pin PLCC (MSM82C51A-2JS)

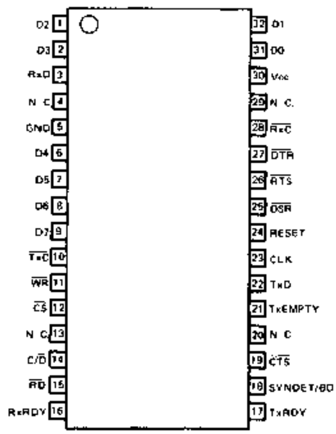
FUNCTIONAL BLOCK DIAGRAM



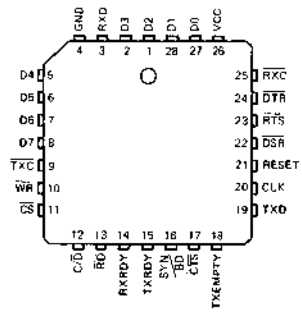
PIN CONFIGURATION



MSM82C51A-2RS (Top View)
28 Lead Plastic DIP



MSM82C51A-2GS (Top View)
32 Lead Plastic Flat Package



MSM82C51A-2JS (Top View)
28 Plastic Leaded
Chip Carrier

FUNCTION

Outline

The MSM82C51A's functional configuration is programed by software.

Operation between the MSM82C51A and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

Table 1 Operation between MSM82C51A and CPU

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	X	X	X	Data bus 3-state
0	X	1	1	Data bus 3-state
0	1	0	1	Status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting the MSM82C51A. Fig. 1 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.

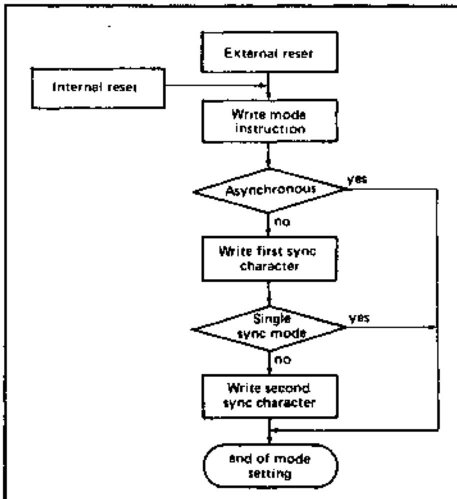


Fig. 1 Function-Setting Sequence (Mode Instruction Sequence)

Control Words

There are two types of control word.

1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the MSM82C51A. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."

Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- No. of synchronous characters (synchronous mode)

The bit configuration of mode instruction is shown in Fig.'s 2 and 3. In the case of synchronous mode, it is necessary to write one- or two-byte sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_2	S_1	EP	PEN	L_2	L_1	B_2	B_1

Baud rate factor

0	1	0	1
0	0	1	1
Refer to Fig. 3 SYNC	1x	16x	64x

Character length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity check

0	1	0	1
0	0	1	1
Disable	Odd parity	Disable	Even parity

Stop bit length

0	1	0	1
0	0	1	1
Inhibit	1 bit	1.5 bits	2 bits

Fig. 2 Bit Configuration of Mode Instruction (Asynchrnous)

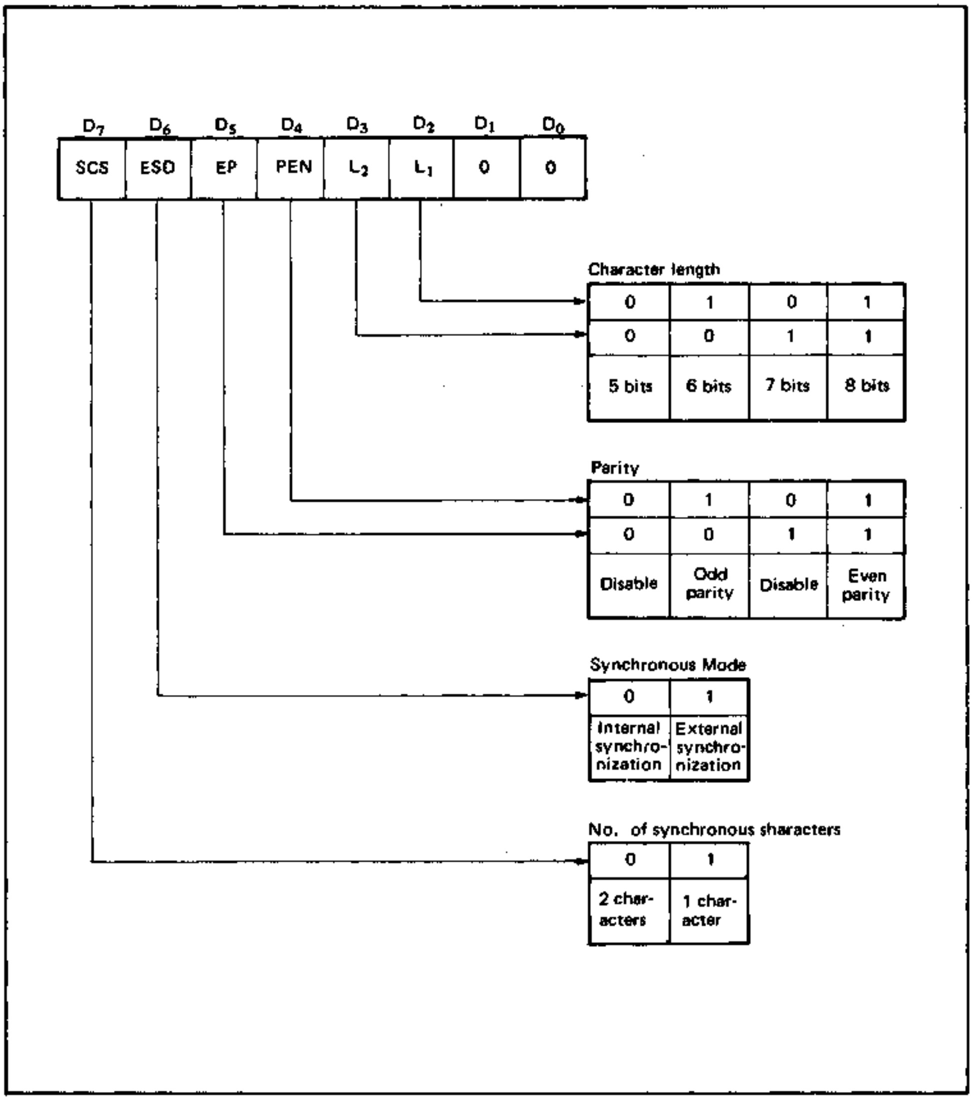


Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

2) Command

Command is used for setting the operation of the MSM82C51A.

It is possible to write a command whenever necessary after writing a mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data.
- Resetting of error flag.
- Sending of break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.

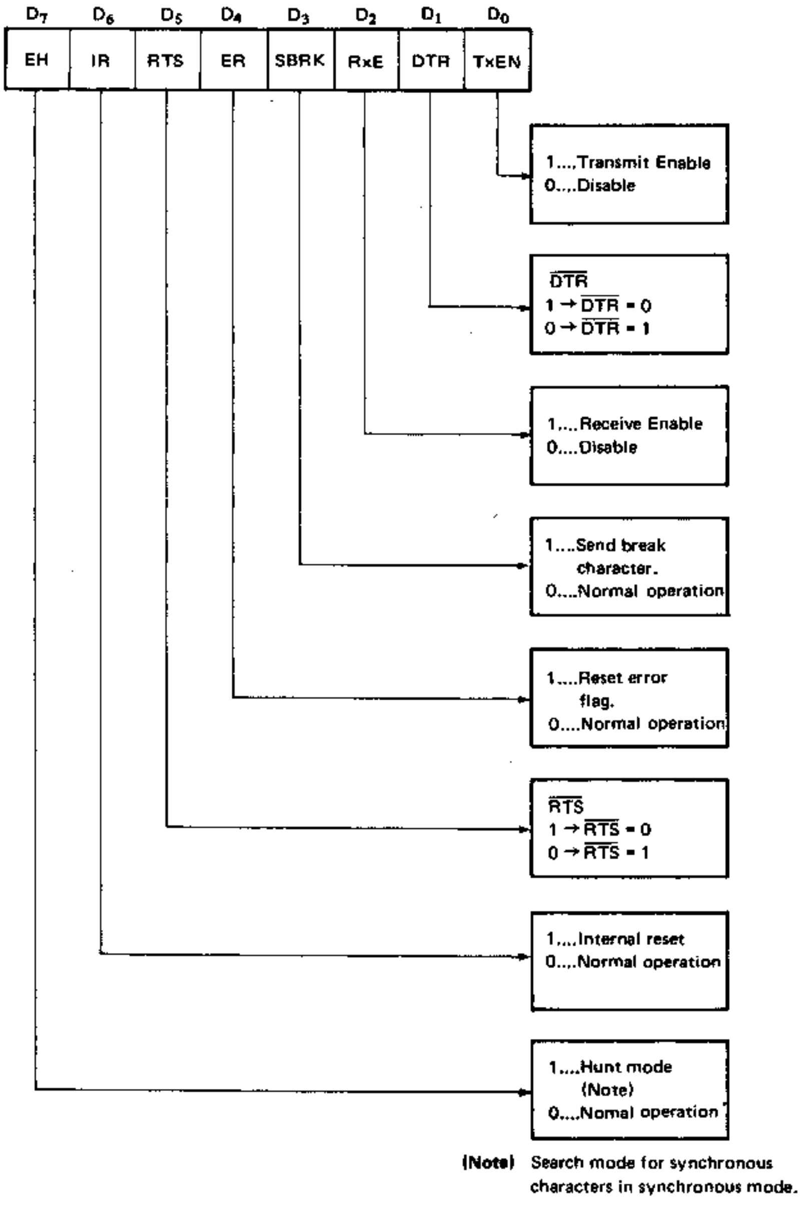


Fig. 4 Bit Configuration of Command

5

Status Word

It is possible to see the internal status of MSM-82C51A by reading a status word.

The bit configuration of status word is shown in Fig. 5.

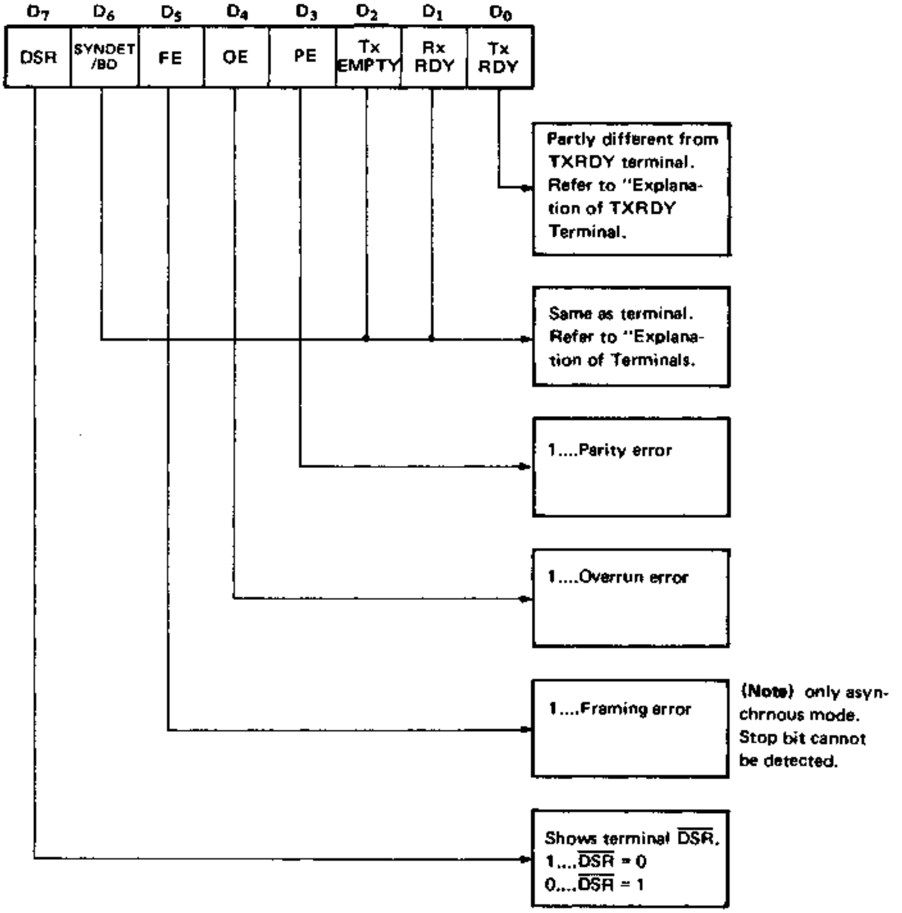


Fig. 5 Bit Configuration of Status Word

5

Standby Status

It is possible to put the MSM82C51A in "standby status".

When the following conditions have been satisfied the MSM82C51A is in "standby status."

(1) $\overline{CS}$ terminal is fixed at Vcc level.

(2) Input pins other than $\overline{CS}$, D_0 to D_7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are fixed at Vcc or GND level (including SYNDET in external synchronous mode).

Note When all output currents are 0, ICCS specification is applied.

Pin Description

D_0 to D_7 (I/O terminal)

This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the MSM82C51A into "reset status."

The device waits for the writing of "mode instruction."

The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing.

CLK signal is independent of $\overline{RXC}$ or $\overline{TXC}$.

However, the frequency of CLK must be greater than 30 times the $\overline{RXC}$ and $\overline{TXC}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{WR}$ (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the MSM82C51A.

$\overline{RD}$ (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the MSM82C51A.

C/$\overline{D}$ (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the MSM82C51A is accessed by the CPU.

If C/$\overline{D}$ = low, data will be accessed.

If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input terminal)

This is the "active low" input terminal which selects the MSM82C51A at low level when the CPU accesses.

Note The device won't be in "standby status"; only setting $\overline{CS}$ = High.
Refer to "Explanation of Standby Status."

TXD (Output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out.

The device is in "mark status" (high level) after resetting or during a status when transmit is disabled.

It is also possible to set the device in "break status" (low level) by a command.

TXRDY (Output terminal)

This is an output terminal which indicates that the MSM82C51A is ready to accept a transmitted data character. But the terminal is always at low level if $\overline{CTS}$ = high or the device was set in "TX disable status" by a command.

Note TXRDY status word indicates that transmit data character is receivable, regardless of $\overline{CTS}$ or command.

IF the CPU writes a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the MSM82C51A has transmitted all the characters and had no data character.

In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted.

If the CPU writes a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

Note As the transmitter is disabled by setting $\overline{CTS}$ "High" or command, data written before disable will be sent out. Then TXD and TXEMPTY will be "High".
Even if a data is written after disable, that data is not sent out and TXE will be "High". After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

$\overline{TXC}$ (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data.

In "synchronous mode," the baud rate will be the same as the frequency of $\overline{TXC}$.

In "asynchronous mode", it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16 or 1/64 the $\overline{TXC}$.

The falling edge of $\overline{TXC}$ sifts the serial data out of the MSM82C51A.

RXD (Input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the MSM82C51A contains a character that is ready to READ.

If the CPU reads a data character, RXRDY will be reset by the leading edge of $\overline{RD}$ signal.

Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

$\overline{\text{RXC}}$ (Input terminal)

This is a clock input signal which determines the transfer speed of received data.

In "synchronous mode," the baud rate is the same as the frequency of $\overline{\text{RXC}}$.

In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.

It can be 1, 1/16, 1/64 the $\overline{\text{RXC}}$.

SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode.

In "internal synchronous mode," this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset.

In "external synchronous mode," this is an input terminal.

A "High" on this input forces the MSM82C51A to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level" output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

$\overline{\text{DSR}}$ (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

$\overline{\text{DTR}}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{DTR}}$ by a command.

$\overline{\text{CTS}}$ (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

$\overline{\text{RTS}}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{RTS}}$ by a command.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits			Unit	Conditions
		MSM82C51A-2RS	MSM82C51A-2GS	MSM82C51A-2JS		
Power supply voltage	V_{CC}	−0.5 ~ +7			V	With respect to GND
Input voltage	V_{IN}	−0.5 ~ V_{cc} + 0.5			V	
Output voltage	V_{OUT}	−0.5 ~ V_{cc} + 0.5			V	
Storage temperature	T_{stg}	−55 ~ +150			°C	—
Power dissipation	P_D	0.9	0.7	0.9	W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	T_{OP}	−40	+25	+85	°C
"L" input voltage	V_{IL}	−0.3		+0.8	V
"H" input voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

(Vcc = 4.5 ~ 5.5V Ta = −40°C ~ +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
"L" output voltage	V_{OL}			0.45	V	I_{OL} = 2.5 mA
"H" output voltage	V_{OH}	3.7			V	I_{OH} = −2.5 mA
Input leak current	I_{LI}	−10		10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output leak current	I_{LO}	−10		10	μA	$0 \leq V_{OUT} \leq V_{CC}$
Operating supply current	I_{CCO}			5	mA	Asynchronous X64 during transmitting/receiving
Standby supply current	I_{CCS}			100	μA	All input voltage shall be fixed at V_{CC} or GND level.

AC CHARACTERISTICS

(Vcc = 4.5 ~ 5.5V, Ta = −40 ~ 85°C)

CPU Bus Interface Part

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address stable before $\overline{RD}$	t_{AR}	20		NS	Note 2
Address hold time for $\overline{RD}$	t_{RA}	20		NS	Note 2
$\overline{RD}$ pulse width	t_{RR}	130		NS	
Data delay from $\overline{RD}$	t_{RD}		100	NS	
$\overline{RD}$ to data float	t_{DF}	10	75	NS	
Recovery time between $\overline{RD}$	t_{RVR}	6		T_{cy}	Note 5
Address stable before $\overline{WR}$	t_{AW}	20		NS	Note 2
Address hold time for $\overline{WR}$	t_{WA}	20		NS	Note 2
$\overline{WR}$ pulse width	t_{WW}	100		NS	
Data set-up time for $\overline{WR}$	t_{DW}	100		NS	
Data hold time for $\overline{WR}$	t_{WD}	0		NS	
Recovery time between $\overline{WR}$	t_{RVW}	6		T_{cy}	Note 4
RESET pulse width	t_{RESW}	6		T_{cy}	

Serial Interface Part

Parameter		Symbol	Min.	Max.	Unit	Remarks
Main clock period		t_{cy}	160		NS	Note 3
Clock low time		$t_{\overline{\phi}}$	50		NS	
Clock high time		t_{ϕ}	70	$t_{cy}-50$	NS	
Clock rise/fall time		t_R, t_F		20	NS	
TXD delay from falling edge of $\overline{TXC}$		t_{DTX}		1	μS	
Transmitter clock frequency	1X Baud	f_{TX}	DC	64	kHz	Note 3
	16X, Baud	f_{TX}	DC	615	kHz	
	64X, Baud	f_{TX}	DC	615	kHz	
Transmitter clock low time	1X Baud	t_{TPW}	13		T_{cy}	
	16X, 64X Baud	t_{TPW}	2		T_{cy}	
Transmitter clock high time	1X Baud	t_{TPD}	15		T_{cy}	
	16X, 64X Baud	t_{TPD}	3		T_{cy}	
Receiver clock frequency	1X Baud	f_{RX}	DC	64	kHz	Note 3
	16X Baud	f_{RX}	DC	615	kHz	
	64X Baud	f_{RX}	DC	615	kHz	
Receiver clock low time	1X Baud	t_{RPW}	13		T_{cy}	
	16X, 64X Baud	t_{RPW}	2		T_{cy}	
Receiver clock high time	1X Baud	t_{RPD}	15		T_{cy}	
	16X, 64X Baud	t_{RPD}	3		T_{cy}	
Time from the center of last bit to the rise of TXRDY		t_{TXRDY}		8	T_{cy}	
Time from the leading edge of $\overline{WR}$ to the fall of TXRDY		$t_{TXRDY\ CLEAR}$		400	NS	
Time from the center of last bit to the rise of RXRDY		t_{RXRDY}		26	T_{cy}	

5

Parameter	Symbol	Min.	Max.	Unit	Remarks
Time from the leading edge of $\overline{RD}$ to the fall of RXRDY	$t_{RXRDY\ CLEAR}$		400	NS	
Internal SYNDET delay time from rising edge of $\overline{RXC}$	t_{IS}		26	T_{cy}	
SYNDET setup time for $\overline{RXC}$	t_{ES}	18		T_{cy}	
TXE delay time from the center of last bit	$t_{TXEMPTY}$	20		T_{cy}	
MODEM control signal delay time from rising edge of $\overline{WR}$	t_{WC}	8		T_{cy}	
MODEM control signal setup time for falling edge of $\overline{RD}$	t_{CR}	20		T_{cy}	
RXD setup time for rising edge of $\overline{RXC}$ (1X Baud)	t_{RXDS}	11		T_{cy}	
RXD hold time for falling edge of $\overline{RXC}$ (1X Baud)	t_{RXDH}	17		T_{cy}	

Caution 1) AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.

2) Addresses are $\overline{CS}$ and C/$\overline{D}$.

3) f_{TX} or $f_{RX} \leq 1/(30\ Tcy)$ 1 x baud
f_{TX} or $f_{RX} \leq 1/(5\ Tcy)$ 16 x, 64 x Baud

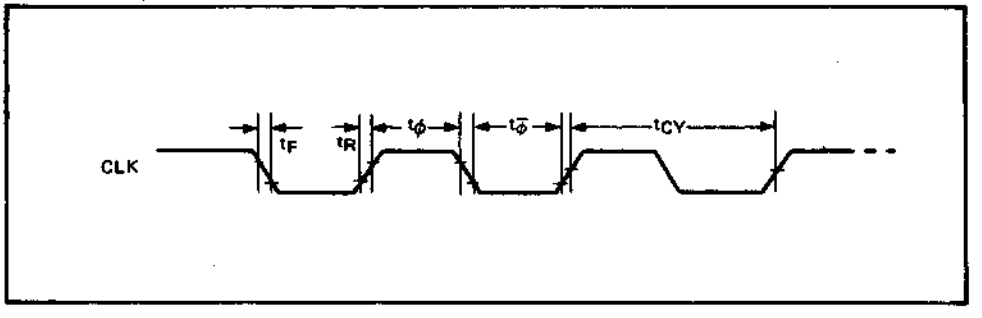
4) This recovery time is mode Initialization only. Recovery time between command writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 18 t_{CY}.
Write Data is allowed only when TXRDY = 1.

5) This recovery time is Status read only.
Read Data is allowed only when RXRDY = 1.

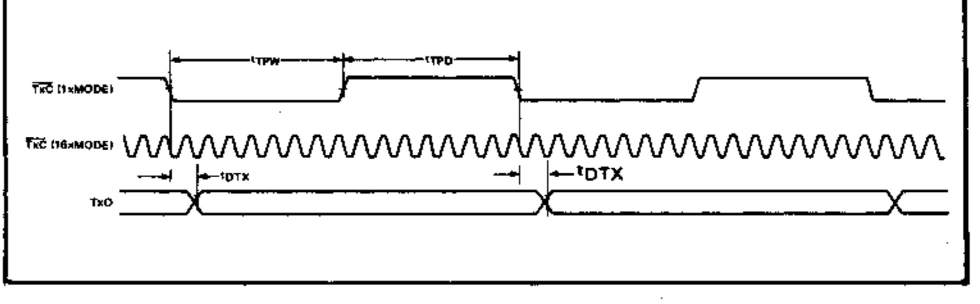
6) Status update can have a maximum delay of 28 clock periods from event affecting the status.

TIMING CHART

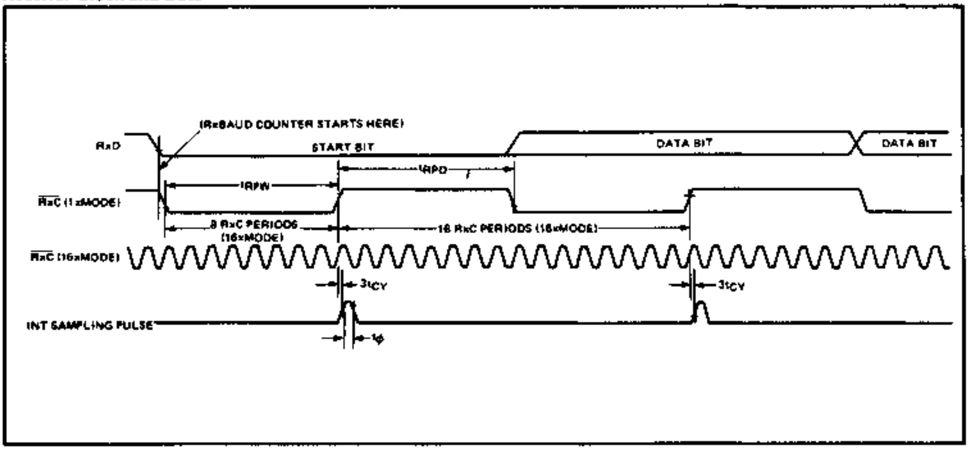
System Clock Input



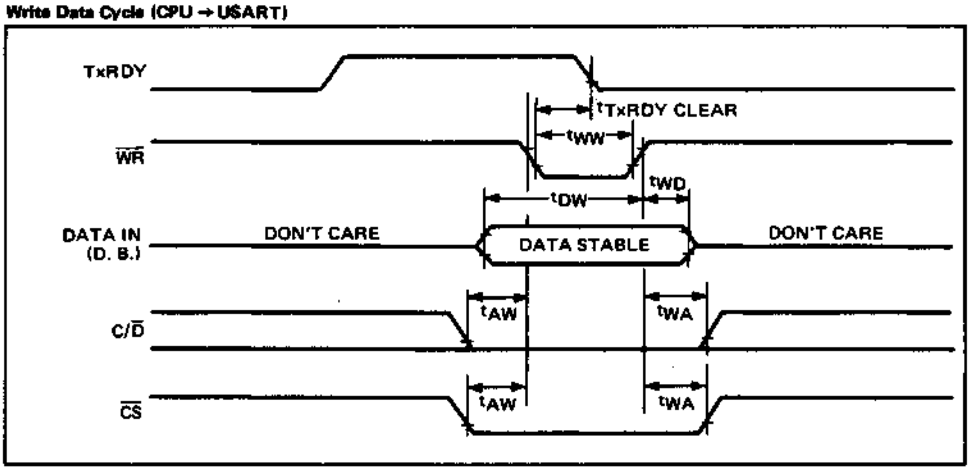
Transmitter Clock and Data



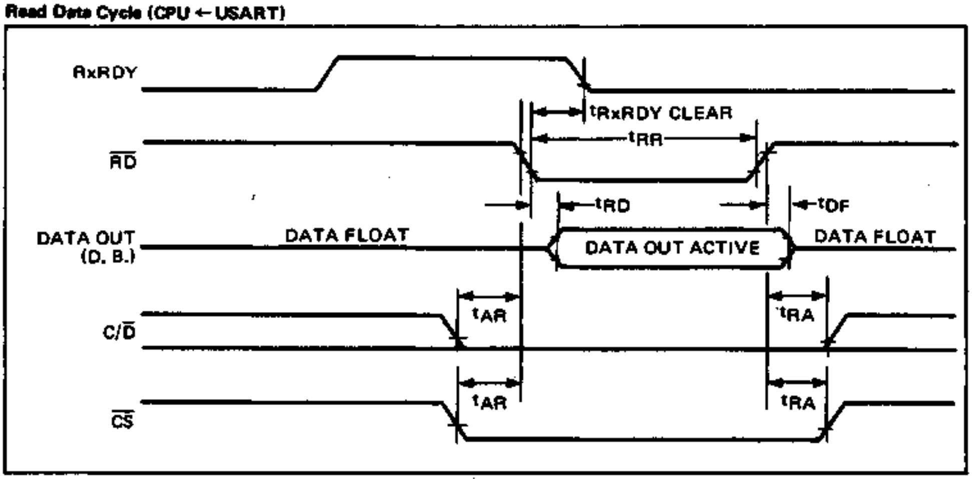
Receiver Clock and Data



Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)



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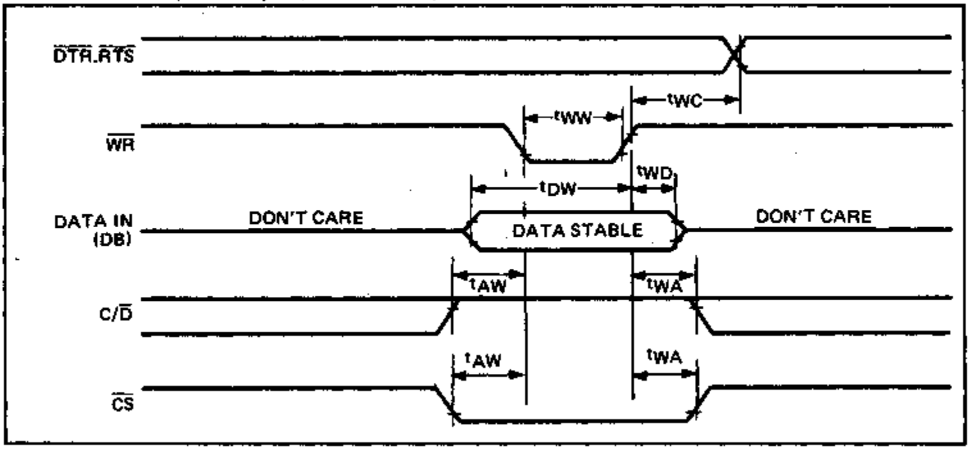
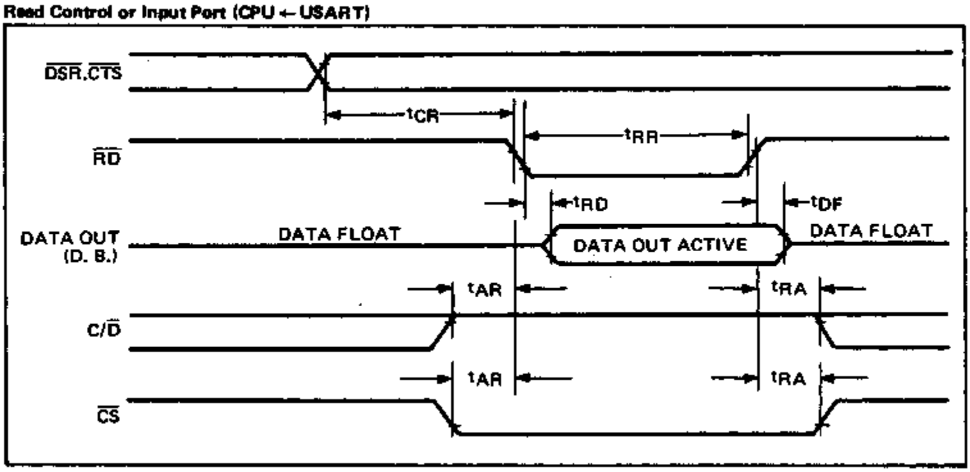
Write Control or Output Port Cycle (CPU → USART)



Read Control or Input Port (CPU ← USART)



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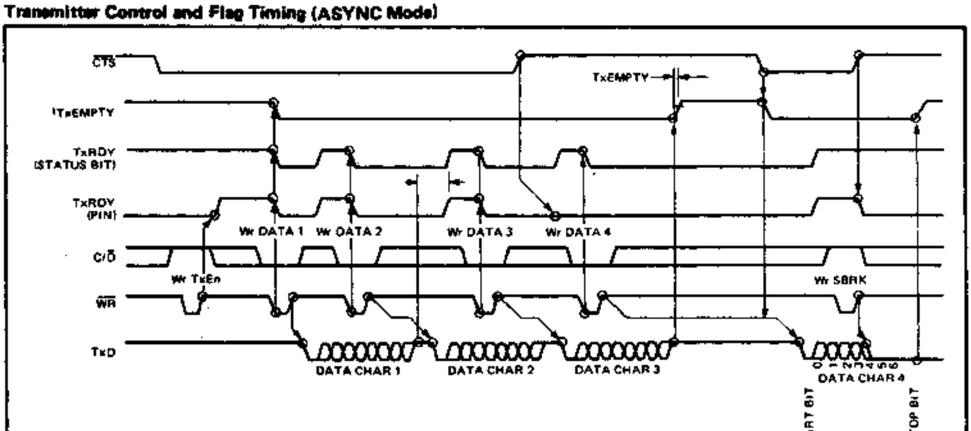
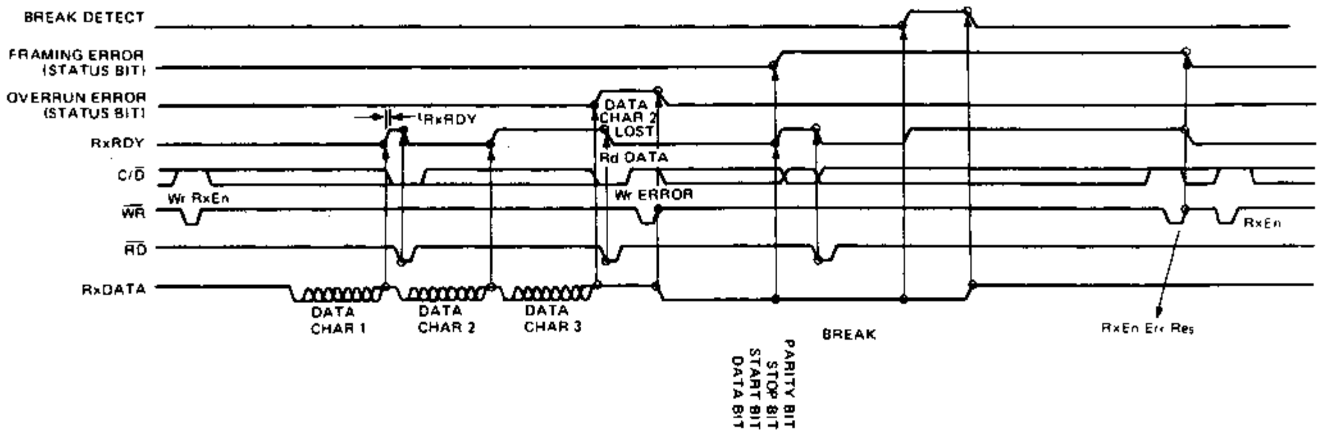
Transmitter Control and Flag Timing (ASYNC Mode)



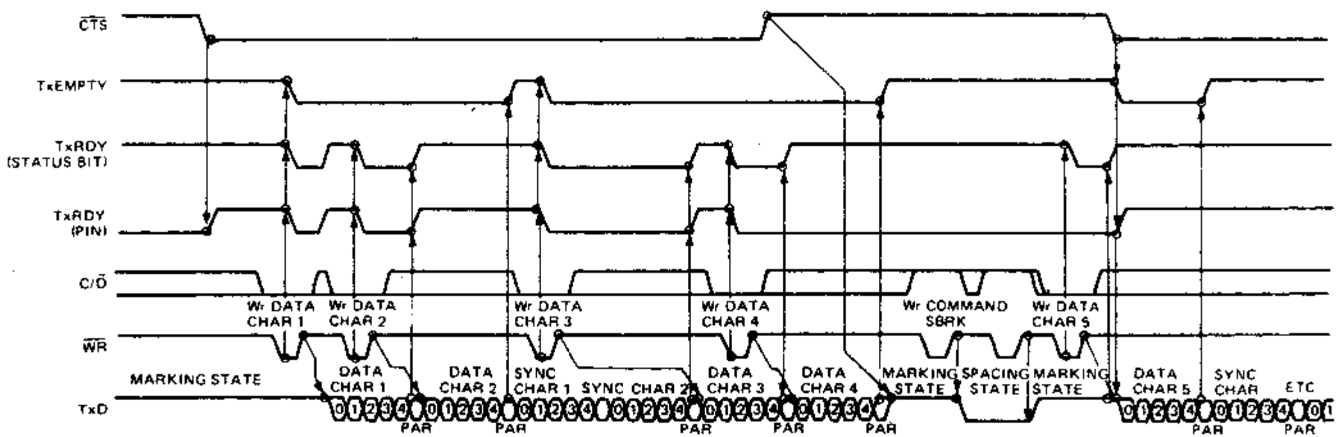
(Note) The wave-form chart is based on the case of 7 bit data length + parity bit + 2 stop bit.

Receiver Control and Flag Timing (ASYNC Mode)



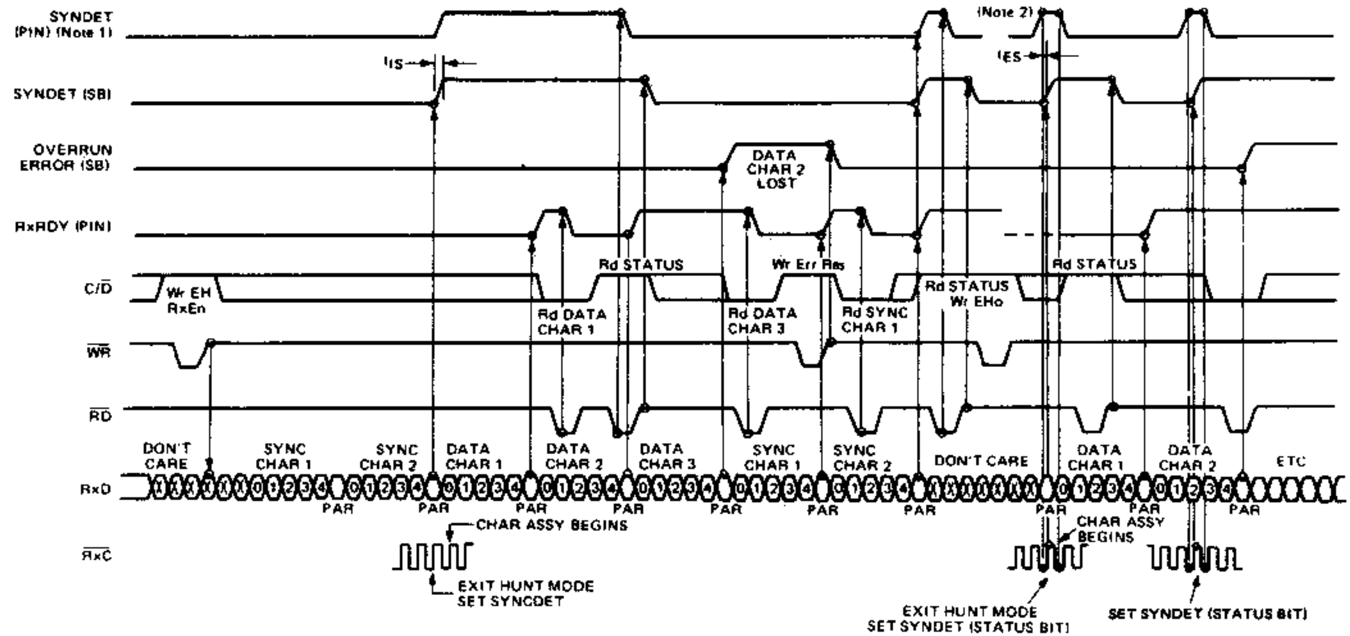
(Note) The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.

Transmitter Control and Flag Timing (SYNC Mode)



(Note) The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous characters.

Receiver Control and Flag Timing (SYNC Mode)



(Note 1) Internal synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous characters.

(Note 2) External synchronization is based on the case of 5 data bit length + parity bit.

OKI semiconductor

MSM82C53-5RS/GS/JS
MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

The MSM82C53-5RS/GS/JS and MSM82C53-2RS/GS/JS are programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100 μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 5 mA (max.) at 5 MHz of current required.

The devices consist of three independent counters, and can count up to a maximum of 5 MHz (MSM82C53-5) and 8 MHz (MSM82C53-2). The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

- Maximum operating frequency of 5 MHz (MSM82C53-5)
- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24-pin DIP (MSM82C53-5RS/MSM82C53-2RS)
- 32-pin flat package (MSM82C53-5GS/MSM82C53-2GS)
- 28-pin PLCC Package (MSM82C53-5JS/MSM82C53-2JS)

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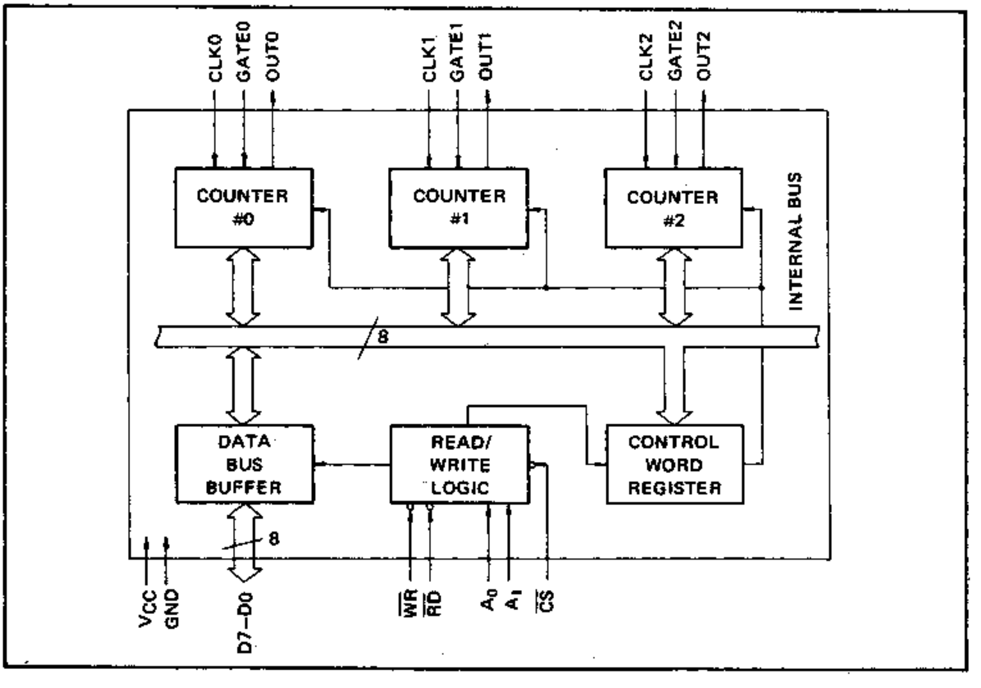
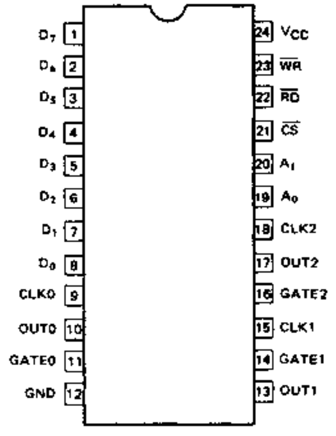
FUNCTIONAL BLOCK DIAGRAM

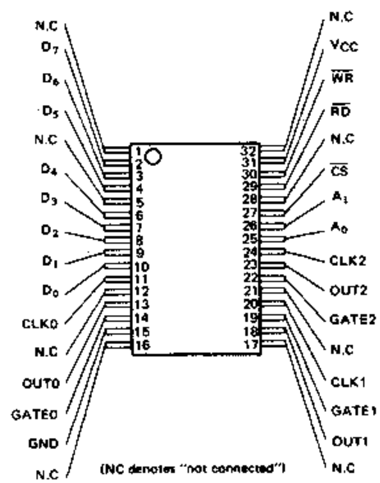


PIN CONFIGURATION

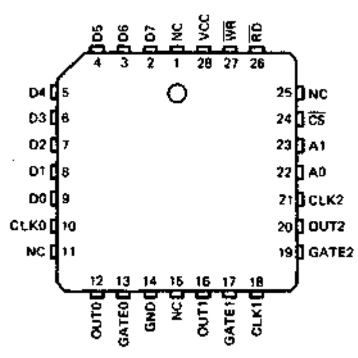
MSM82C53-5RS (Top View)
MSM82C53-2RS
24 LEAD PLASTIC DIP



MSM82C53-5GS (Top View)
MSM82C53-2GS
32 LEAD PLASTIC FLAT PACKAGE



MSM82C53-5JS (Top View)
MSM82C53-2JS
28 Plastic Leaded Chip Carrier



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-5RS MSM82C53-2RS	MSM82C53-5GS MSM82C53-2GS	MSM82C53-5JS MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}	Respect to GND	−0.5 to V_{cc} + 0.5			V
Output Voltage	V_{OUT}	Respect to GND	−0.5 to V_{cc} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA				0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	V_{CC}=4.5V to 5.5V	−10		10	µA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	Ta=−40°C to +85°C	−10		10	µA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ − 0.2V $V_{IL} \leq$ 0.2V				100	µA
Operating Supply Current	I_{CC}	t_{CLK} = 200 ns C_L = 0pF				5	mA
		t_{CLK} = 125 ns C_L = 0pF	MSM82C53-2			8	mA

AC CHARACTERISTICS

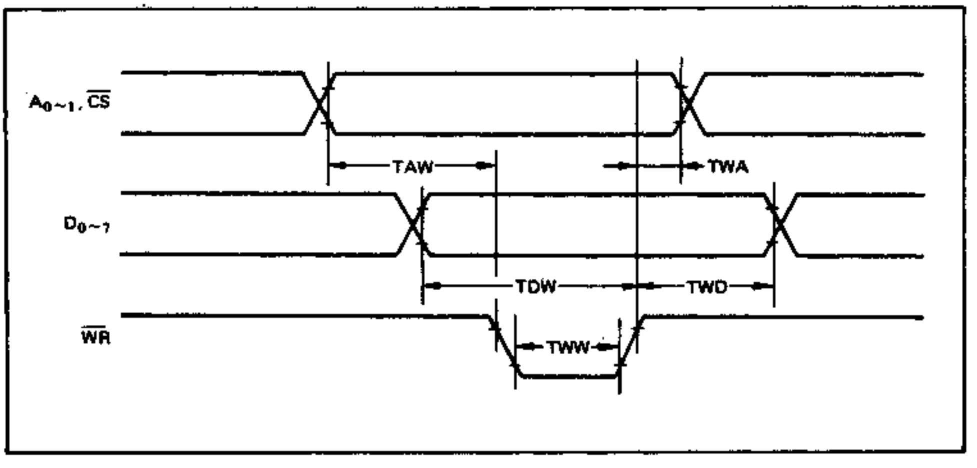
(V_{CC} = 4.5V ~ 5.5V, Ta = −40 ~ +85°C)

Parameter	Symbol	MSM82C53-5 Min.	MSM82C53-5 Max.	MSM82C53-2 Min.	MSM82C53-2 Max.	Unit	Conditions	
Address Set-up Time before reading	TAR	30		30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		0		ns		
Read Pulse Width	TRR	150		150		ns		
Read Recovery Time	TRVR	200		200		ns		
Address Set-up Time before writing	TAW	0		0		ns	Write cycle	
Address Hold Time after writing	TWA	30		20		ns		
Write Pulse Width	TWW	150		150		ns		
Data Input Set-up Time before writing	TDW	100		100		ns		
Data Input Hold Time after writing	TWD	30		20		ns		
Write Recovery time	TRVW	200		200		ns		
Clock Cycle Time	TCLK	200	D.C.	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		60		ns		
Clock "L" Pulse Width	TPWL	60		60		ns		
"H" Gate Pulse Width	TGW	50		50		ns		
"L" Gate Pulse Width	TGL	50		50		ns		
Gate Input Set-up Time before clock	TGS	50		50		ns		
Gate Input Hold Time after clock	TGH	50		50		ns		
Output Delay Time after reading	TRD		120		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	5	90	ns		
Output Delay Time after gate	TODG		120		120	ns		
Output Delay Time after clock	TOD		150		150	ns		
Output Delay Time after address	TAD		180		180	ns		

Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

Write Timing



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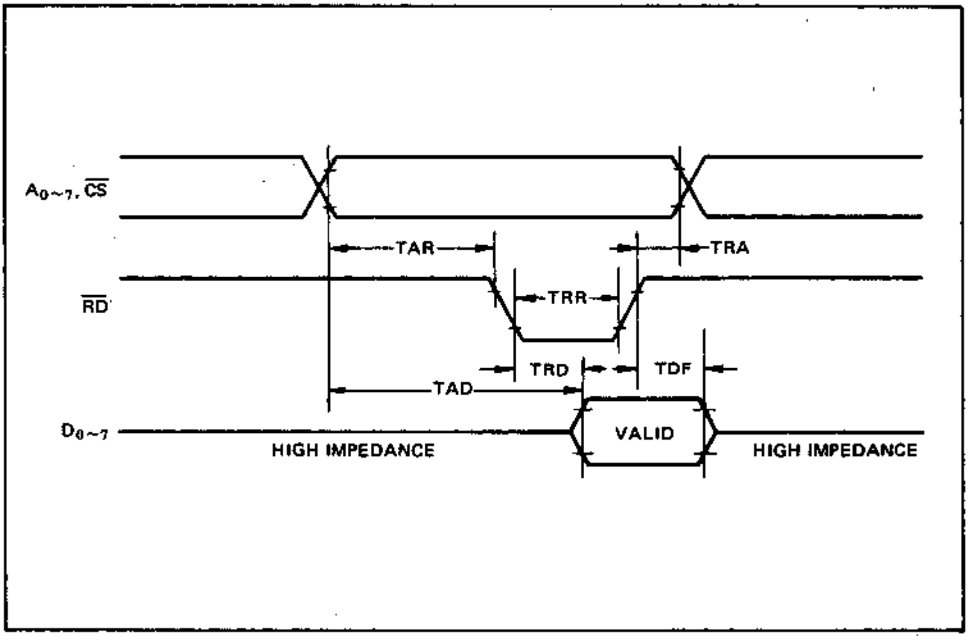
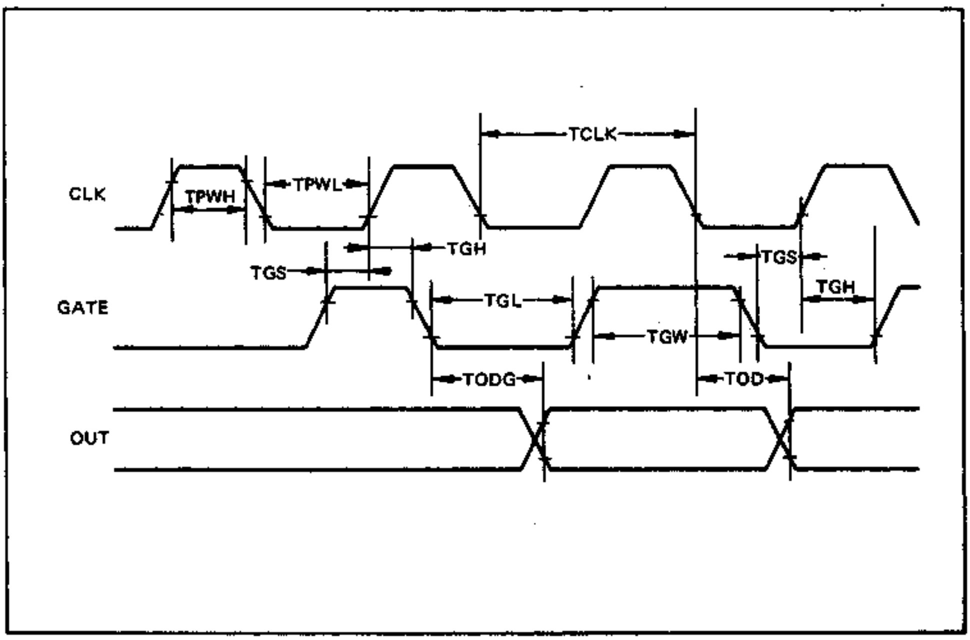
Read Timing



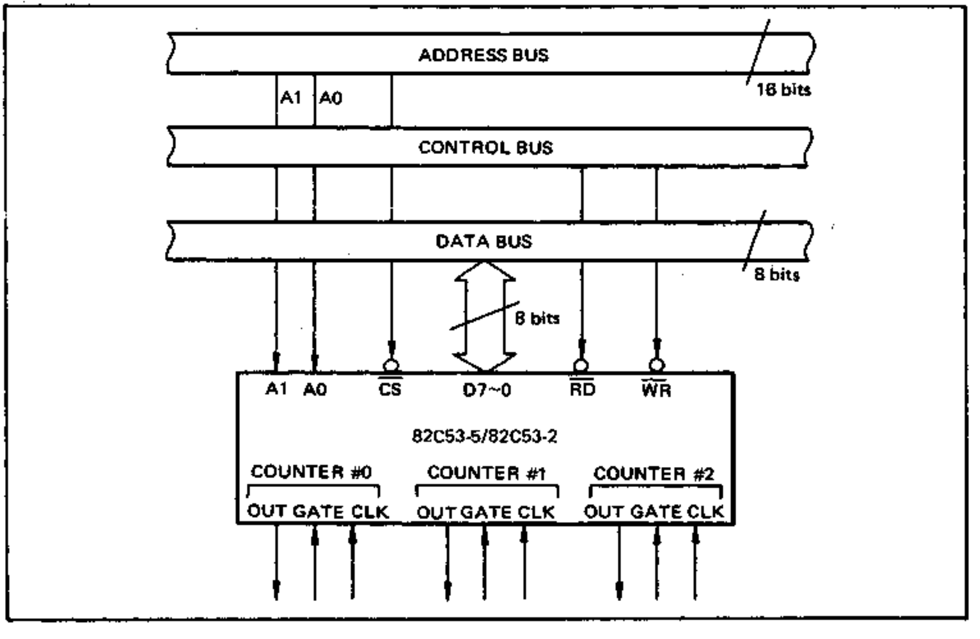
Clock & Gate Timing



DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	Data bus in high impedance status
0	1	1	x	x	Data bus in high impedance status

x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

- **Example of control word and count value setting**

  Counter # 0: Read/Load LSB only, Mode 3, Binary count, count value 3H
  Counter # 1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
  Counter # 2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH ]  Counter #0 control word setting
OUT n3     ]
MVI A, 6AH ]  Counter #1 control word setting
OUT n3     ]
MVI A, B1H ]  Counter #2 control word setting
OUT n3     ]
MVI A, 03H ]  Counter #0 count value setting
OUT n0     ]
MVI A, AAH ]  Counter #1 count value setting
OUT n1     ]
MVI A, 34H ]
OUT n2     ]  Counter #2 count value setting
MVI A, 12H ]  (LSB then MSB)
OUT n2     ]
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**

  The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.

  Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.

  When Count Values are written during counting, the operation is as follows:

  1 byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

  2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**

  The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.

  Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**

  The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.

  An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

- **Mode 3 (square waveform rate generator)**

  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.

  The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n – 1)/2 clock inputs at "L" level.

  If a new count value is written during counting, the new count value is reflected immediately after the

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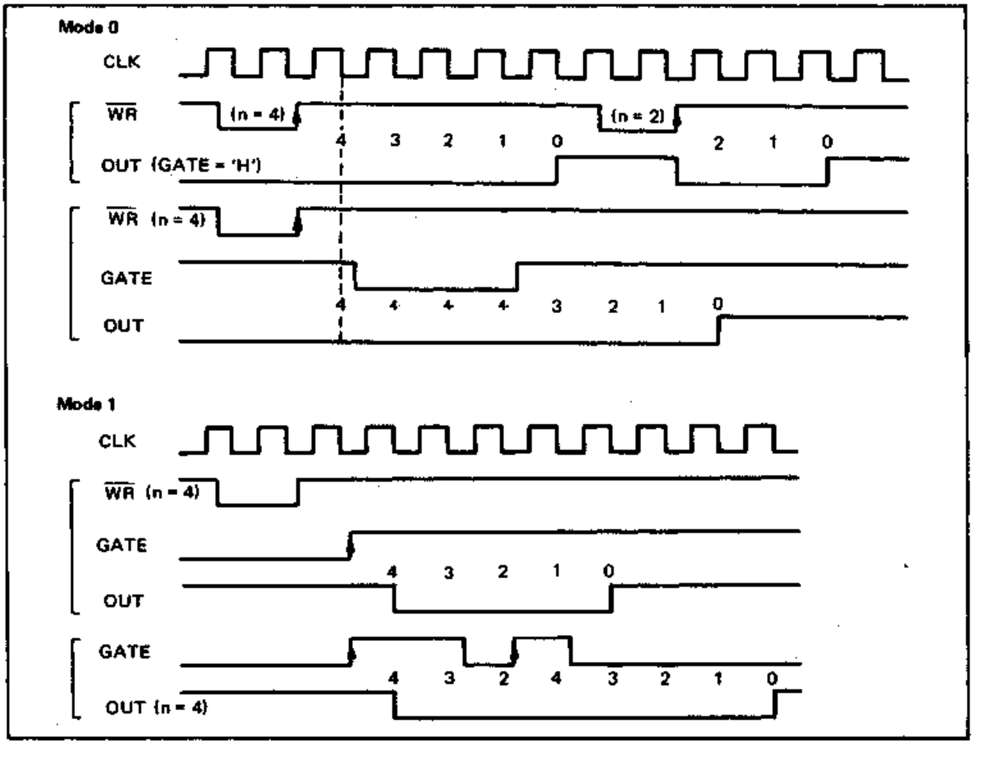
change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

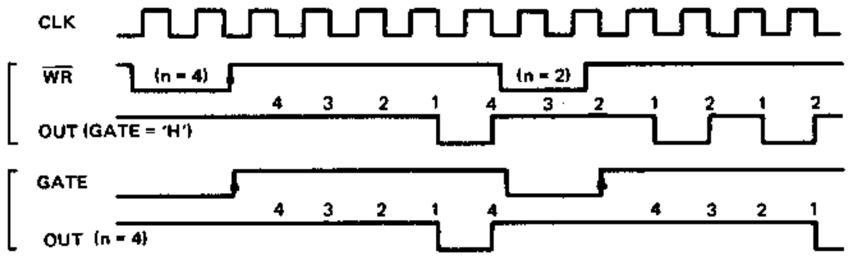
- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

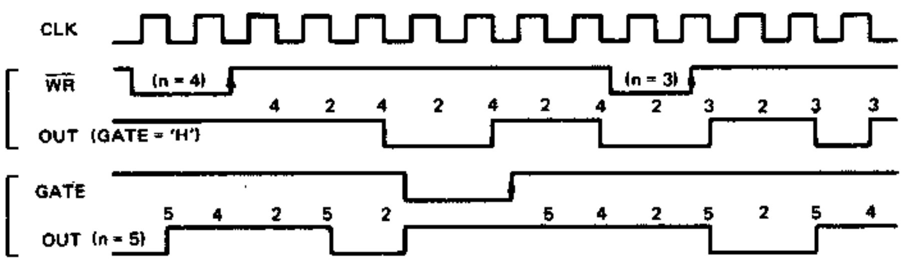
Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



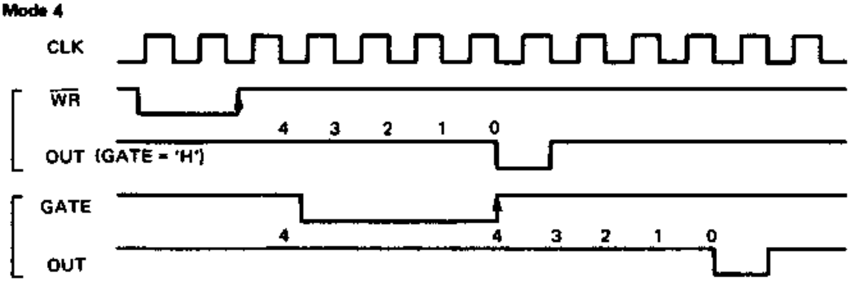
Mode 2



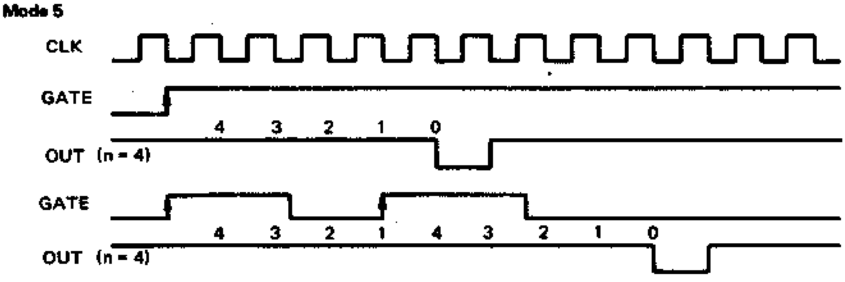
Mode 3



Mode 4



Mode 5



Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

- **Direct reading**

  Counter values can be read by direct reading operations.

  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**

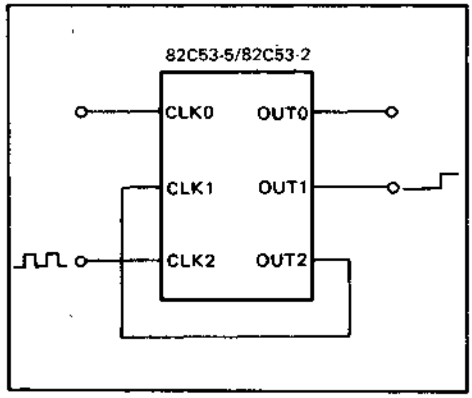
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.

  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  0 1 0 0 x x x x
            └── Denotes counter latching
OUT n3 ──────┬── Write in control word address (n3)
             └── The counter value at this point is latched
IN n1 ───────┬── Reading of the LSB of the counter value latched from counter #1.
             └── n1: Counter #1 address
MOV B, A
IN n1       ──── Reading of MSB from counter #1.
MOV C, A
```

Example of Practical Application

- 82C53 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.

Preliminary

OKI semiconductor

MSM82C54-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

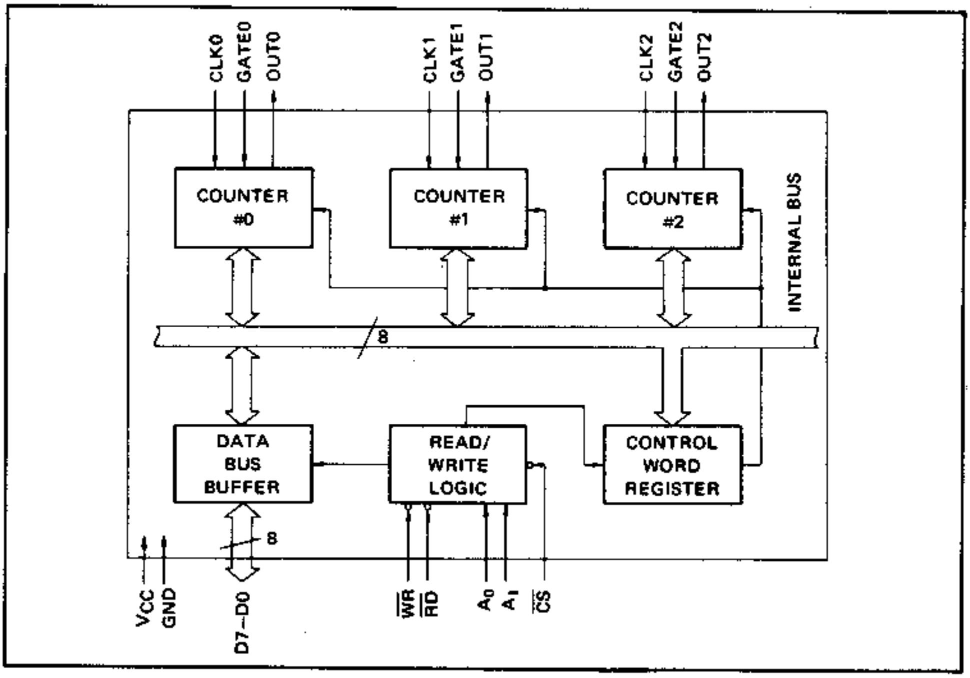
The MSM82C54-2RS/GS/JS is a programmable universal timer designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 10 μA (max.) when the chip is in the non-selected state. And during timer operation, the power consumption is still very low with only 10mA (max.) of current required.

It consists of three independent counters, and can count up to a maximum of 10 MHz. The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are frealy programmable.

FEATURES

- Maximum operating frequency of 10 MHz (V_{CC}=5V)
- High speed and low power consumption achieved by silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- Status Read Back Commound
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24-pin DIP (MSM82C54-2RS)
- 32-pin flat package (MSM82C54-2GS)
- 28-pin PLCC package (MSM82C54-2JS)

FUNCTIONAL BLOCK DIAGRAM



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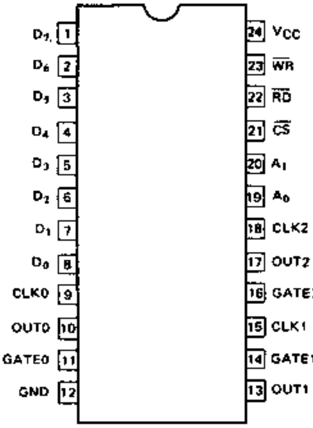
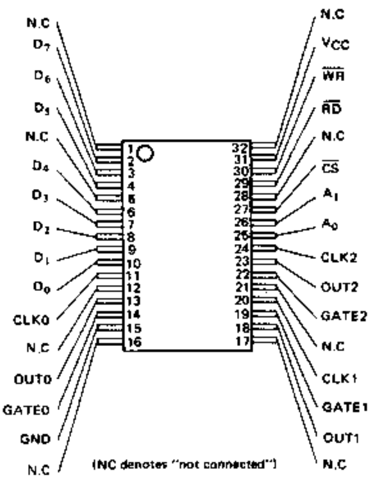
PIN CONFIGURATION

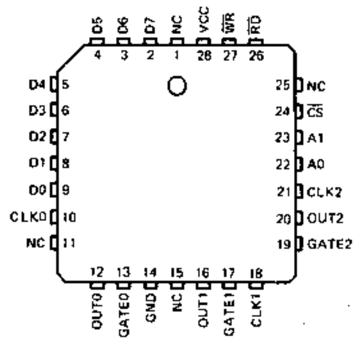
MSM82C54-2RS (TOP VIEW)
24 LEAD PLASTIC DIP



MSM82C54-2GS (TOP VIEW)
32 LEAD PLASTIC FLAT PACKAGE



MSM82C54-2JS (TOP VIEW)
28 Plastic Leaded Chip Carrier PACKAGE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C54-2RS	MSM82C54-2GS	MSM82C54-2JS	
Supply voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}	Respect to GND	-0.5 to $V_{CC}+0.5$			V
Output Voltage	V_{OUT}	Respect to GND	-0.5 to $V_{CC}+0.5$			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	-40	+25	+85	°C
"L" Input Voltage	V_{IL}	-0.5		+0.8	V
"H" Input Voltage	V_{IH}	2.2		$V_{CC}+0.5$	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 2.5mA	V_{CC}=4.5V to 5.5V, Ta=−40°C to +85°C			0.40	V
"H" Output Voltage	V_{OH}	I_{OH} = −2.5mA		3.0			V
		I_{OH} = −100µA		$V_{CC}-0.4$			
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	µA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	µA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{IH} \geq V_{CC}-0.2V$ $V_{IL} \leq 0.2V$				10	µA
Operating Supply Current	I_{CC}	t_{CLK}=100ns CL=0pF				10	mA

AC CHARACTERISTICS

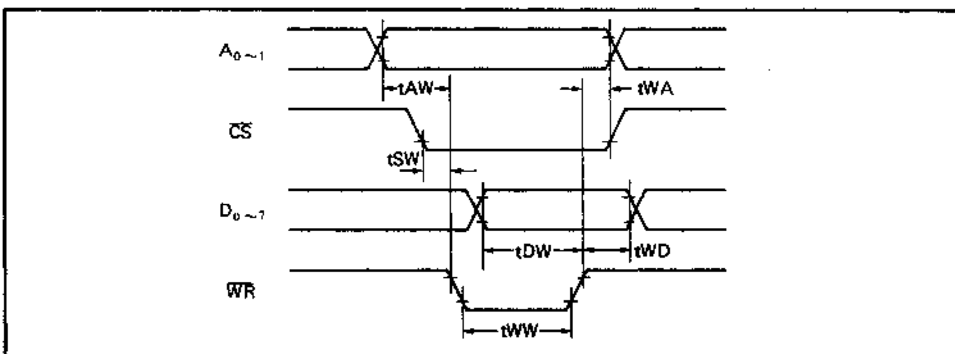
(V_{CC} = 4.5V ~ 5.5V, Ta = −40 ~ +85°C)

Parameter	Symbol	82C54-2 Min	82C54-2 Max	Unit	Conditions	
Address set-up time to falling edge of $\overline{RD}$	tAR	30		nS	Read timing	CL=150pF
Chip select input set-up time to falling edge of $\overline{RD}$	tSR	0		nS		
Address hold time from rising edge of $\overline{RD}$	tRA	0		nS		
$\overline{RD}$ pulse width	tRR	95		nS		
Data access time from falling edge of $\overline{RD}$	tRD		94	nS		
Data access time after address determination	tAD		185	nS		
Delay time from rising edge of $\overline{RD}$ to data floating state	tDF	5	65	nS		
$\overline{RD}$ recovery time	tRV	165		nS		
Address set-up time to falling edge of $\overline{WR}$	tAW	0		nS	Write timing	
Chip select input set-up time to falling edge of $\overline{WR}$	tSW	0		nS		
Address hold time from rising edge of $\overline{WR}$	tWA	0		nS		
$\overline{WR}$ pulse width	tWW	95		nS		
Data determination set-up time to rising edge of $\overline{WR}$	tDW	85		nS		
Data hold time after rising edge of $\overline{WR}$	tWD	0		nS		
$\overline{WR}$ recovery time	tRV	165		nS		
CLK cycle time	tCLK	100	D.C.	nS	Clock gate timing	
CLK "H" level width	tPWH	30		nS		
CLK "L" level width	tPWL	50		nS		
CLK rise time	tR		25	nS		
CLK fall time	tF		25	nS		
GATE "H" level width	tGW	50		nS		
GATE "L" level width	tGL	50		nS		
GATE input set-up time before rising edge of CLK	tGS	40		nS		
GATE input hold time before rising edge of CLK	tGH	50		nS		
Output delay time after falling edge of CLK	tOD		100	nS		
Output delay time after falling edge of GATE	tODG		100	nS		
CLK rise delay time after rising edge of $\overline{WR}$ for count value loading	tWC	0	55	nS		
GATE sampling delay time after rising edge of $\overline{WR}$ for count value loading	tWG	−5	40	nS		
Output delay time after falling edge of $\overline{WR}$ for mode set	tWO		240	nS		
CLK fall set-up time to falling edge of for counter latch command	tCL	−40	40	nS		

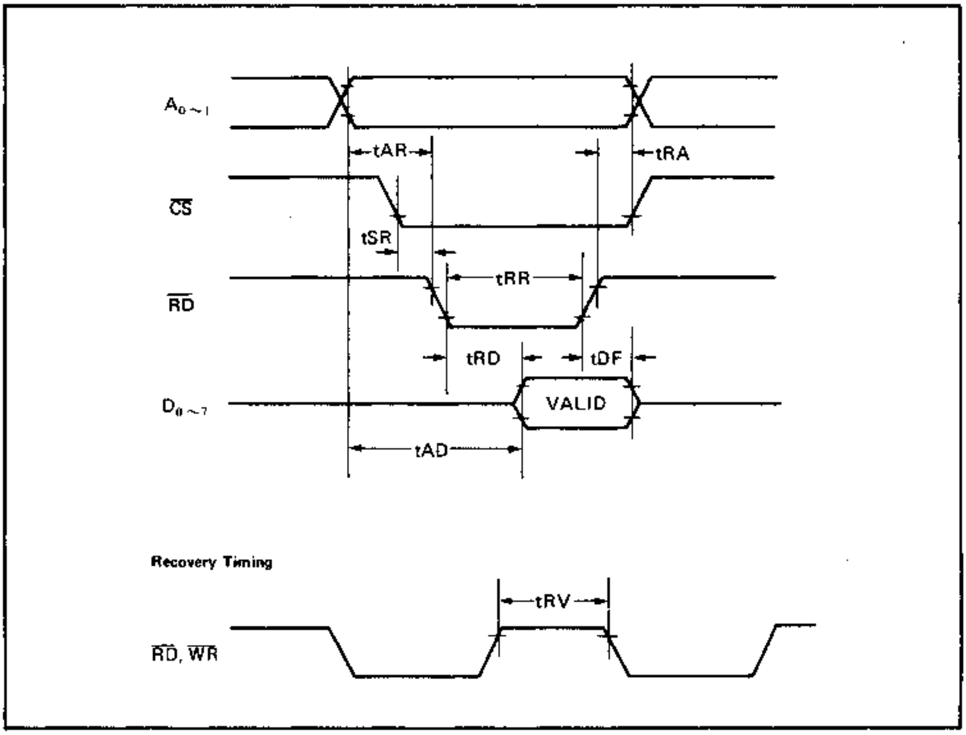
Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

Write Timing



Read Timing



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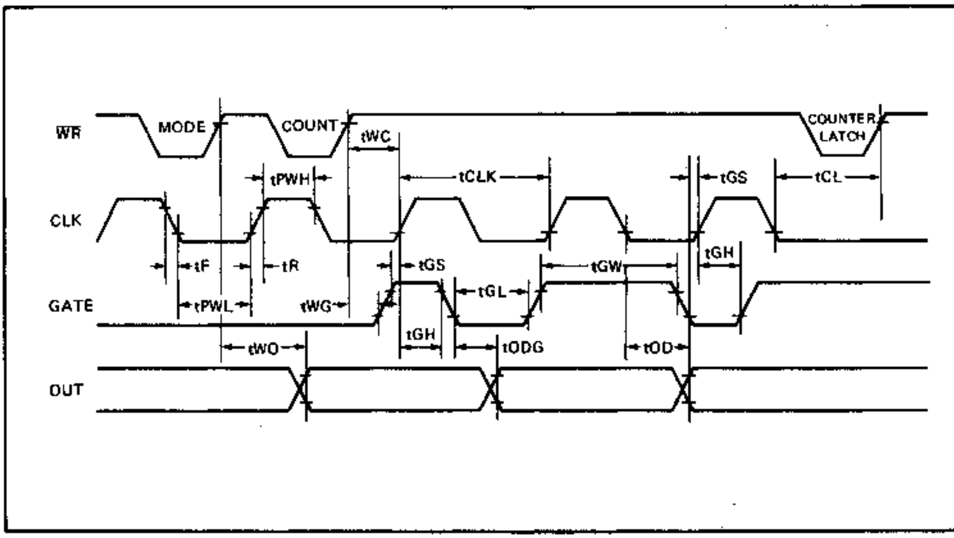
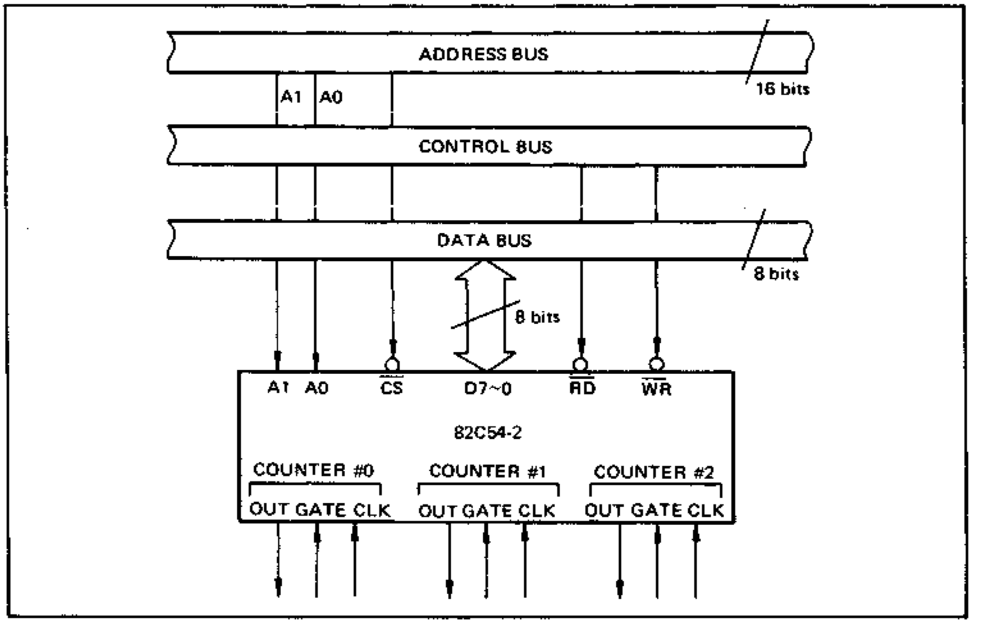
Clock & Gate Timing



DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C54-2 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C54-2 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C54-2.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	Data bus in high impedance status
0	1	1	x	x	Data bus in high impedance status

x denotes "not specified".

DESCRIPTION OF OPERATION

82C54-2 functions are selected by control words from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operating mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	READ BACK COMMAND

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, the count value is set first. In next clock, loading is performed, then counting starts.) This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to 0000H during control word setting. The counter value (0000H) can't be read.

The program sequence of the 82C54-2 is flexible. Free sequence programming is possible as long as the two following rules are observed:

(i) Write the control word before writing the initial count value in each counter.

(ii) Write the initial count value according to the count value read/write format specified by the control word.

(Note) Unlike the 82C53-5, the 82C54-2 allows count value setting for another counter between LSB and MSB settings.

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- **Example of control word and count value setting**

Counter # 0: Read/Load LSB only, Mode 3, Binary count, count value 3H
Counter # 1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
Counter # 2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

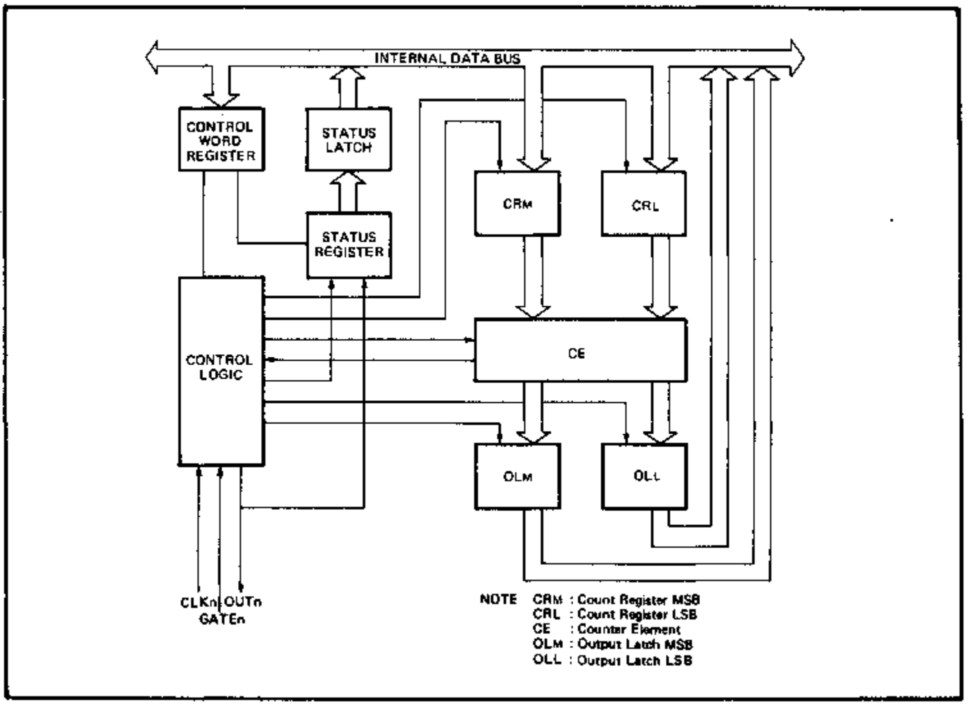
```
MVI A, 1EH ]  Counter #0 control word setting
OUT n3     ]
MVI A, 6AH ]  Counter #1 control word setting
OUT n3     ]
MVI A, B1H ]  Counter #2 control word setting
OUT n3     ]
MVI A, 03H ]  Counter #0 count value setting
OUT n0     ]
MVI A, AAH ]  Counter #1 count value setting
OUT n1     ]
MVI A, 34H ]
OUT n2     ]  Counter #2 count value setting
MVI A, 12H ]  (LSB then MSB)
OUT n2     ]
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min	Max	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	0	1 cannot be counted
4	1	0	
5	1	0	

INTERNAL BLOCK DIAGRAM OF A COUNTER



Mode definition

Mode 0

- Use: Event counter
- Output operation: The output is set to "L" level by the control word setting, and kept at "L" level until the counter value becomes 0.
- Gate function: "H" level validates the count operation, and "L" level invalidates it. The gate does not affect the output.
- Count value load timing: after the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. The first clock pulse does not cause the count value to be decremented. In other words, if the initial count value is N, the output is not set to "H" level until the input of (N+1) the clock pulse after the initial count value writing.
- Count value writing during counting:
  The count value is loaded in the CE at the falling edge of the next clock, and counting with the new count value continues. The operation for 2-byte count is as follows:
  1) The counting operation is suspended when the first byte is written. The output is immediately set to "L" level. (no clock pulse is required.)
  2) After the scond byte is written, the new count value is loaded to the CE at the falling edge of the next clock.
     For the output to go to "H" level again, N+1 clock pulses are necessary after new count value N is written.
- Count value writing when the gate signal is "L" level:
  The count value is also loaded to the CE at the falling edge of the next clock pulse in this case. When the gate signal is set to "H" level, the output is set to "H" level after the lapse of N clock pulses. Since the count value is already loaded in the CE, no clock pulse for loading in the CE is necessary.

Mode 1

- Use: Digital one-shot
- Output operation: The output is set to "H" level by the control word setting. It is set to "L" level at the falling edge of the clock succeeding the gate trigger, and kept at "L" level until the counter value becomes 0. Once the output is set to "H" level, it is kept at "H" level until the clock pulse succeeding the next trigger pulse.
- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the clock pulse succeeding the gate trigger and set the output to "L" level. The one-shot pulse starts in this way. If the initial count value is N, the one-shot pulse interval equals N clock pulses. The one-shot pulse is not repetitive.
- Gate function: The gate signal setting to "L" level after the gate trigger does not affect the output. When it is set to "H" level again from "L" level, gate retriggering occurs, the CR count value is loaded again, and counting continues.
- Count value writing during counting
  It does not affect the one-shot pulse being counted until retriggering occurs.

Mode 2

- Use: Rate generator, real-time interrupt clock.
- Output operation: The output is set to "H" level by control word setting. When the initial count value is decremented to 1, the output is set to "L" level during one clock pulse, and is then set to "H" level again. The initial count value is reloaded, and the above sequence repeats. In mode 2, the same sequence is repeated at intervals of N clock pulses if the initial count value is N for example.
- Gate function: "H" level validates counting, and "L" level invalidates it. If the gate signal is set to "L" level when the output pulse is "L" level, the output is immediately set to "H" level. At the falling edge of the clock pulse succeeding the trigger, the count value is reloaded and counting starts. The gate input can be used for counter synchronization in this way.
- Count value load timing:
  After the control word and initial count value is written, the count value is loaded to the CE at the falling edge of the next clock pulse. The output is set to "L" level upon lapse of N clock pulses after writing the initial count value N. Counter synchronization by software is possible in this way.
- Count value writing during counting:
  Count value writing does not affect the current counting operation sequence. If new count value writing completes and the gate trigger arrives before the end of current counting operation, the count value is loaded to the CE at the falling edge of the next clock pulse and counting continues from the new count value. If no gate trigger arrives, the new count value is loaded to the CE at the end of the current counting operation cycle. In mode 2, count value of 1 is prohibited.

Mode 3

- Use: Baud rate generator, square wave generator
- Output operation: Same as mode 2 except that the output duty is different.
  The output is set to "H" level by control word setting. When the count becomes half the initial count value, the output is set to "L" level and kept at "L" level during the remainder of the count.
  Mode 3 repeats the above sequence periodically. If the initial count value is N, the output becomes a square wave with a period of N.
- Gate operation: "H" level validates counting, and "L" level invalidates it. If the gate signal is set to "L" level when the output is "L" level, the output is immediately set to "H" level.
  The initial count value is reloaded at the falling edge of the clock pulse succeeding the next gate trigger. The gate can be used for counter synchronization in this way.

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- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. Counter synchronization by software is possible in this way.
- Count value writing during counting:
  The count value writing does not affect the current counting operation. When the gate trigger input arrives before the end of a half cycle of the square wave after writing the new count value, the new count value is loaded in the CE at the falling edge of the next clock pulse, and counting continues using the new count value. If there is no gate trigger, the new count value is loaded at the end of the half cycle and counting continues.
- Even number counting operation:
  The output is initially set to "H" level. The initial count value is loaded to the CE at the falling edge of the next clock pulse, and is decremented by 2 by consecutive clock pulses. When the counter value becomes 2, the output is set to "L" level, the initial value is reloaded and then the above operation is repeated.
- Odd number counting operation:
  The output is initially set to "H" level. At the falling edge of the next clock pulse, the initial count value minus one is loaded in the CE, and then the value is decremented by 2 by consecutive clock pulses. When the counter value becomes 0, the output is set to "L" level, and then the initial count value minus 1 is reloaded to the CE. The value is then decremented by 2 by consecutive clock pulses. When the counter value becomes 2, the output is again set to "H" level and the initial count value minus 1 is again reloaded. The above operations are repeated. In other words, the output is set to "H" level during (N+1)/2 counting and to "L" level during (N−1)/2 counting in the case of odd number counting.

Mode 4

- Use: Software trigger strobe
- Output operation: The output is initially set to "H" level. When the counter value becomes 0, the output goes to "L" level during one clock pulse, and then restores "H" level again.
  The count sequence starts when the initial count value is written.
- Gate function: "H" level validates counting, and "L" level invalidates counting. The gate signal does not affect the output.
- Count value load timing:
  After the control word and initial count value are written, the count value is loaded to the CE at the falling edge of the next clock pulse. The clock pulse does not decrement the initial count value. If the initial count value is N, the strobe is not output unless N+1 clock pulses are input after the initial count value is written.
- Count value writing during counting:
  The new count value is written to the CE at the falling edge of the next clock pulse, and counting continues using the new count value. The operation for 2-byte count is as follows:
  1) First byte writing does not affect the counting operation.
  2) After the second byte is written, the new count value is loaded to the CE at the falling edge of the next clock pulse.

  This means that the counting operation is retriggered by software. The output strobe is set to "L" level upon input of N+1 clock pulses after the new count value N is written.

Mode 5

- Use: Hardware trigger strobe
- Output operation: The output is initially set to "H" level. When the counter value becomes 0 after triggering by the rising edge of the gate pulse, the output goes to "L" level during one clock pulse, and then restores "H" level.
- Count value load timing:
  Even after the control word and initial count value are written, loading to the CE does not occur until the input of the clock pulse succeeding the trigger. For the clock pulse for CE loading, the count value is not decremented. If the initial count value is N, therefore, the output is not set to "L" level until N+1 clock pulses are input after triggering.
- Gate function:
  The initial count value is loaded to the CE at the falling edge of the clock pulse succeeding gate triggering. The count sequence can be retriggered. The gate pulse does not affect the output.
- Count value writing during counting:
  The count value writing does not affect the current counting sequence. If the gate trigger is generated after the new count value is written and before the current counting ends, the new count value is loaded to the CE at the falling edge of the next clock pulse, and counting continues using the new count value.

The various roles of the gate input signals in the above modes are summarized in the following table.

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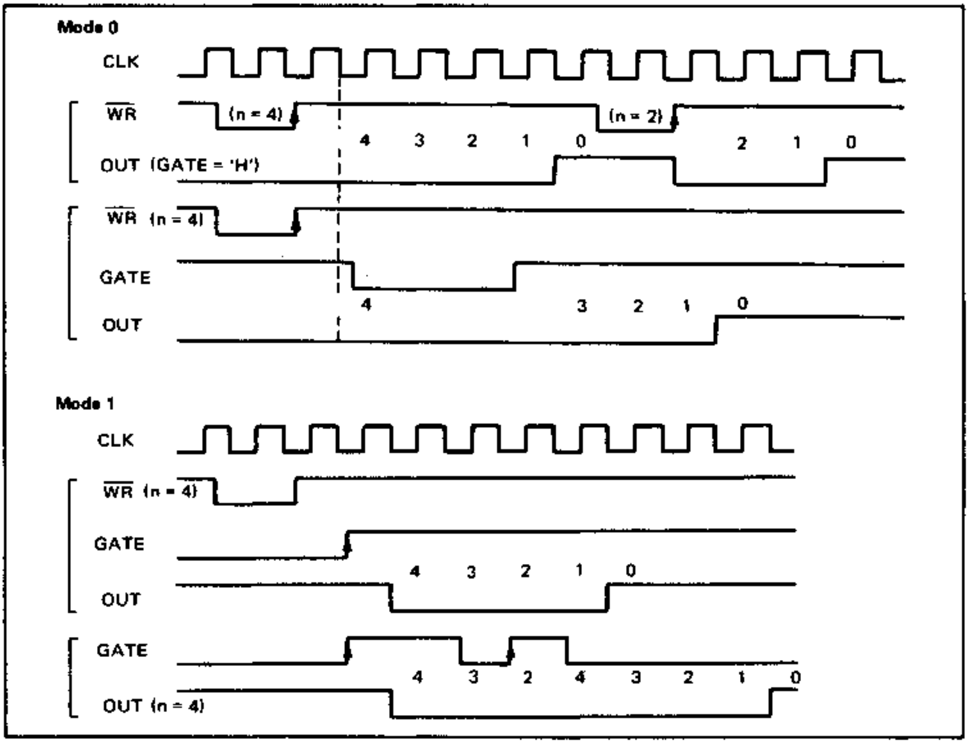
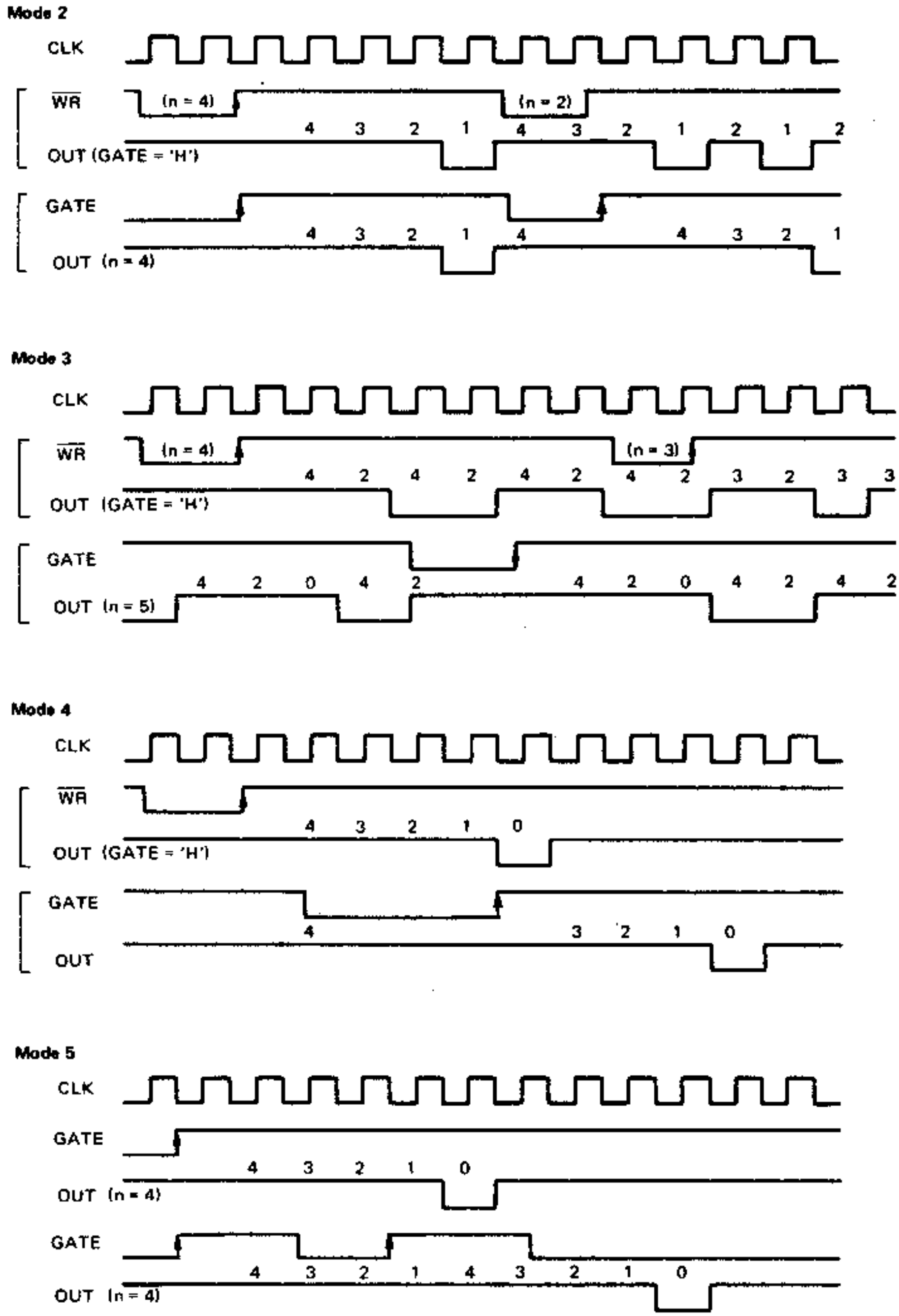
Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	





Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

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Reading Counter Values

All 82C54-2 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, (2) counter latching ("read on the fly"), and (3) read back command.

(1) **Direct reading**

Counter values can be read by direct reading operations.

Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

(2) **Counter latching**

In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. The output latch (OL) of the selected counter latches the count value when a counter latch command is written. The count value is held until it is read by the CPU or the control word is set again.

If a counter latch command is written again before reading while a certain counter is latched, the second counter latch command is ignored and the value latched by the first counter latch command is maintained.

The 82C54-2 features independent reading and writing from and to the same counter.

When a counter is programmed for the 2-byte counter value, the following sequence is possible:

1. Count value (LSB) reading
2. New count value (LSB) writing
3. Count value (MSB) reading
4. New count value (MSB) writing

An example of a counter latching program is given below.

Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  0 1 0 0 x x x x
           └── Denotes counter latching
OUT n3 ────┬── Write in control word address
           │   (n3)
           └── The counter value at this point
               is latched
IN n1 ─────┬── Reading of the LSB of the
           │   counter value latched from
           │   counter #1.
           └── n1: Counter #1 address
MOV B, A
IN n1   ────── Reading of MSB from counter
MOV C, A       #1.
```

(3) **Read Back Command Operation**

Use of the read back command enables the user to check the count value, program mode, output pin state and null count flag of the selected counter.

The command is written in the control word register, and the format is as shown below. For this command, the counter selection occurs according to bits D3, D2 and D1.

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT2	CNT1	CNT0	0

($\overline{CS}$ = 0, A0, A1 = 1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

D5: 0 = Selected counter latch operation
D4: 0 = Selected counter status latch operation
D3: 1 = Counter #2 selection
D2: 1 = Counter #1 selection
D1: 1 = Counter #0 selection
D0: 0 Fixed

It is possible to latch multiple counters by using the read back command. Latching of a read counter is automatically cancelled but other counters are kept latched. If multiple read back commands are written for the same counter, commands other than the first one are ignored.

It is also possible to latch the status information of each counter by using the read back command. The status of a certain counter is read when the counter is read.

The counter status format is as follows:

Bits D5 to D0 indicates the mode programmed by the most recently written control word.

Bit D7 indicates the status of the output pin.

Use of this bit makes it possible to monitor the counter output, so the corresponding hardware may be omitted.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RL1	RL0	M2	M1	M0	BCD

D7: 1 = Output pin status is 1.
0 = Output pin status is 0.
D6: 1 = Null count
0 = Count value reading is effective
D5 – D0: Programmed mode of counter (See the control word format.)

Null count indicates the count value finally written in the counter register (CR) has been loaded in the counter element (CE). The time when the count value was loaded in the CE depends on the mode of each counter, and it cannot be known by reading the counter value because the count value does not tell the new count value if the counter is latched.

The null count operation is shown below.

Operation	Result
A. Control word register writing	Null count = 1
B. Count register (CR) writing	Null count = 1
C. New count loading to CE (CR → CE)	Null count = 0

(Note) The null count operation for each counter is independent. When the 2-byte count is programmed, the null count is set to 1 when the count value of the second byte is written.

If status latching is carried out multiple times before status reading, other than the first status latch is ignored.

Simultaneous latching of the count and status of the selected counter is also possible. For this purpose, set bits D4 and D3, $\overline{\text{COUNT}}$ and $\overline{\text{STATUS}}$ bits, to 00. This is functionally the same as writing two separate read back commands at the same time. If counter/status latching is carried out multiple times before each reading, other than the first one is ignored here again. The example is shown below.

Command								Contents	Counter 0		Counter 1		Counter 2	
D7	D6	D5	D4	D3	D2	D1	D0		Count	Status	Count	Status	Count	Status
1	1	0	0	0	0	1	0	Read back status and count (counter 0)	L	L	–	–	–	–
1	1	1	0	0	1	0	0	Read back status (counter 1)	L	L	–	L	–	–
1	1	1	0	1	1	0	0	Read back status (counters 1 and 2)	L	L	–	L (NOTE)	–	L
1	1	0	1	1	0	0	0	Read back count (counter 2)	L	L	–	L	L	L
1	1	0	0	0	1	0	0	Read back status and count (counter 1)	L	L	L	L (NOTE)	L	L
1	1	1	0	0	0	1	0	Read back status (counter 0)	L	L (NOTE)	L	L	L	L

L: Latched, –: Not latched

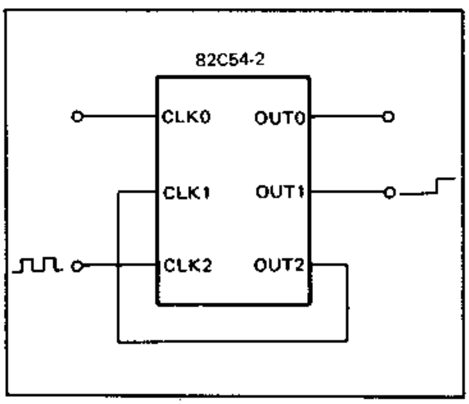
(Note) The latch command at this time point is ignored, and the first latch command is valid.

If both the count and status are latched, the status latched in the first counter read operation is read. The order of count latching and status latching is irrelevant.

The count(s) of the next one or two reading operations is or are read.

Example of Practical Application

- 82C54-2 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.

OKI semiconductor

MSM82C55A-5RS/GS
MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

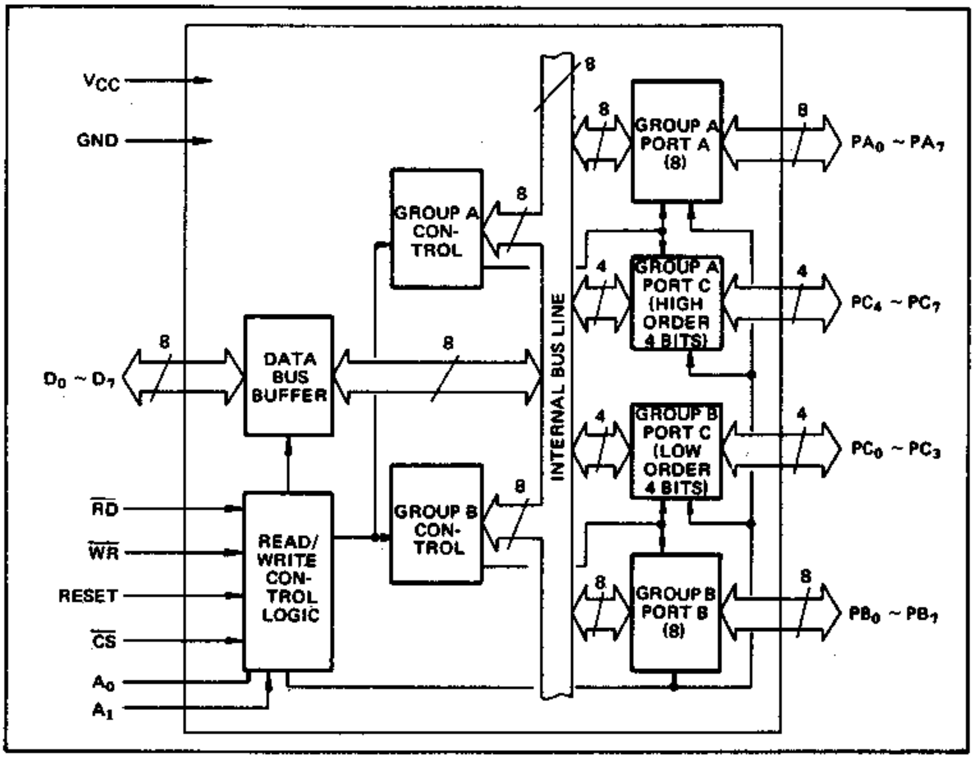
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- 40-pin DIP (MSM82C55A-5RS/MSM82C55A-2RS)
- 44-pin flat package (MSM82C55A-5GS/MSM82C55A-2GS)
- 44-pin PLCC (MSM82C55A-2JS)
- Compatible with 8255A-5

CIRCUIT CONFIGURATION



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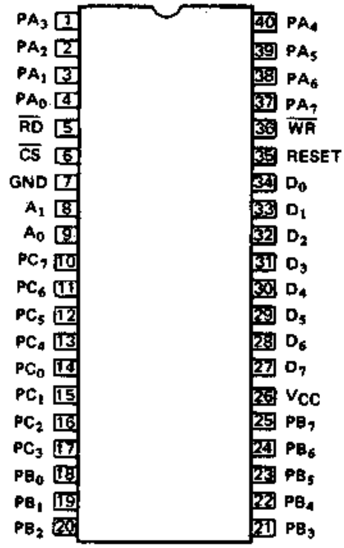
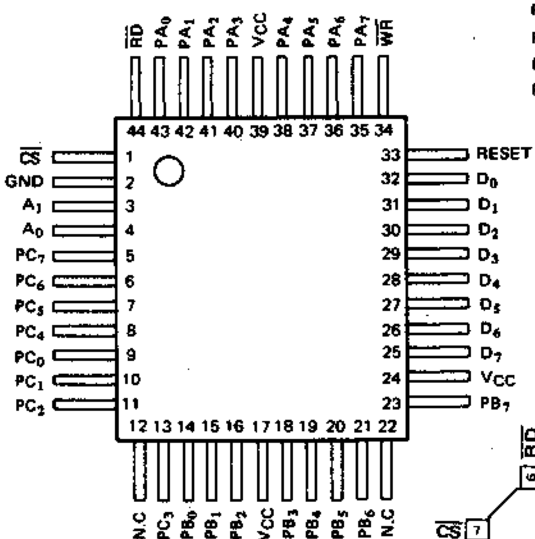
PIN CONFIGURATION

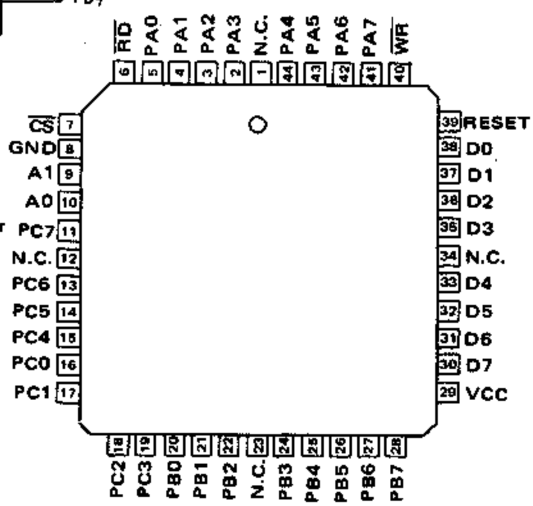
MSM82C55A-5RS (Top View)
MSM82C55A-2RS
40 Lead Plastic DIP





MSM82C55A-2GS
44 Lead Plastic Flat Package

MSM82C55A-2VJS (Top View)
44-pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-5RS MSM82C55A-2RS	MSM82C55A-5GS MSM82C55A-2GS	MSM82C55A-2JS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	–	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-5			MSM82C55A-2			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA				0.45			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −400 µA		2.4			—			V
		I_{OH} = −40 µA		4.2						V
		I_{OH} = −2.5 mA		–			3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)	−10		10	−1		1	µA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	−10		10	µA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ −0.2V $V_{IL} \leq 0.2V$			0.1	100		0.1	10	µA
Average Supply Current (active)	I_{CC}	I/O write cycle 82C55A-5 .... 3MHzCPU timing 82C55A-2 ... 8MHzCPU timing				5			8	mA

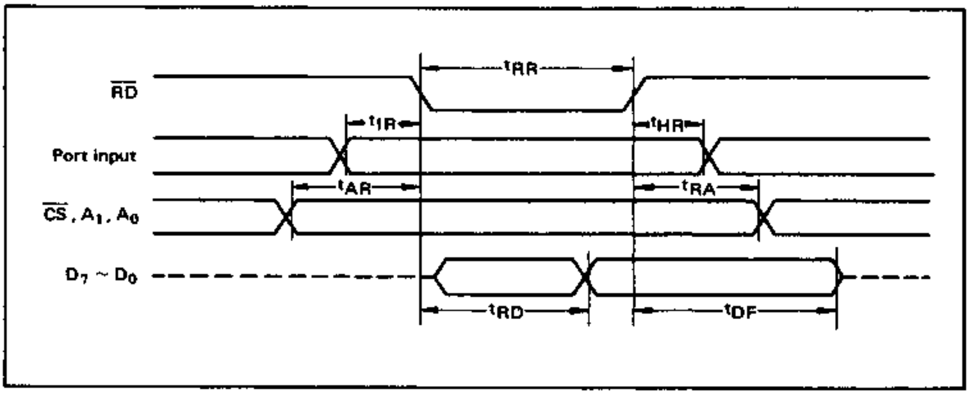
AC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

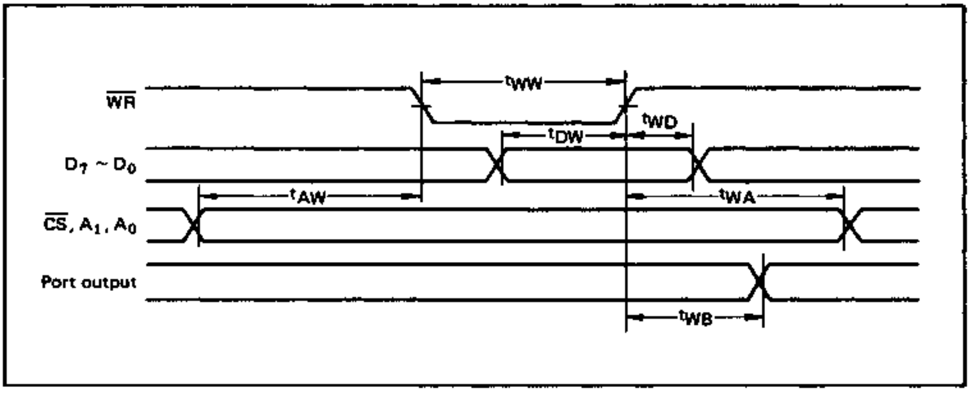
Parameter	Symbol	MSM82C55A-5		MSM82C55A-2		Unit	Remarks
		Min.	Max.	Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		20		ns	
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	20		0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	300		100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		200		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	100	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	850		200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	30		20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	300		150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	100		50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	40		30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		350		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	20		10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	300		100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	300		100		ns	Load 150 pF
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	180		50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		300		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		650		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		350		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		300		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		300		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		400		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		300		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		350		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		850		250	ns	

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

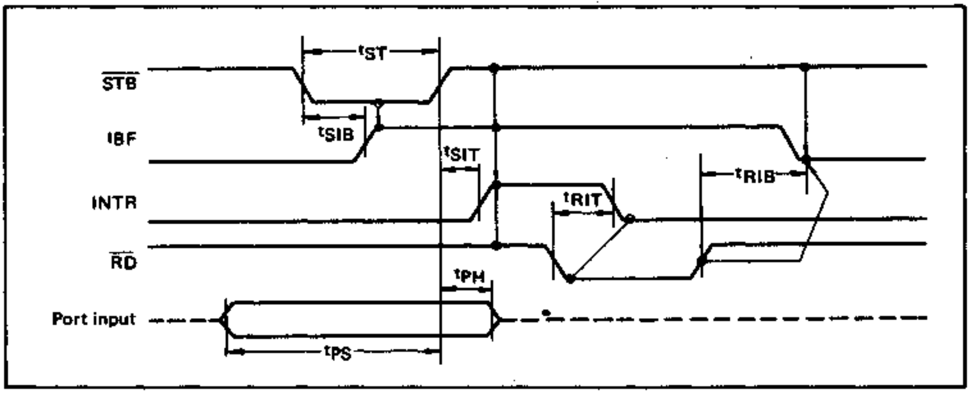
Basic Input Operation (Mode 0)



Basic Output Operation (Mode 0)



Strobe Input Operation (Mode 1)



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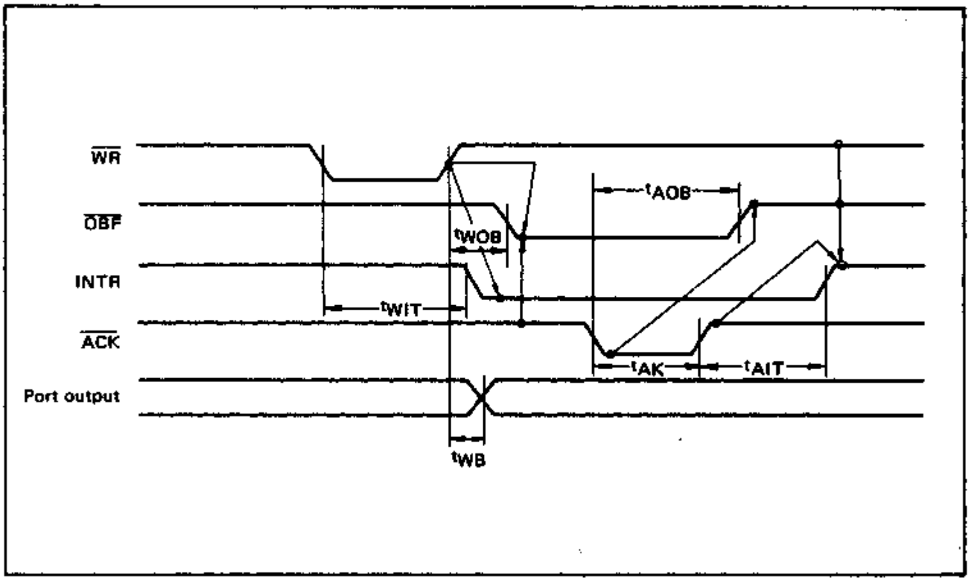
Strobe Output Operation (Mode 1)



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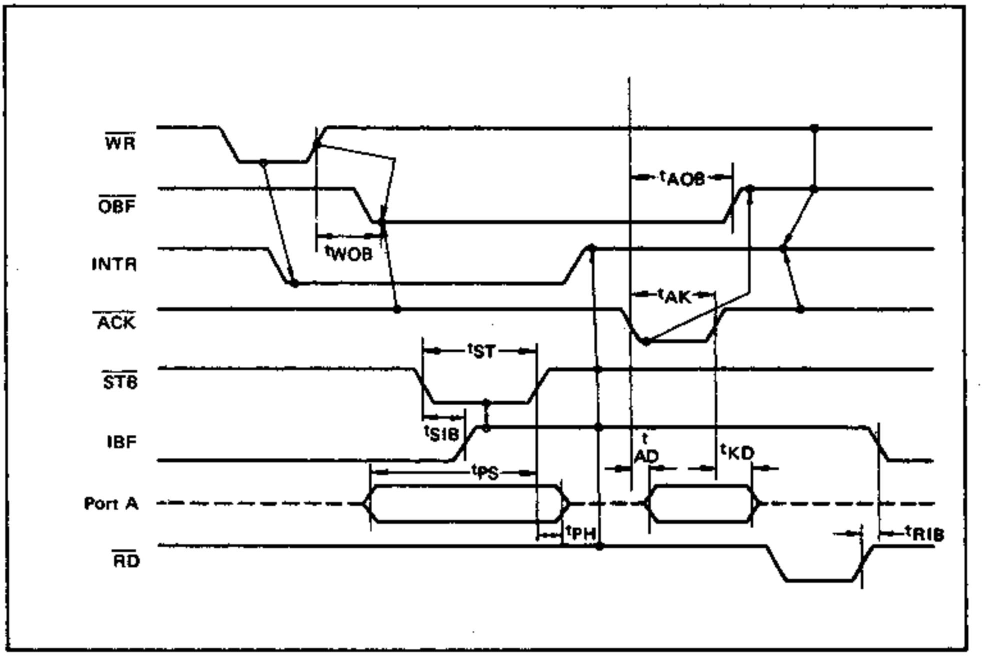
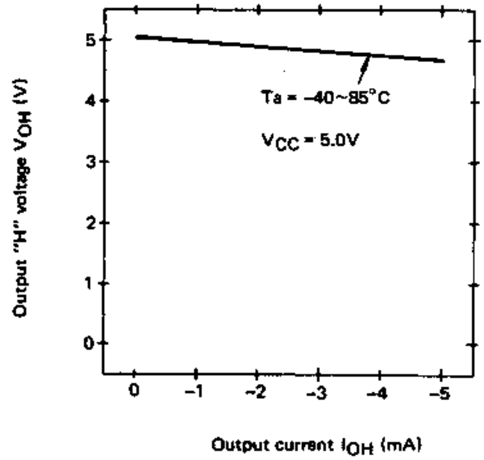
Bidirectional Bus Operation (Mode 2)

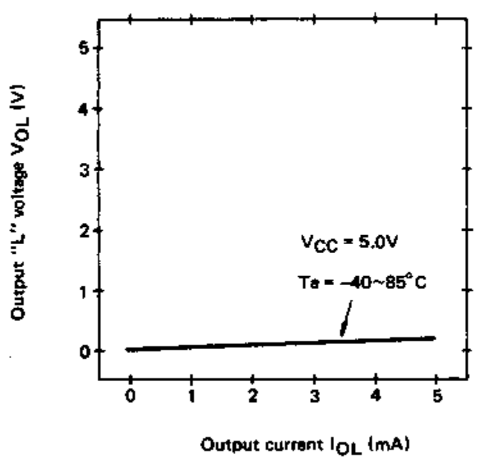


OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

5

FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status).
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

OPERATIONAL DESCRIPTION

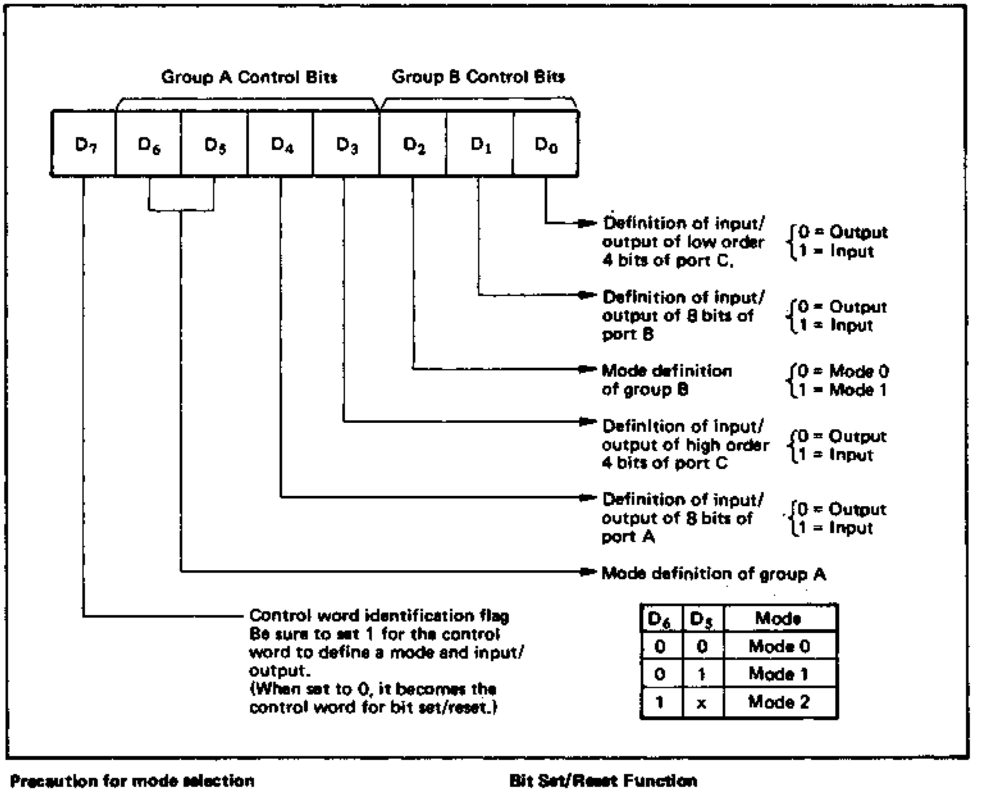
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



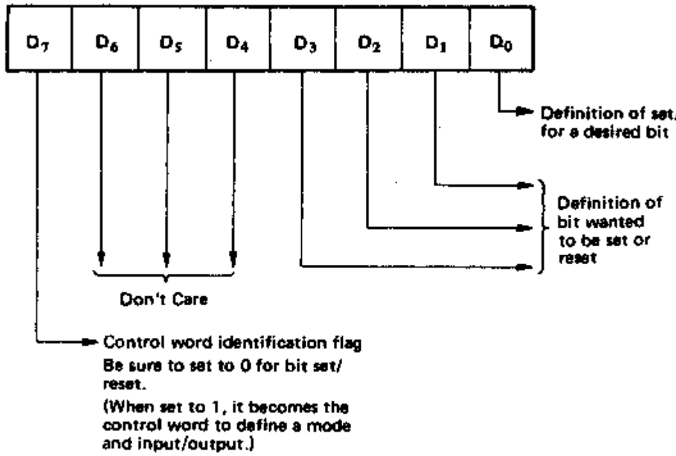
D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.



Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input) .

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

$INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

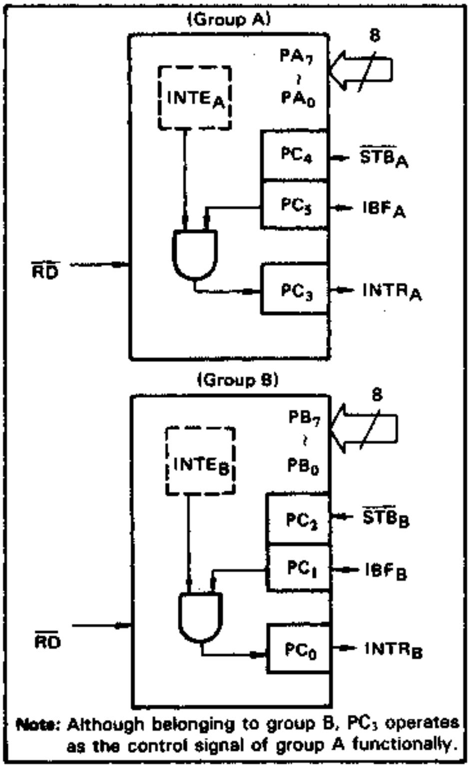
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

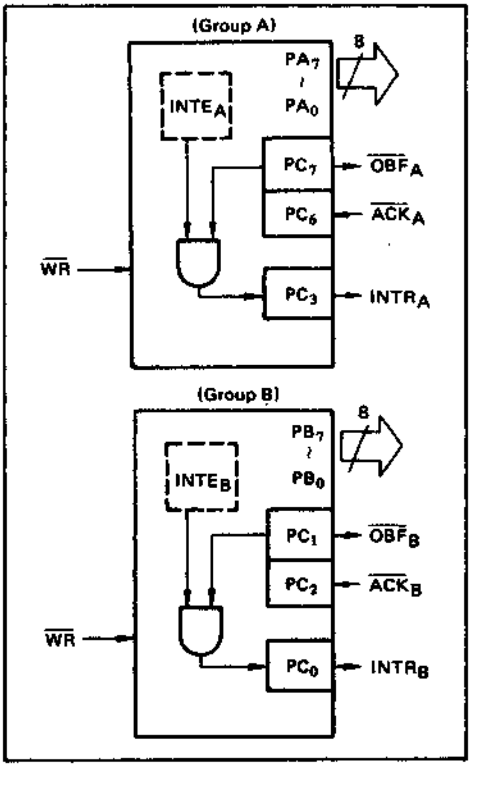
$INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output



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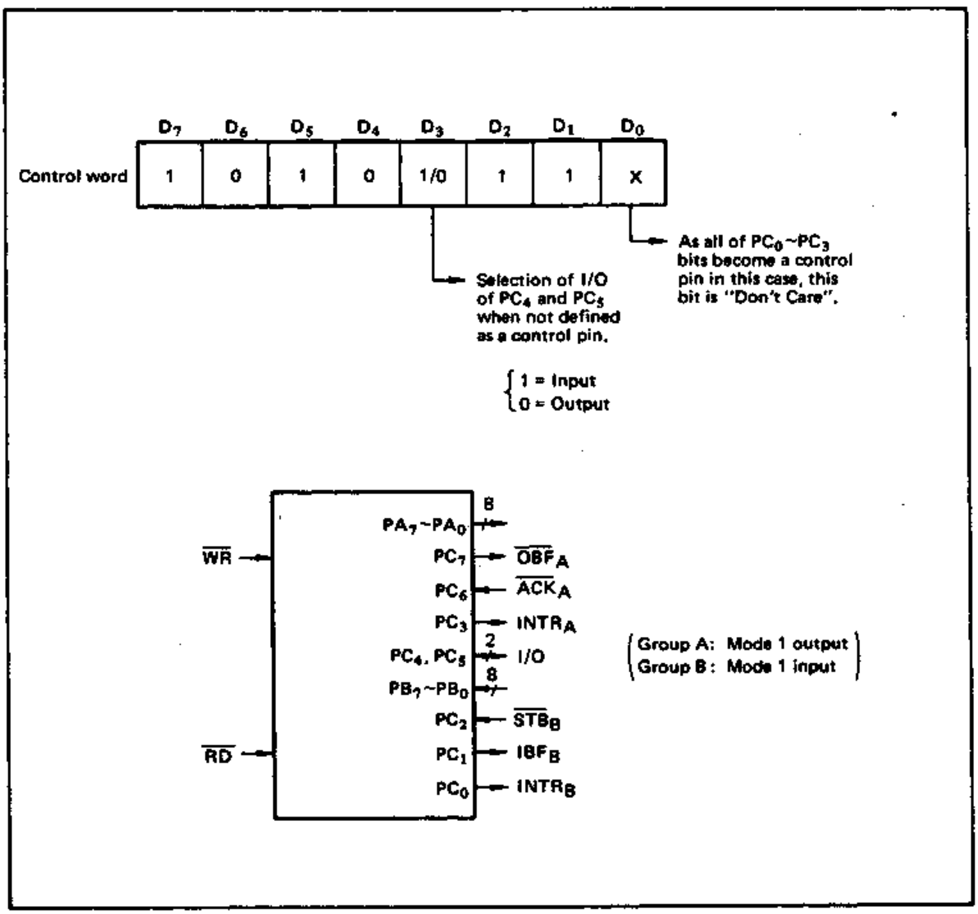
Port C Function Allocation in Mode 1

Port C \ Combination of Input/Output	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:

(a) When group A is mode 1 output and group B is mode 1 input.

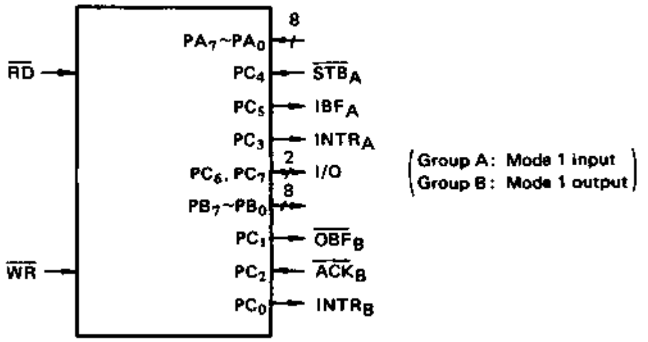


(b) When group A is mode 1 input and group B is mode 1 output.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	1/0	1	0	X

D_3 → Selection of I/O of PC6 and PC7 when not defined as a control pin

{1 = Input
{0 = Output



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

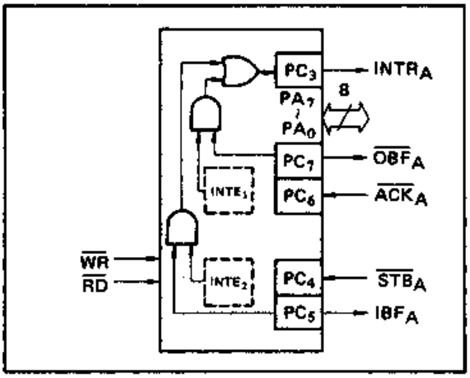
IBF (Input buffer full flag output)

- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

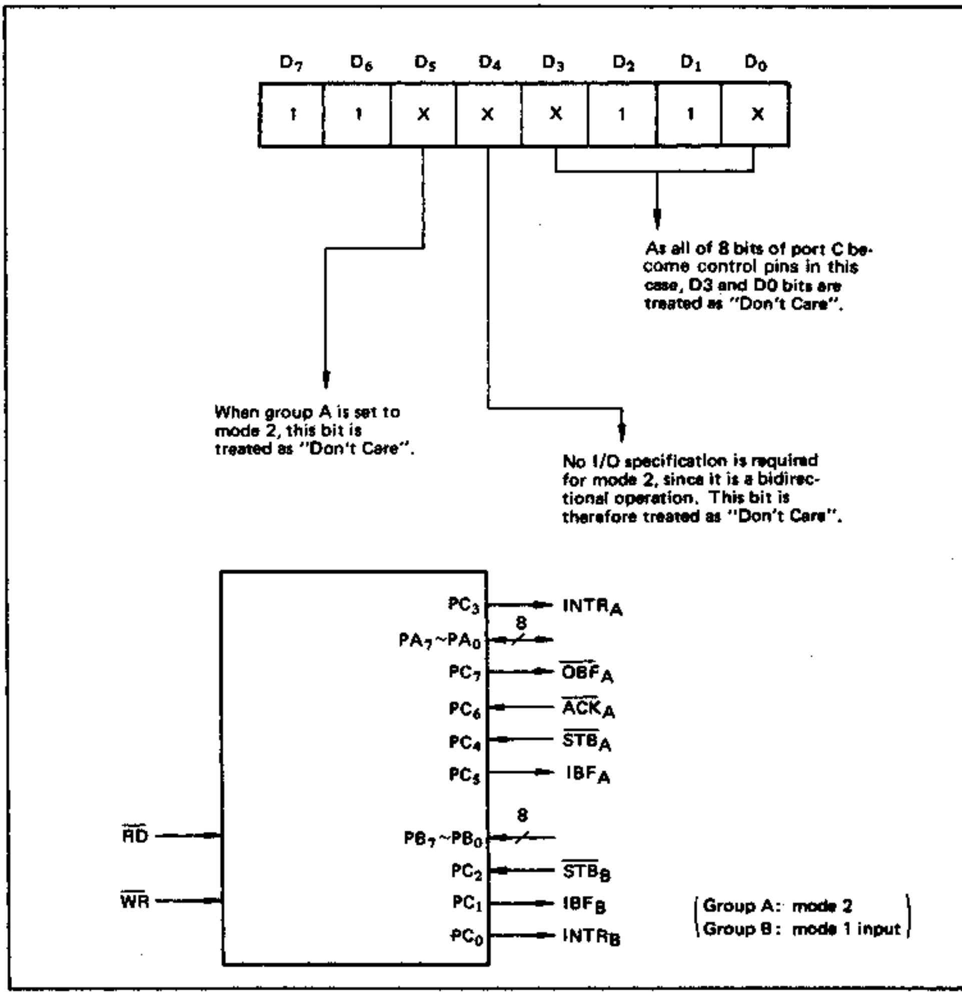
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



4. When Group A is Different in Mode from Group B
Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O

(PC_7–PC_4): Controlled at the 3rd bit (D3) of the control word
(PC_3–PC_0): Controlled at the 0th bit (D0) of the control word

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.

The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

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6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note:

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

OKI semiconductor

MSM82C59A-2RS/GS/JS

PROGRAMMABLE INTERRUPT CONTROLER

GENERAL DESCRIPTION

The MSM82C59A-2 is a programmable interrupt controller for use in MSM80C85A/A-2 and MSM80C86/88 microcomputer systems.

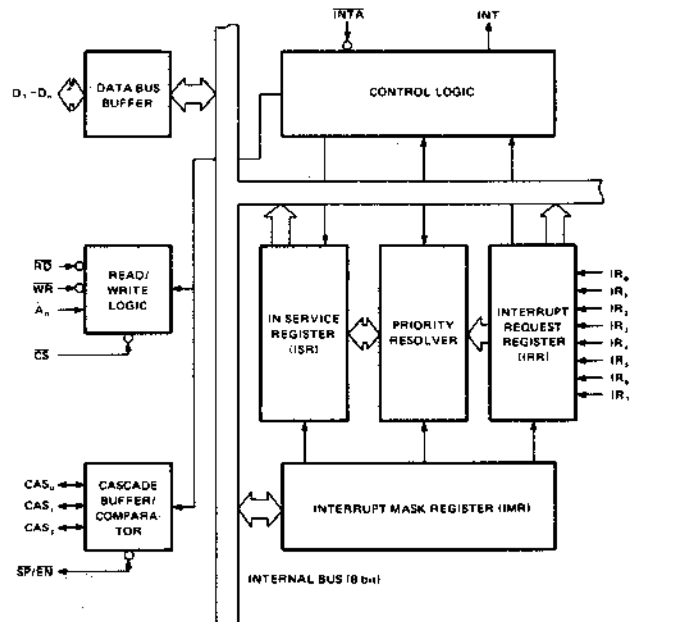
Based on CMOS silicon gate technology, this device features an extremely low standby current of 100 μA (max.) in chip non-selective status. During interrupt control status, the power consumption is very low with only 5 mA (max.) being required.

Internally, the MSM82C59A-2 can control priority interrupts up to 8 levels, and can be expanded up to 64 levels by cascade connection of a number of devices.

FEATURES

- Silicon gate CMOS technology for high speed and low power consumption.
- 3 V to 6 V single power supply
- 80C85A system compatibility (MAX5MHz)
- 80C86/88 system compatibility (MAX8MHz)
- 8-level priority interrupt control
- Interrupt levels expandable up to 64 levels
- Programmable interrupt mode
- Maskable interrupt
- Automatically generated CALL code (85 mode)
- TTL compatible
- 28-pin plastic DIP (MSM82C59A-2RS)
- 32-pin plastic flat package (MSM82C59A-2GS)
- 28-pin PLCC Package (MSM82C59A-2JS)

CIRCUIT CONFIGURATION



MSM82C59A-2 Internal block diagram

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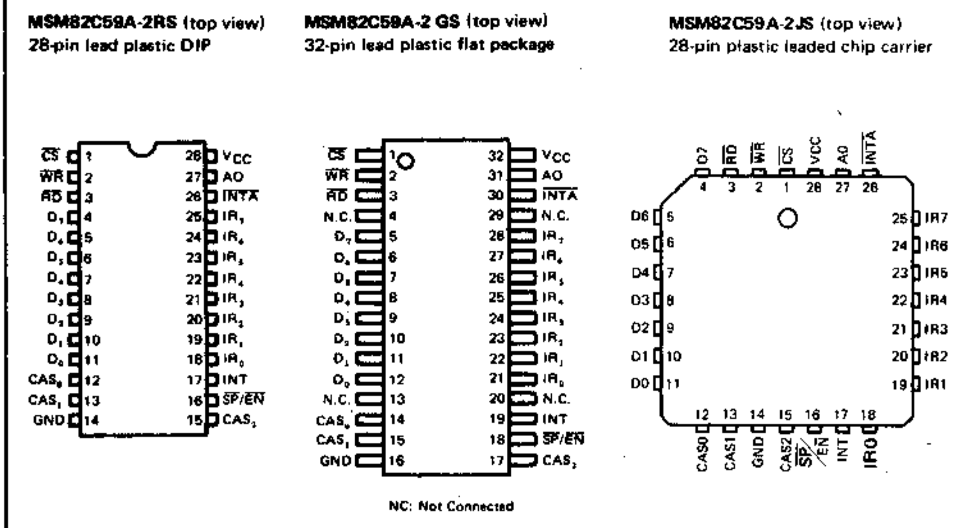
PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C59A-2RS	MSM82C59A-2GS	MSM82C59A-2JS	
Power supply voltage	V_{CC}	Respect to GND	−0.5 ~ +7			V
Input voltage	V_{IN}	Respect to GND	−0.5 ~ V_{CC} + 0.5			V
Output voltage	V_{OUT}	Respect to GND	−0.5 ~ V_{CC} + 0.5			V
Storage temperature	T_{stg}	—	−55 ~ +150			°C
Power dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

Operating Ranges

Parameter	Symbol	Range	Unit
Power supply voltage	V_{CC}	3 ~ 6	V
Operating temperature	T_{OP}	-40 ~ +85	°C

Recommended Operating Conditions

Parameter	Symbol	Max.	Typ.	Min.	Unit
Power supply voltage	V_{CC}	4.5	5	5.5	V
Operating temperature	Top	-40	+25	+85	°C
"L" level input voltage	V_{IL}	-0.5		+0.8	V
"H" level input voltage	V_{IH}	2.2		V_{CC} +0.5	V

DC Characteristics

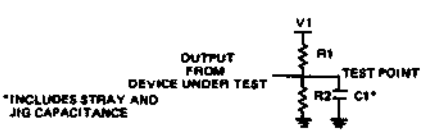
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" level output voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC}=4.5V~5.5V Ta=-40°C~+85°C			0.4	V
"H" level output voltage	V_{OH}	I_{OH} = -2.5 mA		3.0			V
		I_{OH} = -100 μA		V_{CC} − 0.4			
Input leak current	I_{LI}	$0V \leq V_{IN} \leq V_{CC}$		-1		1	μA
IR input leak current	I_{LIR}			-300		10	μA
Output leak current	I_{LO}	$0V \leq V_{OUT} \leq V_{CC}$		-10		10	μA
Standby power supply current	I_{CCS}	$\overline{CS}$=V_{CC}, IR = V_{CC} V_{IL}=0V, V_{IH}=V_{CC}			0.1	100	μA
Average operation power supply current	I_{CC}	V_{IN}=0V/V_{CC} C_L = 0 pF				5	mA

AC Characteristics

Ta = -40°C ~ +85°C, V_{CC} = 5V ±10%

Parameter	Symbol	Min.	Max.	Unit	TEST	Conditions
Address setup time (to $\overline{RD}$)	TAHRL	10		nS		Read $\overline{INTA}$ timing
Address hold time (after $\overline{RD}$)	TRHAX	5		nS		
$\overline{RD}$/$\overline{INTA}$ pulse width	TRLRH	160		nS		
Address setup time (to $\overline{WR}$)	TAHWL	0		nS		Write timing
Address hold time (after $\overline{WR}$)	TWHAX	0		nS		
$\overline{WR}$ pulse width	TWLWH	190		nS		
Data setup time (to $\overline{WR}$)	TDVWH	160		nS		
Data hold time (after $\overline{WR}$)	TWHDX	0		nS		
IR input width (Low)	TJLJH	100		nS		$\overline{INTA}$ sequence
CAS input setup time (to $\overline{INTA}$) (slave)	TCVIAL	40		nS		
End of $\overline{RD}$ to Next $\overline{RD}$ End of $\overline{INTA}$ to Next $\overline{INTA}$	TRHRL	160		nS		Other timing
End of $\overline{WR}$ to Next $\overline{WR}$	TWHWL	190		nS		
End of Command to Next command	TCHCL	400		nS		
Data valid following $\overline{RD}$/$\overline{INTA}$	TRLDV		120	nS	1	Delay times
Data floating following $\overline{RD}$/$\overline{INTA}$	TRHDZ	10	85	nS	2	
INT output delay time	TJHIH		300	nS	1	
CAS valid following 1st. $\overline{INTA}$ (master)	TIALCV		360	nS	1	
$\overline{EN}$ active following $\overline{RD}$/$\overline{INTA}$	TRLEL		100	nS	1	
$\overline{EN}$ inactive following $\overline{RD}$/$\overline{INTA}$	TRHEH		150	nS	1	
Data valid after address	TAHDV		200	nS	1	
Data valid after CAS	TCVDV		200	nS	1	

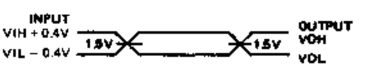
AC TEST CIRCUITS



TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8KΩ	1.8KΩ	30 pf

TEST CONDITION DEFINITION TABLE

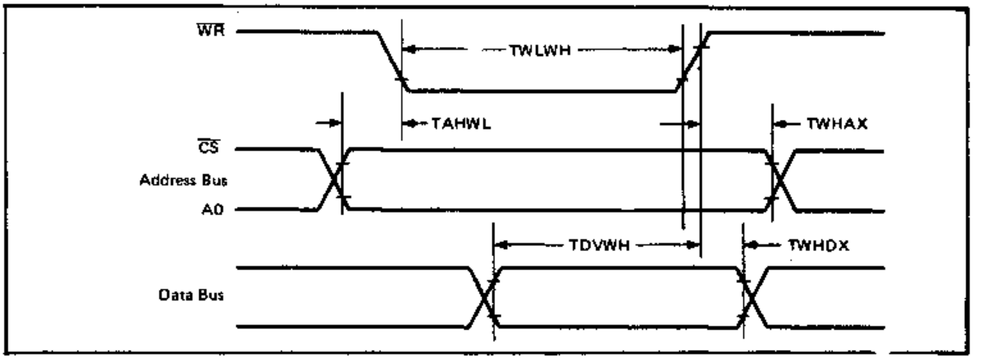
A.C. TESTING INPUT, OUTPUT WAVEFORM



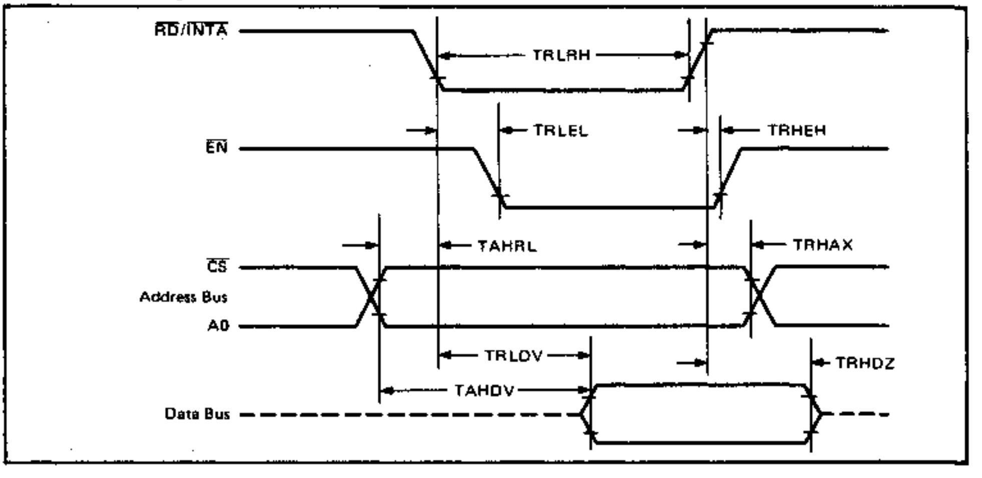
A.C. Testing: All input signals must switch between VIL−0.4V and VIH+0.4V. T_R and T_F must be less then or equal to 15 ns.

TIME CHART

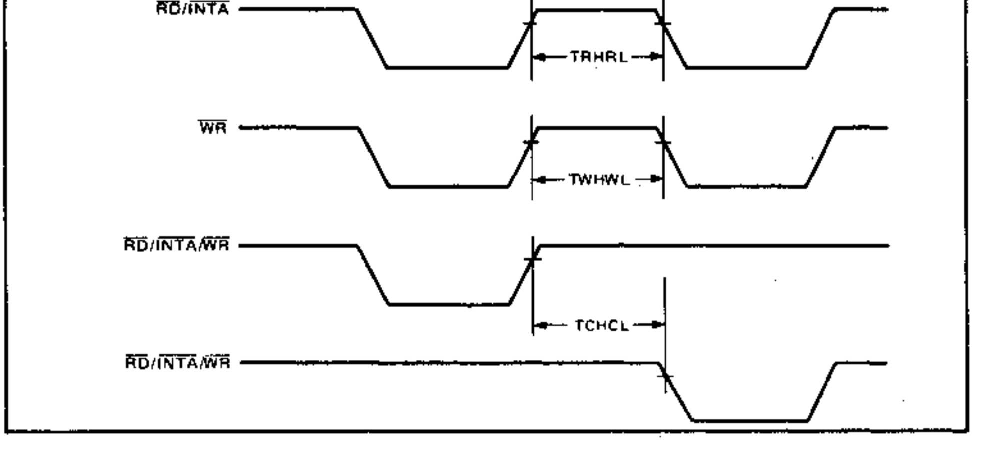
Write Timing



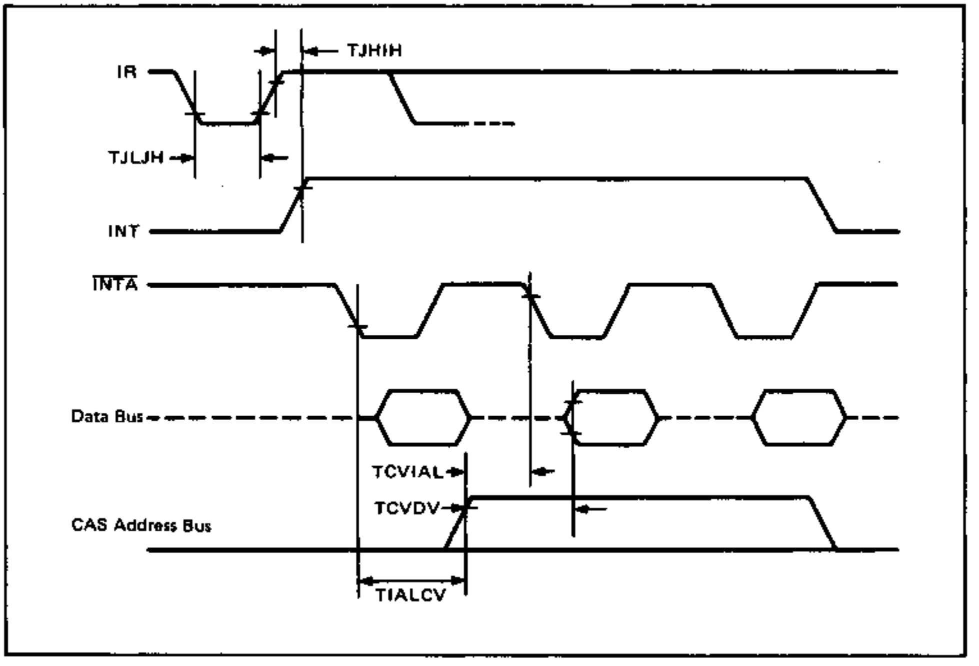
Read/INTA Timing



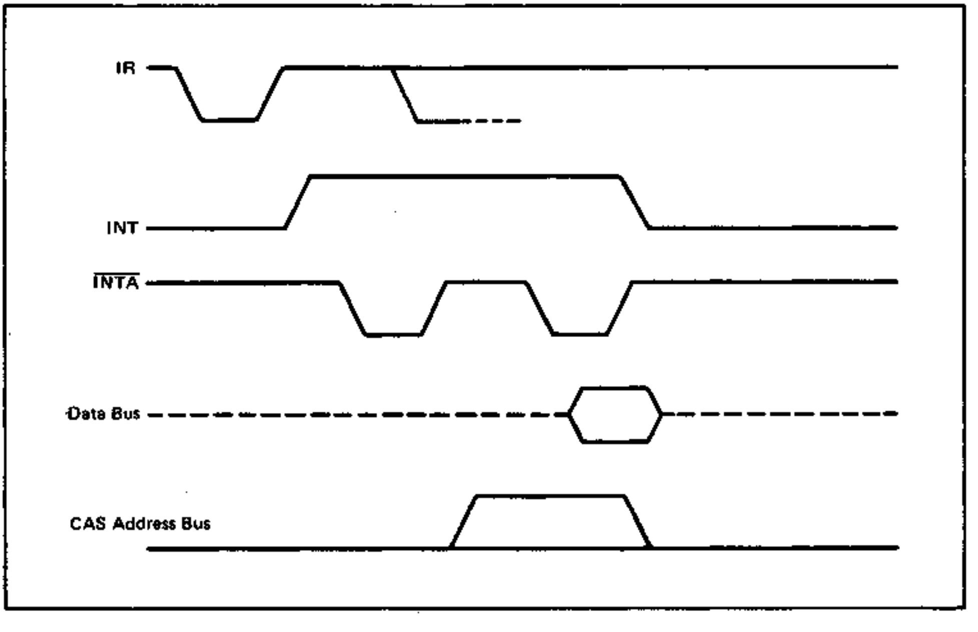
Other Timing



$\overline{\text{INTA}}$ Sequence (85 mode)



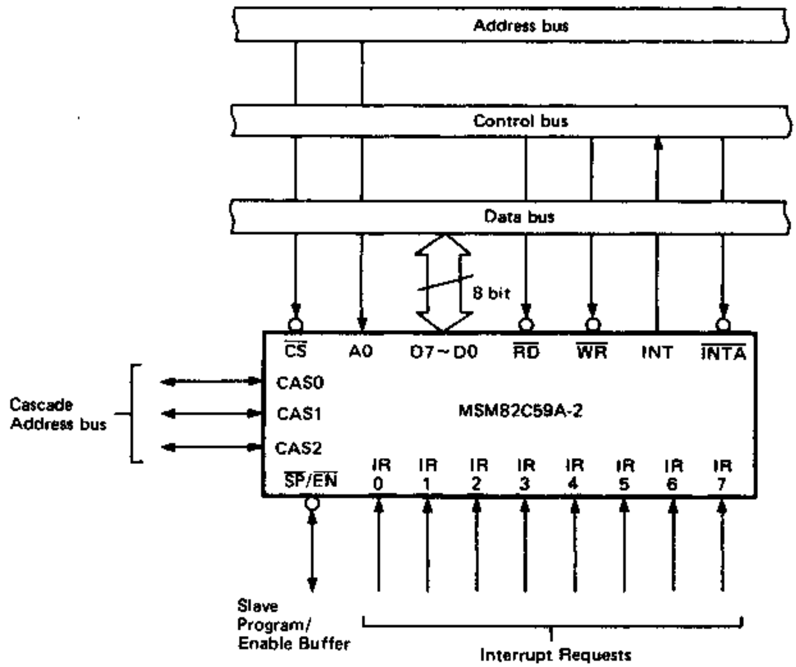
$\overline{\text{INTA}}$ Sequence (86 mode)



PIN FUNCTION DESCRIPTION

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	This 3-state 8-bit bidirectional data bus is used in reading status registers and writing command words through the $\overline{RD}/\overline{WR}$ signal from the CPU, and also in reading the CALL instruction code by the $\overline{INTA}$ signal from the CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled by $\overline{RD}/\overline{WR}$ when this pin is at low level. The data bus (D0 thru D7) is switched to high impedance when the pin is at high level. Note that $\overline{CS}$ does not effect $\overline{INTA}$.
$\overline{RD}$	Read input	Input	Data is transferred from the 82C59A to the CPU when this pin is at low level. IRR (Interrupt Request Register), ISR (In-Service Register), IMR (Interrupt Mask Register), or a Poll word is selected by OCW3 and A0.
$\overline{WR}$	Write input	Input	Commands are transferred from the CPU to the 82C59A when this pin is at low level.
A0	Address input	Input	This pin is used together with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ signals to write commands in the command registers, and to select and read status registers. This is normally connected to the least significant bit of the address bus. (A0 for 80C85A, and A1 for 80C86/88).
CAS0 ~ 2	Cascade address	Input/output	These pins are outputs when the 82C59A is used as the master, and inputs when used as a slave (in cascade mode). These pins are outputs when in single mode.
$\overline{SP}/\overline{EN}$	Slave program input/enable buffer output	Input/output	This dual function pin is used as an output to enable the data bus buffer in Buffered mode, and as an input for deciding whether the 82C59A is to be master ($\overline{SP}/\overline{EN}$ = 1) or a slave ($\overline{SP}/\overline{EN}$ = 0) during Non-buffered mode.
INT	Interrupt output	Output	When an interrupt request is made to the 82C59A, the INT output is switched to high level, and INT interrupt is sent to the CPU.
$\overline{INTA}$	Interrupt acknowledge input	Input	When this pin is at low level, the CALL instruction code or the interrupt vector data is enabled onto the data bus. When the CPU acknowledges the INT Interrupt, $\overline{INTA}$ is sent to the 82C59A. (Interrupt acknowledge sequence).
IR0 ~ 7	Interrupt request input	Input	These interrupt request input pins for the 82C59A can be set to edge trigger mode or level trigger mode (by ICW1). In edge trigger mode, interrupt request is executed by the rising edge of the IR input and holds it until that input is acknowledged by the CPU. In level trigger mode, interrupt requests are executed by high level IR inputs and holds them until that input is acknowledged by the CPU. These pins have a pull up resistor.

SYSTEM INTERFACE



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BASIC OPERATION DESCRIPTION

Data transfers between the 82C59A internal registers and the data bus are listed below.

A0	D4	D3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function	Operation
0	X	X	0	1	0	IRR, ISR, or Poll word → Data bus	Read
1	X	X	0	1	0	IMR → Data bus	Read
0	0	0	1	0	0	Data bus → OCW2	Write
0	0	1	1	0	0	Data bus → OCW3	Write
0	1	X	1	0	0	Data bus → ICWI	Write
1	X	X	1	0	0	Data bus → OCW1, ICW2, ICW3, ICW4	Write
X	X	X	1	1	0	Data bus set to high impedance (when $\overline{INTA}$ = 1)	–
X	X	X	X	X	1		
X	X	X	0	0	X	Combinations prohibited	–

OPERATION DESCRIPTION

The 82C59A has been designed for real time interrupt driven microcomputer systems. The 82C59A is capable of handling up to 8 levels of interrupt requests, and can be expanded to cover a maximum of 64 levels when connected to other 82C59A devices.

Programming involves the use of system software in the same way as other microcomputer peripheral I/O devices. Selection of priority mode involves program execution, and enables the method of requesting interrupts to be processed by the 82C59A to be suitably configured for system requirements. That is, the priority mode can be dynamically updated or reconfigured during the main program at any time. A complete interrupt structure can be defined as required, based on the entire system environment.

(1) Functional Description of Each Block

Block name	Description of function
IRR, ISR	IR input line interrupts are processed by a cascaded interrupt request register (IRR) and the in-service register (ISR). The IRR stores all request levels where interrupt service is requested, and the ISR stores all interrupt levels being serviced.
Priority resolver	This logic block determines the priority level of the bits set in the IRR. The highest priority level is selected, and the corresponding ISR bit is set during $\overline{INTA}$ pulses.
Read/write logic	This block is capable of receiving commands from the CPU. These command words (ICW) and the operation command words (OCW) store the various control formats for 82C59A operations. This block is also used to transfer the status of the 82C59A to the Data Bus.
Cascade buffer comparator	This functional block is involved in the output and comparison of all 82C59A IDs used in the system. These three I/O pins (CAS0 thru CAS2) are outputs when the 82C59A operates as a master, and inputs when it operates as a slave. When operating as a master, the 82C59A sends a slave ID output to the slave where an interrupt has been applied. Furthermore, the selected slave sends the preprogrammed subroutine address onto the data bus during next one or two $\overline{INTA}$ pulses from the CPU.

(2) Interrupt Sequence

The major features of the 82C59A used in microcomputer systems are the programmability and the addressing capability of interrupt routines. This latter feature enables direct or indirect jumping to specific interrupt routines without polling the interrupt devices. The operational sequence during an interrupt varies for different CPUs.

The procedure for the 85 system (8085A/80C85A) is outlined below.

(i) One or more interrupt requests (IR0 thru IR7) becomes high, and the corresponding IRR bit is set.

(ii) The 82C59A evaluates these requests, and sends an INT signal to the CPU if the request is judged to be suitable.

(iii) The CPU issues an $\overline{INTA}$ output pulse upon reception of the INT signal.

(iv) Upon reception of the $\overline{INTA}$ signal from the CPU, the 82C59A releases the CALL instruction code (11001101) to the 8-bit data bus.

(v) A further two $\overline{INTA}$ pulses are then sent to the 82C59A from the CPU by this CALL instruction.

(vi) These two $\overline{INTA}$ pulses result in a preprogrammed subroutine address being sent from the 82C59A to the data bus. The lower 8-bit address is released by the first $\overline{INTA}$ pulse, and the higher 8-bit address is released by the second pulse.
The Falling Edge of the second $\overline{INTA}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.

(vii) 3-byte CALL instructions are thus released by the 82C59A. In Automatic End Of Interrupt (AEOI) mode, the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. In other cases, the ISR bit remains set until reception of a suitable EOI command at the end of the interrupt routine.

The procedure for the 86 system (80C86/88) is identical to the first three steps of the 85 system. The subsequent steps are described below.

(iv) Upon reception of the $\overline{INTA}$ signal from the CPU, the ISR bit with the highest priority is set, and the corresponding IRR bit is reset. In this cycle, the 82C59A sets the data bus to high impedance without driving the Data Bus.

(v) The CPU generates a second $\overline{INTA}$ output pulse, resulting in an 8-bit pointer to the data bus by the 82C59A.
The Falling Edge of the $\overline{INTA}$ signal sets the ISR bit with the highest priority, and the Rising Edge of it resets the IRR bit.

(vi) This completes the interrupt cycle. In AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. In other cases, the ISR bit remains set until reception of a suitable EOI command at the end of the interrupt routine.

If the interrupt request is cancelled prior to step (iv), that is, before the first $\overline{INTA}$ pulse has been received, the 82C59A operates as if a level 7 interrupt has been received, and the vector byte and CAS line operate as if a level 7 interrupt has been requested.

(3) Interrupt Sequence Output

85 Mode (80C85A)

The sequence in this case consists of three $\overline{INTA}$ pulses. A CALL operation code is released to the data bus by the first $\overline{INTA}$ pulse.

Contents of the first interrupt vector byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL code	1	1	0	0	1	1	0	1

The lower address of the interrupt service routine is released to the data bus by the second $\overline{INTA}$ pulse. If A5 ~ A7 is programmed with an address interval of 4, A0 ~ A4, is automatically inserted. And if A6 and A7 are programmed at an address interval of 8, A0 ~ A5 is automatically inserted.

Contents of the second interrupt vector byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

The higher address of the interrupt service routine programmed by the second byte (A8 ~ A15) of the initialization sequence is released to the data bus.

Contents of the third interrupt vector byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

86 Mode (80C86/88)

Apart from the two interrupt acknowledge cycles and the absence of a CALL operation code, the 86 mode is the same as the 85 mode. The first $\overline{INTA}$ cycle freezes interrupt status to resolve the priority internally in the same way as in 85 mode. When the device is used as a master, an interrupt code is issued to the cascade line at the end of the $\overline{INTA}$ pulse. During this first cycle, the data bus buffer is kept at high impedance without any data to the CPU. During the second $\overline{INTA}$ cycle, the 82C59A sends a byte of interrupt code to the CPU. Note that in 86 mode, the Address Interval (ADI) control status is ignored and A5 ~ A10 is not used.

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Contents of interrupt vector byte in 86 system mode

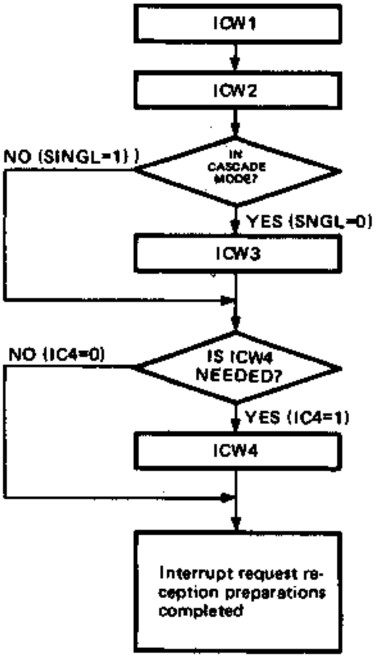
	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

(4) Programming the 82C59A

The 82C59A receives two types of command words generaed by the CPU.

(i) Initialization Command Words (ICW1 thru ICW4)

Before commencing normal operations, each 82C59A in the system must be initialized by two to four $\overline{WR}$ pulse sequence.



Initialization sequence

(ii) Operation Command Words (OCW1 thru OCW3)

These commands are used in operating the 82C59A in the following modes.

a. Fully Nested Mode
b. Rotating Priority Mode
c. Special Mask Mode
d. Polled Mode

The OCW can be written into the 82C59A any time after initialization has been completed.

(5) Initialization Command Words (ICW1 thru ICW4)

When a command is issued with D4 = 1 and A0 = 0, it is always regarded as an Initialization Command Word 1 (ICW1). Starting of the initialization sequence by ICW1 results in automatic execution of the following steps.

a. The edge sense circuit is reset, and a low to high transition is necessary to generate an interrupt.
b. The interrupt mask register is cleared.
c. The IR7 input is assigned priority 7 (lowest priority)
d. Slave mode address is set to 7.
e. The Special Mask Mode is cleared, and the Status Read is set to IRR.
f. All ICW4 functions are cleared if IC4 = 0, resulting in a change to Non-Buffered mode, no-Auto EOI, and 85 mode.

Note: Master/slave in ICW4 can only be used in buffered mode.

(i) Initialization Command Words 1 and 2 (ICW1 and ICW2)

A4 thru A15: (Starting address of interrupt service routines)

In 85 mode, 8 request levels CALL 8 locations at equivalent intervals in the memory. The memory location interval can be set at this stage to 4 or 8 by program. (→ ADI) Hence, either 32 or 64 bytes/page respectively are used in the 8 routines.

The address format is 2 bytes long (A0 thru A15). When the routine interval is 4, A0 thru A4 is inserted automatically by the 82C59A, and A5 thru A15 is programmed externally. When the interval is 8, on the other hand, A0 thru A5 are inserted automatically by the 82C59A, and A6 thru A15 are programmed externally. In 86 mode, T3 thru T7 are inserted in the 5 most significant bits of the vector type, and the 82C59A sets the 3 least significant bits according to the interrupt level. A0 thru A10 are ignored, and the ADI (address interval) has no effect.

LTIM: The 82C59A is operated in level triggered mode when LTIM = 1, and the interrupt input edge circuit becomes disabled.

ADI: Designation of the CALL address interval. Interval = 4 when ADI = 1, and interval = 8 when ADI = 0.

SNGL: SNGL = 1 indicates the existence of only one 82C59A in the system. ICW3 is not required when SNGL = 1.

IC4: ICW4 is required when this bit is set, but not required when IC4 = 0.

(ii) Initialization Command Word 3 (ICW3)

This command word is written when there is more than one 82C59A used in cascade connections in the system, and is loaded into an 8-bit slave register. The functions of this slave register are listed below.

a. In a master mode system (BUF = 1 and M/S = 1 in ICW4 or $\overline{SP}/\overline{EN}$ = 1). "1" is set in each bit where a slave has been connected.
   In 85 mode, the master 82C59A releases byte 1 of the CALL sequence to enable the corresponding slave to release byte 2 or 3 (only byte 2 in 86 mode) through the cascade line.

b. In slave mode (BUF = 1 and M/S = 0 in ICW4 or $\overline{SP}/\overline{EN}$ = 0). Bits 0 thru 2 identify the slave. The slave compares these bits with the cascade input, and releases bytes 2 and 3 of the CALL sequence (only byte 2 in 86 mode) if a matching result is obtained.

(iii) Initialization Command Word 4 (ICW4)

SFNM: Special Fully Nested Mode is programmed when SFNM = 1.

BUF: Buffered mode is programmed when BUF = 1. In Buffered mode, $\overline{SP}/\overline{EN}$ is an output, and Master/slave is selected by the M/S bit.

M/S: If buffered mode is selected, the 82C59A is programmed as the master when M/S = 1, and as a slave when M/S = 0. M/S is ignored, however, when BUF = 0.

AEOI: Automatic End Of Interrupt mode is programmed by AEOI = 1.

μPM: (Microprocessor mode)
The 82C59A is set to 85 system operation when μPM = 0, and to 86 system operation when μ PM = 1.

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ICW1

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	A7	A6	A5	1	LTIM	ADI	SNGL	IC4

- IC4 — 1: ICW4 required; 0: ICW4 not required
- SNGL — 1: Single; 0: Cascade
- ADI — CALL address interval; 1: Interval = 4; 0: Interval = 8
- LTIM — 1: Level triggered mode; 0: Edge triggered mode
- A7, A6, A5 — Interrupt vector address A5 thru A7 (Valid only in 85 mode)

ICW2

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	A15/T7	A14/T6	A13/T5	A12/T4	A11/T3	A10	A9	A8

- D7–D0 — Interrupt vector address A8 thru A15 (85 mode); Interrupt vector address T3 thru T7 (86 mode)

ICW3 (master)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	S7	S6	S5	S4	S3	S2	S1	S0

- S7–S0 — 1: IR input holds slave; 0: IR input does not hold slave

ICW3 (slave)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	ID2	ID1	ID0

Slave ID

	0	1	2	3	4	5	6	7
ID0	0	1	0	1	0	1	0	1
ID1	0	0	1	1	0	0	1	1
ID2	0	0	0	0	1	1	1	1

Note: Slave ID indicates the IR input of the corresponding master.

ICW4

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SFNM	BUF	M/S	AEOI	μPM

- μPM — 1: 86 mode; 0: 85 mode
- AEOI — 1: Automatic EOI mode; 0: Normal EOI mode
- BUF, M/S:

BUF	M/S	
0	x	Non-buffered mode
1	0	Buffered mode (slave)
1	1	Buffered mode (master)

Note: X denotes not specified

- SFNM — 1: Special Fully Nested mode; 0: Not Special Fully Nested mode

Initialization Command Words (ICW1 thru ICW4)

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(6) Operation Command Words (OCW1 thru OCW3)

When Initialization Command Words (ICW) are programmed in the 82C59A, the interrupt input line is ready to receive interrupt requests. The Operation Command Words (OCWs) enable the 82C59A to be operated in various modes while the device is in operation.

(i) Operation Command Word 1 (OCW1)

OCW1 sets and resets the mask bits of the Interrupt Mask Register (IMR). M0 thru M7 represent 8 mask bits. The channel is masked when M = 1, but is enabled when M = 0.

(ii) Operation Command Word 2 (OCW2)

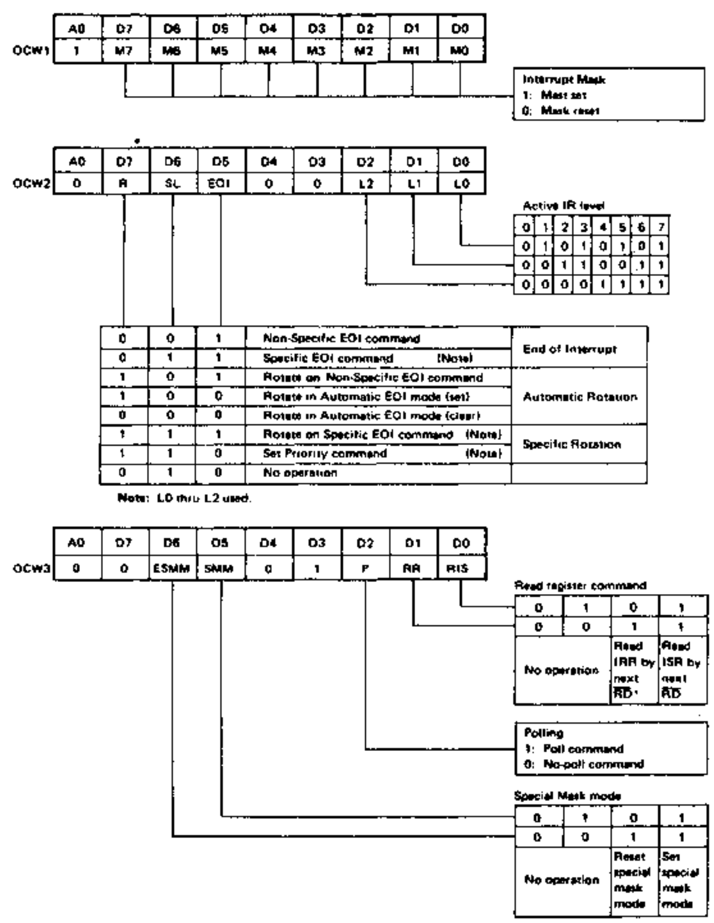
R, SL, EOI: The Priority Rotation and the End of Interrupt mode plus combinations of the two are controlled by combinations of these 3 bits. These combinations are listed in the operation command word format table.

L2, L1, L0: These bits indicate the specified interrupt level when SL = 1.

(iii) Operation Command Word 3 (OCW3)

ESMM: This enables the Special Mask Mode. The special mask mode can be set and reset by the SMM bit when ESMM = 1. The SMM bit is ignored when ESMM = 0.

SMM: (Special Mask Mode)
The 82C59A is set to Special Mask Mode when ESMM = 1 and SMM = 1, and is returned to normal mask mode when ESMM = 1 and SMM = 0. SMM is ignored when ESMM = 0.



Operation Command Words (OCW1 thru OCW3)

(7) Fully Nested Mode

As long as the 82C59A has not been programmed to another mode, this Fully Nested mode is set automatically after initialization. The interrupt requests are ordered in priority sequentially from 0 to 7 (where 0 represents highest priority). If an interrupt is then requested and is acknowledged highest priority, a corresponding vector address is released, and the corresponding bit in the in-service register (ISR) is set. The IS bit remains set until an End of Interrupt (EOI) command is issued from the microprocessor before returning from the interrupt service routine, or until the rising edge of the last $\overline{INTA}$ pulse arrives when the AEOI bit has been set.

When the IS bit is set, interrupts of the same or lower priority are inhibited - only interrupts of higher priority can be generated. In this case, interrupts can be ackowledged only when the internal interrupt enable F/F in the microprocessor has been enabled again through software. Following the initialization sequence, IR0 has the highest priority, and IR7 has the lowest. This priority can be changed by rotating priority mode in OCW2.

(8) End of Interrupt (EOI)

When the AEOI bit in ICW4 is set, the in-service (IS) bit is automatically reset by the rising edge of the last $\overline{INTA}$ pulse, or else is reset only when an EOI command is issued to the 82C59A prior to returning from the interrupt service routine.

And in cascade mode, the EOI command must be issued twice - once for the master, and once for the corresponding slave.

EOI commands are classified into specific EOI commands and Non-Specific EOI commands. When the 82C59A is operated in Fully Nested mode, the IS bit to be reset can be determined on EOI. If the Non-Specific EOI command is issued, the highest IS bit of those that are set is reset automatically, because the highest IS level is always the last servicing level in the Fully Nested mode. If, however, it is not in the fully Nested mode, the 82C59A will no longer be able to determine the last acknowledged level. In this case, it will be necessary to issue a Specific EOI which includes the IS level to be reset as part of the command. When the 82C59A is in Special Mask mode, care must be taken to ensure that IS bits masked by the IMR bit can not reset by the Non-Specific EOI.

(9) Automatic End of Interrupt (AEOI) Mode

When AEOI = 1 in ICW4, the 82C59A continues to operate in AEOI mode until programmed again by ICW4. In this mode, the 82C59A automatically performs Non-Specific EOI operation at the rising edge of the last $\overline{INTA}$ pulse (the third pulse in 85 systems, and the second pulse in 86 systems). In terms of systems, this mode is best used in nested multiple level interrupt configurations. It is not necessary when there is only one 82C59A. AEOI mode is only used in a master 82C59A device, not in a slave.

(10) Automatic Rotation (Devices with Equal Priority)

In some applications, there is often a number of devices with equal priority. In this mode, the device where an interrupt service has just been completed is set to the lowest priority. At worst, therefore, a particular interrupt request device may have to wait for seven other devices to be serviced at least once each. There are two methods for Automatic Rotation using OCW2 - Rotation on Non-Specific EOI command, and Rotation in Automatic EOI mode.

Before Rotation (IR4 the highest priority requesting service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
IS status	0	1	0	1	0	0	0	0
Priority status	7	6	5	4	3	2	1	0
	Lowest							Highest

After Rotation (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
IS status	0	1	0	0	0	0	0	0
Priority status	2	1	0	7	6	5	4	3
			Highest	Lowest				

(11) Specific Rotation (Specific Priority)

All priority levels can be changed by programming the lowest priority level (Set Priority Command in OCW2). For example, if IR5 is programmed as the device of lowest priority, IR6 will have the highest priority. In this mode, the internal status can be updated during OCW2 by software control. This is unrelated, however, to the EOI command in the same OCW2.

Priority level can also be changed by using the OCW2 Rotate On Specific EOI command.

(12) Interrupt Mask

Interrupt inputs can be masked individually by Interrupt Mask Registers (IMR) programmed through the OCW1. Each interrupt channel is masked (disabled) when the respective IMR bit is set to "1". IR0 is masked by bit 0, and IR1 is masked by bit 1. Masking of any particular channel has no effect on other channels.

(13) Special Mask Mode

In some applications, there is a need for dynamic updating of the system's priority level structure by software control during execution of an interrupt service routine. For example, it may be necessary to inhibit the lower priority requests for part of the execution of a certain routine while enabling for another part. In this case, it is difficult to enable all lower priority requests if the IS bit has not yet been reset by the EOI command after an interrupt request has been acknowledged (during execution of a service routine). All of these requests would normally be disabled.

Hence the use of the Special Mask mode. When a mask bit is set by OCW1 in this mode, the corresponding interrupt level requests are disabled. And all other unmasked level requests (at both higher and lower priority levels) are enabled. Interrupts can thus be enabled selectively by loading the mask register.

In this mode, the specific EOI Command should be used.

This Special Mask mode is set by OCW3 ESMM = 1 and SMM = 1, and reset by ESMM = 1 and SMM = 0.

(14) POLL Command

In this mode, the INT output in not used, the internal interrupt enable F/F of the microprocessor is reset, and interrupt inputs are disabled. Servicing the I/O device is executed by software using the Poll command.

The Poll command is issued by setting P in OCW3 to "1". The 82C59A regards the next $\overline{RD}$ pulse as reception of an interrupt, and if there is a request, the corresponding IS bit is set and the priority level is read out. Interrupts are frozen between $\overline{WR}$ and $\overline{RD}$.

	D7	D6	D5	D4	D3	D2	D1	D0
Poll word	1	0	0	0	0	W2	W1	W0

W0 thru W2: Binary coded highest priority level of service being requested.

1: Set to "1" when there is an interrupt.

This mode is useful when there is a common routine for a number of levels, and the $\overline{INTA}$ sequence is not required. ROM space can thus be saved.

(15) Reading 82C59A Status

The status of a number of internal registers can be read out for updating user information on the system. The following registers can be read by means of OCW3 (IRR and ISR) and OCW1 (IMR).

a. IRR: (Interrupt Request Register) 8-bit register for storing interrupt requesting levels.

b. ISR: (In-Service Register) 8-bit register for storing priority levels being serviced.

c. IMR: (Interrupt Mask Register) 8-bit register for storing interrupt request lines to be masked.

The IRR can be read when a Read Register Command is issued with OCW3 (RR = 1 and RIS = 0) prior to the $\overline{RD}$ pulse, and the ISR can be read when a Read Register Command is issued with OCW3 (RR = 1 and RIS = 1) prior to the $\overline{RD}$ pulse. And as long as the read status does not change, OCW3 is not required each time before the status is read. This is because the 82C59A remembers whether IRR or ISR was selected by the previous OCW3. But this is not true when poll is used.

The 82C59A is set to IRR after initialization. OCW3 is not required to read IMR. IMR is issued to the data bus if $\overline{RD}$ = 0 and A0 = 1 (OCW1).

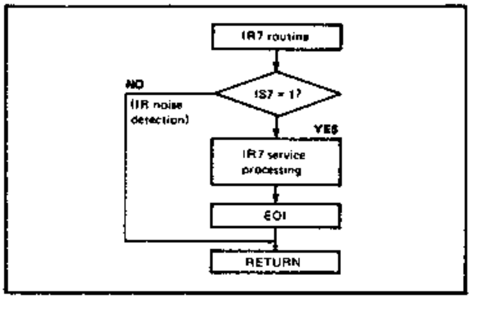
Reading status is disabled by polling when P = 1 and RR = 1 in OCW3.

(16) Edge and Level Trigger Mode

This mode is programmed by using bit 3 (LTIM) in ICW1. When LTIM = 0, the interrupt request is recognized by the IR input transition from Low to High. As long as the IR input is kept at High, no other interrupt is generated. Since interrupt requests are recognized by the IR input "H" level when LTIM = 1, edge detection is not required.

The interrupt request must be cancelled before output of the EOI command, and before the interrupt is enabled in order to prevent the generation of a second interrupt by the CPU.

The IR input must be held at High level until the falling edge of the first $\overline{INTA}$ pulse, irrespective of whether edge sense or level sense is employed. If the IR input is switched to Low level before the first $\overline{INTA}$ pulse, the default IR7 is generated when the interrupt is acknowledged by the CPU. This can be an effective safeguard to be adopted to detect interrupts generated by the noise glitches on the IR inputs. To take advantage of this feature, the IR7 routine is used as a "clean up" routine where the routine is simply executing a return instruction and the interrupt is subsequently ignored. When the IR7 is required for other purposes, the default IR7 can be detected by reading the ISR. Although correct IR7 interrupts involve setting of the corresponding ISR bit, the default IR7 is not set.



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(17) Special Fully Nested Mode

This mode is used in large systems where the cascade mode is used and the respective Interrupt Requests within each slave have to be given priority levels. In this case, the Special Fully Nested mode is programmed to the master by using ICW4. This mode is practically identical to the normal Fully Nested mode, but differs in the following two respects.

a. When an interrupt request is received from a particular slave during servicing, a new interrupt request from an IR with a higher priority level than the interrupt level of the slave being serviced is recognized by the master and the interrupt is applied to the processor without the master priority logic being inhibited by the slave. In normal Fully Nested mode, if the request is in service, a slave is masked and no other requests can be recognized from the same slave.

b. When exiting from an interrupt service routine, it is first necessary to check whether or not the interrupt which has just been serviced by software was the only interrupt from that slave. This is done by sending a Non-Specific EOI command to that slave, followed by reading of the In-Service Register (ISR) to see whether that register has become all '0'. A Non-Specific EOI is sent to the master too if the ISR is empty, and if not no EOI should be sent.

(18) Buffered Mode

Control for buffer enabling is required when the 82C59A is used in a large system where a data bus drive buffer is needed and cascade mode is used. When buffered mode is selected, the 82C59A sends an enable signal on the $\overline{SP}/\overline{EN}$ pin to enable the buffer. In this mode, the $\overline{SP}/\overline{EN}$ output always becomes active while the 82C59A's data bus output is enabled. Therefore, the 82C59A requires programming to enable it to distinguish master from slave. Buffered mode is programmed by bit 3 in ICW4, and the ability to distinguish master from slave is programmed by bit 2 in ICW4.

(19) Cascade Mode

To enable the 82C59A to handle up to 64 priority levels, a maximum of 8 slaves can be easily connected to one master device.

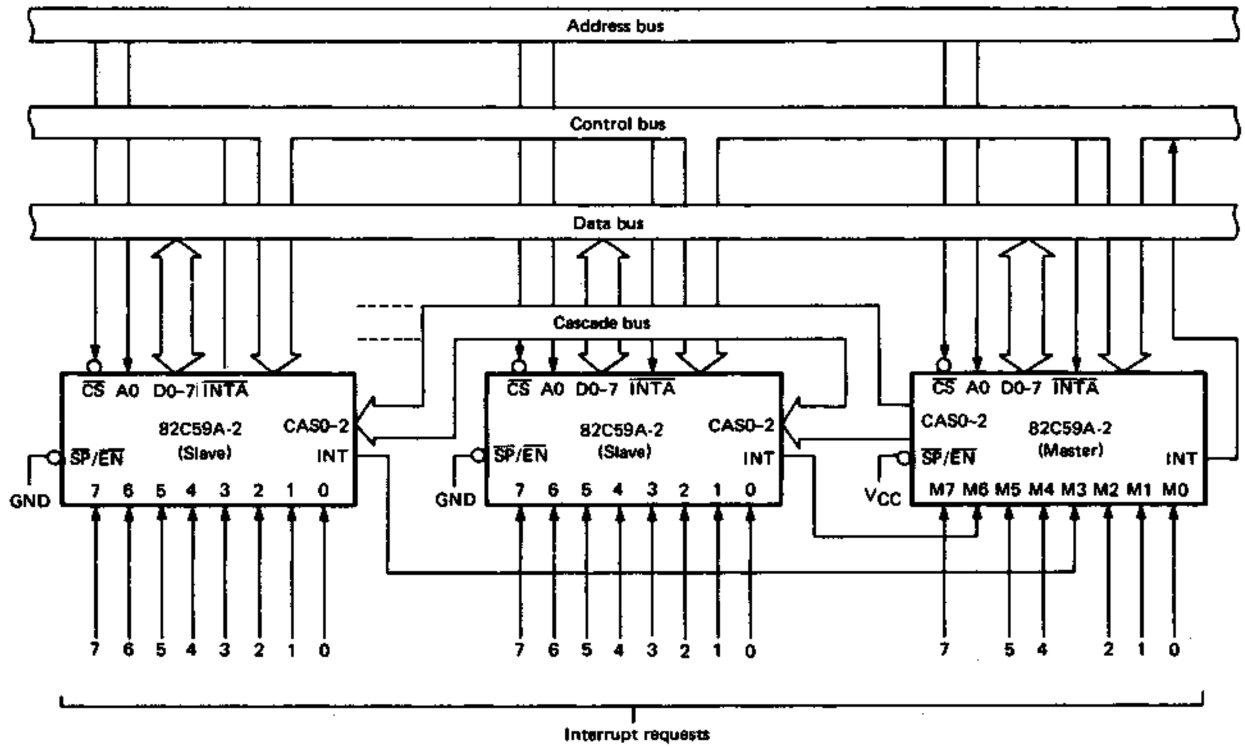
The master controls the slaves through three cascade lines, the cascade bus executes like a slave chip select during the $\overline{INTA}$ sequence.

In cascade configuration, slave interrupt outputs (INT) are connected to master interrupt request inputs (IR). When a slave IR becomes active and is acknowledged, the master enables the corresponding slave to release the routine address for that device during bytes 2 and 3 (only byte 2 in 86 mode) of the $\overline{INTA}$ sequence.

The cascade bus line is normally kept at low level, and holds the slave address during the period from the rising edge of the first $\overline{INTA}$ pulse up to the rising edge of the third $\overline{INTA}$ pulse (or the second $\overline{INTA}$ pulse in 86 mode).

Each 82C59A device in the system can operate in different modes in accordance with their initialization sequences. EOI commands must be issued twice, once for the master once for the corresponding slave. Each 82C59A requires an address decoder to activate the respective chip select (CS) inputs.

Since the cascade line is normally kept at low level, note that slaves must be connected to the master IR0 only after all slaves have been connected to the other IRs.



82C59A-2 cascade connections

OKI semiconductor

MSM82C84ARS/GS

CLOCK GENERATOR AND DRIVER

GENERAL DESCRIPTION

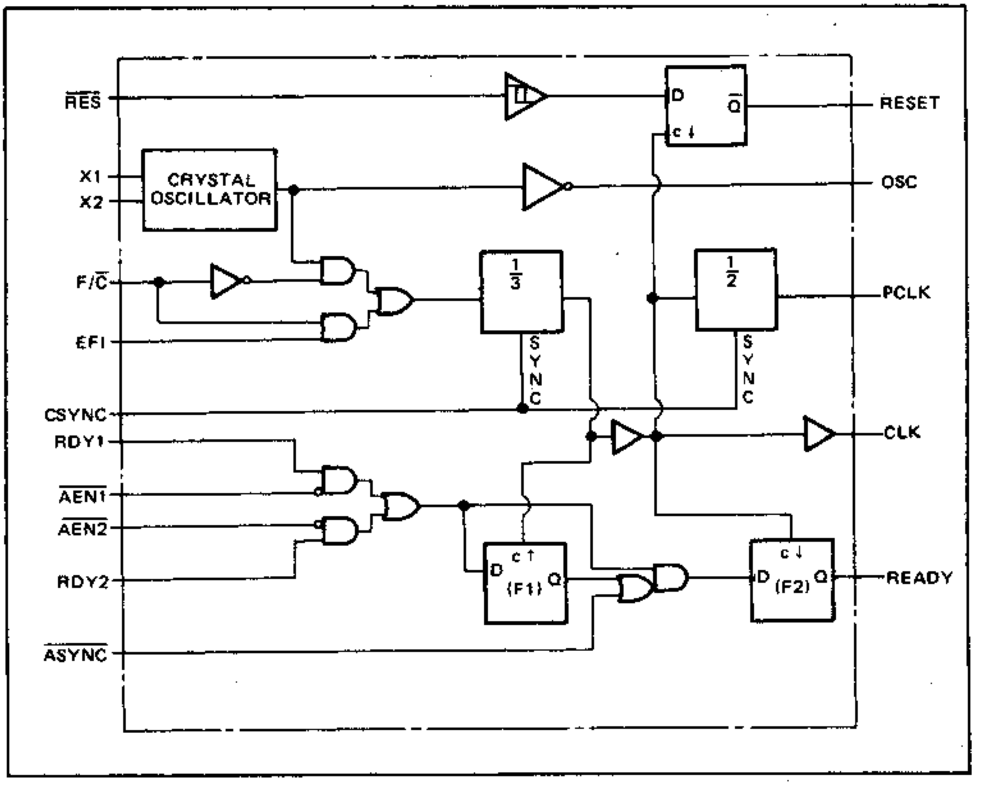
The MSM82C84ARS/GS is a clock generator designed to generate MSM80C86 and MSM80C88 system clocks.

Due to the use of silicon gate CMOS technology, standby current is only 100μA (MAX.), and the power consumption is very low with 10 mA (MAX.) when a 5 MHz clock is generated.

FEATURES

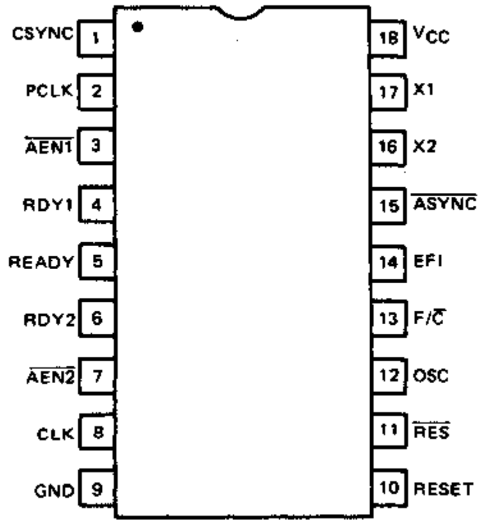
- Operating frequency of 6 to 15 MHz (CLK output 2 to 5 MHz)
- 3μ silicon gate CMOS technology for low power consumption
- Built-in crystal oscillator circuit
- 3V ~ 6V single power supply
- Built-in synchronized circuit for MSM80C86 and MSM80C88 READY and RESET
- TTL compatible
- Built-in Schmitt trigger circuit ($\overline{RES}$ input)
- 18-pin DIP (MSM82C84ARS)
- 24-pin flat package (MSM82C84AGS)

FUNCTIONAL BLOCK DIAGRAM

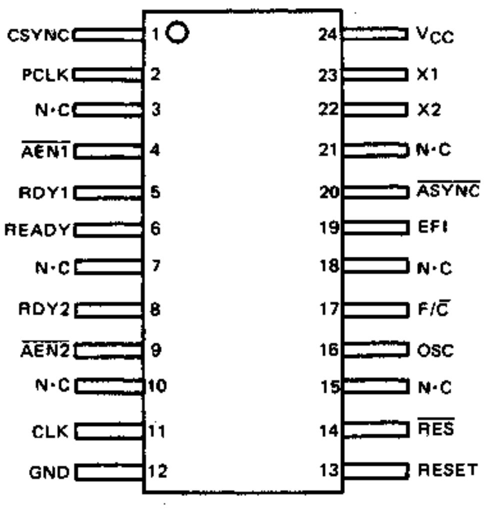


PIN CONFIGURATION

18 Lead Plastic DIP



24 Lead Plastic Flat Package



(N·C not connected)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits		Unit	Conditions
		MSM82C84ARS	MSM82C84AGS		
Supply Voltage	V_{CC}	−0.5 ~ +7		V	Respect to GND
Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5		V	
Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5		V	
Storage Temperature	Tstg	−55 ~ +150		°C	–
Power Dissipation	P_D	0.8	0.7	W	Ta = 25°C

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Level Input Voltage (except $\overline{RES}$)	V_{IH}	2.2		V_{CC} +0.3	V
"H" Level Input Voltage ($\overline{RES}$)		3.0			

DC CHARACTERISTICS

Parameter	Symbol	MIN	MAX	Unit	Conditions	
"L" Level Output Voltage	V_{OL}	–	0.45	V	I_{OL} = 5mA	V_{CC} = 4.5V ~ 5.5V Ta = −40°C ~ +85°C
"H" Level Output Voltage	V_{OH}	3.7	–	V	I_{OH} = −1mA	
$\overline{RES}$ Input Hysteresis	$V_{IHR}-V_{ILR}$	0.25	–	V	–	
Input Leak Current	I_{LI}	−10	10	μA	$0 \leqq V_{IN} \leqq V_{CC}$	
Standby Supply Current	I_{CCS}	–	100	μA	$X1 \geqq V_{CC}$ −0.2V $X2 \leqq 0.2V$ $F/\overline{C} \geqq V_{CC}$ −0.2V $V_{IH} \geqq V_{CC}$ −0.2V $V_{IL} \leqq 0.2V$	
Operating Supply Current	I_{CC}	–	10	mA	Input frequency 15 MHz Output load capacitance C_L = 0pF	

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AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = −40 ~ 85°C)

(1)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
EFI "H" Pulse Width	t_{EHEL}	20		ns	90%–90%	Output load capacitance CLK output C_L = 100pF Others 30pF
EFI "L" Pulse Width	t_{ELEH}	20		ns	10%–10%	
EFI Cycle Time	t_{ELEL}	66		ns		
Crystal Oscillator Frequency		6	15	MHz		
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Active)	t_{R1VCL}	35		ns	$\overline{\text{ASYNC}}$ = High	
Set Up Time of RDY1 or RDY2 to CLK Rising Edge (Active)	t_{R1VCH}	35		ns	$\overline{\text{ASYNC}}$ = Low	
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Inactive)	t_{R1VCL}	35		ns		
Hold Time of RDY1 or RDY2 to CLK Falling Edge	t_{CLR1X}	0		ns		
Set Up Time of $\overline{\text{ASYNC}}$ to CLK Falling Edge	t_{AYVCL}	50		ns		
Hold Time of $\overline{\text{ASYNC}}$ to CLK Falling Edge	t_{CLAYX}	0		ns		
Set Up Time of $\overline{\text{AEN1}}$ ($\overline{\text{AEN2}}$) to RDY1 (RDY2) Rising Edge	t_{A1R1V}	15		ns		
Hold Time of $\overline{\text{AEN1}}$ ($\overline{\text{AEN2}}$) to CLK Falling Edge	t_{CLA1X}	0		ns		
Set Up Time of CSYNC to EFI Rising Edge	t_{YHEH}	20		ns		
Hold Time of CSYNC to EFI Rising Edge	t_{EHYL}	10		ns		
CSYNC Pulse Width	t_{YHYL}	2 × t_{ELEL}		ns		
Set Up Time of $\overline{\text{RES}}$ to CLK Falling Edge	t_{I1HCL}	65		ns		
Hold Time of $\overline{\text{RES}}$ to CLK Falling Edge	t_{CLI1H}	20		ns		
Input Rising Edge Time	t_{ILIH}		20	ns		
Input Falling Edge Time	t_{IHIL}		20	ns		

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

5

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = −40 ~ 85°C)

(2)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
CLK Cycle Time	t_{CLCL}	200		ns		Output load capacitance CLK output C_L = 100pF Others 30pF
CLK "H" Pulse Width	t_{CHCL}	65		ns		
CLK "L" Pulse Width	t_{CLCH}	119		ns		
CLK Rising and Falling Edge Times	t_{CH1CH2} t_{CL2CL1}		15	ns	1.0V−3.5V	
PCLK "H" Pulse Width	t_{PHPL}	180		ns		
PCLK "L" Pulse Width	t_{PLPH}	180		ns		
Time from READY Falling Edge to CLK Falling Edge	t_{RYLCL}	−8		ns		
Time from READY Rising Edge to CLK Rising Edge	t_{RYHCH}	114		ns		
Delay from CLK Falling Edge to RESET Falling Edge	t_{CLIL}		40	ns		
Delay from CLK Falling Edge to PCLK Rising Edge	t_{CLPH}		22	ns		
Delay from CLK Falling Edge to PCLK Falling Edge	t_{CLPL}		22	ns		
Delay from OSC Falling Edge to CLK Rising Edge	t_{OLCH}	−5	22	ns		
Delay from OSC Falling Edge to CLK Falling Edge	t_{OLCL}	2	35	ns		
Output Rising Edge Time (Except CLK)	t_{OLOH}		15	ns	0.8V~2.2V	
Output Falling Edge Time (Except CLK)	t_{OHOL}		15	ns	2.2V~0.8V	

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

5

PIN DESCRIPTION

Pin symbol	Name	Input/ output	Function
CSYNC	Clock synchronization signal	Input	Synchronizing signal for output of in-phase CLK signals when more than one MSM82C84A is used. The internal counter is reset when this signal is at high level, and a high level CLK output is generated. The internal counter is subsequently activated and a 33% duty CLK output is generated when this signal is switched to low level. When this signal is used, external synchronization of EFI is necessary. When the internal oscillator is used, it is necessary for this pin to be kept to be low level.
PCLK	Peripheral clock output	Output	This peripheral circuit clock signal is output in a 50% duty cycle at a frequency half that of the clock signal.
$\overline{AEN1}$ $\overline{AEN2}$	Address enable signals	Input	The $\overline{AEN1}$ signal enables RDY1, and the $\overline{AEN2}$ signal enables RDY2. The respective RDY inputs are activated when the level applied to these pins is low. Although two separate inputs are used in multi-master systems, only the $\overline{AEN}$ which enables the RDY input to be used is to be switched to low level in the case of not using multi-master systems.
RDY1 RDY2	Bus ready signals	Input	Completion of data bus reading and writing by the device connected to the system data bus is indicated when one of these signals is switched to high level. The relevant RDY input is enabled only when the corresponding $\overline{AEN}$ is at low level.
READY	Ready output	Output	This signal is obtained by synchronizing the bus ready signal with CLK. This signal is output after guaranteeing the hold time for the CPU in phase with the RDY input.
CLK	Clock output	Output	This signal is the clock used by the CPU and peripheral devices connected to the CPU system data bus. The output waveform is generated in a 33% duty cycle at a frequency 1/3 the oscillating frequency of the crystal oscillator connected to the X1 and X2 pins, or at a frequency 1/3 the EFI input frequency.
$\overline{RES}$	Reset in	Input	This low-level active input is used to generate a CPU reset signal. Since a Schmitt trigger is included in the input circuit for this signal, "power on resetting" can be achieved by connection of a simple RC circuit.
RESET	Reset output	Output	This signal is obtained by CLK synchronization of the input signal applied to $\overline{RES}$ and is output in opposite phase to the $\overline{RES}$ input. This signal is applied to the CPU as the system reset signal.
F/$\overline{C}$	Clock select signal	Input	This signal selects the fundamental signal for generation of the CLK signal. The CLK is generated from the crystal oscillator output when this signal is at low level, and from the EFI input signal when at high level.
EFI	External clock signal	Input	The signal applied to this input pin generates the CLK signal when F/$\overline{C}$ is at high level. The frequency of the input signal needs to be three times greater than the desired CLK frequency.
X1, X2	Crystal oscillator connecting pins	Input	Crystal oscillator connections. The crystal oscillator frequency needs to be three times greater than the desired CLK frequency.
OSC	Crystal resonator output	Output	Crystal oscillator output. This output frequency is the same as the oscillating frequency of the oscillator connected to the X1 and X2 pins. As long as a Xtal oscillator is connected to the X1 and X2 pins, this output signal can be obtained independently even if F/C is set to high level to enable the EFI input to be used for CLK generation purposes.

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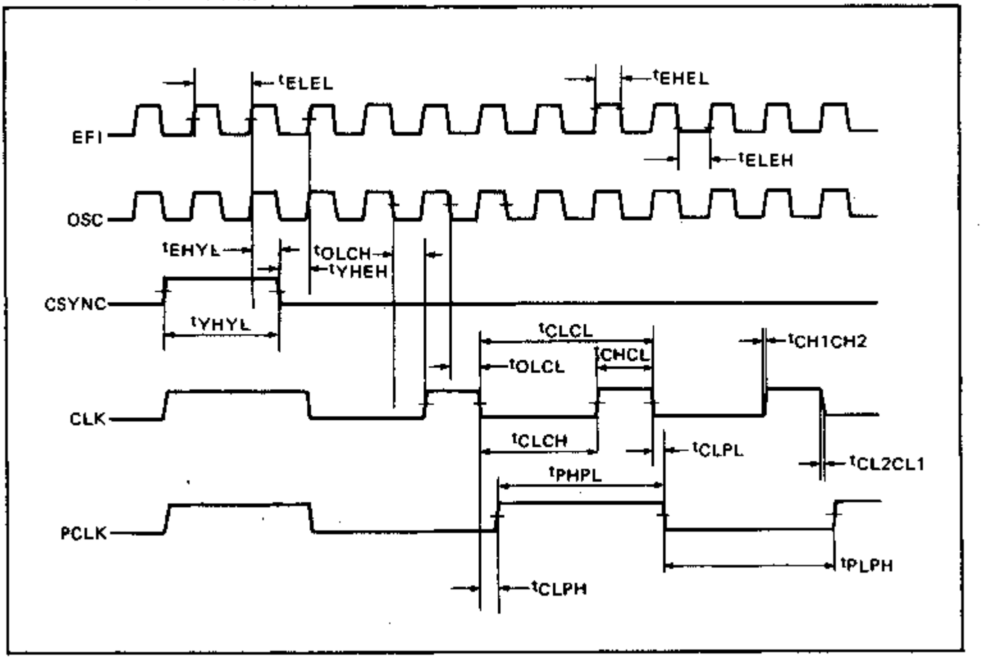
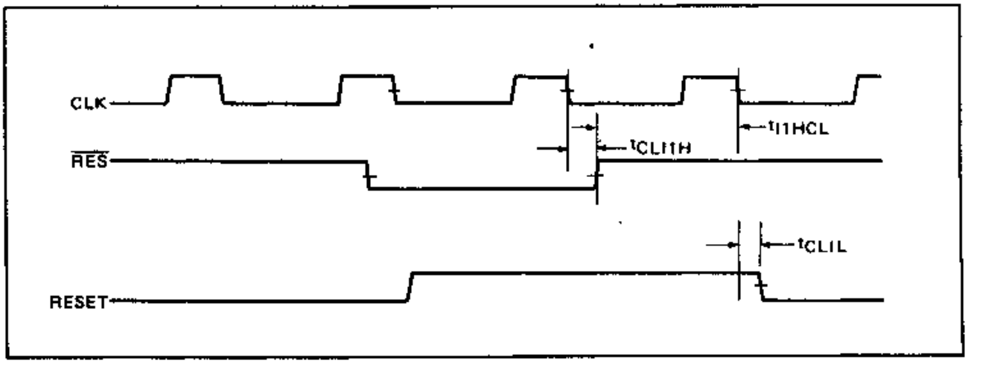
Pin symbol	Name	Input/output	Function
$\overline{ASYNC}$	Ready synchronization select signal	Input	Signal for selection of the synchronization mode of the READY signal generator circuit. When this signal is at low level, the READY signal is generated by double synchronization. And when at high level, the READY signal is generated by single synchronization. Since this pin has not been equipped with internal pull-up resistance, this pin must not be opened.
V_{CC}			+5V power supply
GND			GND

TIMING CHART

CLK · PCLK · OSC waveforms



RESET waveform



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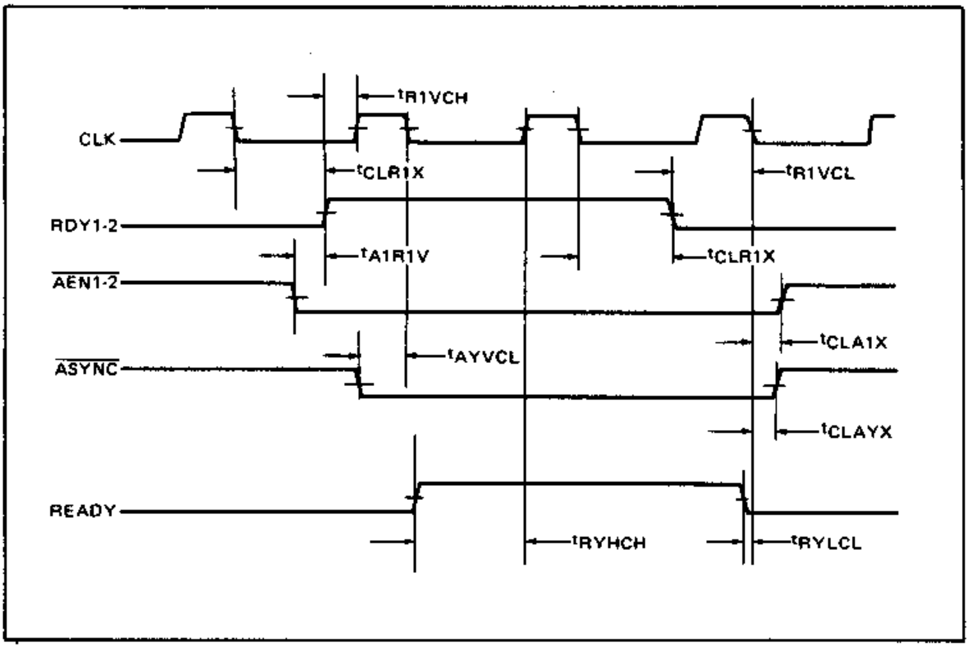
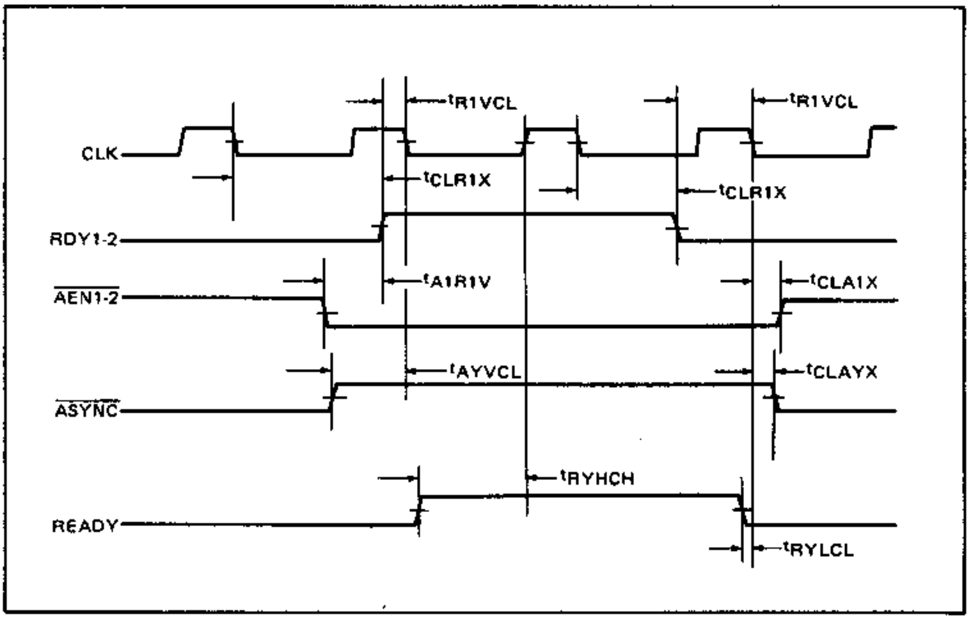
READY waveform ($\overline{ASYNC}$ = L)



READY waveform ($\overline{ASYNC}$ = H)



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DESCRIPTION OF OPERATION

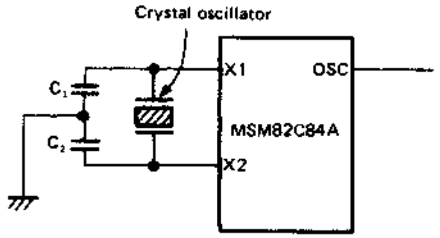
(1) Oscillator Circuit

The MSM82C84A internal oscillator circuit can be driven by connecting a crystal oscillator to the X1 and X2 pins.

The frequency of the crystal oscillator in this case needs to be three times greater than the desired CLK frequency.

Since the oscillator circuit output (the same output as for the crystal resonator frequency) appears at the OSC pin, independent use of this output is also possible.

Recommended Oscillator Circuit



When input frequency is 6 to 15 MHz,

$C_1 = C_2 = 33$ pF

(2) Clock Generator Circuit

This circuit generates two clock outputs—CLK obtained by dividing the input external clock or crystal oscillator circuit output by three, and PCLK obtained by halving CLK. CLK and PCLK are generated from the external clock applied to the EFI pin when F/$\overline{C}$ is at high level, and are generated from the crystal oscillator circuit when at low level.

(3) Reset Circuit

Since a Schmitt trigger circuit is used in the $\overline{RES}$ input, the MSM82C84A can be reset by "power on" by connection to a simple RC circuit. If the 80C86 or 80C88 is used as the CPU in this case, it is necessary to keep the $\overline{RES}$ input at low level for at least 50 μs after V_{CC} reaches the 4.5V level.

(4) Ready Circuit

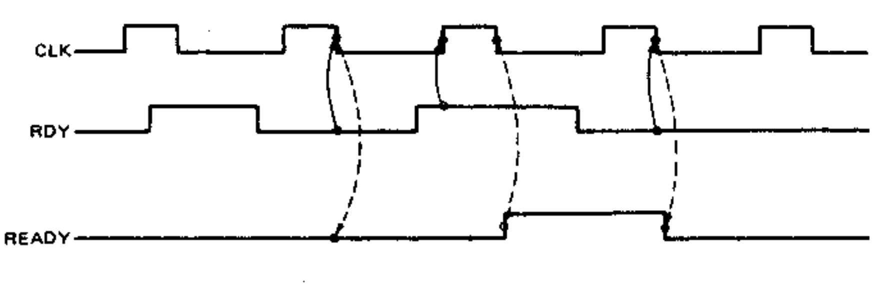
The READY signal generator circuit can be set to synchronization mode by $\overline{ASYNC}$.

(i) When $\overline{ASYNC}$ is at low level

The RDY input is output as the READY signal by double synchronization.

The high-level RDY input is synchronized once by the rising edge of the CLK of the first stage flip-flop (F1 in the circuit diagram), and then synchronized again by the falling edge of the CLK of the next stage flip-flop (F2 in the circuit diagram), resulting in output of a high-level READY output signal (see diagram below).

○ The low-level RDY input is synchronized directly by the falling edge of the CLK of the next stage flip-flop, resulting in output of a low-level READY output signal (see diagram below).



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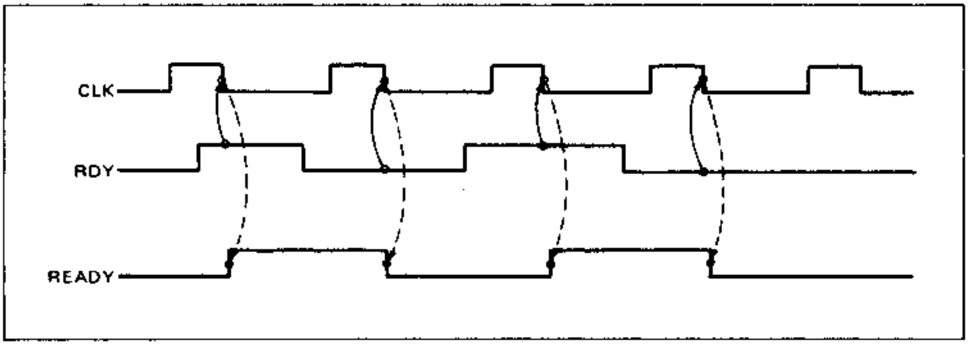
(ii) When $\overline{ASYNC}$ is at high level
The RDY input is output as the READY signal by single synchronization:

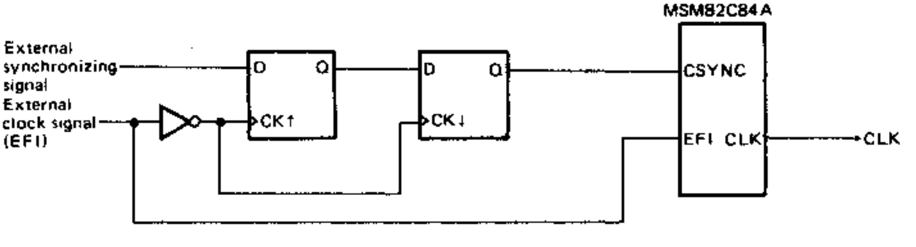
○ Both low-level and high-level RDY inputs are synchronized by the falling edge of the CLK of the next stage flip-flop, resulting in output of respective low-level and high-level READY output signals (see diagram below).



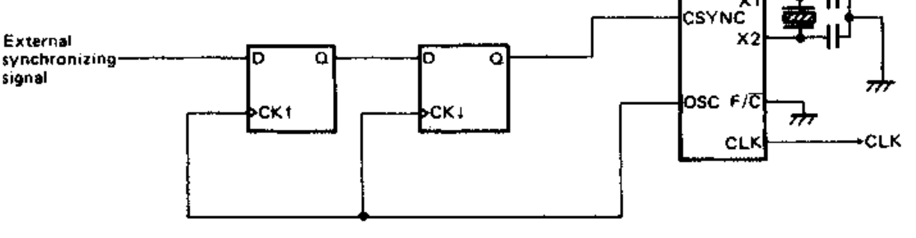
EXAMPLE OF USE (CSYNC)

The 82C84A 1/3 frequency divider counter is unsettled when the power is switched on. Therefore, the CSYNC pin has been included to synchronize CLK with another signal. When CSYNC is at high level, both CLK and PCLK are high-level outputs. If CSYNC is then switched to low level, CLK is output from the next input clock rising edge, and is divided by 3.

If CSYNC has not been synchronized with the input clock, use the following circuit to achieve the required synchronization.



When an external clock EFI is used as the clock source



When the crystal oscillator is used as the clock source

OKI semiconductor

MSM82C84A-5RS/GS

CLOCK GENERATOR AND DRIVER

GENERAL DESCRIPTION

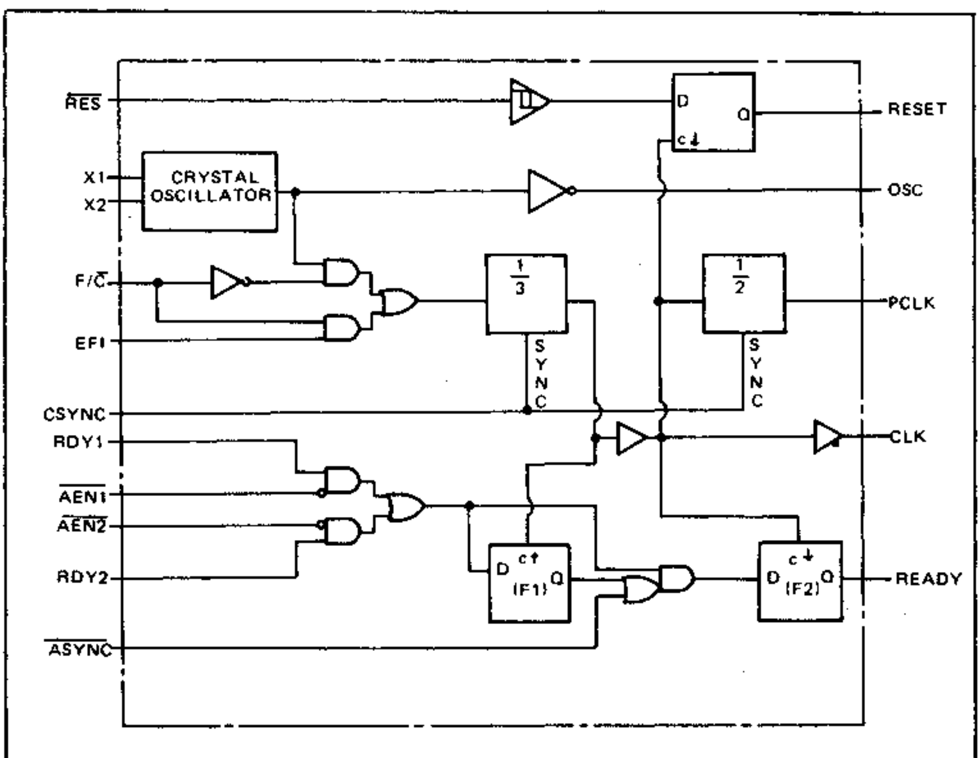
The MSM82C84A-5RS/GS is a clock generator designed to generate MSM80C86 and MSM80C88 system clocks.

Due to the use of silicon gate CMOS technology, standby current is only 40 μA (MAX.), and the power consumption is very low with 10 mA (MAX.) when a 5 MHz clock is generated.

FEATURES

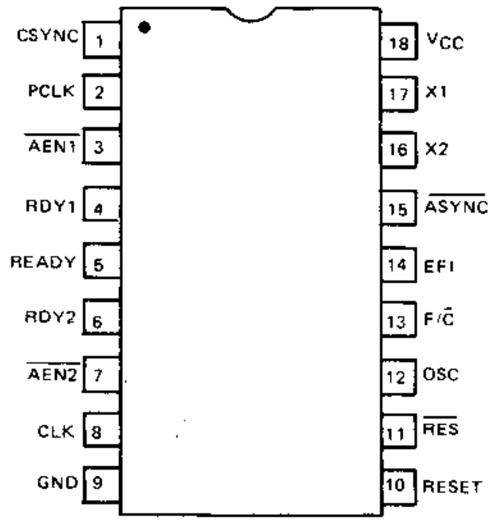
- Operating frequency of 6 to 15 MHz (CLK output 2 to 5 MHz)
- 3μ silicon gate CMOS technology for low power consumption
- Built-in crystal oscillator circuit
- 3V ~ 6V single power supply
- Built-in synchronized circuit for MSM80C86 and MSM80C88 READY and RESET
- TTL compatible
- Built-in Schmitt trigger circuit ($\overline{RES}$ input)
- 18-pin DIP (MSM82C84A-5RS)
- 24-pin flat package (MSM82C84A-5GS)

FUNCTIONAL BLOCK DIAGRAM

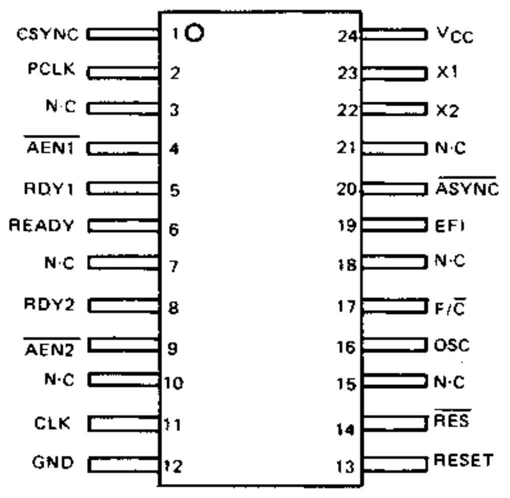


PIN CONFIGURATION

18 Lead Plastic DIP



24 Lead Plastic Flat Package



(N·C not connected)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits		Unit	Conditions
		MSM82C84A-5RS	MSM82C84A-5GS		
Supply Voltage	V_{CC}	−0.5 ~ +7		V	Respect to GND
Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5		V	
Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5		V	
Storage Temperature	Tstg	−55 ~ +150		°C	–
Power Dissipation	P_D	0.8	0.7	W	Ta = 25°C

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	−0.5		+0.8	V
"H" Level Input Voltage (except $\overline{RES}$)	V_{IH}	2.2		V_{CC}+0.5	V
"H" Level Input Voltage ($\overline{RES}$)		0.6*V_{CC}			

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

Parameter	Symbol	MIN	MAX	Unit	Conditions
"L" Level Output Voltage (CLK)	V_{OL}	–	0.4	V	I_{OL} = 4 mA
"L" Level Output Voltage (OTHERS)	V_{OL}	–	0.4	V	I_{OL} = 2.5mA
"H" Level Output Voltage (CLK)	V_{OH}	V_{CC} − 0.4	–	V	I_{OH} = −4mA
"H" Level Output Voltage (OTHERS)	V_{OH}	V_{CC} − 0.4		V	I_{OH} = −1mA
$\overline{RES}$ Input Hysteresis	$V_{IHR} - V_{ILR}$	0.2 * V_{CC}		V	
Input Leak Current (EXCEPT $\overline{ASYNC}$)	I_{LI}	−1	+1	μA	$0 \leq V_{in} \leq V_{CC}$
Input Current ($\overline{ASYNC}$)	I_{LIA}	−100	+10	μA	$0 \leq V_{in} \leq V_{CC}$
Standby Supply Current	I_{CCS}		+40	μA	NOTE 1
Operating Supply Current	I_{CC}		10	mA	f = 15MHz, C_L = 0_{pF}
Input Capacitance	C_{in}		7	pF	f = 1 MHz

NOTE 1: X1 ≥ V_{CC} − 0.2V, X2 ≤ 0.2V
F/C ≥ V_{CC} − 0.2V, $\overline{ASYNC}$ = V_{CC} or open
VIH ≥ V_{CC} − 0.2V, VIL ≤ 0.2V

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

(1)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
EFI "H" Pulse Width	t_{EHEL}	20		ns	90%–90%	Output load capacitance CLK output C_L = 100pF Others 30pF
EFI "L" Pulse Width	t_{ELEH}	20		ns	10%–10%	
EFI Cycle Time	t_{ELEL}	66		ns		
Crystal Oscillator Frequency		6	15	MHz		
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Active)	t_{R1VCL}	35		ns	$\overline{ASYNC}$ = High	
Set Up Time of RDY1 or RDY2 to CLK Rising Edge (Active)	t_{R1VCH}	35		ns	$\overline{ASYNC}$ = Low	
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Inactive)	t_{R1VCL}	35		ns		
Hold Time of RDY1 or RDY2 to CLK Falling Edge	t_{CLR1X}	0		ns		
Set Up Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{AYVCL}	50		ns		
Hold Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{CLAYX}	0		ns		
Set Up Time of $\overline{AEN1}$ ($\overline{AEN2}$) to RDY1 (RDY2) Rising Edge	t_{A1R1V}	15		ns		
Hold Time of $\overline{AEN1}$ ($\overline{AEN2}$) to CLK Falling Edge	t_{CLA1X}	0		ns		
Set Up Time of CSYNC to EFI Rising Edge	t_{YHEH}	20		ns		
Hold Time of CSYNC to EFI Rising Edge	t_{EHYL}	10		ns		
CSYNC Pulse Width	t_{YHYL}	2 × t_{ELEL}		ns		
Set Up Time of $\overline{RES}$ to CLK Falling Edge	t_{I1HCL}	65		ns		
Hold Time of $\overline{RES}$ to CLK Falling Edge	t_{CLI1H}	20		ns		
Input Rising Edge Time	t_{ILIH}		15	ns		
Input Falling Edge Time	t_{IHIL}		15	ns		

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

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AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = −40 ~ 85°C)

(2)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
CLK Cycle Time	t_{CLCL}	200		ns		Output load capacitance CLK output C_L = 100pF Others 30pF
CLK "H" Pulse Width	t_{CHCL}	$\frac{1}{3}T_{CLCL}+2$		ns		
CLK "L" Pulse Width	t_{CLCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
CLK Rising and Falling Edge Times	t_{CH1CH2} t_{CL2CL1}		10	ns	1.0V−3.5V	
PCLK "H" Pulse Width	t_{PHPL}	$T_{CLCL}-20$		ns		
PCLK "L" Pulse Width	t_{PLPH}	$T_{CLCL}-20$		ns		
Time from READY Falling Edge to CLK Falling Edge	t_{RYLCL}	−8		ns		
Time from READY Rising Edge to CLK Rising Edge	t_{RYHCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
Delay from CLK Falling Edge to RESET Falling Edge	t_{CLIL}		40	ns		
Delay from CLK Falling Edge to PCLK Rising Edge	t_{CLPH}		22	ns		
Delay from CLK Falling Edge to PCLK Falling Edge	t_{CLPL}		22	ns		
Delay from OSC Falling Edge to CLK Rising Edge	t_{OLCH}	−5	22	ns		
Delay from OSC Falling Edge to CLK Falling Edge	t_{OLCL}	2	35	ns		
Output Rising Edge Time (Except CLK)	t_{OLOH}		15	ns	0.8V~2.2V	
Output Falling Edge Time (Except CLK)	t_{OHOL}		15	ns	2.2V~0.8V	

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

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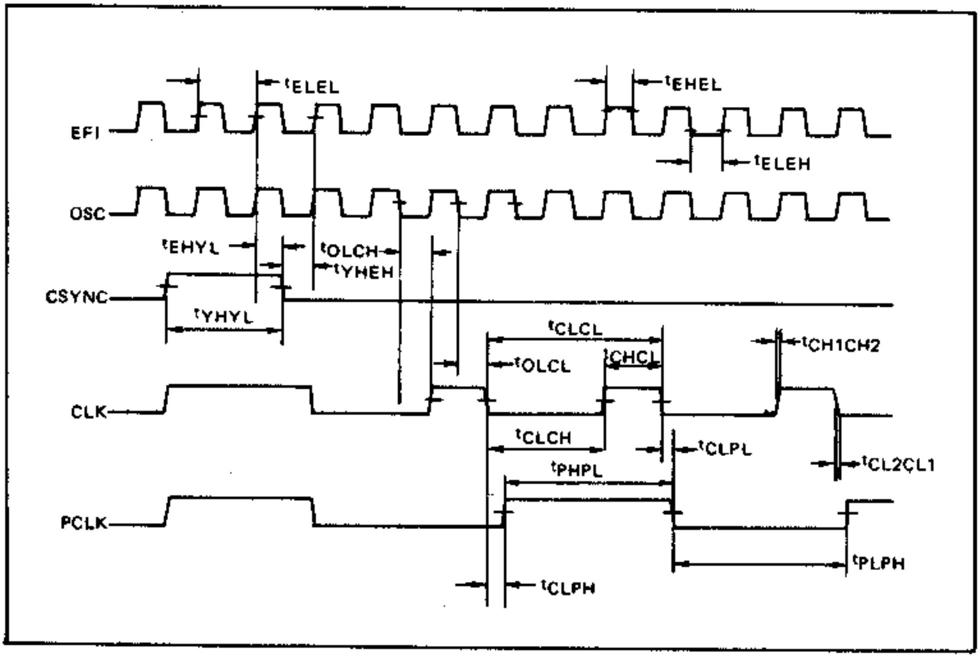
PIN DESCRIPTION

Pin symbol	Name	Input/ output	Function
CSYNC	Clock synchronization singal	Input	Synchronizing signal for output of in-phase CLK signals when more than one MSM82C84A-5 is used. The internal counter is reset when this signal is at high level, and a high level CLK output is generated. The internal counter is subseqently activated and a 33% duty CLK output is generated when this signal is switched to low level. When this signal is used, external synchronization of EFI is necessary. When the internal oscillator is used, it is necessary for this pin to be kept to be low level.
PCLK	Peripheral clock output	Output	This peripheral circuit clock signal is output in a 50% duty cycle at a frequency half that of the clock signal.
$\overline{\text{AEN1}}$ $\overline{\text{AEN2}}$	Address enable signals	Input	The $\overline{\text{AEN1}}$ signal enables $\overline{\text{RDY1}}$, and the $\overline{\text{AEN2}}$ signal enables RDY2. The respective RDY inputs are activated when the level applied to these pins is low. Although two separate inputs are used in multi-master systems, only the $\overline{\text{AEN}}$ which enables the RDY input to be used is to be switched to low level in the case of not using multi-master systems.
RDY1 RDY2	Bus ready signals	Input	Completion of data bus reading and writing by the device connected to the system data bus is indicated when one of these signals is switched to high level. The relevant RDY input is enables only when the corresponding $\overline{\text{AEN}}$ is at low level.
READY	Ready output	Output	This signal is obtained by synchronizing the bus ready signal with CLK. This signal is output after guaranteeing the hold time for the CPU in phase with the RDY input.
CLK	Clock output	Output	This signal is the clock used by the CPU and peripheral devices connected to the CPU system data bus. The output waveform is generated in a 33% duty cycle at a frequency 1/3 the oscillating frequency of the crystal oscillator connected to the X1 and X2 pins, or at a frequency 1/3 the EFI input frequency.
$\overline{\text{RES}}$	Reset in	Input	This low-level active input is used to generate a CPU reset signal. Since a Schmitt trigger is included in the input circuit for this signal, "power on resetting" can be achieved by connection of a simple RC circuit.
RESET	Reset output	Output	This signal is obtained by CLK synchronization of the input signal applied to $\overline{\text{RES}}$ and is output in opposite phase to the $\overline{\text{RES}}$ input. This signal is applied to the CPU as the system reset signal.
F/C	Clock select signal	Input	This signal selects the fundamental signal for generation of the CLK signal. The CLK is generated from the crystal oscillator output when this signal is at low level, and from the EFI input signal when at high level.
EFI	External clock signal	Input	The signal applied to this input pin generates the CLK signal when F/$\overline{\text{C}}$ is at high level. The frequency of the input signal needs to be three times greater than the desired CLK frequency.
X1, X2	Crystal oscillator connecting pins	Input	Crystal oscillator connections. The crystal oscillator frequency needs to be three times greater than the desired CLK frequency.
OSC	Crystal resonator output	Output	Crystal oscillator output. This output frequency is the same as the oscillating frequency of the oscillator connected to the X1 and X2 pins. As long as a Xtal oscillator is connected to the X1 and X2 pins, this output signal can be obtained independently even if F/C is set to high level to enable the EFI input to be used for CLK generation purposes.

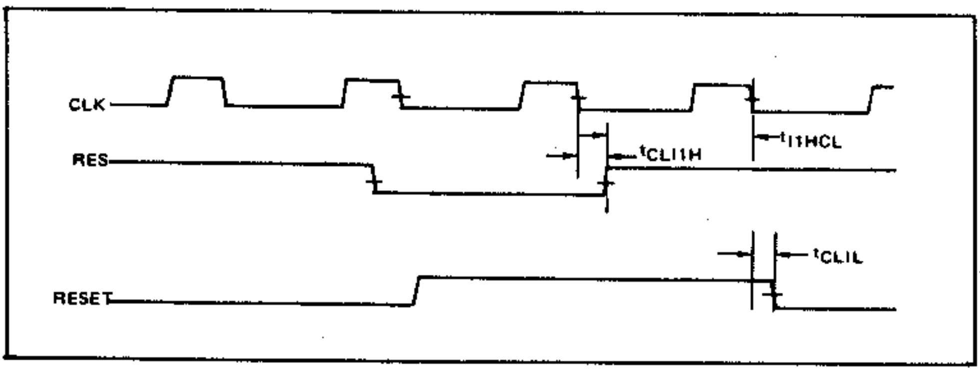
Pin symbol	Name	Input/ output	Function
$\overline{ASYNC}$	Ready synchronization select signal	Input	Signal for selection of the synchronization mode of the READY signal generator circuit. When this signal is at low level, the READY signal is generated by double synchronization. And When at high level, the READY signal is generated by single synchronization. This pin is equipped with internal pull-up resister.
V_{CC}			+5V power supply
GND			GND

TIMING CHART

CLK · PCLK · OSC waveforms



RESET waveform



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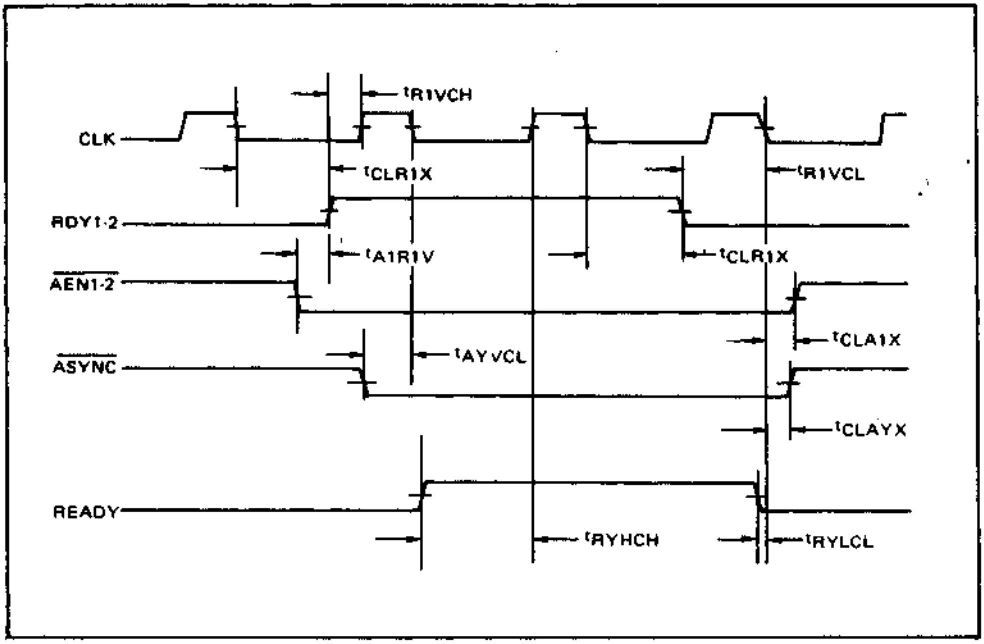
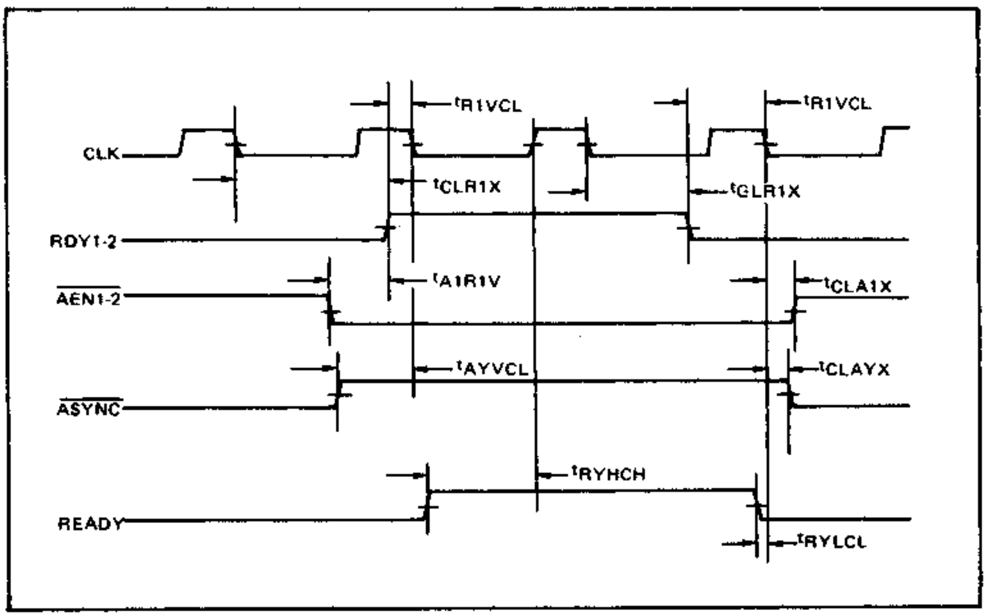
READY waveform (ASYNC = L)



READY waveform (ASYNC = H)



DESCRIPTION OF OPERATION

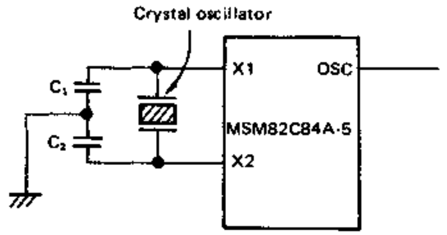
(1) Oscillator Circuit

The MSM82C84A-5 internal oscillator circuit can be driven by connecting a crystal oscillator to the X1 and X2 pins.

The frequency of the crystal oscillator in this case needs to be three times greater than the desired CLK frequency.

Since the oscillator circuit output (the same output as for the crystal resonator frequency) appears at the OSC pin, independent use of this output is also possible.

Recommended Oscillator Circuit



When input frequency is 6 to 15 MHz.

$C_1 = C_2 = 33$ pF

(2) Clock Generator Circuit

This circuit generates two clock outputs—CLK obtained by dividing the input external clock or crystal oscillator circuit output by three, and PCLK obtained by halving CLK. CLK and PCLK are generated from the external clock applied to the EFI pin when F/C is at high level, and are generated from the crystal oscillator circuit when at low level.

(3) Reset Circuit

Since a Schmitt trigger circuit is used in the $\overline{RES}$ input, the MSM82C84A-5 can be reset by "power on" by connection to a simple RC circuit. If the 80C86 or 80C88 is used as the CPU in this case, it is necessary to keep the $\overline{RES}$ input at low level for at least 50 μs after V_{CC} reaches the 4.5V level.

(4) Ready Circuit

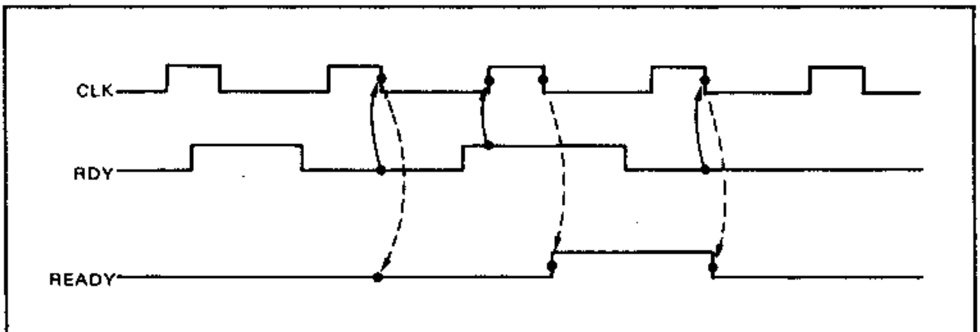
The READY signal generator circuit can be set to synchronization mode by $\overline{ASYNC}$.

(i) When $\overline{ASYNC}$ is at low level

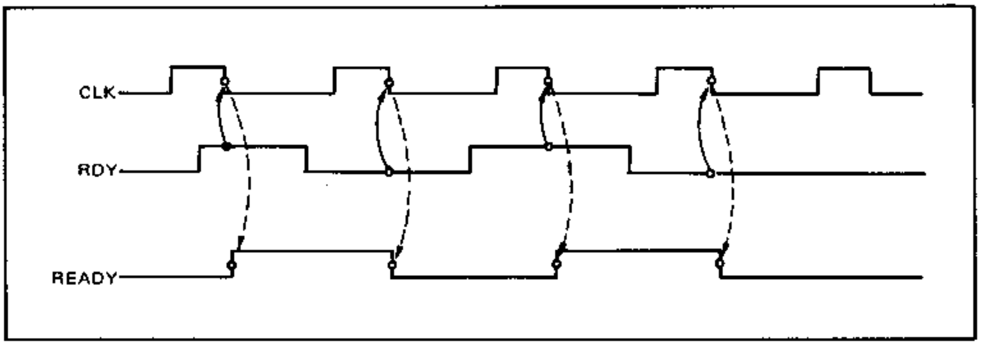
The RDY input is output as the READY signal by double synchronization.

The high-level RDY input is synchronized once by the rising edge of the CLK of the first stage flip-flop (F1 in the circuit diagram), and then synchronized again by the falling edge of the CLK of the next stage flip-flop (F2 in the circuit diagram), resulting in output of a high-level READY output signal (see diagram below).

- The low-level RDY input is synchronized directly by the falling edge of the CLK of the next stage flip-flop, resulting in output of a low-level READY output signal (see diagram below).



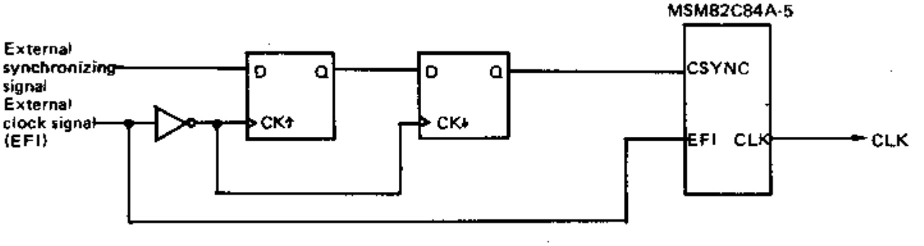
(ii) When $\overline{ASYNC}$ is at high level
The RDY input is output as the READY signal by single synchronization.
- Both low-level and high-level RDY inputs are synchronized by the falling edge of the CLK of the next stage flip-flop, resulting in output of respective low-level and high-level READY output signals (see diagram below).



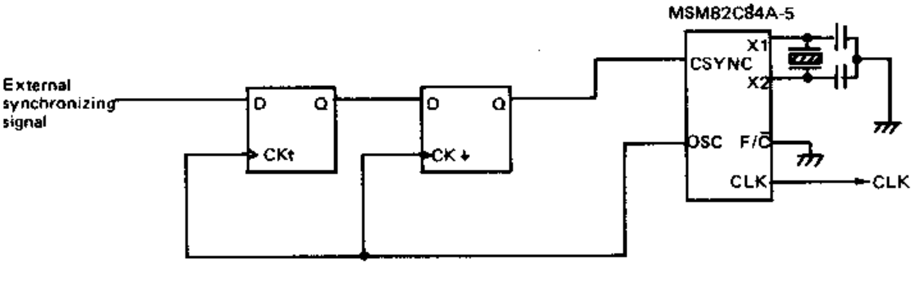
EXAMPLE OF USE (CSYNC)

The 82C84A-5 1/3 frequency divider counter is unsettled when the power is switched on. Therefore, the CSYNC pin has been included to synchronize CLK with another signal. When CSYNC is at high level, both CLK and PCLK are high-level outputs. If CSYNC is then switched to low level, CLK is output from the next input clock rising edge, and is divided by 3.

If CSYNC has not been synchronized with the input clock, use the following circuit to achieve the required synchronization



When an external clock EFI is used as the clock source



When the crystal oscillator is used as the clock source

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OKI semiconductor

MSM82C84A-2RS/GS/JS

CLOCK GENERATOR AND DRIVER

GENERAL DESCRIPTION

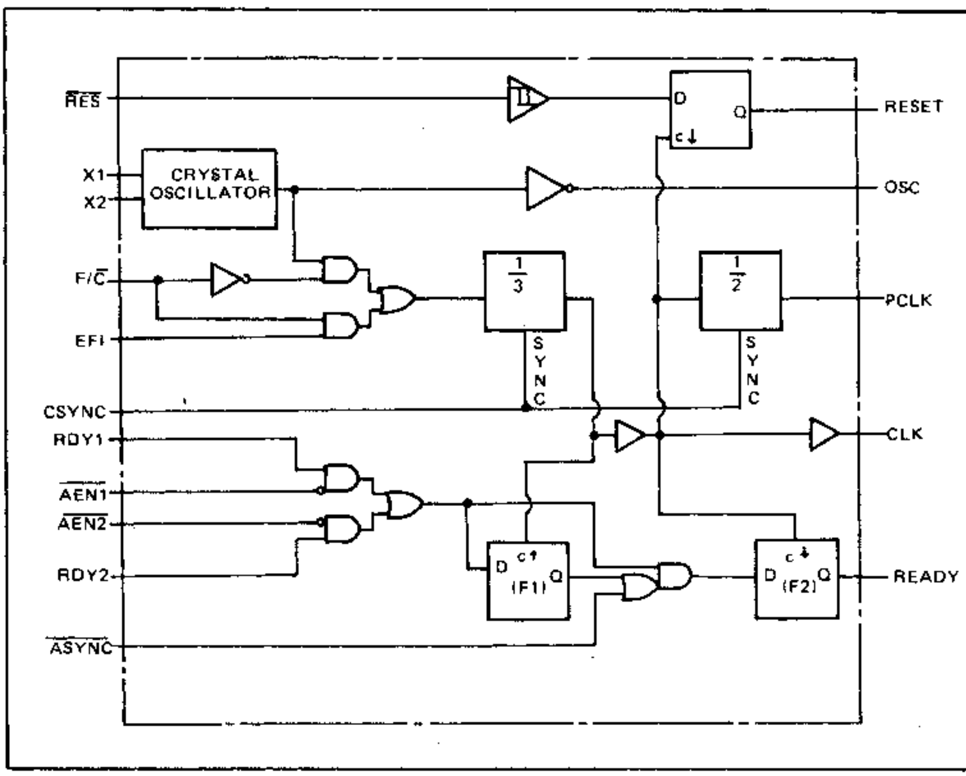
The MSM82C84A-2RS/GS is a clock generator designed to generate MSM80C86 and MSM80C88 system clocks.

Due to the use of silicon gate CMOS technology, standby current is only 40 μA (MAX.), and the power consumption is very low with 16 mA (MAX.) when a 8 MHz clock is generated.

FEATURES

- Operating frequency of 6 to 24 MHz (CLK output 2 to 8 MHz)
- 3μ silicon gate CMOS technology for low power consumption
- Built-in crystal oscillator circuit
- 3V ~ 6V single power supply
- Built-in synchronized circuit for MSM80C86 and MSM80C88 READY and RESET
- TTL compatible
- Built-in Schmitt trigger circuit ($\overline{RES}$ input)
- 18-pin DIP (MSM82C84A-2RS)
- 24-pin flat package (MSM82C84A-2GS)
- 20-pin PLCC (MSM82C84A-2JS)

FUNCTIONAL BLOCK DIAGRAM



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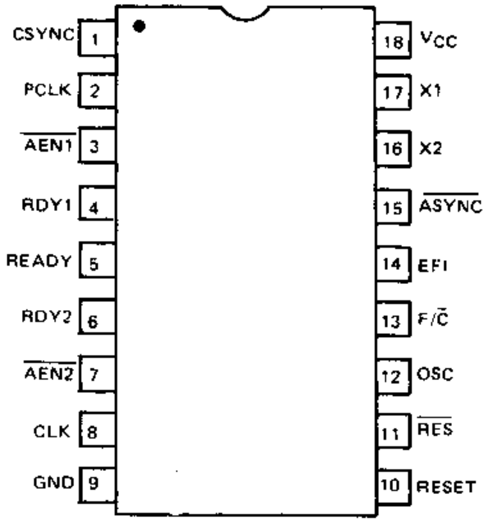
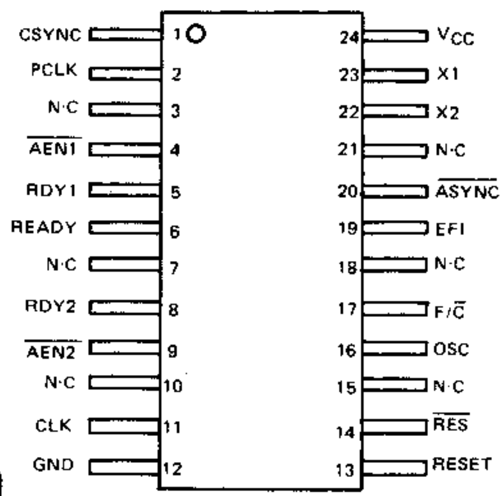
PIN CONFIGURATION

18 Lead Plastic DIP

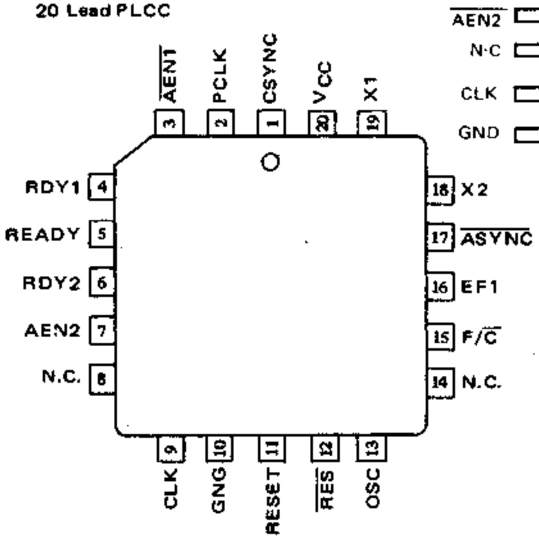


24 Lead Plastic Flat Package



(N·C not connected)

20 Lead PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits		Unit	Conditions
		MSM82C84A-2RS/JS	MSM82C84A-2GS		
Supply Voltage	V_{CC}	−0.5 ~ +7		V	Respect to GND
Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5		V	
Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5		V	
Storage Temperature	Tstg	−55 ~ +150		°C	−
Power Dissipation	P_D	0.8	0.7	W	Ta = 25°C

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	−0.5		+0.8	V
"H" Level Input Voltage (except $\overline{RES}$)	V_{IH}	2.2		V_{CC} +0.5	V
"H" Level Input Voltage ($\overline{RES}$)		0.6*V_{CC}			

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

Parameter	Symbol	MIN	MAX	Unit	Conditions
"L" Level Output Voltage (CLK)	V_{OL}	−	0.4	V	I_{OL} = 4 mA
"L" Level Output Voltage (OTHERS)	V_{OL}	−	0.4	V	I_{OL} = 2.5mA
"H" Level Output Voltage (CLK)	V_{OH}	V_{CC} − 0.4	−	V	I_{OH} = −4mA
"H" Level Output Voltage (OTHERS)	V_{OH}	V_{CC} − 0.4		V	I_{OH} = −1mA
$\overline{RES}$ Input Hysteresis	$V_{IHR} - V_{ILR}$	0.2 * V_{CC}		V	
Input Leak Current (EXCEPT $\overline{ASYNC}$)	I_{LI}	−1	+1	μA	$0 \leq V_{in} \leq V_{CC}$
Input Current ($\overline{ASYNC}$)	I_{LIA}	−100	+10	μA	$0 \leq V_{in} \leq V_{CC}$
Standby Supply Current	I_{CCS}		40	μA	NOTE 1
Operating Supply Current	I_{CC}		16	mA	f = 24MHz, $C_L = 0_{pF}$
Input Capacitance	C_{in}		7	pF	f = 1 MHz

NOTE 1: X1 ≧ V_{CC} − 0.2V, X2 ≦ 0,2V
F/C ≧ V_{CC} − 0.2V, $\overline{ASYNC}$ = V_{CC} or open
VIH ≧ V_{CC} − 0.2V, VIL ≦ 0,2V

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

(1)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
EFI "H" Pulse Width	t_{EHEL}	13		ns	90%−90%	Output load capacitance CLK output C_L = 100pF Others 30pF
EFI "L" Pulse Width	t_{ELEH}	17		ns	10%−10%	
EFI Cycle Time	t_{ELEL}	36		ns		
Crystal Oscillator Frequency		6	24	MHz		
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Active)	t_{R1VCL}	35		ns	$\overline{ASYNC}$ = High	
Set Up Time of RDY1 or RDY2 to CLK Rising Edge (Active)	t_{R1VCH}	35		ns	$\overline{ASYNC}$ = Low	
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Inactive)	t_{R1VCL}	35		ns		
Hold Time of RDY1 or RDY2 to CLK Falling Edge	t_{CLR1X}	0		ns		
Set Up Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{AYVCL}	50		ns		
Hold Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{CLAYX}	0		ns		
Set Up Time of $\overline{AEN1}$ ($\overline{AEN2}$) to RDY1 (RDY2) Rising Edge	t_{A1R1V}	15		ns		
Hold Time of $\overline{AEN1}$ ($\overline{AEN2}$) to CLK Falling Edge	t_{CLA1X}	0		ns		
Set Up Time of CSYNC to EFI Rising Edge	t_{YHEH}	20		ns		
Hold Time of CSYNC to EFI Rising Edge	t_{EHYL}	10		ns		
CSYNC Pulse Width	t_{YHYL}	2 × t_{ELEL}		ns		
Set Up Time of $\overline{RES}$ to CLK Falling Edge	t_{I1HCL}	65		ns		
Hold Time of $\overline{RES}$ to CLK Falling Edge	t_{CLI1H}	20		ns		
Input Rising Edge Time	t_{ILIH}		15	ns		
Input Falling Edge Time	t_{IHIL}		15	ns		

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

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AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = −40 ~ 85°C)

(2)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
CLK Cycle Time	t_{CLCL}	125		ns		Output load capacitance CLK output C_L = 100pF Others 30pF
CLK "H" Pulse Width	t_{CHCL}	$\frac{1}{3}T_{CLCL}+2$		ns		
CLK "L" Pulse Width	t_{CLCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
CLK Rising and Falling Edge Times	t_{CH1CH2} t_{CL2CL1}		10	ns	1.0V−3.5V	
PCLK "H" Pulse Width	t_{PHPL}	$T_{CLCL}-20$		ns		
PCLK "L" Pulse Width	t_{PLPH}	$T_{CLCL}-20$		ns		
Time from READY Falling Edge to CLK Falling Edge	t_{RYLCL}	−8		ns		
Time from READY Rising Edge to CLK Rising Edge	t_{RYHCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
Delay from CLK Falling Edge to RESET Falling Edge	t_{CLIL}		40	ns		
Delay from CLK Falling Edge to PCLK Rising Edge	t_{CLPH}		22	ns		
Delay from CLK Falling Edge to PCLK Falling Edge	t_{CLPL}		22	ns		
Delay from OSC Falling Edge to CLK Rising Edge	t_{OLCH}	−5	22	ns		
Delay from OSC Falling Edge to CLK Falling Edge	t_{OLCL}	2	35	ns		
Output Rising Edge Time (Except CLK)	t_{OLOH}		15	ns	0.8V~2.2V	
Output Falling Edge Time (Except CLK)	t_{OHOL}		15	ns	2.2V~0.8V	

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

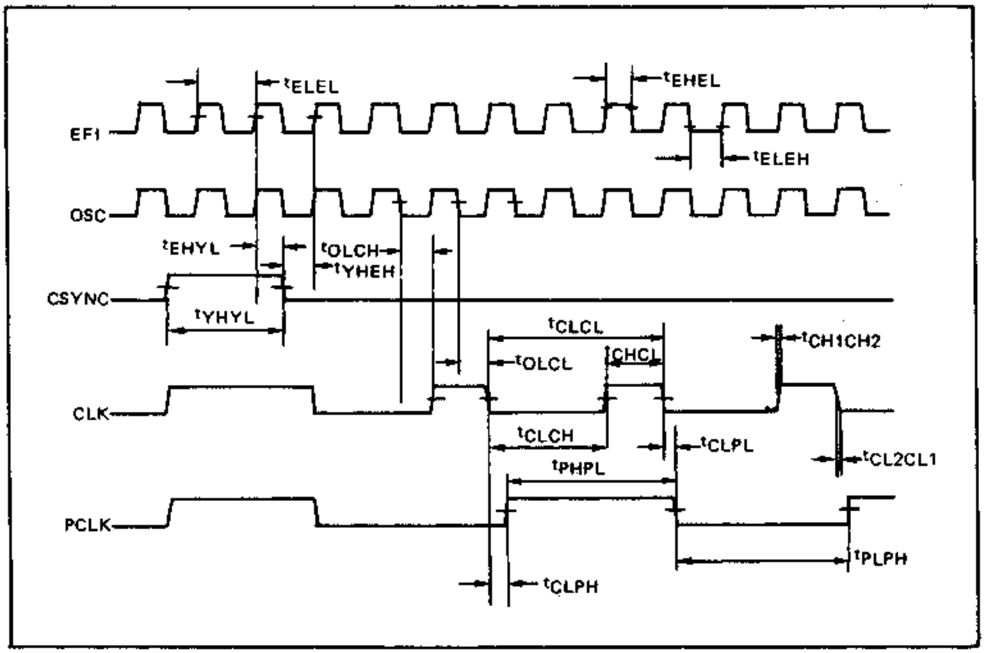
PIN DESCRIPTION

Pin symbol	Name	Input/ output	Function
CSYNC	Clock synchronization singal	Input	Synchronizing signal for output of in-phase CLK signals when more than one MSM82C84A-2 is used. The internal counter is reset when this signal is at high level, and a high level CLK output is generated. The internal counter is subseqently activated and a 33% duty CLK output is generated when this signal is switched to low level. When this signal is used, external synchronization of EFI is necessary. When the internal oscillator is used, it is necessary for this pin to be kept to be low level.
PCLK	Peripheral clock output	Output	This peripheral circuit clock signal is output in a 50% duty cycle at a frequency half that of the clock signal.
$\overline{AEN1}$ $\overline{AEN2}$	Address enable signals	Input	The $\overline{AEN1}$ signal enables $\overline{RDY1}$, and the $\overline{AEN2}$ signal enables RDY2. The respective RDY inputs are activated when the level applied to these pins is low. Although two separate inputs are used in multi-master systems, only the $\overline{AEN}$ which enables the RDY input to be used is to be switched to low level in the case of not using multi-master systems.
RDY1 RDY2	Bus ready signals	Input	Completion of data bus reading and writing by the device connected to the system data bus is indicated when one of these signals is switched to high level. The relevant RDY input is enables only when the corresponding $\overline{AEN}$ is at low level.
READY	Ready output	Output	This signal is obtained by synchronizing the bus ready signal with CLK. This signal is output after guaranteeing the hold time for the CPU in phase with the RDY input.
CLK	Clock output	Output	This signal is the clock used by the CPU and peripheral devices connected to the CPU system data bus. The output waveform is generated in a 33% duty cycle at a frequency 1/3 the oscillating frequency of the crystal oscillator connected to the X1 and X2 pins, or at a frequency 1/3 the EFI input frequency.
$\overline{RES}$	Reset in	Input	This low-level active input is used to generate a CPU reset signal. Since a Schmitt trigger is included in the input circuit for this signal, "power on resetting" can be achieved by connection of a simple RC circuit.
RESET	Reset output	Output	This signal is obtained by CLK synchronization of the input signal applied to $\overline{RES}$ and is output in opposite phase to the $\overline{RES}$ input. This signal is applied to the CPU as the system reset signal.
F/C	Clock select signal	Input	This signal selects the fundamental signal for generation of the CLK signal. The CLK is generated from the crystal oscillator output when this signal is at low level, and from the EFI input signal when at high level.
EFI	External clock signal	Input	The signal applied to this input pin generates the CLK signal when F/$\overline{C}$ is at high level. The frequency of the input signal needs to be three times greater than the desired CLK frequency.
X1, X2	Crystal oscillator connecting pins	Input	Crystal oscillator connections. The crystal oscillator frequency needs to be three times greater than the desired CLK frequency.
OSC	Crystal resonator output	Output	Crystal oscillator output. This output frequency is the same as the oscillating frequency of the oscillator connected to the X1 and X2 pins. As long as a Xtal oscillator is connected to the X1 and X2 pins, this output signal can be obtained independently even if F/C is set to high level to enable the EFI input to be used for CLK generation purposes.

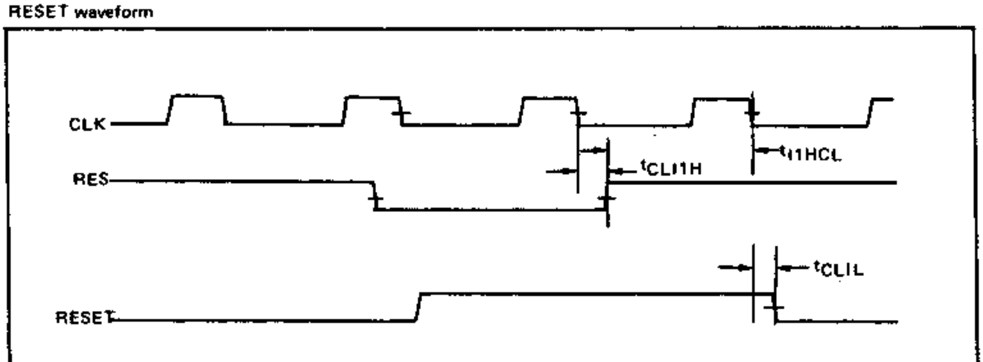
Pin symbol	Name	Input/ output	Function
$\overline{ASYNC}$	Ready synchronization select signal	Input	Signal for selection of the synchronization mode of the READY signal generator circuit. When this signal is at low level, the READY signal is generated by double synchronization. And When at high level, the READY signal is generated by single synchronization. This pin is equipped with internal pull-up resister.
V_{CC}			+5V power supply
GND			GND

TIMING CHART

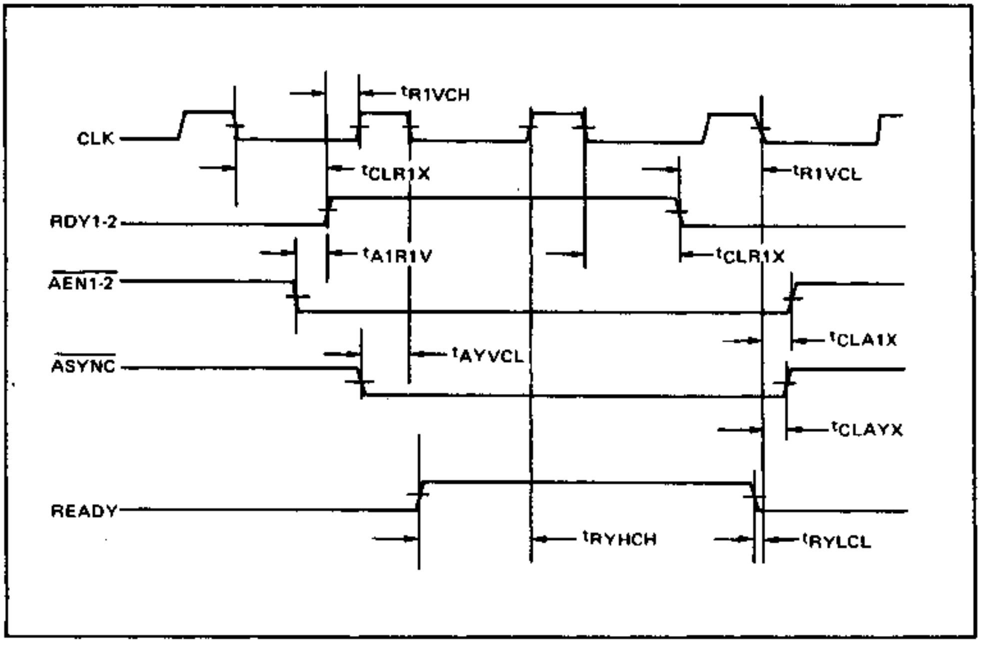
CLK · PCLK · OSC waveforms



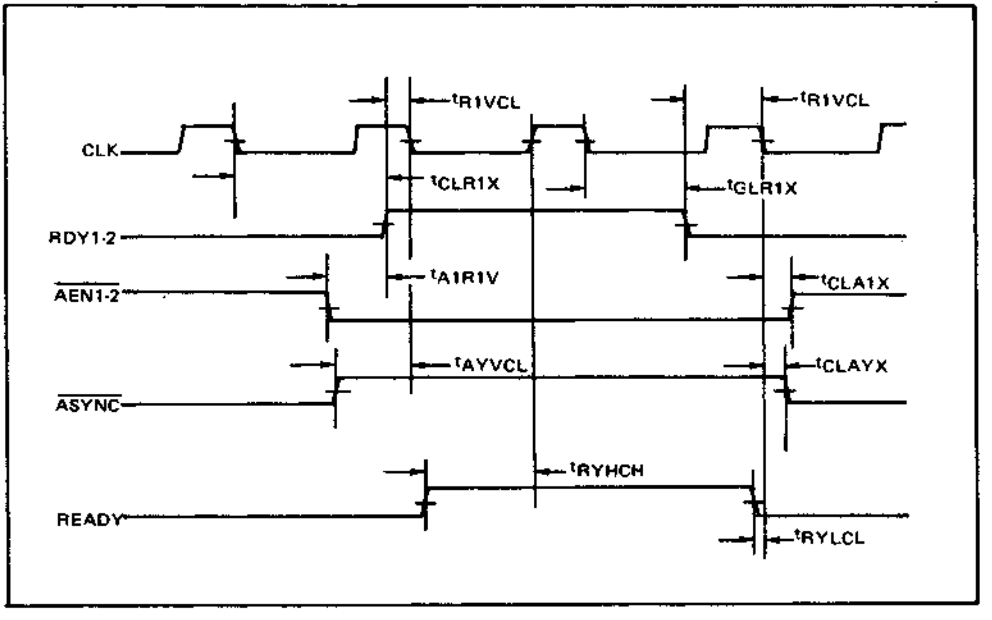
RESET waveform



READY waveform ($\overline{ASYNC}$ = L)



READY waveform ($\overline{ASYNC}$ = H)



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DESCRIPTION OF OPERATION

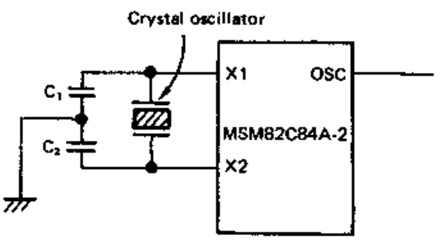
(1) Oscillator Circuit

The MSM82C84A-5 internal oscillator circuit can be driven by connecting a crystal oscillator to the X1 and X2 pins.

The frequency of the crystal oscillator in this case needs to be three times greater than the desired CLK frequency.

Since the oscillator circuit output (the same output as for the crystal resonator frequency) appears at the OSC pin, independent use of this output is also possible.

Recommended Oscillator Circuit



When input frequency is 6 to 24 MHz.

$C_1 = C_2 = 33$ pF

(2) Clock Generator Circuit

This circuit generates two clock outputs—CLK obtained by dividing the input external clock or crystal oscillator circuit output by three, and PCLK obtained by halving CLK. CLK and PCLK are generated from the external clock applied to the EFI pin when F/C is at high level, and are generated from the crystal oscillator circuit when at low level.

(3) Reset Circuit

Since a Schmitt trigger circuit is used in the $\overline{RES}$ input, the MSM82C84A-2 can be reset by "power on" by connection to a simple RC circuit. If the 80C86 or 80C88 is used as the CPU in this case, it is necessary to keep the $\overline{RES}$ input at low level for at least 50 μs after V_{CC} reaches the 4.5V level.

(4) Ready Circuit

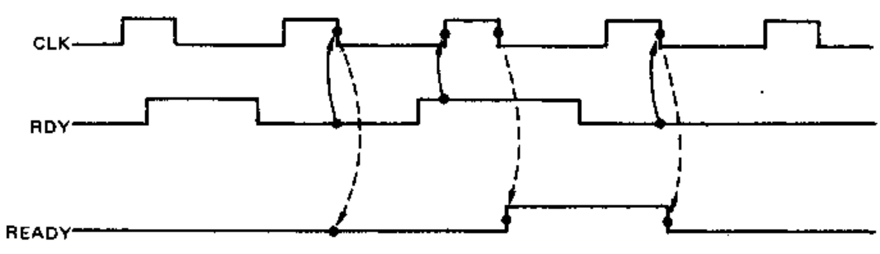
The READY signal generator circuit can be set to synchronization mode by $\overline{ASYNC}$.

(i) When $\overline{ASYNC}$ is at low level

The RDY input is output as the READY signal by double synchronization.

The high-level RDY input is synchronized once by the rising edge of the CLK of the first stage flip-flop (F1 in the circuit diagram), and then synchronized again by the falling edge of the CLK of the next stage flip-flop (F2 in the circuit diagram), resulting in output of a high-level READY output signal (see diagram below).

- The low-level RDY input is synchronized directly by the falling-edge of the CLK of the next stage flip-flop, resulting in output of a low-level READY output signal (see diagram below).



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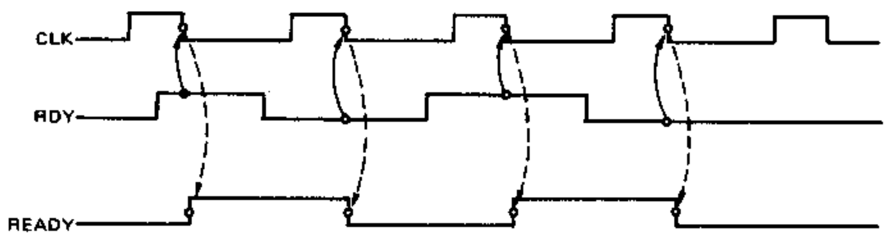
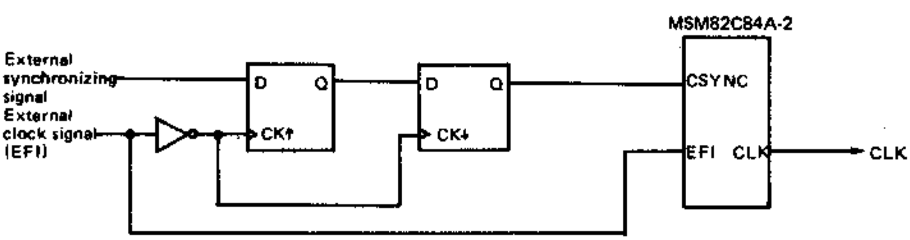
(ii) When $\overline{ASYNC}$ is at high level
The RDY input is output as the READY signal by single synchronization.
- Both low-level and high-level RDY inputs are synchronized by the falling edge of the CLK of the next stage flip-flop, resulting in output of respective low-level and high-level READY output signals (see diagram below).



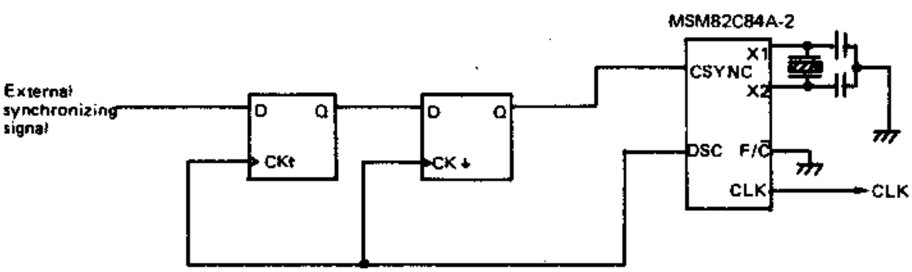
EXAMPLE OF USE (CSYNC)

The 82C84A-2 1/3 frequency divider counter is unsettled when the power is switched on. Therefore, the CSYNC pin has been included to synchronize CLK with another signal. When CSYNC is at high level, both CLK and PCLK are high-level outputs. If CSYNC is then switched to low level, CLK is output from the next input clock rising edge, and is divided by 3.

If CSYNC has not been synchronized with the input clock, use the following circuit to achieve the required synchronization



When an external clock EFI is used as the clock source



When the crystal oscillator is used as the clock source

OKI semiconductor

MSM82C88AS/GS

BUS CONTROLLER

GENERAL DESCRIPTION

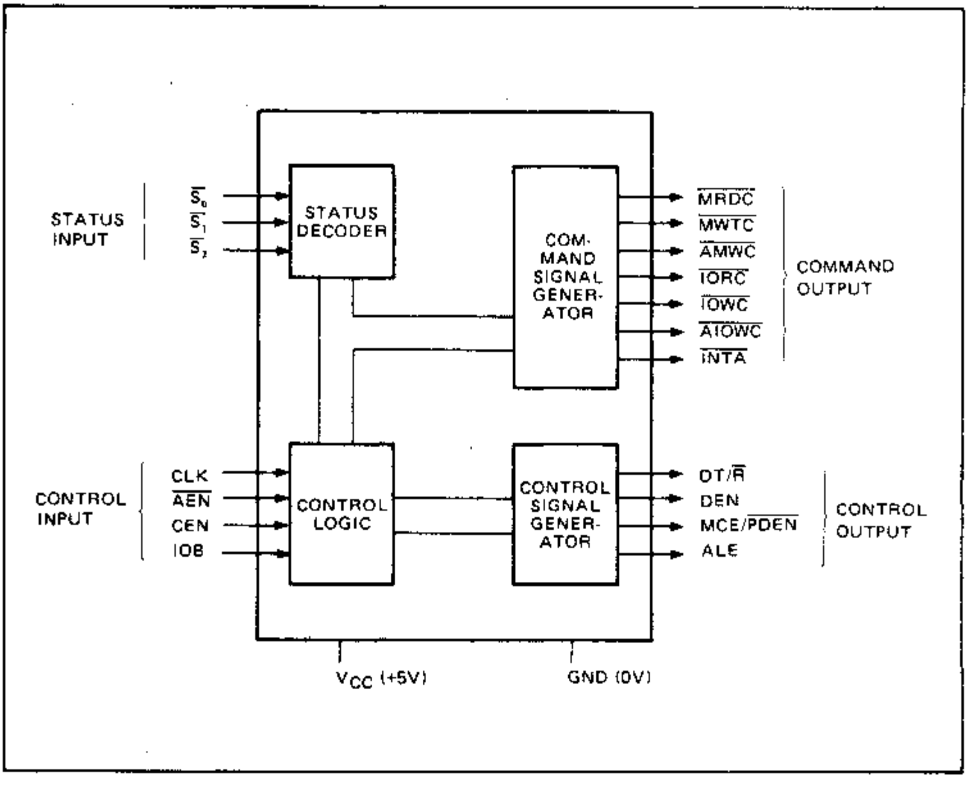
The MSM82C88 is a bus controller for the MSM80C86 and the MSM80C88 CPUs. Based on silicon gate CMOS technology, a low-power 16-bit microprocessor system can be realized.

The MSM82C88 generates commands control timing signals on reception of status signals from the CPU.

FEATURES

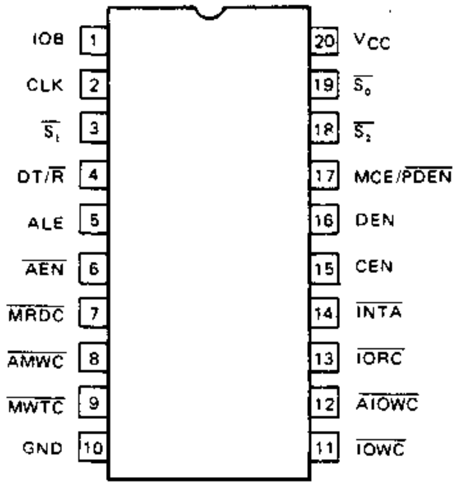
- Silicon gate CMOS technology for low power consumption
- 3 to 6V wide voltage range and single power supply
- −40 to 85°C wide guaranteed operating temperature range
- Advanced write control output
- Three-state command output driver
- System bus mode & I/O bus mode
- 20-pin DIP (MSM82C88AS)
- 24-pin flat package (MSM82C88GS)

CIRCUIT CONFIGURATION

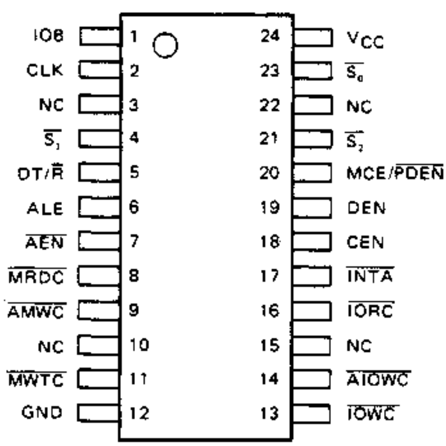


PIN CONFIGURATION

MSM82C88AS (top view)
20-lead DIP



MSM82C88GS (top view)
24-lead plastic flat package



Note: NC pin must not be connected.

5

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM82C88AS	MSM82C88GS	
Power Supply Voltage	V_{CC}	With respect to GND	−0.5 ~ +7		V
Input Voltage	V_{IN}		−0.5 ~ V_{CC} +0.5		V
Output Voltage	V_{OUT}		−0.5 ~ V_{CC} +0.5		V
Storage Temperature	Tstg	—	−55 ~ 150		°C
Power Dissipation	P_D	Ta = 25°C	1.1	0.7	W

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL1}	−0.3	–	+0.8	V
"H" Input Voltage	V_{IH1}	3.0	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL2}	−0.3	–	+0.8	V
"H" Input Voltage	V_{IH2}	2.2	–	V_{CC} +0.3	V

Note: V_{IL1} and V_{IH1} are input voltages for CLK, $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$.
V_{IL2} and V_{IH2} are input voltages for $\overline{AEN}$, CEN, and IOB.

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40°C to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
"L" Output Voltage	V_{OL}	Command output I_{OL} = 12mA	–	–	0.45	V	
		Control output I_{OL} = 8mA	–	–	0.45	V	
"H" Output Voltage	V_{OH}	Command output I_{OH} = −5mA	3.7	–	–	V	
		Control output I_{OH} = −1mA	3.7	–	–	V	
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	−10	–	10	μA	Note 1
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	−10	–	10	μA	
Status Input Current	I_{LIS}	$0 \leq V_{IN} \leq V_{CC}$	−100	–	10	μA	Note 2
Operation Power Supply Current	I_{CCO}	C_L = 0pF t_{CLCL} = 200ns	–	–	10	mA	
Standby Power Supply Current	I_{CCS}	Note 3	–	–	100	μA	

Note 1. This input leak current is the leak current on input pins except status inputs ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$).

Note 2. The status input leak current is the leak current at the status inputs ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$).

Note 3. The measuring conditions for the standby power supply current include the $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ status inputs being at V_{CC} potential, and the other inputs being at V_{CC} or GND. All output pins are left open.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40°C to +85°C)

Timing conditions

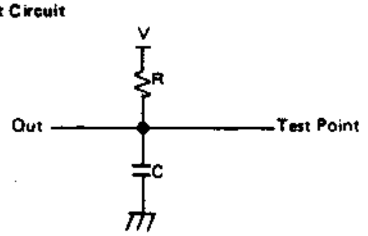
Parameter	Symbol	Min.	Max.	Unit
Clock Cycle	t_{CLCL}	200	–	nS
Clock Low Time	t_{CLCH}	118	–	nS
Clock High Time	t_{CHCL}	65	–	nS
Status Active Setup Time	t_{SVCH}	35	–	nS
Status Inactive Hold Time	t_{CHSV}	10	–	nS
Status Inactive Setup Time	t_{SHCL}	35	–	nS
Status Active Hold Time	t_{CLSH}	10	–	nS

Timing response

Parameter	Symbol	Min.	Max.	Unit	Test Circuit	Remarks
Delay from CLK Leading Edge to DEN, $\overline{PDEN}$ Active	t_{CVNV}	5	45	nS	4	
Delay from CLK Trailing Edge to DEN, $\overline{PDEN}$ Inactive	t_{CVNX}	5	45	nS	4	
Delay from CLK Trailing to ALE Active	t_{CLLH}	–	35	nS	4	
Delay from CLK Trailing Edge to MCE Active	t_{CLMCH}	–	35	nS	4	
Delay from Status Input Falling Edge to ALE Active	t_{SVLH}	–	35	nS	4	
Delay from Status Input Falling Edge to MCE Active	t_{SVMCH}	–	35	nS	4	
Delay from CLK Leading Edge to ALE Inactive	t_{CHLL}	4	35	nS	4	
Delay from CLK Trailing Edge to Command Output Active	t_{CLML}	5	45	nS	3	
Delay from CLK Trailing Edge to Command Output Inactive	t_{CLMH}	5	45	nS	3	
Delay from CLK Leading Edge to DT/$\overline{R}$ Active	t_{CHDTL}	–	50	nS	4	
Delay from CLK Leading Edge to DT/$\overline{R}$ Inactive	t_{CHDTH}	–	35	nS	4	
Delay from $\overline{AEN}$ Leading Edge to Command Enable	t_{AELCH}	–	45	nS	2	
Delay from $\overline{AEN}$ Trailing Edge to Command Disable	t_{AEHCZ}	–	40	nS	1	
Delay from $\overline{AEN}$ Leading Edge to Command Output Active	t_{AELCV}	90	250	nS	3	
Delay from $\overline{AEN}$ to DEN	t_{AEVNV}	–	35	nS	4	
Delay from CEN to DEN, $\overline{PDEN}$	t_{CEVNV}	–	35	nS	4	
Delay from CEN to Command Output	t_{CELRH}	–	t_{CLML}+20	nS	3	
Output Rise Time	t_{OLOH}	–	20	nS	3, 4	From 0.8V to 2.2V
Output Fall Time	t_{OHOL}	–	12	nS	3, 4	From 2.2V to 0.8V

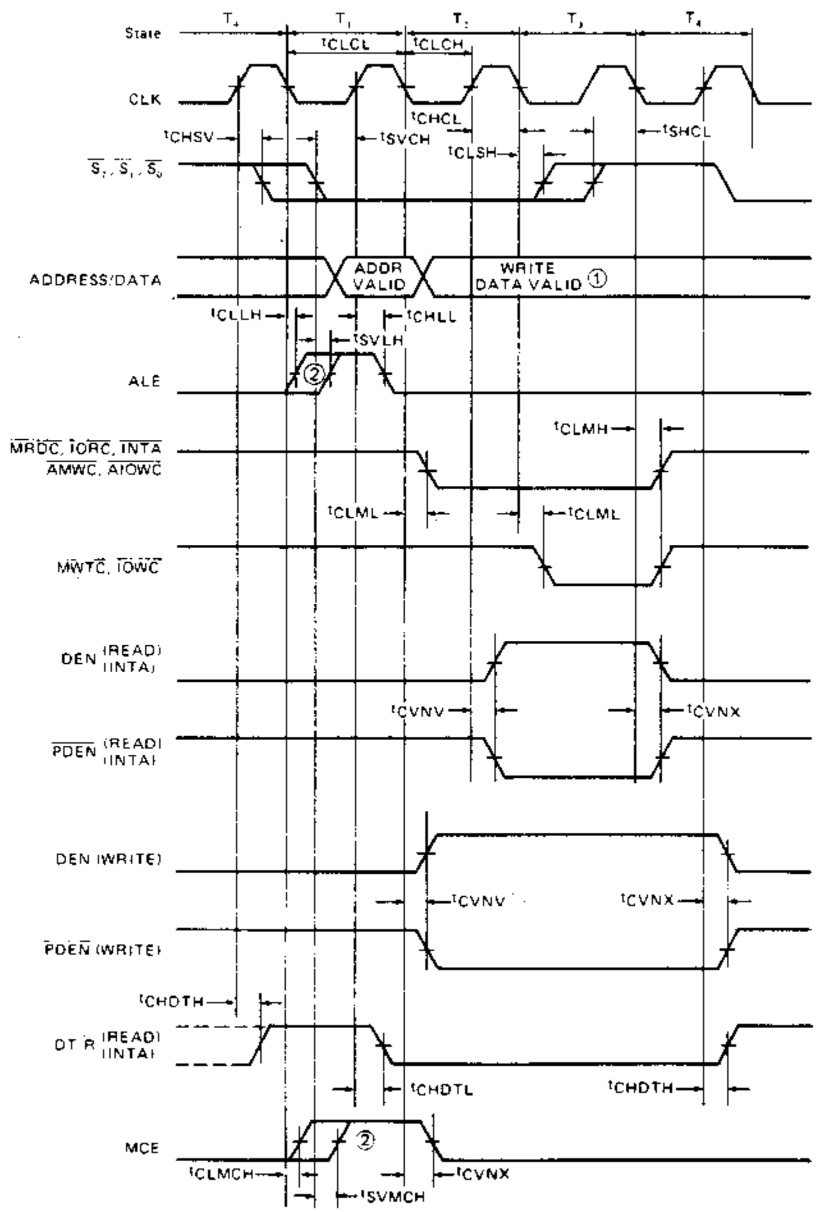
Note: AC timing measurements are made at 1.5V for both logic "1" and "0".
Input rise and fall times are
5 ± 2 nS between 0.8V and 2.2V for $\overline{AEN}$, CEN and IOB.
8 ± 2 nS between 0.8V and 3.0V for $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ and CLK.

Test Circuit



Test Circuit	$V_{(V)}$	$R_{(\Omega)}$	$C_{(PF)}$
1	1.5	180	50
2	1.5	300	150
3	2.74	190	150
4	3.34	360	80

TIME CHARTS



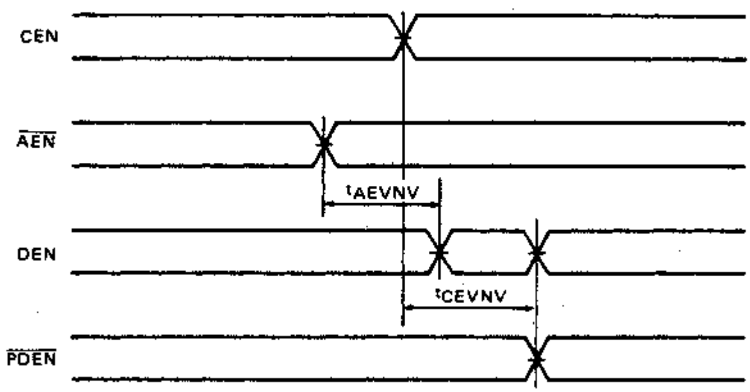
Note 1. The ADDRESS/DATA bus signal is shown for reference purposes.

Note 2. The ALE and MCE leading edges are synchronized with the falling edge of CLK or status going active, whichever occurs last

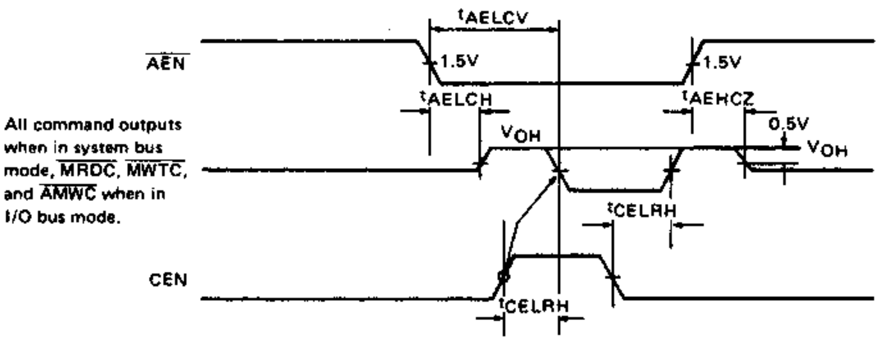
Note 3. All timing measurements are made at 1.5V unless specified otherwise

5

DEN, $\overline{PDEN}$ Timing



$\overline{AEN}$ Timing



Note: To control the command and control signal outputs, CEN must be switched to low level before T_2

PIN DESCRIPTION

Pin Name	Input/output	Function
$\overline{S_0}, \overline{S_1}, \overline{S_2}$	Input	These pins are input pins for status signals ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$), output from the CPU (MSM80C86, 80C88). The MSM82C88 generates commands and control signals after decoding these status signals. Since these pins are connected to an internal pull-up resistor, they are set to high level when the CPU status output is at high impedance.
CLK	Input	This pin is the input pin for clock signal output from the clock generator (MSM82C84A). The timing of all MSM82C88 output signals is controlled by this clock signal.
ALE	Output	Strobe signal for latching output address from the CPU to address latch. Address latching occurs on the trailing edge of ALE.
DEN	Output	Control signal for setting the data bus transceiver to data enable. The local bus or system bus transceiver is enabled when this signal is high. DEN is switched to low when the CEN input is low.
DT/$\overline{R}$	Output	Control of the direction of data flow in the data bus transceiver. When the CPU is switched to write mode, this signal is high, and when switched to read mode, this signal is low.
$\overline{AEN}$	Input	Address enable signal. • IOB = L (SYSTEM BUS MODE) When the $\overline{AEN}$ input is switched to high level, all command outputs are switched to high impedance status. • IOB = H (I/O BUS MODE) When the $\overline{AEN}$ input is switched to high level, only the $\overline{MRDC}$, $\overline{MWTC}$, and $\overline{AMWC}$ command outputs are switched to high impedance status. When $\overline{AEN}$ is switched from high to low level, high impedance command outputs are not switched to active status (low level) for at least 90 nS, irrespective of the IOB input status.
CEN	Input	Command enable signal. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to inactive status when a low level input is applied to CEN. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to active status when a high level input is applied to CEN.
IOB	Input	I/O bus mode signal. The MSM82C88 is switched to I/O bus mode when a high level input is applied to IOB, and to system bus mode when a low level input is applied.
$\overline{IOWC}$	3-state output	This pin is active-low, and three-state output. This signal is for writing data into the I/O device.
$\overline{AIOWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into I/O devices like the I/O write command ($\overline{IOWC}$), it is made active one clock earlier than $\overline{IOWC}$.
$\overline{IORC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from I/O devices.
$\overline{MWTC}$	3-state output	This pin is active-low and three-state output. This signal is for writing data into memory.
$\overline{AMWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into memory like the memory write command ($\overline{MWTC}$), it is made active one cycle earlier than $\overline{MWTC}$.
$\overline{MRDC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from memory.
$\overline{INTA}$	3-state output	This pin is active-low and three-state output. This signal informs the interrupt controller that the interrupt has been accepted, and then requests output of a vector address onto the data bus.

5

Pin Name	Input/output	Function
MCE/$\overline{PDEN}$	Output	This pin has two functions. MCE (IOB = Low) master cascade enable function. This is an active-high signal and is used to enable a slave PIC (priority interrupt controller) to read the cascade address output on the data bus by the master PIC during an interrupt sequence. $\overline{PDEN}$ (IOB = High) peripheral data enable function. This is a an active-low signal and is used to enable the data bus transceiver on the I/O bus.

FUNCTION

Command Logic

The command output is decided by decoding status signals ($\overline{s_0}$, $\overline{s_1}$, $\overline{s_2}$) output from the CPU.

These status signals have the following meanings.

$\overline{s_2}$	$\overline{s_1}$	$\overline{s_0}$	CPU status	Command output
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	I/O read	$\overline{IORC}$
0	1	0	I/O write	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	–
1	0	0	Instruction fetch	$\overline{MRDC}$
1	0	1	Memory read	$\overline{MRDC}$
1	1	0	Memory write	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	–

I/O Bus Mode (IOB = High)

When an I/O access status signal is received from the CPU in I/O bus mode, one of the I/O commands ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) corresponding to the status signal becomes active irrespective of the $\overline{AEN}$ status. At the same time, the $\overline{PDEN}$ and DT/$\overline{R}$ outputs which control the data bus transceiver are generated.

As in system bus mode, the memory commands ($\overline{MRDC}$, $\overline{MWTC}$, and $\overline{AMWC}$) are not switched to low level for at least 90 ns after $\overline{AEN}$ is switched to low level.

System Bus Mode (IOB = Low)

When the bus is usable, the MSM82C88 is enabled by the $\overline{AEN}$ signal from the bus arbiter. Consequently, no command output becomes active unless the $\overline{AEN}$ signal becomes low. Also note that there is a delay of at least 90 ns before any command output becomes active after the $\overline{AEN}$ signal is switched to low level.

System bus mode is used when more than one CPU is connected to a single bus, and the bus I/O, memory, etc. are used in common.

Command Outputs

The advanced write commands ($\overline{AIOWC}$ and $\overline{AMWC}$) become active one cycle earlier than normal write commands ($\overline{IOWC}$ and $\overline{MWTC}$). This prevents the CPU from being switched to an additional period of wait status.

$\overline{INTA}$ (interrupt acknowledge) is output during the interrupt acknowledge cycle in the same way as $\overline{MRDC}$ in the read cycle. The purpose of this signal is to inform the device which has requested the interrupt that the interrupt has been accepted, and requests a vector address output on the data bus.

$\overline{MRDC}$ – Memory read command
$\overline{MWTC}$ – Memory write command
$\overline{IORC}$ – I/O read command
$\overline{IOWC}$ – I/O write command
$\overline{AMWC}$ – Advanced memory write command
$\overline{AIOWC}$ – Advanced I/O write command
$\overline{INTA}$ – Interrupt acknowledge

Control Output

The control output signals are DEN (Data Enable), DT/$\overline{R}$ (Transmit/Receive), and MCE/$\overline{PDEN}$ (Master Cascade Enable/Peripheral Data Enable).

The DEN signal enables the local bus or system bus, when it is high.

The DT/$\overline{R}$ signal determines the direction of the data on the local bus or system bus.

The function of the MCE/$\overline{PDEN}$ pin is switched according to IOB. The $\overline{PDEN}$ function is selected in I/O bus mode (IOB = high) to provide the I/O or peripheral/system bus data enable signal. When the MCE function is selected in system bus mode (IOB = low), the MCE signal is active (high) level at an interrupt acknowledge status.

The MCE signal is used when a master and slave interrupt controller exists in the system.

ALE (Address Latch Enable)

ALE is generated in each machine cycle to latch the current address to the address latch.

CEN (Command Enable)

This signal is used to enable command outputs. All command outputs become inactive if a low level input is applied to the CEN pin.

5

PRELIMINARY

OKI semiconductor

MSM82C88-2RS/GS/JS

BUS CONTROLLER

GENERAL DESCRIPTION

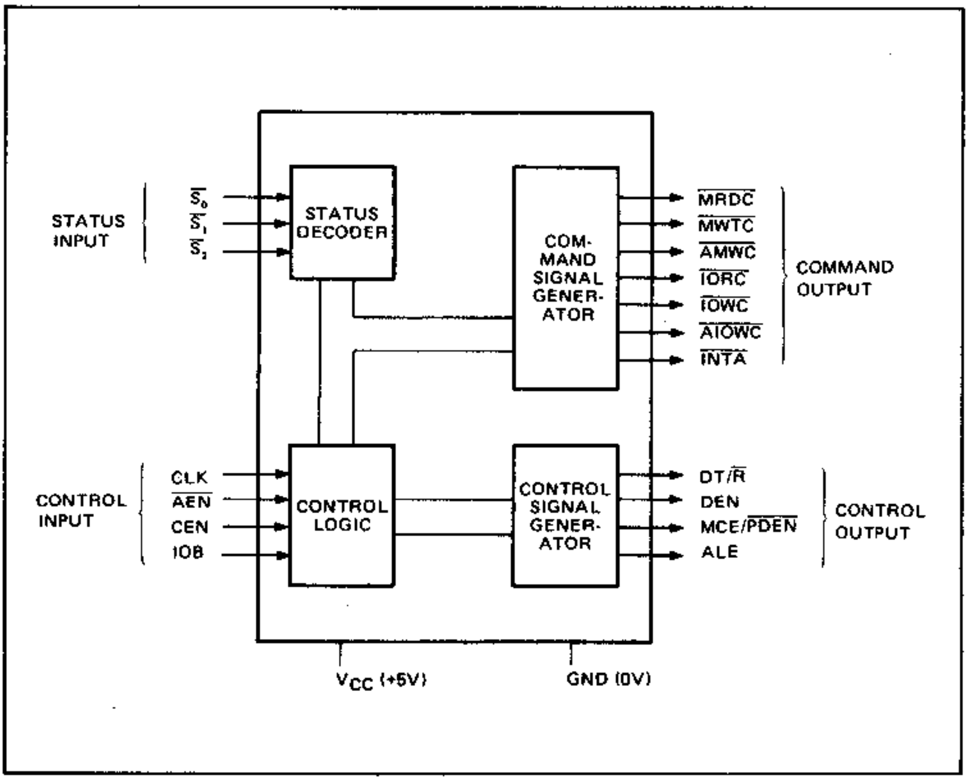
The MSM82C88 is a bus controller for the MSM80C86 and the MSM80C88 CPUs. Based on silicon gate CMOS technology, a low-power 16-bit microprocessor system can be realized.

The MSM82C88 generates commands contol timing signals on reception of status signals from the CPU.

FEATURES

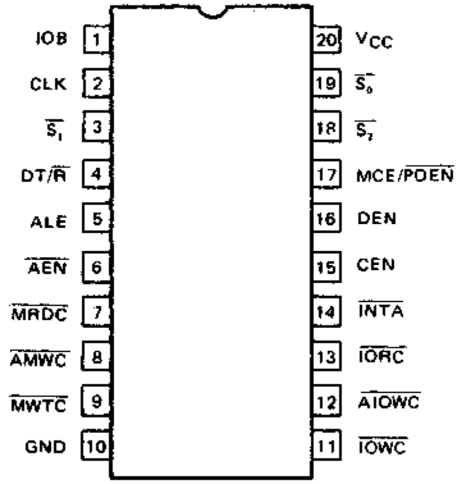
- Silicon gate CMOS technology for low power consumption
- 3 to 6V wide voltage range and single power supply
- −40 to 85°C wide guaranteed operating temperature range
- Advanced write control output
- Three-state command output driver
- System bus mode & I/O bus mode
- 20-pin DIP (MSM82C88-2RS)
- 24-pin flat package (MSM82C88-2GS)
- 20-pin PLCC (MSM82CC88-2JS)

CIRCUIT CONFIGURATION

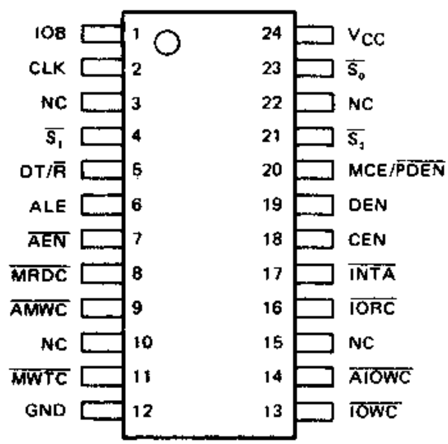


PIN CONFIGURATION

MSM82C88-2RS (Top View)
20-lead DIP

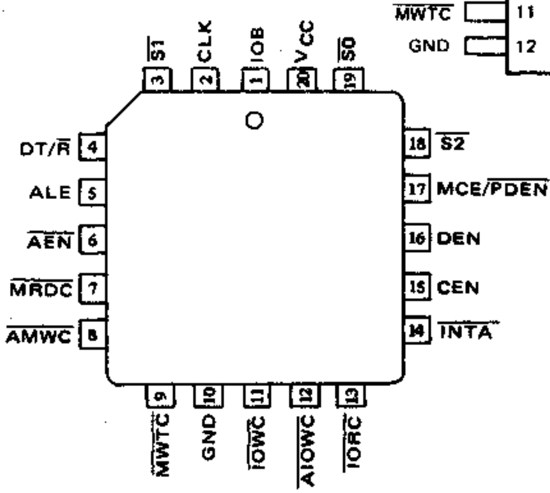


MSM82C88-2GS (Top View)
24-lead plastic flat package



Note: NC pin must not be connected.

MSM82C88-2JS (Top View)
20 Pin PLCC PACKAGE



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM82C88-2RS/JS	MSM82C88-2GS	
Power Supply Voltage	V_{CC}	With respect to GND	−0.5 ~ +7		V
Input Voltage	V_{IN}		−0.5 ~ V_{CC} +0.5		V
Output Voltage	V_{OUT}		−0.5 ~ V_{CC} +0.5		V
Storage Temperature	Tstg	–	−55 ~ 150		°C
Power Dissipation	P_D	Ta = 25°C	0.7	0.7	W

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Operating Temperature	T_{OP}	−40 ~ 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL1}	−0.3	–	+0.8	V
"H" Input Voltage	V_{IH1}	3.0	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL2}	−0.3	–	+0.8	V
"H" Input Voltage	V_{IH2}	2.2	–	V_{CC} +0.3	V

Note: V_{IL1} and V_{IH1} are input voltages for CLK, $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$.
V_{IL2} and V_{IH2} are input voltages for $\overline{AEN}$, CEN, and IOB.

5

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40°C to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
"L" Output Voltage	V_{OL}	Command output I_{OL} = 20mA	−	−	0.5	V	
		Control output I_{OL} = 8mA	−	−	0.45	V	
"H" Output Voltage	V_{OH}	Command output I_{OH} = −8mA	3.7	−	−	V	
		Control output I_{OH} = −4mA	3.7	−	−	V	
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$	−10	−	10	μA	Note 1
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$	−10	−	10	μA	
Status Input Current	I_{LIS}	$0 \leq V_{IN} \leq V_{CC}$	−100	−	10	μA	Note 2
Operation Power Supply Current	I_{CCO}	C_L = 0pF t_{CLCL} = 200ns	−	−	10	mA	
Standby Power Supply Current	I_{CCS}	Note 3	−	−	100	μA	

Note 1. This input leak current is the leak current on input pins except status inputs ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$).

Note 2. The status input leak current is the leak current at the status inputs ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$).

Note 3. The measuring conditions for the standby power supply current include the $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ status inputs being at V_{CC} potential, and the other inputs being at V_{CC} or GND. All output pins are left open.

AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40°C to +85°C)

Timing conditions

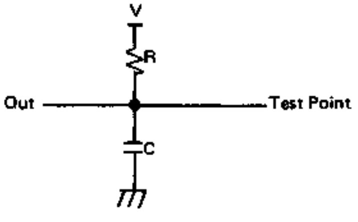
Parameter	Symbol	Min.	Max.	Unit
Clock Cycle	t_{CLCL}	125	−	nS
Clock Low Time	t_{CLCH}	66	−	nS
Clock High Time	t_{CHCL}	40	−	nS
Status Active Setup Time	t_{SVCH}	35	−	nS
Status Inactive Hold Time	t_{CHSV}	10	−	nS
Status Inactive Setup Time	t_{SHCL}	35	−	nS
Status Active Hold Time	t_{CLSH}	10	−	nS

Timing response

Parameter	Symbol	Min.	Max.	Unit	Test Circuit	Remarks
Delay from CLK Leading Edge to DEN, $\overline{PDEN}$ Active	t_{CVNV}	5	45	nS	4	
Delay from CLK Trailing Edge to DEN, $\overline{PDEN}$ Inactive	t_{CVNX}	5	45	nS	4	
Delay from CLK Trailing to ALE Active	t_{CLLH}	–	25	nS	4	
Delay from CLK Trailing Edge to MCE Active	t_{CLMCH}	–	25	nS	4	
Delay from Status Input Falling Edge to ALE Active	t_{SVLH}	–	25	nS	4	
Delay from Status Input Falling Edge to MCE Active	t_{SVMCH}	–	30	nS	4	
Delay from CLK Leading Edge to ALE Inactive	t_{CHLL}	4	25	nS	4	
Delay from CLK Trailing Edge to Command Output Active	t_{CLML}	5	35	nS	3	
Delay from CLK Trailing Edge to Command Output Inactive	t_{CLMH}	5	45	nS	3	
Delay from CLK Leading Edge to DT/$\overline{R}$ Active	t_{CHDTL}	–	50	nS	4	
Delay from CLK Leading Edge to DT/$\overline{R}$ Inactive	t_{CHDTH}	–	30	nS	4	
Delay from $\overline{AEN}$ Leading Edge to Command Enable	t_{AELCH}	–	40	nS	2	
Delay from $\overline{AEN}$ Trailing Edge to Command Disable	t_{AEHCZ}	–	40	nS	1	
Delay from $\overline{AEN}$ Leading Edge to Command Output Active	t_{AELCV}	100	250	nS	3	
Delay from $\overline{AEN}$ to DEN	t_{AEVNV}	–	35	nS	4	
Delay from CEN to DEN, $\overline{PDEN}$	t_{CEVNV}	–	35	nS	4	
Delay from CEN to Command Output	t_{CELRH}	–	$t_{CLML}+10$	nS	3	
Output Rise Time	t_{OLOH}	–	15	nS	3, 4	From 0.8V to 2.2V
Output Fall Time	t_{OHOL}	–	15	nS	3, 4	From 2.2V to 0.8V

Note: AC timing measurements are made at 1.5V for both logic "1" and "0".
Input rise and fall times are
5 ± 2 nS between 0.8V and 2.2V for $\overline{AEN}$, CEN and IOB.
8 ± 2 nS between 0.8V and 3.0V for $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ and CLK.

Test Circuit



Test Circuit	V(V)	R(Ω)	C(PF)
1	1.5	187	50
2	1.5	187	150
3	2.29	91	150
4	2.13	220	80

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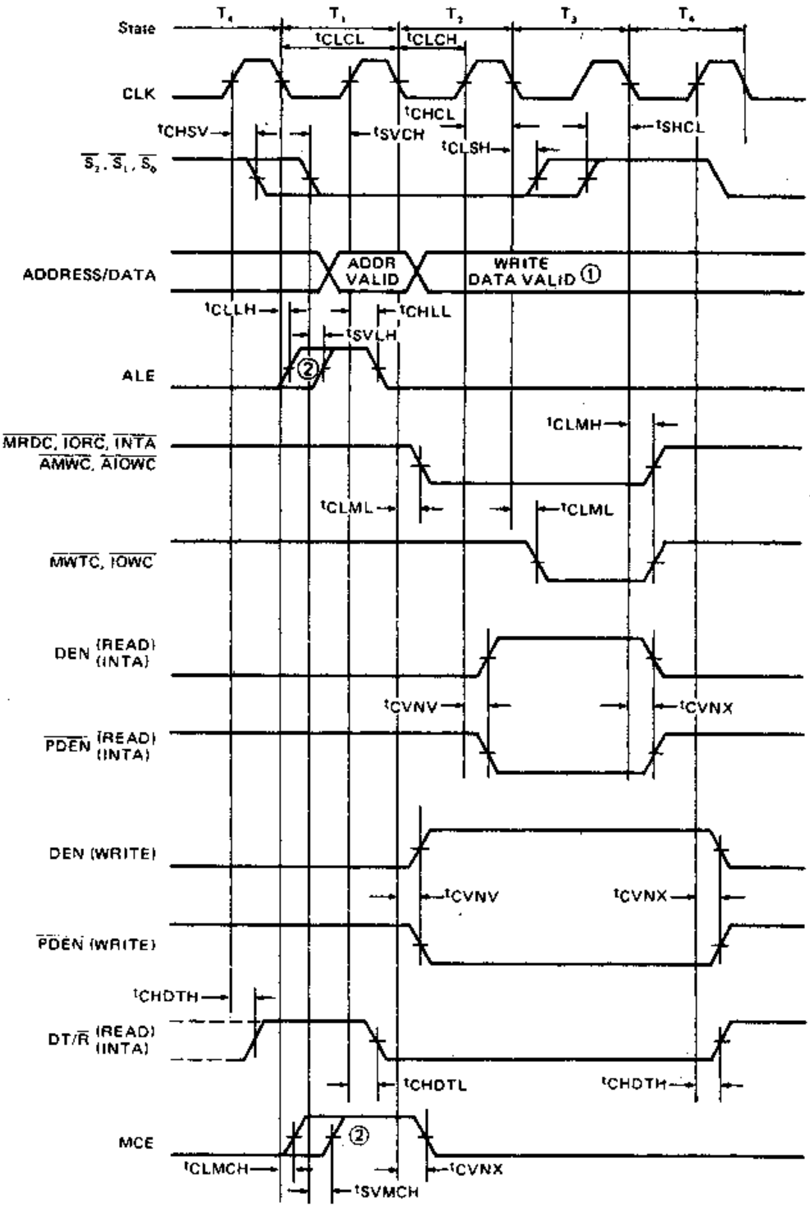
TIME CHARTS

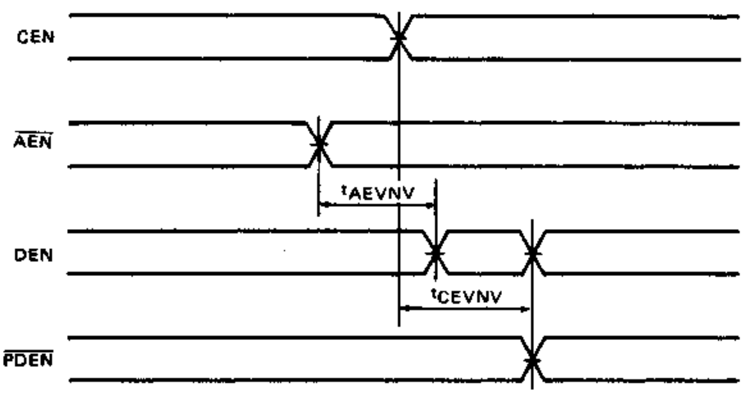


Note 1. The ADDRESS/DATA bus signal is shown for reference purposes.

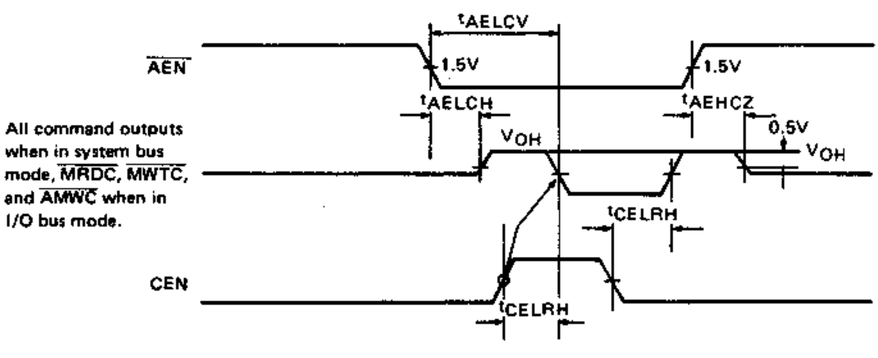
Note 2. The ALE and MCE leading edges are synchronized with the falling edge of CLK or status going active, whichever occurs last.

Note 3. All timing measurements are made at 1.5V unless specified otherwise.

DEN, $\overline{PDEN}$ Timing



$\overline{AEN}$ Timing



Note: To control the command and control signal outputs, CEN must be switched to low level before T_2

5

PIN DESCRIPTION

Pin Name	Input/output	Function
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Input	These pins are input pins for status signals ($\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$), output from the CPU (MSM80C86, 80C88). The MSM82C88 generates commands and control signals after decoding these status signals. Since these pins are connected to an internal pull-up resistor, they are set to high level when the CPU status output is at high impedance.
CLK	Input	This pin is the input pin for clock signal output from the clock generator (MSM82C84A). The timing of all MSM82C88 output signals is controlled by this clock signal.
ALE	Output	Strobe signal for latching output address from the CPU to address latch. Address latching occurs on the trailing edge of ALE.
DEN	Output	Control signal for setting the data bus transceiver to data enable. The local bus or system bus transceiver is enabled when this signal is high. DEN is switched to low when the CEN input is low.
DT/$\overline{R}$	Output	Control of the direction of data flow in the data bus transceiver. When the CPU is switched to write mode, this signal is high, and when switched to read mode, this signal is low.
$\overline{AEN}$	Input	Address enable signal. ● IOB = L (SYSTEM BUS MODE) When the $\overline{AEN}$ input is switched to high level, all command outputs are switched to high impedance status. ● IOB = H (I/O BUS MODE) When the $\overline{AEN}$ input is switched to high level, only the $\overline{MRDC}$, $\overline{MWTC}$, and $\overline{AMWC}$ command outputs are switched to high impedance status. When $\overline{AEN}$ is switched from high to low level, high impedance command outputs are not switched to active status (low level) for at least 90 nS, irrespective of the IOB input status.
CEN	Input	Command enable signal. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to inactive status when a low level input is applied to CEN. All command outputs, DEN and $\overline{PDEN}$ outputs are switched to active status when a high level input is applied to CEN.
IOB	Input	I/O bus mode signal. The MSM82C88 is switched to I/O bus mode when a high level input is applied to IOB, and to system bus mode when a low level input is applied.
$\overline{IOWC}$	3-state output	This pin is active-low, and three-state output. This signal is for writing data into the I/O device.
$\overline{AIOWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into I/O devices like the I/O write command ($\overline{IOWC}$), it is made active one clock earlier than $\overline{IOWC}$.
$\overline{IORC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from I/O devices.
$\overline{MWTC}$	3-state output	This pin is active-low and three-state output. This signal is for writing data into memory.
$\overline{AMWC}$	3-state output	This pin is active-low and three-state output. Although this signal is also used for writing into memory like the memory write command ($\overline{MWTC}$), it is made active one cycle earlier than $\overline{MWTC}$.
$\overline{MRDC}$	3-state output	This pin is active-low and three-state output. This signal is for reading data from memory.
$\overline{INTA}$	3-state output	This pin is active-low and three-state output. This signal informs the interrupt controller that the interrupt has been accepted, and then requests output of a vector address onto the data bus.

Pin Name	Input/output	Function
MCE/$\overline{PDEN}$	Output	This pin has two functions. MCE (IOB = Low) master cascade enable function. This is an active-high signal and is used to enable a slave PIC (priority interrupt controller) to read the cascade address output on the data bus by the master PIC during an interrupt sequence. $\overline{PDEN}$ (IOB = High) peripheral data enable function. This is an active-low signal and is used to enable the data bus transceiver on the I/O bus.

FUNCTION

Command Logic

The command output is decided by decoding status signals ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) output from the CPU.

These status signals have the following meanings.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CPU status	Command output
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	I/O read	$\overline{IORC}$
0	1	0	I/O write	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	–
1	0	0	Instruction fetch	$\overline{MRDC}$
1	0	1	Memory read	$\overline{MRDC}$
1	1	0	Memory write	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	–

I/O Bus Mode (IOB = High)

When an I/O access status signal is received from the CPU in I/O bus mode, one of the I/O commands ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) corresponding to the status signal becomes active irrespective of the $\overline{AEN}$ status. At the same time, the $\overline{PDEN}$ and DT/$\overline{R}$ outputs which control the data bus transceiver are generated.

As in system bus mode, the memory commands ($\overline{MRDC}$, $\overline{MWTC}$, and $\overline{AMWC}$) are not switched to low level for at least 90 ns after $\overline{AEN}$ is switched to low level.

System Bus Mode (IOB = Low)

When the bus is usable, the MSM82C88 is enabled by the $\overline{AEN}$ signal from the bus arbiter. Conseuqnetly, no command output becomes active unless the $\overline{AEN}$ signal becomes low. Also note that there is a delay of at least 90 ns before any command output becomes active after the $\overline{AEN}$ signal is switched to low level.

System bus mode is used when more than one CPU is connected to a single bus, and the bus I/O, memory, etc. are used in common.

Command Outputs

The advanced write commands ($\overline{AIOWC}$ and $\overline{AMWC}$) become active one cycle earlier than normal write commands ($\overline{IOWC}$ and $\overline{MWTC}$). This prevents the CPU from being switched to an additional period of wait status.

$\overline{INTA}$ (interrupt acknowledge) is output during the interrupt acknowledge cycle in the same way as $\overline{MRDC}$ in the read cycle. The purpose of this signal is to inform the device which has requested the interrupt that the interrupt has been accepted, and requests a vector address output on the data bus.

$\overline{MRDC}$ – Memory read command
$\overline{MWTC}$ – Memory write command
$\overline{IORC}$ – I/O read command
$\overline{IOWC}$ – I/O write command
$\overline{AMWC}$ – Advanced memory write command
$\overline{AIOWC}$ – Advanced I/O write command
$\overline{INTA}$ – Interrupt acknowledge

Control Output

The control output signals are DEN (Data Enable), DT/$\overline{R}$ (Transmit/Receive), and MCE/$\overline{PDEN}$ (Master Cascade Enable/Peripheral Data Enable).

The DEN signal enables the local bus or system bus, when it is high.

The DT/$\overline{R}$ signal determines the direction of the data on the local bus or system bus.

The function of the MCE/$\overline{PDEN}$ pin is switched according to IOB. The $\overline{PDEN}$ function is selected in I/O bus mode (IOB = high) to provide the I/O or peripheral/system bus data enable signal. When the MCE function is selected in system bus mode (IOB = low), the MCE signal is active (high) level at an interrupt acknowledge status.

The MCE signal is used when a master and slave interrupt controller exists in the system.

ALE (Address Latch Enable)

ALE is generated in each machine cycle to latch the current address to the address latch.

CEN (Command Enable)

This signal is used to enable command outputs. All command outputs become inactive if a low level input is applied to the CEN pin.

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MSM83C55-XXRS/GS/JS

2048 x 8 BIT MASK ROM WITH I/O PORTS

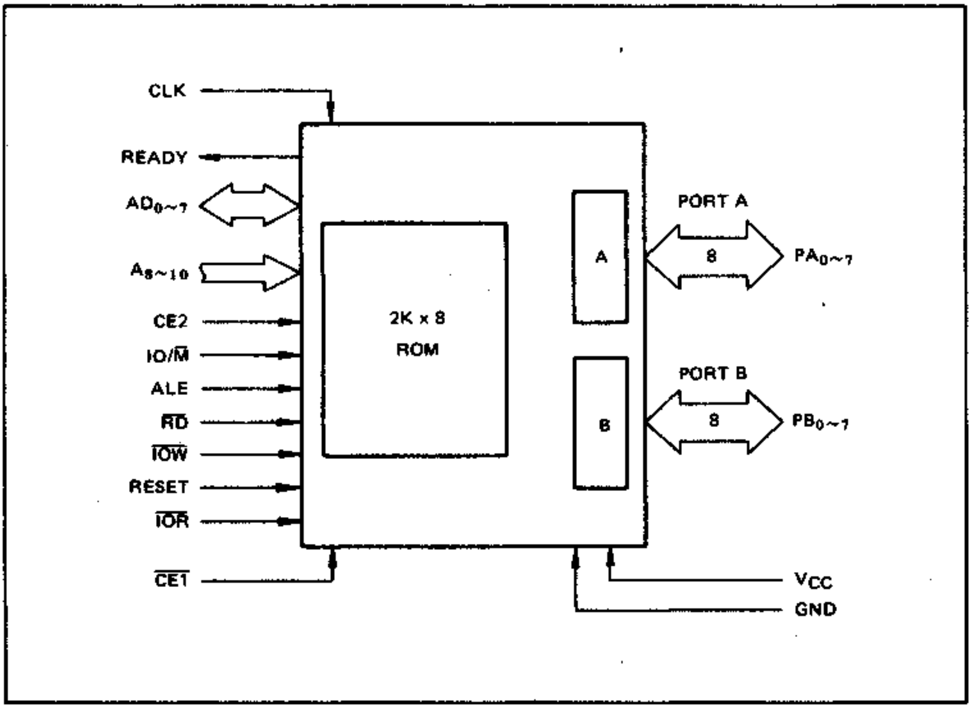
GENERAL DESCRIPTION

The MSM83C55 is a combination of MROM and I/O devices used in a microcomputer system. Owing to the adoption of the CMOS silicon gate technology, it operates on a power supply as small as 100 μA (max.) standby current in the chip non-select status. Since the ROM is composed of 2048 words × 8 bits and its access time (max.) is 400 ns, it can be applied without using the wait state in the 80C85A system, too. The I/O circuit is composed of 2 universal I/O ports. Each of these I/O ports has 8 port lines and each of these port lines can be programmed as input or output line independently.

FEATURES

- High speed and low power consumption owing to adoption of silicon gate CMOS
- Composed of 2048 words x 8 bits
- 3 ~ 6 V single power supply
- Address latch circuit incorporated
- Provided with 2 universal 8-bit I/O ports
- TTL Compatible
- Indivisual I/O port line programmable as input or output
- Time division address/data bus
- 40-pin DIP (MSM83C55-xxRS)
- 44-pin flat package (MSM83C55-xxGS)
- 44-pin PLCC Package (MSM83C55-xxJS)
- Direct interface with MSM80C85A (3MHz)

CIRCUIT CONFIGURATION



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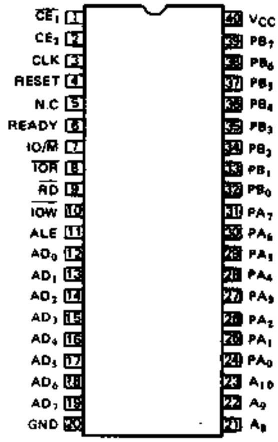
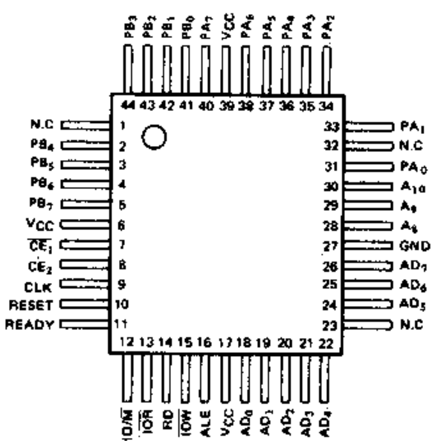
PIN CONFIGURATION

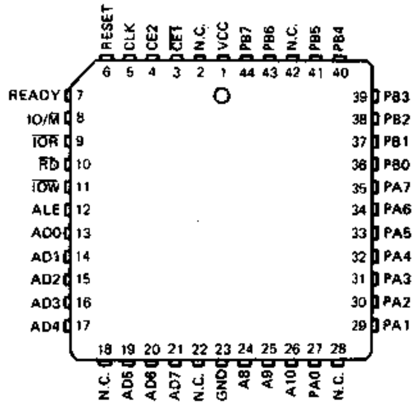
MSM83C55-xxRS (Top View)
40 Lead Plastic DIP





MSM83C55-xxGS (Top View)
44 Lead Plastic Flat Package

MSM83C55-XXJS (Top View)
44-pin Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM83C55RS	MSM83C55GS	MSM83C55JS	
Supply Voltage	V_{CC}	With respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	-40 to +85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	-40	+25	+85	°C
"L" Input Voltage	V_{IL}	-0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

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DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL}=2mA	V_{CC}=4.5V to 5.5V Ta=-40°C to +85°C			0.45	V
"H" Output Voltage	V_{OH}	I_{OH}=-400μA		2.4			V
		I_{OH}=-40μA		4.2			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		-10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		-10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CE1} \geq V_{CC}$-0.2V CE2≤0.2V $V_{IH} \geq V_{CC}$-0.2V V_{IL} ≤0.2V			0.1	100	μA
Average Supply Current (active)	I_{CC}	IO write cycle time: 1 μs				5	mA

AC CHARACTERISTICS

(V_{CC}=4.5V to 5.5V, Ta=-40°C to +85°C)

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	t_{CYC}	320		ns
Clock Pulse Width	T_1	80		ns
Clock Pulse Width	T_2	120		ns
Clock Rise and Fall Time	t_f, t_r		30	ns
Address to Latch Setup Time	t_{AL}	50		ns
Address Hold Time after Latch	t_{LA}	30		ns
Latch to READ/WRITE Control	t_{LC}	100		ns
Valid Data Out Delay from READ Control	t_{RD}		170	ns
Address Stable to Data Out Valid	t_{AD}		400	ns
Latch Enable Width	t_{LL}	100		ns
Data Bus Float after READ	t_{RDF}	0	100	ns
READ/WRITE Control to Latch Enable	t_{CL}	20		ns
READ/WRITE Control Width	t_{CC}	250		ns
Data In to WRITE Setup Time	t_{DW}	150		ns
Data In Hold Time after WRITE	t_{WD}	10		ns
WRITE to Port Output	t_{WP}		400	ns
Port Input Setup Time	t_{PR}	50		ns
Port Input Hold Time	t_{RP}	50		ns
READY Hold Time	t_{PYH}	0	160	ns
Address to READY	t_{ARY}		160	ns
Recovery Time between Controls	t_{RV}	300		ns
Data Out Delay from READ Control	t_{RDE}	10		ns
ALE to Data Out Valid	t_{LD}		350	ns

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and output
Load condition: C_L = 150 pF

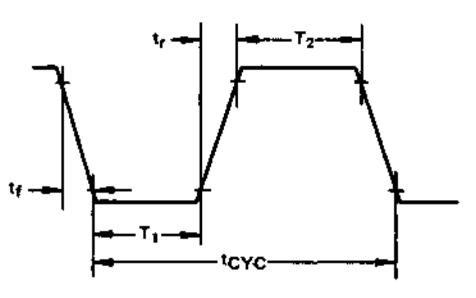

Fig. 1 Clock Signal for MSM83C55

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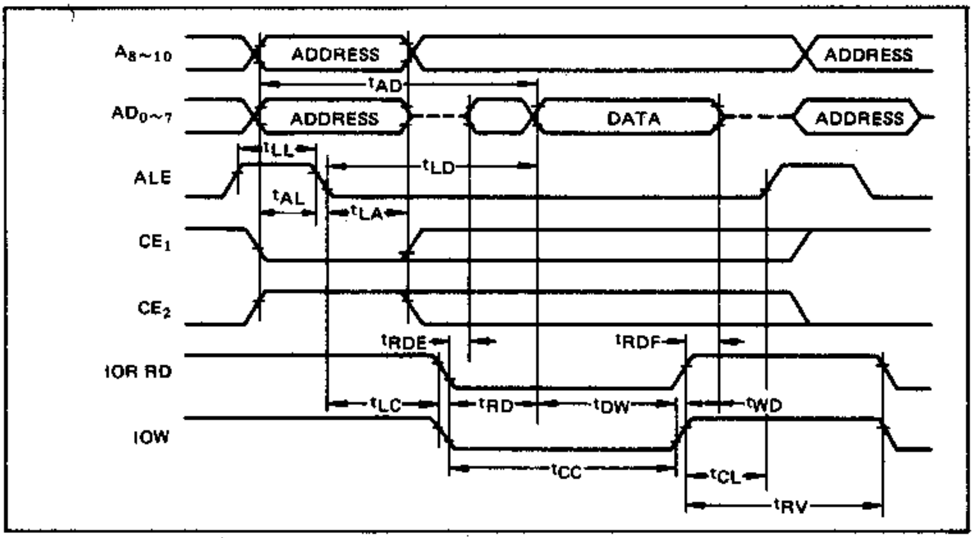


Fig. 2 Timing for ROM Reading and for I/O Reading and Writing

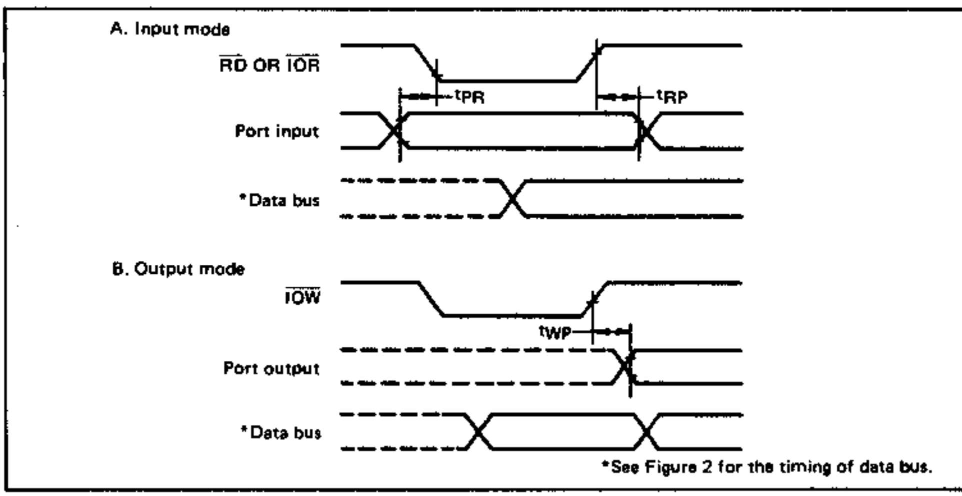


Fig. 3 I/O Port Timing

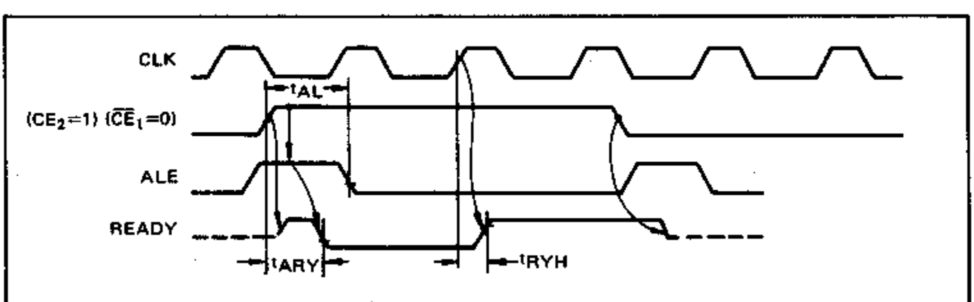


Fig. 4 Wait State Timing (READY = 0)

PIN DESCRIPTION

Pin symbol	Function
RESET	When this signal becomes high level, ports A and B become the input mode.
ALE	This pin is used to fetch the AD 0~7, A 8~10, IO/$\overline{M}$, $\overline{CE1}$, and CE2 signals to their respective latch circuits at the fall of the ALE (Address Latch Enable) signal.
$\overline{CE1}$, CE2	When $\overline{CE}$1 fetched to the latch circuit is high level or CE2 is low level, no read or write operation is performed. The AD 0~7 and READY output signals are made into the floating status.
AD0~7	Three-stake bidirectional address/data bus. This bus fetches 8-bit address information to the latch circuit upon the fall of the ALE signal. When $\overline{CE1}$ in holding is low level and CE2 is high level, data is output from chip to but if RD or IOR is low level and it is fetched from bus to chip if $\overline{IOW}$ is low level.
A8~10	These are high order bits of ROM address and have no relation to I/O operation.
IO/$\overline{M}$	When $\overline{RD}$ is low level, this pin selects the I/O port if the IO/$\overline{M}$ in hold is high level or ROM if it is low level.
$\overline{RD}$	If $\overline{RD}$ is low level, the memory data is output to AD 0~7 when the ROM cycle is selected, but the selected port data is output to the same port when the I/O cycle is selected.
$\overline{IOR}$	The port data selected at low level is output to AD 0~7. When turned to the low level, the $\overline{IOR}$ becomes the same function as that when IO/$\overline{M}$ is turned to the high level and $\overline{RD}$ to the low level. When both $\overline{RD}$ and $\overline{IOR}$ become high level, the output of AD 0~7 is made into the floating state.
$\overline{IOW}$	At the low level, the AD 0~7 data is written to the selected port.
CLK	This signal is used to generate the READY signal for the generation of 1 wait cycle built into the 83C55.
READY	This signal becomes low level when the ALE is high level and the $\overline{CE1}$ and CE2 are active. It becomes high level at the rise of CLK after the fall of the ALE.
PA0~7	These are universal I/O pins and the input/output is determined by the content of the data direction register. When writing data to port A, make the chip enable active and turn the $\overline{IOW}$ to low level after selecting AD 0, 1 to 0, 0. When reading it, turn the $\overline{IOR}$ to low level instead of $\overline{IOW}$ and IO/$\overline{M}$ to high level.
PB0~7	Same as the operation of PA0~7, excepting that AD0 is selected to 1 and AD1 to 0.
V_{CC}	+5 V power supply
GND	0 V

OPERATIONAL DESCRIPTION

ROM Block

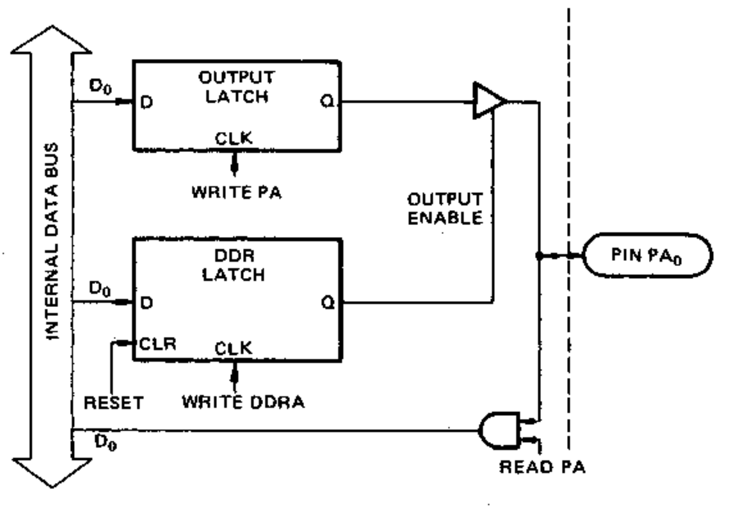
The ROM block in the chip is specified in address by the chip enable and 11-bit address. Upon the fall of the ALE signal, the address and chip enable are fetched in the address latch circuit. When the chip enable is active and IO/$\overline{M}$ is low level, 8-bit content of ROM at the address held in the address latch circuit is transmitted to the bus through the output buffer of AD 0~7 upon the fall of the $\overline{RD}$.

I/O Block

The I/O block in the chip is specified in the address by the value of 2 bits of AD 0 ~ 1 and chip enable. Two 8-bit data direction registers (DDR) built in the MSM83C55 are used to turn corresponding individual port pins to the input mode or output mode. It becomes the input mode when set to 0 and the output mode when set to 1. It is impossible to read the DDR from outside, however.

AD_1	AD_0	Selection
0	0	Port A
0	1	Port B
1	0	Port A data direction register (DDRA)
1	1	Port B data direction register (DDRB)

Upon the fall of $\overline{IOW}$ when the chip enable is active, the AD 0~7 data is written to the I/O port to be determined by the value of AD 0 ~ 1 in hold. During this operation, the selected side I/O bits are all subject to its influence irrespective of the I/O status and IO/M status. The output level remains unchanged until the $\overline{IOW}$ returns to high level. The data can be read from the ports when the chip enable in holding is active and IO/M is high level and yet the $\overline{RD}$ or $\overline{IOR}$ signal falls. In both input and output, the data on the selected side exists on the line of AD 0 ~ 7. The function of I/O ports and DDR (data direction register) is shown in the block diagram below:



Writing "0" to the DDR is equivalent to the RESET operation when the port output is put into High impedance status and the input mode is specified. Note that the data can be written to the ports even if the output pin was already in the high impedance status (input mode) by the DDR. Likewise, it is also possible to read the data once set to those ports.

PERIPHERALS

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OKI semiconductor

MSM5832RS

REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM5832RS is a metal-gate CMOS Real Time Clock/Calendar for use in bus-oriented microprocessor applications. The on-chip 32.768Hz crystal controlled oscillator time base is divided to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ±30 second correction.

The MSM5832RS normally operates from a 5V ±5% supply. Battery backup operation down to 2.2V allows continuation of time keeping when main power is off. The MSM5832RS is offered in an 18-lead dual-in-line plastic (RS suffix) package.

FEATURES

- 7 Function – SECOND, MINUTE, HOUR, DAY, DAY-OF-WEEK, MONTH, YEAR
- Automatic leap year calendar
- 12 or 24 hour format
- ±30 second error correction
- 4-BIT DATA BUS
- 4-BIT ADDRESS
- READ, WRITE, HOLD, and CHIP SELECT inputs
- Reference signal outputs – 1024, 1, 1/60, 1/3600Hz
- 32.768kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to V_{DD} = 2.2V
- Low power dissipation
  90 μW Max. at V_{DD} = 3V
  2.5 mW Max. at V_{DD} = 5V
- 18 pin plastic DIP package

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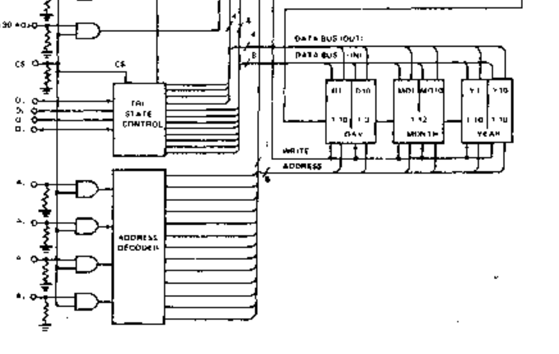
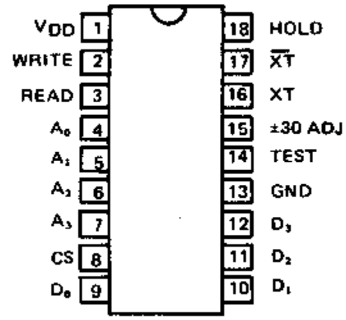
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

A0 to A3	:	Address Inputs
WRITE	:	Write Enable
READ	:	Read Enable
HOLD	:	Count Hold
CS	:	Chip Select
D0 to D3	:	Data Input Output
TEST	:	Test Input
±30 ADJ	:	±30 Second Correction Input
XT & $\overline{XT}$	:	xtal oscillator connections
V_{DD}	:	+5V Supply
GND	:	Ground



REGISTER TABLE

Address Input				Register Name	Data Input/Output				Data Limit	Remarks
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S1	*	*	*	*	0 ~ 9	S1 or S10 are reset to zero irrespective of input data D0—D3 when write instruction is executed with address selection.
1	0	0	0	S10	*	*	*		0 ~ 5	
0	1	0	0	MI1	*	*	*	*	0 ~ 9	
1	1	0	0	MI10	*	*	*		0 ~ 5	
0	0	1	0	H1	*	*	*	*	0 ~ 9	
1	0	1	0	H10	*	*	†	†	0 ~ 1 / 0~2	D2 = "1" for PM D3 = "1" for 24 hour format D2 = "0" for AM D3 = "0" for 12 hour format
0	1	1	0	W	*	*	*		0 ~ 6	
1	1	1	0	D1	*	*	*	*	0 ~ 9	
0	0	0	1	D10	*	*	†		0 ~ 3	D2 = "1" for 29 days in month 2 (2) D2 = "0" for 28 days in month 2
1	0	0	1	MO1	*	*	*	*	0 ~ 9	
0	1	0	1	MO10	*				0 ~ 1	
1	1	0	1	Y1	*	*	*	*	0 ~ 9	
0	0	1	1	Y10	*	*	*	*	0 ~ 9	

(1) *data valid as "0" or "1".
Blank does not exist (unrecognized during a write and held at "0" during a read)
†data bits used for AM/PM, 12/24 HOUR and leap year.
(2) If D2 previously set to "1", upon completion of month 2 day 29, D2 will be internally reset to "0".

Table 1

OSCILLATOR FREQUENCY DEVIATIONS

Frequency Deviation vs Temperature

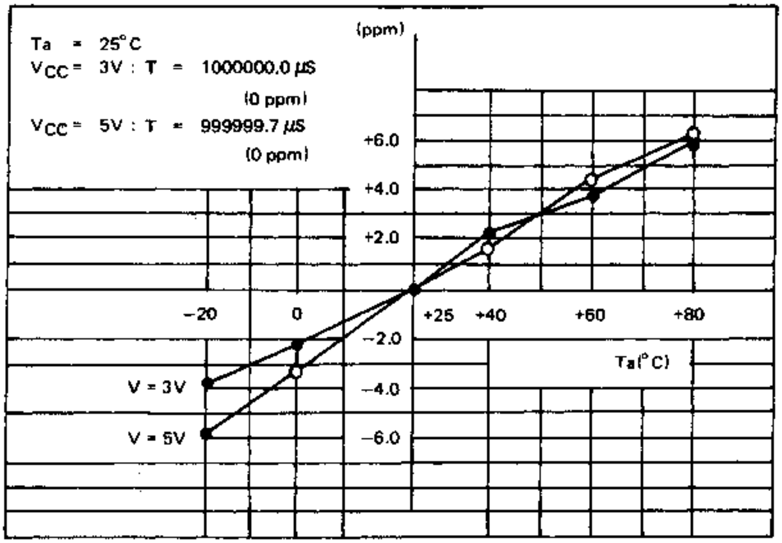


Figure 1

Frequency Deviation vs Supply Voltage

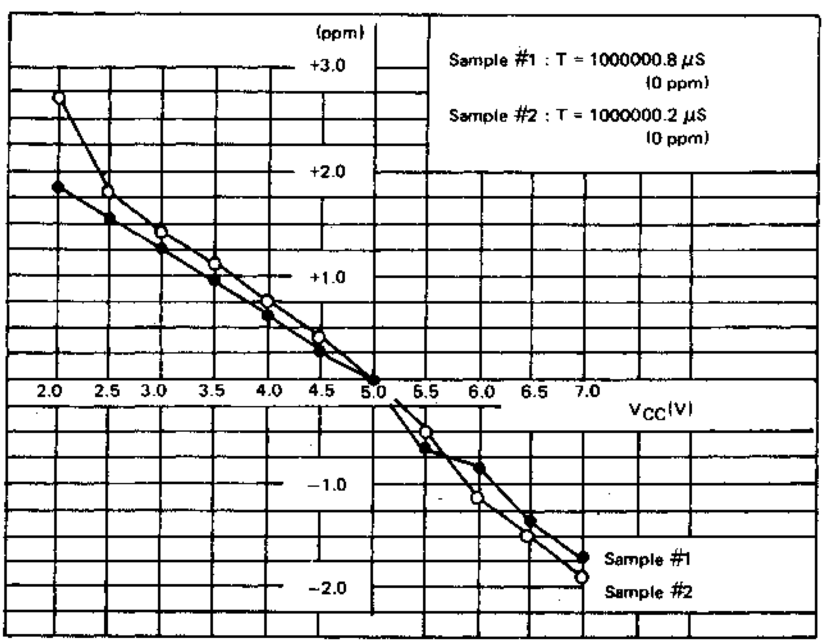


Figure 2

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD} + 0.3	V
Data I/O voltage	$V_{\overline{O}}$	−0.3 ~ V_{DD} + 0.3	V
Storage Temperature	Tstg	−55 ~ 150	°C

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	4.5	5	7	V	
Standby Supply Voltage	V_{DH}	2.2	–	7	V	
Input Signal Level	V_{IH}	3.6	–	V_{DD}	V	V_{DD} = 5V ± 5% Respect to GND
	V_{IL}	−0.3	–	0.8	V	
Crystal Oscillator Freq.	f(XT)	–	32.768	–	kHz	
Operating Temperature	T_{OP}	−30	–	+85	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ±5%; T_A = −30 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I_{IH}	10	25	50	μA	V_{IN}=5V, V_{DD}=5V
	I_{IL}	–	–	-1	μA	V_{IN} = 0V
Data I/O Leakage Current	I_{LD}	-10	–	10	μA	$V_{I/O}$ = 0 to V_{DD} CS = "0"
Output Low Voltage	V_{OL}	–	–	0.4	V	I_O = 1.6 mA, CS = "1", READ = "1"
Output Low Current	I_{OL}	1.6	–	–	mA	V_O = 0.4V, CS = "1", READ = "1"
Operating Supply Current	I_{DDS}	–	15	30	μA	V_{CC} = 3V, Ta = 25°C
	I_{DD}	–	100	500	μA	V_{CC} = 5V, Ta = 25°C

(1) XT, $\overline{XT}$ and D_0 ~ D_3 excluded.

5

SWITCHING CHARACTERISTICS

(1) READ mode

(V_{DD} = 5V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	———	150	–	–	μs
HOLD Hold Time	t_{HH}	———	0	–	–	μs
HOLD Pulse Width	t_{HW}	———	–	–	990	ms
HOLD "L" Hold Time	t_{HL}	———	130	–	–	μs
READ Hold Time	t_{RH}	———	0	–	–	μs
READ Set-up Time	t_{RS}	———	0	–	–	μs
READ Access Time	t_{RA}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	–	–	6	μs
ADDRESS Set-up Time	t_{AS}	———	3	–	–	μs
ADDRESS Hold Time	t_{AH}	———	0.2	–	–	μs
READ Pulse Width	t_{RW}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	2	–	–	μs
DARA Access Time	t_{AC}	$R_{PULL-UP}$ = 5KΩ C_L = 15pF	–	–	0.6	μs
OUTPUT Disable Time	t_{OFF}	$R_{PULL-UP}$ = 5KΩ C_L = 15 pF	–	–	0.6	μs
CS Enable Delay Time	t_{CS1}	———	–	–	0.6	μs
CS Disable Delay Time	t_{CS2}	———	–	–	0.6	μs

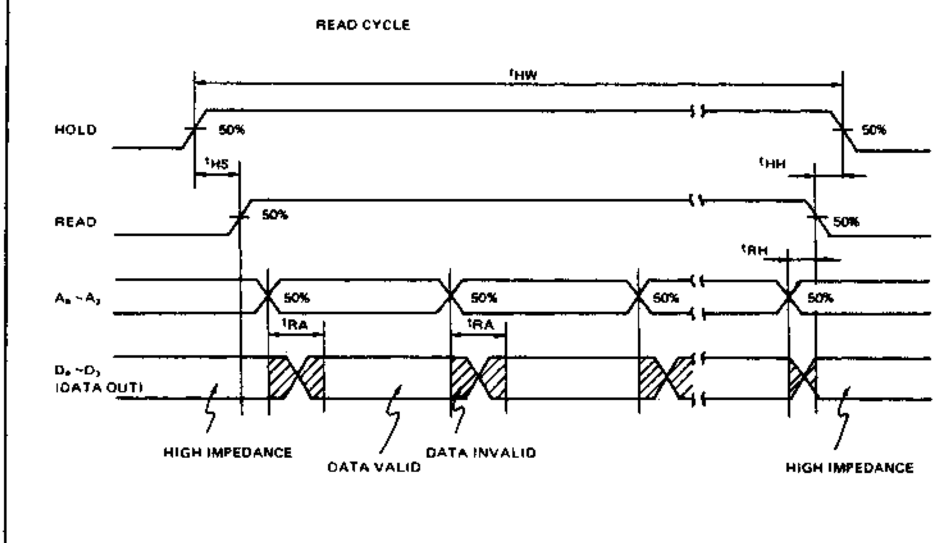


Figure 3 Read Cycle

Notes: 1. A Read occurs during the overlap of a high CS and a high READ.
2. CS may be a permanent "1", or may be coincident with HOLD pulse.

5

SWITCHING CHARACTERISTICS

(2) WRITE mode

(V_{DD} = 5V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
HOLD Set-up Time	t_{HS}	——	150	–	–	μs
HOLD Bold Time	t_{HH}	——	0	–	–	μs
HOLD Pulse Width	t_{HW}	——	–	–	990	ms
HOLD "L" Hold Time	t_{HL}	——	130	–	–	μs
ADDRESS Pulse Width	t_{AW}	——	1.7	–	–	μs
Data Pulse Width	t_{DW}	——	1.7	–	–	μs
DATA Set-up Time	t_{DS}	——	0.5	–	–	μs
DATA Hold Time	t_{DH}	——	0.2	–	–	μs
WRITE Pulse Width	t_{WW}	——	1.0	–	–	μs
CS Enable Delay Time	t_{CS1}	——	–	–	0.6	μs
CS Disoble Delay Time	t_{CS2}	——	–	–	0.6	μs

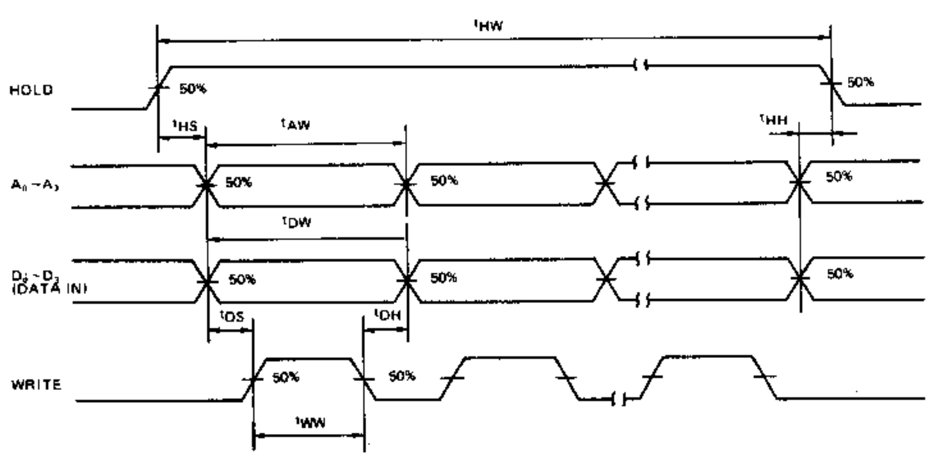
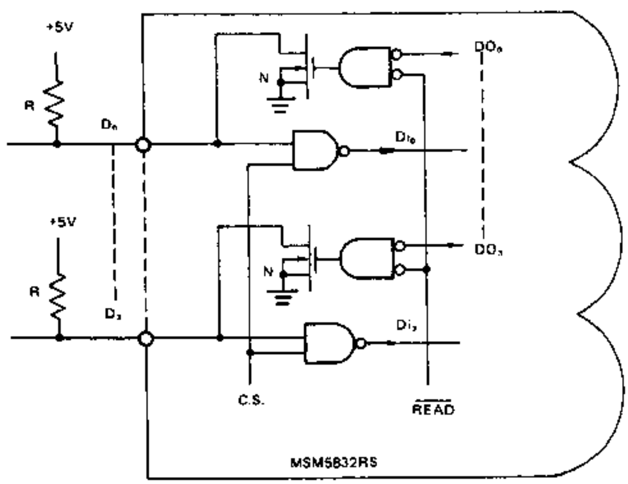


Figure 4 Write Cycle

Notes: 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE.
2. CS may be permanent "1", or may be coincident with HOLD pulse.

5

PIN DESCRIPTION

Name	Pin No.	Description
VDD	1	Power supply pin. Application circuits for power supply are described in Figure 9.
WRITE	2	Data write pin. Data write cycle is described in Figure 4.
READ	3	Data read pin. Data read cycle is described in Figure 3.
$A_0 \sim A_3$	4 ~ 7	Address input pins used to select internal counters for read/write operations. The address is specified by 4-bit binary code as shown in Table 1.
C S	8	Chip slect pin which is required to interface with the external circuit. HOLD, WRITE, READ, ±30ADJ, TEST, $D_0 \sim D_3$ and $A_0 \sim A_3$ pins are activated if CS is set at H level, while all of these pins are disabled if CS is set at L level.
$D_0 \sim D_3$	9 ~ 12	Data input/output pins (bidirectional bus). As shown in Figure 5, external pull-up registers of 4.7 kΩ ~ 10 kΩ are required by the open-drain NMOS output. D_3 is the MSB, while D_0 is the LSB  Figure 5

Name	Pin No.	Description
GND	13	Ground pin.
TEST	14	Test pin. Normally this pin should be left open or should be set at ground level. With CS at V_{DD}, pulses to V_{DD} on the TEST input will directly clock the S_1, MI_{10}, W, D_1 and Y_1 counters, depending on which counter is addressed (W and D_1 are selected by D_i address in this mode only). Roll-over to next counter is enabled in this mode.
±30ADJ	15	This pin is used to adjust the time within the extent of ± 30 seconds. If this pin is set at H level when the seconds digits are 0 ~ 29, the seconds digits are cleared to 0. If this pin is set at H level when the seconds digits are 30 ~ 59, the second digits will be cleared to 0 and the minutes digits will be increased by +1. To enable this function, 31.25 ms or more width's pulse should be input to this pin.
XT	16	Oscillator pin. 32.768 kHz crystal, capacitor and trimmer condensor for frequency adjustment connected to these pins. See Figure 6. As for oscillator frequency deviation, refer to Figure 1 and Figure 2. If an external clock is to be used for the MSM5832RS's oscillation source, the external clock is to be input to XT, and $\overline{XT}$ should be left open.
$\overline{XT}$	17	

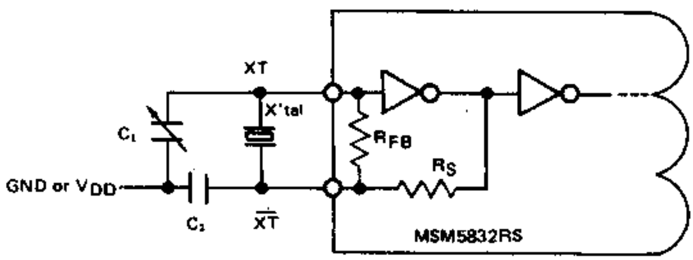


Figure 6

Name	Pin No.	Description
HOLD	18	Switching this input to V_{DD} inhibits the internal 1 Hz clock to the S1 counter. After the specified HOLD set-up time (150 μs), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 990 ms, real time accuracy will be undisturbed. Pull-down to GND is provided by an internal resistor.

5

REFERENCE SIGNAL OUTPUT PIN

Condition	Output	Reference Frequency	Pulse Width
HOLD = L	D_0 (1)	1024 Hz	duty 50%
READ = H	D_1	1 Hz	122.1 μS
CS = H	D_2	1/60 Hz	122.1 μS
$A_0 \sim A_3$ = H	D_3	1/3600 Hz	122.1 μS

(1) 1024 Hz signal at D_0 not dependent on HOLD input level.

APPLICATION EXAMPLE

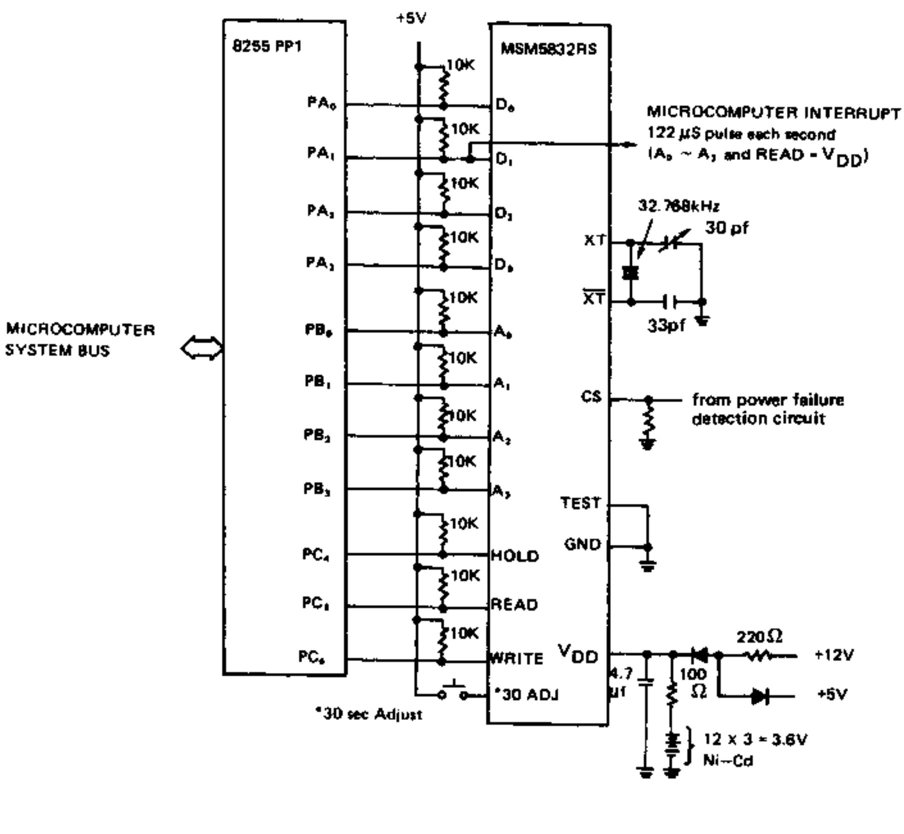
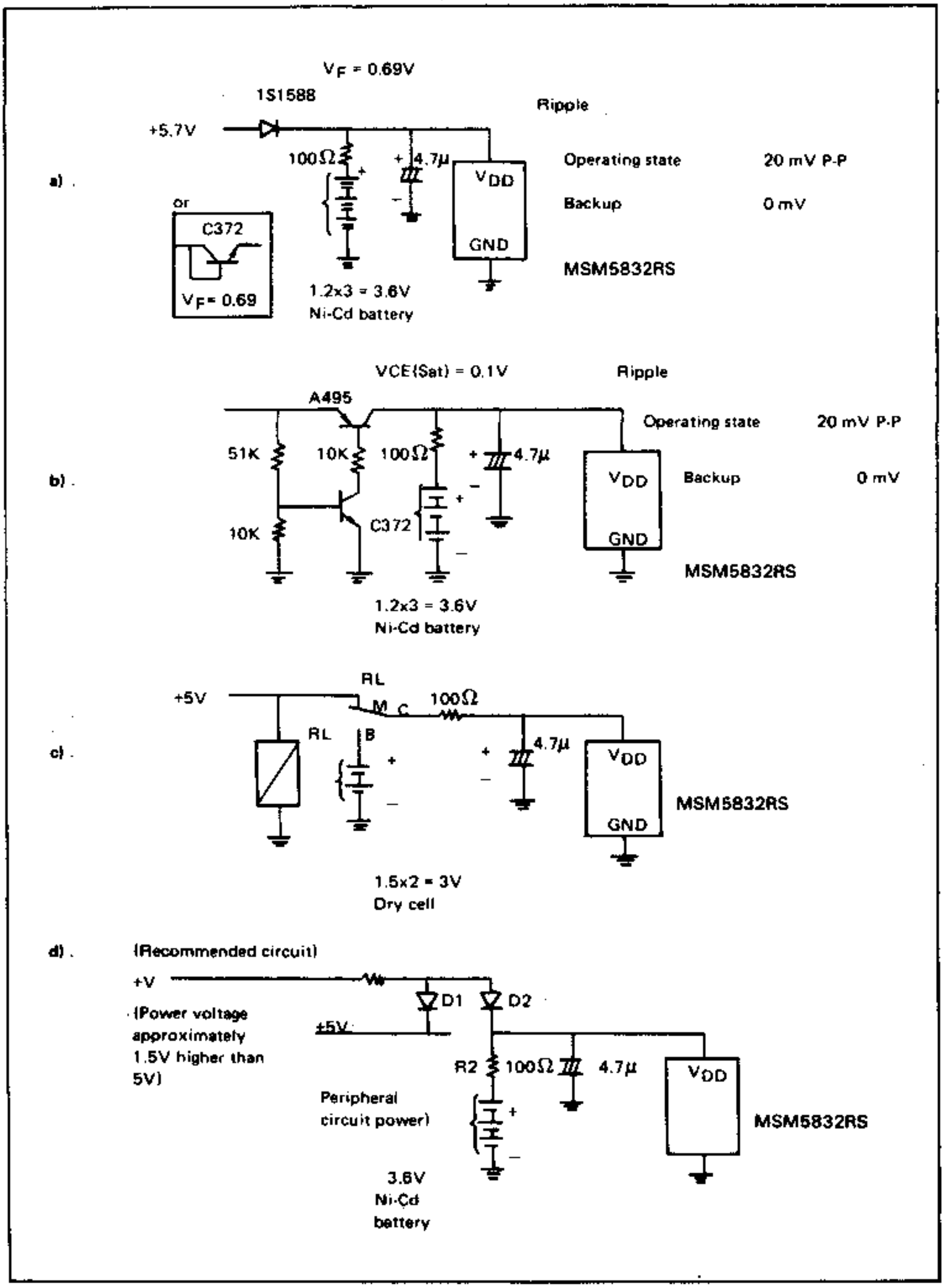


Figure 7

APPLICATION CIRCUIT – POWER SUPPLY CIRCUIT

Open or ground unused pins (pins other than the XT, $\overline{XT}$, D0–D3, and $\overline{BUSY}$ pins).



Note: Use the same diodes for D1 and D2 to reduce the level difference between +5V and V_{DD} of the MSM5832RS.

OKI semiconductor

MSM58321RS

REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM58321RS is a metal gate CMOS Real Time Clock/Calendar with a battery backup function for use in bus-oriented microprocessor applications.

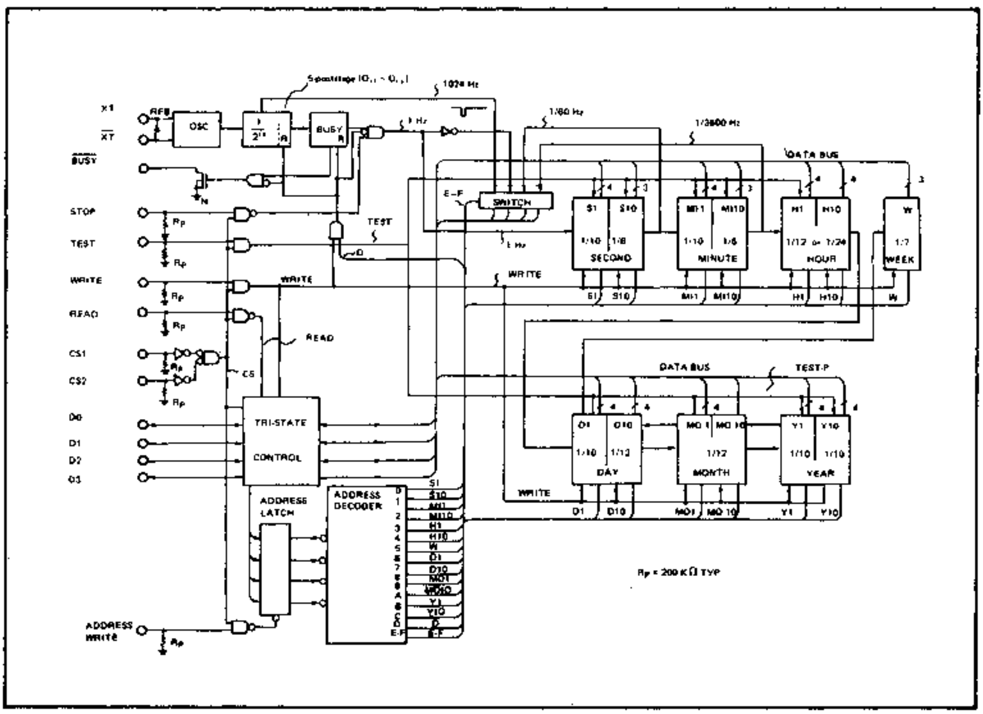
The 4-bit bidirectional bus line method is used for the data I/O circuit; the clock is set, corrected, or read by accessing the memory.

The time is read with 4-bit DATA I/O, ADDRESS WRITE, READ, and $\overline{\text{BUSY}}$; it is written with 4-bit DATA I/O, ADDRESS WRITE, WRITE, and $\overline{\text{BUSY}}$.

FEATURES

- 7 Function-Second, Minute, Hour, Day, Day-of-Week, Month, Year
- Automatic leap year calender
- 12/24 hour format
- Frequency divider 5-poststage reset
- Reference signal output
- 32.768kHz crystal controlled operation
- Single 5V power supply
- Back-up battery operation to V_{DD} = 2.2V
- Low power dissipation
  90μW max. at V_{DD} = 3V
  2.5mW max. at V_{DD} = 5V
- 16 pin plastic DIP package

FUNCTIONAL BLOCK DIAGRAM



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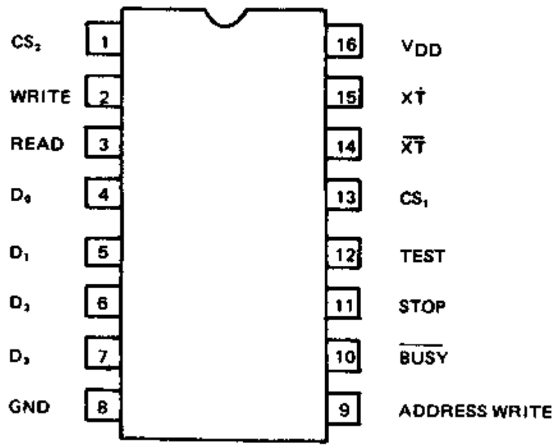
PIN CONFIGURATION



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REGISTER TABLE

Address	Address input				Register Name	Data input/output				Count value	Remarks
	D_0 (A_0)	D_1 (A_1)	D_2 (A_2)	D_3 (A_3)		D_0	D_1	D_2	D_3		
0	0	0	0	0	S_1	•	•	•	•	0 ~ 9	
1	1	0	0	0	S_{10}	•	•	•		0 ~ 5	
2	0	1	0	0	MI_1	•	•	•	•	0 ~ 9	
3	1	1	0	0	MI_{10}	•	•	•		0 ~ 5	
4	0	0	1	0	H_1	•	•	•	•	0 ~ 9	
5	1	0	1	0	H_{10}	•	•	•	⊙	0~1 or 0~2	D2 = 1 specifies PM, D2 = 0 specifies AM, D3 = 1 specifies 24-hour timer, and D3 = 0 specifies 12-hour timer. When D3 = 1 is written, the D2 bit is reset inside the IC.
6	0	1	1	0	W	•	•	•		0 ~ 6	
7	1	1	1	0	D_1	•	•	•	•	0 ~ 9	
8	0	0	0	1	D_{10}	•	•	◎	◎	0 ~ 3	The D2 and D3 bits in D10 are used to select a leap year.
9	1	0	0	1	MO_1	•	•	•	•	0 ~ 9	
A	0	1	0	1	MO_{10}	•				0 ~ 1	
B	1	1	0	1	Y_1	•	•	•	•	0 ~ 9	
C	0	0	1	1	Y_{10}	•	•	•	•	0 ~ 9	
D	1	0	1	1							A selector to reset 5 poststages in the $1/2^{14}$ frequency divider and the BUSY circuit. They are reset when this code is latched with ADDRESS LATCH and the WRITE input goes to 1.
E~F	0/1	1	1	1							A selector to obtain reference signal output. Reference signals are output to D0 ~ D3 when this code is latched with ADDRESS LATCH and READ input goes to 1.

Calender	D_2	D_3	Remainder obtained by dividing the year number by 4
Gregorian calender	0	0	0
Showa	1	0	3
	0	1	2
	1	1	1

Notes: (1) There are no bits in blank fields for data input/output. 0 signals are output by reading and data is not stored by writing because there are no bits.
(2) The bit with marked ⊙ is used to select the 12/24-hour timer and the bits marked ◎ are used to select a leap year. These three bits can be read or written.
(3) When signals are input to bus lines D0 – D3 and ADDRESS WRITE goes to 1 for address input, ADDRESS information is latched with ADDRESS LATCH.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	Ta = 25°C	–0.3 ~ 7	V
Input voltage	V_I	Ta = 25°C	GND–0.3 ~ V_{DD} + 0.3	V
Output voltage	V_O	Ta = 25°C	GND–0.3 ~ V_{DD} + 0.3	V
Storage temperature	Tstg	–	–55 ~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power voltage	V_{DD}	–	4.5 ~ 7	V
Data hold voltage	V_{DH}	–	2.2 ~ 7	V
Crystal frequency	f(XT)	–	32.768	kHz
Operating temperature	Top	–	–30 ~ +85	°C

Note: The data hold voltage guarantees the clock operations, though it does not guarantee operations outside the IC and data input/output.

DC CHARACTERISTICS

(V_{DD} = 5 V ±5%, Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H input voltage	V_{IH1}	– Note 1	3.6	–	–	V
	V_{IH2}	– Note 2	V_{DD}–0.5	–	–	
L input voltage	V_{IL}	–	–	–	0.8	V
L output voltage	V_{OL}	I_O = 1.6 mA	–	–	0.4	V
L output current	I_{OL}	V_O = 0.4 V	1.6	–	–	mA
H input current	I_{IH1}	V_1 = V_{DD}V Note 3	10	30	80	μA
	I_{IH2}	V_1 = V_{DD}V Note 4	–	–	1	
L input current	I_{IL}	V_I = 0 V	–	–	–1	μA
Input capacity	C_I	f = 1 MHz	–	5	–	pF
Current consumption	I_{DD}	f = 32.768 kHz V_{DD} = 5V/V_{DD} = 3V	–	100/15	500/30	μA

Note: 1. CS_2, WRITE, READ, ADDRESS WRITE, STOP, TEST, D_0 ~ D_3
2. CS_1
3. CS_1, CS_2, WRITE, READ, ADDRESS WRITE, STOP, TEST
4. D_0 ~ D_3

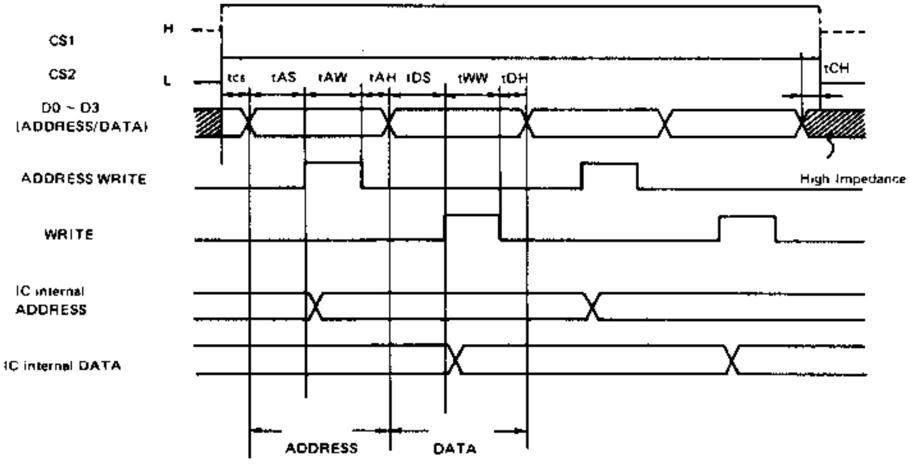
5

SWITCHING CHARACTERISTICS

(1) WRITE mode

(V_{DD} = 5 V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CS setup time	t_{CS}	–	0	–	–	µs
CS Hold time	t_{CH}	–	0	–	–	µs
Address setup time	t_{AS}	–	0	–	–	µs
Address write pulse width	t_{AW}	–	0.5	–	–	µs
Address hold time	t_{AH}	–	0.1	–	–	µs
Data setup time	t_{DS}	–	0	–	–	µs
Write pulse width	t_{WW}	–	2	–	–	µs
Data hold time	t_{DH}	–	0	–	–	µs



Write Cycle

Note: ADDRESS WRITE and WRITE inputs are activated by the level, not by the edge.

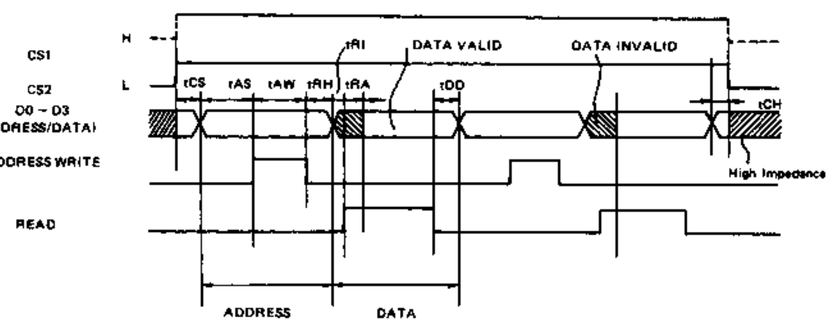
5

(2) READ mode

(V_{DD} = 5 V ±5%, Ta = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CS setup time	t_{CS}	–	0	–	–	μs
CS Hold time	t_{CH}	–	0	–	–	μs
Address setup time	t_{AS}	–	0	–	–	μs
Address write pulse width	t_{AW}	–	0.5	–	–	μs
Address hold time	t_{AH}	–	0.1	–	–	μs
Read access time	t_{RA}	–	–	–	see Note 1	μs
Read delay time	t_{DD}	–	–	–	1	μs
Read inhibit time	t_{RI}	–	0	–	–	μs

Note 1. $t_{RA} = 1\,\mu s + CR \ln\left(\frac{V_{DD}}{V_{DD} - V_{IH}\,min}\right)$



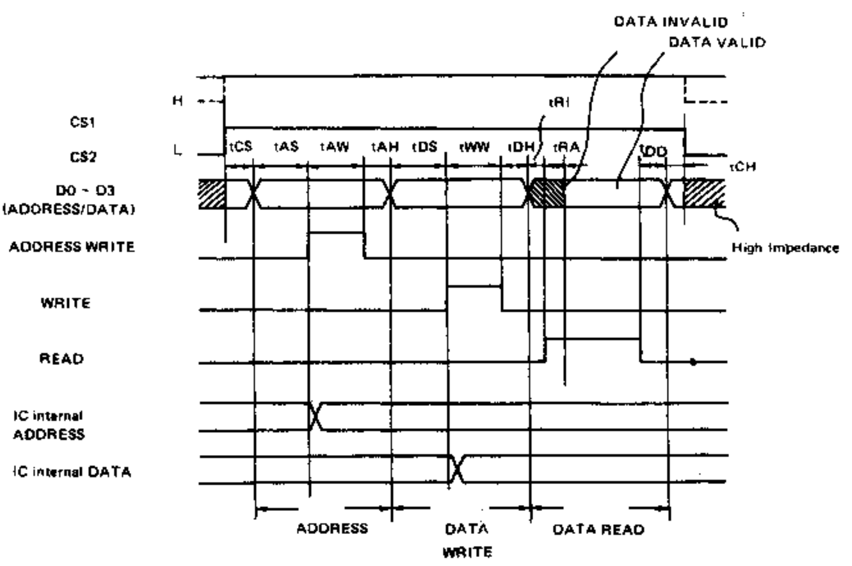
Read Cycle

Note: ADDRESS WRITE and READ inputs are activated by the level, not by the edge.

(3) WRITE & READ mode

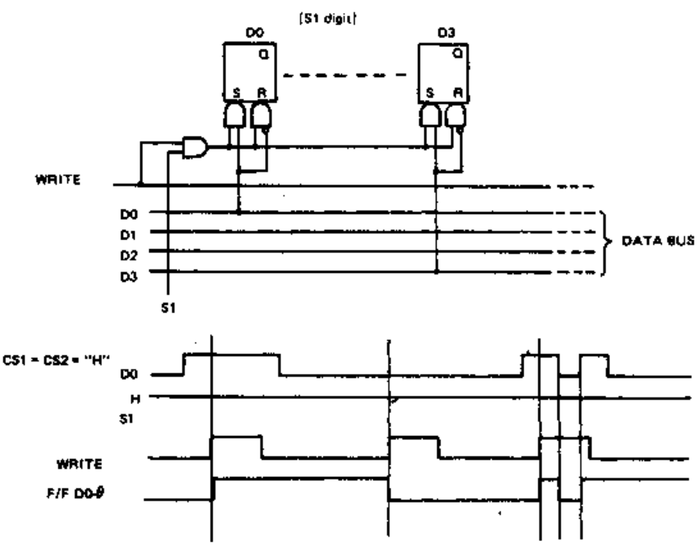
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CS setup time	t_{CS}	–	0	–	–	μs
CS hold time	t_{CH}	–	0	–	–	μs
Address setup time	t_{AS}	–	0	–	–	μs
Address write pulse width	t_{AW}	–	0.5	–	–	μs
Address hold time	t_{AH}	–	0.1	–	–	μs
Data setup time	t_{DS}	–	0	–	–	μs
Write pulse width	t_{WW}	–	2	–	–	μs
Data hold time	t_{DH}	–	0	–	–	μs
Read access time	t_{RA}	–	–	–	see Note 1	μs
Read delay time	t_{DD}	–	–	–	1	μs
Read inhibit time	t_{RI}	–	0	–	–	μs

Note 1. $t_{RA} = 1\,\mu s + CR \ln\left(\frac{V_{DD}}{V_{DD} - V_{IH}\min}\right)$



Read & Write Cycle

PIN DESCRIPTION

Name	Pin No.	Description
CS_2	1	Chip select pins. These pins enable the interface with the external circuit when both of these pins are set at H level simultanuously.
CS_1	13	If one of these pins is set at L level, STOP, TEST, WRITE, READ, ADDRESS WRITE pins and $D_0 \sim D_3$ pins are inactivated. Since the threshold voltage VT for the CS_1 pin is higher than that for other pins, it should be connected to the detector of power circuit and peripherals and CS_2 is to be connected to the microcontroller.
WRITE	2	WRITE pin is used to write data; it is activated when it is at the H level. Data bus data inside the IC is loaded to the object digit while this WRITE pin is at the H level, not at the WRITE input edge. Refer to Figure 2 below.
		 Figure 2

Name	Pin No.	Description
READ	3	READ pin is used to read data; it is activated when it is at the H level. Address contents are latched with ADDRESS LATCH inside the IC at the D0 – D3 and ADDRESS WRITE pins to select the object digit, then an H-level signal is input to the READ pin to read data. If a count operation is continued by setting the STOP input to the L level, read operation must be performed, in principle, while the $\overline{BUSY}$ output is at the H level. While the $\overline{BUSY}$ output is at the L level, count operations are performed by digit counters and read data is not guaranteed, therefore, read operations are inhibited in this period. Figure 3 shows a time chart of the $\overline{BUSY}$ output, 1 Hz signal inside the IC, and READ input. A read operation is stopped temporarily within a period of 244 μs from the $\overline{BUSY}$ output trailing edge and it is restarted when the $\overline{BUSY}$ output goes to the H level again.

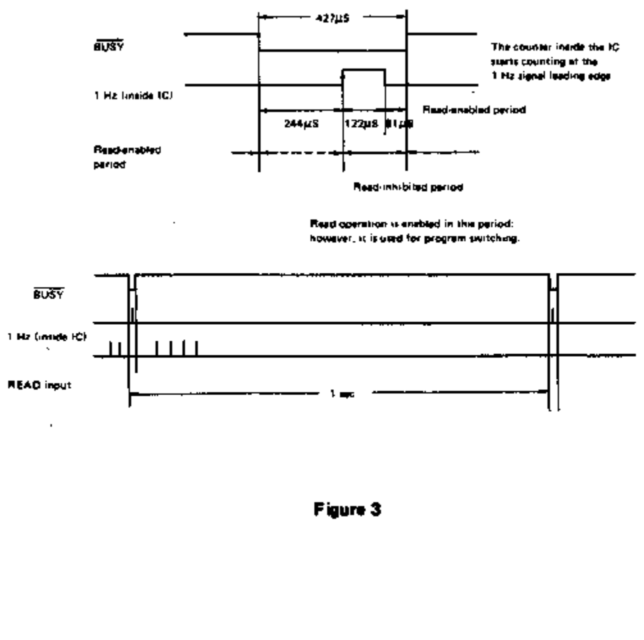


Figure 3

If the counter operation is stopped by setting the STOP input to the H level, read operations are enabled regardless of the $\overline{BUSY}$ output.
A read operation is enabled by microcomputer software regardless of the $\overline{BUSY}$ output during the counter operation by setting the STOP input to the L level.
In this method, read operations are performed two or more times continuously and data that matches twice is used as guaranteed data.

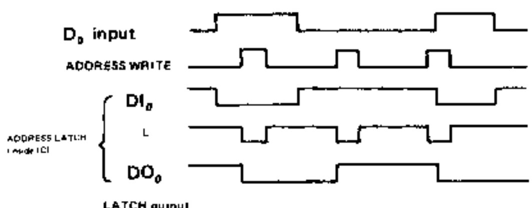
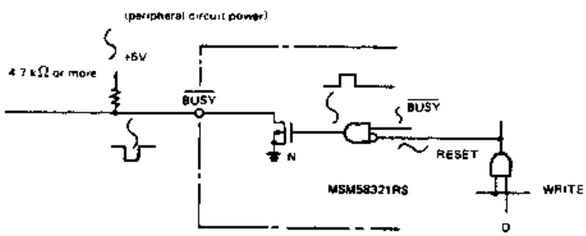
<table>
<tr><th>Name</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>$D_0 \sim D_3$</td><td>4~7</td><td>Data input/output pins. (Bidirectional bus). The output is a open-drain type and 4.7 kΩ ~ 10 kΩ pull-up registers are required utilize these pins as output pins.</td></tr>
<tr><td>GND</td><td>8</td><td>Ground pin.</td></tr>
<tr><td>ADDRESS WRITE</td><td>9</td><td>ADDRESS WRITE pin is used to load address information from the D0 – D3 I/O bus pins to the ADDRESS LATCH inside the IC; it is activated when it is at the H level. This input is activated by the level, not by the edge. Figure 4 shows the relationships between the D0 address input, ADDRESS WRITE input, and ADDRESS LATCH input/output.


Figure 4</td></tr>
<tr><td>$\overline{BUSY}$</td><td>10</td><td>$\overline{BUSY}$ pin outputs the IC operation state. It is N-channel MOSFET open-drain output. An external pull-up resistor of 4.7 kΩ or more must be connected (see Figure 5) to use the $\overline{BUSY}$ output. The signals are output in negative logics. If the oscillator oscillates at 32.768 kHz, the frequency is always 1 Hz regardless of the CS1 and CS2 unless the D output of the ADDRESS DECODER inside the IC is H (CODE = H·L·H·H) and CS1 = CS2 = WRITE = H.
Figure 6 shows the $\overline{BUSY}$ output time chart.


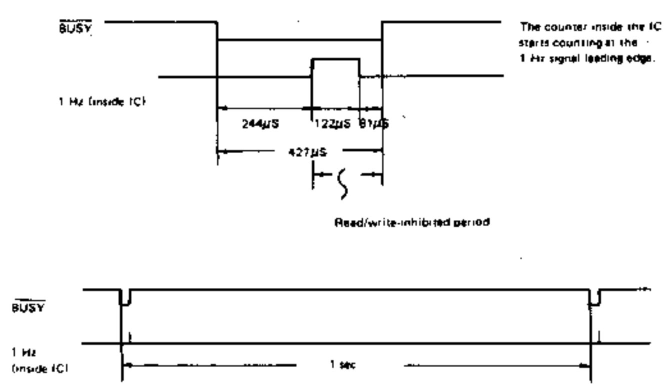


Figure 6</td></tr>
</table>

<table>
<tr><th>Name</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>STOP</td><td>11</td><td>The STOP pin is used to input on/off control for a 1 Hz signal. When this pin goes to the H level, 1 Hz signals are inhibited and counting for all digits succeeding the S1 digit is stopped. When this pin goes to the L level, normal operations are performed; the digits are counted up. This STOP input controls stopping digit counting. Writing of external data in digits can be assured by setting the STOP input to the H level to stop counting, then writing sequentially from the low-order digits.</td></tr>
<tr><td>TEST</td><td>12</td><td>
The TEST pin is used to test this IC; it is normally open or connected to GND. It is recommended to connect it to GND to safeguard against malfunctions from noise.
The TEST pulse can be input to the following nine digits:
S1, S10, MI10, H1, D1(W), M01, Y1 and Y10
When a TEST pulse is input to the D1 digit, the W digit is also counted up simultaneously.

Input a TEST pulse as follows:
Set the address to either digit explained above, then input a pulse to the TEST pin while CS1 = CS2 = STOP = H and WRITE = L. The specified and succeeding digits are counted up. (See Figure 7)

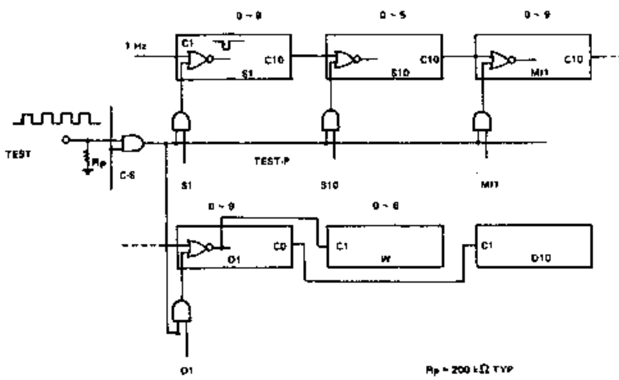
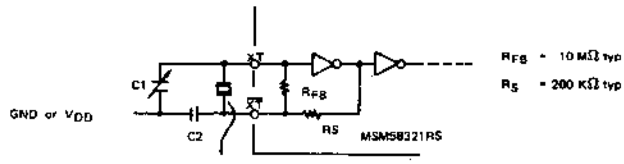


Figure 7

A digit is counted up at the leading edge (changing point from L to H) of a TEST pin input pulse. The pulse condition for TEST pin input at V_{DD} = 5 V ±5% is described in Figure 8 below.

Figure 8
</td></tr>
</table>

<table>
<tr><th>Name</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>$\overline{XT}$
XT</td><td>14
15</td><td>Oscillator pin. A 32.768kHz crystal oscillator, capacitor and trim capacitor for frequency adjustment are to be connected as shown in Figure 8 below.



X-TAL 32.768 kHz, The crystal impedance is 30 kΩ or less.

Figure 8

If an external clock is to be used for MSM58321RS's oscillation source, the external clock is to be input to XT, while $\overline{XT}$ should be left open. Refer to the Figure 9 below.

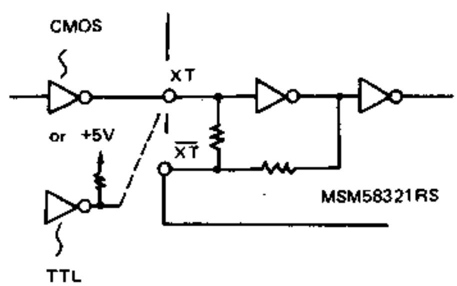


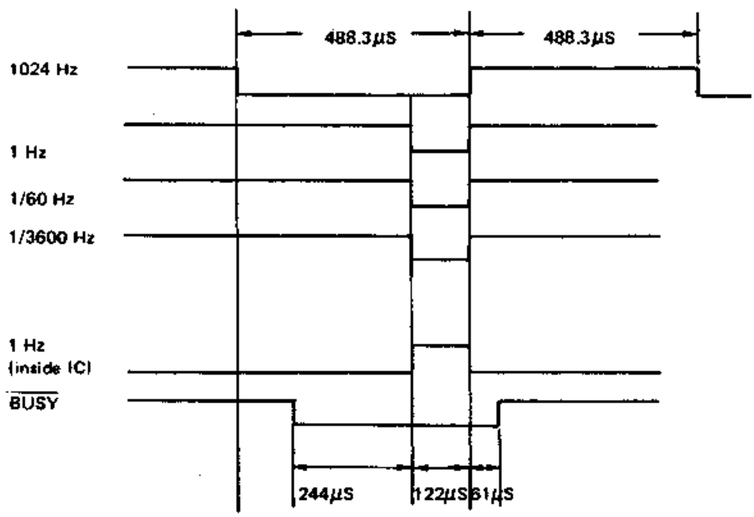
Figure 9</td></tr>
<tr><td>V_{DD}</td><td>16</td><td>Power supply pin. Refer to the application circuit.</td></tr>
</table>

5

REFERENCE SIGNAL OUTPUT

Reference signals are output from the D0 – D3 pins under the following conditions:

Conditions	Output pin	Reference signal frequency	Pulse width	Output logic
WRITE = L	D_0	1024 Hz	488.3 μs	Positive logic
READ = H	D_1	1 Hz	122.1 μs	Negative logic
CS1 = CS2 = H	D_2	1/60 Hz	122.1 μs	Negative logic
ADDRESS = E or F	D_3	1/3600 Hz	122.1 μs	Negative logic



$$122.1\mu S = \frac{10^{-3}}{32{,}768} \times 4$$

$$488.3\mu S = \frac{10^{-3}}{32{,}768} \times 16$$

Figure 10

APPLICATION NOTES

■ WRITE and STOP

Note that the timing relationships between the STOP and WRITE inputs vary by the related digit when counting is stopped by the STOP input to write data. The time (t_{SH}) between the STOP input leading edge and WRITE input trailing edge for each digit is limited to the minimum value. (See Figure 11)

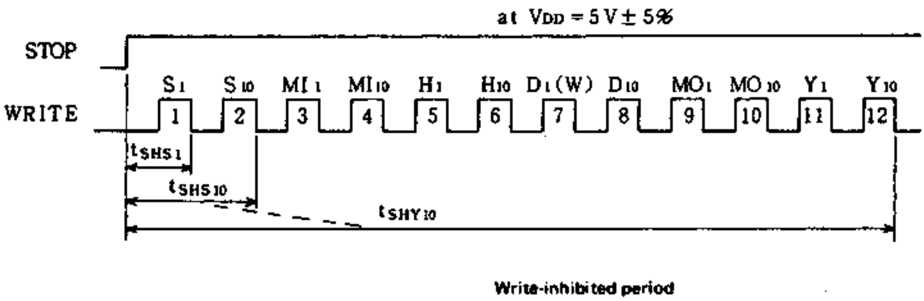


Figure 11

t_{SHS1} = 1 μs, t_{SHS10} = 2 μs, t_{SHMI1} = 3 μs, t_{SHM10} = 4 μs, t_{SHH1} = 5 μs
t_{SHH10} = 6 μs, t_{SHD1} = 7 μs, $t_{SHW'}$ = 7 μs, t_{SHD10} = 8 μs, t_{SHMO1} = 9 μs
t_{SHMO10} = 10 μs, t_{SHY1} = 11 μs, t_{SHY10} = 12 μs.

5

If a count operation is continued by setting the STOP input to the L level, write operation must be performed, in principle, while the $\overline{\text{BUSY}}$ output is at the H level. While the $\overline{\text{BUSY}}$ output is at the L level, count operations are performed by the digit counters and write operation is inhibited, but there is a marginal period of 244 μs from the $\overline{\text{BUSY}}$ output trailing edge. If the $\overline{\text{BUSY}}$ output goes to the L level during a write operation, the write operation is stopped temporarily within 244 μs and it is restarted when the $\overline{\text{BUSY}}$ output goes to the H level again. Figure 12 shows a time chart of $\overline{\text{BUSY}}$ output, 1 Hz signal inside the IC, and WRITE input.

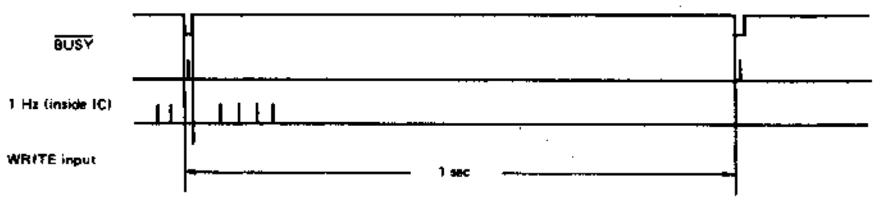


Figure 12

■ Frequency divider and $\overline{\text{BUSY}}$ circuit reset

If A0–A3 = H·L·H·H is input to ADDRESS DECODER, the DECODER output (D) goes to the H level. If CS1 = CS2 = H and WRITE = H in this state, the 5 poststages in the 15-stage frequency divider and the $\overline{\text{BUSY}}$ circuit are reset.

In this period, the $\overline{\text{BUSY}}$ output remains at the H level and the 1 Hz signal inside the IC remains at the L level, and counting is stopped. If this reset is inactivated while the oscillator operates, the $\overline{\text{BUSY}}$ output goes to the L level after 1000.1221 ±31.25 ms and the 1 Hz signal inside the IC goes to the H level after 1000.3663 ±31.25 ms. These times are not the same because the first ten stages in the 15-stage frequency divider are not reset. (See Figure 13)

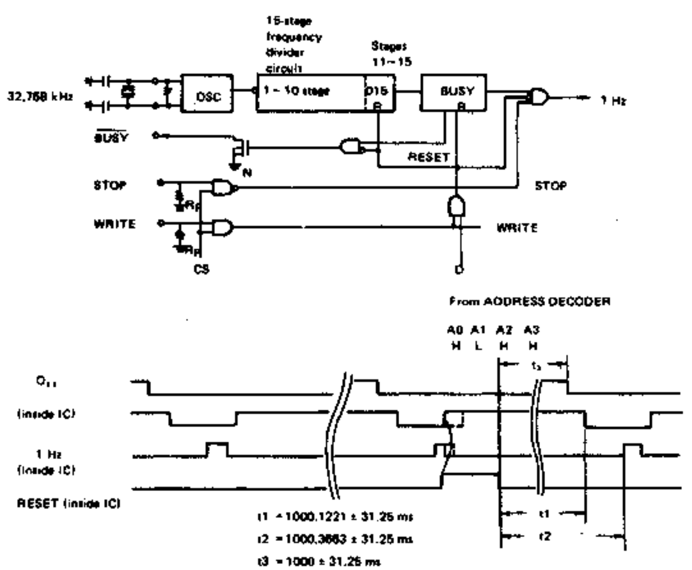


Figure 13

■ Selection of leap year

This IC is designed to select leap year automatically.

Four types of leap years can be selected by writing a select signal in the D2 and D3 bits of the D10 digit (CODE = L·L·L·H). (See Table 1 for the functions.)

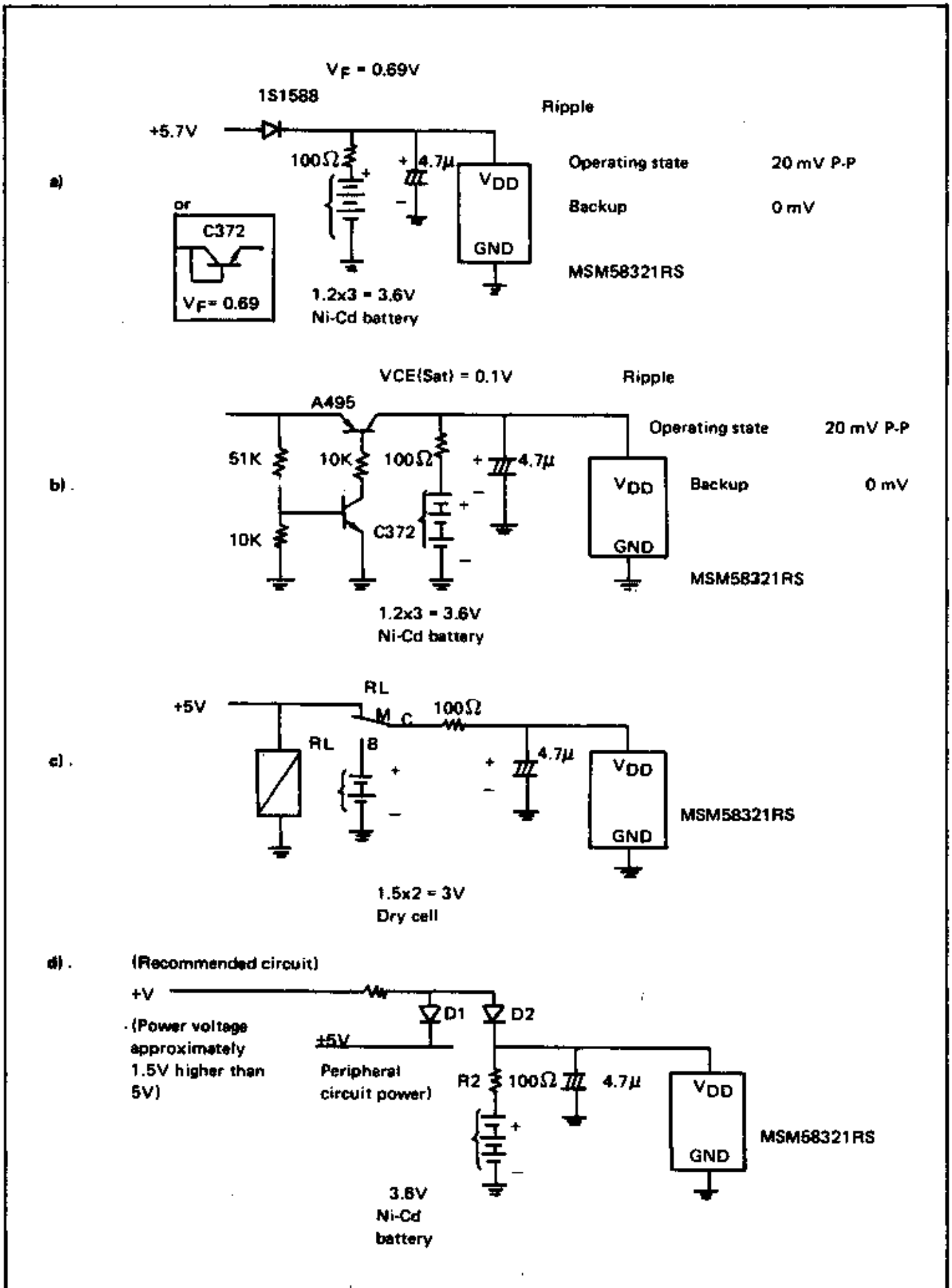
Gregorian calendar, Japanese Showa, or other calendars can be set arbitrarily in the Y1 and Y2 digits of this IC. There is a leap year every four years and the year number varies according to whether the Gregorian calendar or Showa is used. There are four combinations of year numbers and leap years. (See the Table below).

No. 1: Gregorian calendar year. The remainder obtained by dividing the leap year number by 4 is 0.
No. 2: Showa year. The remainder obtained by dividing the leap year number by 4 is 3.
No. 3: The remainder obtained by dividing the leap year number by 4 is 2.
No. 4: The remainder obtained by dividing the leap year number by 4 is 1.

No. 1	Calendar	D10 digit		Remainder obtained by dividing the leap year number by 4	Leap years (examples)
		D2	D3		
1	Gregorian	L	L	0	1980, 1984, 1988, 1992, 1996, 2000, 2004
2	Showa	H	L	3	(83) (87) (91) (95) (99) 55, 59, 63, 67, 71, 75, 79
3		L	H	2	82, 86, 90, 94, 98, 102, 106
4		H	H	1	81, 85, 89, 93, 97, 101, 105

5

APPLICATION EXAMPLE - POWER SUPPLY CIRCUIT



Note: Use the same diodes for D1 and D2 to reduce the level difference between +5V and V_{DD} of the MSM58321RS.

OKI semiconductor

MSM6242BRS/GS-VK/JS

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM6242B is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microprocessor/Microcomputer applications. An on-chip 32.768KHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS0}$, CS1), $\overline{WRITE}$, $\overline{READ}$, and ALE. Control Registers D, E and F provide for 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the ITRPT/STND (INTERRUPT/STANDARD). Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The MSM6242B can operate in a 12/24 hour format and Leap Year timing is automatic.

The MSM6242B normally operates from a 5V ± 10% supply at −30 to 85° C. Battery backup operation down to 2.0V allows continuation of time keeping when main power is off. The MSM6242B is offered in a 18-pin plastic DIP, a 24-pin FLAT package, and a 18-pin PLCC package.

FEATURES

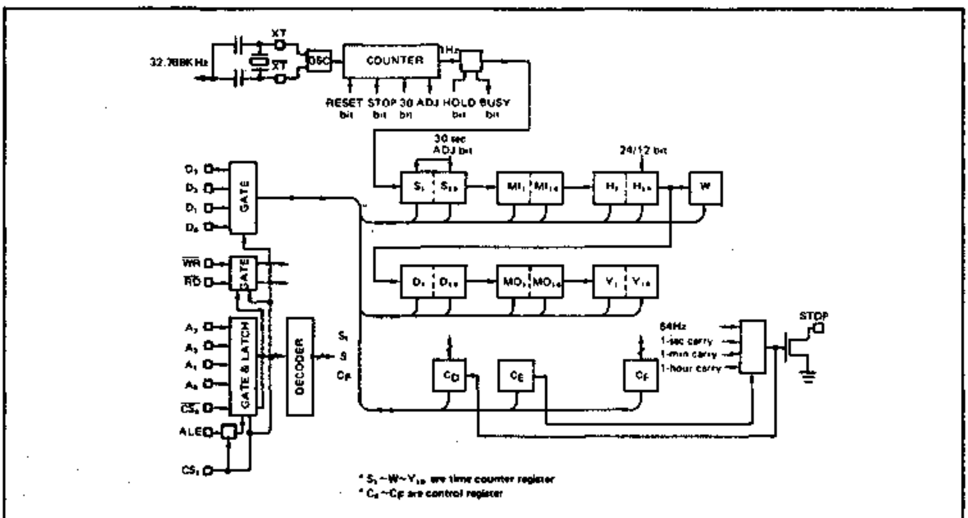
DIRECT MICROPROCESSOR/MICROCONTROLLER BUS CONNECTION

TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	80	7

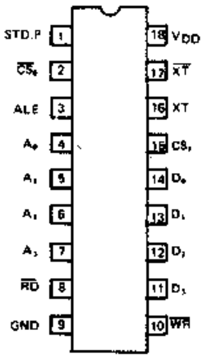
- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$, ALE and CHIP SELECT INPUTS
- Status registers — IRQ and BUSY
- Selectable interrupt outputs — 1/64 second, 1 second, 1 minute, 1 hour
- Interrupt masking
- 32.768KHz crystal controlled operation
- 12/24 hour format
- Auto leap year
- ±30 second error correction
- Single 5V supply
- Battery backup down to V_{DD} = 2.0V
- Low power dissipation:
  20 µW max at V_{DD} = 2V
  150 µW max at V_{DD} = 5V
- 18-pin plastic DIP, 24-pin FLAT and 18-pin PLCC package

5

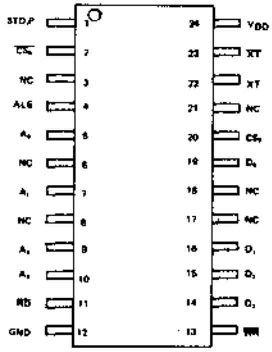
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



18 pin Plastic DIP Package



24 pin Plastic Flat Package

A0-A3:	Address input
D0-D3:	Data input/output
$\overline{CS0}$, $\overline{CS_1}$	CHIP SELECTS 0, 1
$\overline{RD}$:	READ enable
$\overline{WR}$:	WRITE enable
ALE:	Address latch enable
STD.P:	Standard pulse output
XT, $\overline{XT}$:	XTAL oscillator input/output
VDD:	+5V supply
VSS:	ground

REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count value	Description
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 ~ 9	1-second digit register
1	0	0	0	1	S_{10}	*	S_{40}	S_{20}	S_{10}	0 ~ 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 ~ 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 ~ 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 ~ 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/ AM	h_{20}	h_{10}	0 ~ 2 or 0 ~ 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 ~ 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 ~ 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 ~ 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 ~ 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 ~ 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 ~ 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 ~ 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	–	Control Register D
E	1	1	1	0	C_E	t_1	t_0	ITRPT /STND	MASK	–	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	–	Control Register F

REST = RESET
ITRPT/STND = INTERRUPT/STANDARD

Note 1) – Bit * does not exist (unrecognized during a write and held at "0" during a read).
Note 2) – Be sure to mask the AM/PM bit when processing 10's of hour's data.
Note 3) – BUSY bit is read only. The IRQ FLAG bit can only be set to a "0". Setting the IRQ FLAG to a "1" is done by hardware.

Figure 1. Register Table

OSCILLATOR FREQUENCY DEVIATIONS

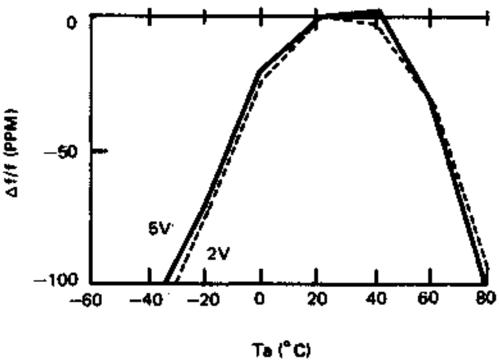


Figure 2. Frequency Deviation (PPM) vs Temperature

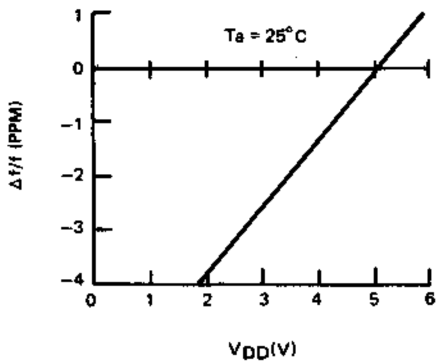
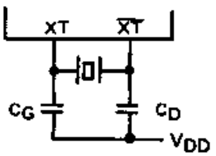


Figure 3. Frequency Deviation (PPM) vs Voltage

Note: 1. The graphs above showing frequency deviation vs temperature/voltage are primarily characteristic of the MSM6242B with the oscillation circuit described below.



Crystal: Type N_4, P_3 by kinseki (32.768 KHz)

C_G, C_D: 22pF (Temperature Characteristics: 0)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3~ 7	V
Input Voltage	V_I	Ta = 25°C	GND − 0.3~V_{DD} + 0.3	V
Output Voltage	V_O	Ta = 25°C	GND − 0.3~V_{DD} + 0.3	V
Storage Temperature	T_{STG}		−55~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	–	4 ~ 6	V
Standby Supply Voltage	V_{BAK}	–	2 ~ 6	V
Crystal Frequency	$f_{(XT)}$	–	32.768	kHz
Operating Temperature	T_{OP}	–	−30~+85	°C

D.C. CHARACTERISTICS

V_{DD} = 5V ± 10%, T_A = −30 ~ +85

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage	$V_{IH}1$	–	2.2	–	–	V	All input terminals except CS_1
"L" Input Voltage	$V_{IL}1$	–	–	–	0.8	V	All input terminals except CS_1
Input Leak Current	$I_{LK}1$	V_I = V_{DD}/0V	–	–	1/−1	μA	Input terminals other than $D_0 \sim D_3$
Input Leak Current	$I_{LK}2$	V_I = V_{DD}/0V	–	–	10/−10	μA	$D_0 \sim D_3$
"L" Output Voltage	$V_{OL}1$	I_{OL} = 2.5mA	–	–	0.4	V	$D_0 \sim D_3$
"H" Output Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–	V	$D_0 \sim D_3$
"L" Output Voltage	$V_{OL}2$	I_{OL} = 2.5mA	–	–	0.4	V	STD.P
OFF Leak Current	I_{OFFLK}	V = V_{DD}/0V	–	–	10	μA	STD.P
Input Capacitance	C_I	Input frequency 1MHz	–	5	–	PF	All input terminals
Current Consumption	$I_{DD}1$	$f_{(xt)}$ = 32.768 KHz T_a=25°C, V_{DD} = 5V	–	–	30	μA	V_{DD}
Current Consumption	$I_{DD}2$	$f_{(xt)}$ = 32.768 KHz T_a=25°C, V_{DD} = 2V	–	–	10	μA	V_{DD}
"H" Input Voltage	$V_{IH}2$	V_{DD} = 2~5.5V	4/5V_{DD}	–	–	V	CS_1
"L" Input Voltage	$V_{IL}2$	V_{DD} = 2~5.5V	–	–	1/5V_{DD}	V	CS_1

SWITCHING CHARACTERISTICS

(1) WRITE mode (ALE = V_{DD})

(V_{DD} = 5V ± 10% = Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before WRITE	t_{AW}	–	20	–	
Address Stable After WRITE	t_{WA}	–	10	–	
WRITE Pulse Width	t_{WW}	–	120	–	
Data Set up Time	t_{DS}	–	100	–	
Data Hold Time	t_{DH}	–	10	–	

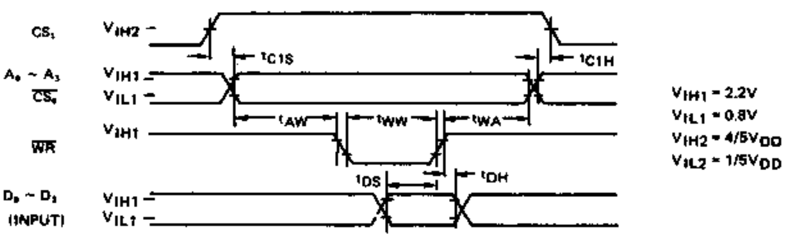


Figure 4. Write Cycle — (ALE = VDD)

(2) WRITE mode (With use of ALE)

(V_{DD} = 5 V ± 10%, Ta = –3C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{CIS}	–	1000	–	ns
Address Set up Time	t_{AS}	–	25	–	
Address Hold Time	t_{AH}	–	25	–	
ALE Pulse Width	t_{AW}	–	40	–	
ALE Before WRITE	t_{ALW}	–	10	–	
WRITE Pulse Width	t_{WW}	–	120	–	
ALE After WRITE	t_{WAL}	–	20	–	
DATA Set up Time	t_{DS}	–	100	–	
DATA Hold Time	t_{DH}	–	10	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

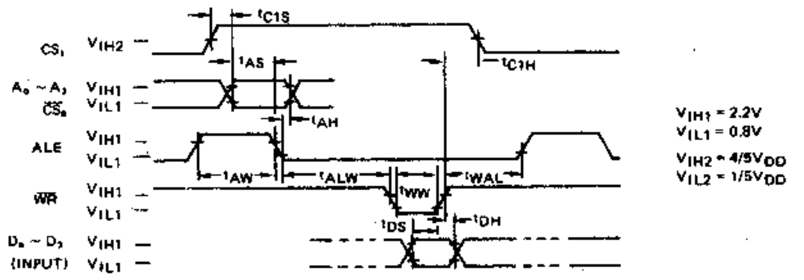


Figure 5. Write Cycle – (With Use of ALE)

(3) READ mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before READ	t_{AR}	–	20	–	
Address Stable After READ	t_{RA}	–	0	–	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	–	120	
Data Hold	t_{DR}	–	0	–	

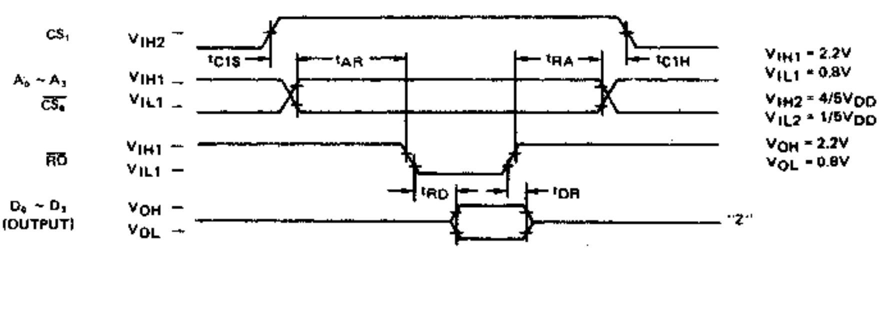


Figure 6. Read Cycle – (ALE = VDD)

(4) READ mode (With use of ALE)

(V_{DD} = 5V ±10%, Ta = −30~+85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
Address Set up Time	t_{AS}	–	25	–	
Address Hold Time	t_{AH}	–	25	–	
ALE Pulse Width	t_{AW}	–	40	–	
ALE Before READ	t_{ALR}	–	10	–	
ALE after READ	t_{RAL}	–	10	–	
RD to Data	t_{RD}	C_L = 150pF	–	120	
DATA Hold	t_{DR}	–	0	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

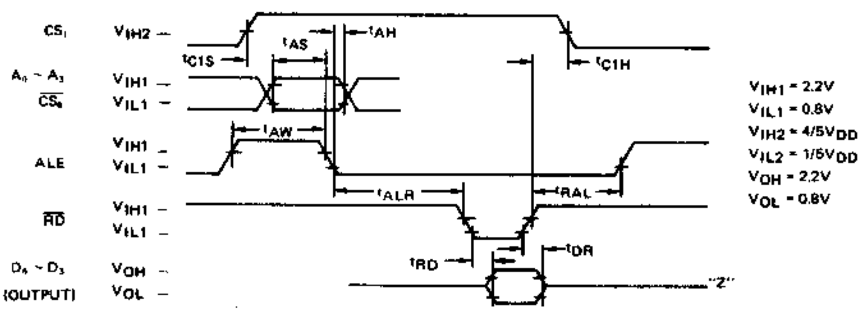
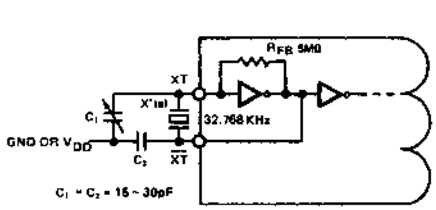


Figure 7. Read Cycle – (With Use of ALE)

5

PIN DESCRIPTION

Name	Pin No. RS	Pin No. GS	Description
D_0	14	19	Data Input/Output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers. D0 = LSB and D3 = MSB.
D_1	13	16	
D_2	12	15	
D_3	11	14	
A_0	4	5	Address input pin for use by a microcomputer to select internal clock/calendar's registers and control registers for Read/Write operations (See Function Table Figure 1). Address input pins A0-A3 are used in combination with ALE for addressing registers.
A_1	5	7	
A_2	6	9	
A_3	7	10	
ALE	3	4	Address Latch Enable pin. This pin enables writing of address data when ALE = 1 and $\overline{CS0}$ = 0; address data is latched when ALE = 0 Microcontroller/Microprocessors having an ALE output should connect to this pin; otherwise it should be connected at V_{DD}.
$\overline{WR}$	10	13	Writing of data is performed by this pin. When CS_1 = 1 and $\overline{CS_0}$ = 0, D_0 ~ D_3 data is written into the register at the rising edge of $\overline{WR}$.
$\overline{RD}$	8	11	Reading of register data is accomplished using this pin. When CS_1 = 1, $\overline{CS_0}$ = 0 and $\overline{RD}$ = 0, the data of the register is output to D_0 ~ D_3. If both $\overline{RD}$ and $\overline{WR}$ are set at 0 simaltanuously, $\overline{RD}$ is to be inhibited.
$\overline{CS_0}$	2	2	Chip Select Pins. These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation. $\overline{CS_0}$ and ALE work in combination with one another, while CS_1 work independent with ALE. CS_1 must be connected to power failure detection as shown in Figure 18.
CS_1	15	20	
STD.P	1	1	Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1. Refer to Figure 9 and FUNCTIONAL DESCRIPTION OF REGISTERS.
XT	16	22	32.768 kHz crystal is to be connected to these pins. When an external clock of 32.768 kHz is to be used for MSM6242's oscillation source, either CMOS output or pull-up TTL output is to be input from XT, while $\overline{XT}$ should be left open.
$\overline{XT}$	17	23	
V_{DD}	18	24	Power supply pin. +2 ~ +6V power is to be applied to this pin.
GND	9	12	Ground pin.



The impedance of the crystal should be less than 30kΩ

Figure 8. Oscillator Circuit

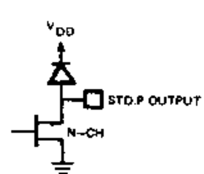


Figure 9.

FUNCTIONAL DESCRIPTION OF REGISTERS

■ S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, $\overline{MO}_1$, $\overline{MO}_{10}$, Y_1, Y_{10}, W

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.

b) All registers are logically positive. For example, (S8, S4, S2, S1) = 1001 which means 9 seconds.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

d) PM/AM, h_{20}, h_{10}
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the setting of 12-hour mode h_{20} is to be set. Otherwise it causes a discrepancy. In reading out the PM/AM bit in the 24-hour mode, it is continuously read out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously read out as 0 unless 1 is being written into this bit.

e) Registers Y1, Y10, and Leap Year. The MSM62428 is designed exclusively for the Christian Era and is capable of identifying a leap year automatically. The result of the setting of a non-existant day of the month is shown in the following example: If the date February 29 or November 31, 1985, was written, it would be changed automatically to Match 1, or December 1, 1985 at the exact time at which a carry pulse occurs for the day's digit.

f) The Register W data limits are 0–6 (Table 1 shows a possible data definition).

TABLE 1

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

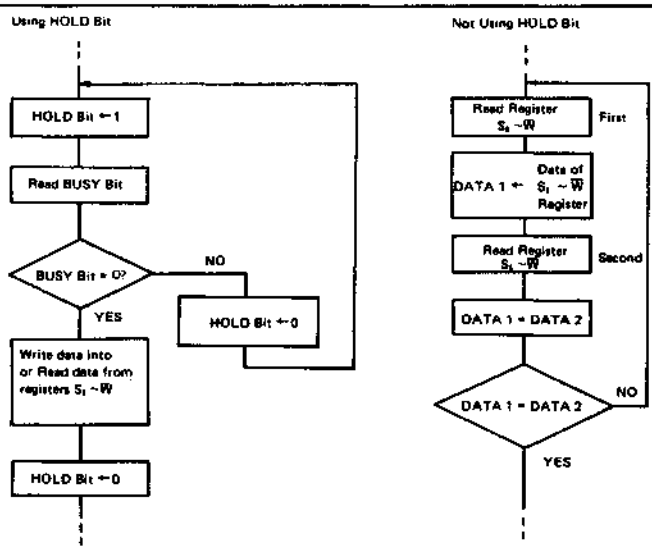
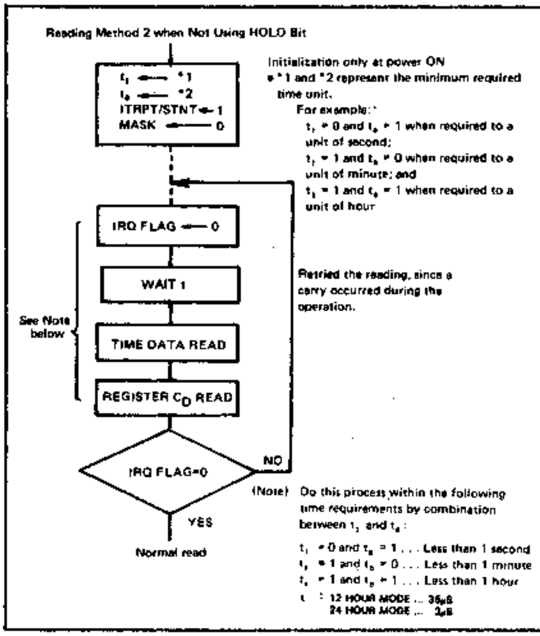
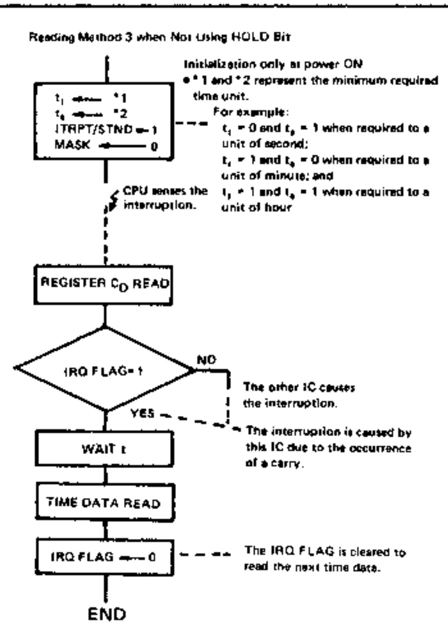


Figure 10. Reading and Writing of Registers S_1 ~ $\overline{W}$





■ CD REGISTER (Control D Register)

a) HOLD (D0) – Setting this bit to a "1" inhibits the 1Hz clock to the S1 counter, at which time the Busy status bit can be read. When Busy = 0, register's S_1 ~ $\overline{W}$ can be read or written. During this procedure if a carry occurs the S1 counter will be incremented by 1 second after HOLD = 0 (this condition is guaranteed as long as HOLD = 1 does not exceed 1 second in duration). If CS1 = 0 then HOLD = 0 irrespective of any condition.

b) BUSY (D1) – Status bit which shows the interface condition with microcontroller/microprocessors. As for the method of writing into and reading from S_1 ~ $\overline{W}$ (address ϕ ~ C), refer to the flow chart described in Figure 10.

c) IRQ FLAG (D2) – This status bit corresponds to the output level of the STD.P output. When STD.P = 0, then IRQ = 1; when STD.P = 1, then IRQ = 0. The IRQ FLAG indicates that an interrupt has occurred to the microcomputer if IRQ = 1. When D0 of register C_E (MASK) = 0, then the STD.P output changes according to the timing set by D3 (t_1) and D2 (t_0) of register E. When D1 of register E (ITRPT/STND) = 1 (interrupt mode), the STD.P output remains low until the IRQ FLAG is written to a "0". When IRQ = 1 and timing for a new interrupt occurs, the new interrupt is ignored. When ITRPT/STND = 0 (Standard Pulse Output mode) the STD.P output remains low until either "0" is written to the IRQ FLAG; otherwise, the IRQ FLAG automatically goes to "0" after 7.8125 ms.

When writing the HOLD or 30 second adjust bits of register D, it is necessary to write the IRQ FLAG bit to a "1".

d) ±30 ADJ (D3) – When 30-second adjustment is necessary, a "1" is written to bit D3 during which time the internal clock registers should not be read from or written to 125μs after bit D3 = 1 it will automatically return to a "0", and at that time reading or writing of registers can occur.

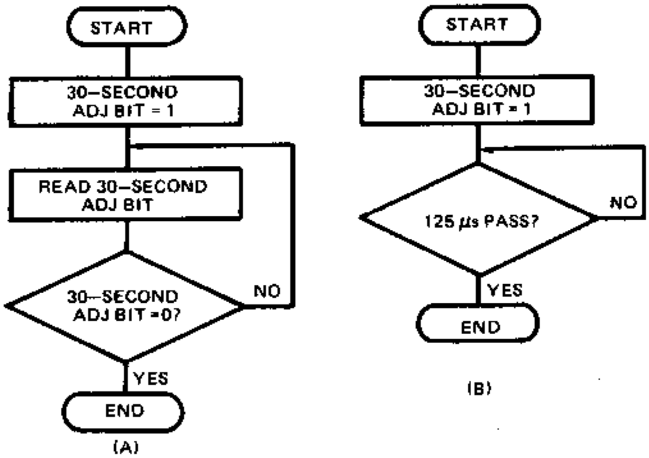


Figure 11. Writing 30-Second Adj. bit (Two Ways A, B)

■ CE REGISTER (Control E Register)

a) MASK (D0) — This bit controls the STD.P output. When MASK = 1, then STD.P = 1 (open); when MASK = 0, then STD.P = output mode. The relationship between the MASK bit and STD.P output is shown Figure 12.

b) INTRPT/STND (D1) — The INTRPT/STND input is used to switch the STD.P output between its two modes of operation, interrupt and Standard timing waveforms. When INTRPT/STND 0 a fixed cycle waveform with a low-level pulse width of 7.8125 ms is present at the STD.P output. At this time the MASK bit must equal 0, while the period in either mode is determined by T0(D2) and T1(D3) of Register E.

c) T0 (D2), T1 (D3) — These two bits determine the period of the STD.P output in both Interrupt and Fixed timing waveform modes. The tables below show the timing associated with the T0, T1 inputs as well as their relationship to INTRPT/STND and STD.P.

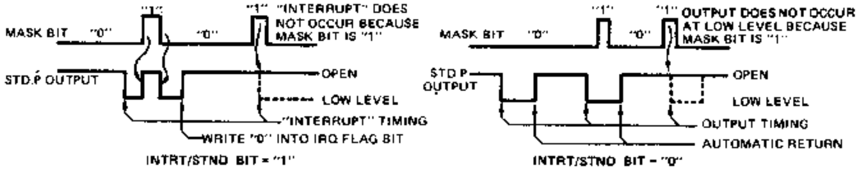


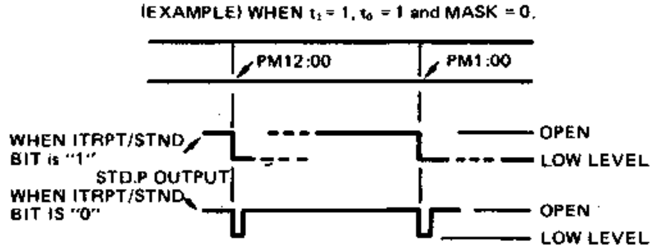
Figure 12.

t_1	t_0	Period	Duty CYCLE of "0" level when ITRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

TABLE 2

5

The timing of the STD.P output designated by T1 and T0 occurs the moment that a carry occurs to a clock digit.



d) The low-level pulse width of the fixed cycle waveform (ITRPT/STND = 0) is 7.8125 ms independent of T0/T1 inputs.

e) The fixed cycle waveform mode can be used for adjustment of the oscillator frequency time base. (See Figure 14).

f) During ±30 second adjustment a carry can occur that will cause the STD.P output to go low when T0/T1 = 1,0 or 1,1. However, when T1/T0 = 0, 0 and ITRPT/STND = 0, carry does not occur and the STD.P output resumes normal operation.

g) The STD.P output is held (frozen) at the point at which STOP = 1 while ITRPT/STND = 0.

h) No STD.P output change occurs as a result of writing data to registers S1 ~ H1.

• C_F REGISTER (Control F Register)

a) REST (D0) — "RESET" — This bit is used to clear the clock's internal divider/counter of less than a second. When REST = 1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If CS1 = 0 then REST = 0 automatically.

b) STOP (D1) — The STOP FLAG Only inhibits carries into the 8192Hz divider stage. There may be up to 122μs delay before timing starts or stops after changing this flag; 1 = STOP/0 = RUN.

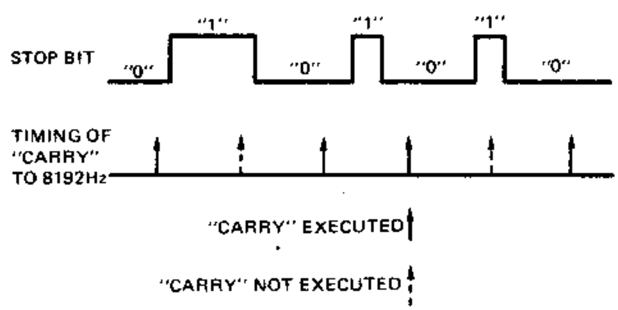


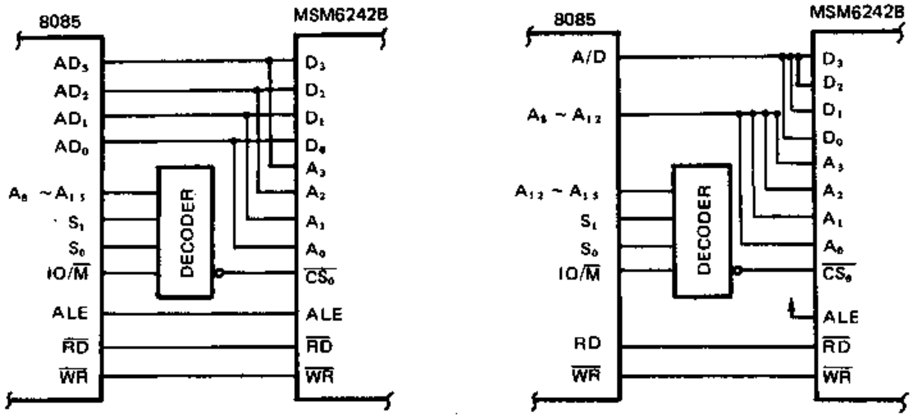
Figure 13

c) 24/12 (D2) — "24 HOUR/12 HOUR" — This bit is for selection of 24/12 hour time modes. If D2 = 1—24 hour mode is selected and the PM/AM bit is invalid. If D2 = 0—12 hour mode is selected and the PM/AM bit is valid.

Setting of the 24/12 hour bit is as follows:
1) REST bit = 1
2) 24/12 hour bit = 0 or 1
3) REST bit = 0
* REST bit must = 1 to write to the 24/12 hour bit.

d) TEST (d3) — When the TEST flag is a "1", the input to the SECONDS counter comes from the counter/divider stage instead of the 15th divider stage. This makes the SECONDS counter count at 5.4163KHz instead of 1Hz. When TEST = 1 (Test Mode) the STOP & REST (Reset) flags do not inhibit internal counting. When Hold = 1 during Test (Test = 1) internal counting is inhibited; however, when the HOLD FLAG goes inactive (Hold = 0) counter updating is not guaranteed.

TYPICAL APPLICATION INTERFACE WITH MSM6242B AND MICROCONTROLLERS



MEMORY MAPPED

I/O MAPPED

Figure 15.

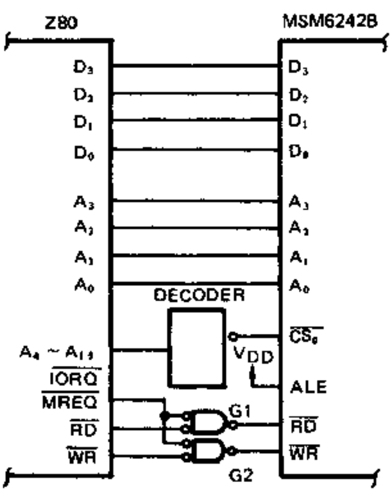


Figure 16.

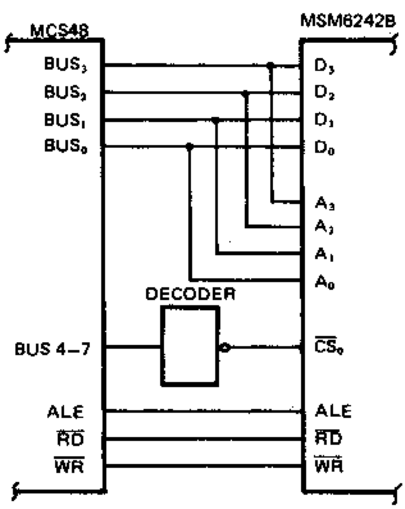


Figure 17.

TYPICAL APPLICATIONS – INTERFACE WITH MSM80C49

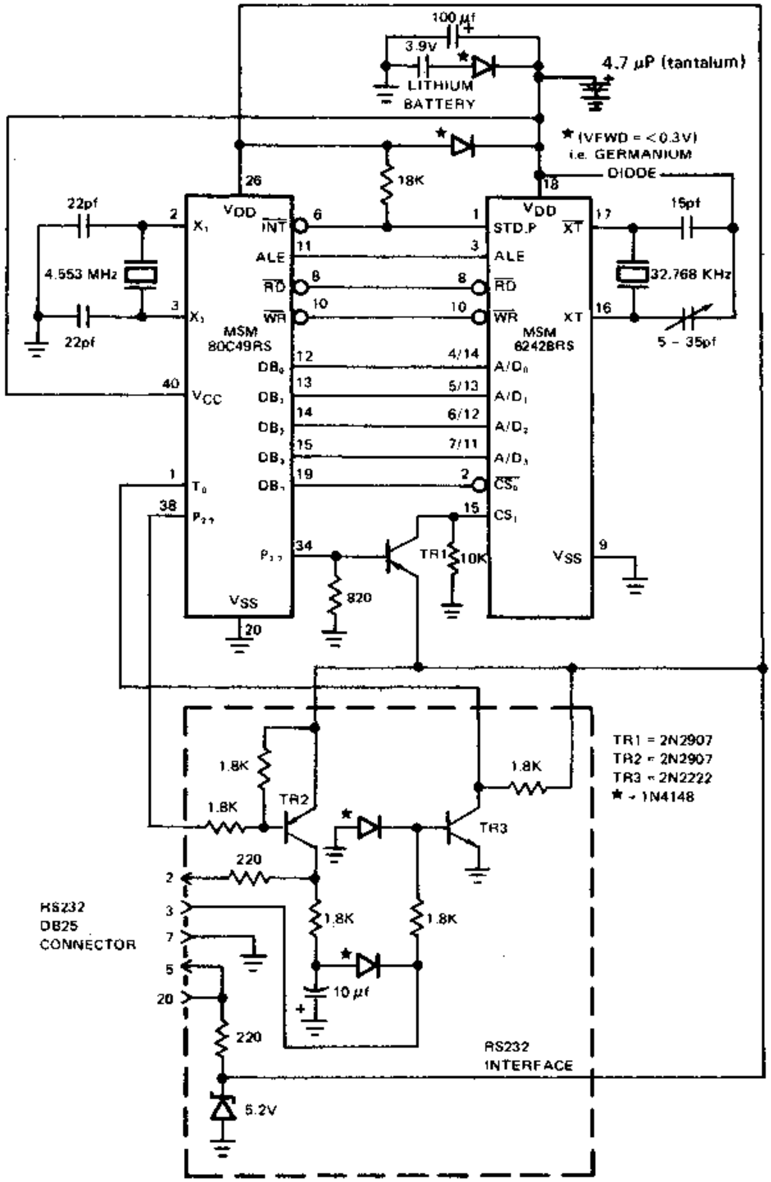
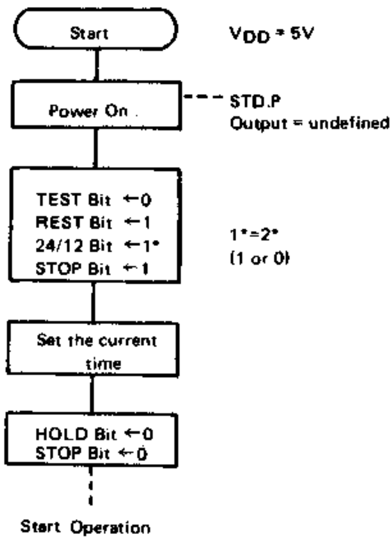


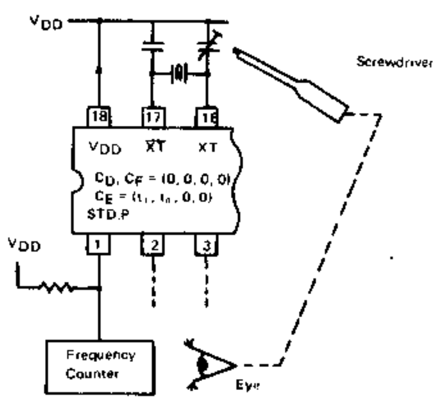
Figure 18.

APPLICATION NOTE

1. Power Supply

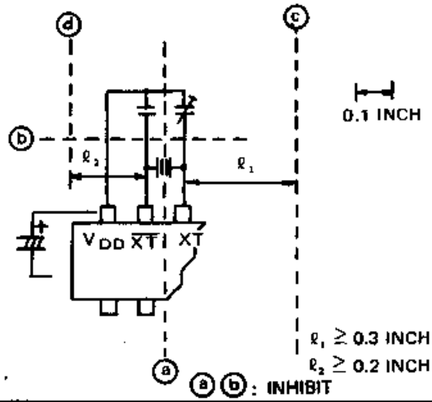


2. Adjustment of Frequency



$C_D \sim C_F$ are to be set at as described in the figure and the capacitor is to be adjusted to meet the settle frequency of t_0 and t_1.
If the right oscillation can not be obtained,

1. Check the waveform of $\overline{XT}$
2. Check $C_D \sim C_F$ content
3. Check the noise.



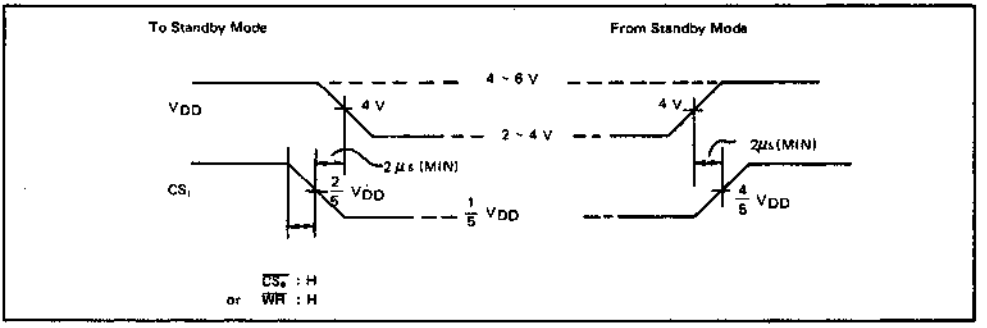
3. CH_1 (Chip Select)

V_{IH} and V_{IL} of CH_1 has 3 functions.

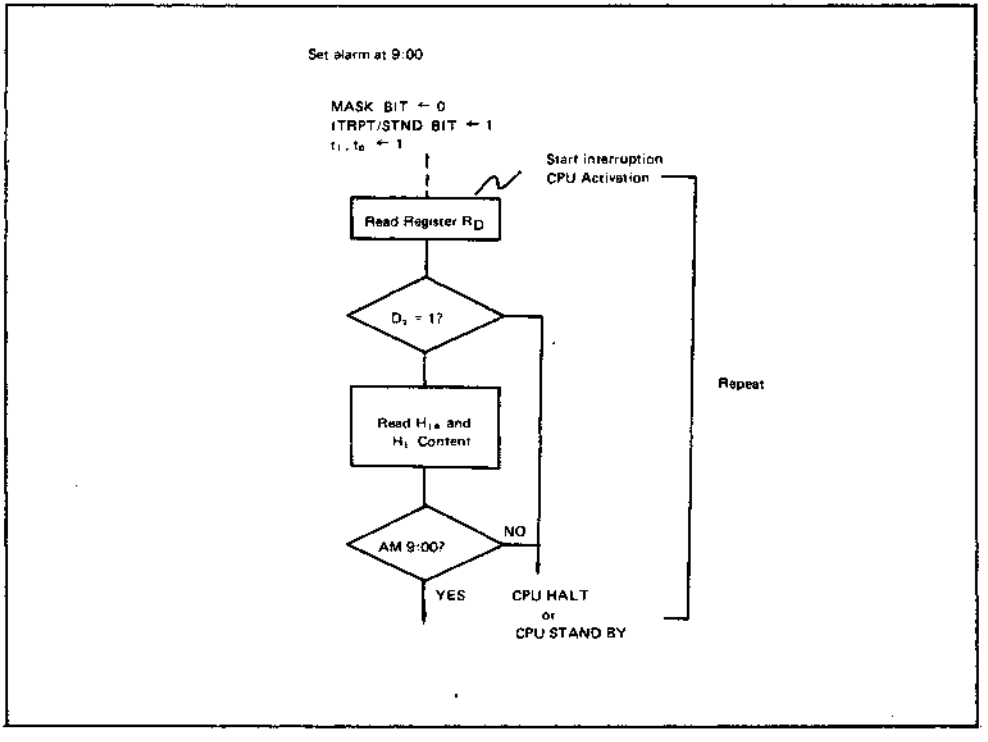
a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

a) More than 4/5 V_{DD} should be applied to the MSM6242B for the interface with a microcontroller/microprocessor in 5V operation.
b) In moving to the standby mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0V should be applied.
c) To and from the standby mode, obey following Timing chart.



4. Set STD.P at arlarm mode



TYPICAL APPLICATION – POWER SUPPLY CIRCUIT

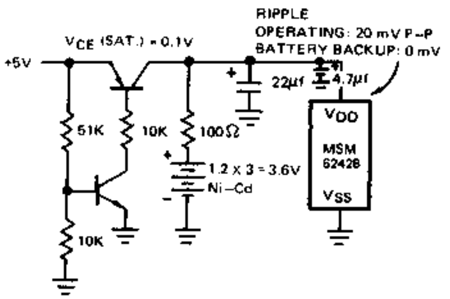


Figure 19.

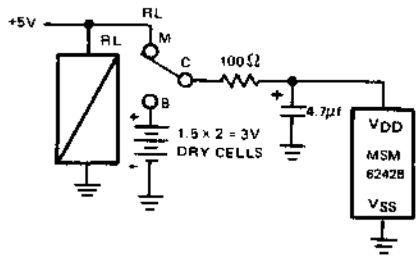


Figure 20.

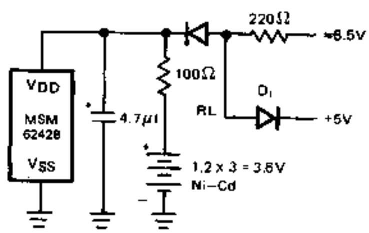
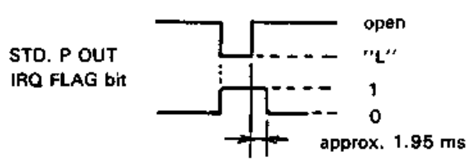


Figure 21.

4.7 µF: tantalum

SUPPLEMENTARY DESCRIPTION

- When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec ADJ bit and the HOLD bit, the IRQ FLAG = 1 and was generated before the writing and IRQ FLG = 1 generated in a moment then will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1"
- Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0, or ITRPT/STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.
- The relationship between SDT. P OUT and IRQ FLAG bit is shown below:



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