μPD2732
μPD2732-4
32,768 (4K × 8) BIT UV ERASABLE PROM

Description

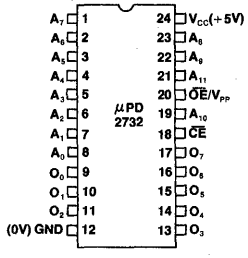
The μPD2732 is a 32,768-bit (4096 x 8 bit) Ultraviolet Erasable and Electrically Programmable Read-Only Memory (EPROM). It operates from a single +5V supply, making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with an attendant 80% savings in power consumption.

A distinctive feature of the μPD2732 is a separate output control, output enable ($\overline{OE}$) from the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2732 features fast, simple one-pulse programming controlled by TTL-level signals. Total programming time for all 32,768 bits is only 210 seconds.

Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—390 ns max
- ☐ Single location programming
- ☐ Programmable with single pulse
- ☐ Low power dissipation: 150 mA max active current, 30 mA max standby current
- ☐ Input/Output TTL-compatible for reading and programming
- ☐ Single +5V power supply
- ☐ 24-pin ceramic DIP
- ☐ Three-state outputs

Pin Configuration



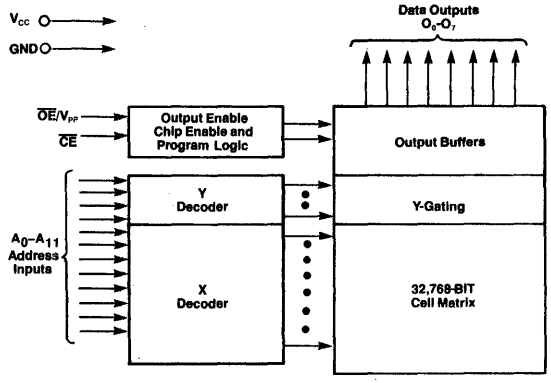
Pin Names

A_0-A_{11}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable

PINS	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	OUTPUTS
MODE				
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Table 1 – Mode Selection

Block Diagram



Absolute Maximum Ratings* (T_a = 25°C)

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.3 to +6 Volts
Input Voltage	−0.3 to +6 Volts
Supply Voltage V_{CC}	−0.3 to +6 Volts
Supply Voltage V_{PP}	−0.3 to +26.5 Volts

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance Except $\overline{OE}/V_{PP}$	C_{IN1}			6	pF	V_{IN} = 0V
$\overline{OE}/V_{PP}$ Input Capacitance	C_{IN2}			30	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			12	pF	V_{OUT} = 0V

DC Characteristics

Read Mode and Standby Mode

T_a = 0°C ~ 70°C; V_{CC} = +5V ± 5%

Parameter		Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25 V
Input Leakage Current	except $\overline{OE}/V_{PP}$	I_{LI1}			10	μA	V_{IN} = 5.25 V
	$\overline{OE}/V_{PP}$	I_{LI2}			10	μA	V_{IN} = 5.25 V
V_{CC} Current	Standby	I_{CC1}		15	30	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}/V_{PP}$ = V_{IL}
	Active	I_{CC2}		85	150	mA	$\overline{OE}/V_{PP}$ = $\overline{CE}$ = V_{IL}

4

DC Characteristics (Cont.)

Program, Program Verify and Program Inhibit Mode
T_a = 25 ± 5°C, V_{CC} = +5 V ± 5%, V_{PP} = +25 V ± 1 V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		$V_{CC}+1$	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1 mA
V_{CC} Current	I_{CC}		85	150	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}$ V_{PP}

AC Characteristics

Read Mode and Standby Mode
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			①	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			①	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{OH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: ① μPD2732 (450 ns max)
μPD2732-4 (390 ns max)

Test Conditions —
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.8 to 2.2V
Timing Measurement Reference Level:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify and Program Inhibit Mode
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +25V ± 1V

Parameter	Symbol	Limits Min	Typ	Max	Units	Test Conditions
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	
Data Valid from $\overline{CE}$	t_{DV}			1	μs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	50			ns	
V_{PP} Recovery Time	t_{VR}	2			μs	

Test Conditions —
Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1.0V and 2.0V
Output Timing Reference Level = 0.8V and 2V

Function

The μPD2732 operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the μPD2732 is achieved with a single 50 ms TTL pulse. Total programming time for all 32,768 bits is only 210 sec. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The μPD2732 features a standby mode which reduces the power dissipation from a maximum active power dissipation of 788 mW to a maximum standby power dissipation of 158 mW. This results in an 80% savings with no increase in access time.

Erasure of the μPD2732 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2732. Consequently, if the μPD2732 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the μPD2732 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15 W-sec/cm². The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000 μW/cm² power rating.

During erasure, the μPD2732 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the μPD2732 are listed in Table 1. In READ mode, the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for $\overline{OE}/V_{PP}$ which is pulsed from TTL level to 25V.

Read Mode

When $\overline{CE}$ and $\overline{OE}/V_{PP}$ are at low (0) level, READ is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2732 is placed in standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input. The active power dissipation is reduced by 80% from 788 mW to 158 mW.

Programming

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2732 is placed in programming mode by applying a high (1) level TTL signal to the $\overline{CE}$ and with $\overline{OE}/V_{PP}$ at +25V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially or at random.

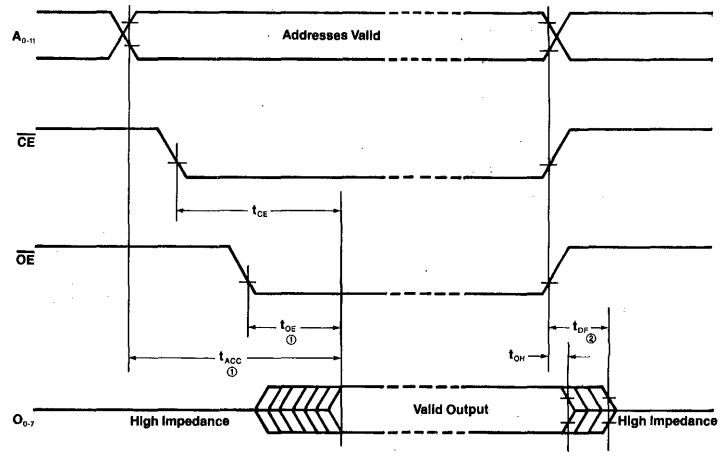
When multiple μPD2732s are connected in parallel, except for $\overline{CE}$, individual μPD2732s can be programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ input of the desired μPD2732 to be programmed.

Programming of multiple μPD2732s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ inputs.

Programming Inhibit Mode

Programming multiple μPD2732s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel μPD2732s may be common. Programming is accomplished by applying the TTL-level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +25V. A high (1) level applied to the $\overline{CE}$ of the other μPD2732 will inhibit it from being programmed.

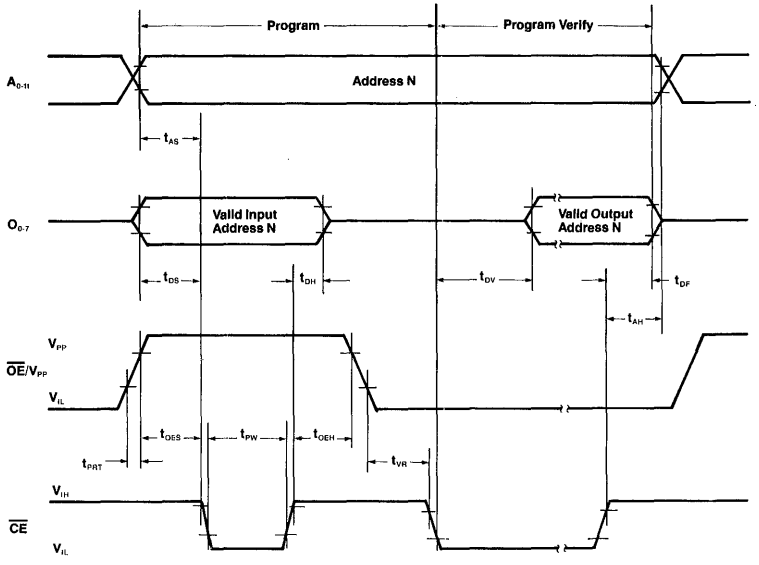
Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

4

Program Mode ①



Note: ① 0.1μF capacitor must be connected between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low (0) levels.

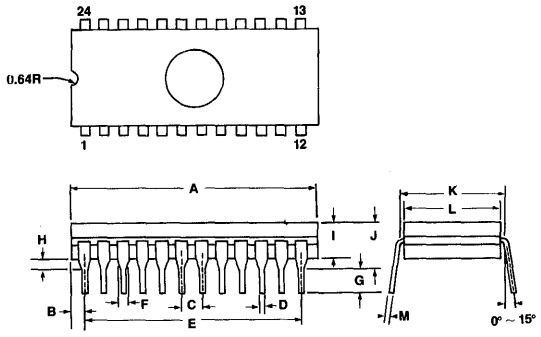
Output Deselect

The data outputs of two or more μPD2732s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2732s should be deselected by raising the $\overline{OE}/V_{PP}$ input to a TTL high.

Window Label

An amber-colored window label is provided unattached for the convenience of the user. The window label filters ultra-violet light frequencies, thus preventing accidental erasure or long-term degradation caused by ambient light or sunlight.

Package Outline μPD2732 D (Cerdip)



Item	Millimeters	Inches
A	33.5 MAX.	1.32 MAX.
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.020
I	5.0 MAX.	0.20
J	5.5 MAX.	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002