μPD2316E/EA8316E
READ ONLY MEMORY
2048 WORDS, 8 BITS/WORD

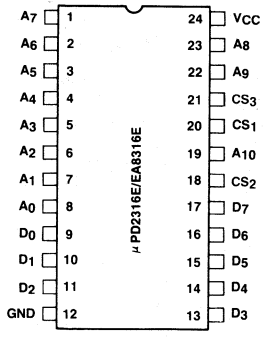
Description

The μPD2316E/EA8316E is a 16,384-bit Read Only Memory utilizing MOS N-channel silicon gate technology. The device is completely static in operation, organized as 2,048 words by 8 bits, and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has three programmable chip select inputs and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of any external logic. Programming of the device is accomplished by a custom mask during fabrication. The EA8316E pin-out is compatible with 2708 and 2716 EPROMs and can replace two 2708s or one 2716 for production. The EA8316E is available to two access time specifications, the standard 450 ns or the faster 350 ns version.

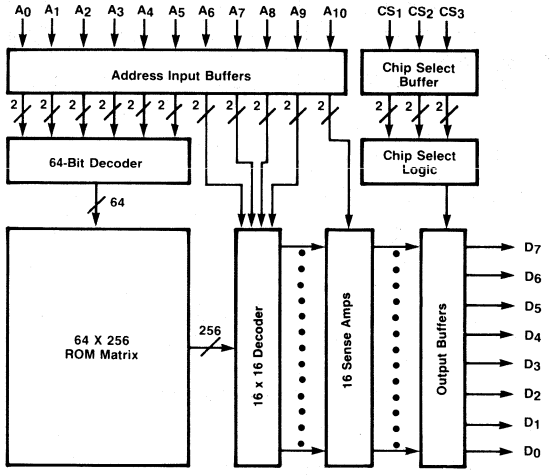
Features

- ☐ Two Fast Access Time Options
  - — 450 ns Maximum, EA8316E
  - — 350 ns Maximum, EA8316E-5
- ☐ All Outputs Drive 2 TTL Loads Directly
- ☐ All Inputs TTL Compatible
- ☐ Single +5 Volt Supply with ±5% Tolerance
- ☐ Three-State Outputs for Direct Bus Compatibility
- ☐ Three Programmable Chip Select Inputs
- ☐ Pin-Compatible to 2708 and 2716 EPROMs
- ☐ Fully Static Operation
- ☐ All Inputs Protected Against Static Charge

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

T_a = 25°C, f = 1 MHz

Voltage on All Inputs, Outputs, and Supply Pins	−0.5 to 7.0V
Maximum Junction Temperature	+150°C
θ_{JC} (Hermetic DIP)	+65°C/W
Storage Temperature	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, f = 1MHz. All pins at 0 volts.

		Limits			
Parameter	Symbol	Min	Typ	Max	Test Conditions
Input Capacitance	C_{IN}		5pF	7pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		7pF	10pF	V_{OUT} = 0V

DC Characteristics

T_a = −10°C to +70°C and V_{CC} = 5V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Load Current	I_{IL}			10	μA	V_{IN} = 0 to + 5.25V
Output "Low" Voltage	V_{OL}			0.40	V	I_{OL} = +3.2 mA
Output "High" Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Output Leakage Current	I_{LO}			10	μA	Chip disabled, V_{OUT} = +0.4V to V_{CC}
Power Supply Current	I_{CC}		60	90	mA	All inputs +5.25V, Outputs unloaded

μPD2316E/EA8316E

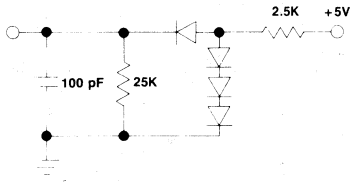
AC Characteristics

T_a = −10°C to +70°C

Parameter	Symbol	EA8316E-5 Min	EA8316E-5 Max	EA8316-E Min	EA8316-E Max	Unit
Address to Output Delay Time	t_{ACC}		350		450	ns
Chip Select to Output Delay Time	t_{CO}		150		150	ns
Chip Deselect to Output Data Float Time	t_{DF}		100		100	ns
Previous Data Valid After Address Change	t_{OH}	20		20		ns

AC Test Conditions

Input Pulse Rise and Fall Times. . . . . 20 ns
Timing Measurement Reference
Levels: . . . . . V_{IH}, V_{OH} = 2.0V; V_{OL}, V_{IL} = 0.8V.



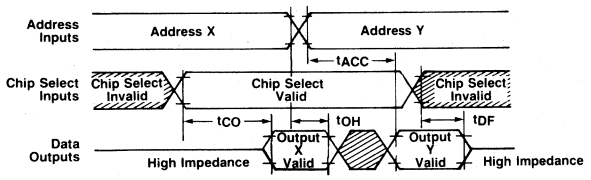
Output Load (AC): 1 TTL Load + 100 pF.

Standard Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground. Positive current flows into the referenced pin.

Output Load (AC): 2 Series 74 TTL, C_L = 100 pF
$0°C \leq t_A \leq +70°C$
$+4.75V \leq V_{CC} \leq +5.25V$

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid Address and the corresponding valid Data Out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, t_{CO}

Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

Custom Programming Instructions

Bit Pattern Submittal Options

The customer's unique bit pattern can be submitted to Electronic Arrays via several convenient methods such that it is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to EA contained within:

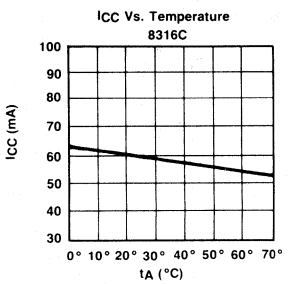
1. One programmed 2716 EPROM
2. Two programmed 2708 EPROMs
3. One customer-programmed 8316E ROM
4. Punched computer cards per the detail format shown below.

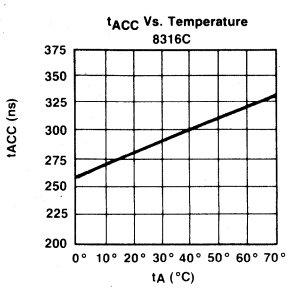
Bit Pattern Verification

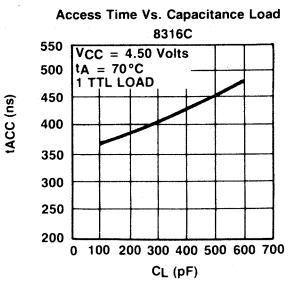
For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found by experience to be most expeditious.

Customer Pattern Submitted Via:	Verification Routine
1. One programmed 2716	Customer sends EA one additional erased 2716. EA programs the spare 2716 with the pattern data base extracted from the programmed 2716, and returns to customer for pattern verification.
2. Two programmed 2708s	Customer sends EA two additional erased 2708s. EA programs the spare 2708s with the pattern data base extracted from the programmed 2708s and returns to customer for pattern verification.

Typical Characteristics







Customer Pattern Submitted Via:	Verification Routine
3. One mask-programmed 8316E (or one 16K ROM)	Customer sends EA one erased 2716 or two erased 2708s. EA programs these EPROMs with the pattern data base extracted from the 8316 and returns to the customer for pattern verification.
4. Punched computer cards	After extracting the bit pattern from the card deck, EA's data base is used to punch a new deck. This deck, plus a complete printout, is returned to customer for pattern verification.

In all cases a computer printout of the complete bit pattern is also available upon customer request. The original 2716s, 2708s, or 8316s are retained by EA as the original bit pattern source data, at least until the first sample EA8316Es are tested and customer-approved.

The data base tape derived from the above source devices or card deck is utilized in turn to produce a pattern generator tape and ROM test pattern. The pattern generator tape drives EA's automatic pattern generation mask equipment, resulting in mask tooling that contains the customer's unique one/zero pattern. The ROM test pattern is used at production sort and final test to test each device 100% to the complete custom bit pattern.

Chip Select Level Programming

CS_1, CS_2, and CS_3 must be programmed by the customer to be selected by either a logic 1 or a logic 0 level. Accordingly, the customer must furnish EA with the desired chip selection level (1 or 0 only) for CS_1, CS_2, and CS_3, concurrent with submission of the bit pattern. The CS input logic levels are permanently established within each ROM in the same manner as the bit pattern.

Punched Computer Card Instructions

This technique requires that the customer supply EA with a deck of standard 80-column computer cards describing the data to be stored in the ROM array.

Title Card

All customer ROM "Data Cards" must be preceded by a "Title Card" which contains all unique information pertaining to that ROM other than the ROM data content. The required punching format is as follows:

Card Column No.	Card Contents
1	*(Asterisk)
2-19	Customer Name
20-21	Blank (no punch)
22-23	Month; e.g., 05 for May
24	/(slash)
25-26	Day of the month; e.g., 04 for the 4th day
27	/(slash)
28-29	The last two digits of the year
30-31	Blank
32-36	ROM Type (i.e., 8316E)
37	Blank
38-41	CS_1 =
42	CS_1 level desired for chip selection (1 or 0 only)
43	Blank
44-47	CS_2 =
48	CS_2 level desired for chip selection (1 or 0 only)
49-54	Blank
55-80	Customer part number

Alternative Data File Formats

In addition to the standard EA octal format, it is possible to furnish data to EA in other formats if prearranged with the factory. A standard hexadecimal format is currently available. Other nonstandard formats may be acceptable. Contact EA sales personnel.

Data Cards

The required punching format is described below. All addresses must be included with their outputs defined. That is, no assumptions are made regarding the bit configuration of undefined outputs. Therefore, the customer must submit cards defining the entire ROM contents, when portions of the ROM may be unused (zero).

Card Column No.	Octal Pattern Format Card Contents
1-4	Punch a 4-digit octal number representing the input address for the first of the 16 output words appearing on this card (this is the initial address).
5-7	Punch a 3-digit octal number representing the outputs for the input address specified in column 1-4.
8-10	Punch a 3-digit octal number representing the outputs for the initial input address + 1.
11-13	Punch a 3-digit octal number representing the outputs for the initial input address + 2.
—	—
—	—
—	—
50-52	Punch a 3-digit octal number representing the outputs for the initial input address + 15.
53-59	Blank
60-80	Not used by EA. May contain customer identification.

Each card, therefore, carries (in octal) the initial input address for the 16 output words contained on that card, the 16 output words themselves (in octal) and the unique ROM number. The cards must be provided for all possible sequential address locations (in blocks of 16). A 2,048-word ROM therefore, requires 128 cards, with all 16 output words defined on each card.

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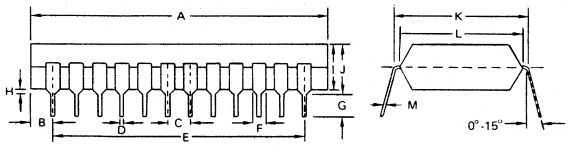
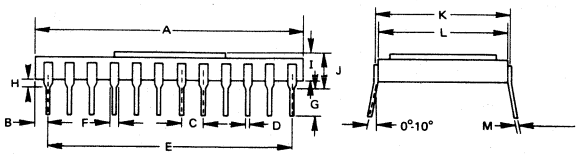
μPD2316E/EA8316E

Package Outlines
μPD2316EC
EA8316EC
Plastic



Item	Millimeters	Inches
A	33 Max	1.3 Max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 Min	0.1 Min
H	0.5 Min	0.02 Min
I	5.22 Max	0.205 Max
J	5.72 Max	0.225 Max
K	15.24	0.6
L	13.2	0.55 Max
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

μPD2316ED
EA8316ED
Ceramic



Item	Millimeters	Inches
A	30.78 Max	1.23 Max
B	1.53 Max	0.07 Max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.125 Min
H	1.02 Min	0.04 Min
I	3.23 Max	0.13 Max
J	4.25 Max	0.17 Max
K	15.24 Typ	0.60 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.010 ± 0.002