INTERSIL

IM6316
16,384 Bit (2048x8) CMOS ROM

FEATURES

- **Low standby power: 550 μW maximum**
- **High speed: 450 ns maximum**
- **On-chip address registers**
- **TTL compatible inputs and three-state outputs**
- **Single 5V supply**
- **Two mask programmable chip selects (active level latched/unlatched)**
- **Outputs mask programmable (latched/unlatched)**
- **883B Processing available**
- **Military temperature range available (—55° C to +125° C)**

GENERAL DESCRIPTION

The IM6316 is a 16,384-bit static silicon-gate CMOS read-only-memory (ROM) organized 2048 words by 8 bits. In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and two mask programmable chip-selects simplify system interfacing requirements.

The IM6316 operates over a 4.5V to 5.5V range, with an access time of 450ns and standby current of 100 μA guaranteed over the industrial temperature range.

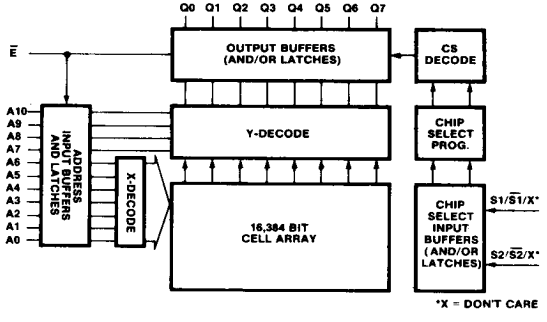
FUNCTIONAL DESCRIPTION

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle. Address and chip selects to be latched must be present a setup time (TAVEL) prior to, and a hold time (TELAX) following the falling edge of $\overline{E}$. After an access time, valid data will be available.

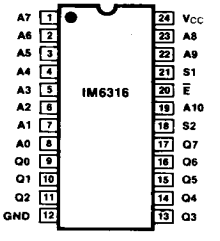
Optional latched outputs are active when S1 and S2 (or latched S1 and S2) are active. For unlatched outputs, $\overline{E}$ must also be low to enable.

Optional latches for S1 and S2 are level sensitive. When $\overline{E}$ is high, latched S1 and S2 thus perform as if they were not latched.

BLOCK DIAGRAM

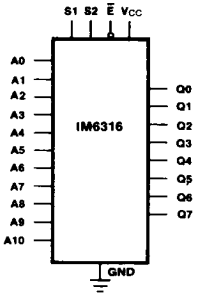


PIN CONFIGURATION



(outline dwg JG, PG)

LOGIC SYMBOL



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM6316IPG	24 PIN PLASTIC	−40°C to +85°C
IM6316IJG	24 PIN CERDIP	−40°C to +85°C
IM6316MJG	24 PIN CERDIP	−55°C to +125°C

PIN NAMES

A0-A10	ADDRESS INPUTS
Q0-Q7	DATA OUTPUTS
$\overline{E}$	ADDR. STROBE/CHIP ENABLE
S1, S2	CHIP SELECTS

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Input or Output Voltage Applied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
  Temperature
    Industrial ..... −40°C to +85°C
  Voltage
    IM6316I ..... 4.5V to 5.5V

Note:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} −2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage Current	I_{ILK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	µA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC} −0.01			V
	V_{OH}	I_{OUT} = −0.2mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
	V_{OL}	I_{OUT} = 2.0mA			0.45	
Output Leakage Current	I_{OLK}	GND ≤ V_{IN} ≤ V_{CC}	−1.0		+1.0	µA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC}			100	
Operating Supply Current	I_{CCOP}	f = 1Mhz			10	mA
Input Capacitance	C_{IN}	(Note 1)			7.0	pF
Output Capacitance	C_O	(Note 1)			10.0	

Note 1: These parameters sampled but not 100% tested.

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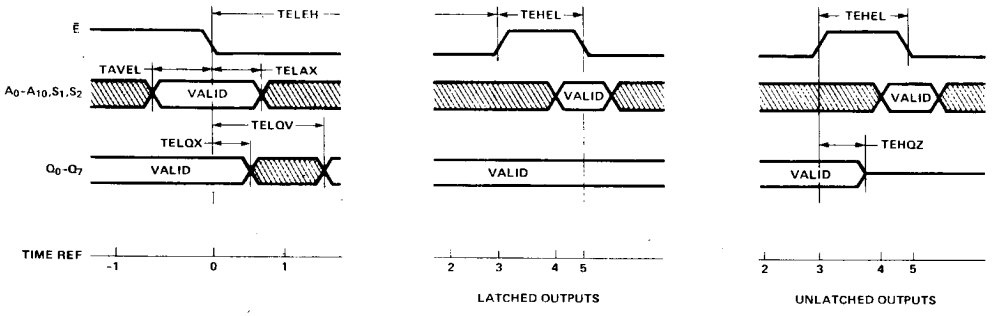
AC CHARACTERISTICS

Test Conditions: V_{CC} = 5V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	6316I			6316M			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Access Time From $\overline{E}$	TELQV			450			600	ns
Output Enable Time	TSVQX			130			150	ns
Chip Deselect Time	TSXQZ			130			150	ns
Output Disable Time	TEHQZ			130			150	ns
$\overline{E}$ Pulse Width (Pos)	TEHEL	140			150			ns
$\overline{E}$ Pulse Width (Neg)	TELEH	450			600			ns
Address Setup Time	TAVEL	10			10			ns
Address Hold Time	TELAX	90			100			ns
Latched Chip Select Enable Time	TELQX			0			0	ns

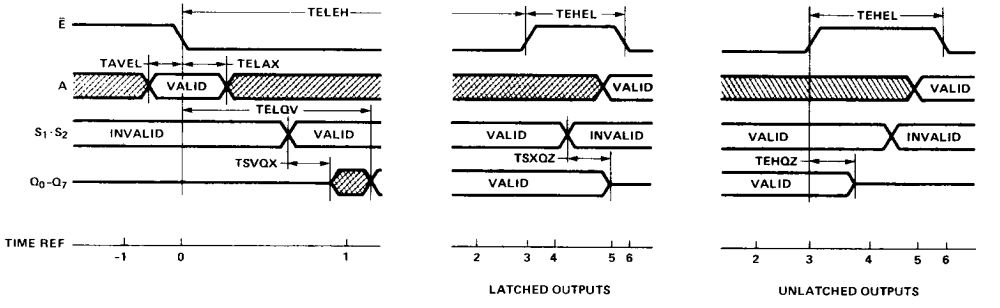
READ CYCLE TIMING • Latched Chip Selects



FUNCTION TABLE • Latched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	E	A	$S_1 \cdot S_2$	LATCHED	UNLATCHED	
−1	H	X	V	V	Z	LATCHED DATA VALID FROM PREVIOUS CYCLE
0	↘	V	V	Z	Z	STROBE LATCHES VALID ADDRESS, CHIP SELECT INFORMATION
1	L	X	X	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	X	V	V	OUTPUTS VALID
3	↗	X	X	V	V	STROBE RETURNS HIGH, LATCHES OUTPUT
4	H	X	X	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	↘	V	V	V	Z	NEXT CYCLE BEGINS, SAME AS 0.

READ CYCLE TIMING • Unlatched Chip Selects



FUNCTION TABLE • Unlatched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	E	A	$S_1 \cdot S_2$	LATCHED	UNLATCHED	
−1	H	X	$\overline{V}$	Z	Z	MEMORY INACTIVE, OUTPUTS HIGH Z
0	↘	V	$\overline{V}$	Z	Z	STROBE LATCHES ADDRESS INFORMATION
1	L	X	V	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	V	V	V	OUTPUTS VALID
3	↗	X	V	V	V	STROBE RETURNS HIGH, LATCHES OUTPUTS
4	H	X	V	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	H	X	$\overline{V}$	Z	Z	OUTPUTS DISABLED ON LATCHED DEVICES
6	↘	V	$\overline{V}$	Z	Z	NEXT CYCLE BEGINS, SAME AS 0.

NOTES:
1. X = Don't Care 2. V = Valid 3. Z = High Impedance 4. $\overline{V}$ = Invalid.

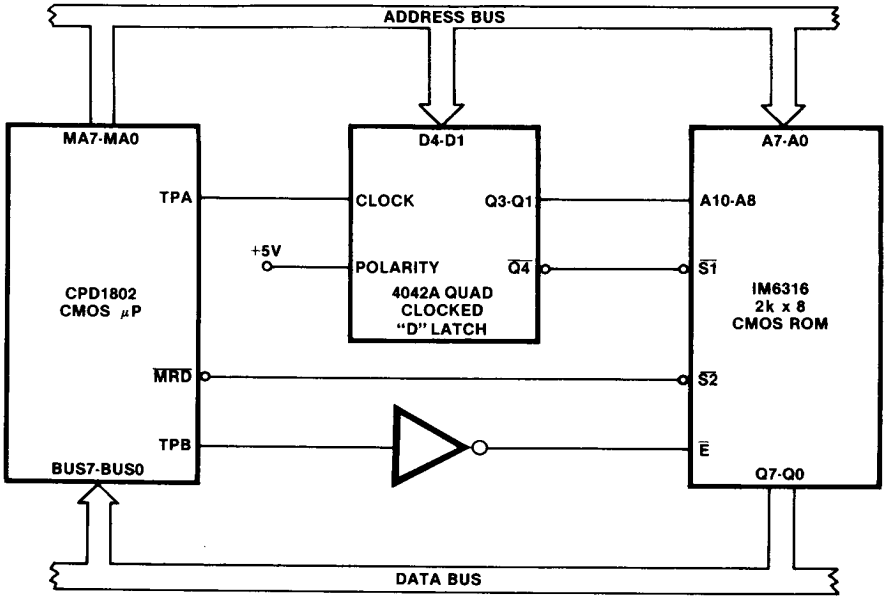


FIG. 1. 2K x 8 CMOS ROM MEMORY FOR CPD1802 CMOS MICROPROCESSOR

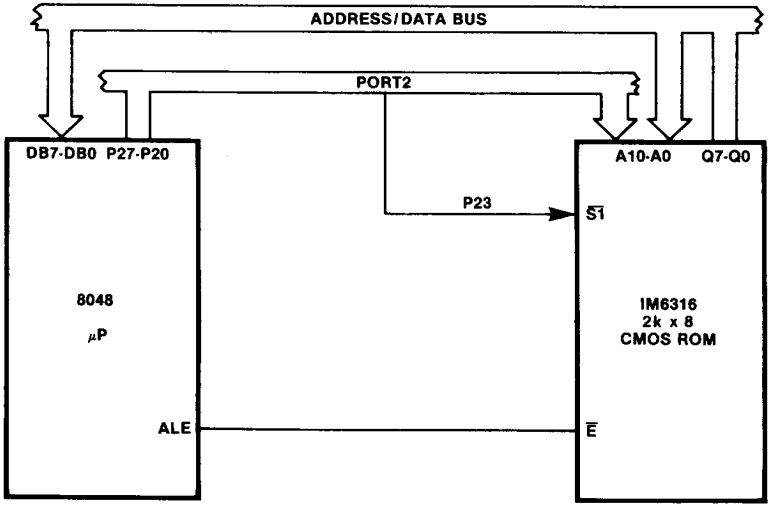


FIG. 2. 2 k x 8 CMOS ROM MEMORY FOR 8048 or 8035 MICROCOMPUTERS

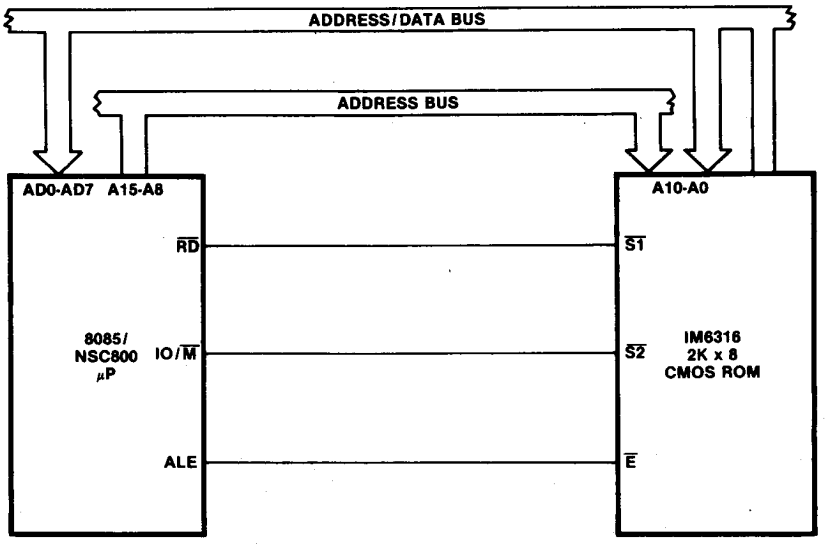


FIG. 3. 2 k x 8 CMOS ROM MEMORY FOR 8085/NSC 800 MICROPROCESSORS

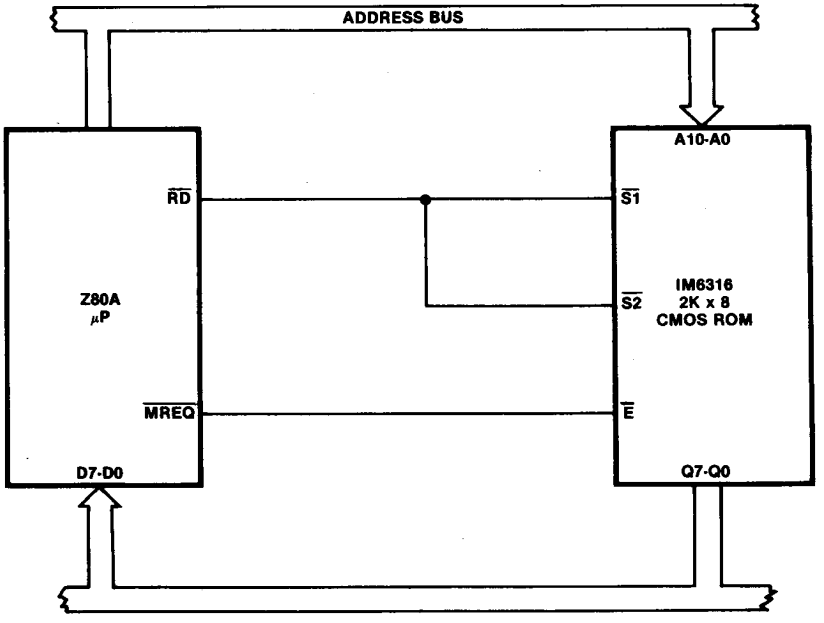


FIG. 4. 2 k x 8 CMOS ROM MEMORY FOR Z80A MICROPROCESSOR DATA BUS