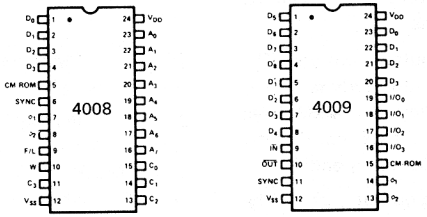
4008/4009
STANDARD MEMORY AND I/O INTERFACE SET

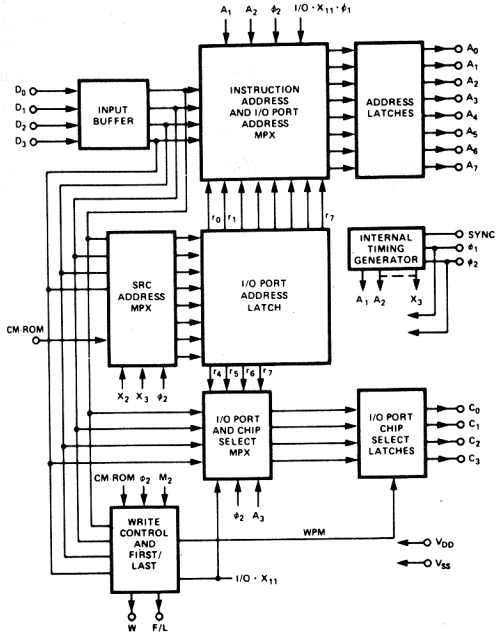
- **Direct Interface to Standard Memories**
- **Allows Write Program Memory**
- **24 Pin Dual In-Line Packages**
- **Standard Operating Temperature Range of 0° to 70 °C**

The standard memory and I/O interface set (4008/4009) provides the complete control functions performed by the 4001 or 4308 in MCS-40™ systems. The 4008/4009 are completely compatible with other members of the MCS-40 family. All activity is still under control of the CPU. One set of 4008/4009 and several TTL decoders is sufficient to interface to 4K words of program memory, sixteen four-bit input ports and sixteen four-bit output ports.

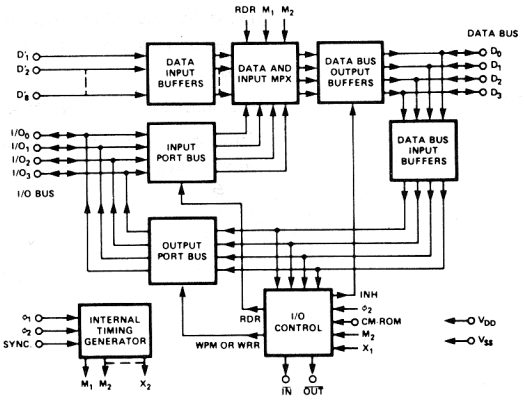
PIN CONFIGURATIONS



4008 BLOCK DIAGRAM



4009 BLOCK DIAGRAM



Pin Description

4008

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
7-8	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
6	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
5	CM-ROM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
23-16	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
15-13, 11	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3, or during an SRC are transferred here.
9	F/L/Neg.	Output signal generated by the 4008 to indicate which half-byte of PROGRAM MEMORY is to be operated on.
10	W/Pos.	Output signal, active low, generated by the 4008 when the processor executes a WPM instruction.
12	V_{SS}	Most positive supply voltage.
24	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.

4009

Pin No.	Designation/ Type of Logic	Description of Function
23-20	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8, 1-4	D'_1-D'_8/Pos.	The eight bits of instruction from the program memory are transferred on these 4009 pins (most significant bit is D'_8).
14-13	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
11	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
15	CM-ROM/Neg.	Command input driven by CM-ROM output of Processor.
9	IN/Neg.	Output signal, active low, generated by the 4289 when the processor executes an RDR instruction.
10	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4009 when the processor executes a WRR instruction.
19-16	I/O_0-I/O_3/Pos.	Bidirectional I/O data bus. Data to and from I/O ports or data to write PROGRAM MEMORY are transferred via these pins.
23	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
12	V_{SS}	Most positive supply voltage.

Functional Description

The 4008 is the address latch chip which interfaces the 4004 or 4040 to standard PROMs, ROMs and RAMs used for program memory. The 4008 latches the low order eight bits of the program address sent out by the CPU during A1 and A2 time. During A3 time it latches the high order four bits of the program address from the CPU. The low-order eight bits of the program address are then presented at pins A0 through A7 and the high-order four bit (also referred to as page number) are presented at pins C0 through C3. These four bits must be decoded externally and one page of program memory is selected.

The 4009 then transfers the eight bit instruction from program memory to the CPU four bits at a time at M1 and M2. The command signal sent by the CPU activates the 4009 and initiates this transfer.

When the CPU executes an SRC (Send Register Control) instruction, the 4008 responds by storing the I/O address in its eight bit SRC register. The content of this SRC register is always transferred to the address lines (A0 through A7) and the chip select lines (C0 through C3) at X1 time. The appropriate I/O port is then selected by decoding the chip select lines. The IN and OUT lines of the 4009 indicate whether an input or output operation will occur.

The 4009 is primarily an instruction and I/O transfer device. When the CPU executes an RDR (Read ROM Port) instruction, the 4009 will send an input strobe (pin 9) to enable the selected input port. It also enables I/O input buffers to transfer the input data from the I/O bus to the data bus. When the 4009 interprets a WRR (Write ROM Port) instruction, it transfers output data from the CPU to the I/O bus and sends an output strobe (pin 10) to enable the selected output port.

The WPM (Write Program Memory) instruction is used in conjunction with the 4008/4009 to write data into the RAM program memory. When an instruction is to be stored in RAM program memory, it is written in two four-bit segments. The F/L signal from the 4008 keeps track of which half is being written. When the CPU executes a WPM instruction, the chip select lines of the 4008 are jammed with "1111". In the system design this should be designated as the RAM channel. The W line on the 4008 is also activated by the WPM instruction. The previously selected SRC address on line A0 through A7 of the 4008 becomes the address of the RAM word being written. By appropriately decoding the chip select lines, the W line, and F/L, the write strobes can be generated for the memory.

The F/L line is initially high (V_{SS}) when power comes on. It then pulses low (V_{DD}) when every second WPM is executed. A high (V_{SS}) on the F/L lines means that the first four bits (OPR) are being written, and a low means that the last four bits (OPA) are being written. The 4009 transfers the segment of the instruction to the I/O bus at X2 of the WPM instruction. The SRC address sent to RAM is only 8 bits. When more than one page of RAM (256 bytes) is being written, an output port must be used to supply additional address lines for higher order addresses.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-55°C to + 125°C
Input Voltages and Supply Voltage with respect to V_{SS}	+0.5V to -20V
Power Dissipation	1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current (4008 only)		10	20	mA	T_A = 25°C
I_{DD}	Average Supply Current (4009 only)		13	30	mA	T_A = 25°C
INPUT CHARACTERISTICS–ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS–ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitance Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}[1]	Address Line Sinking Current (4008 only)	7	13		mA	V_{OUT} = V_{SS}
I_{OL}	In, Out, F/L, Chip Select	1.6	4		mA	V_{OUT} = V_{SS} -4.85
I_{OL}[2]	W Output, Sinking Current (4008 only)	2.5	5		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level (4008 only)		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level (4008 only)		.6	1.2	kΩ	V_{OUT} = V_{SS} -.5V
R_{OH}	Output Resistance, Data Line "0" Level (4009 only)		130	250	Ω	V_{OUT} = V_{SS} -2V
I_{CF}[3]	Address, C/S Output "1" Clamp Current (4008 only)			16	mA	V_{OUT} = V_{SS} -6V
I_{CF}[3]	In, Out "1" Clamp Current (4009 only)			16	mA	V_{OUT} = V_{SS} -6V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}[4]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (4009 only)	V_{DD}		V_{SS}-4.2	V	
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance (4009 only)		.25	1.0	kΩ	V_{OUT} = V_{SS} -.5
I_{OL}	I/O Output "1" Sink Current (4009 only)	5	12		mA	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current (4009 only)	1.6	4		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current (4009 only)			16	mA	V_{OUT} = V_{SS} -6V
CAPACITANCE						
C_{ϕ}	Clock Capacitance		8	15	pF	V_{IN} = V_{SS}
C_{DB}	Data Bus Capacitance		7	10	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance (4008 only)			10	pF	V_{IN} = V_{SS}
C_{IN}	Input Capacitance (4009 only)			15	pF	V_{IN} = V_{SS}
C_{OUT}	Output Capacitance			10	pF	V_{IN} = V_{SS}

Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. A 6.8kΩ resistor must be connected between Pin W and V_{DD} for TTL capability.
3. Resistors in series with TTL inputs may be required to limit current into V_{DD} or V_{SS} from TTL input clamp diodes.
4. TTL V_{OH} = 2.4V will ensure 4009 V_{IH} = V_{SS} -1.5 via the 4009 latch. Refer to Figure 3.

A.C. Characteristics

$T_A = 0°C$ to $70°C$, $V_{SS} - V_{DD} = 15V \pm 5\%$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Times			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay $\phi 1$ to ϕ_2	400		500	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500 pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}	Address to Output Delay at A_1, X_1 (4008)			580	ns	C_L = 250pF
t_{A2}	Address to Output Delay A_2 (4008)			580	ns	C_L = 250pF
t_{CS}	Chip Select Output Delay at A_3 (4008)			300	ns	C_L = 50pF
t_{WD}	W Output Delay (4008)			600	ns	C_L = 100pF
t_{FD}	F/L Output Delay (4008)	0.1		1	μs	C_L = 100pF
t_{WI}	Data In Write Time (4009)	470			ns	C_L = 200pF on data bus
t_D	I/O Output Delay (4009)			1.0	μs	C_L = 300pF
t_{S1}	IN Strobe Delay (4009)			450	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay (4009)			1.0	μs	C_L = 50pF

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

Timing Diagram

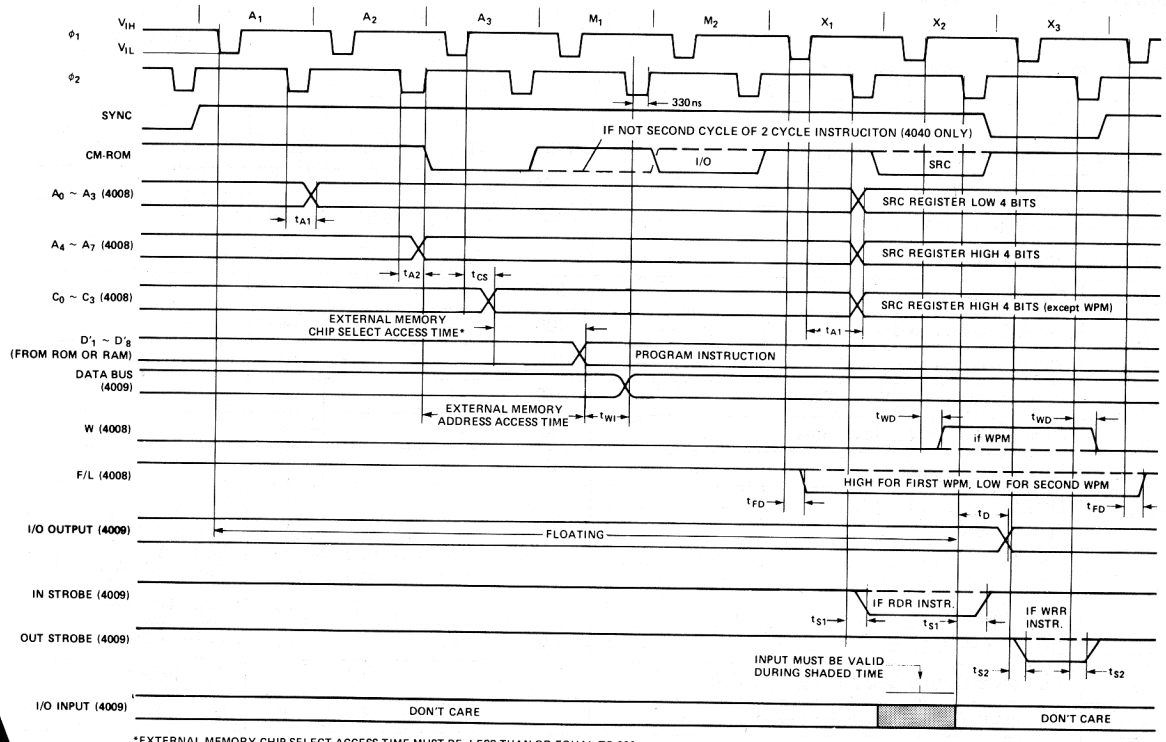


Figure 1. 4008 and 4009 Timing Diagram.

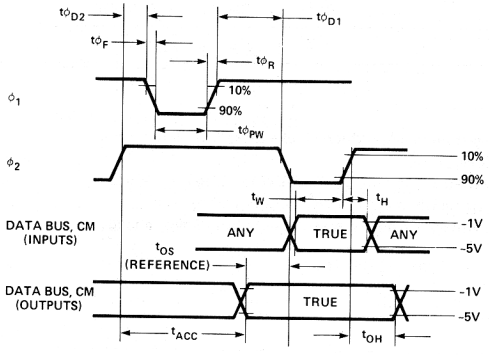
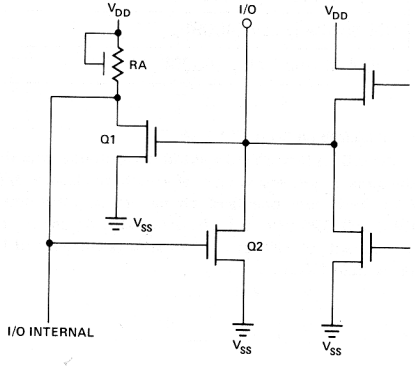


Figure 2. MCS-40 Timing Detail.



EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4009 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO $V_{CC} = V_{SS}$ ON TTL OUTPUTS, AS R_I DOES ON 4001/4308 INPUT PORTS.

Figure 3. 4009 I/O Latch.