PRELIMINARY

2816A
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- 5 Volt Only Operation
- Fast Read Access Time:
  - —2816A-2, 200ns Max
  - —2816A, 250ns Max
  - —2816A-3, 350ns Max
  - —2816A-4, 450ns Max
- Byte Erase/Write with TTL Level $\overline{WE}$ Signal
- 9ms Byte Erase/Write Time
- 9ms Chip Erase Time
- HMOS*-E Flotox Cell Design
- Minimum Endurance of 10,000 Erase/Write Cycles per Byte
- Unlimited Number of Read Cycles
- Conforms to JEDEC Universal Site
- Erase/Write Specifications Guaranteed 0–70°C
- Write Protect Circuit to Preserve Data on Power Up and Power Down

The Intel 2816A is a 16,384-bit electrically erasable programmable read-only memory (E^2PROM). The 2816A can be easily erased and reprogrammed on a byte basis with a TTL-low level signal on $\overline{WE}$. The 2816A operates from a single 5 Volt supply. External programming voltage and write pulse shaping are not required because they are generated by on-chip circuitry.

The Intel 2816A is compatible with the Intel 2816 E^2PROM. Dual voltage detection logic allows the 2816A to use an existing, externally supplied high voltage programming pulse required with the 2816 to write to the Intel 2816A. No hardware changes are required when substituting a 2816A in an existing 2816 socket. System upgrades to 5 volt only operation can be implemented, however, by removing the 21V and write shaping circuitry. The 2816A, like the 2816, has fast read access speeds allowing zero wait state read cycles with high performance microprocessors such as the iAPX286.

The electrical erase/write capability of the 2816A makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write. Any byte can be erased in 9ms without affecting the data in any other byte. Alternatively, the entire memory can be erased in 9ms allowing the total time to rewrite all 2k bytes to be cut by 50%. The 2816A is part of the Intel E^2PROM family that provides a significant increase in flexibility allowing new applications (remote firmware update of program code, dynamic parameter storage) never before possible.

The 2816 E^2PROM possesses Intel's 2-line control architecture to eliminate bus contention in a system environment. A power down mode is also featured; in standby mode, power consumption is reduced by over 50% without increasing access time. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

*HMOS is a patented process of Intel Corporation

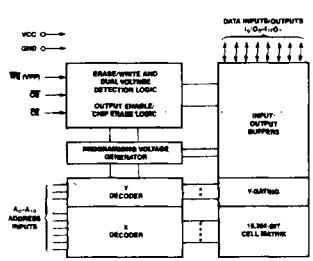

Figure 1. 2816A Functional Block Diagram

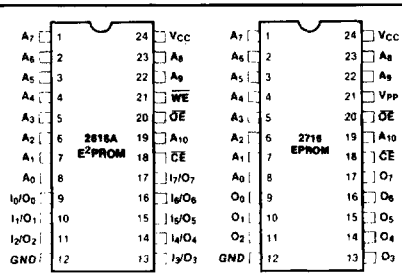

Figure 2. Pin Configuration

PIN NAMES	
A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
$\overline{WE}$ (VPP)	WRITE ENABLE (VPP OPTION)

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DEVICE OPERATION

The 2816A has six modes of operation, listed in Table 1. All operational modes are designed to provide maximum microprocessor compatibility and system consistency.

Table 1. Mode Selection

PIN / MODE	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	INPUTS/ OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	$D_{IN}=V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase	V_{IL}	+10V to +15V	V_{IL}	$D_{IN}=V_{IH}$
No Operation	V_{IL}	V_{IH}	V_{IH}	High Z
E/W Inhibit	V_{IH}	V_{IH}	V_{IL}	High Z

All control inputs are TTL-compatible with the exception of chip erase.

READ MODE

Optimal system efficiency depends to a great extent on a tightly coupled microprocessor/memory interface. The E^2PROM device should respond rapidly with data to allow the highest possible CPU performance. The 2816A satisfies this high performance requirement because of read access times typically less than 250ns. Program execution directly out of electrically erasable memory has never before been possible; the 2816A opens this new, powerful applications segment.

The 2816A uses Intel's proven 2-line control architecture for read operation. The 2-line control function removes bus contention from the system environment and allows low power dissipation (by deselecting unused devices).

Figure 3 shows the timing disadvantages of a single-line control architecture. 2-line control, shown in Figure 4, has been developed by Intel to solve this bus contention and the associated system reliability problems. Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and should be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a time delay of t_{OE}, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Figure 5 shows a typical system interconnection. Here the 2816A contains program information that the 8086 requires for system function. $\overline{CE}$ (pin 18) is decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in system, and connected

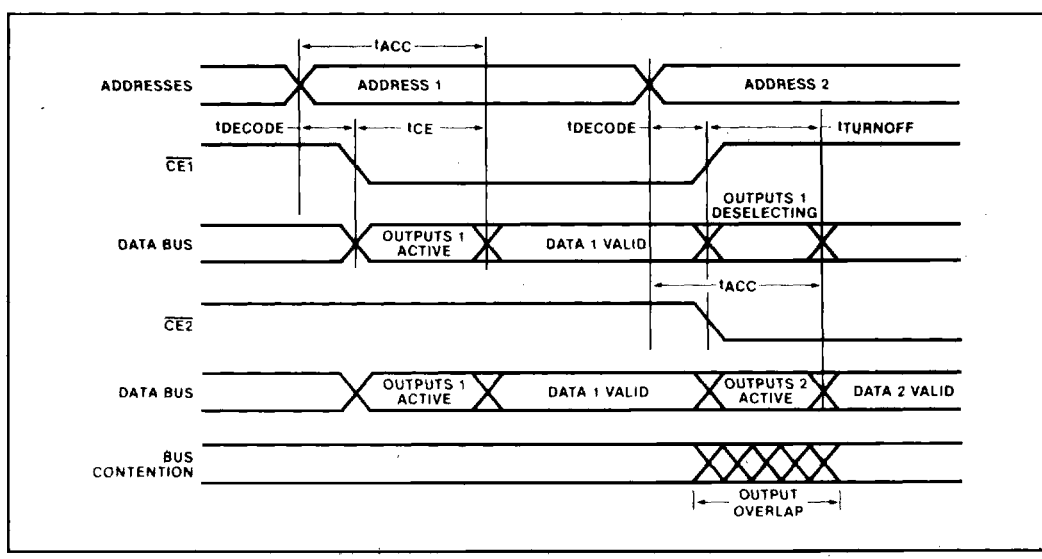


Figure 3. Single-Line Control and Bus Contention

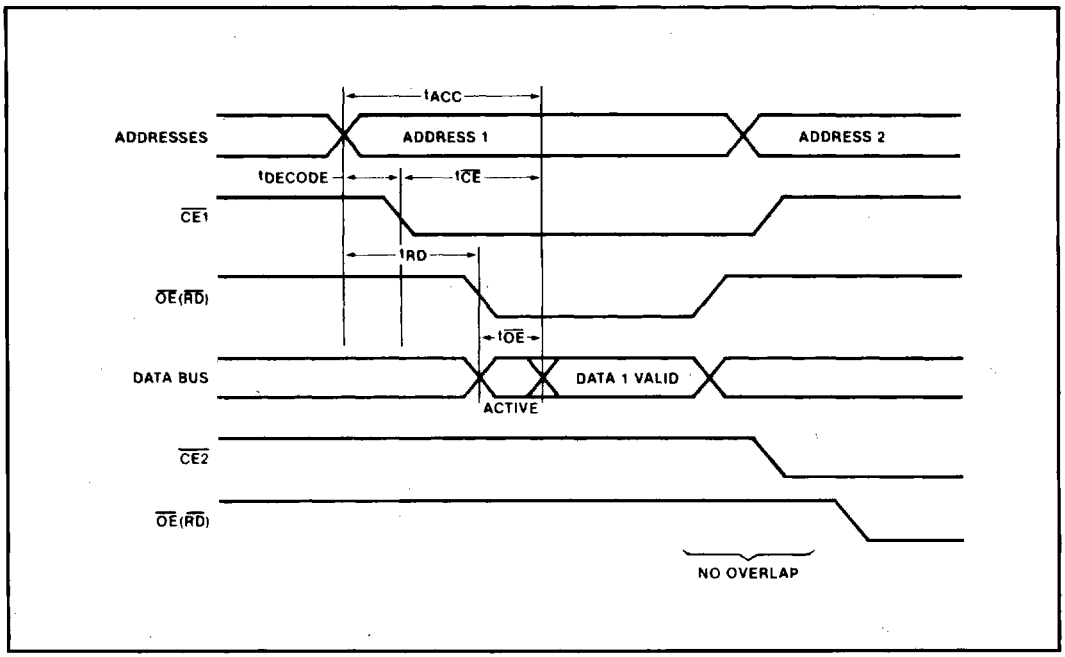


Figure 4. Two-Line Control Architecture

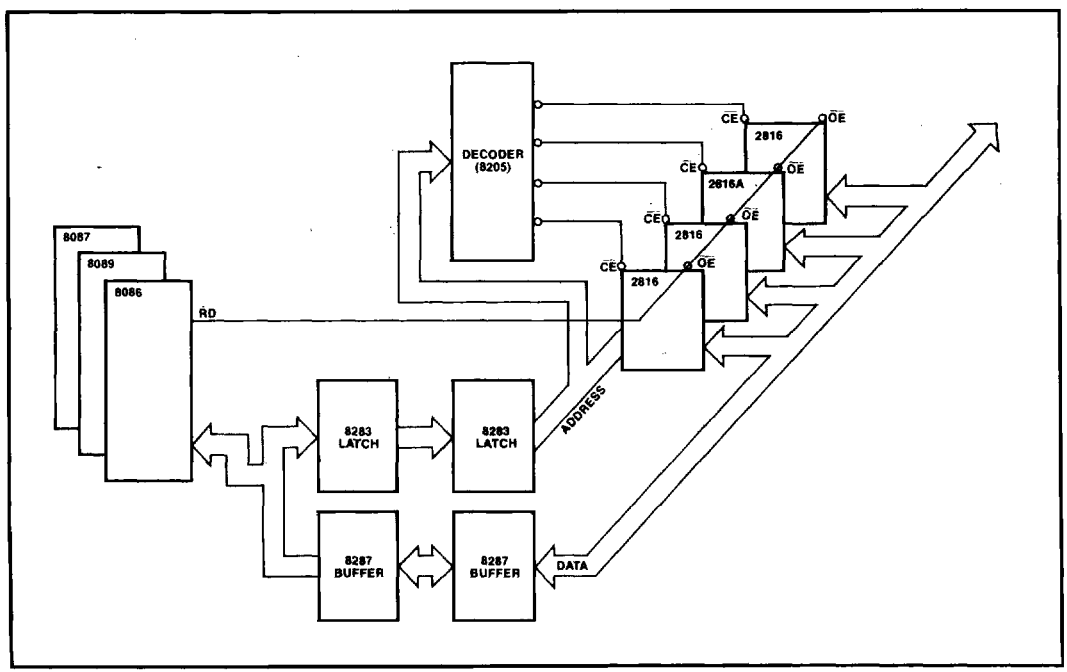


Figure 5. iAPX 86/2816A Read Architecture

to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

WRITE MODE

The 2816A is erased and reprogrammed electrically as opposed to EPROMs which require ultraviolet light for erasure. The device offers dynamic flexibility because both byte (single location) and chip erase are possible.

A close examination of the broad application spectrum for the E^2 device reveals an inherent need for single location erase capability. Program store applications can be classified in several ways. Figure 6 lists various storage modes and the required erase function. In greater than 80% of all cases, a byte erase feature is necessary.

APPLICATION TYPE	IDEAL ERASE MODE
• STRICT PROGRAM STORE	CHIP
• RELOCATABLE PROGRAM STRUCTURE	BYTE
• PROGRAM STORE EXTENSION	BYTE
• PROGRAM EXECUTION CONSTANTS	BYTE
• PROGRAM DEPENDENT DATA STORE	BYTE
• DATA STORE APPLICATIONS	BYTE

Figure 6. Microprocessor Storage Types

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by placing the byte address at the address input pins, applying logic 1 (TTL-high) to all eight data input pins, and lowering $\overline{CE}$, $\overline{WE}$ to V_{IL}. The $\overline{OE}$ pin must be held at V_{IH} during byte erase and write operations. The $\overline{WE}$ pulse width must be a minimum of 9ms, and a maximum of 15ms. Once the location has been erased, the same operation is repeated for a data write. The data input pins in this case reflect the byte that is to be stored. The data to be programmed, address and control signals must be presented to the 2816A throughout the required programming time.

Because the device is designed to be written in system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (0–70°C).

CHIP ERASE MODE

Should one wish to erase the entire 2816A array at once, the device offers a chip erase function. When the chip erase function is performed, all 2K bytes are returned to a logic 1 (FF) state.

The 2816A's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9 volts. When $\overline{OE}$ is greater that 9 volts and $\overline{CE}$ and $\overline{WE}$ are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10ms. The data input pins must be held to a TTL-high level during this time.

STANDBY MODE

The 2816A has a standby mode which reduces active power dissipation by 50% from 100ma to 50ma. The 2816A is placed in standby mode by applying a TTL-high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ and $\overline{WE}$ input.

The standby mode for the 2816A is a superset of the standby mode for the 2816. The standby mode for the 2816A includes the E/W Inhibit mode of the 2816.

NO OPERATION MODE

This mode is frequently entered while in a read or write cycle. In the READ cycle, $\overline{CE}$ may go low before $\overline{OE}$ goes low because t_{CE} ($\overline{CE}$ to Output Delay) is longer than t_{OE} ($\overline{OE}$ to Output Delay). While $\overline{CE}$ is low with $\overline{OE}$ and $\overline{WE}$ at TTL-high, no READ, ERASE, or WRITE operation will occur. The read operation would begin in the READ cycle when $\overline{OE}$ input also falls to TTL-low.

The No Operation mode differs from Standby Mode in that active power is drawn by the 2816A in this mode.

WRITE TIME CHARACTERISTICS

The 2816A write time specification is 9ms (min.) and 15ms (max.). If the write pulse width applied to the $\overline{WE}$ input is 9ms, the programmed byte is guaranteed to be correctly and reliably programmed to any location in the 2816A.

The maximum pulse width to the $\overline{WE}$ input of 15ms limits the duration of the pulse width. Exceeding this specification may overstress the E^2PROM cells and affect long term device reliability. Any write pulse width between 9ms and 15ms will also guarantee byte programming and chip erase over the full temperature range.

Programmed data will be retained by the Intel 2816A for over 10 years.

Although the number of read cycles is unlimited, a characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The 2816A has been designed and manufactured to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

On-Chip Write Protection on V_{CC} Power Up and Power Down

An erase/write of a byte in the 2816A is accomplished with input signals $\overline{CE}$, $\overline{WE} = V_{IL}$. During system (Vcc) power up and power down, this condition may be present as Vcc ramps up to or down from its steady state value of 5 volts. To prevent the possibility of an inadvertent byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if Vcc falls below 4 volts (V_{LKO}).

VPP OPTION

Although the Intel® 2816A requires only 5 volts for programming, it was designed to be totally upward compatible with the Intel 2816. No hardware changes are required when substituting a 2816A into a 2816 socket. Shaping of the Vpp programming pulse is also not required with the 2816A. Table 2 lists the Vpp Option Modes.

Table 2. VPP Option Modes

PIN / MODE	$\overline{CE}$ (18)	$\overline{OE}$ (20)	VPP (21)	INPUTS/ OUTPUTS
Byte Erase	V_{IL}	V_{IH}	20–22V	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	20–22V	D_{IN}
Chip Erase	V_{IL}	+10V to +15V	20–22V	$D_{IN} = V_{IH}$

APPLICATIONS

The 2816A E^2PROM is a new and powerful addition to the Intel non-volatile family. Like other Intel E^2PROMs, it offers a high degree of flexibility through in-circuit alterability while retaining the non-volatile characteristics of ROM.

Because of these device parameters, the device is ideal in many applications. Some of the potential uses are listed below:

1. Calibration constants storage (continuous calibration)
2. Software alterable central stores (dynamic reconfiguration)
3. Remote communication programming
4. PC and NC Industrial Applications
5. CRT Terminal configuration and custom graphic and font sets
6. Military replacement for core memory and fuse-link PROMs
7. Point of sale terminals
8. Remote alterable look-up tables
9. Printer communications, controllers
10. Remote data or error logging
11. Replacing CMOS RAM and battery backup
12. Remote firmware update of program code

AVAILABLE LITERATURE

To give the system designer an opportunity to more thoroughly understand the device attributes and uses, a library of E^2PROM information is available in the Memory Component Handbook. Some of the E^2PROM application information included is listed below.

AR 119 — 16-K EE-PROM Relies On Tunneling for Byte-Erasable Program Storage

AP 100 — Reliability Aspects of a Floating Gate E^2PROM

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +100°C
All Input or Output Voltages with
Respect to Ground..... +6V to −0.3V
Maximum Duration of Erase/Write Cycle ... 20ms
V_{OE} with Respect to Ground..... +17V to −0.1V

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. OPERATING CONDITIONS DURING READ AND WRITE

Temperature Range	0°C-70°C
V_{CC} Power Supply	5V ± 5%

D.C. CHARACTERISTICS

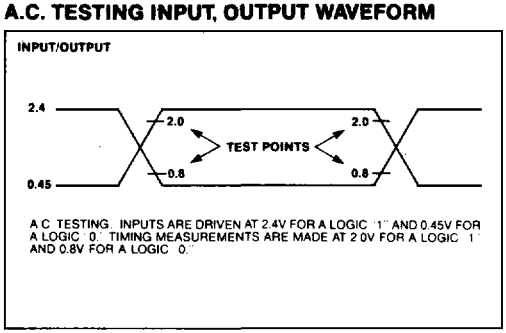
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Leakage Current			10	μA	$V_{IN}=5.25V$[2]
I_{LO}	Output Leakage Current			10	μA	$V_{OUT}=5.25V$
I_{CCA}	V_{CC} Current (Active)		50	100	mA	$OE=CE=V_{IL}$
I_{CCS}	V_{CC} Current (Standby)		25	50	mA	$CE=V_{IH}$
I_{CCW}	V_{CC} Current (Byte Erase/Write)			130	mA	$WE=CE=V_{IL}$
$V_{IL(D.C.)}$	Input Low Voltage (D.C.)	−0.1		0.8	V	
$V_{IL(A.C.)}$	Input Low Voltage (A.C.)	−0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL}=2.1mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH}=-400\mu A$
V_{OE}	$\overline{OE}$ Voltage for Chip Erase	10		15	V	$I_{OE}=10\mu A$
V_{LKO}	V_{CC} Lockout Level for Data Protection	4.0		4.4	V	

A.C. TEST CONDITIONS

Output Load ..... 1TTL gate and C_L = 100pF
Input Rise and Fall Times (10% to 90%) 20ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level..... 0.8V and 2.0V
Output Timing Reference Level .... 0.8V and 2.0V

Notes:
1. This parameter is only sampled and not 100% tested.
2. $I_{LI(Max)}$ is less than 10μa when V_{IN} is less than 5.25V.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

CAPACITANCE[1] $T_A = 25°C$, $f = 1$ MHz

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	5	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance		10	pF	$V_{OUT} = 0V$
C_{VCC}	V_{CC} Capacitance		500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
$C_{WE\ (VPP)}$	WE Input Capacitance		50	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. CHARACTERISTICS

READ

Symbol	Parameter	2816A-2 Limits			2816A Limits			2816A-3 Limits			2816A-4 Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
t_{ACC}	Address to Output Delay		150	200		200	250		300	350		400	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		150	200		200	250		300	350		400	450	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay	10		75	10		100	10		120	10		150	ns	$\overline{CE} = V_{IL}$
t_{DF}[2]	$\overline{OE}$ High to Output Float	0		60	0		60	0		100	0		130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

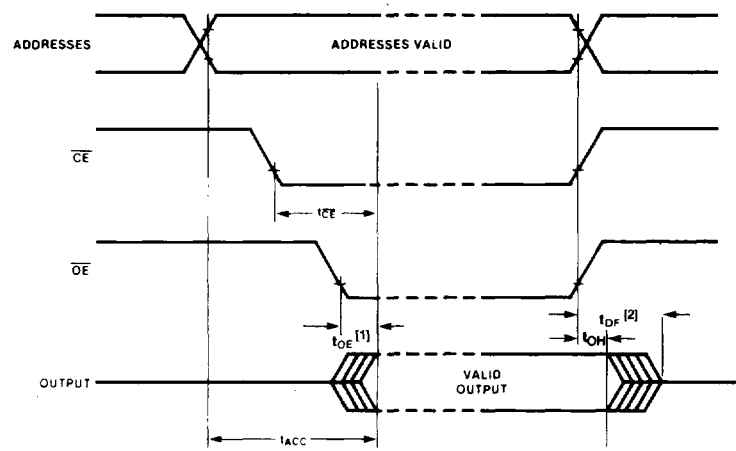
WRITE

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
t_{AS}	Address to Write Set-Up Time	150			ns	
t_{CS}	$\overline{CE}$ to Write Set-Up Time	150			ns	
t_{DS}[3]	Data to Write Set-Up Time	0			ns	
t_{DH}[3]	Data Hold Time	100			ns	
t_{WP}[4]	Write Pulse Width for 2816A	9		15	ms	
t_{WR}	Write Recovery Time	100			ns	
t_{OS}	Chip Erase Set-Up Time	0			ns	V_{OE} = 10V
t_{OH}	Chip Erase Hold Time	0			ns	V_{OE} = 10V
t_{BOS}	Byte Erase/Write Set-Up Time	0			ns	
t_{BOH}	Byte Erase/Write Hold Time	0			ns	
t_{WWR}[5]	Cycle Delay Time Following Write Cycle	40			μs	

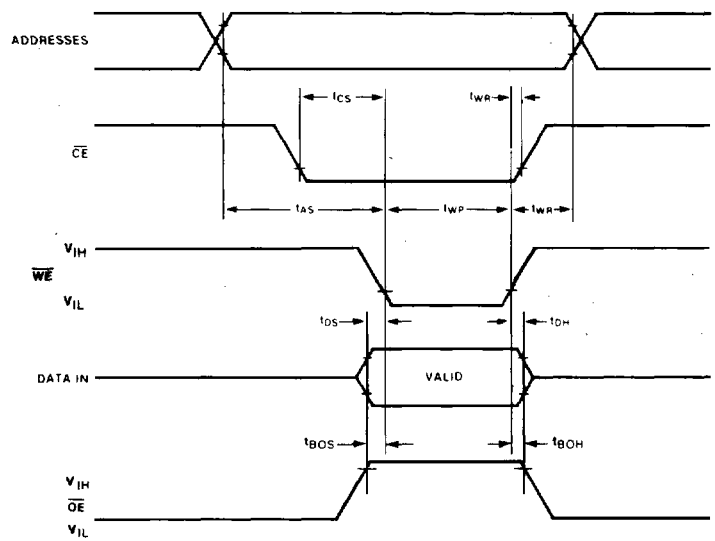
NOTES:
1. This parameter is only sampled and not 100% tested.
2. t_{DF} is measured from the point when $\overline{CE}$ or $\overline{OE}$ returns high (whichever occurs first) to the time when the outputs are no longer driven. This parameter is not 100% tested.
3. The data is set up and hold times for chip erase are identical to those specified for byte erase.
4. Adherence to t_{WP} specification is important to device reliability.
5. Adherence to t_{WWR} is important for device reliability.

WAVEFORMS

READ



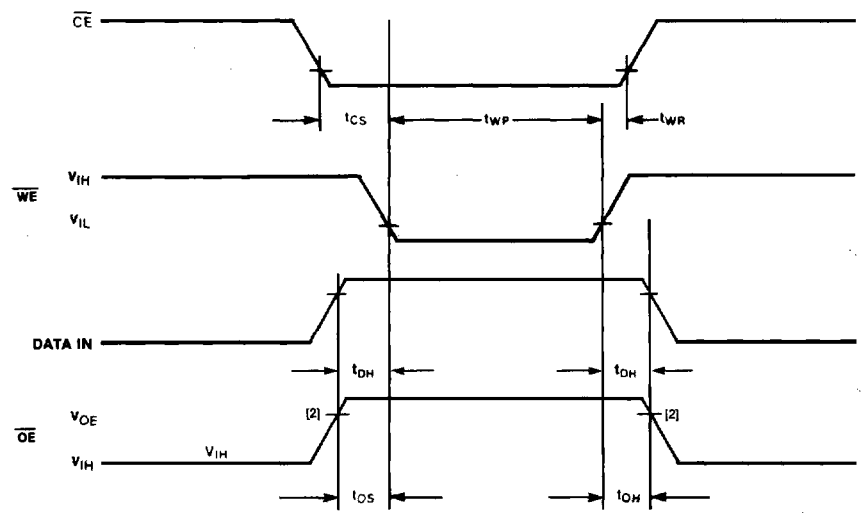
BYTE ERASE OR WRITE[3]



NOTES:
1. $\overline{OE}$ may be delayed up to 150 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for 2816A.
2. t_{DF} is measured from the point when $\overline{CE}$ or $\overline{OE}$ returns high (whichever occurs first) to the time when the outputs are no longer driven. This parameter is not 100% tested.
3. Prior to a data write, an erase operation must be performed. For a byte erase, data in = V_{IH}.

WAVEFORMS (Continued)

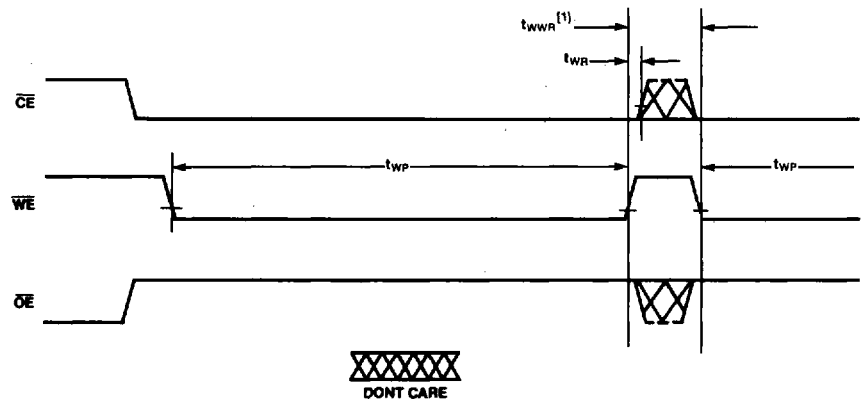
CHIP ERASE[1]



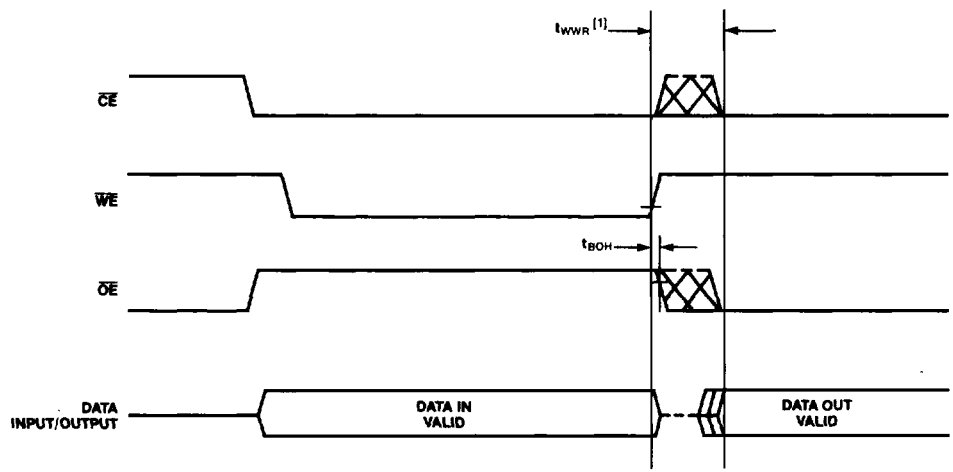
NOTES:
1. In the chip erase mode $D_{IN} = V_{IH}$.
2. Timing reference for $\overline{OE}$ during Chip Erase is 90% of V_{OE}.

WAVEFORMS (Continued)

CONSECUTIVE BYTE ERASE OR WRITE CYCLES



BYTE WRITE FOLLOWED BY READ CYCLE



NOTE:
1. Adherence to t_{WWR} is important for device reliability.

VPP OPTION SPECIFICATIONS[1]

ABSOLUTE MAXIMUM RATINGS

Vpp Supply Voltage with Respect to Ground
During Write/Erase ..... +22.5V to −0.1V
Maximum Duration of Vpp Supply at 22V
During Erase/Write Inhibit ..... 24 Hrs.
Maximum Duration of Vpp Supply at 22V
During Write/Erase ..... 20 ms

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[2]	Max.		
$I_{PP(R)}$	V_{PP} Current (Read)			10	μa	$\overline{CE} = V_{IL}$, $V_{PP} = 4$ to 6
V_{PP}	Read Voltage	4		6	V	
$I_{PP(W)}$	V_{PP} Current (Byte Erase/Write)			10	μa	$\overline{CE} = V_{IL}$
V_{PP}	Write/Erase Voltage	20	21	22	V	
$I_{PP(C)}$	V_{PP} Current (Chip Erase)			10	μa	

CAPACITANCE[2] $T_A = 25°C$, f = 1 MHz

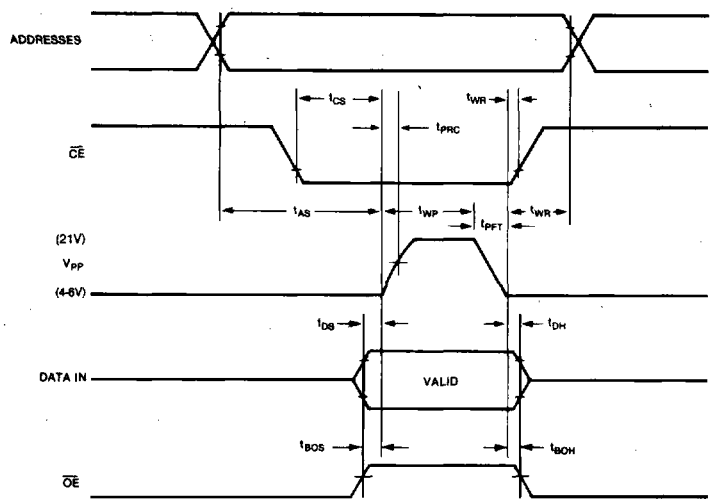
Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{VPP}	V_{PP} Capacitance		50	pf	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. CHARACTERISTICS

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[2]	Max.		
t_{PRC}	V_{PP} RC Time Constant			750	μs	
t_{PFT}	V_{PP} Fall Time			100	μs	

NOTES:
1. Only specifications unique to V_{PP} option operation are shown. All other specifications under 5 volt only operation apply to V_{PP} option operation as well, except where noted.
2. This parameter is only sampled and not 100% tested.

BYTE ERASE OR WRITE WITH VPP OPTION[1,2]



NOTES:

1. Only specifications unique to V_{PP} option operation are shown. All other specifications under 5 volt only operation apply to V_{PP} option operation as well, except where noted.
2. Prior to a data write, an erase operation must be performed. For a byte erase, data in = V_{IH}.