

M8212 8-BIT INPUT/OUTPUT PORT

Military

- Not Recommended for New Designs
- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current 0.25 mA Max
- 3-State Outputs
- Military Temperature Range:
-55°C to +125°C (Tc)
- 3.4V Output High Voltage for Direct Interface to M8080A CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- ±10% Power Supply Tolerance
- 24-Pin Dual-In-Line Package

The Intel M8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

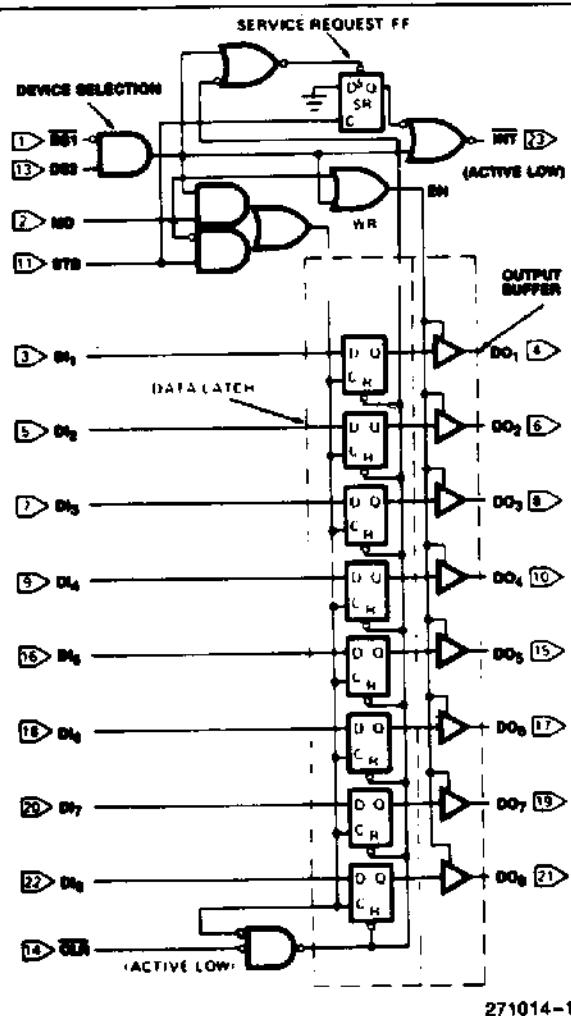
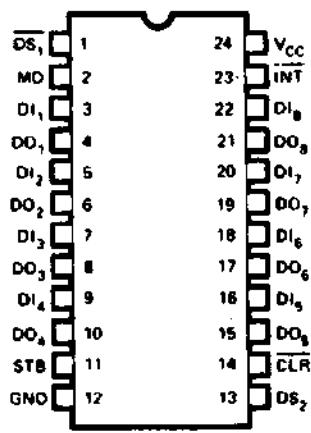


Figure 1. Logic Diagram



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DI ₁ -DI ₈	Data In
DO ₁ -DO ₈	Data Out
DS ₁ -DS ₂	Device Select
MD	Mode
STB	Strobe
INT	Interrupt (Active Low)
CLR	Clear (Active Low)

Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias ⁽¹⁾	-55°C to +125°C
Storage Temperature	-65°C to +160°C
All Output or Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100 mA

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_C^{(1)} = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_F	Input Load Current STB, DS ₂ , CR, DI ₁ -DI ₈ Inputs			-0.25	mA	$V_F = 0.45\text{V}$
I_F	Input Load Current MD Input			-0.75	mA	$V_F = 0.45\text{V}$
I_F	Input Load Current DS, Input			-1.0	mA	$V_F = 0.45\text{V}$
I_R	Input Leakage Current STB, DS, CR, DI ₁ -DI ₈ Inputs			10	μA	$V_R = V_{CC}$
I_R	Input Leakage Current MD Input			30	μA	$V_R = V_{CC}$
I_R	Input Leakage Current DS, Input			40	μA	$V_R = V_{CC}$
V_C	Input Forward Voltage Clamp			-1.2	V	$I_C = -5\text{ mA}$
V_{IL}	Input "Low" Voltage			0.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 10\text{ mA}$
V_{OH}	Output "High" Voltage	3.5	4.0		V	$I_{OH} = -0.5\text{ mA}$
I_{OS}	Short Circuit Output Current	-15		-75	mA	$V_{CC} = 5.0\text{V}$
I_{OL}	Output Leakage Current High Impedance State			20	μA	$V_O = 0.45$ to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

CAPACITANCE $F = 1\text{ MHz}$, $V_{BIAS} = 2.5\text{V}$, $V_{CC} = +5\text{V}$, $T_C^{(1)} = 25^\circ\text{C}$

Symbol	Test	Limits	
		Typ	Max
C_{IN}	DS MD Input Capacitance	9 pF	15 pF
C_{IN}	DS, CLR, STB, DI ₁ -DI ₈ Input Capacitance	5 pF	10 pF
C_{OUT}	DO ₁ -DO ₈ Output Capacitance	8 pF	15 pF

NOTE:

- Case temperatures are "instant on".

CONDITIONS OF TEST

Input Pulse Amplitude = 2.5V

Input Rise and Fall Times: 5 ns between 1V and 2V

Measurements made at 1.5V

A.C. CHARACTERISTICS $T_C^{(1)} = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$

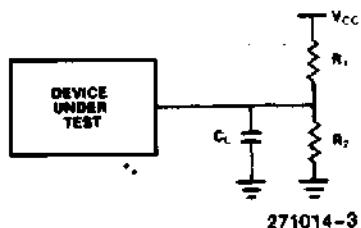
Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	(Note 2)
t_{WE}	Write Enable To Output Delay		50	ns	(Note 2)
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	(Note 2)
t_S	Set To Output Delay		35	ns	(Note 2)
t_E	Output Enable/Disable Time		50	ns	(Note 2) $C_L = 30 \text{ pF}$
t_C	Clear To Output Delay		55	ns	(Note 2)

NOTE:

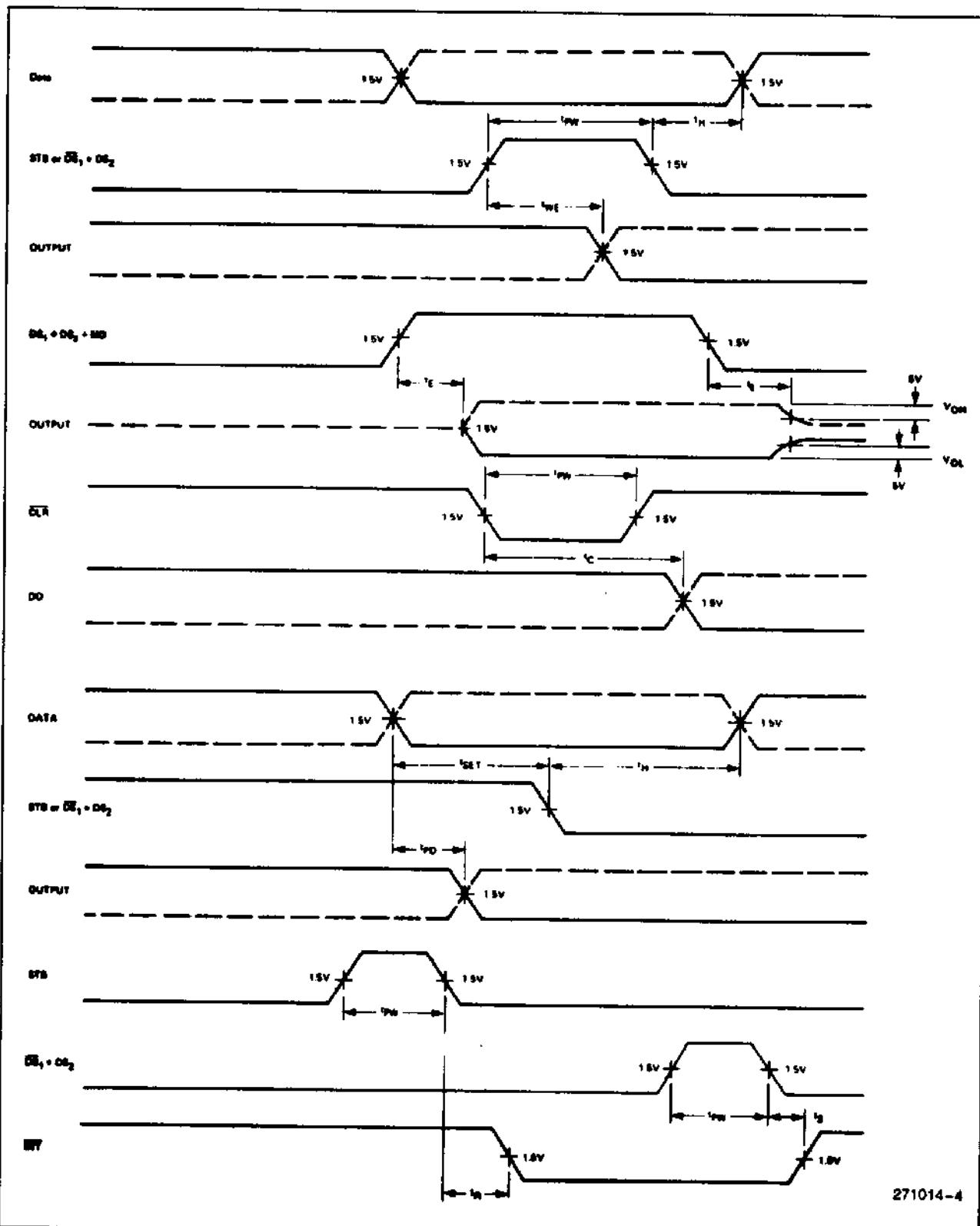
1. Case temperatures are "instant on".

NOTE 2:

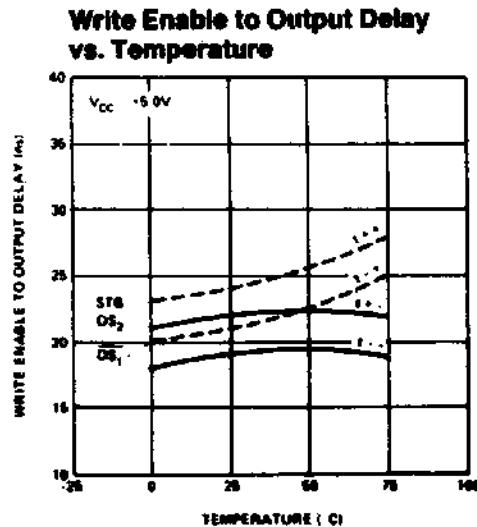
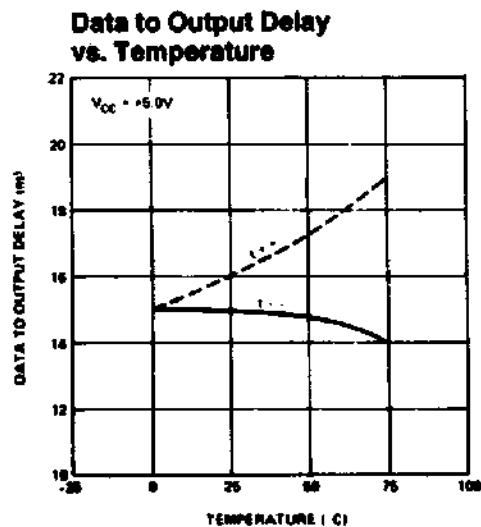
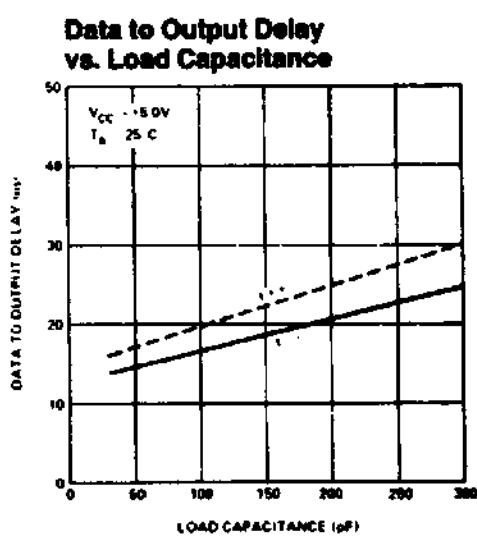
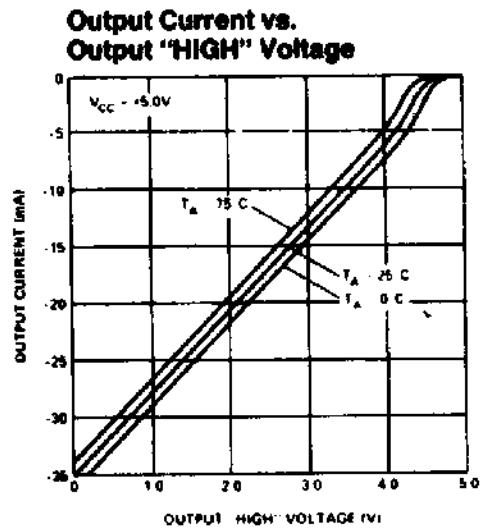
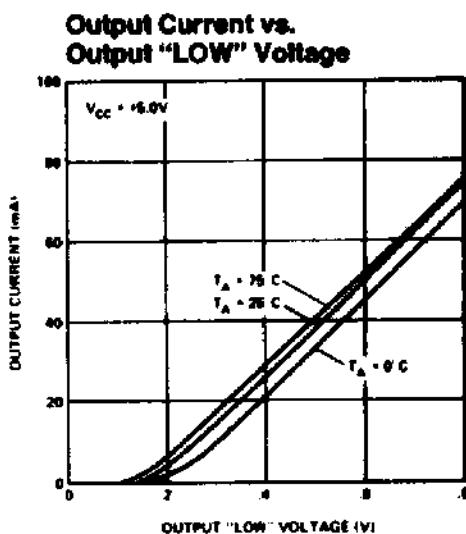
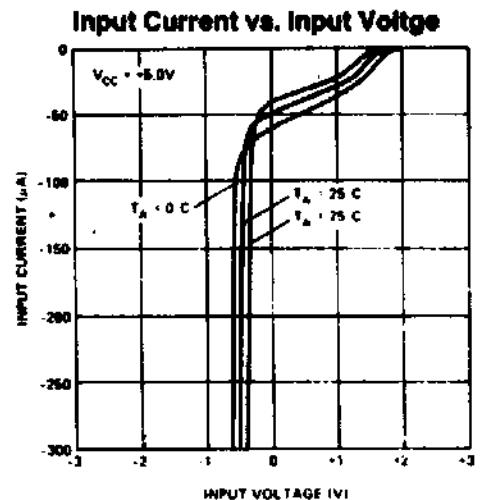
Test	C_L	R_1	R_2
$t_{PD}, t_{WE}, t_R, t_S, t_C$	30 pF	300Ω	600Ω
$t_E, \text{ENABLE } \uparrow$	30 pF	10 KΩ	1 KΩ
$t_E, \text{ENABLE } \downarrow$	30 pF	300Ω	600Ω
$t_E, \text{DISABLE } \uparrow$	5 pF	300Ω	600Ω
$t_E, \text{DISABLE } \downarrow$	5 pF	10 KΩ	1 KΩ

A.C. TESTING LOAD CIRCUIT

WAVEFORMS



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TYPICAL CHARACTERISTICS

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