HN48016P

2048-word × 8-bit Electrically Erasable and Programmable ROM

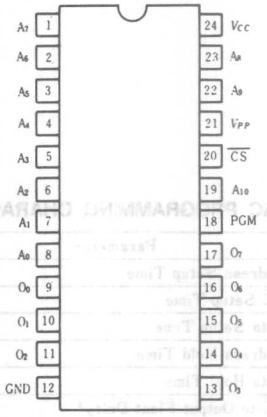
This device operates from a single power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 42 seconds.

(DP-24)

■ FEATURES

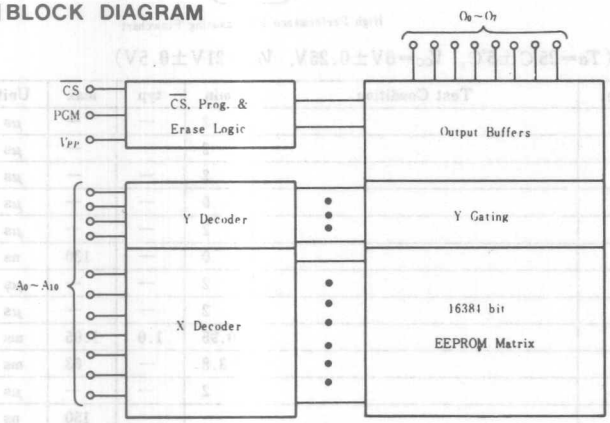
- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program voltage: +25V D.C.
  Program with one 20ms pulse.
- Electrically Erasing ..... Erase Voltage: +25V D.C.
  Erase all words with one 200ms pulse.
- Fully Static ..... No clocks required.
- Inputs and Outputs TTL compative during read, program and erase mode.
- Fully Decoded ..... On-Chip Address Decode.
- Access Time ..... 350ns Max.
- Low Power Dissipation .... 300mW Max.
- Three State Output ..... OR-Tie Capability
- Pin-out Compatible with Intel 2716.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (8~11, 13~17)
Read	V_{IL}	V_{IL}	+5	+5	Dout
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
Program Verify	V_{IL}	V_{IL}	+25	+5	Dout
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z
Erase	Pulsed V_{IL} to V_{IH}	V_{IL}	+25	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
All Input and Output Voltage	V_{IN}, V_{out}	−0.3 to V_{CC} +0.3 or V_{PP} +0.3	V
V_{CC} Voltage	V_{CC}	−0.3 to +7.0	V
V_{PP} Voltage	V_{PP}	−0.3 to +28	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V,* Ta = 0 to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	—	—	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	—	—	10	μA
V_{CC} Current	I_{CC1}	$\overline{CS}$ = V_{IH} / V_{IL}	—	32	50	mA
V_{PP} Current	I_{PP1}	V_{PP} = 5.85V	—	4	7	mA
Input Voltage	V_{IL}		−0.1	—	0.8	V
	V_{IH}		2.0	—	—	V
Output Voltage	V_{OL}	I_{OL} = 1.6mA	—	—	0.4	V
	V_{OH}	I_{OH} = −100 μA	2.4	—	—	V

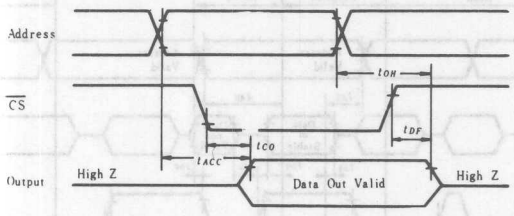
* The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.

● AC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V, Ta = 0 to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address to Output Delay	t_{ACC}	PGM = $\overline{CS}$ = V_{IL}	—	200	350	ns
Chip Select to Output Delay	t_{CO}	PGM = V_{IL}	—	70	150	ns
Chip Deselect to Output Float	t_{DF}		0	40	100	ns
Address to Output Hold	t_{OH}	PGM = $\overline{CS}$ = V_{IL}	10	—	—	ns

● TEST CONDITION

Input pulse levels: 0.8V to 2.0V
Input rise and fall time: ≦ 20ns
Output load: 1TTL Gate + 100 pF
Reference level for Measuring Timing: Inputs 1V and 1.8V
Outputs 0.8V and 2.0V



● CAPACITANCE (Ta = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	7.5	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	15	pF

■ PROGRAM OPERATION

● DC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=0 to +70℃)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
V_{CC} Supply Current	I_{CC2}		—	32	50	mA
V_{PP} Supply Current	I_{PP2}		—	10	20	mA
Input Voltage	V_{IL}		−0.1	—	0.8	V
	V_{IH}		2.0	—	—	V

● AC PROGRAMMING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta=0 to +70℃)

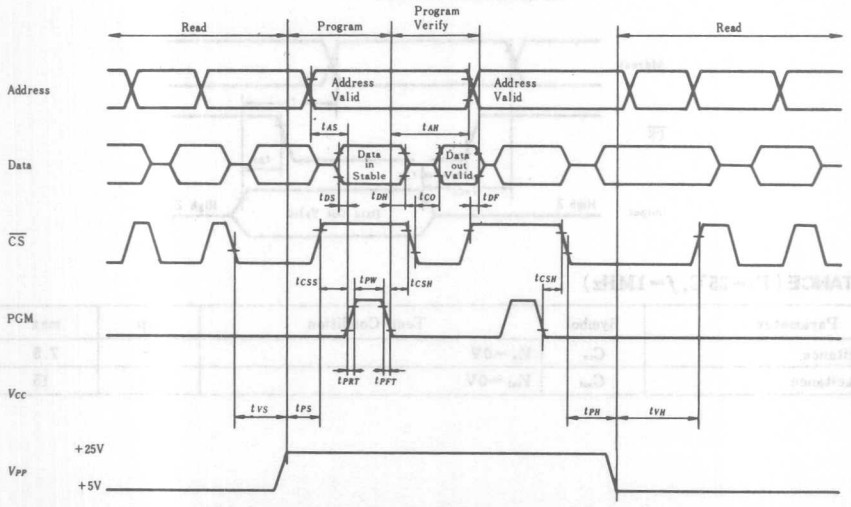
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{CS}$ Setup Time	t_{CSS}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		2*	—	—	μs
$\overline{CS}$ Hold Time	t_{CSH}		7	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
Chip Deselect to Output Float Delay	t_{DF}		0	40	100	ns
Chip Select to Output Delay	t_{CO}		—	70	150	ns
Program Pulse Width	t_{PW}		15	20	25	ms
Program Pulse Rise Time	t_{PRT}		5	—	—	ns
Program Pulse Fall Time	t_{PFT}		5	—	—	ns
V_{PP} Setup Time	t_{PS}		10	—	—	μs
V_{PP} Hold Time	t_{PH}		10	—	—	μs
$\overline{CS}$ to Program Mode Time	t_{VS}		10	—	—	μs
V_{PP} Read Mode Time	t_{VH}		10	—	—	μs

* If the mode changes from program mode to program verify mode sequentially (in the same address), t_{AH} must be larger than $t_{CSH} + t_{CO}$.

● TEST CONDITION

Test Condition

Input pulse levels:	0.8V to 2.0V
Input rise and fall time:	20ns (10% to 90%)
Reference level for Measuring Timing:	Input; 1V and 1.8V
	Output: 0.8V and 2.0V



■ ERASE OPERATION

● DC ERASING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN}=5.25V	—	—	10	μA
V_{CC} Supply Current	I_{CC3}		—	32	50	mA
V_{PP} Supply Current	I_{PP3}		—	10	20	mA
Input Voltage	V_{IL}		−0.1	—	0.8	V
	V_{IH}		2.0	—	—	V

● AC ERASING CHARACTERISTICS (V_{CC}=5V±5%, V_{PP}=25V±1V, Ta= 0 to +70℃)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
$\overline{CS}$ Setup Time	t_{ECSS}		2	—	—	μs
PGM to Output Delay	t_{EO}		7	—	—	μs
Erase Pulse Width	t_{EPW}		190	200	210	ms
Erase Pulse Rise Time	t_{ERT}		5	—	—	ns
Erase Pulse Fall Time	t_{EFT}		5	—	—	ns
V_{PP} Setup Time	t_{ES}		10	—	—	μs
V_{PP} Hold Time	t_{EH}		10	—	—	μs
Erase Program Time t_{EP}	t_{EP}		10	—	—	μs
Program Enase Time t_{PE}	t_{PE}		10	—	—	μs

● TEST CONDITION

Test Condition

Input pulse levels:	0.8V to 2.0V
Input rise and fall time:	20ns (10% to 90%)
Reference level for Measuring Timing:	Input; 1V and 1.8V Output; 0.8V and 2.0V

■ POWER SUPPLY SEQUENCE PRECAUTIONS

To protect the written data, power supply to the HN48016P should be turned on and off in the following order:

- **Power On-Off Order and Input Level Limitation for $\overline{CS}$ and PGM Terminals**

Table 1 shows the relationship between the order in which power supply for the HN48016P should be turned on and off and the input levels of the $\overline{CS}$ and PGM terminals.

(1) For the 5V V_{PP} and V_{CC}, there is no limitation as to the order in which power is turned on and off the state of the input terminals $\overline{CS}$ and PGM.

(2) When turning on and off power supply for the 25V V_{PP}, keep V_{CC} at between 4.5V and 7V, and PGM at "Low."

(3) When turning on and off power supply for the 5V V_{CC} while V_{PP} equals 25V ± 1V (this being a rare case for the HN48016P), make sure to keep PGM at "Low."

Fig. 1 shows the timing order in which power is turned on and off.

● Table 1. Power On-Off Order for HN48016P

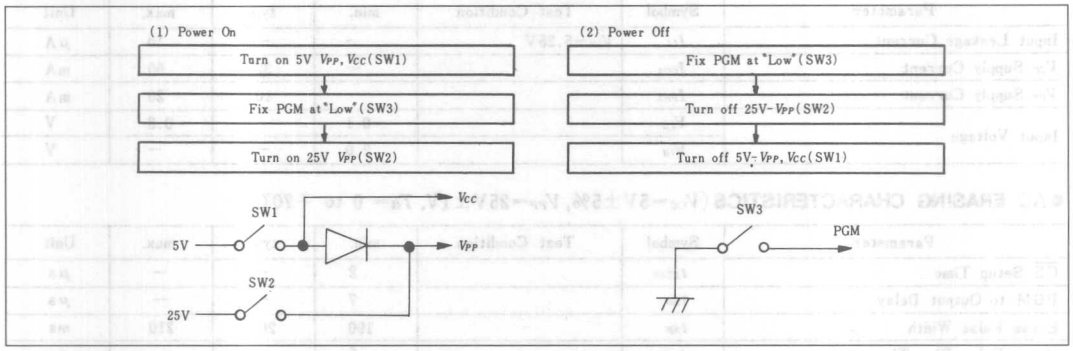
Input Level		Power On-Off	
PGM	$\overline{CS}$	5V-V_{PP}-V_{CC}	25V-V_{PP}
V_{IL}	V_{IL}	Possible	Possible only when V_{CC}=4.5~7V*2
V_{IL}	V_{IH}		
V_{IH}	V_{IL}	Possible	impossible*2
V_{IH}	V_{IH}		

Note 1. If Power for the 25V Vpp were turned on or off while V_{CC} = −0.3V to +4.5V, the data holding characteristic would probably deteriorate.

Note 2. If the 25V Vpp were operated to choose a "write" or "erase" mode while PGM = "V_{IH}," contents of ROM would probably change.

● Example of Standard Power Supply Sequence

The following is an example of standard power supply sequence:



● Inter-mode Timing

The HN48016P has six operating modes, 5V V_{PP} read-out, non-selected, 25V V_{PP} write, write check, write inhibit, and erase. To protect the written data, keep the terminal PGM at "Low" for a period of 10μs before and after turning the terminal V_{PP} from 5V to 25V and vice versa.

The following describes the inter-mode timing for a system that uses the HN48016P.

● Readout→Write→Readout

Before turning the terminal V_{PP} to 25V, keep the terminal PGM at "Low" for a period of 10μs minimum (as indicated by t_{VS}). After the terminal V_{PP} has been turned to 25V, keep the terminal $\overline{CS}$ at "Low" for a period of 10μs minimum (as indicated by t_{PS}). Before turning the terminal V_{PP} to 5V, keep the terminal $\overline{CS}$ at "Low" for a period of 10μs minimum (as indicated by t_{PH}). After the terminal V_{PP} has been turned to 5V, keep the terminal PGM at "Low" for a period of 10μs minimum (as indicated by t_{VH}).

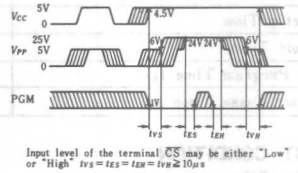
● Readout→Erase→Readout

This timing sequence is shown in Fig. 3. After turning the terminal V_{PP} to 25V, keep the terminal PGM at "Low" for a period of 10μs minimum (as indicated by t_{ES}). Keep the terminal PGM at "Low" for a period of 10μs minimum (as indicated by t_{EH}) before turning the terminal V_{PP} to 5V, as well.

● Erase→Write→Erase

This timing sequence is shown in Fig. 4. Before turning the terminal $\overline{CS}$ to "High (write mode)," keep the terminal.

PGM at "Low" for a period of 10μs minimum (as indicated by t_{EP}). Before turning from "write" to "erase," keep the terminal $\overline{CS}$ at "Low" for a period of 10μs minimum (as indicated by t_{PE}).



Input level of the terminal $\overline{CS}$ may be either "Low" or "High" $t_{VS} = t_{ES} = t_{EH} = t_{VH} \geq 10\mu s$

Fig. 1. Power on-off timing sequence.

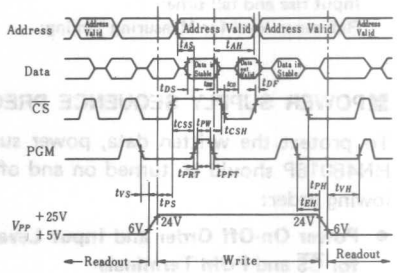


Fig. 2. "Readout→Write→Readout" timing

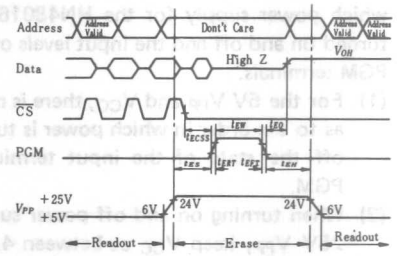


Fig. 3. "Readout→Erase→Readout" timing.

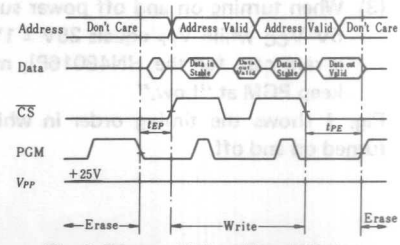


Fig. 4. "Erase→Write→Erase" timing.