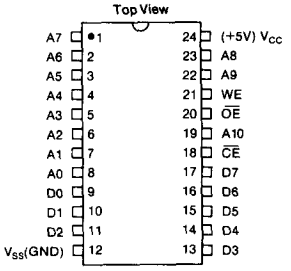
Word Alterable 16K Bit Electrically Erasable and Programmable ROM

FEATURES

- No high voltages – +5V only operation in all modes
- Electrically Word or Block Erasable
- 2048 word x 8 bit organization, fully decoded
- Access time: 300ns maximum
- 20ms Erase and Write times
- Minimum of 10 years' non-volatile data retention
- N-Channel, Si-Gate SNOS technology
- Unlimited Read capability
- Conforms to JEDEC byte-wide pinout standards
- Functionally equivalent to Intel 2816 EEPROM
- Similar pinout to 2716 EPROM

PIN CONFIGURATION

24 PIN DUAL IN LINE



DESCRIPTION

The ER5916 is a high speed electrically word or block erasable and programmable memory fabricated in General Instrument's SNOS technology. Its microprocessor and microcomputer compatible architecture makes it very easy to interface with most popular processors, as does its 300ns maximum access time.

Making it even more attractive to the system design engineer is its +5V only operation in all modes; no high voltages are required for erasing and writing. The ER5916, therefore, offers increased flexibility and opportunities for innovation in new designs since a large amount of data can now be stored in a non-volatile medium and selected portions of it altered with great ease during normal system operation.

This device conforms to JEDEC byte-wide family standards and is functionally compatible with the ER5816 and the Intel 2816 EEPROM. Some differences of pin functions and control logic levels are necessary due to the ER5916's 5V only operation. Refer to the comparison of these two devices included in this data sheet.

Bus contention problems are minimized by the two-line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$). Programming operations are controlled by one TTL level input, WRITE ENABLE (WE).

OPERATION

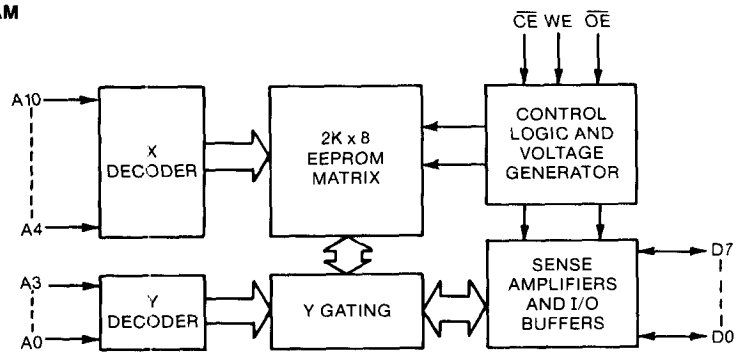
Reading is a ripple-through operation initiated by an address change. If both $\overline{CE}$ and $\overline{OE}$ are low, data appears at the outputs after the normal access time, T_A has elapsed. $\overline{OE}$, when held high, disables the outputs and allows fast access to data when pulsed low.

Erasing and writing of one byte are essentially the same except that all input data bits must be held high for an erase operation.

A chip erase mode is also provided for applications such as program storage in which software updates are made at infrequent intervals. In this mode, all locations are erased into the '1' state with the same, 20ms pulse as required for a single byte erase.

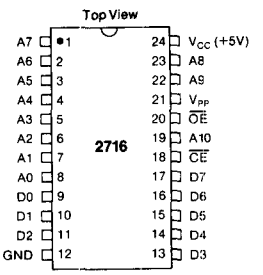
There is a trade-off to be made between the data retention time and the number of Erase/Write cycles performed per location. A gradual, logarithmic reduction in retention time is experienced as the number of Erase/Write cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cut-off or end of life. After 10^5 cycles a typical retention time is 1 year.

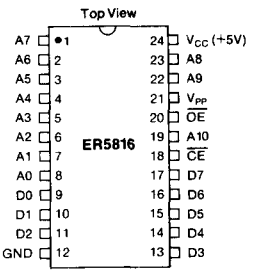
BLOCK DIAGRAM

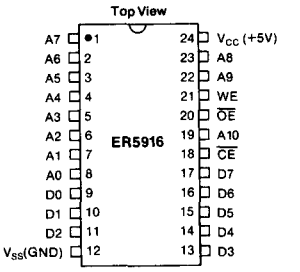


PIN CONFIGURATION

DEVICE	2716				ER5816				ER5916			
MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O	$\overline{CE}$ (18)	$\overline{OE}$ (20)	WE (21)	I/O
READ	V_{IL}	V_{IL}	+5	D_{OUT}	V_{IL}	V_{IL}	+4 to +6	D_{OUT}	V_{IL}	V_{IL}	V_{IL}	D_{OUT}
BYTE ERASE	—	—	—	—	V_{IL}	V_{IH}	+21	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}
BYTE WRITE	Pulsed	V_{IH}	+25	D_{IN}	V_{IL}	V_{IH}	+21	D_{IN}	V_{IL}	V_{IH}	V_{IH}	D_{IN}
CHIP ERASE		ULTRAVIOLET			V_{IL}	+8 to +15	+21	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Don't Care
STANDBY	V_{IH}	Don't Care	+5	High-Z	V_{IH}	Don't Care	+4 to +6	High-Z	V_{IH}	Don't Care		High-Z
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	High-Z	V_{IH}	Don't Care		High-Z	V_{IH}	Don't Care		High-Z







MODES OF OPERATION

$\overline{CE}$	$\overline{OE}$	WE	D0-D7	OPERATING MODE	
0	0	0	D_{OUT}	READ	— Data stored at the addressed location appears at the output pins a time, t_A after an address change.
0	1	1	$D_{IN} = 1$	BYTE ERASE	— Only the selected word is erased to the '1' state.
0	1	1	D_{IN}	BYTE WRITE	— Data at the data inputs is written into the selected location. Note that correct writing may only occur if the location has been previously erased.
0	0	1	Don't Care	BLOCK ERASE	— The entire contents of memory is erased to the '1' state.
1	Don't Care		High-Z	CHIP DESELECTED	

PIN FUNCTIONS

NAME	FUNCTION
A0-A10	11-Bit Word Address
D0-D7	Data input and output ports — high impedance in deselected mode.
V_{CC}	Power supply input. Normally +5 ± 10% volts.
V_{SS}	Supply pin. Normally at ground potential.
$\overline{CE}$	Chip enable input.
$\overline{OE}$	Output enable input.
WE	Write enable input.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground except pins 20 and 21 ..... +6V to −0.3V
Input voltage, pins 20 and 21 with respect to Ground ..... +24V to −0.3V
Storage Temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{CC} = +5 ±5% volts
Operating Temperature Ranges (T_A): 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1" (except pins 20 and 21)	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input Logic "1" (pins 20 and 21)	V_{IC}	2.0	—	+ 22	V	
Input Logic "0"	V_{IL}	−0.1	—	+ 0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −400μA
Output Logic "0"	V_{OL}	V_{SS}	—	0.4	V	I_{OL} = 2.1mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	40	90	mA	
Chip Deselected	I_{CC}	—	15	25	mA	
Power Dissipation:						
Chip Selected	P_D	—	200	450	mW	
Chip Deselected	P_D	—	75	125	mW	

NOTE 1: (T_A) = −40 to +85°C V_{CC} = +5 ±5%, unless otherwise specified.

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Input capacitance	C_I	—	4	6	pF	V_{IN} = 0V
Output capacitance	C_O	—	—	10	pF	V_{OUT} = 0V
Read Mode						All AC Test conditions:
Access time — Address to output delay	t_A	—	—	300	ns	Output load: 1TTL gate + C_L = 100pF
CE to output delay	t_{CE}	—	—	350	ns	
OE to output delay	t_{OE}	10	—	120	ns	Input pulse levels: 0.5V to 2.2V
Data hold time	t_{DH}	—	—	100	ns	
Byte Erase/Write Mode						
Address, $\overline{CE}$ and $\overline{OE}$ setup time	t_{CS}	200	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Address, data, $\overline{CE}$ and $\overline{OE}$ hold time	t_{CH}	2	—	—	μs	
Erase time	t_E	20	25	30	ms	
Write time	t_W	20	25	30	ms	
Block Erase Mode						
CE setup time	t_{CS}	200	—	—	ns	
CE hold time	t_{CH}	2	—	—	μs	
Block erase time	t_{BE}	20	25	30	ms	

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erase time — byte or block	t_E	20	25	30	ms	
Erased state	V_E	—	V_{IH}, V_{OH}	—	—	
Write time	t_W	20	25	30	ms	
Written state	V_W	—	V_{IL}, V_{OL}	—	—	
Data retention time (powered or unpowered)	t_S	10	—	—	Yrs	
Number of Erase/Write cycles per byte	N_{EW}	10^4	—	—	—	See Note 1
Number of Read accesses between refresh	N_{RA}	—	—	—	—	Unlimited

NOTE:
1. Does not imply end of useful life. See "Operation" for further explanation.

TIMING DIAGRAMS

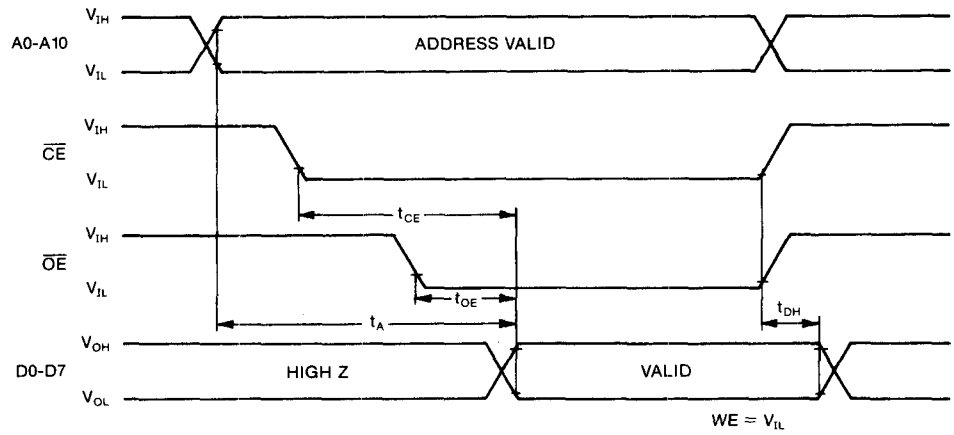


Fig. 1 READ MODE TIMING

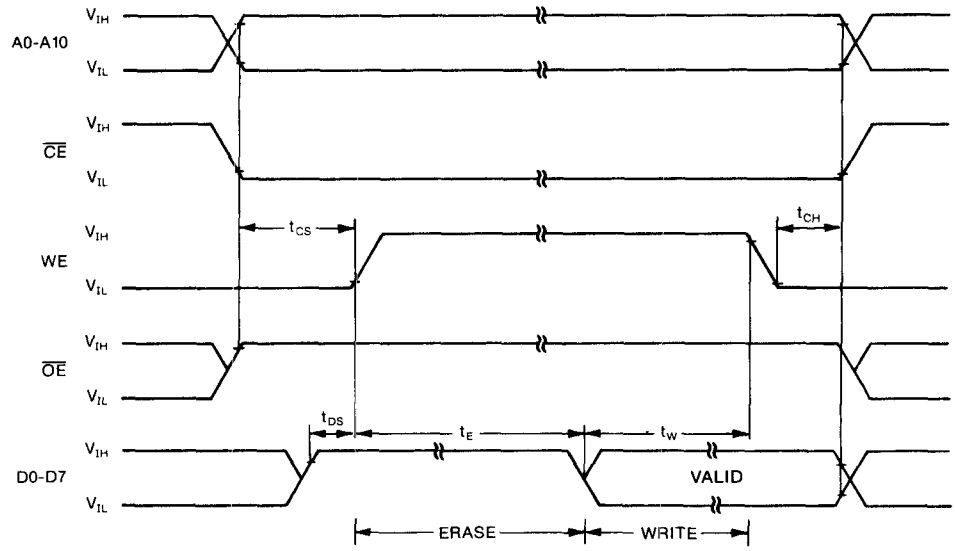


Fig. 2 BYTE ERASE AND WRITE TIMING

TIMING DIAGRAM

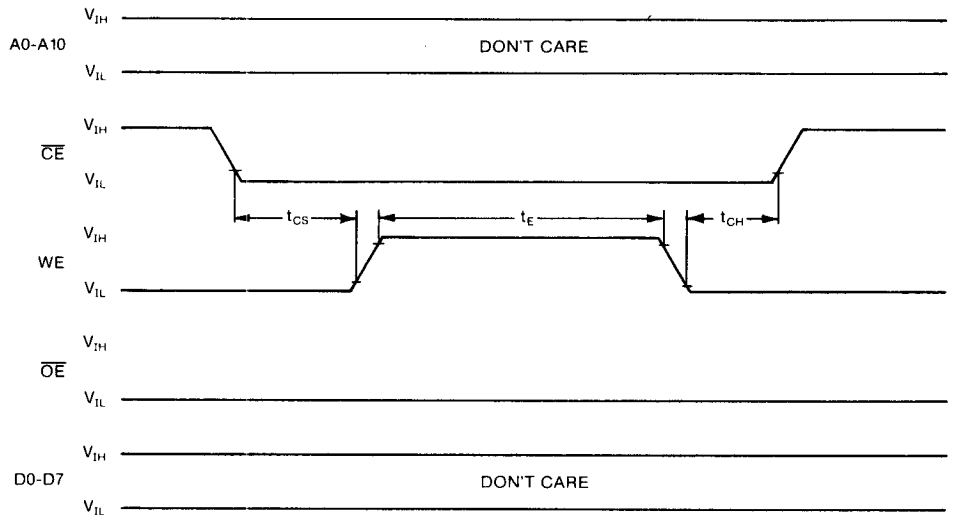


Fig. 3 BLOCK ERASE TIMING