4200 | Static
4300 | RAMs

4096 x 1 N-MOS TTL In/Out

Features

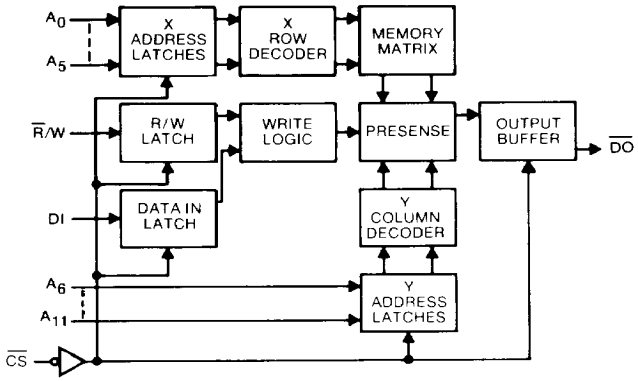
- Fully static Random Access Memory
- Access times as low as 120 nS maximum
- Cycle times as low as 250 nS maximum
- Typical operating power less than 450 mW
- Typical stand-by power less than 30 mW
- Data retention with low V_{DD}
- Pin and voltage compatible with standard 22-pin 4K Dynamic RAMs
- TTL compatible Three-State outputs
- Fully decoded

General Description

The GTE Microcircuits 4200/4300 Static RAMs are N-Channel Random Access Memories, organized as 4096 words by one bit configurations. They use a fully static memory cell which eliminates the need for refresh circuitry. All inputs are TTL compatible, and the three-state data outputs can each drive one TTL load of any type.

The $\overline{\text{Chip Select}}$ input provides for simple memory expansion and low system power, by putting unselected devices into a high output impedance and low power state. For additional power savings, V_{DD} can be reduced significantly, thus allowing data to be retained economically under battery power conditions.

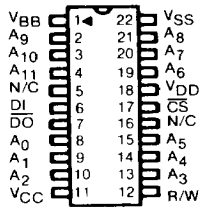
Block Diagram



Pin Configuration

A_N	Address Inputs
DI	Data Input
$\overline{DO}$	$\overline{\text{Data Output}}$
$\overline{CS}$	$\overline{\text{Chip Select}}$ Input
$\overline{R/W}$	$\overline{\text{Read}}$/Write Input
N/C	No Internal Connection
V_{SS}	Ground
V_{BB}	Supply Voltage (—5V)
V_{CC}	Supply Voltage (+5V)
V_{DD}	Supply Voltage (+12V)

TOP VIEW



Specifications

	MAX. ACCESS TIME (nSec)	MIN. CYCLE TIME (nSec)	MAX. V_{DD} SELECTED CURRENT (mA)	MAX. V_{DD} UNSELECTED CURRENT (mA)	MAX. V_{DD} STANDBY CURRENT (mA)
4200A	200	350	50	15	6
4200B	150	300	55	15	6
4300A	120	250	45	8	6

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Microcircuits

Recommended Operating Conditions (T_{AMB} = 0° C to 70° C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Substrate Voltage	V_{BB}	-4.5	-5	-5.5	Vdc
Input High Level	V_{IH}	2.4	–	5.25	Vdc
Input Low Level (4200)	V_{IL}	-0.1	–	0.7	Vdc
Input Low Level (4300)	V_{IL}	-0.1	–	0.8	Vdc
Chip Select High Level	V_{CH}	8	12	15	Vdc
Chip Select Low Level	V_{CL}	-1	–	0.5	Vdc

DC Electrical Characteristics (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	4300A MIN	4300A MAX	UNIT	CONDITIONS
Input Current	I_{IN}	-20	+20	-20	+20	-20	+20	μA	V_{IN} = 0.7V or 5V
Chip Select Input Current	I_{CS}	-20	+20	-20	+20	-20	+20	μA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	–	0.5	–	0.5	–	0.5	Vdc	I_{OL} = 2.0mA Fig. 4
Output "High" Voltage	V_{OH}	2.7	V_{CC}	2.7	V_{CC}	2.7	V_{CC}	Vdc	I_{OH} = -500μA Fig. 4
Output Current (Unselected)	I_{DO}	-20	+20	-20	+20	-20	+20	μA	V_{OUT} = 2.7V, V_{CS} = 12V
Supply Current (Selected and Averaged Over One Cycle) 4300A 4200A 4200B T_{CSW} 120 200 150 T_C 210 350 300 For Other Conditions See Figure 3A and 3B	I_{DD}	–	50	–	55	–	45	mA	T_{AMB} = 25°C V_{DD} = 12V V_{CC} = 5V V_{BB} = -5V V_{CS} = 0.5V
Supply Current (Unselected) T_{AMB} = 25°C	I_{DD}	–	5	–	5	–	4	mA	V_{DD} = 12V V_{CC} = 5V V_{BB} = -5V V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 70°C	I_{DD}	–	15	–	15	–	8	mA	
Substrate Current	I_{BB}		-3	–	-3	–	-2	mA	
Reference Supply Current	I_{CC}	–	100	–	100	–	100	μA	
Standby Current at Reduced Voltages T_{AMB} = 25°C	I_{DDS}	–	2	–	2	–	2	mA	V_{CS} = 4V to 15V V_{DD} = 4V V_{BB} = -4V V_{CC} = 0V
Standby Current at Reduced Voltages T_{AMB} = 70°C	I_{DDS}	–	6	–	6	–	6	mA	

Read Cycle—AC Characteristics

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	4300A MIN	4300A MAX	UNIT	CONDITIONS
Chip Select Read Pulse Width	T_{CSR}	200	–	150	–	120	∞	nS	Full Operating Voltage and Temperature Range
Chip Select Rise and Fall Time*	T_{CR}, T_{CF}	–	100	–	100	–	100	nS	
Set Up Time	T_P	0	–	0	–	0	–	nS	
Access Time	T_A	–	200	–	150	–	120	nS	
Cycle Time, T_{CR} = T_{CF} = 10ns	T_C	350	–	300	–	250	–	nS	
Data Hold Time	T_H	100	–	100	–	75	–	nS	
Output Recovery Time	T_{DR}	10	–	10	–	10	–	nS	
Read Recovery Time	T_{CRR}	125	–	125	–	90	–	nS	

Write Cycle—AC Characteristics

CHARACTERISTICS	SYMBOL	4200A MIN	4200A MAX	4200B MIN	4200B MAX	4300A MIN	4300A MAX	UNIT	CONDITIONS
Chip Select Write Pulse Width	T_{CSW}	200	–	150	–	140	∞	nS	Full Operating Voltage and Temperature Range
Chip Select Rise and Fall Time *	T_{CR}, T_{CF}	–	100	–	100	–	100	nS	
Set Up Time	T_P	0	–	0	–	0	–	nS	
Cycle Time, T_{CR} = T_{CF} = 10ns	T_C	350	–	300	–	250	–	nS	
Data Hold Time	T_H	100	–	100	–	75	–	nS	
Write Recovery Time	T_{CWR}	125	–	125	–	90	–	nS	

*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10ns For Read and Write Cycle

Capacitance (Over Full Temperature Range and Worst Case Voltage Conditions)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance (Except Chip Select)	C_{IN}	–	4	6	pF	V_{IN} = 2.4V, V_{CS} = 12V
Input Capacitance Chip Select	C_{CS}	–	6	10	pF	V_{CS} = 12V or 0V
Output Capacitance	C_O	–	6	8	pF	V_O = 2.7V V_{CS} = 12V

Absolute Maximum Ratings (See Note 1) (Referenced to GND)

RATING	SYMBOL	VALUE	UNIT
Supply Voltages	V_{DD}	-.5 to +18	Vdc
	V_{CC}	-.5 to +7	Vdc
	V_{BB}	+.5 to -18	Vdc
Input & Output Voltages (Except Chip Select)	V_I, V_O	V_{BB} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{BB} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range		-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C ambient. Derate 13.5mW/°C.

Figure 1 — Read Cycle

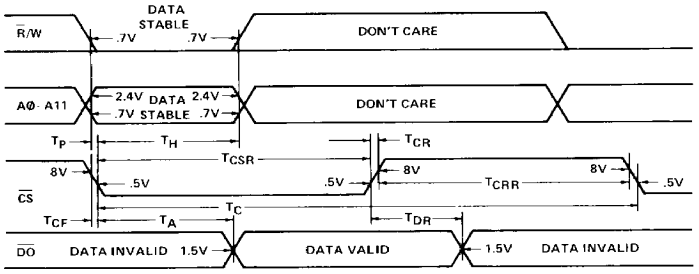
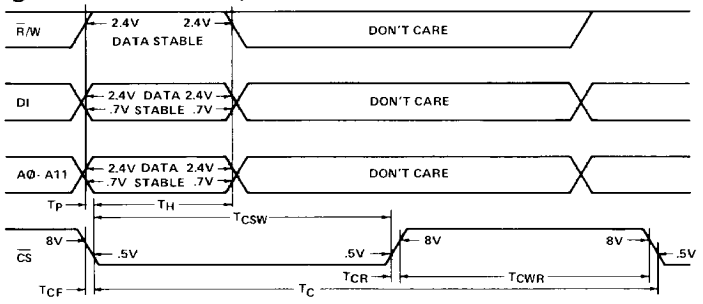


Figure 2 — Write Cycle



Functional Description

The GTE Microcircuits 4200/4300 are 4096 bit static RAMs with memory cells organized in an array of 64 rows by 64 columns (4096 words x 1 bit). Each memory cell is addressed by simultaneously decoding the X addresses (A_0 through A_5) for the rows and the Y addresses (A_6 through A_{11}) for the columns. Data is written or read on separate input (DI) and output ($\overline{DO}$) pins. Logic level 1 is represented by a high state on pin DI but is represented on $\overline{DO}$ by a low state. The operation on the memory is controlled by Chip Select ($\overline{CS}$) and Read/Write ($\overline{R}/W$). When $\overline{CS}$ is high, all pins are in an inoperative high impedance state, and power is supplied only to the memory elements. When $\overline{CS}$ is low, the memory is enabled for reading and writing.

The negative going edge of $\overline{CS}$ begins timing for a read cycle. Data on $\overline{R}/W$ and address pins (A_N) must be stable for time T_H. $\overline{R}/W$ and A_N will then have been latched into D type flip flops and no longer need to be held stable. Output data will be presented on $\overline{DO}$ within time T_A and will remain until time T_{DR} after $\overline{CS}$ goes high. Data will then be invalid. After time T_C another read or write cycle can be initiated.

The negative going edge of $\overline{CS}$ also begins timing for a write cycle. $\overline{R}/W$, A_N and DI must be held stable for time T_H. These inputs will then have been latched and DI will be entered within time T_{CSW}. Another read or write cycle can be initiated after time T_C.

The memory cells (because they are cross coupled high impedance static cells) will retain data down to V_{DD} = 4V, V_{BB} = -4V.

Figure 3A — 4200 Operating I_{DD} as a Function of Cycle Time

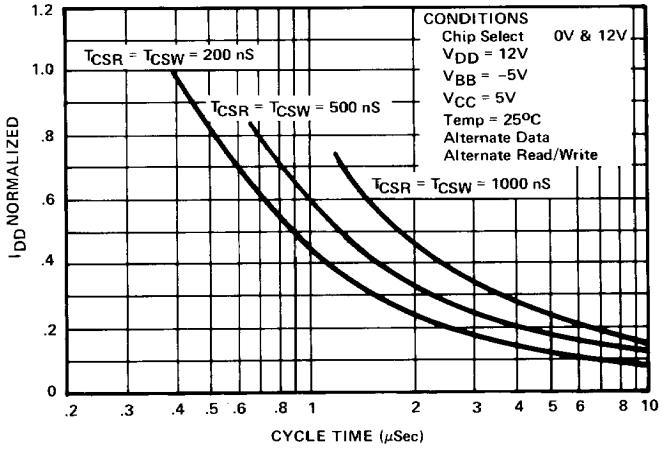


Figure 3B — 4300 Operating I_{DD} as a Function of Cycle Time

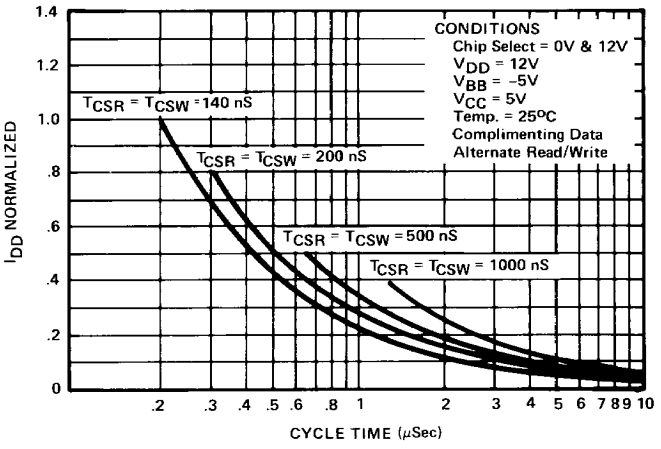
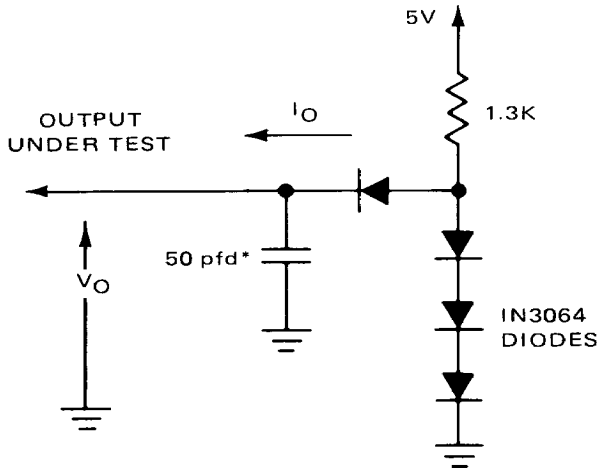


Figure 4 — Output Test Load



*Capacitance loading to simulate effect of seven additional outputs plus one TTL input.

Packaging Dimensions

4200/4300 (22 Pin)

DIMENSIONS

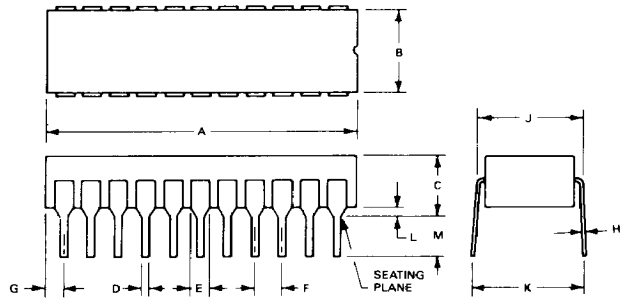
"P" PACKAGE (PLASTIC)

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	27.940	29.718	1.100	1.170
B	8.636	9.144	0.340	0.360
C	4.318	5.080	0.170	0.200
D	0.356	0.559	0.014	0.022
E	1.016	1.778	0.040	0.070
F	2.413	2.667	0.095	0.105
G	1.016	2.032	0.040	0.080
H	0.203	0.305	0.008	0.012
J	9.144	10.160	0.360	0.400
K	10.160	REF.	0.400	REF.
L	0.508	1.016	0.020	0.040
M	2.540	3.937	0.100	0.155

"D" PACKAGE (CERDIP)

DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	26.787	27.559	1.055	1.085
B	9.398	10.160	0.370	0.400
C	3.937	5.588	0.155	0.220
D	0.381	0.584	0.015	0.023
E	1.016	1.651	0.040	0.065
F	2.286	2.794	0.090	0.110
G	0.381	1.016	0.015	0.040
H	0.203	0.305	0.008	0.012
J	10.160	10.795	0.400	0.425
K	10.160	12.192	0.400	0.480
L	.381	1.016	0.015	0.040
M	2.540	4.445	0.100	0.160

TYPICAL OUTLINE DRAWING



Ordering Information

Device	Access	Cycle	Package	Temp. Range
4200ACD	200	350	Cerdip	0°C to + 70°C
4200ACP	200	350	Plastic	0°C to + 70°C
4200BCD	150	300	Cerdip	0°C to + 70°C
4200BCP	150	300	Plastic	0°C to + 70°C
4300ACD	120	250	Cerdip	0°C to + 70°C
4300ACP	120	250	Plastic	0°C to + 70°C

WARNING:

MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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