# EMM8108

## SEMI 8108 300NSEC, STATIC, TTL IN/OUT 1024 x 8 N-MOS RAM
## SEMI 8108 500NSEC, STATIC, TTL IN/OUT 1024 x 8 N-MOS RAM

EMM SEMI, INC. 8108 300 NSEC, STATIC, TTL IN/OUT 1024 x 8 N-MOS RAM

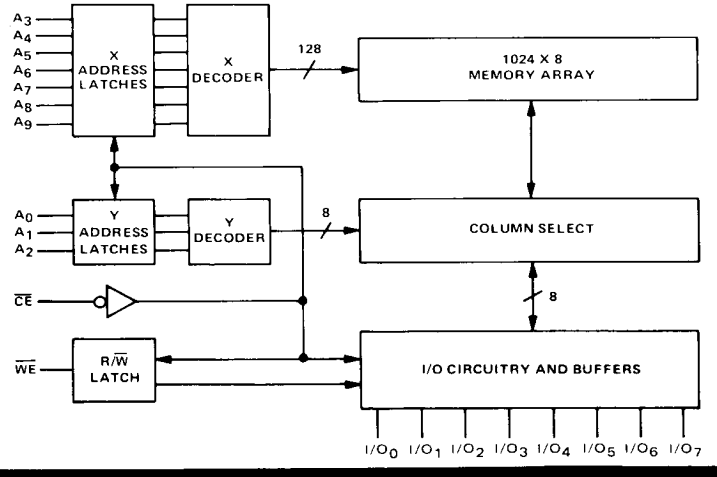
### FEATURES

- 1024 words X 8 bits
- EPROM, PROM, ROM pinout compatible
- Common I/O bus
- Single +5V power supply
- No maximum limit on Chip Enable ($\overline{CE}$) pulse width
- 300 or 500 nsec maximum access time
- Less than 60 mW power (disabled)
- Less than 270 mW power (enabled)

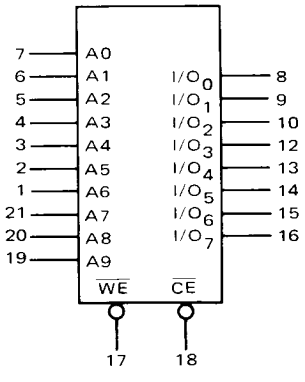
### GENERAL DESCRIPTION

EMM SEMI'S 8108 is a 8192-bit static RAM, ideally suited for microprocessor applications, with a choice of 300 or 500 nanosecond maximum access time. The 8108 has common data input/output pins for connection to a data bus. It requires only a single +5 volt power supply, and is TTL compatible on all inputs and outputs. This device also has a low power disabled mode which dissipates less than 60 mW power.

### BLOCK DIAGRAM

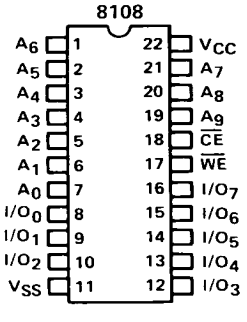



### LOGIC SYMBOL




| $\overline{CE}$ | $\overline{WE}$ | $I/O_n$ | STATUS | MODE |
|---|---|---|---|---|
| H | Don't Care | High Z | Disabled | Standby |
| L | H | Data | Enabled | Read |
| L | L | L | Enabled | Write 0 |
| L | L | H | Enabled | Write 1 |

### PIN CONFIGURATION




### PIN NAMES

| | |
|---|---|
| $A_n$ | Address Inputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{WE}$ | Write Enable Control Input |
| $I/O_n$ | Data Bus Input/Output Pins |
| $V_{CC}$ | +5V Power Supply |
| $V_{SS}$ | 0V Power Supply |

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## RECOMMENDED OPERATING CONDITIONS: ($T_{AMB}$ = 0°C to 70°C)

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Input High Level | $V_{IH}$ | 2.0 | – | 5.25 | V |
| Input Low Level | $V_{IL}$ | -0.5 | – | 0.8 | V |

## DC CHARACTERISTICS: $T_A$ = 0°C to +70°C. $V_{CC}$ = +5V ± +5%, unless otherwise noted.

| PARAMETER | SYMBOL | 8108 | | | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Output HIGH Voltage | $V_{OH}$ | 2.4 | – | 5.25 | V | $I_{OH}$ = -200 μA |
| Output LOW Voltage | $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = 2.1 mA (NOTE 1) |
| Output Leakage Current | $I_{LO}$ | -10 | – | +10 | μA | $V_{I/O}$ = 0.4 V to $V_{CC}$ $\overline{CE}$ = 2.0 V |
| Input Leakage Current | $I_{LI}$ | -10 | – | +10 | μA | $V_{IN}$ = 0 to 5.25 V |
| Power Supply Current (Device Disabled) | $I_{CC1}$ | – | 5 | 10 | mA | CE ⩾ 2.0 V |
| Power Supply Current (Device Enabled) | $I_{CC2}$ | – | 25 | 50 | mA | CE ⩽ 0.8 V |

## READ CYCLE – AC CHARACTERISTICS

| CHARACTERISTICS | SYMBOL | 8108-3 | | 8108-5 | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Chip Enable Read Pulse Width | $T_{CER}$ | 300 | ∞ | 500 | ∞ | nS | Full Operating Voltage and Temperature Range |
| Chip Enable Rise and Fall Time* | $T_{CR}$, $T_{CF}$ | – | 100 | – | 100 | nS | |
| Set Up Time | $T_P$ | 0 | – | 0 | – | nS | |
| Access Time | $T_A$ | – | 300 | – | 500 | nS | |
| Cycle Time, $T_{CR}$ = $T_{CF}$ = 10 nS | $T_C$ | 450 | – | 700 | – | nS | |
| Data Hold Time | $T_H$ | 100 | – | 100 | – | nS | |
| Output Recovery Time | $T_{DR}$ | 0 | 75 | 0 | 75 | nS | |
| Read Recovery Time | $T_{CRR}$ | 130 | – | 180 | – | nS | |

## WRITE CYCLE – AC CHARACTERISTICS

| CHARACTERISTICS | SYMBOL | 8108-3 | | 8108-5 | | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Chip Enable Write Pulse Width | $T_{CEW}$ | 300 | ∞ | 500 | ∞ | nS | Full Operating Voltage and Temperature Range |
| Chip Enable Rise and Fall Time (NOTE 2) | $T_{CR}$, $T_{CF}$ | – | 100 | – | 100 | nS | |
| Set Up Time | $T_P$ | 0 | – | 0 | – | nS | |
| Cycle Time, $T_{CR}$ = $T_{CF}$ = 10 nS | $T_C$ | 450 | – | 700 | – | nS | |
| Data Hold Time | $T_H$ | 100 | – | 100 | – | nS | |
| Write Recovery Time | $T_{CWR}$ | 130 | – | 180 | – | nS | |

## CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | – | 5 | pF | $V_{I/O}$ = 0V |
| Output Capacitance | $C_{OUT}$ | – | 5 | pF | |

NOTE 1: Output terminated per test output load diagram. Any valid combination of input voltages, $V_{CC}$, and temperature.

NOTE 2: Typical Chip Select Rise and Fall Time ($T_{CR}$ and $T_{CF}$) is 10 nS For Read and Write Cycle.

## ABSOLUTE MAXIMUM RATEINGS
## (See NOTE 1 ) (Referenced to GND)

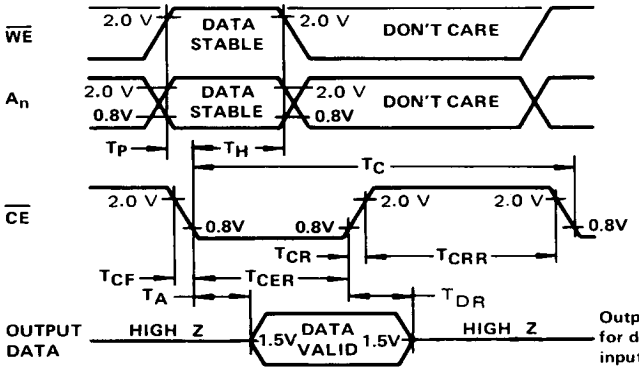
| RATING | VALUE | UNIT |
|---|---|---|
| Voltage to Any Pin With Respect to GND | -0.5 to +7.0 | Vdc |
| Power Dissipation | 1.6 (NOTE 2) | W |
| Current Into/From Output | 50 | ma |
| Operating Ambient Temperature Range ($T_{AMB}$) | 0 to 70 | °C |
| Storage Temperature ($T_{STOR}$) | -65 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

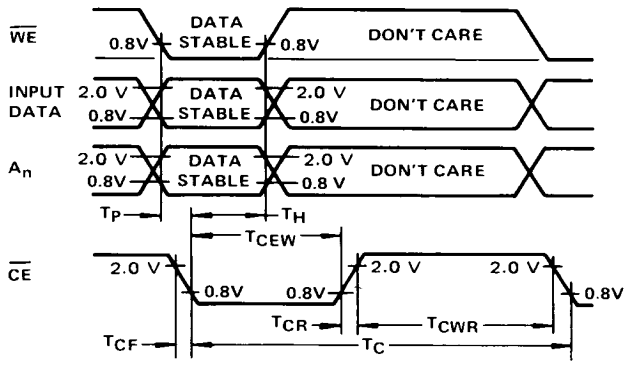
NOTE 2: At 25°C Ambient. Derate 13.5 mW/°C.

**READ CYCLE – AC CHARACTERISTICS**




Output Voltage is HIGH for data originally input as HIGH

**WRITE CYCLE – AC CHARACTERISTICS**




## FUNCTIONAL DESCRIPTION

The EMM SEMI 8108 is an 8192-bit static RAM with memory cells organized in eight arrays of 128 rows by 8 columns (1024 words X 8 bits). Each eight-bit word is addressed by simultaneously decoding the X addresses (A3 through A9) for the rows, and the Y addresses (A0 through A2) for the columns. Data is written or read in parallel on eight common input/output pins ($I/O_n$). The operation of the 8108 is controlled by Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$).

When $\overline{CE}$ is high, all outputs are in an inoperative high impedance state, and power is supplied only to the memory elements. When $\overline{CE}$ is low, the memory is enabled for reading and writing.

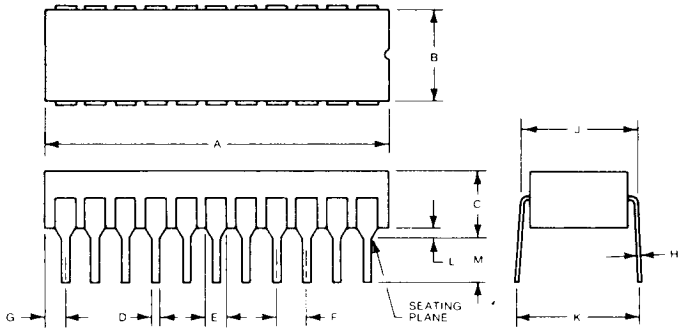
The negative going edge of $\overline{CE}$ begins timing for a read cycle. Data on $\overline{WE}$ and address pins ($A_n$) must be stable for time $T_H$. $\overline{WE}$ and $A_n$ will then have been latched into "D" type flip flops and no longer need to be held stable. Output data will be presented on the eight output pins ($I/O_n$) within time $T_A$ and will remain until time $T_{OTD}$ after $\overline{CE}$ goes high. Data will then be invalid. After time $T_C$ another read or write cycle can be initiated.

The negative going edge of $\overline{CE}$ also begins timing for a write cycle. $\overline{WE}$ and I/O must be held stable for time $T_H$. These inputs will then have been latched and I/O will be entered within time $T_{CEW}$. Another read or write cycle can be initiated after time $T_C$.

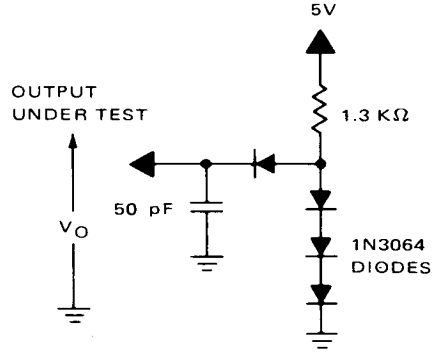
## PACKAGING DIMENSIONS

"D" PACKAGE (CERDIP)

| DIM. | MILLIMETERS MIN. | MILLIMETERS MAX. | INCHES MIN. | INCHES MAX. |
|---|---|---|---|---|
| A | 26.787 | 27.559 | 1.055 | 1.085 |
| B | 9.398 | 10.160 | 0.370 | 0.400 |
| C | 3.937 | 5.588 | 0.155 | 0.220 |
| D | 0.381 | 0.584 | 0.015 | 0.023 |
| E | 1.016 | 1.651 | 0.040 | 0.065 |
| F | 2.286 | 2.794 | 0.090 | 0.110 |
| G | 0.381 | 1.016 | 0.015 | 0.040 |
| H | 0.203 | 0.305 | 0.008 | 0.012 |
| J | 10.160 | 10.795 | 0.400 | 0.425 |
| K | 10.160 | 12.192 | 0.400 | 0.480 |
| L | .381 | 1.016 | 0.015 | 0.040 |
| M | 2.540 | 4.445 | 0.100 | 0.160 |




## TEST OUTPUT LOAD




## ORDERING INFORMATION

| DEVICE | ACCESS TIME | CYCLE TIME | PACKAGE | TEMP. RANGE |
|---|---|---|---|---|
| 8108-3CD | 300 | 450 | CERDIP | 0°C to 70°C |
| 8108-5CD | 500 | 700 | CERDIP | 0°C to 70°C |

**WARNING:**

**MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE**

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

Represented in your area by:

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