PRELIMINARY SPECIFICATION

4044

4K STATIC N-MOS RAM
4096 x 1, 450 ns, TTL In/Out

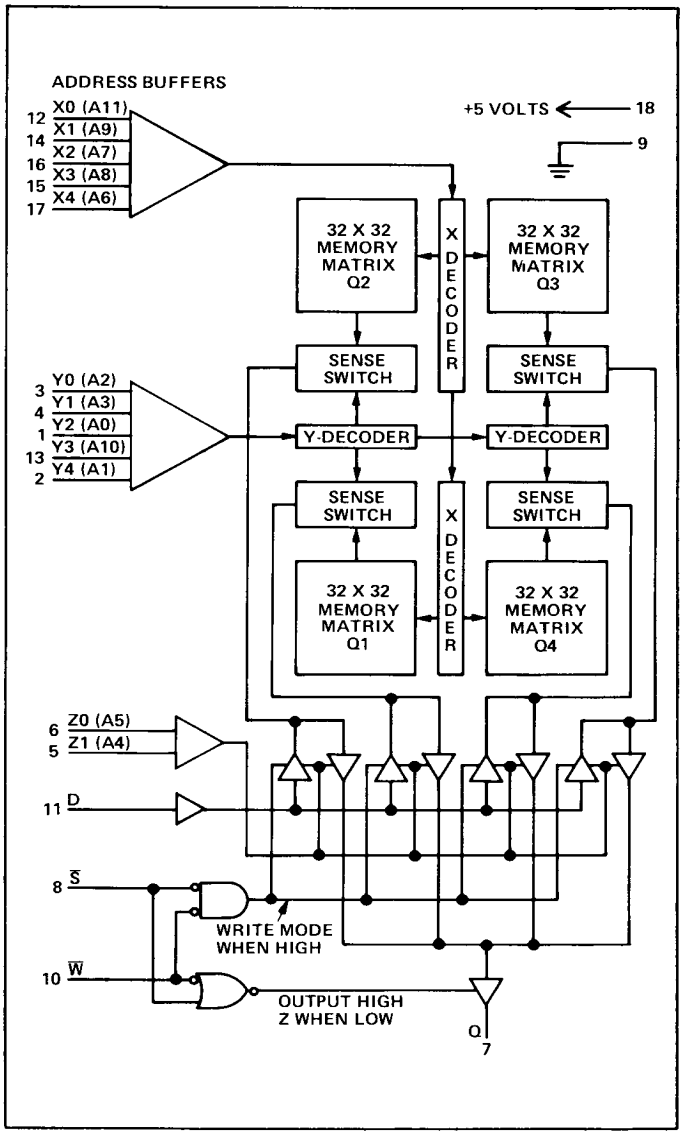
FEATURES

- 4096 words X 1 bit RAM
- High speed 450 ns ACCESS and CYCLE time
- Fully STATIC memory—no clock or refresh required
- Single +5V power supply
- 18-pin ceramic or plastic package
- Low power dissipation—275 mw max @ 70° C
- Three-State, high impedance output
- TTL compatible interface
- Replaces 4 ea 1024 x 1 static RAMs

GENERAL DESCRIPTION

SEMI's 4044 RAMs are fully STATIC 4096 word X 1 bit N-MOS Random Access Memories—requiring no external clocks, strobes or refresh circuitry. The high impedance THREE-STATE output reflects virtually no load, and is ideally suited for multiple-RAM, common bus applications. For simplicity, a single +5V input is the only power supply required. The 4044 is available in a choice of power dissipation (275 or 495 mw max) and plastic or ceramic packaging to meet your particular requirement. SEMI's 4044 is the first choice of designers everywhere—offering high performance, large (expandable) capacity and simplicity of interfacing.

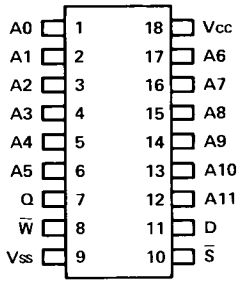
BLOCK DIAGRAM



TRUTH TABLE

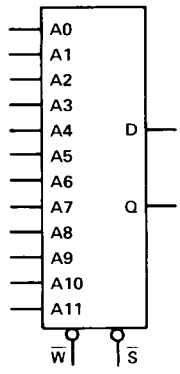
$\overline{S}$	$\overline{W}$	D	Q	STATUS	MODE
H	Don't Care	Don't Care	High Z	Deselect	Standby
L	H	Don't Care	Data	Selected	READ
L	L	L	High Z	Selected	Write 0
L	L	H	High Z	Selected	Write 1

PIN CONFIGURATION



AN	Address Inputs
D	Data Input
Q	Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Vss	Ground
Vcc	+5 V Power Supply

LOGIC SYMBOL



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RECOMMENDED OPERATING CONDITIONS (T_{AMB} = 0° C to 70° C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Level	V_{IH}	2.0		5.5	Vdc
Input Low Level	V_{IL}	-0.5		0.8	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I_{LI}	-10		+10	μA	V_{IN} = -0.5 to +5.5V
Output Leakage Current	I_{LO}	-10		+10	μA	V_{OUT} = 0.0 to 5.5V
Output Voltage High	V_{OH}	2.4			Vdc	I_{OH} = -1.0 ma, V_{CC} = 4.5V
Output Voltage Low	V_{OL}			0.4	Vdc	I_{OL} = 3.2 ma
Power Supply Current						
4044	I_{CC}		50	70	ma	T_{AMB} = 25° C
	I_{CC}			90	ma	T_{AMB} = 70° C
L4044	I_{CC}		35	40	ma	T_{AMB} = 25° C
	I_{CC}			50	ma	T_{AMB} = 70° C

READ CYCLE—AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Read Cycle Time	T_{RC}	450			ns	Full Operating Voltage and Temperature Range
Access Time	T_A			450	ns	
Chip Enable to Output Enable	T_{CO}			100	ns	
Data Valid After Address	T_{OHA}	10			ns	
Output Disable From Deselection	T_{OTD}			100	ns	

WRITE CYCLE — AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Write Cycle Time	T_{WC}	450			ns	Full Operating Voltage and Temperature Range
Address To Write Time	T_{AW}	0			ns	
Write Pulse Width	T_W	200			ns	
Write Recovery Time	T_{WR}	0			ns	
Data Set Up Time	T_{DW}	200			ns	
Data Hold Time	T_{DH}	0			ns	
Output Disable From Write or Chip Enable	T_{OTW}			100	ns	
Output Enabled After Write Disabled	T_{OE}			100	ns	
Chip Select To Output Active	T_{CX}	20			ns	
Read, Modify-Write Cycle	T_{RWC}	650			ns	

CAPACITANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Capacitance	C_{IN}		4	5	pF	V_{OUT} = 0.0 to 5.5 V
Output Capacitance	C_{OUT}		4	5	pF	

ABSOLUTE MAXIMUM RATINGS (See NOTE 1) (Referenced to GND)

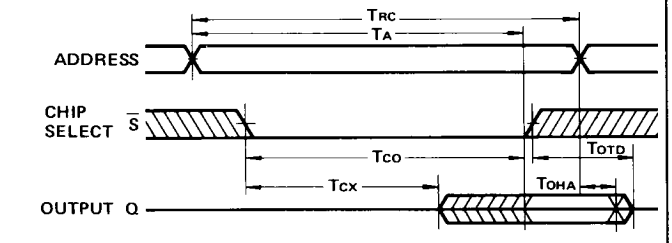
RATING	VALUE	UNIT
Voltage to Any Pin With Respect to GND	-0.5 to +7.0	Vdc
Power Dissipation	1.6 (NOTE 2)	W
Current Into/From Output	50	ma
Operating Ambient Temperature Range (T_{AMB})	0 to 70	°C
Storage Temperature (T_{STOR})	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

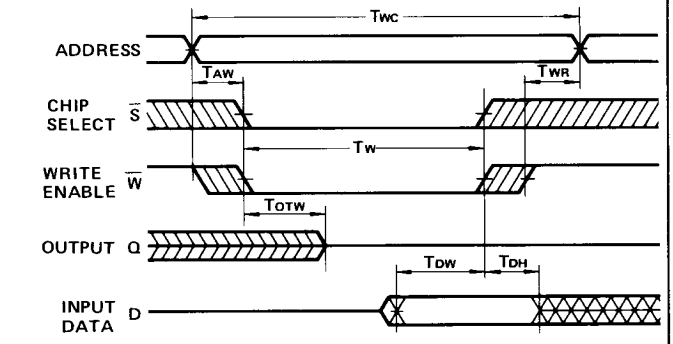
NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25° C Ambient. Derate 13.5 mw/° C.

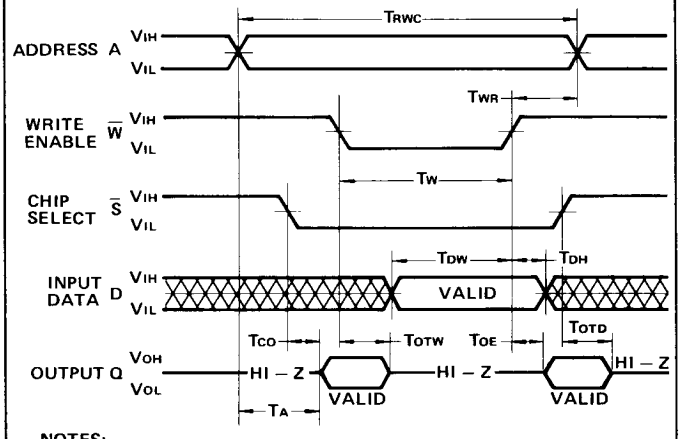
READ CYCLE TIMING



WRITE CYCLE TIMING



READ/MODIFY-WRITE CYCLE TIMING



NOTES:
1. $\overline{W}$ is high for a Read Cycle.
2. Tw is measured from the latter of $\overline{S}$ or $\overline{W}$ going low to the earlier of $\overline{S}$ or $\overline{W}$ going high.
3. $\overline{W}$ or $\overline{S}$ must be high prior to a write cycle to prevent an erroneous write during the address transitions.

FUNCTIONAL DESCRIPTION

EMM SEMI's 4044 is a 4096 bit static RAM, organized in a 4096 word X 1 bit configuration. Each word is selectively accessed by address lines A_0 through A_{11}, with data being read or written on separate data input/output lines (D and Q), as controlled by the Write Enable ($\overline{W}$) or Chip Select ($\overline{S}$) functions.

Since no address setup time is required, data access is quite simple. The 4044 is in a read mode whenever $\overline{W}$ is high. With $\overline{W}$ high and $\overline{S}$ low, the array may be read by simply toggling the input address. Valid output data becomes available after time T_A, following each address change. However, should $\overline{S}$ be used to control the read mode, valid data access time must be equal to or greater than T_A, but can not occur earlier than T_{CO} from $\overline{S}$ going low.

The write mode occurs whenever $\overline{S}$ and $\overline{W}$ are both low. Stored data is therefore preserved as long as either $\overline{S}$ or $\overline{W}$ is high.

Possible write modes are as follows:

1. $\overline{S}$ is held low. T_{AW} and T_W are then defined by $\overline{W}$ going from a high state to a low state and T_{WR} is defined by $\overline{W}$ going from a low state to a high state.
2. $\overline{W}$ is held low. $\overline{S}$ going low is then used to define T_{AW} and T_W. $\overline{S}$ going high is used to define T_{WR}.
3. $\overline{S}$ and $\overline{W}$ are both used. Timing at the beginning of the cycle is then defined by the latter of $\overline{S}$ or $\overline{W}$ going low and timing at the end of the cycle is determined by the earlier of $\overline{S}$ or $\overline{W}$ going high.

The address must remain stable for the full write cycle. However, data inputs are not required to remain stable for the full cycle. The correct logic level will be entered as long as input data is stable for the time period T_{DW} during the write cycle.

NOTES:

1. T_{AW} is measured from the latter of $\overline{S}$ or $\overline{W}$ going low.
2. T_W is measured from the latter of $\overline{S}$ or $\overline{W}$ going low to the earlier of $\overline{S}$ or $\overline{W}$ going high.
3. T_{WR} is measured from the earlier of $\overline{S}$ or $\overline{W}$ going high.
4. T_{DH} and T_{DW} are measured from the earlier of $\overline{S}$ or $\overline{W}$ going high.
5. T_{OTW} is measured from $\overline{W}$ going low or $\overline{S}$ going high, whichever occurs first.
6. Timing diagrams are based on loading to simulate the capacitive effect of ten additional outputs plus the current loading effect of one TTL input.
7. Input pulse levels are 0.8 volts for logic low, to 2.0 volts for logic high.
8. Input rise and fall times are of equal value (10 ns).
9. Timing is measured from the 1.5 volt level whether the level is going high or low.
10. The output line (Q) is a high impedance during the write mode, or when $\overline{S}$ is high. The input (D) always represents a high impedance.

ORDERING INFORMATION

DEVICE	ACCESS TIME	MAXIMUM POWER DISSIPATION	PACKAGE	TEMP. RANGE
4044-UCA	450 ns	495 mw	18-Pin Ceramic	0°C to 70°C
L4044-UCA	450 ns	275 mw	18-Pin Ceramic	0°C to 70°C
4044-UCB	450 ns	495 mw	18-Pin Plastic	0°C to 70°C
L4044-UCB	450 ns	275 mw	18-Pin Plastic	0°C to 70°C

EMM/SEMI reserves the right to make changes at any time in order to improve design and to supply the best product possible.

WARNING: MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or in conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

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