# Introduction to CMOS Non-Volatile Memories

## Product Line Overview

The Cypress CMOS family of high-performance byte-wide and word-wide (x16) non-volatile memories spans 4-kilobit to 1-megabit densities and three functional configurations. Products are typically available as EPROMs (Erasable, Programmable ROMs) in 300- and 600-mil windowed cerDIP packages, leadless chip carriers (LCCs), leaded chip carriers (CLCC, PLCC) and flatpacks. They are also available as PROMs in similarly configured plastic and opaque hermetic packages. With the exception of the 4K PROMs (registered only) and 1M EPROMs, all densities are available in both registered and non-registered versions. The registered devices operate in either synchronous or asynchronous modes and may have an INITIALIZATION feature to preload the pipeline register, which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at or above the speed level of their bipolar counterparts with the advantages of lower power consumption and reprogrammability inherent in CMOS technology. They operate with 10% power supply tolerances and can withstand 2000 volts of electrostatic discharge.

## Technology Introduction

Cypress non-volatile memories are executed in N-well CMOS EPROM processes that provide basic gate delays of 235 picoseconds for a fanout of one with a power consumption of 45 femto-joules. These processes provide the basis for the development of Cypress LSI products, which outperform the fastest bipolar equivalents.

Historically, CMOS static RAMs have challenged bipolar RAMs for speed, while CMOS PROMs have been slower than the fused bipolar devices because (1) the typical single transistor CMOS cell is slow compared to any "fuse," and (2) CMOS technologies were optimized for programmability and density at the expense of speed. Innovative Cypress EPROM technology overcomes both of these historical limitations. A substrate bias generator is employed in an EPROM technology to improve performance and raise latch-up immunity to greater than 200 mA. The result is a CMOS EPROM technology that outperforms bipolar fuse technology for both density and speed, particularly at higher densities. Limitations of devices implemented in the bipolar fuse technology such as programming yield, power dissipation and higher-density performance are eliminated or greatly reduced using Cypress CMOS EPROM technology.

## Programming

### Differential Memory Cells

Cypress non-volatile memories are programmed a byte at a time by applying VPP (~12V) to the programming pin and the desired logic levels to input pins. Both logic 1 and logic 0 are programmed into the differential cell. A bit is programmed by applying VPP on the control gate and 9 volts on the drain of the floating-gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate, thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts, resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is the corrected logic state. Because an unprogrammed cell has neither a 1 nor a 0 in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference, which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual bits allowing the monitoring of the quality of programming during the manufacturing operation.

### Single-Ended Memory Cells (All CY7C products except CY7C271A, CY27C128, and CY27C256)

The programming mechanism of the EPROM transistor in a single-ended memory cell is the same as its counterpart in a double-ended memory cell. The difference is that only 1s are programmed in a single-ended cell. A 1 applied to the I/O pin during programming causes an erased EPROM transistor to be programmed, while a 0 allows the EPROM transistor to remain unprogrammed. Erasure resets all bits to 0.

### Single-Ended Memory Cells (All CY27H and CY27C products except CY27C128, and CY27C256)

These devices are similar except that 0s are programmed. A 1 does not program a bit. After erasure, all bits are reset to 1.

## Erasability

This is available for devices in windowed packages, both registered and non-registered. Wavelengths of light less than 4000 Angstroms begin to erase Cypress non-volatile memories. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm2. For an ultraviolet lamp with a 12 $mV/cm^2$ power rating, the exposure time would be approximately 35 minutes.

The device needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. The recommended maximum dosage is 7258 Wsec/cm2.

Some devices are sensitive to photo-electric effects during programming. Cypress recommends covering the windows of reprogrammable devices during programming.

## Reliability

CMOS technology has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed an erased multiple times, CMOS PROMs

from Cypress can be tested 100% for programmability during the manufacturing process. Because each device contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged, thus assuring the user that not only will every cell program, but that the product performs to the specification.

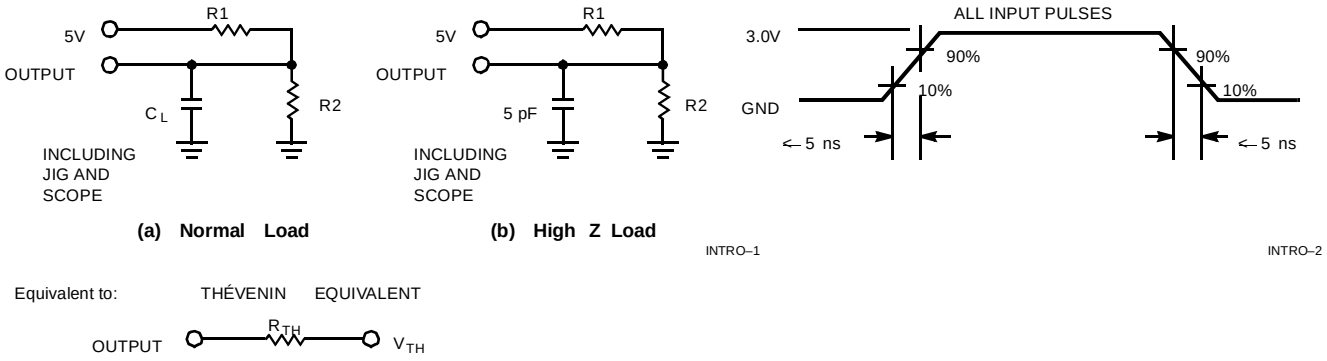
## General Testing Information

Incoming test procedures on high speed (faster that 45 ns) devices should be carefully planned, taking into account the high-performance and output drive capabilities of the parts. The following notes may be useful:

- Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1 µF or larger capacitor and a 0.01 µF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
- All device test loads should be located within 2″ of device outputs.
- Do not leave any inputs disconnected (floating) during any tests.
- Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
- $V_{OH}$ and $V_{OL}$ are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- Capacitance is tested initially and after any design or process changes that may affect these parameters.
- The CMOS process does not provide a clamp diode. However, the Cypress PROM Products are insensitive to -3V dc input levels and -5V undershoot pulses of less than 10 ns (measured at 50%).

## Switching Tests

### AC Test Loads and Waveforms




Load circuit (a) is used to test all switching characteristics except High Z parameters. Load circuit (b) is used to test High Z parameters. R1 is a resistor connected from the output to VCC and R2 is connected between the output and ground for testing purposes. Values of R1 and R2 are given in the individual datasheet for each product. Speed is measured at 1.5V reference levels except for delay to output High Z.

Document #: 38-00234-A