Am9732/Am2732

4096 x 8-Bit UV Erasable PROM

DISTINCTIVE CHARACTERISTICS

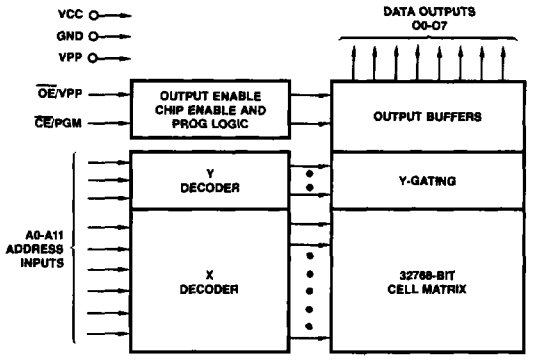
- Direct replacement for Intel 2732
- Pin compatible with Am9233 – 32K ROM
- Single +5V power supply
- Fast access time – 450ns
- Low power dissipation
  - –787mW active
  - –157mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2732 is a 32768-bit ultraviolet erasable and programmable read-only memory. It is organized as 4096 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2732 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

BLOCK DIAGRAM

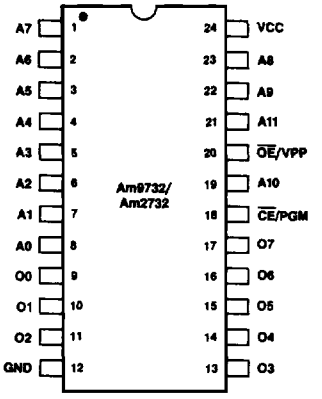


MOS-490

MODE SELECTION

Mode \ Pins	CE/PGM (18)	OE/VPP (20)	VCC (24)	Outputs (9-11, 13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	Don't Care	+5	High Z
Program	VIL	VPP	+5	DIN
Program Verify	VIL	VIL	+5	DOUT
Program Inhibit	VIH	VPP	+5	High Z

CONNECTION DIAGRAM



MOS-491

Top View

Pin 1 is marked for orientation.

A0-A11: Addresses
O0-O7: Outputs
CE/PGM: Chip Enable/Program
OE/VPP: Output Enable

ORDERING INFORMATION

Package Type	Ambient Temperature Specification	Order Number	
		450ns	550ns
Hermetic DIP Transparent Window	$0°C \leq T_A \leq +70°C$	AM2732DC	AM2732-6DC

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +125°C
Ambient Temperature Under Bias	−10 to +80°C
Voltage on All Inputs/Outputs (Except $\overline{OE}$/VPP) with Respect to GND	+6 to −0.3V
$\overline{OE}$/VPP with Respect to GND	+26.5 to −0.3V

3

READ OPERATION

DC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, VCC = +5V ±5%

Parameters	Description	Test Conditions	Min	Max	Units
ILI	Input Load Current	VIN = 5.25V		10	μA
ILO	Output Leakage Current	VOUT = 5.25V		10	μA
ICC1	VCC Current (Standby)	$\overline{CE}$ = VIH, $\overline{OE}$ = VIL		30	mA
ICC2	VCC Current (Active)	$\overline{OE}$ = $\overline{CE}$ = VIL		150	mA
VIL	Input Low Voltage		−0.1	0.8	Volts
VIH	Input High Voltage		2.0	VCC+1	Volts
VOL	Output Low Voltage	IOL = 2.1mA		0.45	Volts
VOH	Output High Voltage	IOH = −400μA	2.4		Volts

AC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, VCC = +5V ±5%

Parameters	Description	Test Conditions		Am2732 Min	Am2732 Max	Am2732-6 Min	Am2732-6 Max	Units
tACC	Address to Output Delay	Output Load: 1 TTL gate and CL = 100pF Input Rise and Fall Times: ≤20ns Input Pulse Levels: 0.8 to 2.2V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	$\overline{CE}$ = $\overline{OE}$ = VIL		450		550	ns
tCE	$\overline{CE}$ to Output Delay		$\overline{OE}$ = VIL		450		550	ns
tOE	Output Enable to Output Delay		$\overline{CE}$ = VIL		120		120	ns
tDF	Output Enable High to Output Float		$\overline{CE}$ = VIL	0	100	0	100	ns
tOH	Address to Output Hold		$\overline{CE}$ = $\overline{OE}$ = VIL	0		0		ns

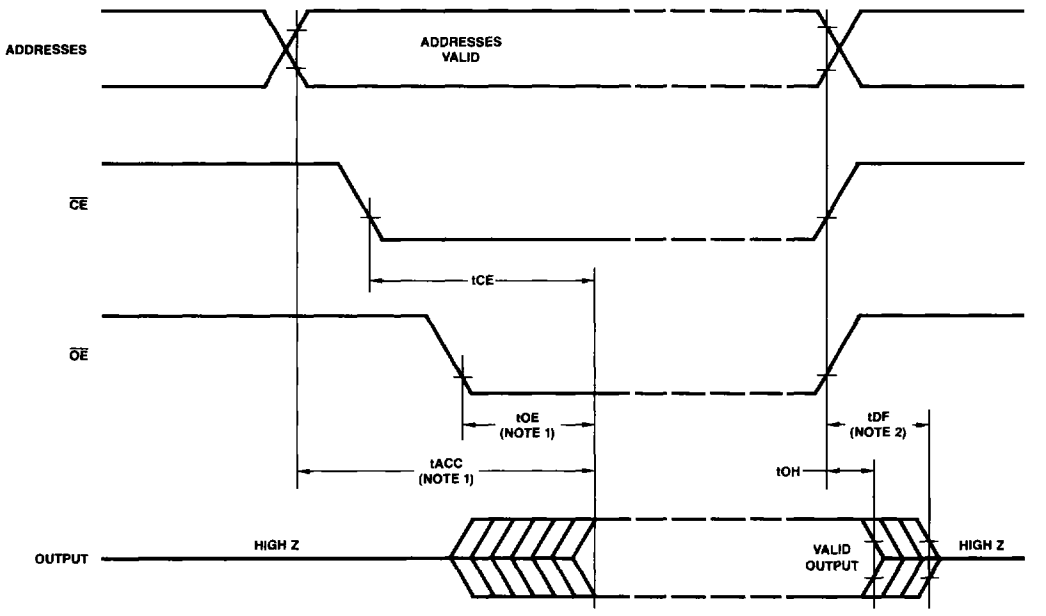
CAPACITANCE (Note 1)

T_A = +25C, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
CIN1	Input Capacitance (Except $\overline{OE}$/VPP)	VIN = 0V	4	6	pF
CIN2	$\overline{OE}$/VPP Input Capacitance	VIN = 0V		20	pF
COUT	Output Capacitance	VOUT = 0V		12	pF

Note: 1. This parameter is only sampled and is not 100% tested.

AC WAVEFORMS (Note 1)



Notes: 1. $\overline{OE}$ may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on tACC.
2. tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, VCC = 5V ±5%, VPP = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
ILI	Input Current (All Inputs)	VIN = VIL or VIH		10	μA
VOL	Output Low Voltage During Verify	IOL = 2.1mA		0.45	Volts
VOH	Output High Voltage During Verify	IOH = −400μA	2.4		Volts
ICC	VCC Supply Current			150	mA
VIL	Input Low Level (All Inputs)		−0.1	0.8	Volts
VIH	Input High Level (All Inputs Except $\overline{OE}$/VPP)		2.0	VCC+1	Volts
IPP	VPP Supply Current	$\overline{CE}$ = VIL, $\overline{OE}$ = VPP		30	mA

3

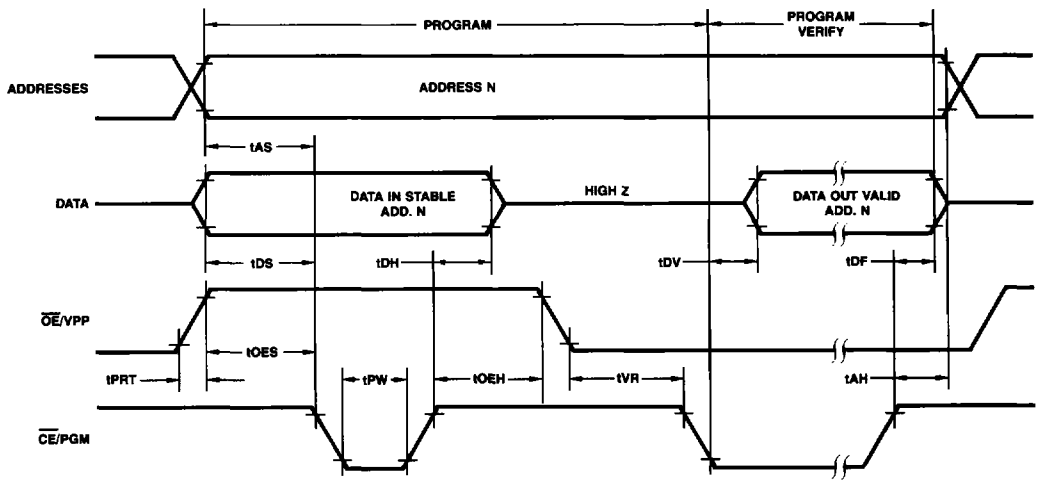
AC PROGRAMMING CHARACTERISTICS (Note 1)

T_A = +25°C ±5°C, VCC = 5V ±5%, VPP = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
tAS	Address Set-up Time	Input tR and tF (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V	2		μs
tOES	Output Enable Set-up Time		2		μs
tDS	Data Set-up Time		2		μs
tAH	Address Hold Time		0		μs
tOEH	Output Enable Hold Time		2		μs
tDH	Data Hold Time		2		μs
tDF	Chip Enable to Output Float Delay		0	120	ns
tDV	Data Valid From $\overline{CE}$ ($\overline{CE}$ = VIL, $\overline{OE}$ = VIL)		–	1	μs
tPW	Program Pulse Width		45	55	ms
tPRT	Program Pulse Rise Time		50	–	ns
tVR	VPP Recovery Time		2	–	μs

Note: 1. When programming the Am2732, a 0.1μF capacitor is required across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device.

PROGRAMMING WAVEFORMS



ERASING THE Am2732

In order to clear all locations of their programmed contents, it is necessary to expose the Am2732 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2732. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING THE Am2732

Upon delivery, or after each erasure the Am2732 has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}$/VPP pin. A 0.1μF capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

READ MODE

The Am2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs 120ns (tOE) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC − tOE.

STANDBY MODE

The Am2732 has a standby mode which reduces the active power dissipation by 80%, from 787mW to 157mW. The Am2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732s may be common. A TTL level program pulse applied to an Am2732's $\overline{CE}$/PGM input with VPP at 25V will program that Am2732. A high level $\overline{CE}$/PGM input inhibits the other Am2732 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at VIL. Data should be verified tDV after the falling edge of $\overline{CE}$.