Am1702A

256 x 8-Bit Programmable ROM

DISTINCTIVE CHARACTERISTICS

- Access times down to 550 nanoseconds
- 100% tested for programmability
- Inputs and outputs TTL compatible
- Three-state output — wired-OR capability
- Typical programming time of less than 2 minutes/device
- Clocked VGG mode for lower power dissipation

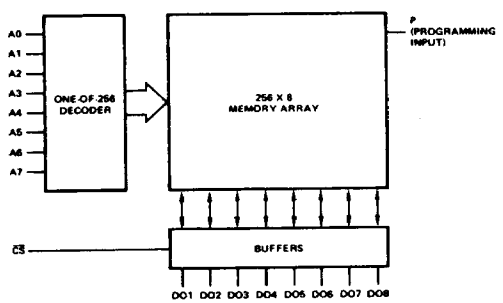
GENERAL DESCRIPTION

The Am1702A is a 2048-bit electrically programmable ultraviolet light erasable Read Only Memory. It is organized as 256 by 8 bits. It is packaged in a 24 pin dual in-line hermetic cerdip package with a foggy lid.

The transparent lid allows the user to erase any previously stored bit pattern by exposing the die to an ultraviolet (UV) light source. Initially, and after each erasure, all 2048 bits are in the zero state (output low). The data is selectively written into specified address locations by writing in ones.

A low power version, the Am1702AL, is available which permits the VGG input to be clocked for lower average power dissipation.

BLOCK DIAGRAM



BD000180

PRODUCT SELECTOR GUIDE

Access Time (ns)			Clocked VGG
1000	650	550	
Am1702A	Am1702A-2	Am1702A-1	No
Am1702AL	Am1702AL-2	Am1702AL-1	Yes
Am9702AHDL	Am9702A-2HDL	Am9702A-1HDL	No
Am90702ALHDL	Am9702AL-2HDL	Am9702AL-1HDL	Yes

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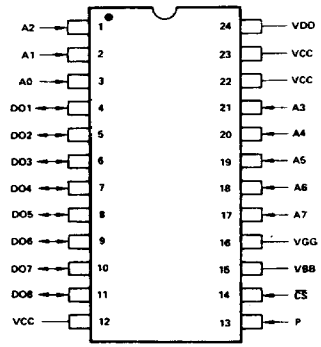
CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation

ORDERING INFORMATION

Am1702A **L-** **2** **D** **C**

- C — Temperature Range: C – Commercial (0°C to +70°C); L – Extended (–55°C to +100°C)
- D — Package: D – 24-pin CERDIP
- 2 — Speed Select: See Product Selector Guide
- L — Clocked VGG: See Product Selector Guide
- Am1702A — Device Type: 256 x 8 ROM

Valid Combinations		
		Clocked VGG
Am1702A Am1702A-2 Am1702A-1	DC, DC, DC	NO
Am1702AL Am1702AL-2 Am1702AL-1	DL, DL, DL	YES
Am9702AHDL Am9702A-2HDL Am9702AL-1HDL	DL, DL, DL	NO
Am90702AL-HDL Am90702AL-2HDL Am90702AL-1HDL	DL	YES

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PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage to the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape from the gate region, erasing the program and restoring the device to all LOW.

In order to program a specified byte, all 8 address lines must be in the binary complement of the address desired when pulsed VDD and VGG move to their negative level. The complemented address must be stable for at least tACW before VDD and VGG make their negative transitions. The voltage swing of the address lines during programming is between −47V ±1V and 0V. The addresses must then make a transition to the true state at least tATW before the program pulse is applied. For good data retention, the addresses should be programmed in sequence from 0 to 255, a minimum of 32 times. DO1 through DO8 are used as the data inputs to program the desired pattern. A low level at the data input (−47V ±1V) will program the selected bit to 1 and a high level (0V) will program it to a 0. All 8 bits addressed are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm^2 at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficient UV to erase or "soften" the PROM.)

CAUTION

Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which is harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

PROGRAMMING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI1P}	Input Current, Address and Data	$V_I = -48V$			10	mA
I_{LI2P}	Input Current, Program and V_{GG} Inputs	$V_I = -48V$			10	mA
I_{BB}	V_{BB} Current			0.05		mA
I_{DDP}	I_{DD} Current During Programming Pulse	$V_{DD} = V_{Prog} = -48V$, $V_{GG} = -35V$		200	Note 8	mA
V_{IHP}	Input HIGH Voltage				0.3	Volts
V_{IL1P}	Voltage Applied to Output to Program a HIGH		−46		−48	Volts
V_{IL2P}	Input LOW Level on Address Inputs		−40		−48	Volts
V_{IL3P}	Voltage Applied to V_{DD} and Program Inputs		−46		−48	Volts
V_{IL4P}	Voltage Applied to V_{GG} Input		−35		−40	Volts
$t_{\phi PW}$	Programming Pulse Width	$V_{GG} = -35V$, $V_{DD} = V_{Prog} = -48V$			3.0	ms
t_{DW}	Data Set-up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{GG} and V_{DD} Set-up Time		100			μs
t_{VD}	V_{GG} and V_{DD} Hold Time		10		100	μs
t_{ACW}	Address Set-up Time (Complement)		25			μs
t_{ACH}	Address Hold Time (Complement)		25			μs
t_{ATW}	Address Set-up Time (True)		10			μs
t_{ATH}	Address Hold Time (True)		10			μs
	Duty Cycle				20	%

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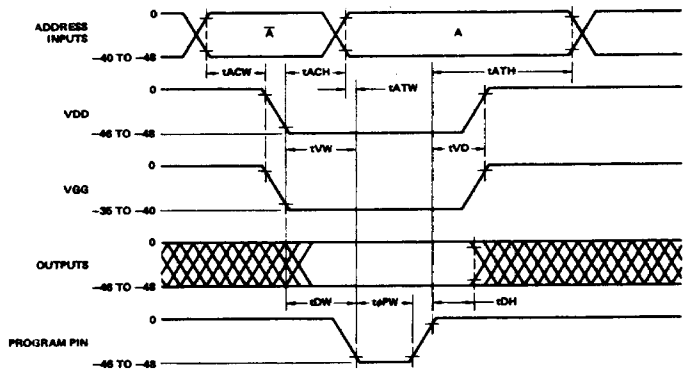
PROGRAMMING WAVEFORMS



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ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +85°C
Input and Supply Voltages
Operating ..... V_{CC} −20V to V_{CC} +0.5V
Programming ..... −50V
Power Dissipation 1.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES

Temperature
1702 Devices ..... 0°C to +70°C
9702 Devices ..... −55°C to +85°C

Supply Voltages
V_{CC}, V_{BB} ..... +4.75V to +5.25V
V_{DD}, V_{GG} ..... −8.55V to +9.45V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

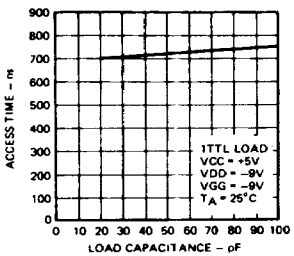
Symbol	Parameter	Test Conditions	Am1702A Am9702A Min	Typ	Max	Am1702AL Am9702AL Min	Typ	Max	Units
I_{CF1}	Output Clamp Current	T_A = 0°C, V_O = −1.0V		8	14		5.5	8	mA
I_{CF2}	Output Clamp Current	T_A = 25°C, V_O = −1.0V			13		5	7	mA
I_{DD0}	V_{DD} Current (Note 4)	V_{GG} = V_{CC}, I_{OL} = 0mA, $\overline{CS}$ = V_{CC} −2.0, T_A = 25°C					7	10	mA
I_{DD1}		I_{OL} = 0mA, $\overline{CS}$ = V_{CC} −2.0, T_A = 25°C		35	50		35	50	mA
I_{DD2}		I_{OL} = 0mA, $\overline{CS}$ = 0, T_A = 25°C		32	46		32	46	mA
I_{DD3}		I_{OL} = 0mA, $\overline{CS}$ = V_{CC} −2.0, T_A = 0°C		38	60		38	60	mA
I_{GG}	V_{GG} Current				1.0			1.0	μA
I_{LI}	Input Leakage Current	V_I = 0V			1.0			1.0	μA
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{CC} −2.0, V_O = 0V			1.0			1.0	μA
I_{OH}	Output Source Current	V_O = 0V	−2.0			−2.0			mA
I_{OL}	Output Sink Current	V_O = 0.45V	1.6	4		2.0			mA
V_{IH}	Input HIGH Level		V_{CC} −2.0		V_{CC} +0.3	V_{CC} −2.0		V_{CC} +0.3	Volts
V_{IL}	Input LOW Level		−1.0		0.65	−1.0		0.65	Volts
V_{OH}	Output HIGH Level	I_{OH} = −200μA	3.5	4.5		3.5	4.5		Volts
V_{OL}	Output LOW Level	I_{OL} 1.6mA		−3.0	0.45				Volts
		I_{OL} 2.0mA						0.4	
C_I	Input Capacitance	T_A = 25°C, All unused pins are at V_{CC}					8	15	pF
C_O	Output Capacitance						10	15	pF
C_{VGG}	V_{GG} Capacitance							30	pF

Notes:

1. During read operations VGG may be clocked high to reduce power consumption. This involves swinging VGG up to VCC. See "Clocked VGG Operation". This mode is possible only with the Am1702AL.
2. During Read operations:
   Pins 12, 13, 15, 22, 23 = +5.0V ±5%
   Pins 16, 24 = −9.0V ±5%
   During Program operations:
   t_A = 25°C
   Pins 12, 22, 23 = 0V
   Pins 13, 24 are pulsed low from 0V to −47V ±1V
   Pin 15 = +12.0V ±10%
   Pin 16 is pulsed low from 0V to −37.5V ±2.5V
3. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
4. IDD may be reduced by pulsing the VGG supply between VCC and −9V. VDD current will be directly proportional to the VGG duty cycle. The data outputs will be unaffected by address or chip select changes while VGG is at VCC. For this option specify AM1702AL.
5. VIL = 0V, VIH = 4.0V, tr = tf ≤ 50ns, Load = 1 TTL gate.
6. The output will remain valid for tOHC after the VGG pin is raised to VCC, even if address change occurs.
7. These parameters are guaranteed by design and are not 100% tested.
8. Do not allow IDD to exceed 300mA for more than 100μsec.

DC OPERATING CHARACTERISTICS

Access Time Versus Load Capacitance



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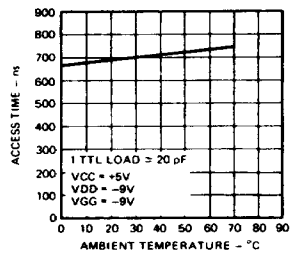
Access Time Versus Temperature



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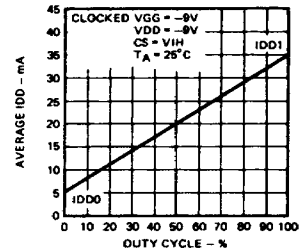
Average Current Versus Duty Cycle for Clocked VGG



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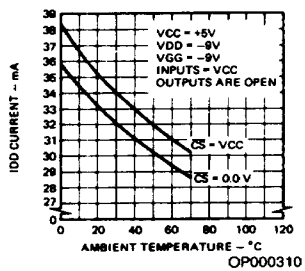
IDD Current Versus Temperature



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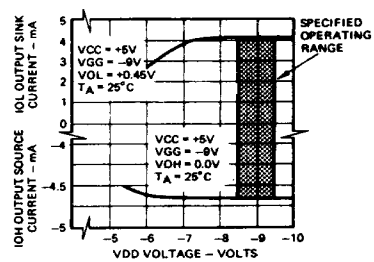
Output Current Versus VDD Supply Voltage



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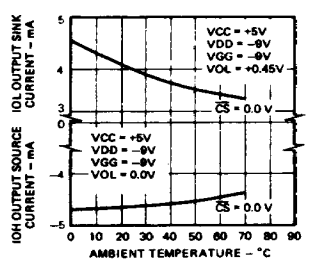
Output Current Versus Temperature



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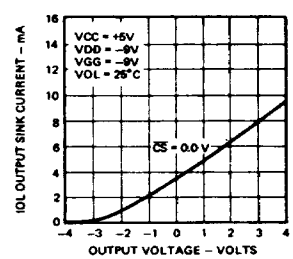
Output Sink Current Versus Output Voltage



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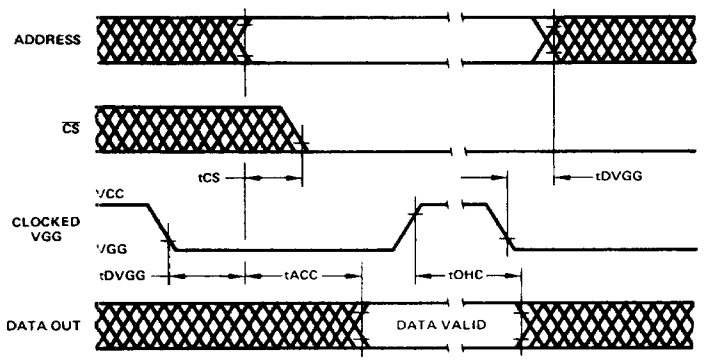
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Symbol	Description	Am1702A-1 Am1702AL-1 Am9702A-1 Am9702AL-1 Min	Am1702A-1 Am1702AL-1 Am9702A-1 Am9702AL-1 Max	Am1702A-2 Am1702AL-2 Am9702A-2 Am9702AL-2 Min	Am1702A-2 Am1702AL-2 Am9702A-2 Am9702AL-2 Max	Am1702A Am1702AL Am9702A Am9702AL Min	Am1702A Am1702AL Am9702A Am9702AL Max	Unit
1	t_{ACC}	Address to Output Access Time		550		650		1000	ns
2	t_{CO}	Output Delay from $\overline{CS}$		450		350		900	ns
3	$t_{\overline{CS}}$	Chip Select Delay		100		300		100	ns
4	t_{DVGG}	Set-up Time, V_{GG}	0.3		0.3		0.4		µs
5	t_{OD}	Output Deselect		300		300		300	ns
6	t_{DH}	Previous Read Data Valid		100		100		100	ns
7	t_{OHC}	Data Out Valid from V_{GG} (Note 6)		5.0		5.0		5.0	µs
8	freq.	Repetition Rate		1.8		1.6		1.0	MHz

SWITCHING WAVEFORMS

READ OPERATION (Note 2)



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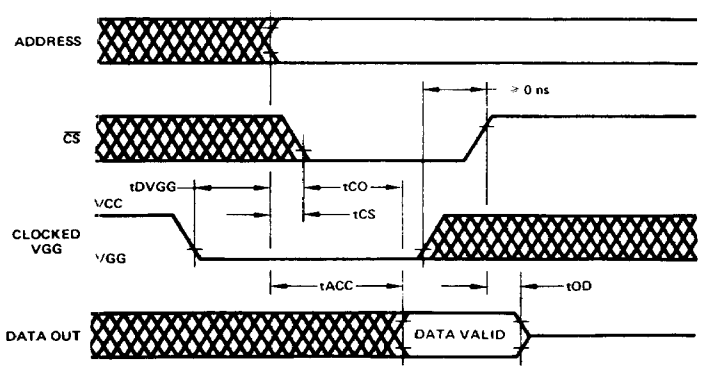
DESELECTION



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Note 1: CLOCKED VGG OPERATION

The VGG input may be clocked between +5V (VCC) and −9V to save power. To read the data, the chip select ($\overline{CS}$) must be low ($\leq$ VIL) and the VGG level must be lowered to −9V at least tDVGG prior to the address selection. Once the data has appeared at the output and the access time has elapsed, VGG may be raised to +5V. The data output will remain stable for tOHC. To deselect the chip, $\overline{CS}$ is raised to $\geq$ VIH, and the output will go the high impedance state after tOD. The chip will be deselected when $\overline{CS}$ is raised to VIH whether the VGG is at +5V or at −9V.

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