TECHNICAL MANUAL

MODEL: ACT-I

REVISION C

ACT-I (REV. C) TECHNICAL MANUAL FOR SERIAL #'s 950-1400

TABLE OF CONTENTS

(continued)

SECTION I: GENERAL OVERVIEW OF THE ACT-I TERMINAL

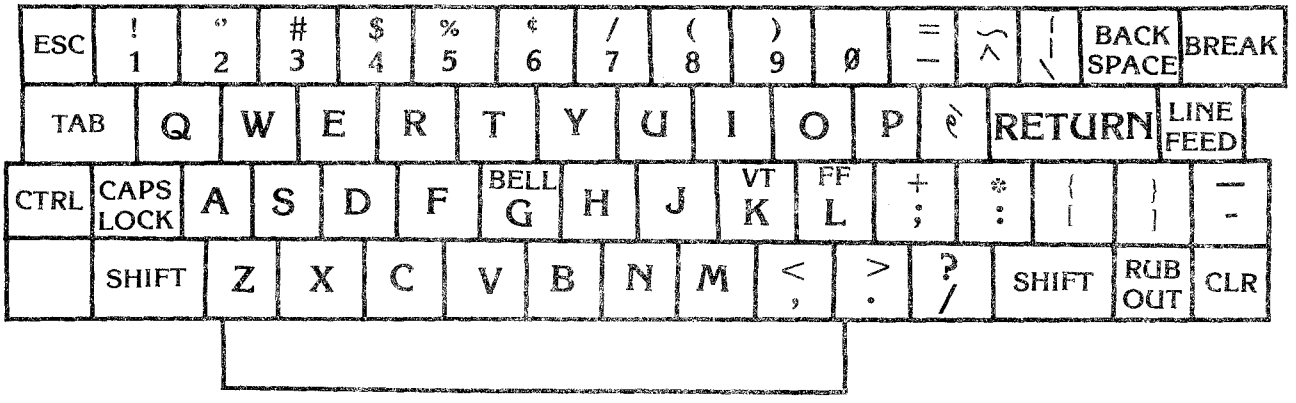
The ACT-I video terminal is divided into seven major sections:

1) Keyboard
2) Power Supply
3) I/O Section
4) Memory
5) Memory Loading
6) Oscillators and Control
7) Video Generator

Of these sections, the first two will be described here, while the latter five sections are briefly described here, but have detailed descriptions in Sections III, IV, V, VI and VII of this manual. The following summary description of the ACT-I can be better understood by referring to the block diagram in Figure I-1.

The keyboard module generates a 7 level ASCII code for the key depressed as illustrated in the following figure, and it also generates a strobe signal to indicate that a key has been depressed. Debouncing is also done in this module. A separate line is used in the ACT-I for the clear function. This is sent from the keyboard as a switch closure to ground when the CLEAR key is depressed. Depressing the BREAK key forces the ACT-I serial out to the logical 0 (space) state.

LEGEND FORMAT



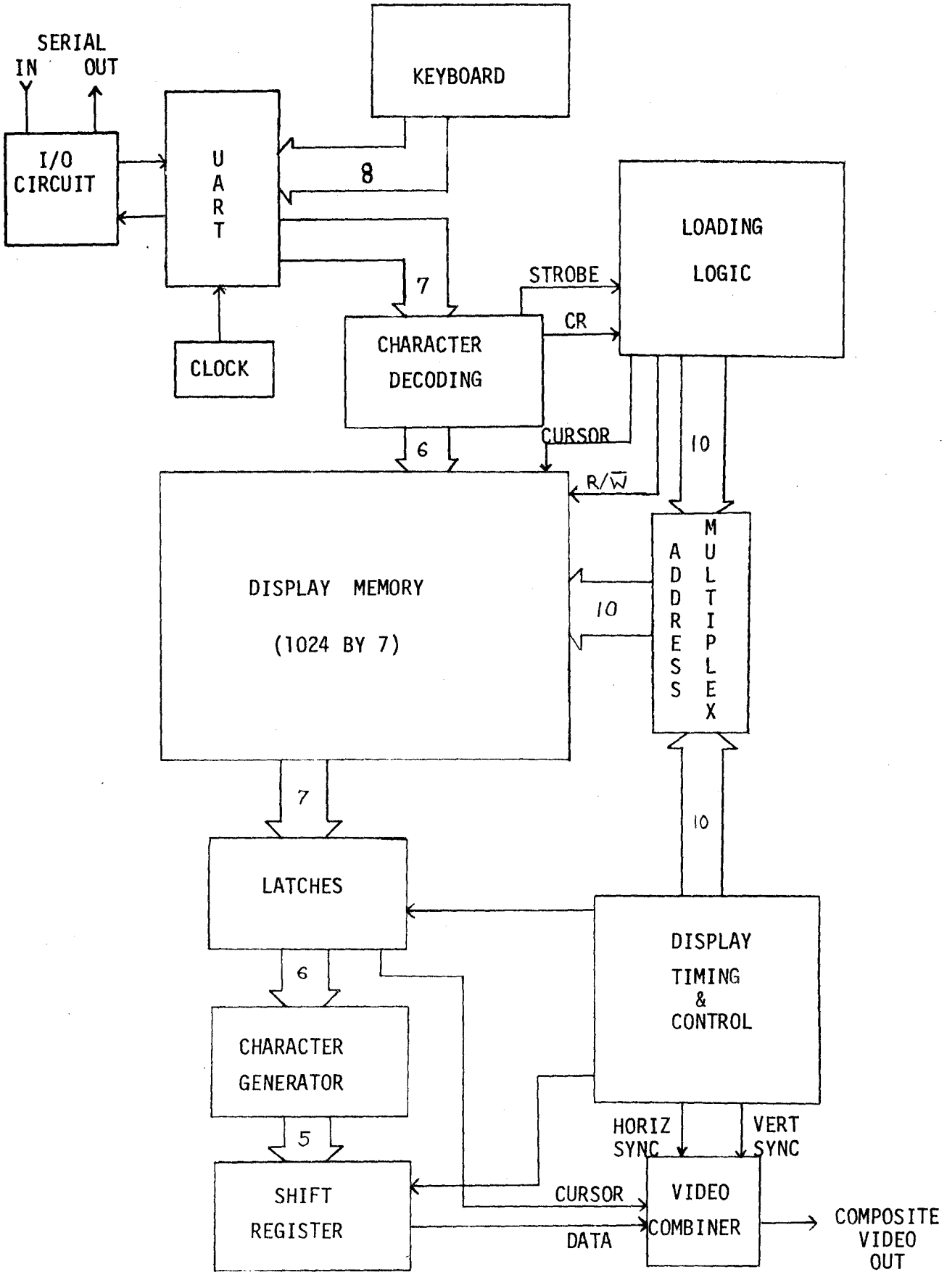
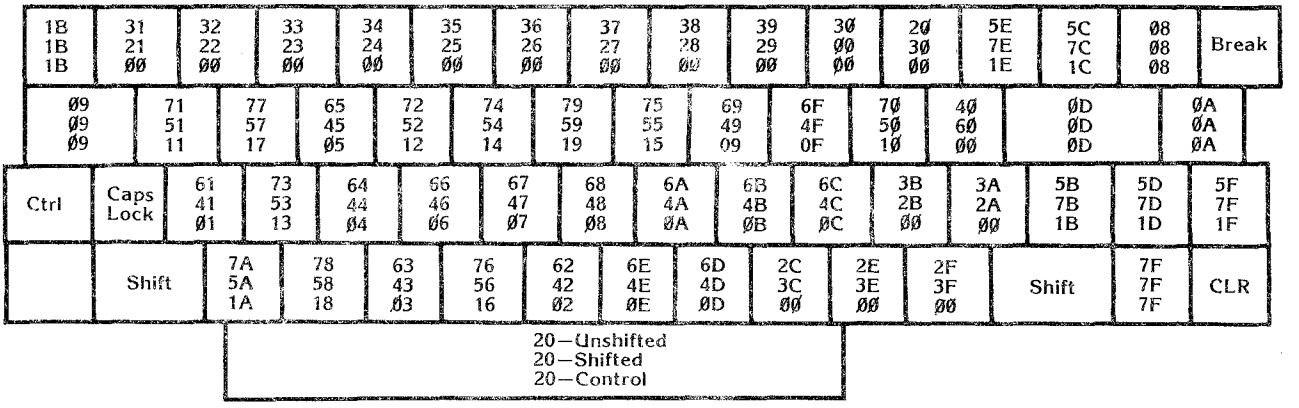


FIGURE I-1: ACT-I BLOCK DIAGRAM

OUTPUT



The keyboard is connected to the ACT-I main circuit board by a ribbon connector (J1), which carries the 7 data bits, the "Key Pressed" signal, the "Page" and "Break" key closures, and +5v, -12v and ground. The keyboard schematic is contained in Section IX. J1 also carries serial data and ground between the jacks on the rear of the cabinet and the circuit board.

The power supply generates +5v, -12v, and ground from 115vac. The supply is fused with a 1/2 amp fuse, and is switched on by the main power switch located on the top of the case. The transformer is mounted to the bottom of the case, and it provides 24 volts center tapped at 12v with a current rating of 1 amp at 50-60 Hz.

The +5v supply yields about 800MA to drive the ACT-I and the keyboard, while the -12v supply is very lightly loaded, at around 20MA.

The I/O section is responsible for performing all the operations needed to interface RS232C or 20MA current loop serial ACT-I. The serial format used is 8 bit ASCII (with the MSB - Most Significant Bit - jumper selectable by the user) start bit and 2 stop bits. The I/O section receives characters to transmit from the keyboard, and passes received characters to the memory loader section.

The memory loader section of the ACT-I carries out the functions of loading incoming characters into the display memory, translating special characters, and ignoring undisplayable characters, executing carriage return, performing scroll, and executing the screen clear ("Page") operation. It receives characters from

the I/O section, and passes them to the video display generation section via the display memory.

The oscillators and control section (described in Section VI) generates all timing and synchronization signals which clock the other circuits. Signals generated by the oscillators and control section include horizontal and vertical sync pulses for use by the video combiner and several other pulse trains used for internal synchronization.

The video generator section (Section VII) generates the dot sequence required to display the contents of the display memory on a video monitor. It also keeps track of line, row and column counts to determine the address of the characters as they are displayed as well as blanking the video during non-display intervals to avoid displaying extraneous dots or characters. The video section also generates the cursor display.

Section VIII contains troubleshooting procedures for determining the faulty circuit of a malfunctioning ACT-I. Included in this section is a list of reported trouble symptoms and their remedies.

All pertinent technical information is presented in the tables and lists in Section IX.

Section X contains the schematic diagram of the ACT-I. The diagram is partitioned into sections which correspond to the circuit descriptions of Sections III through VII.

MICRO-TERM MODEL ACT-I

OPERATING INSTRUCTIONS 3-76

1. Your unit has been factory set for:

   a) DATA RATE (baud) [ ] 110 [X] 300 [ ] 600

   b) RECEIVER MARK [ ] high [X] low

   c) TRANSMITTER MARK [ ] high [X] low

   d) LOGIC LEVELS [X] RS232C (-12V, +5V) [ ] TTL/CURRENT

   e) 8TH BIT [X] high [ ] low [ ] parity even [ ] parity odd

   If any of the above specifications do not match your processor's serial interface, refer to section 4 to accommodate the ACT-I to your processor.

2. PRELIMINARY CHECK-OUT

   a) Connect the video output of the ACT-I to the low impedance (75 ohm) input of a high quality monitor (5 Mhz band pass) which will accept a standard composite video signal. We recommend the use of a high bandwidth monitor such as the units offered by MICRO-TERM so that each dot in the 5 x 7 character matrix can be resolved, lending to a sharp, unambiguous character display. Modified television sets will, in general, display characters which appear slightly smeared in the horizontal direction resulting in a display which may be somewhat more tiring to view, particularly over an extended period of time.

   b) If your unit has the same receiver and transmitter polarity (i.e., both mark high or both mark low), then your ACT-I can be self-tested by connecting the serial OUT data from the transmitter directly to the serial IN jack of the receiver. This may be accomplished by electrically connecting the center, "tip", conductor of two phone plugs together with a short length of wire and inserting the plugs into the serial OUT and IN jacks at the rear of the cabinet.

c) Activate the ACT-I to 110 VAC 60Hz and flip the power switch. The switch should illuminate but the monitor screen should remain clear since the ACT-I automatically enters a "clear screen" mode upon power-up. Now depress any key corresponding to a displayable character. The appropriate character should appear on the screen at the lower left hand corner and an underline cursor will appear at the position for the next character. Adjust the monitor brightness and contrast for comfortable viewing.

d) The display line should fill horizontally to the right as data is entered from the keyboard. When the 64th character has been entered on a line, the cursor will disappear to its home (lower left corner) position and the entire display will move up one line (i.e., scroll). This same operation, cursor home and scroll is initiated by receipt of the RETURN key code. Note that receipt of the RETURN code initiates the functional equivalent of the operations associated with RETURN and LINEFEED and that LINE FEED codes are ignored. Automatic scrolling when a line fills allows the ACT-I to be used with software which may use a greater than 64 character format without data loss or overwrite. The invisible cursor home position protects the CRT from phosphor burn caused by long term, concentrated illumination often associated with the most common cursor position.

e) Each time the ACT-I scrolls, the top, 'oldest', line of the 16 lines of display will disappear from the top of the screen. The entire screen may be cleared at any time by depressing the 'CLEAR' key. The 'CLEAR' key operates on the ACT-I display only; no serial code is sent when this key is depressed.

f) The ACT-I keyboard comes set up to operate as an upper case only keyboard; i.e., the upper case code for all alphabetic characters (A-Z) is transmitted when the appropriate key is depressed whether or not the shift key is simultaneously depressed. This is by far the most commonly used mode of

operation. However, if it is necessary to transmit lower case alphabetic characters, refer to the modification, Sec. 4.7.

3. PROCESSOR HOOKUP

a) Two connections are required between the ACT-I and processor, modem, etc.: serial out and serial in. Both of these connections are made via phone plugs to be inserted in the appropriate socket at the rear of the ACT-I. For each phone plug, the center, "tip", conductor must be connected to the "hot" or signal line going into or out of the processor. The signal reference (ground) in each case is the shank conductor. Since the serial in and serial out lines are isolated, the ACT-I operates in full duplex; it can receive and transmit simultaneously. If you are using the current loop interface please refer to 4.1b)-3). Once the phone plugs have been properly connected to the processor serial in and serial out lines and the plugs have been inserted in their appropriate sockets at the rear of the ACT-I, all interconnections are complete.

b) Now bring up your operating system, create a simple program to echo characters or otherwise verify that your processor and the ACT-I are communicating properly. At this point you should be able to put away the instruction manual and enjoy the use of your ACT-I.

4. CHANGING THE ACT-I INTERFACE

a) If you should need to change the ACT-I interface from the factory specifications presented in section 1, you will need a small soldering iron, some small gauge hookup wire, and rosin core solder. Unplug the ACT-I. Remove 6 Phillips screws from the bottom of the cabinet. Carefully separate the cabinet halves by "hinging" the cabinet top at the back. Do not allow excessive strain on the cables at the rear of the cabinet.

4.1. LOGIC LEVELS

a) To change the logic levels from RS232C (-12V + 5 volts) to TTL/current loop (o, +5 volts @ 20ma) or vice versa, locate the word 'OUT' next to a solder pad on the printed circuit board in the upper left hand corner. The jumper from the pad must connect to one of the three nearest pads labeled RS232C, LOOP N or (LOOP) P. For TTL levels connect the jumper to LOOP P. For RS232C compatible levels connect the jumper to the pad labeled RS232C. With the LOOP P pad selected and the output polarity unchanged from the factory setting (O to -, R to +), a logical "1" will be transmitted as 0 volts and a logical 0 as +5 volts. To invert the polarity refer to Sec. 4.2. If this completes your logic level modification, go to section 4.1f).

b) For 20ma current loop applications the logic level jumper described in the previous paragraph must be connected to the LOOP N solder pad if the ACT-I transmitter is to supply the current in the loop to your processor or to the (LOOP) P pad if your processor supplies the loop current and the ACT-I is to sink it. It is important that this information be positively determined so that the proper connection can be made. An erroneous connection may cause the two current sources to fight each other and although the output of the ACT-I is fully protected, your processor interface may be harmed. It is also important to note that both the serial out and serial in lines have a common ground. If your interface has its own 20ma current source which requires an isolated return it should not be used. And finally the voltage level of the current loop sourced by your processor should not exceed +12 volts or be negative relative to ground. If your current loop source does not meet these requirements, then the ACT-I current source should be used instead. The following paragraph illustrates the proper connections to a typical

plug into the serial IN jack at the rear of your ACT-I. This 'loop' should not require polarity verification.

e) Power up your processor and ACT-I. Have your processor send some known character string out to the ACT-I. The ACT-I should display properly. Now attempt to prompt your processor from the keyboard of the ACT-I or have your processor echo back the data sent from the ACT-I. If the expected responses are envoked then the proper polarity is being transmitted from the ACT-I and the current loop connections are complete. Otherwise the output polarity of the ACT-I must be changed. See 4.2.

f) Upon completion of the logic level modification, carefully reassemble the ACT-I and mark the new specifications in section 1 for future reference. Do not attempt to reassemble the cabinet with the power connected.

4.2. POLARITY

a) Refer to 4.a) before opening the ACT-I cabinet. On the main printed circuit board in the upper center there is a dual operational amplifier in an eight pin package marked CA1458. In the immediate vicinity there are two groups of holes labeled +, 0, -, R to the right and -, +, R, I below. The first group determines the output polarity and the second group determines the input polarity. In each group the + and - holes must be connected to the other two holes. NEVER connect the + hole to the - hole or make any other connections than those indicated in the following table.

RS232

DATA	INPUT	JUMPER	OUTPUT	JUMPER
Mark-low	<2v	- to I, + to R	-12v	- to 0, + to R
Space-high	>2v		+5v	
Mark-high	>2v	- to R, + to I	+5v	- to R, + to 0
Space-low	<2v		-12v	

LOOP P

DATA	INPUT	OUTPUT	JUMPER
Mark-low	Input specifications are same as for RS232	(loop closed) 0v	- to R, + to 0
Space-high		(loop open) +5v	
Mark-high	Input specifications are same as for RS232	(loop open) +5v	- to 0, + to R
Space-high		(loop closed) 0v	

LOOP P can be used to sink current to ground. Polarity of the current source must be positive relative to ground and the voltage level must not exceed 12 volts.

LOOP N

DATA	INPUT	OUTPUT	JUMPER
Mark-low	Input specifications are same as for RS232	0 ma	- to R, + to 0
Space-high		20 ma	
Mark-high	Input specifications are same as for RS232	20 ma	- to), + to R
Space-low		0 ma	

In loop N the output current is sourced by the ACT-I.

When the polarity modifications are complete, carefully reassemble the ACT-I and mark the new specifications in section 1 for future reference. Do not attempt to reassemble the cabinet with the ACT-I plugged in.

4.3. DATA RATE SELECTION

a) Before opening the cabinet refer to 4.a). At the upper left of the main printed circuit board is a semicircle of solder pads and the words "BAUD RATE SELECT". To change the ACT-I baud rate, the jumper which is connected from the pad at the center of the semicircle to one

of the labeled pads "110, 300, 600, 1200, 2400, 4800, 9600" must be cut and jumper should be soldered from the center to the appropriately labeled pad. Carefully reassemble your unit and note the new specification in section 1 for future reference. Be sure that your processor's serial interface is set to operate at the new data rate.

4.4a) UART OPTIONS

Your ACT-I transmits a start bit followed by either 5, 6, 7 or 8 ASCII data bits depending on the setting of the word select beits, an odd or even parity bit (if parity is enabled) and then either one or two stop bits. All of these options have default values as follows:

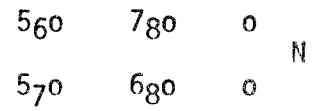
DEFAULT UART OPTIONS

# OF DATA BITS	8
8TH BIT	LOGICAL 1 (HIGH)
PARITY	INHIBITED
# OF STOP BITS	2

4.4b) CHANGING THE UART OPTIONS

Should you desire to change any of the default options locate the appropriate directions below. Note that the default values are enabled by narrow "runs" on the printed circuit board. These connections must be broken before adding the necessary jumpers. If these are not cut and a jumper is inserted the +5 volt supply will be shorted to ground and the ACT-I will not function until the run is cut.

1) # OF DATA BITS - To change the number of data bits locate the pads immediately to the left of the UART chip (the only 40 pin IC on the ACT-I board) which are arranged as per the following sketch:



To change to 7 data bits break the lower connection between N and the pad marked 6_8 and connect the lower N pad to the pad marked 5_7.

To change to 6 data bits break the upper run between N and the 7_8 pad and connect the upper N pad to the 5_6 pad.

To change to 5 data bits break both of the default runs between the N pads and the 7_8 and 6_8 pads and connect the upper N pad to the 5_6 pad and the lower N pad to the 5_7 pad.

2) 8TH BIT - To change the 8th bit from a logical 1 (high level) to a low, cut the run between the B8 pad and the 1 pad and solder a jumper from B8 to 0. These pads are located to the left of the UART chip also.

4.5. PARITY

a) Your ACT-I can be modified to transmit a parity bit in addition to the 8 other bits. To select this option, locate the solder pad marked "PI", parity inhibit near the upper left corner of the circuit board. The jumper wire must connect this pad to the pad marked "$\overline{I}$" to enable the parity computation circuitry. Then to select either odd or even parity, the pad labeled "O/E" must be jumpered to either the "O" pad for odd parity or the "E" pad for even parity. Your ACT-I will now transmit an additional parity bit in the serial input data stream which is even or odd as you have selected.

NOTE: When parity is enabled the parity bit is transmitted immediately following the data bits. Hence if you desire to have your ACT-I send and receive one stop bit, seven ASCII data bits, a parity bit and finally, the stop bits, you will have to change the number of data bits from 8 to 7 (See Sec. 4.4b)1.)

4.6. STOP BITS

a) Your ACT-I can transmit and receive 1 or 2 stop bits. This option is selected by connecting the jumper from the pad marked "SB" to either pad marked "1" or "2" immediately to the left. After making any modifications to your ACT-I, carefully reassemble the cabinet while the line cord is disconnected and mark the new specifications in section 1.

4.7. LOWER CASE TRANSMISSION

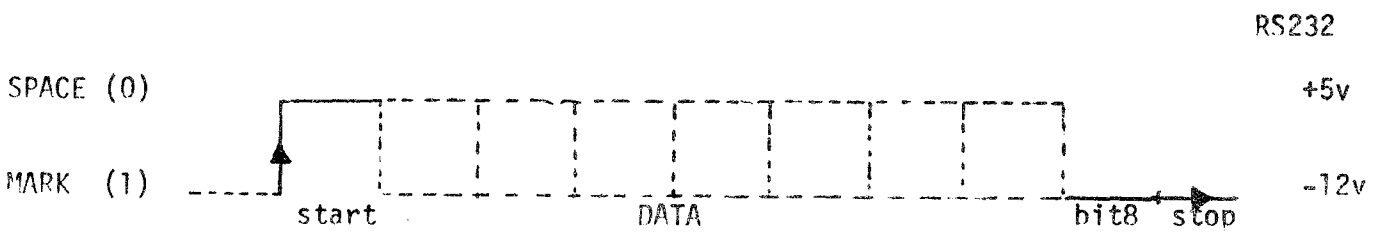
Your ACT-I keyboard can be enabled to transmit lower case alphabetic characters by clipping out the short blue wire which is soldered across the caps lock key. To gain access to the blue wire, unplug the ACT-I and carefully separate the cabinet halves as previously described. The blue jumper wire will be apparent on the back of the printed circuit board to which the keys are attached. The ACT-I will still transmit in an upper case only mode whenever the 'CAPS LOCK' switch is engaged.

5. WARRANTY AND SERVICE

a) The ACT-I requires no maintenance and should perform faithfully for many years. MICRO-TERM will repair any unit which fails within the original warranty period provided that no modifications have been performed on the circuit, other than the jumper modifications outlined in this manual.

b) Beyond the warranty period MICRO-TERM will charge a nominal fee for the repair of any ACT-I. A complete technical manual including schematic, theory of operation and timing diagrams is available to owners of the ACT-I for five dollars. Any further information relating to the operation or interfacing of your ACT-I can be obtained by writing directly to TECHNICAL STAFF, MICRO-TERM, INC.

HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR
00	NUL	20	SP	40	@	60	`
01	SOH	21	!	41	A	61	a
02	STX	22	"	42	B	62	b
03	ETX	23	#	43	C	63	c
04	EOT	24	$	44	D	64	d
05	ENQ	25	%	45	E	65	e
06	ACK	26	&	46	F	66	f
07	BEL	27	'	47	G	67	g
08	BS	28	(	48	H	68	h
09	HT	29	)	49	I	69	i
0A	LF	2A	*	4A	J	6A	j
0B	VT	2B	+	4B	K	6B	k
0C	FF	2C	,	4C	L	6C	l
0D	CR	2D	–	4D	M	6D	m
0E	SO	2E	.	4E	N	6E	n
0F	SI	2F	/	4F	0	6F	o
10	DLE	30	0	50	P	70	p
11	DC1	31	1	51	Q	71	q
12	DC2	32	2	52	R	72	r
13	DC3	33	3	53	S	73	s
14	DC4	34	4	54	T	74	t
15	NAK	35	5	55	U	75	u
16	SYN	36	6	56	V	76	v
17	ETB	37	7	57	W	77	w
18	CAN	38	8	58	X	78	x
19	EM	39	9	59	Y	79	y
1A	SUB	3A	:	5A	Z	7A	z
1B	ESC	3B	;	5B	[	7B	{
1C	FS	3C	<	5C	\	7C	|
1D	GS	3D	=	5D	]	7D	}
1E	RS	3E	>	5E	^	7E	~
1F	VS	3F	?	5F	←	7F	DEL



SECTION III: I/O:

The I/O circuitry of the ACT-I terminal is responsible for the translation between parallel ASCII format and RS-232C or 20MA current loop serial ASCII format. For your convenience a table of the ASCII codes is included in section IX.

The I/O section is also responsible for the generation of the strobe signal to activate the loading section of the terminal upon receipt of a character on the serial in line. The ACT-I operates in full-duplex mode.

Line driving for the serial out line is accomplished by OP10 (for RS232C), or either the MPS5172 transistor ("Loop P"), or the MPS3638 transistor ("Loop N"). OP1I performs the input interfacing. The serial input jack is fed to the "I" pad near OP1 on the board. This pin is jumpered to either the "+" or "-" pads on the board nearby. The "R" pin provides a reference voltage from a 22K/12K voltage divider across the +5v supply, giving a 1.5v reference level. This "R" pin is jumpered to the "+" or "-" pad, whichever is not connected to "I". The default connections are for "I" to be connected to "-", and for "R" to be connected to "+". This is standard for an RS232C interface. The "+" and "-" pads on the board are connected to the + and - inputs of OP1I, which functions as a comparator to detect the "Mark" and "Space" states of the input line. OP1I's output is connected through a 12K resistor to pin 20 of UART U1, the serial input pin. This line is also tied to D4, which prevents the line from excursions below ground to the OP amp negative supply voltage, so that pin 20 of U1 sees a TTL signal (the positive supply to OP1 is =5v, so the positive excursion of the signal is about 5v).

The serial output starts at pin 25 of the UART, its serial out pin, and runs to the pad marked "O" on the board. This pad is jumpered to either the "+" or "-" pads near it, depending on the polarity of the output signal needed. Default

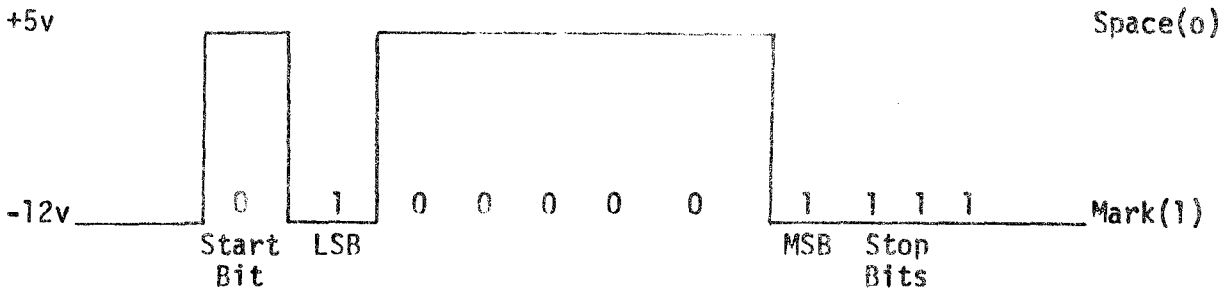
is "-". The other polarity pin should be jumpered to the nearby "R" pad, which is the same 1.5v reference signal used by the serial input detector. Default is for "R" to be jumpered to "+". The "+" and "-" pads feed into the + and - inputs of OP10, which produces at its output (pin 7) an RS232C signal with the high state at about +5v, and the low state at about -12v. This signal appears at the pad labeled "RS232C" on the power supply board, and the serial output jack is connected to it as a default. The "Break" key is connected through a 5.6k resistor to the pad marked "0". When the "Break" key is depressed it pulls pad "0" low and forces the output of OP10 to the logical 0 (space) state (+5v).

The RS232C signal drives transistors Q_N and Qp to generate 20ma current loop outputs. Q_N is capable of sourcing 20ma of current into a load which has its common side at ground potential. D3 insures that OP10's positive output can cut-off Q_N. Q_N sources current (mark state) when the RS232C signal is low (mark state), so no polarity inversion at OP10 is needed when the "Loop N" output is selected. Qp is capable of sinking current (mark state) to ground when the RS232C signal is high (space state). Hence, when the "Loop P" output is selected, OP10 should have its "+" input jumpered to the "0" pad and its "-" input jumpered to the "R" pad.

The UART (Universal Asynchronous Receiver/Transmitter), U1, performs all parallel/serial and serial/parallel conversions. The UART requires a frequency reference of 16 times the desired baud rate. This is supplied by the UART clock divide down chain -- C11 and C76, which is driven by a 1.228MHz clock from C9 in the oscillator and control circuit. Baud rate selection is made by connecting a jumper from U1p17,40 to the desired clock rate signal. For instructions on how to change the data rate refer to Section II-4.3 of this manual.

The transmit section of the UART takes the data from the keyboard when "STROBE" occurs at pin 23. This data is latched in from pins 26 through 33, and is converted to serial format and clocked out the serial output pin (pin 25). Pin 33, the MSB

of data, is not supplied from the keyboard, but is set by the "8th Bit" jumper, which connects U1 pin 33 to either +5v or ground. Default is to tie the 8th bit high. If a zero 8th bit is desired, jumper pin 33 to ground. The following figure shows the ACT-I serial out waveform that should appear at the serial out jack for transmitting the letter A (ASCII code = 1000001) in RS232C format.



The receiver section of the UART is responsible for detecting incoming characters on the serial input line to the ACT-I and passing them to the loader section. The UART waits for a start bit on the serial input (pin 20), and when it gets one, it assembles an 8 bit character, and looks for a stop bit. When the stop bit is detected, the UART raises a flag signal at pin 19 to indicate that it has a character ready. This signal triggers the start of the loading sequence as described in the memory loading section.

SECTION IV: MEMORY

The ACT-I internal refresh memory is organized as 1024 seven-bit words (characters). There are six bits of ASCII data and a cursor bit. The ASCII data is stored in M1 (Least Significant Bit) through M6 (Most Significant Bit). The cursor bit is stored in M7.

When in the display mode, (no characters being loaded) the ten memory address lines (AØ through A9) are driven by the display address lines (DAØ through DA9) by virtue of the multiplex control line (D/$\overline{W}$) at S1 through S3p1 being high to select the display address lines. The data in lines at M1 through M5p11 and M7p11 are held low and M6p11 is held high to force the ASCII space code and a low cursor bit on the input data lines (DI1 through DI7). The data output lines DO1 through DO7 drive the latches in the video generator circuit (Section VII).

When in the load mode M1 through M7p3 (Read/$\overline{\text{Write}}$-"R/$\overline{W}$") and the multiplex control line at S1-S3p1 (Display/$\overline{\text{Write}}$-"D/$\overline{W}$") is pulsed low to allow the load address lines (LAØ through LA9) to address the memory. When loading characters into memory, the data in lines, DI1 through DI6 (M1-M6p11), have the ASCII data and M7p11 (cursor bit in) is held high.

For a detailed description of memory loading refer to Section V of this manual.

SECTION V: MEMORY LOADING

This section describes:

1) Character identification

2) Loading of displayable characters to memory

3) Carriage Return (CR) processing

4) Auto clear and PAGE function

The following components are responsible for performing the above three functions:

A3, N7, MTI5, FF3, N10, N5, C4, C5, C6, OS1 and M1-M7.

V-I: CHARACTER IDENTIFICATION

Character processing is initiated when the UART flag (U1p19) which is applied to OS1bp2 goes high to indicate receiption of a character*. On the next horizontal retrace pulse $\overline{HOR}$ goes low and OS1a is triggered and $\overline{Q}$ pin 12 goes low for 2us and is applied to OS1bp1. Since OS1bp2 is high, OS1b fires and OS1bp4 goes low for 2us pulls MTI5p15 low, and resets the UART flag by pulling U1p18 low. The most significant 5 bits (5 MSB's) of the ASCII character code are tied to pins 10 through 14 of MTI5 and the 2 LSB's (Least Significant Bits) are tied to A3p1 and A3p6. MTI5 decodes the 5 MSB's to detect if the character is a displayable or control character.

V-2: DISPLAYABLE CHARACTER PROCESSING

If the received character is displayable MTI5 produces a $\overline{STROBE}$ pulse at pin 6 for the duration of OS1b's pulse (2us). ASCII data for the character is available during the same 2us interval as follows:

BIT #
1(LSB) at A3p3 and M1p11
2 at A3p4 and M2p11
3 at MTI5p4 and M3p11

*Please refer to Figure V-1.

4 at MTI5p3 and M4p11
5 at MTI5p2 and M5p11
6 at MTI5p1 and M6p11

When a lower case alphabetic character code is received MTI5 and A3 produce the corresponding upper case code. The ASCII code set is given in Section IX of this manual.

Since N5p9 is high N5p10 goes high when $\overline{\text{STROBE}}$ falls (MTI5p6). The high level from N5p10 is applied to pin 1 of S1, S2 and S3 (the select line of the multiplexers for the 10 address lines to M1 through M7). This causes the three switches S1, S2 and S3 to allow C4 and C6 to address the memory. C4 holds the 4 bit address of the row that is presently being loaded (LA6 - LA9). C6 has the 6 bit address of the column into which the present character is to be loaded (LA$\emptyset$ - LA5).

The rising edge of N5p10 is capacitively coupled into N5p12, 13. The capacitive coupling causes a 1.5us R/$\overline{\text{W}}$ (read/$\overline{\text{write}}$) pulse at N5p11 which drives the R/$\overline{\text{W}}$ lines (p3) of M1 through M7. Hence the character is loaded into memory 1.5us after the UART flag and $\overline{\text{HOR}}$ coincide at OS1b.

The rising edge of $\overline{\text{STROBE}}$ (MTI5p6) causes a falling edge at N5p10, C6p1 and S1, S2 and S3p1. This falling edge increments C6 and returns control of the RAM address lines to the display circuitry.

Whenever a displayable character is loaded C6p3(Q6) is low and hence M7p11 (cursor bit into memory) is high and a 1 is loaded into the cursor bit for the position which is being filled.

When a character is loaded into the 64th column a scroll operation is initiated by virtue of C6p3(Q6) going high. The scroll operation is described in Section V-4.

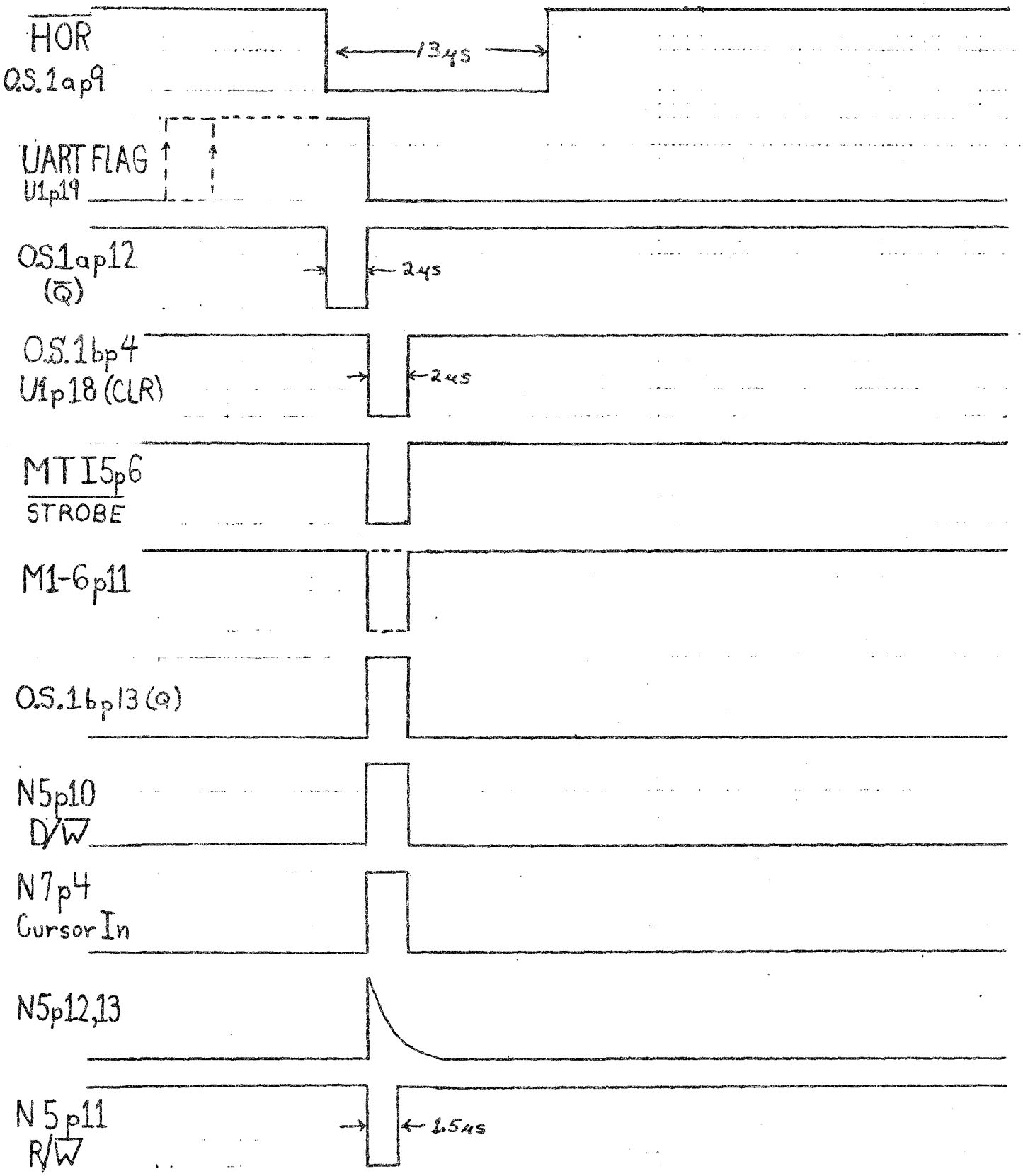


FIG. V-I: Timing Diagram For Character Loading (not 64th Char.)

V-3: CR PROCESSING

When A CR (Code OD Hex) is received by the UART MT15 produces a 2usec low pulse at pin 7 ($\overline{CR}$) which is inverted and applied to FF3ap6 (set input of CR FF). Please refer to Fig. V-2. When the $\overline{CR}$ line falls the CR FF is set and FF3ap2 ($\overline{Q}$) falls -- initiating the CR process.

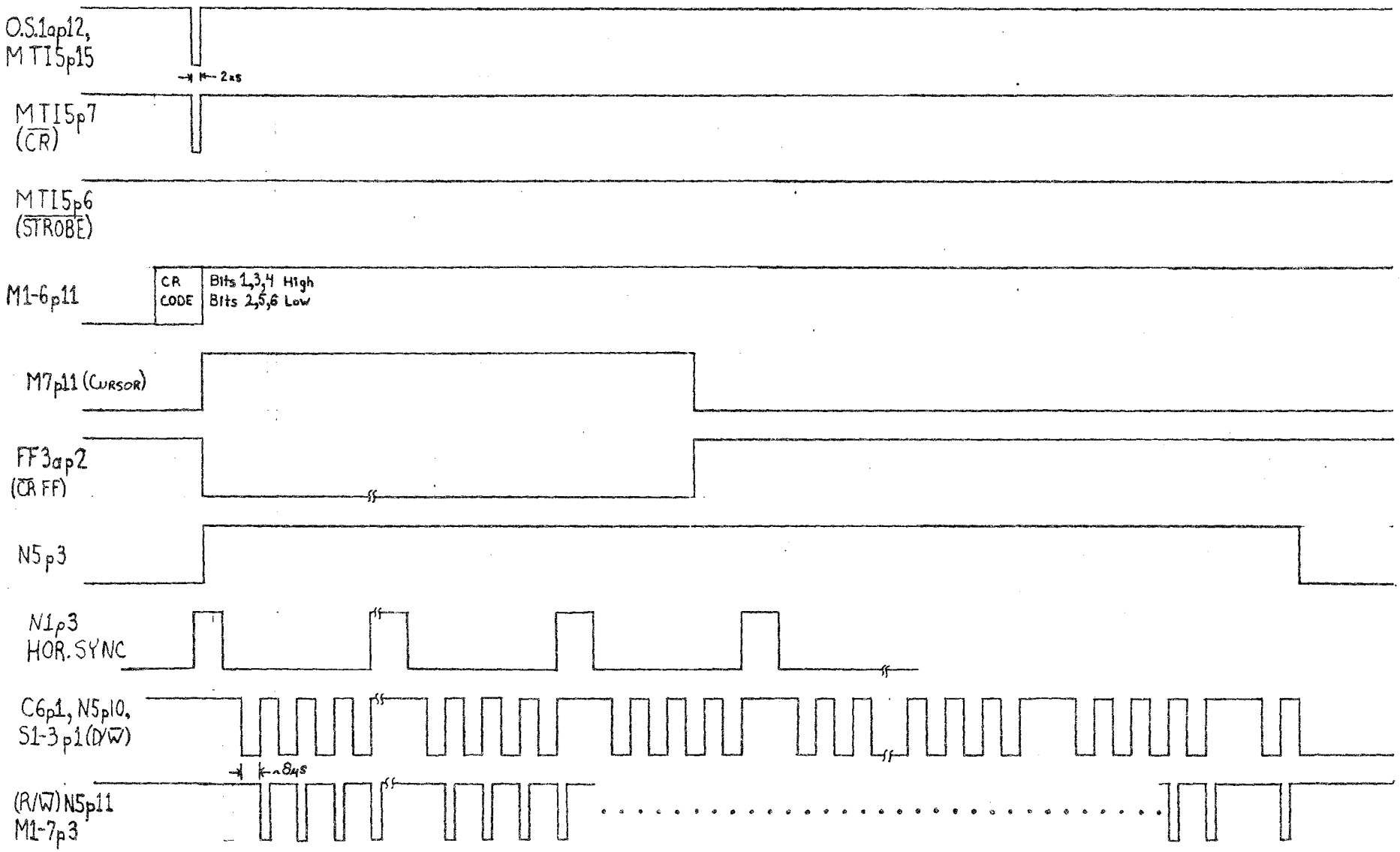
Since MTI5 decodes only the 5 MSB's of the ASCII character code it produces a $\overline{CR}$ pulse for four ASCII codes; i.e., OC-Form Feed; OC-CR: OE-SO and OF-SI.

To perform the CR function first the present row is filled with spaces and high cursor bits; then the pointer to the top row of the display (C4) has to be incremented modulo 16 and finally the bottom row of the display has to be erased. These last two actions comprise a scroll operation which is described in Section V-4.

The low level at FF3ap2 is applied to N5p2 which forces N5p3 and N5p6 high. The high at N5p6 enables a pulse train out of N5p4 as indicated in Fig. V-2.

Since N5p6 and N5p8 are high the pulse train from N10p3 is inverted twice and applied to C6p1, S1, S2 and S3p1. The rising edge at N5p10 is capacitively coupled to N5p12, 13 to produce a 1.5us negative going R/$\overline{W}$ pulse at N5p11 and M1-M7p3.

N7p4 is high (cursor data in) and OS1bp13 (Q) is low so memory data lines 1(LSB) through 5 (at A3p3, A3p4, A5p3, A5p6 and A5p8) are forced low while memory data lines 6 (MSB) and 7 (cursor) are held high. This insures that for each pulse in the train a space is written into memory with the cursor bit high to indicate the position has been filled.


O.S.1ap12, MTI5p15
2μs
MTI5p7 (CR)
MTI5p6 (STROBE)
M1-6p11
CR CODE
Bits 1,3,4 High
Bits 2,5,6 Low
M7p11 (CURSOR)
FF3ap2 (CR FF)
N5p3
N1p3 HOR. SYNC
C6p1, N5p10, S1-3p1 (R/W)
~84μs
(R/W) N5p11 M1-7p3

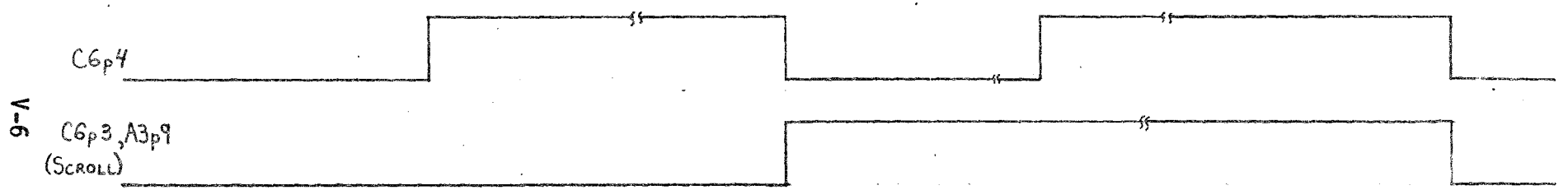


FIG. V-2 (CONT.) (SHEET 2 OF 2)

The falling edge of pulses in the train applied to C6p1 causes C6 to increment each time a space is written into memory. When the 64th column is loaded C6p3 rises.

The rising pulse resets the CR flip-flop (FF3a) and is inverted at N7p4 and applied to C4p1 (Row counter) and increments C4 modulo 16. A scroll operation is performed next.

V-4: SCROLL OPERATION

The scroll state (indicated by C6p3 going high) is entered to complete the CR operation. N7p4 is low and applied to N5p1. FF3ap2 ($\overline{CR}$) and N5p2 are now high so N5p3 remains high and the pulse train continues to pass through N5p4.

When the scroll state is entered as the result of C6 overflowing while loading displayable characters (see last paragraph of Section V-2), N7p4 ($\overline{Scroll}$) and N5p1 go low, FF3ap2 ($\overline{CR}$) and N5p1 are high so N5p3 goes high and allows N5p4 to produce its pulse train which is used to clear the old top row of the display.

Regardless of how the scroll state is entered, the high level at N5p3 enables a pulse train at N5p4 which is inverted once at N5p10 (since N5p6 is high -- $\overline{STROBE}$). These pulses are used to write spaces and <u>low</u> cursor bits into the new bottom row of the display in exactly the same manner as they are used to write spaces and <u>high</u> cursor bits into the memory for filling a row which has been terminated by a CR. Refer to Section V-3 for the details of how the new bottom row is cleared.

When the memory location corresponding to the last (64th) column in the bottom (16th) row is cleared C6p3 falls, forcing N5p3 and N5p6 low. The low level at N5p6 prevents any more pulses writing extra spaces into memory and incrementing C6.

V-5: CLEAR (PAGE) OPERATION

The ACT-I screen clear function can be activated in two ways: 1) during the power-on sequence; and 2) by depressing the PAGE key on the ACT-I keyboard.

Automatic screen clear upon power-up is accomplished by coupling the rising +5 volt power supply through a 15uf capacitor and N7 to the set input of the CR flip-flop (FF3a). The 5.6K resistor discharges the 15uf capacitor causing the set input to fall after approximately 50 milliseconds.

Depressing the PAGE key pulls N7p8 low and forces N7p10 and FF3ap6 (set) high. Hence the CR flip-flop is set for the duration that the PAGE key is depressed.

Holding FF3a in the set state causes the memory loading circuit to scroll repeatedly. Hence, all display memory positions are loaded with the ASCII space code and a low cursor bit. It takes only 40 milliseconds to clear the ACT-I screen.

If the PAGE key is depressed while characters are being received by the UART a clear screen will not always result since the clear and load functions were not designed to operate concurrently.

Programming Hint: In order to clear the ACT-I screen under program control (as opposed to manually depressing the PAGE key), a sequence of 16 carriage returns should be sent from the computer.

SECTION VI: OSCILLATORS AND CONTROL

The oscillators and control section (O & C) of the ACT-I is responsible for generating all timing clocks and control signals. The following components are used to produce these:
N1, N2, N3, N4, N8, N9, N10, A1, A2, A4, C7a, C8, C9, C10, FF1b, FF4a,b.

VI-1: 9.828MHz AND HORIZONTAL OSCILLATORS

All timing signals in the ACT-I are derived from a master, crystal-controlled, 9.828 Megahertz, oscillator. The output of this oscillator at N2p3 drives a divide-by-eight counter, C9, and also feeds N2p12 and A1p13. When N2p13 is high due to FF1b ($\overline{\text{Dot oscillator enable}}$) being in the reset state, the 9.828MHz square wave is gated through N2p11 to produce shift pulses for SR1. The inverted 9.828 MHz signal (N2p8) is applied to C1p1 and A1p9 in the video generator (VG) circuit.

The 1.2285 MHz output of C9 drives the UART count down chain in the input/output section (I/O) and also provides the count in pulses for C10 which is a divide-by-79 counter. The divide-by-79 is accomplished by "anding" the Q_0 (1-C10p12), Q_1 (2-C10p11), Q_2 (4-C10p9), Q_3 (8-C10p6) and Q_6 (64-C10p3) to generate the reset input to C10 at A2p11. This output is high for the duration of the reset propagation delay of C10 (about 100ns). The short positive pulse at A2p11 sets FF4a (Horizontal sync) by clocking it with the D input tied high. This short pulse occurs every 64.3 microseconds (15.550KHz). When C10 reaches a count of 16 (13us after being reset) Q_4 (C10p5) goes high and resets the horizontal sync flip-flop (FF4a). Hence the duration of the buffered Hor. sync and $\overline{\text{Hor. sync}}$ at N4p8 and N1p3 respectively is 13us.

VI-2: LEFT MARGIN DELAY AND DOT OSCILLATOR ENABLE

Q_4 of C10 (p5) is also applied to N3p12 to digitally control the left margin position. When Q_4 and Q_2 of C10 both are high (20 counts after the

reset of C10 and 4 counts after the end of the horizontal sync pulse) N3p11 falls and forces N3p8 high. The rising edge at N3p8 is coupled through a 220pf capacitor to N3p2. If the vertical position of the beam is in the display area (horizontal scan lines 48 through 208), the Display Enable flip-flop (FF4b) will be set and N3p1 will be high so the positive pulse at N3p2 is inverted and causes FF1b to reset. When the FF1b resets its $\overline{Q}$ output (pin 8) rises and allows the 9.828MHz dot oscillator to drive the shift register SR1 and the dot counter (C1). The output of the dot oscillator enable flip-flop (FF1bp8) is gated with the cursor data to the video combiner to prevent the cursor from being displayed outside of the display area.

Q_3 of C10 is used to increment C6 during the carriage return and scroll operations as explained in Section V.

VI-3: VERTICAL SYNC. AND DISPLAY ENABLE

The buffered horizontal sync pulses at N4p8 provide the increment signal to C8 which is a nine bit binary counter (C8 is a modulo 260 counter). When C8 reaches a count of 64 scan lines Q_6 (64-C8p4) is high, Q_7 (128-C8p13) is low, N9p11 rises and clocks FF4b into the set state. FF4bp13 (Q), N3p1, A2p9 and A2p10 rise accordingly. A2p10 is tied to the count-in line of C5. FF4b remains set until C7a reaches a count of 16 when the sixteenth row of characters finishes being displayed.

C7a is incremented each time the divide-by-ten displayable scan line counter (C3) resets. At the same instants positive going pulses are produced at A2p10 to increment C5.

When C8 reaches a count of 259 scan lines Q8 (256-C8p12), Q_0 (1-C8p9) and Q_1 (2-C8p7) rise, forcing N10p11 low resetting C8 and setting the vertical sync flip-flop which is actually two cross-coupled nand gates (N8p5, 6, 4 and N10p8, 9, 10). The output of this flip-flop is buffered through N4. When C8 reaches a count of 4, Q_2 (4-C8p6) rises and resets the vertical sync flip-flop. Hence the duration of the vertical sync pulse is 4 horizontal scans (4x64us = 256us).

SECTION VII: VIDEO DISPLAY GENERATION

The most complex circuit in the ACT-I is the display generation circuit. It is responsible for fetching characters from memory and generating the character and cursor data for the composite video output signal.

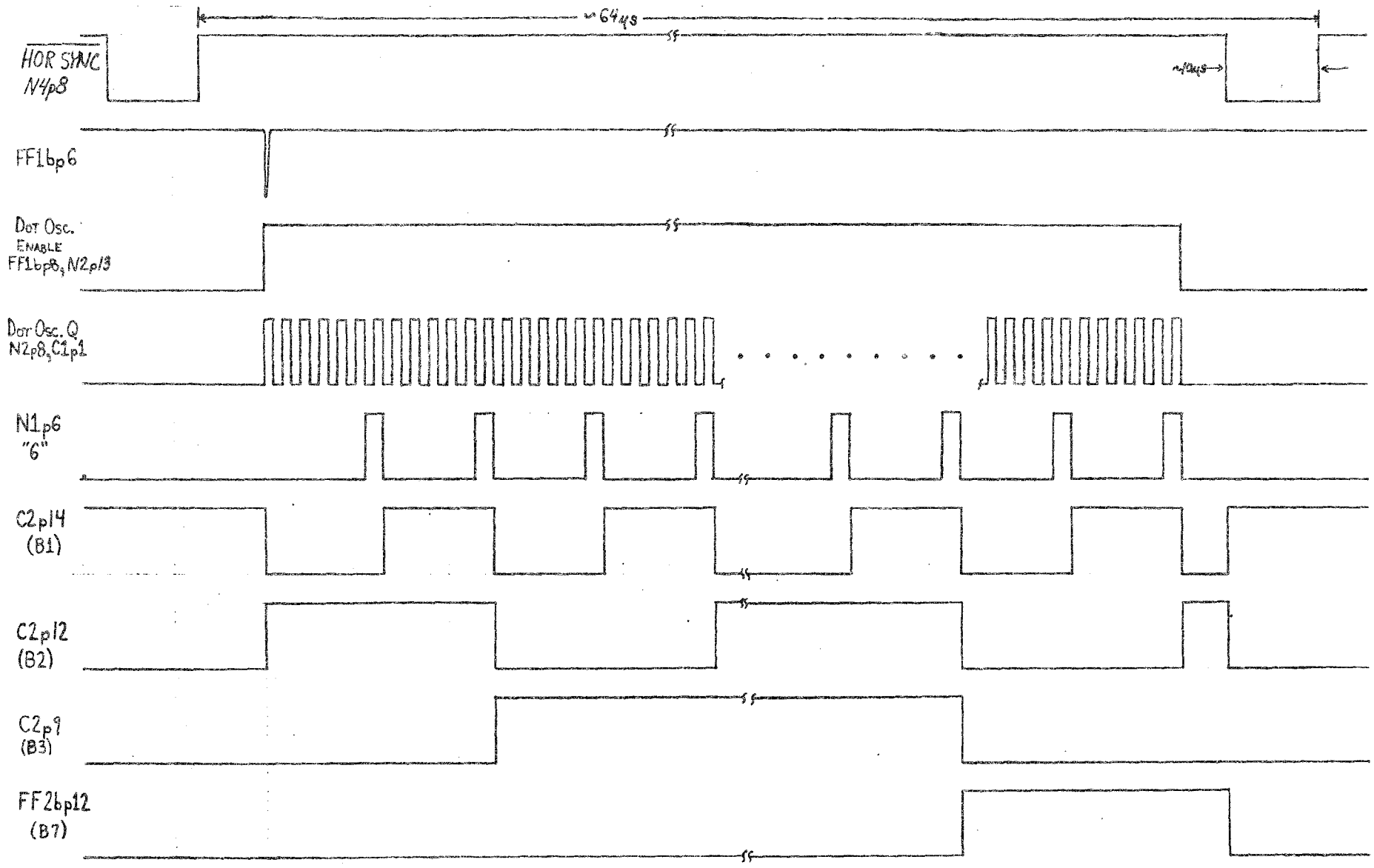
The description of this complicated circuit will start with the vertical retrace pulse and proceed as the beam travels from the top to the bottom of the video frame. The following components are used to generate the display: N1, N9, A1, A2, C1-C3, FF1, FF2, L1, L2, CG1, SR1, O1 and O2.

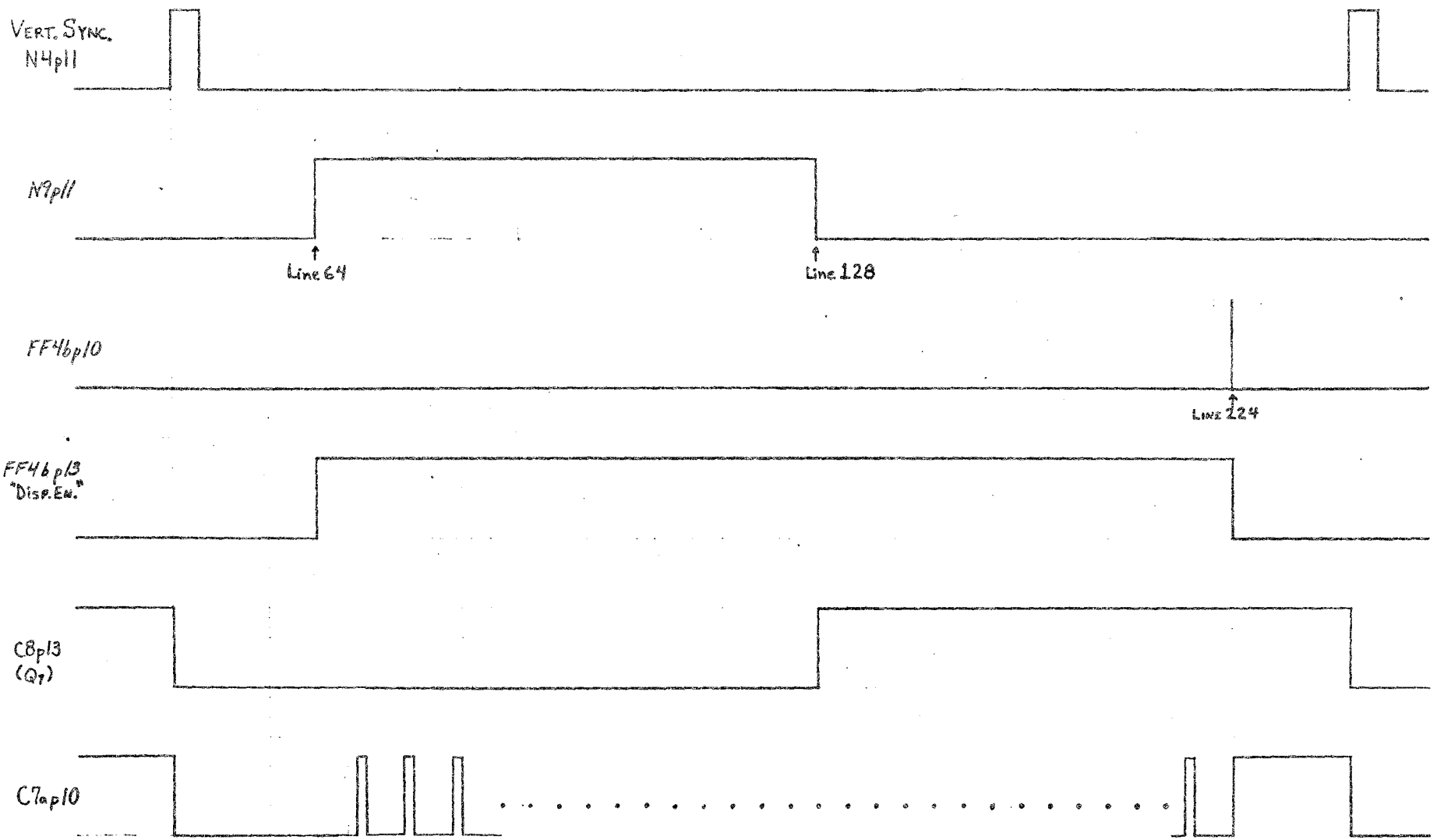
In order to enhance your understanding of the display circuitry's operation refer to Figures VII-1, VII-2 and VII-3.

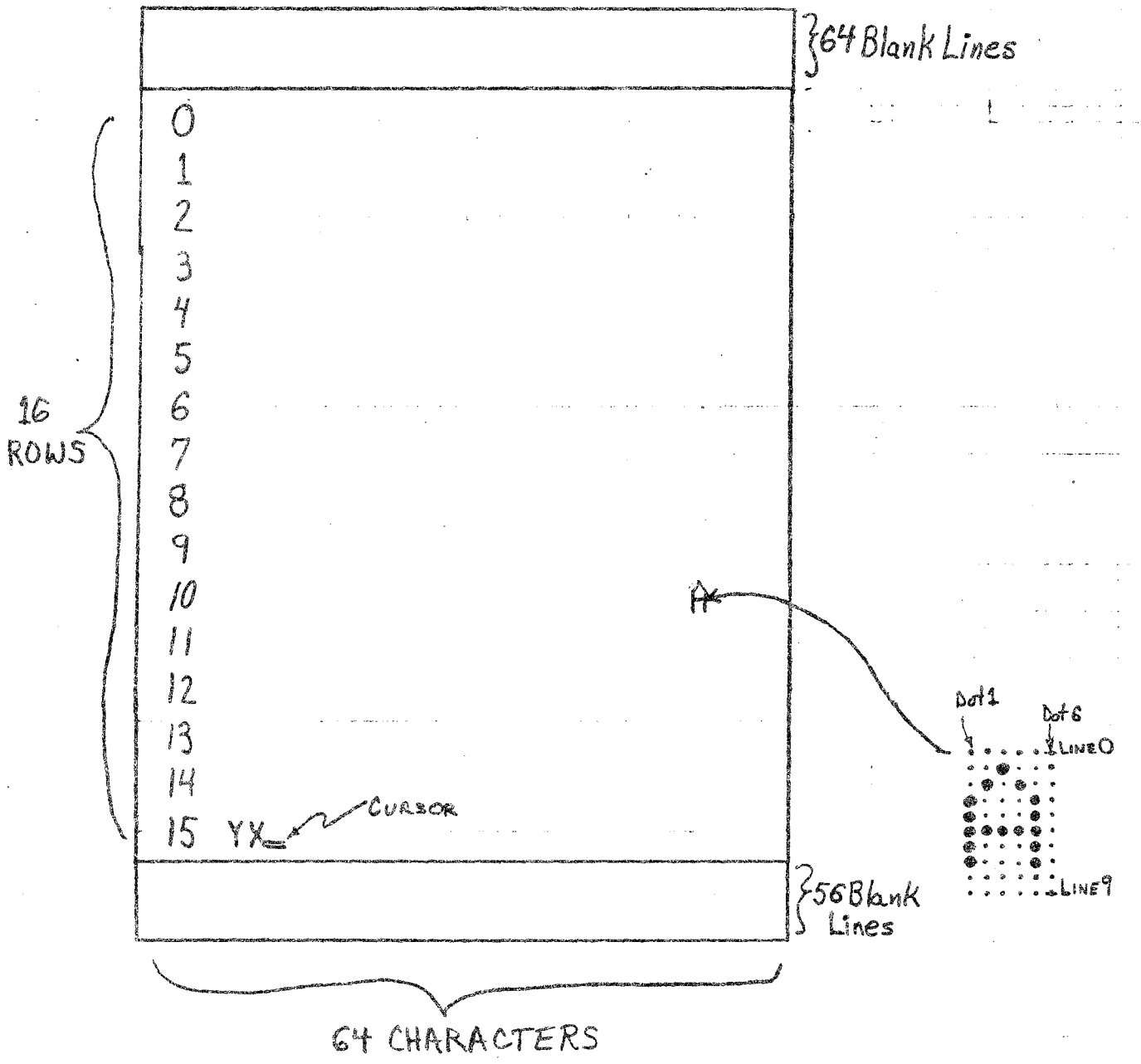
At the top of the screen the vertical sync pulse has just completed and cleared C7a (# of character rows displayed), C3 (Modulo 10 scan line counter to address the character generator chip) C8 (# of horizontal scan lines), and jammed the contents of C4 (pointer to bottom row of characters in memory) into C5 (character row address).

Sixty-four horizontal scan lines later C5p15 rises causing C5 to increment modulo 16. Hence the count in C5 changes from the address of the last row of characters (which was loaded into it by the vertical sync pulse at C5p1) to the address of the first row of characters to be displayed. The Disp. En. (FF4b) is set in coincidence with the end of the horizontal sync pulse since C8 counts on the rising edge of Hor sync.

The trailing edge of the $\overline{\text{Hor}}$ sync is or-ed with C1p12 (LSB of character column counter) to produce the count in signal for C2 (which holds the second, third, fourth and fifth bits of the 6 bit character column address). Hence at the start of the first displayable scan line (line 64) and at all other scan lines from 64 to 224, the character column counter is initiated to a value of 2. The six column address lines can be located as follows:


~64μs
~10μs
HOR SYNC
N4p8
FF1bp6
Dot Osc.
Enable
FF1bp8, N2p13
Dot Osc. Q
N2p8, C1p1
N1p6
"6"
C2p14
(B1)
C2p12
(B2)
C2p9
(B3)
FF2bp12
(B7)


VERT. SYNC.
N4p11
N9p11
Line 64
Line 128
FF46p10
Line 224
FF46p13
"Disp. En."
C8p13
(Q7)
C7ap10


64 Blank Lines
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16 ROWS
YX
CURSOR
A
Dot 1
Dot 6
LINE 0
LINE 9
56 Blank Lines
64 CHARACTERS

Bit #	Location
1 (LSB)	C1p12
2	C2p12
3	C2p9
4	C2p8
5	C2p11
6 (MSB)	FF2ap9

This column address is fed to the memory section through S1-S3 and in combination with the row address count held in C5 provides the memory with the address of the third character to be displayed during the present scan line. Latch L1 contains the ASCII code for the second character to be displayed and the shift register (SR1) holds the dot pattern of the present character scan line (pointed to by C3) of the first character to be displayed. Latch L2a holds the cursor bit for the second character to be displayed and L2b holds the cursor bit for the character presently being displayed.

The pulse train emanating from the dot oscillator drives C1 (dot counter and LSB of character column address), SR1 (shift register holding the dot patterns for the present character), and A1p12 (which gates the shift register data out to the video combiner circuit).

On the rising edge of the dot oscillator pulses (N2p8) C1 increments. The serial output of SR1p13 is anded with the dot oscillator pulses (N2p8) at A1p10. This output (A1p8) is anded with the delayed and inverted C3p11 (MSB of the character generator scan line address-counter). Thus when the beam traverses character scan lines eight and nine the serial data out of SR1 is blocked at A1p1 to avoid displaying erroneous dots during these two blank lines.

When C1 reaches a count of six N1p12 and 13 go high, N1p11 ("$\overline{6}$") goes low, and N1p5 ("6") goes high. The $\overline{6}$ pulses load the dot pattern of the next

character into SR1 by pulsing SR1p15 low during the sixth dot of each character in a scan line. The "6" pulses are applied to FF1ap1 (C) to affect the negation of the dot oscillator enable control signal when the 64th character has been displayed.

The rising edge of the seventh dot pulse causes the three least significant bits of C1 to reset to zero while the MSB increments (toggles). The MSB of C1 is the LSB of the character column counter. As mentioned above C1p12 (LSB col. cnt.) and Hor sync. are or-ed into C2p14 (count in for upper bits of char. col. cnt.). C2 continues to count as the beam scans across the line and "$\overline{6}$" pulses are generated.

When the character column count reaches a count of 64 FF2bp12 (Q) goes high, removing the reset signal from FF1ap2 and enabling FF1a to toggle on the falling edge of the "6" pulses. The $\overline{Q}$ output FF1ap13 is tied to C3p14 (count in line of the character scan line counter) so that C3 is incremented when the beam finishes displaying the 63rd character on the line and the 64th "$\overline{6}$" pulse will jam scan line data for the next line into SR1 while the ASCII code for the second character in the next line is jammed into L1. The Q output of FF1a is tied to FF1bp5 (clock line of the dot oscillator enable FF) and thus causes FF1bp8 (Dot Oscillator Enable) to fall when the beam finishes displaying the 64th character.

Since C3 is a modulo ten counter it increments C7a (Number of rows displayed) and C5 (pointer to present row) every 10 scan lines. When C7a reaches a count of 16 it sends a capacitively coupled rising pulse into the reset pin of FF4b (Display Enable FF) causing FF4p13(Q) to fall until the 64th scan line of the next frame when the entire process repeats.

VIDEO COMBINER AND CURSOR GENERATION

Data shifted out of SR1, cursor information and horizontal and vertical sync. pulses are all combined at transistors Q_1 and Q_2 to create a composite

video output signal which is capacitively coupled to the video out jack on the rear of the ACT-I cabinet. The output impedance is 1.2K.

The cursor data is generated by L2a, L2b and N9. When a negative going edge is sent from L2b to N9p8 through the R-C pulse circuit (which determines the width of the cursor), and C3p11 (character scan line counter MSB) is high, a 1us positive pulse will appear at N9p10 and be summed into the video out signal causing a double underscore cursor to appear at the position into which the next character is to be loaded. When the cursor is in its home position it will not be displayed in order to avoid CRT burn in this heavily used position.

Positive Horizontal or Vertical sync pulses cause Q_1 to pull the video out signal into the blanking level for synchronizing the monitor.

SECTION VIII: TROUBLE SHOOTING

In order to pinpoint the faulty component in a malfunctioning ACT-I, the unit should be placed in the self test mode by choosing RS232C output and connecting the serial out and serial in together.

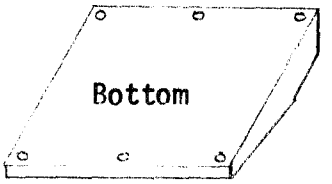
Having placed your unit in the self test mode you are ready to determine which of the four major circuits is malfunctioning. These four circuits are:

1) Power supply
2) Input/Output
3) Memory loading
4) Display

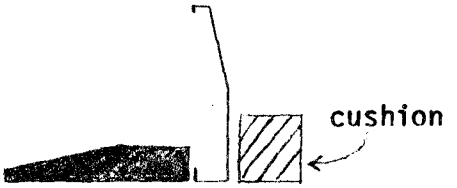
VIII-1: DISASSEMBLY

Performing the following tests requires access to the interior of the ACT-I cabinet. This can be accomplished by executing the following operations:

1) Unplug the ACT-I line and from its 110 volt AC source,
2) Remove the six "phillips" head screws which are located as indicated in the figure below (note that 4 of these are in rubber feet).



3) Place the ACT-I in its upright position and separate the black bottom piece and the white top piece by lifting the front of the white piece from the black piece while holding the rear of both cabinet pieces in close proximity. The white piece should be lifted to a vertical position and propped as below to insure stability.



VIII-2: EQUIPMENT

In order to perform the following tests the following equipment is required:

1) 35 MHz oscilloscope with dual trace
2) voltmeter
3) phillips head screw driver

VIII-3: POWER SUPPLY TEST

With the ACT-I turned on measure the +5 volt and the -12 volt power supplies on the main circuit board. The +5 supply can be found at the rightmost pin of the three 7805 regulator pins. The middle pin should be grounded and the left-most pin should have about +17 volts with about one volt of ripple. The 7805 (plus 5 volt) regulator should be securely fastened to the ACT-I chassis in order to heat sink it.

The minus twelve volt supply can be located at the emitter lead (rightmost) of the MPS3638 pass transistor (Q_3). Minus 12 can be found on the main circuit baord at pin 2 of the UART chip (U1p2) and at pin 1 of the 2513 character generator chip (CG1p1).

The +5 volt regulator (7805) has short circuit and thermal protection and will shut off if its output gets shorted or if it gets too hot. A thermal problem will cause the output to cycle on and off as the chip's temperature changes. Proper heat sinking of the regulator to the ACT-I chassis will prevent any thermal problems.

The -12 volt supply is a zener diode-pass transistor type. It has no short circuit or thermal protection. Should its output become shorted the MPS 3638 pass transistor will be permanently damaged. Under normal operating conditions the -12 supply is loaded very lightly and the MSP3638 needs no heat sink.

VIII-4: DIAGNOSIS OF MAIN BOARD MALFUNCTIONS

Having determined that the main board is a fault you can determine which of the I/O, memory loading, or display circuits is faulty by performing the following tests.

VIII-4.1: I/O TEST

With the unit in the self test mode (described at the beginning of this section) repeatedly strike the letter A and compare actual waveforms with those given in Section III of this manual. If the necessary signals check out and in particular if the negative going pulse ($\overline{\text{STROBE}}$) appears at pin 6 of MTI5 and the UART clock frequency is correct, the I/O circuitry is performing as required.

VIII-4.2: MEMORY LOADING TEST

Depress the PAGE key and verify that FF3a (CR FF) sets and remains set while the PAGE key is depressed. Also verify that C6 and C4 are counting properly and R/$\overline{W}$ pulses appear at M1-M7p3 as described in section V. If these waveforms check out the memory loading circuitry is not at fault.

VIII-4.3: MEMORY TEST

The most common memory failure is a tendency to make bit errors. For example after clearing the screen an ! may appear in one position on the screen. This is due to an errant memory bit in the least significant position (ASCII code for space = 20_{16}, ! = 21_{16}). If this problem occurs the appropriate memory (M1-M7) should be replaced. Another symptom is that when loading a given position with a character the character in a different position is altered. The bit which is modified indicates the faulty memory chip.

VIII-4.4: DISPLAY GENERATION TEST

If the power supply I/O and display loading circuits pass their tests and an abnormal display (or no display at all) persists the display circuitry is at fault. Refer to section VII and verify that all waveforms are as indicated.

Some symptoms and the associated remedies are listed below:

VIII-5: TROUBLE SYMPTOMS AND REMEDIES

The following is a list of reported trouble symptoms and the remedies suggested by the Micro-Term technical staff:

	SYMPTOM	REMEDY
1)	Rubout code (FF Hex) sent instead of struck character	Strobe from keyboard to UART should be delayed 10 microseconds by tying .1uf capacitor from U1p23 to ground (U1p21) and placing a 1K resistor in series with the KBD strobe line KBD pin 6.

SECTION IX: TECHNICAL INFORMATION

IX-1: ASCII CODES

HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR
00	NUL	20	SP	40	@	60	`
01	SOH	21	!	41	A	61	a
02	STX	22	"	42	B	62	b
03	ETX	23	#	43	C	63	c
04	EOT	24	$	44	D	64	d
05	ENQ	25	%	45	E	65	e
06	ACK	26	&	46	F	66	f
07	BEL	27	'	47	G	67	g
08	BS	28	(	48	H	68	h
09	HT	29	)	49	I	69	i
0A	LF	2A	*	4A	J	6A	j
0B	VT	2B	+	4B	K	6B	k
0C	FF	2C	,	4C	L	6C	l
0D	CR	2D	—	4D	M	6D	m
0E	SO	2E	.	4E	N	6E	n
0F	SI	2F	/	4F	0	6F	o
10	DLE	30	0	50	P	70	p
11	DC1	31	1	51	Q	71	q
12	DC2	32	2	52	R	72	r
13	DC3	33	3	53	S	73	s
14	DC4	34	4	54	T	74	t
15	NAK	35	5	55	U	75	u
16	SYN	36	6	56	V	76	v
17	ETB	37	7	57	W	77	w
18	CAN	38	8	58	X	78	x
19	EM	39	9	59	Y	79	y
1A	SUB	3A	:	5A	Z	7A	z
1B	ESC	3B	;	5B	[	7B	{
1C	FS	3C	<	5C	\	7C	!
1D	GS	3D	=	5D	]	7D	}
1E	RS	3E	>	5E	^	7E	~
1F	VS	3F	?	5F	←	7F	DEL

IX-2 GENERAL SPECIFICATIONS

Display (Receiver):

Format - 64 characters by 16 lines

Spacing - Horizontal - one dot between characters
Vertical - 3 scan lines between rows of characters

Character set - Uppercase alphabet, numbers and punctuation;
64 total ASCII codes

Refresh rate - 60 Hz (non-interleaved)

Video out - 1.5 vp-p, RS 170

Cursor - Underline, double stroke, extinguished in home position
to prevent phosphor burn and prolong CRT life

Data Rate - the display (receiver) can load characters at rates
between 110 and 9600 Baud, RS232C or 20 ma current loop

Transmitter:

Character set - uppercase ASCII - includes all control codes

Data Rate - 110 to 9600 Baud crystal controlled - RS232C or 20 ma
current loop

General:

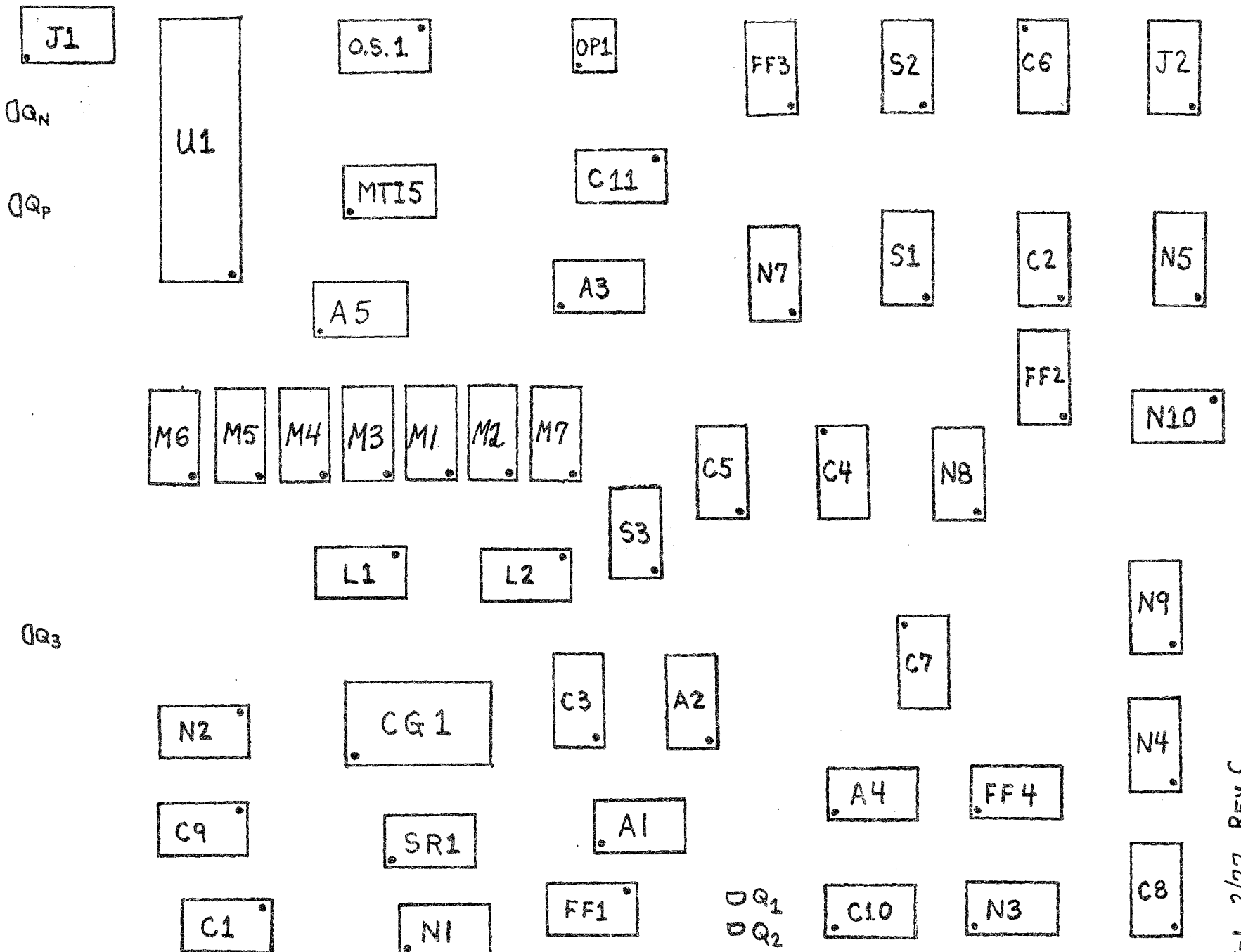
Power - 110 volts AC, 50-60 Hz, 15 watts

Size - 7.5 x 36 x 28 cm (3 x 14 x 11 inches)

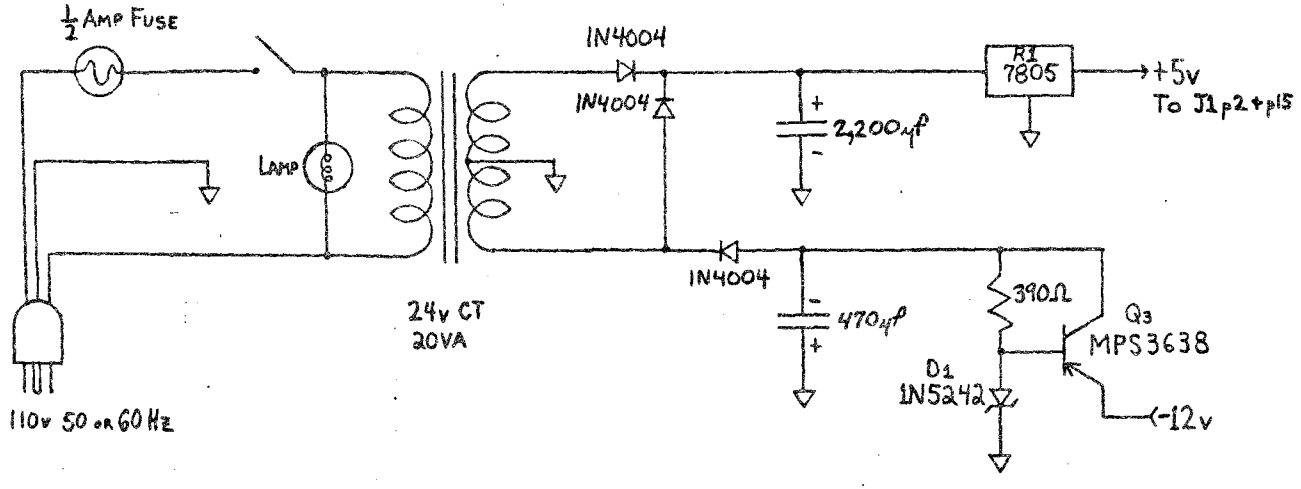
Weight - 5 Kg (8 lbs.)

IX-3: INTEGRATED CIRCUIT IDENTIFICATION AND POWER CONNECTION - REV. C

Part	Type	+5 Pin	Ground Pin	Other Power Pin(s)
A1, A5	74LS08	14	7	
A2, A3	4081	14	7	
A4	4082	14	7	
C1	7492	5	10	
C2	7493	5	10	
C3	7490	5	10	
C4,C6,C10	4024	14	7	
C5	4029	16	8	
C7	4520	16	8	
C8,C11	4040	16	8	
C9	7493	5	10	
CG	2513	24	10	-5v pin 12, -12v pin 1
FFL,FF2	74LS73	4	11	
FF3,FF4	4013	14	7	
L1	74LS174	16	8	
L2	74LS74	14	7	
M1-M7	2102L1PC	10	9	
N1,N3,N4	74LS00	14	7	
N2	7400	14	7	
N5,N7,N8,N10	4011	14	7	
N9	4001	14	7	
O.S.1	74123	16	8	
OP1	MC1458	8	--	-12v pin 4
S1-3	74LS157	16	8	
SR1	74166	16	8	
U1	AY-5-1013	1	3	-12v pin 2

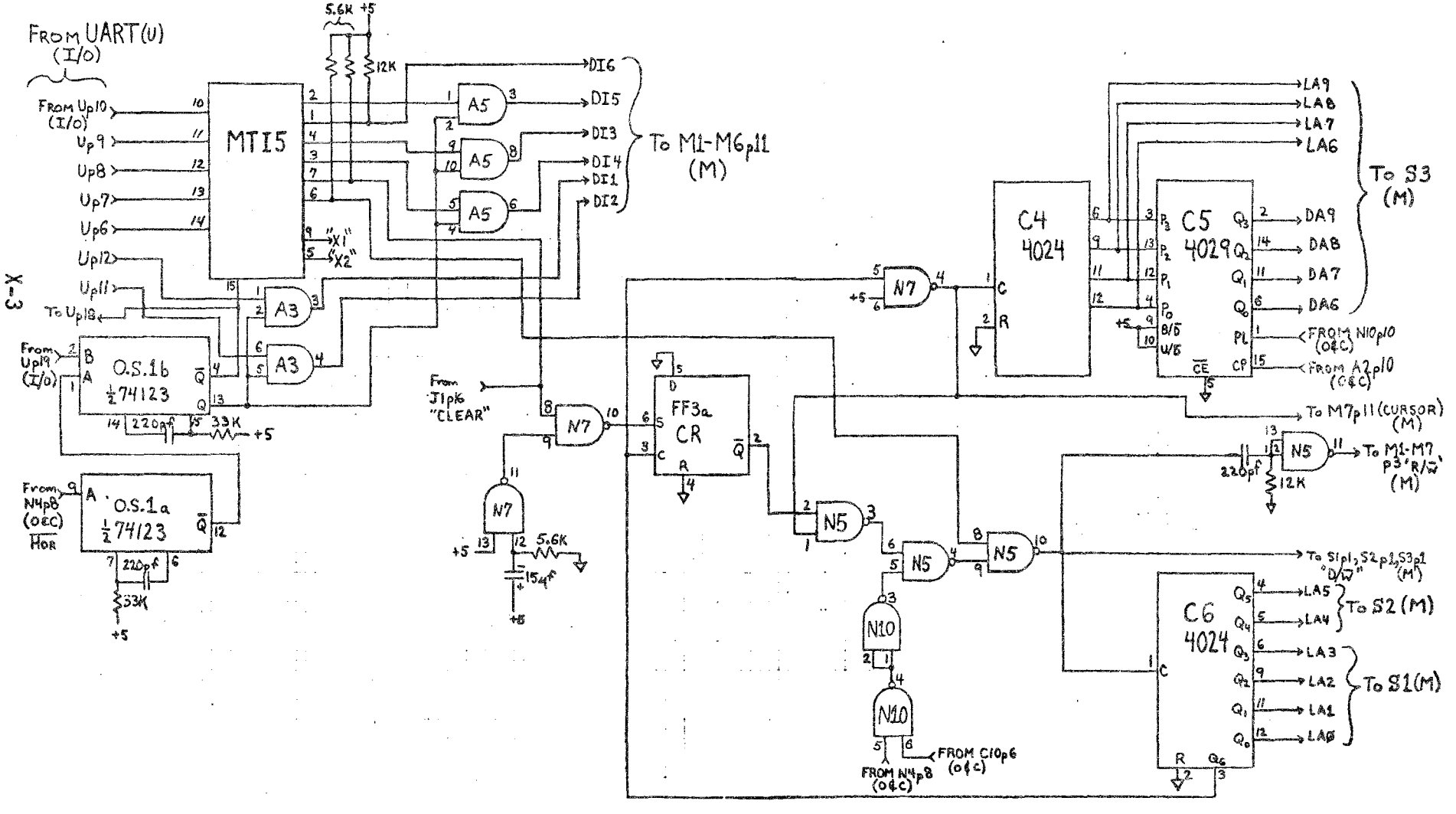


PARTS LOCATION



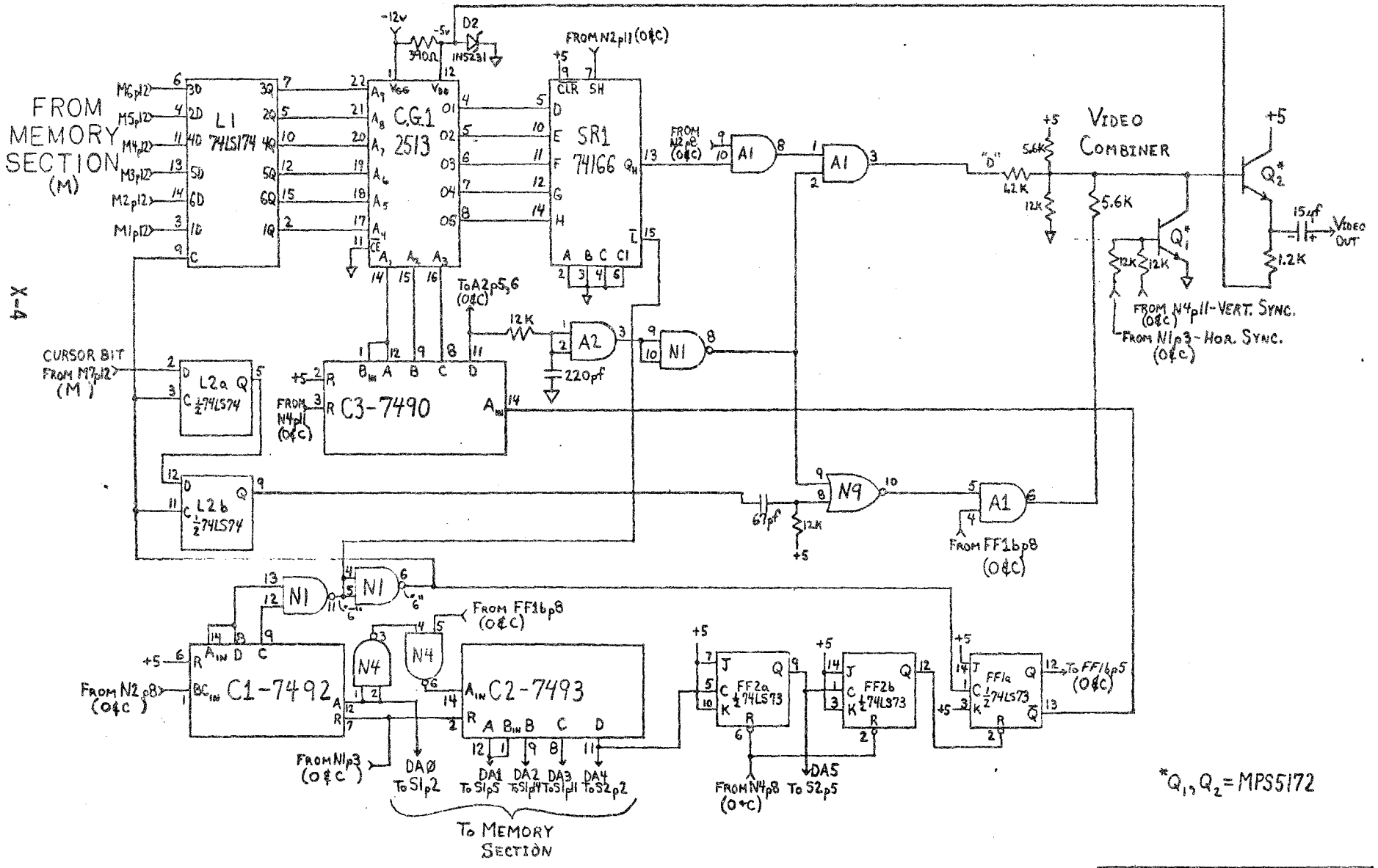
ACT-I Power Supply (P)

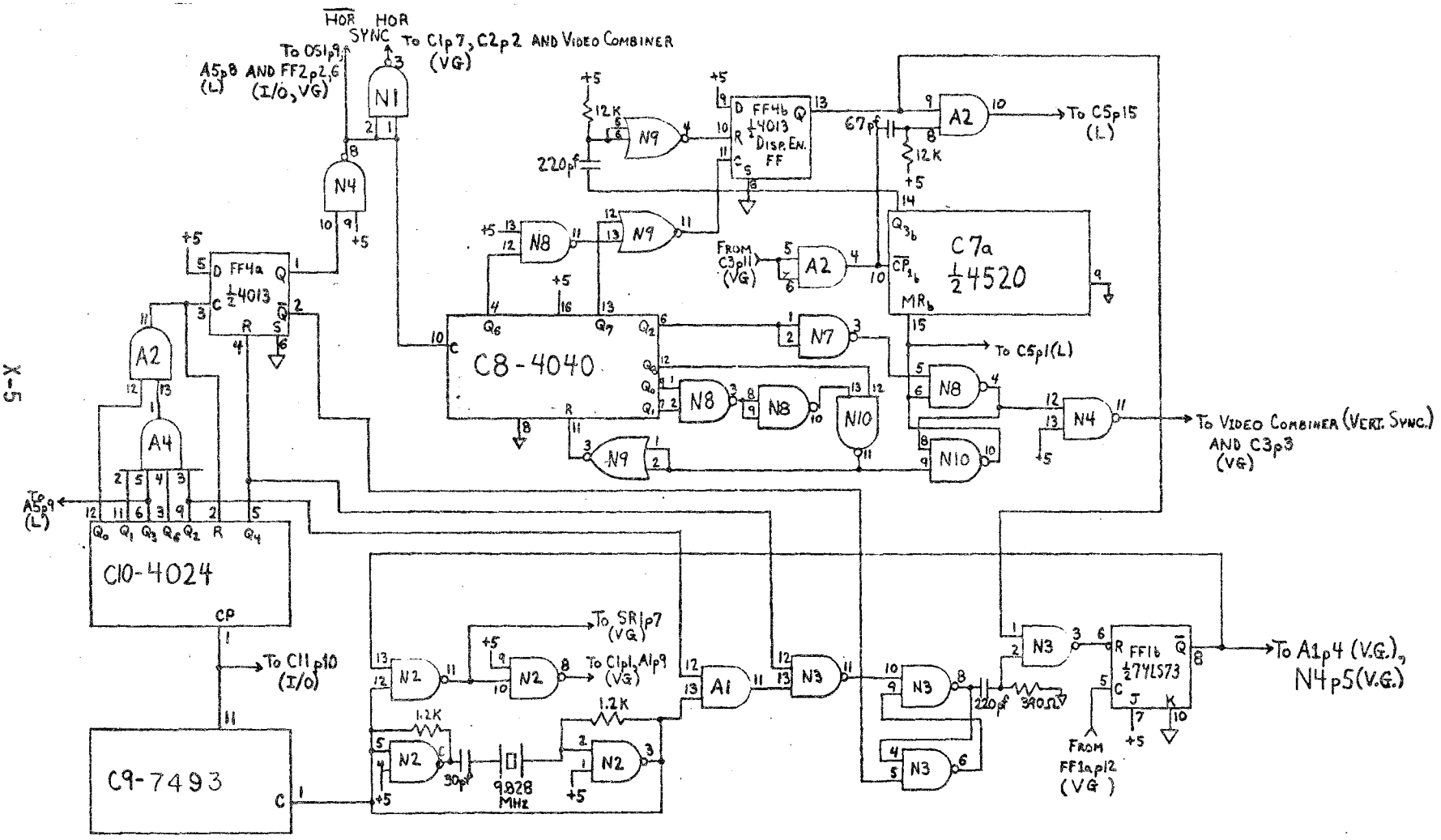
 | Rev C



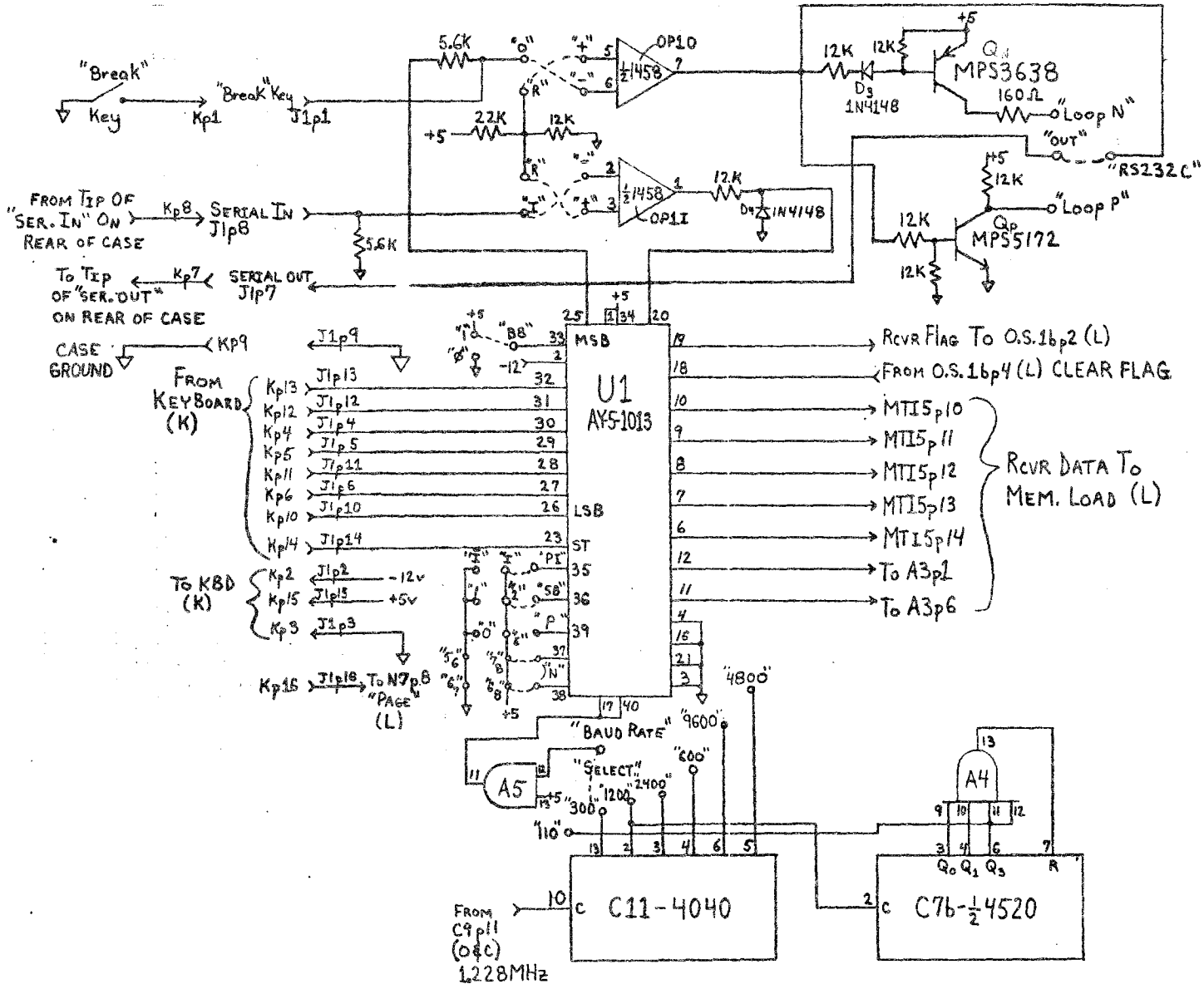
X-3

MEMORY LOADING SECTION (L)

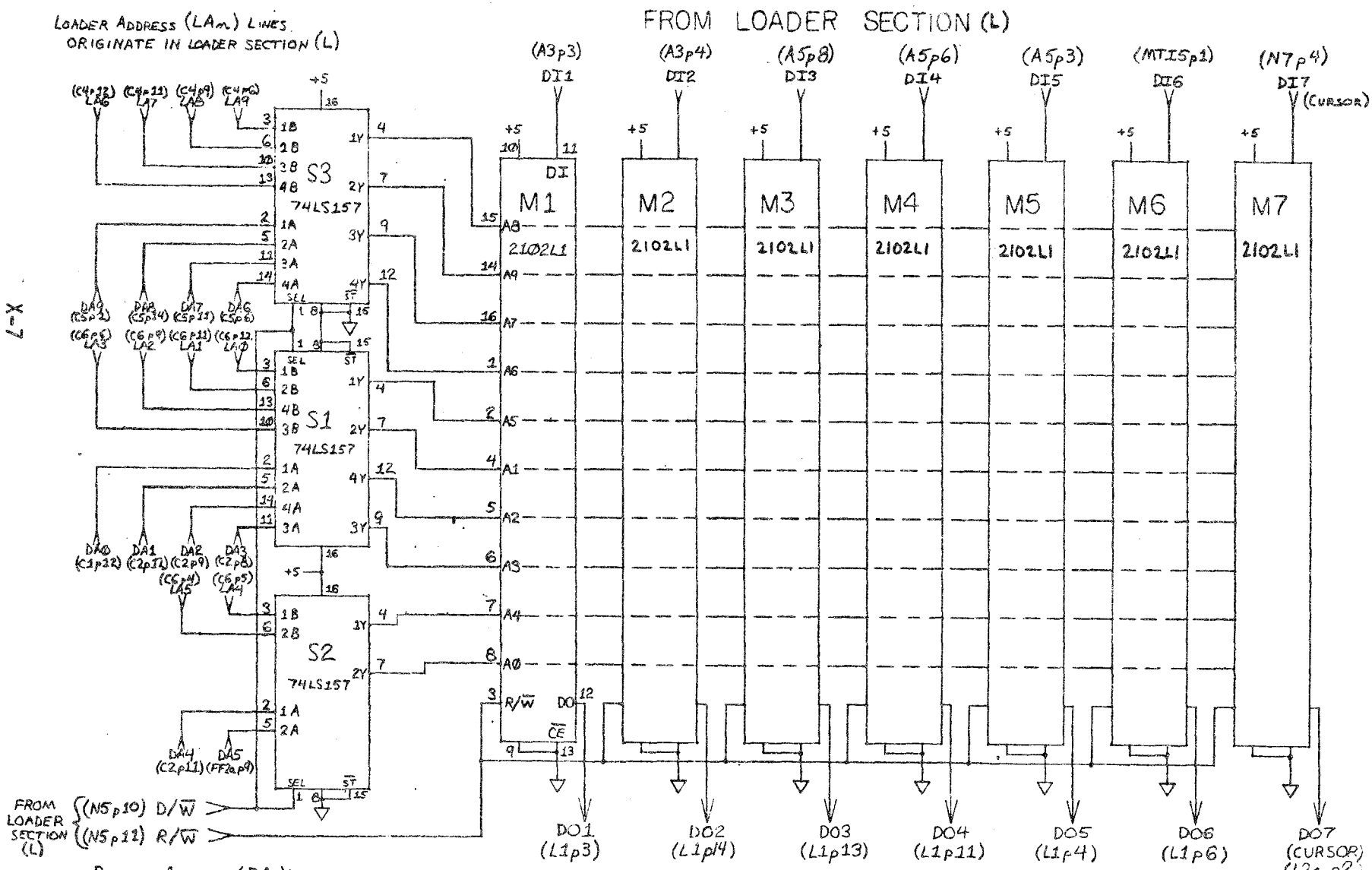

FROM MEMORY SECTION (M)
L1 74LS174
C.G.1 2513
SR1 74166
-12v
-5v
340Ω
D2
IN5231
FROM N2p11 (O&C)
VIDEO COMBINER
+5
5.6K
"D"
4.2K
12K
5.6K
Q2*
Q1*
15μf
VIDEO OUT
1.2K
FROM N4p11-VERT. SYNC. (O&C)
FROM N1p3-HOR. SYNC. (O&C)
ToA2p5,6 (O&C)
12K
220pf
A2
N1
A1
CURSOR BIT FROM M7p12 (M)
L2a 74LS74
L2b 74LS74
C3-7490
FROM N4p11 (O&C)
67pf
N9
FROM FF1bp8 (O&C)
C1-7492
C2-7493
N4
FROM N2p8 (O&C)
FROM N1p3 (O&C)
DA0 To S1p2
DA1 To S1p5
DA2 To S1p4
DA3 To S1p1
DA4 To S2p2
To MEMORY SECTION
FF2a 74LS73
FF2b 74LS73
FF1a 74LS73
FROM N4p8 (O&C)
DA5 To S2p5
To FF1bp5 (O&C)
*Q1, Q2 = MPS5172
ACT-I VIDEO GENERATOR (VG)
X-4

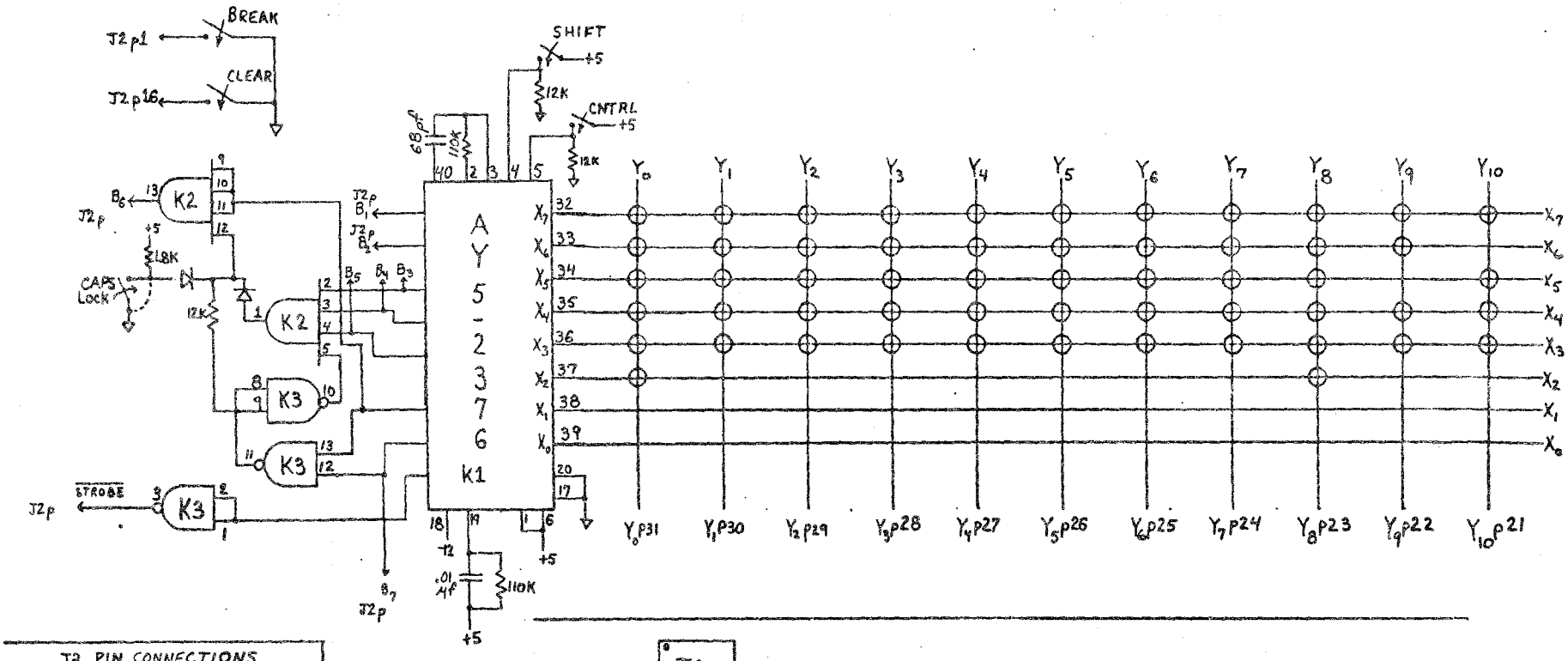

HOR
HOR SYNC
To C1p7, C2p2 AND VIDEO COMBINER (VG)
To OS1p9, A5p8 AND FF2p2,6 (L) (I/O, VG)
N1
N4
+5
12K
N9
220pf
D FF4b Q
R 1/4013 Disp. En. FF
67pf
A2
To C5p15 (L)
12K
N8
FROM C3p11 (VG)
C7a
1/4520
MR
To C5p1(L)
D FF4a Q
C 1/4013 R S
A2
A4
C8-4040
N7
N8
N10
To VIDEO COMBINER (VERT. SYNC.) AND C3p3 (VG)
To A5p9 (L)
C10-4024
CP
To C11p10 (I/O)
C9-7493
To SR1p7 (VG)
To C1p1, A1p9 (VG)
N2
1.2K
30pf
9.828 MHz
A1
N3
FF1b 1/74LS73
220pf
340Ω
FROM FF1ap12 (VG)
To A1p4 (V.G.), N4p5(V.G.)

X-5



NOTE: All Jumpers For Default Values


LOADER ADDRESS (LAm) LINES ORIGINATE IN LOADER SECTION (L)
FROM LOADER SECTION (L)
(A3p3) DI1
(A3p4) DI2
(A5p8) DI3
(A5p6) DI4
(A5p3) DI5
(MT15p1) DI6
(N7p4) DI7 (CURSOR)
S3
S1
S2
74LS157
M1
M2
M3
M4
M5
M6
M7
2102L1
DI
DO
R/W
CE
A8
A9
A7
A6
A5
A1
A2
A3
A4
A0
FROM LOADER SECTION (L)
(N5p10) D/W
(N5p11) R/W
DO1 (L1p3)
DO2 (L1p14)
DO3 (L1p13)
DO4 (L1p11)
DO5 (L1p4)
DO6 (L1p6)
DO7 (CURSOR) (L2a p2)
DISPLAY ADDRESS (DAn) LINES ORIGINATE IN VIDEO GENERATOR SECTION (VG)
TO VIDEO GENERATOR (VG)



8-X

J2 PIN CONNECTIONS

PIN#	SIGNAL
1	BREAK
2	-12v
3	GROUND
4	B5
5	B4
6	B2
7	SERIAL OUTPUT
8	SERIAL INPUT
9	GROUND
10	B1 (LSB)
11	B3
12	B6
13	B7 (MSB)
14	STROBE
15	+5v
16	CLEAR

J2

AY 5-2376
ENCODER K1

K2 K3

Top View (Key switch side)

KEYBOARDS