



ATL-008 MAINTENANCE MANUAL

© 1984 by Beehive

This equipment complies with the requirements in Part 15 of FCC Rules for a Class A computing device. Operation of this equipment in a residential area may cause unacceptable interference to radio and TV reception requiring the operator to take whatever steps are necessary to correct the interference.

Notice: This document has been prepared by Beehive International and is furnished on the condition that it will be used by the customer solely for the purpose of supporting operation, service, and maintenance of Beehive products. Beehive believes that the information described in this manual is accurate and reliable, and much care has been taken in its preparation. However, no responsibility, financial or otherwise, is accepted for any consequences arising out of the use of this manual or this material. Revisions may be issued to advise of such changes and/or additions. This document shall not be duplicated by the customer nor released, disclosed or used, in full or in part, for any purpose other than as stated herein, without the express written permission of Beehive International.

All specifications contained in this manual are subject to change at any time without notice.

DOCUMENT TM0283-T1-2

REV. 7/84

VERSION 1.0



1

**HARDWARE
OVERVIEW**

2

**ON-SITE MAINTENANCE
AND REPAIR**

3

**ATL POWER SUPPLY
FUNCTIONAL
DESCRIPTION**

4

**ATL-008 MONITOR
FUNCTIONAL
DESCRIPTION**

5

**KEYBOARD
FUNCTIONAL
DESCRIPTION**

6

**LOGIC BOARD
FUNCTIONAL
DESCRIPTION**

A

APPENDICES

**ASCII CODE CHART
MEMORY MAP
PAL EQUATIONS & STATE TABLES**

**SCHEMATIC
DRAWINGS**

**H
O**

**M
&
R**

**P
S**

**M
O
N**

**K
B
D**

**L
B**

A

**S
D**

TABLE OF CONTENTS

1

HARDWARE OVERVIEW

INTRODUCTION	1-1
CONTROLS AND INDICATORS	1-1
Power Switch	1-1
Status Lines	1-2
Audio Alarms	1-2
FUSE	1-2
CONNECTORS	1-2
VENTILATION	1-2
HARDWARE DESCRIPTION	1-2
Identification of Optional Components	1-2
Internal Cabling	1-3
Power Supply	1-4
Monitor	1-4
Keyboard	1-4
Logic Board	1-4

2

ON-SITE MAINTENANCE AND REPAIR

GENERAL INFORMATION	2-1
Warranty Provisions	2-1
Operating Environment	2-1
Ventilation and Contaminants	2-1
AC Power	2-2
Potential Hazards	2-2
Tools and Test Equipment	2-3
PROBLEM DIAGANOSIS	2-3
General	2-3
Functional Failures	2-4
Video Failures	2-5
Communications Failures	2-7
KEYBOARD FAILURES	2-9
SUBASSEMBLY REPLACEMENT	2-9
Tools and Tips	2-9
Removing and Replacing the Cover	2-10
Removing and Replacing the Logic Board	2-12
Removing and Replacing the Power Supply	2-15
Removing and Replacing the Monitor Board and Yoke	2-18
Removing and Replacing the Monitor CRT	2-22
Removing and Replacing the Keyboard	2-26

TABLE OF CONTENTS (cont.)

3	ATL POWER SUPPLY FUNCTIONAL DESCRIPTION	
	GENERAL	3-1
	FUNCTION	3-1
4	ATL-008 MONITOR FUNCTIONAL DESCRIPTION	
	GENERAL	4-1
	PRINTED CIRCUIT BOARD ASSEMBLY	4-1
	Video Amplifier	4-2
	Horizontal Deflection	4-2
	Vertical Deflection Processor	4-3
	Dynamic Focus	4-4
	CATHODE RAY TUBE ASSEMBLY	4-4
5	KEYBOARD FUNCTIONAL DESCRIPTION	
	GENERAL	5-1
	8039 MICROCOMPUTER	5-1
	CRYSTAL FREQUENCY	5-1
	INTERFACE TO TERMINAL	5-1
	Keyboard Receive Data	5-2
	Keyboard Transmit Data	5-2
	POWER SUPPLY	5-2
	GROUNDING	5-2
	MATRIX SCANNING	5-2
	Byte-Wide Interface	5-2
	Scanning Levels	5-5
	Keyboard Encoding	5-5
	MEMORY	5-5
	AUDIO ALARM	5-5
	RESET CIRCUIT	5-6
6	ATL-008 LOGIC BOARD FUNCTIONAL DESCRIPTION	
	GENERAL	6-1
	68008 MICROPROCESSOR	6-1
	Address Bus (A0 – A19)	6-2
	Data Bus (D0 – D7)	6-2
	Clock Generator	6-3
	Reset	6-3
	Halt	6-3
	Bus Error	6-3
	Control Bus	6-4
	PERIPHERALS	6-6
	Serial Communications Controller	6-6
	Universal Peripheral Interface	6-7
	CRT Controller	6-9
	Board Revision Level	6-9
	Contrast Control	6-9
	Video Features Register	6-9
	System Control Register	6-10

TABLE OF CONTENTS (cont.)

MEMORY	6-10
Memory Map	6-10
Dynamic RAM Array	6-10
Static RAM	6-14
Read Only Memory Array	6-14
VIDEO SECTION	6-16
9007 CRT Controller	6-17
9021 Video Attributes Controller	6-18
1K × 4 Static RAMs	6-20
BUS ARBITER/REFRESH CONTROLLER	6-21
Bus Arbitration	6-21
Dynamic RAM Refresher	6-22

APPENDIX **A** ASCII CODE CHART

APPENDIX **B** ATL-008 MEMORY MAP

APPENDIX **C** ATL-008 PAL EQUATIONS & STATE TABLES

FIGURES

Figure 1-1	ATL Terminal	1-1
Figure 2-1	Electrified Electronic Technician	2-2
Figure 2-2	Voltage Hazards	2-2
Figure 2-3	Power Supply Output Voltage Locations	2-4
Figure 2-4	+5VDC Adjustment Pot	2-5
Figure 2-5	Logic Card Ribbon Cable Connector to Monitor Card	2-6
Figure 2-6	Video Output from Logic Card (Pin 1)	2-6
Figure 2-7	Horizontal Sync Output from Logic Card (Pin 6)	2-6
Figure 2-8	Vertical Sync Output from Logic Card (Pin 9)	2-7
Figure 2-9	RS232 Loopback Test Connector	2-7
Figure 2-10	Main Port RS422 Loopback Test Connector	2-8
Figure 2-11	20mA Current Loop Loopback Test Connector	2-8
Figure 4-1	Monitor Board Block Diagram	4-1
Figure 5-1	Byte-Wide Pinouts	5-4
Figure 5-2	Byte-Wide Timing Diagram	5-4
Figure 6-1	68008 Input/Output Signal Configuration	6-1
Figure 6-2	68008 System Block Diagram	6-2
Figure 6-3	ATL-008 Memory Map	6-11
Figure 6-4	DRAM Byte Write Cycle Flow Chart	6-12
Figure 6-5	DRAM Write Word Timing Diagram	6-12
Figure 6-6	DRAM Byte Read Cycle Flow Chart	6-13
Figure 6-7	DRAM Read Word Timing Diagram	6-14
Figure 6-8	ROM/EEPROM Read Word Timing Diagram	6-15
Figure 6-9	EEPROM Write Word Timing Diagram	6-16

TABLES

Table 1-1	ATL-008 Optional Component Identification	1-3
Table 2-1	Power Supply Output Voltages	2-4
Table 2-2	Logic Board Video Output Signals	2-5

TABLE OF CONTENTS (cont.)

Table 5-1	J1 Data Jack Pin Assignments	5-2
Table 5-2	Byte-Wide AC Characteristics	5-4
Table 5-3	Keyboard Internal/External Memory Strapping	5-5
Table 6-1	Data Strobe Control of Data Bus	6-4
Table 6-2	Function Code Outputs	6-5
Table 6-3	Main/Auxiliary Port Selection	6-7

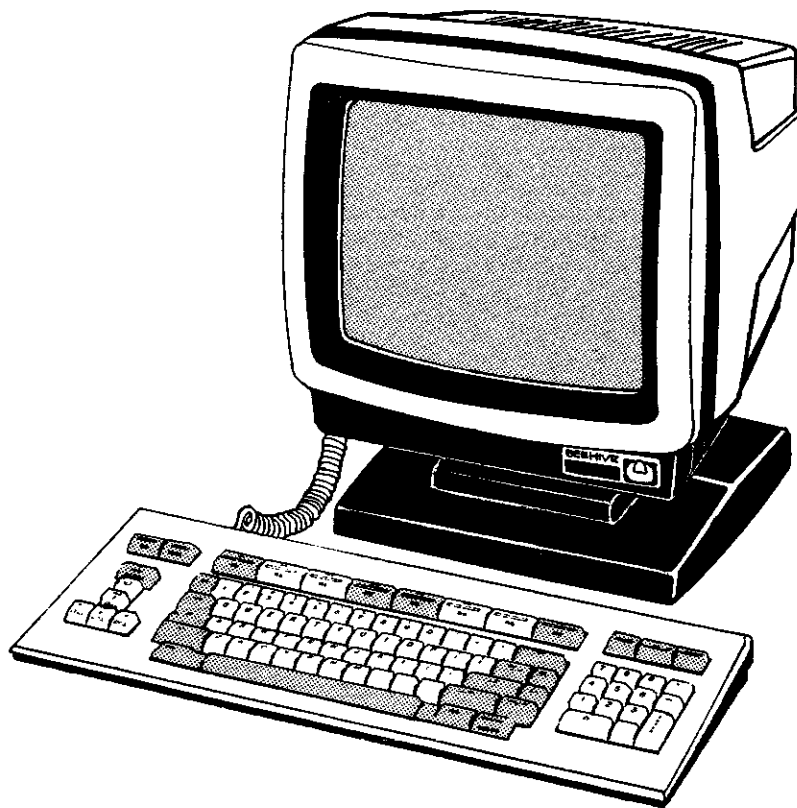
1

HARDWARE OVERVIEW

INTRODUCTION

Members of the Beehive ATL family of terminals consist of a display screen with integral logic, video control, and communications circuitry and a detachable keyboard. The screen housing may be rotated and tilted. See Figure 1-1.

Figure 1-1
ATL Terminal



CONTROLS AND INDICATORS

Power Switch

A rocker switch on the rear panel controls power to the terminal. It is located so it may be easily reached with the right hand while using the terminal. Pressing the lower half of the switch turns the terminal on; pressing the top half turns the terminal off. Aside from the keys on the keyboard, this is the only external control on ATL terminals.

Status Lines

Line 25 divides the ATL screen into two areas: lines 1 to 24 are the data display area, lines 26 and 27 are the status lines. Line 26 indicates terminal status. Line 27 displays the status of the softkeys. These status lines are the only external indicators for ATL terminals.

Other terminal functions (contrast, intensity, error reporting, etc.) are handled by the Terminal Configuration Manager (TCM). See the appropriate Technical User's Manual for a description of TCM controls and indicators.

Audio Alarms

The keyboard is capable of generating two beeps, a ring, warble and a click. The beeps produce a 600 Hz tone or a 1200 Hz tone. A ring is a signal alternating between 600 Hz and 1200 Hz. A warble is the same as a ring but with a different rate of alternation. A keyswitch click is a DC pulse with a duration of 5 msec. A two-level volume control is also provided by the microprocessor. All of these audio sounds and the volume control are under program control.

FUSE

There is no external fuse on ATL terminals. In the event of an overload, a crowbar circuit in the power supply interrupts the AC current. If this happens, it is essential that the power switch be turned off as soon as possible to prevent burning out the crowbar circuit. Remedy the cause of the overload and turn the terminal on again.

There is an internal fuse in the power supply. This fuse is used to protect the unit in the event that the crowbar circuit has engaged and the terminal has not been powered off at the switch for some time. If this fuse blows, the entire power supply must be replaced. See the power supply functional description for more details.

CONNECTORS

ATL terminals have two types of connectors on the rear panel: the power cord connector and the communications cable connectors. The number, type and purpose of the communications cable connectors depend on the type of terminal and the communications options selected. See the corresponding logic board communications section for more information.

VENTILATION

ATL terminals are cooled by convection. This means that air enters through the bottom, side and rear vents to cool the circuitry, and leaves through the top vents. There is no fan. Care must be taken not to cover the vents in the top, back, sides and bottom of the terminal. Even a sheet of paper inadvertently placed on top of the terminal will impede air flow and result in overheating and failure.

HARDWARE DESCRIPTION

ATL terminals consist of a display screen and a detachable keyboard. The screen housing may be rotated and tilted. The screen enclosure contains the power supply, monitor circuitry, and logic board. The logic board contains the CPU, memory, communications controller, and video controller. The keyboard is connected to the screen enclosure by a coiled cable. The keyboard enclosure contains a printed circuit card with the keyboard CPU, clock, ROM, and keyswitches.

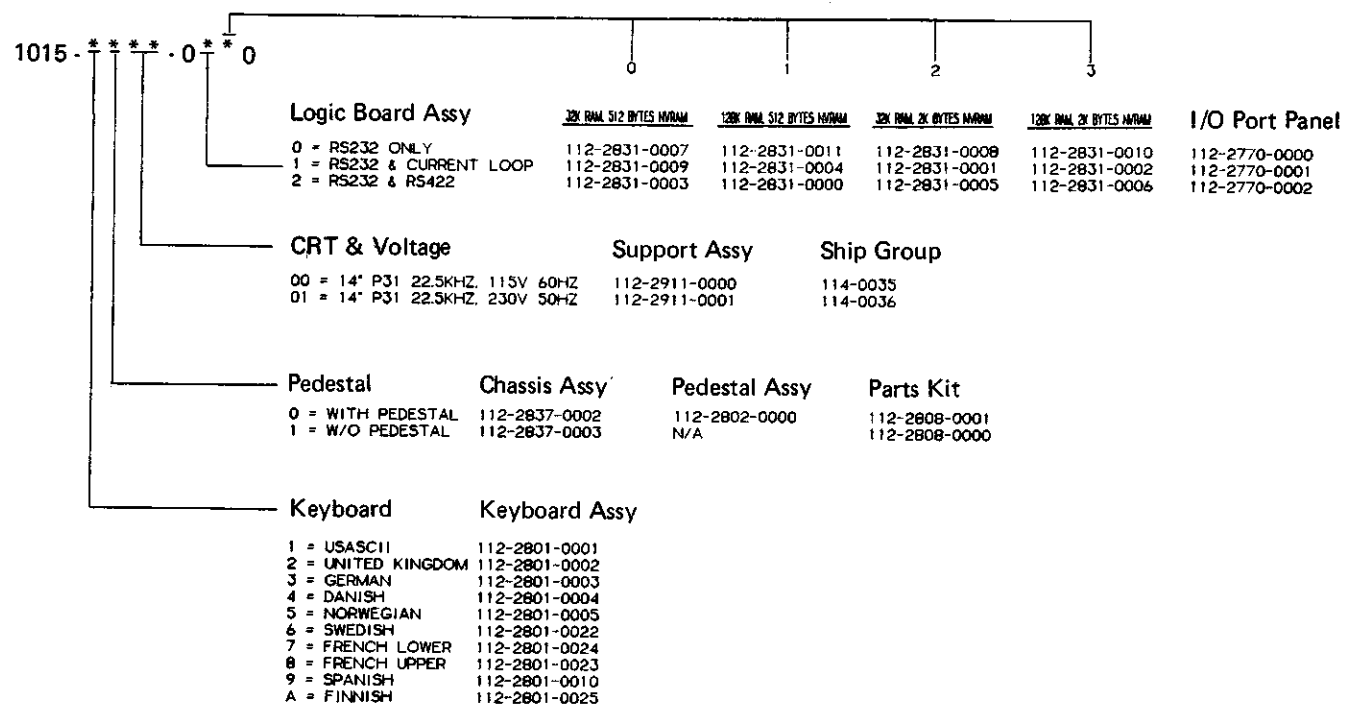
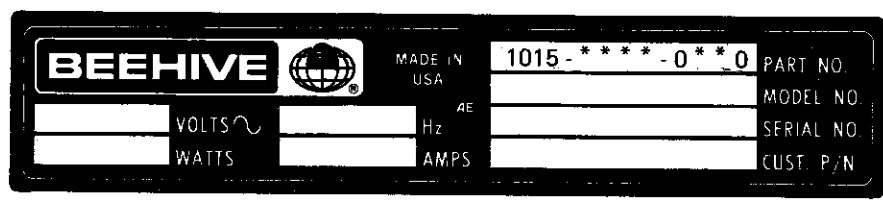
Identification of Optional Components

There are several options available for ATL-008 terminals. The logic board offers three communications options and four memory options. The monitor offers a choice of voltage and display phosphor (B/W or green). The screen

enclosure may be ordered with or without the pedestal. The keyboard may be ordered for eleven different national character sets. The part number on the rear panel is the key to determining which of these options were chosen when a terminal was delivered.

The part number consists of three groups of four digits each. The digits of the last two groups are significant for identifying optional components. See Table 1-1.

Table 1-1
ATL-008 Optional
Component
Identification



Internal Cabling

ATL terminals use three types of internal cables. Ribbon cables connect the logic board to the power supply and to the monitor board. The keyboard cable jack is connected to the logic board by eight small wires. A wire harness connects the monitor board to the CRT yoke; another harness connects the CRT neck socket to the monitor board. Several wires are used to ground the various subassemblies.

The ribbon cable from the power supply to the logic board carries the three voltages needed on the logic board, +5V, $\pm 12V$. The ribbon cable from the logic board to the monitor board provides the signals needed to drive the monitor board. The wires to the keyboard jack carry power, ground, and character information between the logic board and the keyboard. The wires between the monitor board and the CRT neck are color-coded with the corresponding color written on the monitor board. See the ATL-008 schematic in the drawings section.

Power Supply

The 40W ATL power supply is an offline flyback converter that provides three DC outputs: +5V at 2.5 amps, +12V at 2.0 amps, and -12V at 0.25 amps, from a single 115V/230V AC line. The power supply is constructed on a single PC board measuring 6.0 in. \times 3.7 in. \times 1.7 in. It is designed to be cooled by convection in an operating range of 0°C to 60°C.

Monitor

The ATL-008 terminal uses a 90°/20MM, TTL-compatible display requiring separate video, horizontal sync and vertical sync inputs. The +12V monitor operating voltage is supplied through the input signal connector. There is also a provision to connect an external brightness control through the same input signal connector. ATL terminals utilize this feature to provide a contrast control in TCM. The monitor consists of a Printed Circuit Board (PCB) assembly and a Cathode Ray Tube (CRT) assembly. The monitor screen is covered by a nylon mesh anti-glare screen.

Keyboard

The ATL terminal keyboard is a low-profile, detachable, intelligent serial unit. It complies with the DIN specification that the home row keys be 30mm above the work surface and that the keyboard be inclined at an angle between 7 and 11 degrees.

Scanning circuitry is based on the P8039-6 microprocessor and an external 2716 ROM. The microprocessor communicates data between the 94 keystation matrix and the main terminal processor over a 9600 baud bidirectional, full duplex serial link.

Logic Board

The ATL-008 terminal logic board contains the terminal microprocessor, communications circuitry, memory, and video control circuitry. The 68008 microprocessor allows the use of an 8-bit data bus. It controls the system operation by executing instructions read from the program memory. The 8530 Serial Communications Controller (SCC) is a dual channel, full duplex, multi-protocol data communications peripheral which functions as a serial-to-parallel, parallel-to-serial converter/controller. The 8041/8741 is a Universal Peripheral Interface (UPI), designed as a general purpose programmable interface device compatible with a variety of microprocessor systems. It functions basically as an intelligent UART to reduce overhead for the 8039 microprocessor on the keyboard and to provide certain status information about the main and aux ports.

The ATL-008 memory consists of dynamic RAM, static RAM, ROM, and EEPROM. The standard ATL-008 has 32K bytes of DRAM, which is upgradable to 128K bytes. The video section is comprised of a CRT controller, a video attribute controller, four 1K \times 4 bit static RAMs, and a clock generation circuit.

2

ON-SITE MAINTENANCE AND REPAIR

GENERAL INFORMATION

Section two contains information concerning the maintenance and repair of ATL terminals. It begins with some information on warranty provisions, then discusses the operating environment (ventilation considerations, power, etc.). It also illustrates potential shock hazards and lists the tools and test equipment required for board-level troubleshooting and repair. Finally, this section details the failures that can occur and gives illustrated instructions for removing and replacing subassemblies.

Warranty Provisions

Limited warranty information is provided in the appropriate ATL technical user's manual. Warranties can vary considerably in accordance with specific purchase or lease agreements, so check your contract or contact your distributor for details.

Operating Environment

Terminal Placement - ATL terminals are designed to function in a wide variety of office settings, and will provide good service if given the care normally afforded a valued office machine. Position the terminal (including the keyboard) so that it is not in danger of being dropped or otherwise harmed. Be sure to provide adequate room for ventilation—position the terminal so that it has a minimum of 3.5 inches of clearance on all sides.

Temperature and Humidity - Extremes in temperature or humidity can shorten the life of almost any electronic component. They can lead to malfunction or damage of solid state devices, changes in value in passive components, and many other reliability problems. ATL terminals may be operated when the temperature and humidity do not exceed the ranges specified in the appropriate technical user's manual. If the operating environment exceeds these ranges, the terminal should be shut off until the situation is corrected.

Ventilation and Contaminants

ATL terminals are cooled by convection. This means that most of the ATL terminal's case consists of cooling vents. Great care must be taken to avoid spilling liquids into the terminal. Common substances such as coffee, soft drinks, cigarette ash and dust can cause problems with proper heat dissipation if they are spilled onto the circuit components. In extreme cases, such substances can cause short circuits resulting in erratic operation or damage to the terminal.

Preventing contamination is much easier than correcting it. Keep food, drink and smoking materials away from the terminal. Wipe off any spilled substances with a soft, dry cloth.

In areas where airborne dust or other contaminants are unavoidable, it is a good idea to cover the terminal when it is not in use. *Be sure to remove the cover each time the terminal is turned on or overheating can occur. Remember, there is no fan and the cooling vents must be unobstructed.*

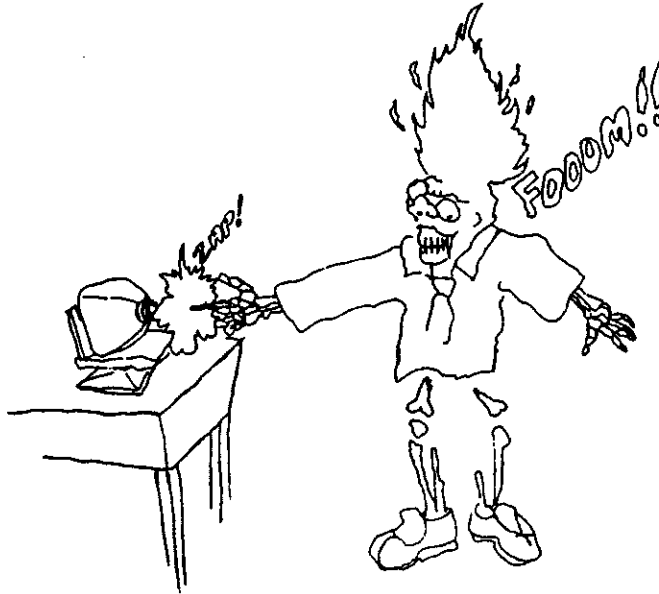
AC Power

The AC power line voltage may vary $\pm 15\%$ from the 115V or 230V that is specified for the terminal. The AC line frequency, however, must not vary more than $\pm 5\%$ from the required 50 or 60 Hz. AC supplied to the terminal should be as free as possible from spikes, noise, and other transient problems.

Potential Hazards

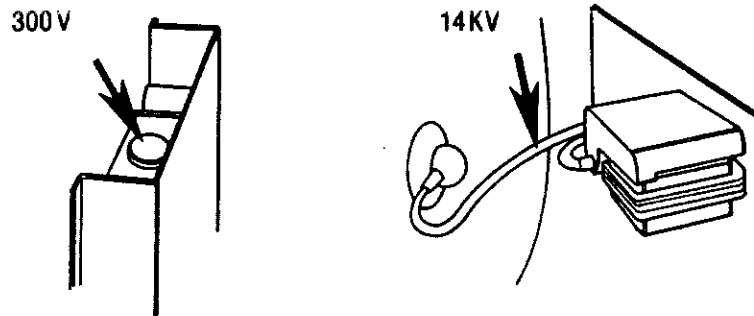
Electric Shock — Potentially **LETHAL** voltages are present at several points in the terminal. See Figure 2-1.

Figure 2-1
Electrified
Electronic
Technician



Take great care to become familiar with these areas and exercise caution. The power supply power transistor produces a 300V signal. The monitor flyback (CRT anode) voltage is approximately 14KV. See Figure 2-2.

Figure 2-2
Voltage Hazards



Tools and Test Equipment

ATL terminals have been designed to be easily and rapidly serviced in the field. Disassembly, board-level troubleshooting, and reassembly require a few hand tools and test devices. The following tools are needed:

Test Equipment

- Digital multimeter
- Tektronics 465 oscilloscope (or equivalent)

Tools

- Antistatic mat with wrist strap
- Medium flat-bladed screwdriver
- Long flat-bladed screwdriver with grounding jumper
- Phillips screwdriver
- Nut driver set
- Adjustable wrench
- Pliers
- Safety goggles

PROBLEM DIAGNOSIS

This section describes procedures for determining the cause of a problem at the board level. A complete set of illustrated instructions for disassembly and replacement of each of the major subassemblies is contained in the next section. Use this section to determine the cause of the problem, then refer to the disassembly instructions to see how to replace the faulty board. This section assumes that the cover has been removed.

The normal power-up sequence is:

- Turn on the terminal.
- It should beep once, but the screen remains blank.
- After 35 to 40 seconds, it will beep again.
- The terminal will display the results of the selftest.

There are four types of problems that can occur: functional failures, video failures, communications failures, and keyboard failures. A functional failure means that the terminal will not power up. A video failure means that the terminal seems to power up (it beeps normally), but the resulting video is incorrect. A communications failure means that the terminal does not communicate with the host in a normal fashion. A keyboard failure means that the keyboard does not function.

General

All repairs to ATL terminals should be effected on an antistatic mat with a conductive wrist strap in use. An inspection of the interior of the terminal may reveal the cause of a problem:

- Check for loose wires that have come unsoldered.
- Be sure that the power supply and monitor board ribbon cables and the CRT neck connectors are firmly seated. Check the connections with the power off.
- ATL terminals have a large number of socketed chips on the logic board. Due to the nature of sockets, it is always a good idea to check the seating of all socketed chips before attempting additional troubleshooting. With the power off, gently press each socketed chip.
- It is also a good idea to check the obvious things like power, keyboard, and communications cable connections.

Functional Failures

The most probable cause of a functional failure is a faulty power supply. If the terminal does not beep normally during power-up, then the logic board is probably not receiving the correct voltages from the power supply. This may result from two causes: either the power supply input voltage is incorrect or the power supply is malfunctioning.

Check for the obvious problem of an unplugged terminal. If the terminal is plugged in, check the input voltage and compare it to the voltage given on the terminal identification plate on the back panel to make sure the power supply and the line voltage are compatible.

If the line voltage is correct, check the output voltages from the power supply. These voltages are -12 , $+12$, and $+5$ VDC. Three capacitors near the power supply ribbon cable connector on the logic board are the best places to check these voltages. These three capacitors are identified by the numbers C29, C30, and C31 on the logic board. Figure 2-3 illustrates the relative positions of these capacitors. Compare the measured voltages with those given in Table 2-1. If the measured values are outside the acceptable ranges, replace the power supply.

Figure 2-3
Power Supply
Output Voltage
Locations

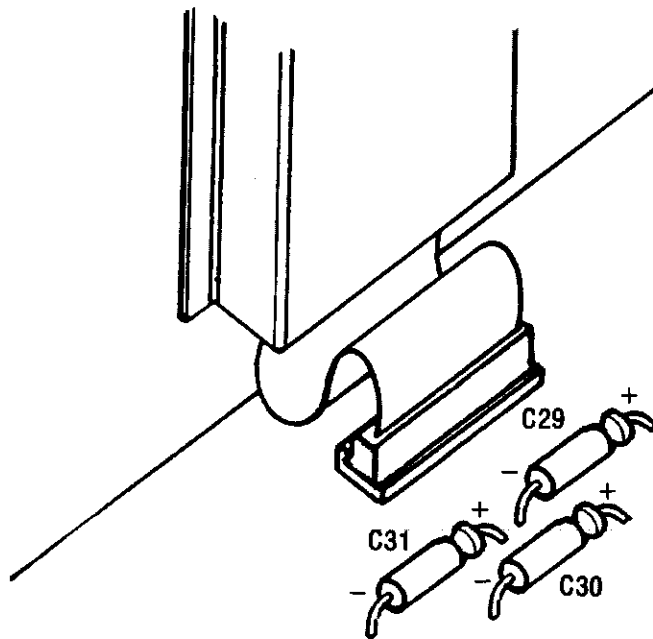
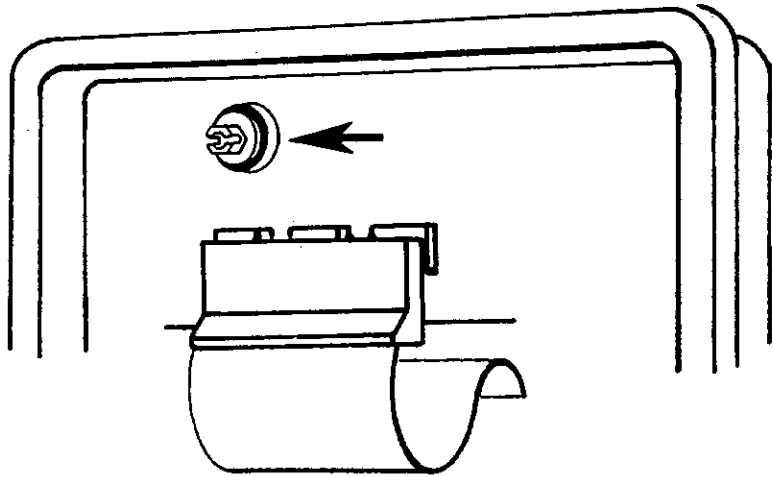


Table 2-1
Power Supply
Output Voltages

VOLTAGE	ACCEPTABLE RANGE	LOCATION
+5V	+4.95V to +5.25V	C29 (positive side)
+12V	+11.4V to +12.6V	C30 (positive side)
-12V	-13.8V to -10.8V	C31 (negative side)

If the $+5$ VDC output drops below 4.85 V (approximately), it will trip the reset circuit. The $+5$ volt supply may be adjusted slightly by tweeking a pot on the power supply printed circuit card. Locate the adjustment pot through the access hole in the side support. It is located immediately above the ribbon cable and requires a small flat-bladed tool. Figure 2-4 illustrates the pot.

Figure 2-4
+5VDC
Adjustment Pot



**M
&
R**

Video Failures

A video failure means that the video output is incorrect. It does not mean that bad data is visible on the screen. Bad data means that there are readable characters on the screen, even if they are not the expected characters. Bad video means that the characters (if any) are not readable. Bad data results from either a communications failure or from a bad logic board. This section deals only with bad video, not bad data.

If the terminal beeps correctly during the power-up sequence but the video is bad, one of three things is happening:

- The logic board is not sending the correct +12VDC, video, horizontal sync, and vertical sync signals to the monitor card, resulting in bad video. If this is the case, replace the logic card.
- The logic board is sending the correct +12VDC, video, horizontal sync, and vertical sync signals to the monitor card, but the monitor card produces bad video. If this is the case, replace the monitor card.
- The cable between the logic card and the monitor card is bad. Check it for shorts and continuity.

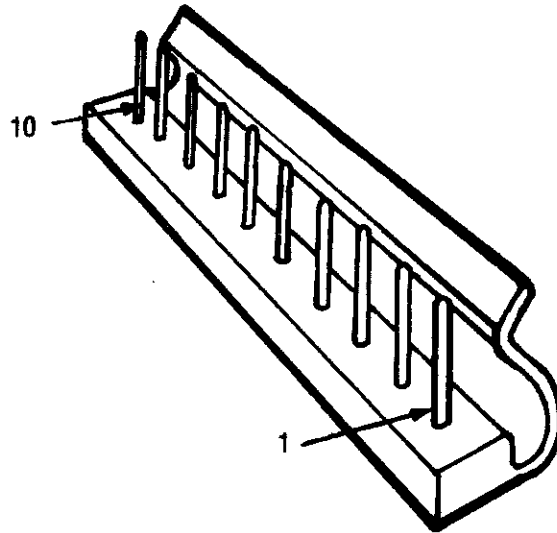
Check the video output signals from the logic board with an oscilloscope. Check the +12VDC signal from the logic board with a voltmeter. The output signals from the logic card to the monitor card are listed in Table 2-2.

Table 2-2
Logic Board Video
Output Signals

SIGNAL	LOCATION
Video	Pin 8
Horizontal Sync	Pin 6
Vertical Sync	Pin 9
+12VDC	Pin 7

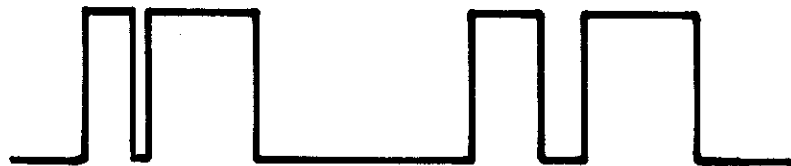
All locations refer to the monitor card ribbon cable connector on the logic board. Pin 1 is closest to the back panel of the terminal and the pins are numbered sequentially as illustrated in Figure 2-5.

Figure 2-5
Logic Card Ribbon
Cable Connector to
Monitor Card



The signals are illustrated in Figures 2-6 through 2-8. Signals may vary slightly from the illustrations, but they should be similar.

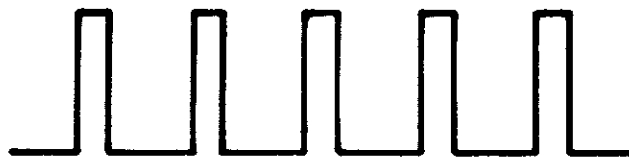
Figure 2-6
Video Output from
Logic Card (Pin 1)



.5 millisecond timebase, 2 volts per vertical division

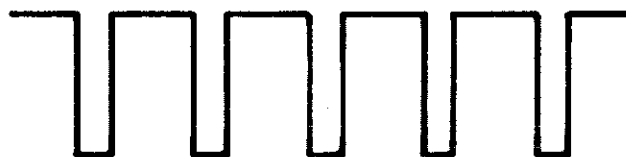
(This illustration shows the video corresponding to the selftest report and the status lines—other displays will have correspondingly different video patterns.)

Figure 2-7
Horizontal Sync
Output from Logic
Card (Pin 6)



20 microsecond timebase, 2 volts per vertical division

Figure 2-8
Vertical Sync Output
from Logic Card
(Pin 9)



5 millisecond timebase, 2 volts per vertical division

Communications Failures

Communications failures may result from three sources:

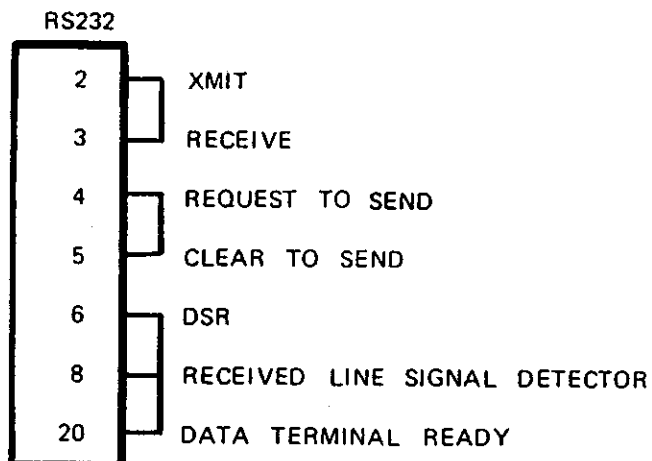
- Incorrect Terminal Configuration Manager settings.
- Faulty modem or line.
- Faulty logic card.

Verify that the TCM settings are correct for the particular installation. Place the terminal online. If the TCM settings are correct and the terminal does not communicate, check the problem port to determine if the source of the problem is the logic card or some external factor.

Main Port RS232 - Pin 2 carries the transmitted data. Connect Pin 2 to an oscilloscope and press a few keys. If the logic board data transmitter section is functioning properly, you will see a momentary change in the scope display. RS232 voltage levels should change from -12VDC to $+12\text{VDC}$. If the oscilloscope shows no change, then the logic board should be replaced. If the scope shows the correct voltage difference and the terminal is not communicating properly, then the problem is caused by some external factor (host, data line, or modem).

Check the logic board RS232 receivers by looping Pin 2 to Pin 3 with the terminal online, Auto Echo off, and full duplex set. Figure 2-9 shows how to build a loopback connector for this test. Type a few keys; the characters should be transmitted out Pin 2, received at Pin 3, and displayed on the screen. If they are not, then replace the logic board.

Figure 2-9
RS232 Loopback
Test Connector

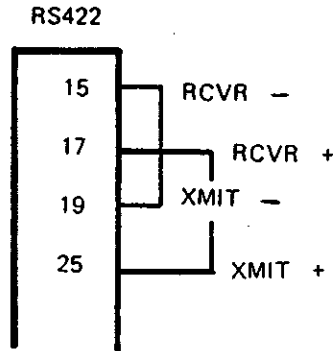


Aux Port RS232 - Pin 3 carries transmitted data from the terminal. Connect Pin 3 to an oscilloscope and press a few keys. If the logic board data transmitter section is functioning properly, you will see a momentary change in the scope display. RS232 voltage levels should change from -12VDC to $+12\text{VDC}$. If the oscilloscope shows no change, then the logic board should be replaced. If the scope shows the correct voltage difference and the terminal is not communicating properly, then the problem is caused by some external factor (host, data line, or modem).

Check the logic board RS232 receivers by looping Pin 3 to Pin 2 with the terminal online, Auto Echo off, and full duplex enabled. The same loopback connector illustrated in Figure 2-9 may be used. Type a few keys; the characters should be transmitted out Pin 3, received at Pin 2, and displayed on the screen. If they are not, then replace the logic board.

Main Port RS422 - Install a loopback test connector constructed as illustrated in Figure 2-10 to test the transmitters and receivers simultaneously. Type a few characters. If they appear on the screen, the port is functioning correctly and the problem is due to some other part of the communications connection. If they do not, replace the logic board.

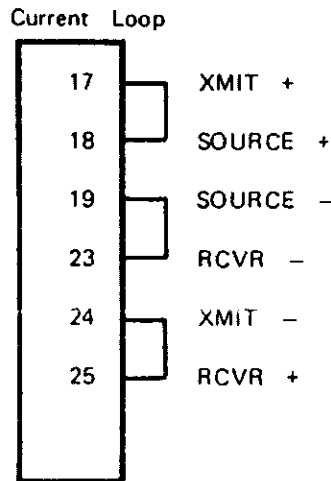
Figure 2-10
Main Port RS422
Loopback Test
Connector



Pin 4 is the RECEIVE DATA line. Monitor the communication by connecting an oscilloscope to Pin 4. The signal should change from -6VDC to +6VDC.

20 mA Current Loop - Connect a loopback test connector constructed as illustrated in Figure 2-11. Type a few characters. If they appear on the screen, the port is functioning correctly and the problem is due to some other part of the communications connection. If they do not, replace the logic board.

Figure 2-11
20 mA Current Loop
Loopback Test
Connector



Pin 2 is the TRANSMIT MINUS line. Monitor the communication by connecting an oscilloscope with a current probe to Pin 2. The current should change from 0 to 20 mA. If the oscilloscope shows no change, then the logic board should be replaced.

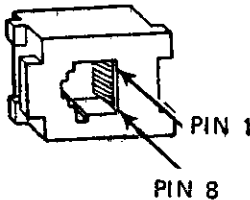
KEYBOARD FAILURES

If the power supply, logic board, and monitor board are all functioning properly, and typing on the keyboard produces no characters on the screen, the problem may stem from three sources:

- The terminal is online and disconnected from the host.
- The logic board is not supplying the correct power to the keyboard.
- The cable from the keyboard to the terminal is faulty.
- The keyboard is faulty.

Check for the first problem by placing the terminal offline. Turn the terminal on and press the EXTENDED screenkey, then press the OFFLINE screenkey. This will put the terminal offline. Type a few characters. If the keyboard does not work, then one of the other problems is the difficulty. Put the terminal online again. If the keyboard does not work, but it worked when the terminal was offline, check for communications problems.

Check the small wires from the keyboard jack to the logic board for apparent damage. Check the voltages on the orange wire, Pin 7 of the keyboard jack. The orange wire carries +12VDC. If this voltage is not present, replace the logic board because it is not supplying the correct power to the keyboard.



Checking for a faulty keyboard cable involves checking each end of the cable for the correct voltages. The preceding paragraph contains instructions for checking the logic board end of the cable. Check the keyboard end by taking the keyboard apart and checking the incoming power regulator for correct voltages from the logic board to the keyboard. It is located at the upper left corner of the keyboard printed circuit. Pin 1 carries +12VDC, Pin 3 carries Ground, and Pin 2 carries +5VDC. The pins are numbered from bottom to top. If the voltages are good at the keyboard jack on the logic board and bad at the regulator, replace the cable.

Check the keyboard function by checking the RECEIVE and XMIT DATA lines of the microprocessor in the keyboard. Pin 39 is the RECEIVE DATA signal; Pin 38 is XMIT DATA. (These signals are also present on Pins 3 and 5 of the keyboard cable connectors.) Connect an oscilloscope to each pin in turn and press a few keys. You should see a momentary change in the scope display. If the display does not change, replace the keyboard.

SUBASSEMBLY REPLACEMENT

Tools and Tips

Read this section completely before disassembly. It gives step-by-step illustrations and descriptions of removal and replacement of ATL terminal subassemblies, with helpful hints pertaining to each subassembly.

Each of the procedures that follow gives a list of tools needed to perform that particular procedure. The following list is a comprehensive list of all tools needed to replace ATL subassemblies.

- Medium flat-bladed screwdriver
- Long flat-bladed screwdriver with grounding jumper
- Phillips screwdriver
- Nut driver set
- Adjustable wrench
- Pliers
- Safety goggles

Use an antistatic mat to protect sensitive integrated circuits. Effect all repairs in a well-lit work area with enough room to accommodate the terminal and the subassemblies being removed. Tilting the screen can sometimes make repairs easier.

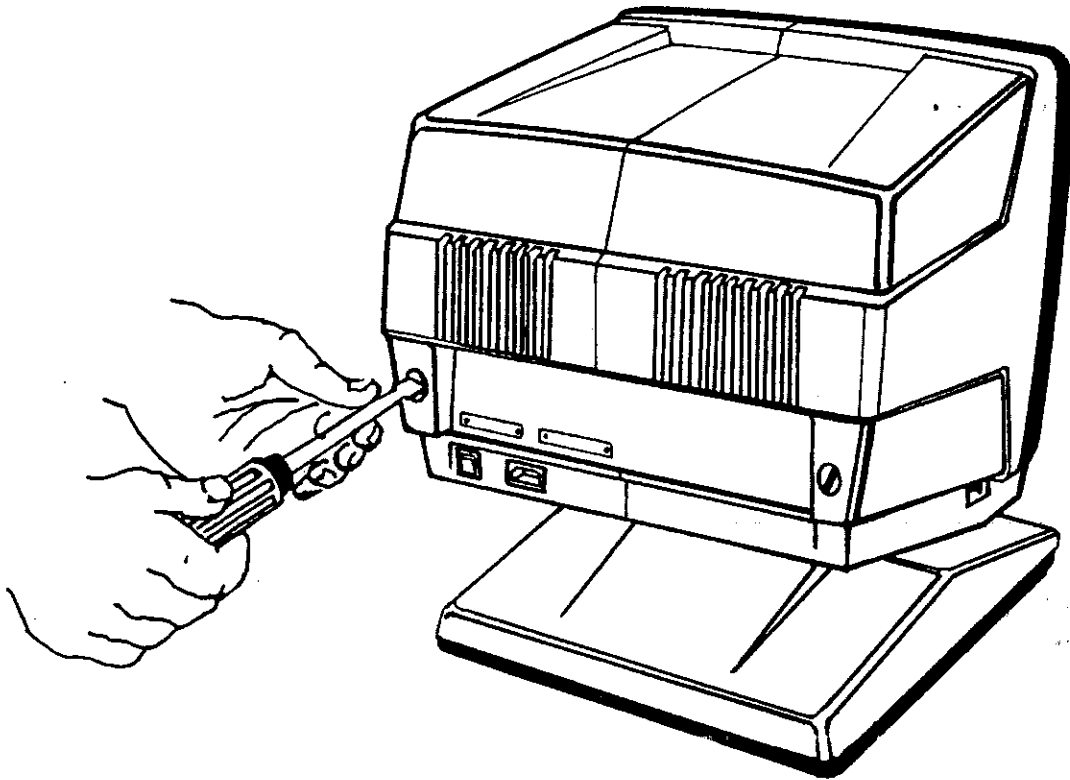
In general, reassembly is the reverse process of disassembly; the last portion of each procedure lists any exceptions to this as well as details that make reassembly easier.

Removing and Replacing the Cover

The only tool needed to remove and replace the cover is a medium flat-bladed screwdriver.

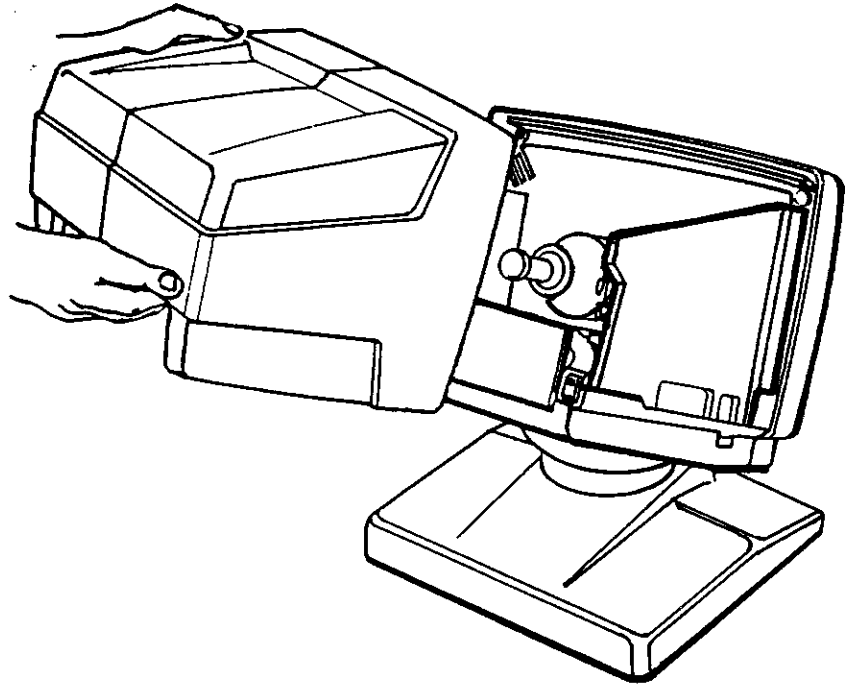
Before any of the subassemblies except the keyboard are serviced, the rear cover must be removed as follows:

1. Turn the terminal off and remove the power cord from the rear panel. You may also wish to remove the strain relief from the bottom of the terminal if it has been installed.

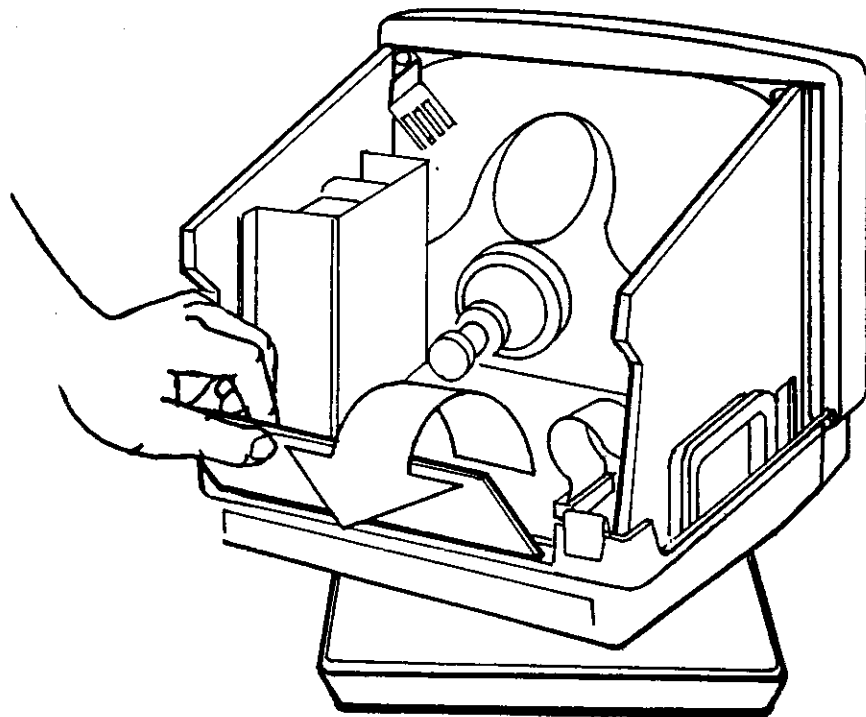


2. Remove the two cover retaining screws with a flat-bladed screwdriver.

3. Slide the cover away from the front bezel and take it off of the terminal. ATL covers fit quite tightly. It may be necessary to use a bit of force to remove the cover. Just remember that this is a sensitive piece of equipment—crowbars, jackhammers and hydraulic rams are not needed. Your bare hands should suffice.

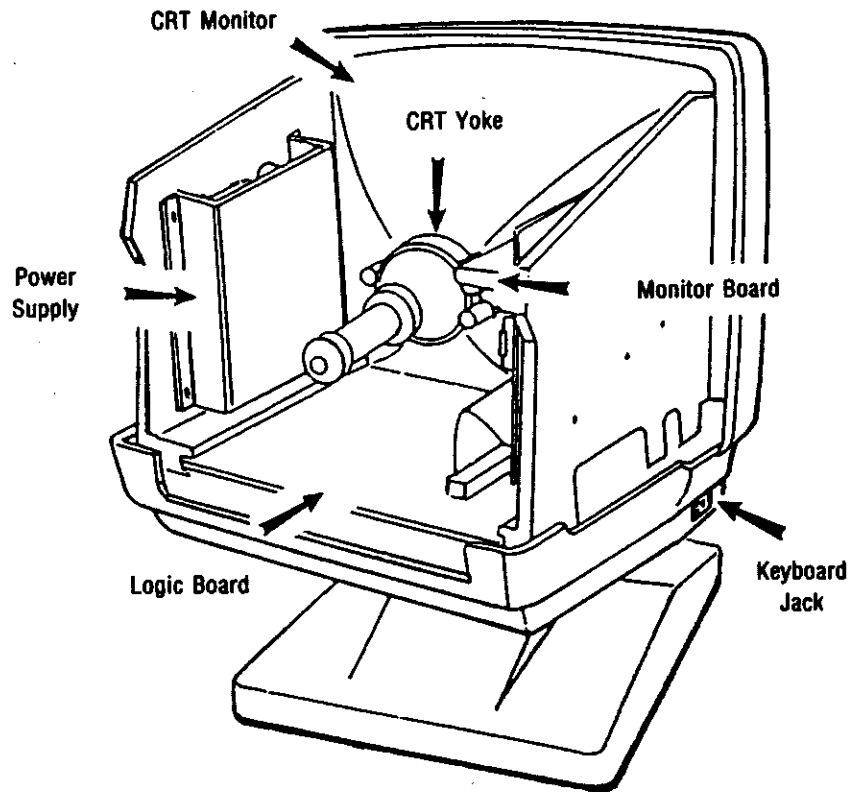


4. Tilt the rear panel as illustrated and lift it out of the groove that it normally occupies. It may usually be left attached by its ground wire.



2
0
3

Once the cover is off, the remaining subassemblies of the screen enclosure are readily identified as in this illustration:



Replacing the cover is the reverse process. The only difficulty that may occur is the proper alignment of the cover with the front bezel. Be sure that they are aligned as you slide the cover back on and you should not have any trouble.

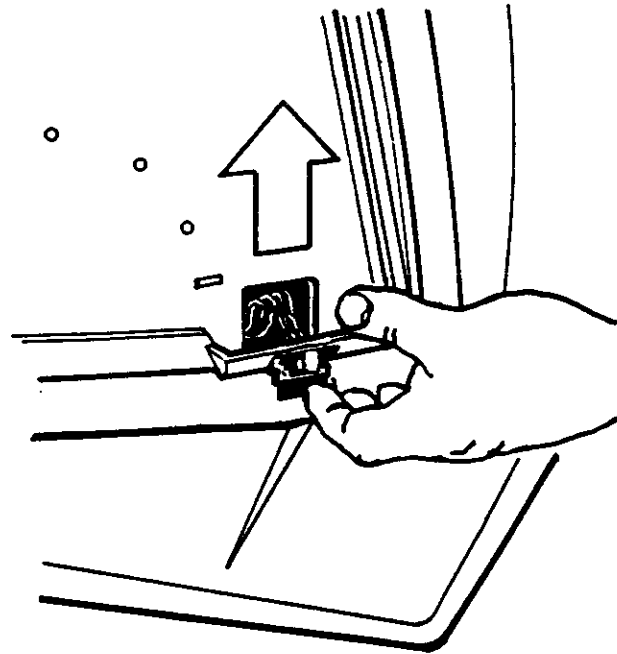
Before replacing the cover, make a final inspection of all wires and cables to be sure that everything is properly connected.

Removing and Replacing the Logic Board

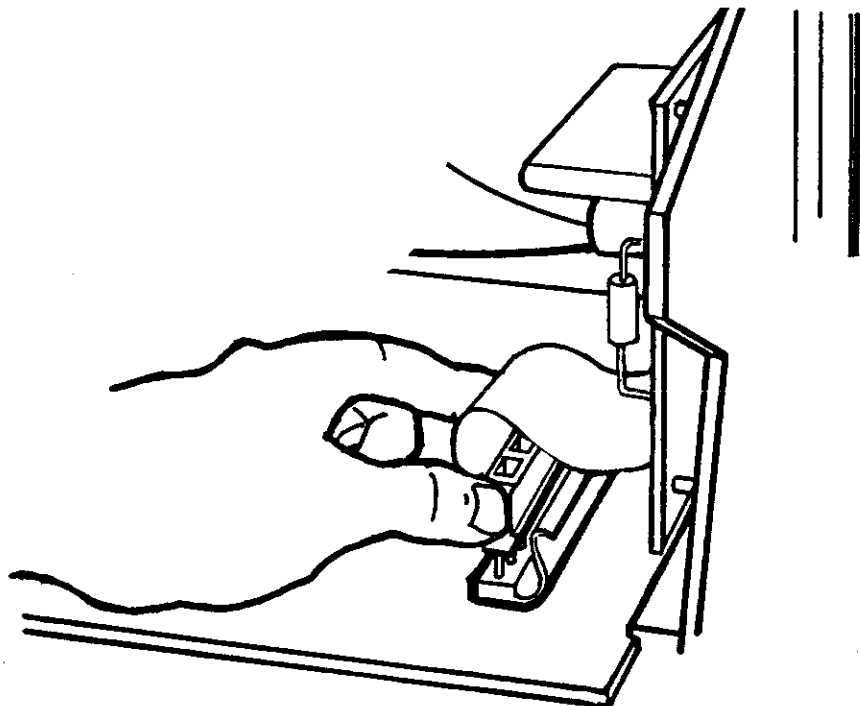
The logic board may be removed with no tools other than your bare hands; however, a medium flat-bladed screwdriver may be useful in separating cable connectors.

This section assumes that the keyboard cable has been unplugged from the side of the screen enclosure (it works like a telephone jack) and that the rear cover has been removed. The logic board has four connections to the rest of the ATL terminal. Disconnect them as follows:

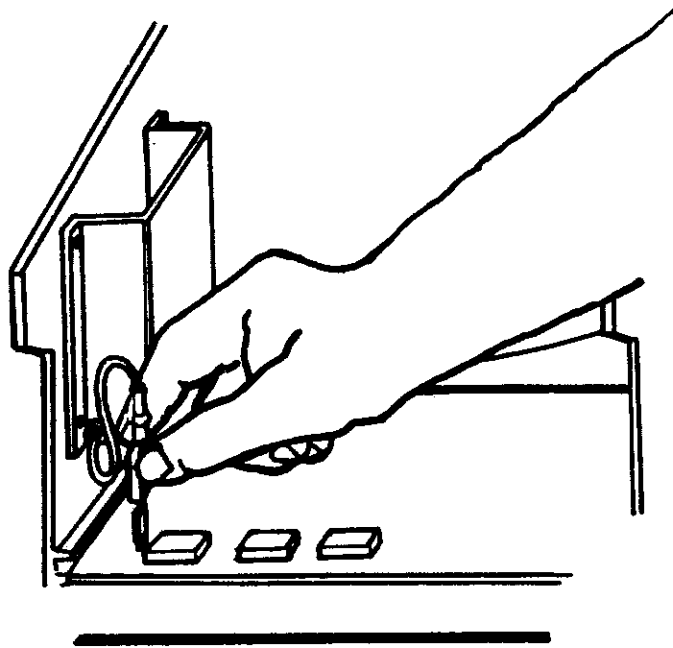
1. Push up on the keyboard cable jack as shown here and tuck it and its connecting wires inside the terminal so that the cable jack rests on the logic board.



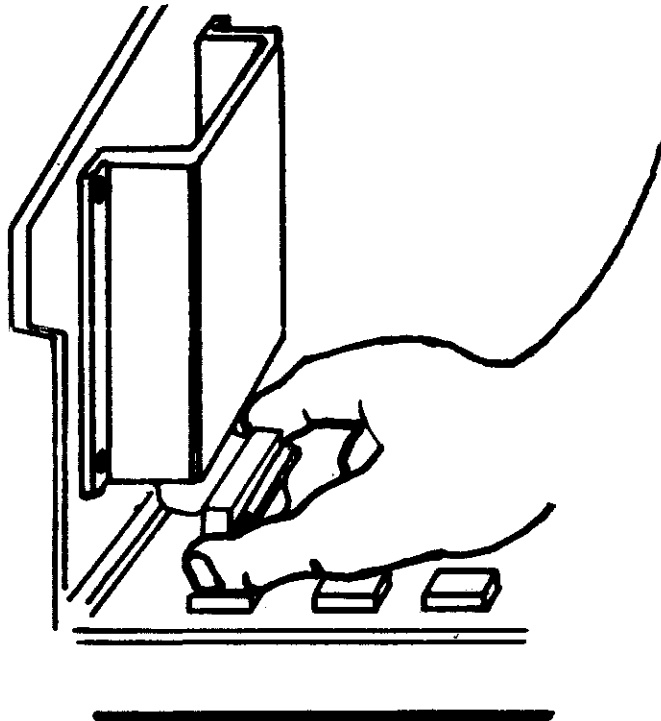
2. Disconnect the ribbon cable from the monitor board at the logic board as shown, lift it up and loop it over one of the wires between the yoke and the monitor board so that it does not snag on any of the logic board components when the board is removed. When reconnecting this cable, be sure to unhook it from the yoke wires first to avoid damage to the fragile neck of the CRT.



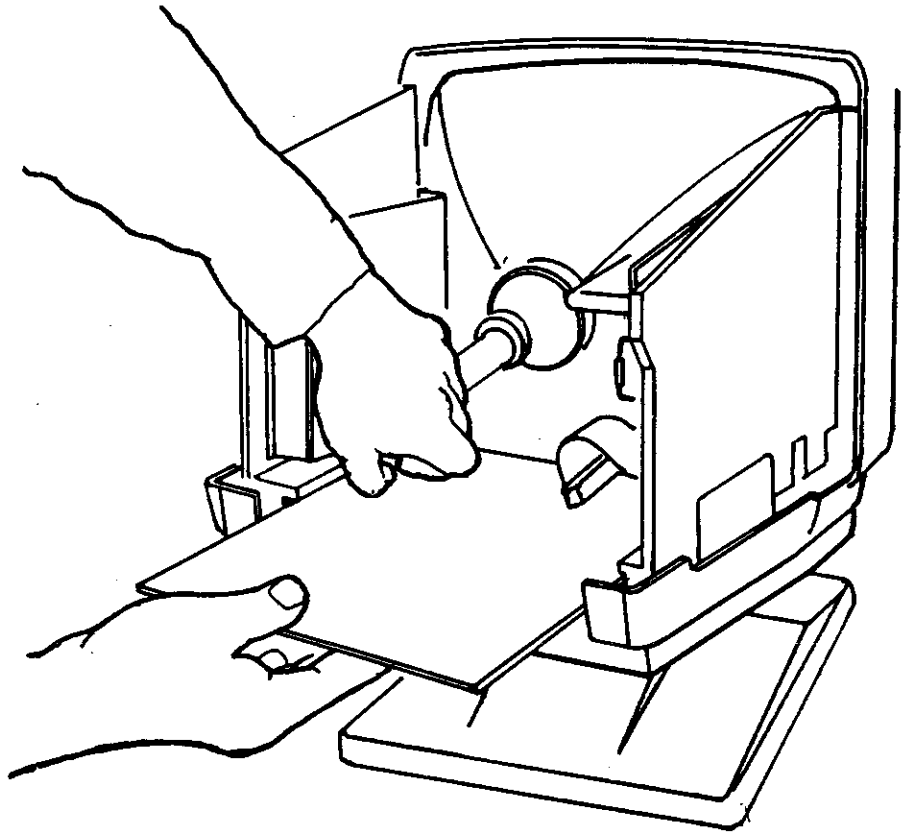
3. Disconnect the ground wire from the logic board to the power supply. Unplug the connector at the logic board as shown.



4. Disconnect the ribbon cable from the power supply at the logic board. Disconnect it at the logic board like this:



5. Hold the power supply ribbon cable so that it does not snag on any of the logic components and slide the logic board out. Take care not to snag the keyboard cable jack and wires.



To replace the logic board, reverse the procedure. The ribbon cable from the power supply is the trickiest to reconnect because of the limited amount of room between the power supply and the logic board. If you hooked the monitor board ribbon cable over a yoke wire during disassembly, be sure to unhook it before reconnecting it to the logic board.

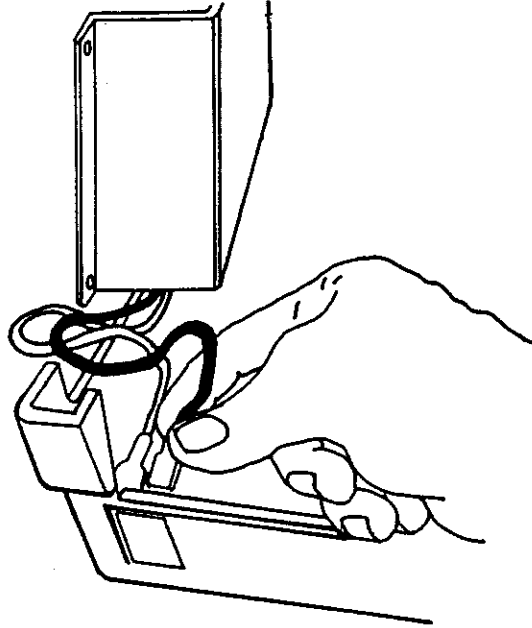
Removing and Replacing the Power Supply

This procedure requires the following tools and parts:

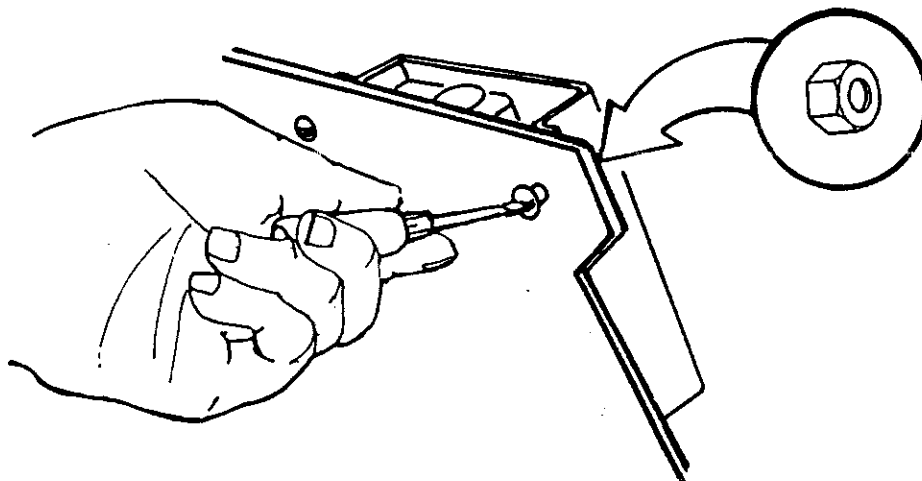
- Medium flat-bladed screwdriver
- Nut driver set

This section assumes that the logic board has been removed. The power supply is the only subassembly that requires prior removal of another subassembly; the monitor and monitor board do not require removal of the logic board.

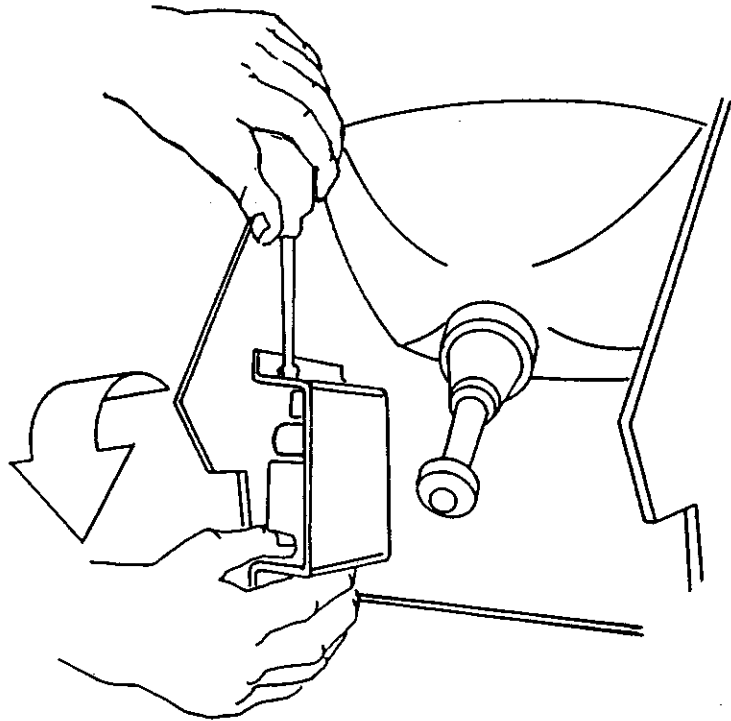
1. The logic board must be removed to expose the wires that connect the power supply to the on/off switch located on the rear panel below the power supply. They are connected with spade connectors as shown. Unclip the connectors from the switch. Note that the blue wire is on the left side of the switch and the brown wire is on the right side of the switch (when viewed from the back of the terminal) as shown.



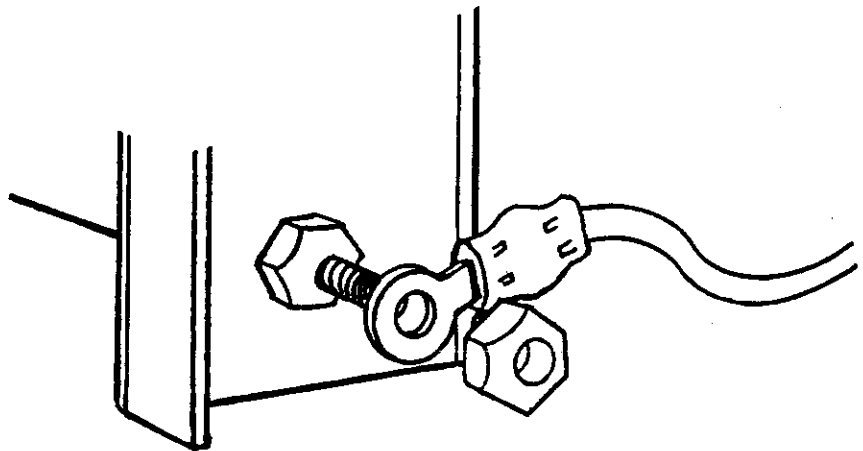
2. The power supply chassis is supported by two flanges on the lower corners and by two screws on the upper corners. Remove the screws.



3. Tilt the power supply away from the side support and remove the ground wires from the top and bottom of the power supply.



4. Remove the power supply while threading the wires to the on/off switch through the side support and around the circuit board guide slots. Note the routing of these wires; it is important that they be routed in the same fashion during reassembly.



Installation of a new power supply is the reverse of this procedure. The wires to the on/off switch must be threaded through the side support and under the guides for the circuit boards.

Removing and Replacing the Monitor Board and Yoke

This procedure requires the following tools:

Long flat-bladed screwdriver
Grounding jumper wire
Phillips screwdriver
Safety goggles

This section assumes prior removal of the cover. Removal of other sub-assemblies is not required.

DANGER



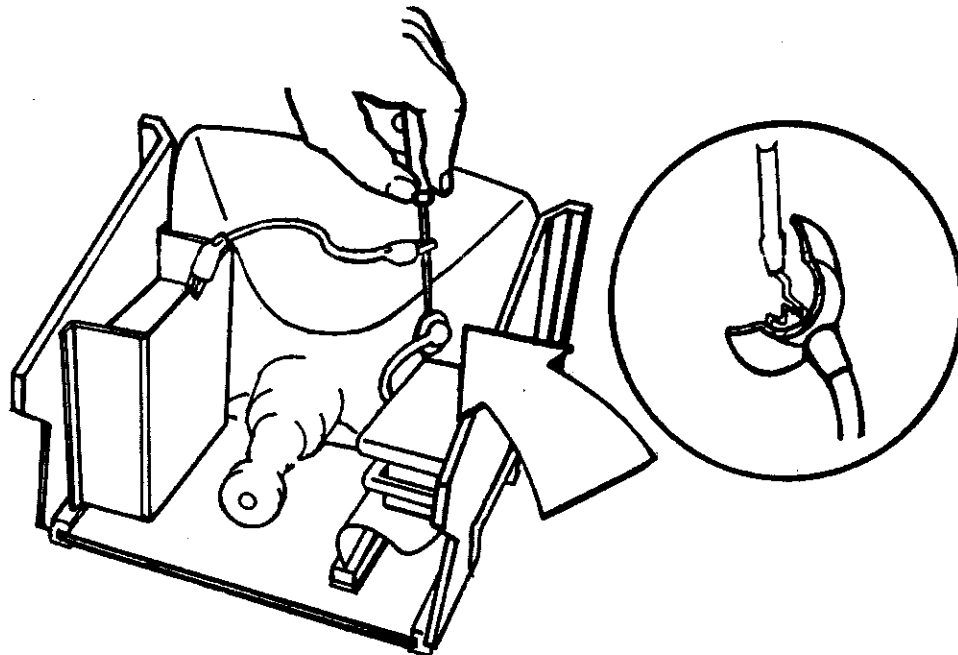
This procedure involves dealing with the high-voltage connection between the monitor board and the CRT. On ATL terminals, this connection carries about 14KV. This voltage is stored in the CRT even after the terminal has been turned off and the power cord has been removed. Unless you have just removed the charge, assume it to be present.

DANGER

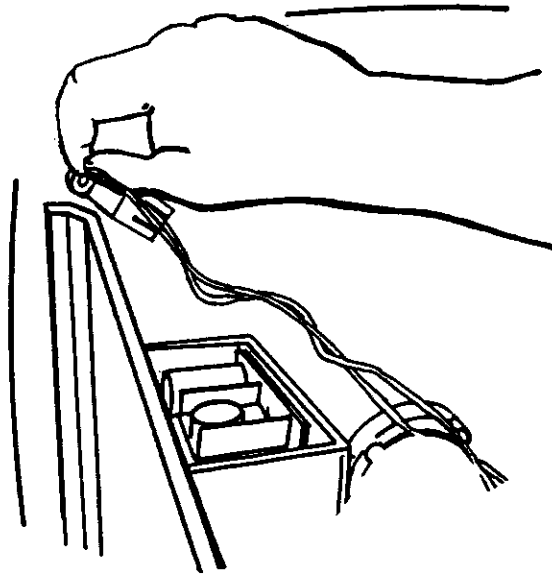


If the glass case of the CRT is damaged, the CRT may implode, resulting in danger from flying glass. Wear safety goggles during this procedure.

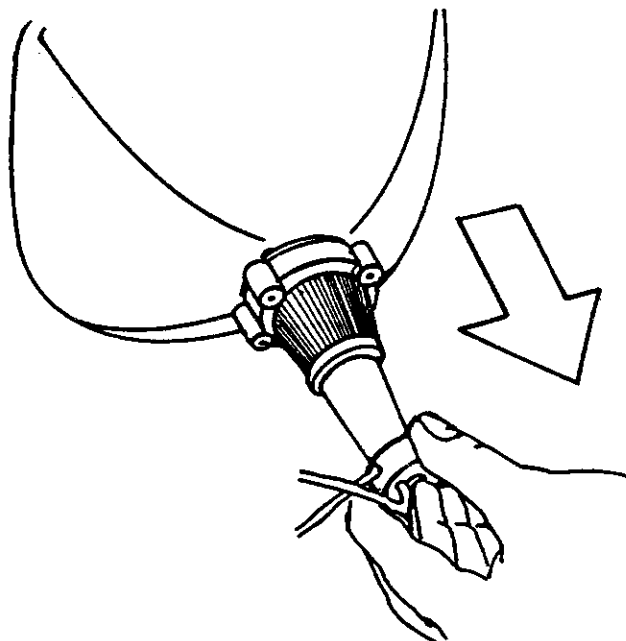
1. To remove the charge from the CRT, connect a jumper wire between a long, flat-bladed insulated screwdriver and ground, insert the tip of the screwdriver under the rubber boot on the side of the CRT and touch the flyback transformer lead with the tip of the screwdriver. It is best that this be done with only one hand so that you do not inadvertently touch the metal portion of the screwdriver or the exposed lead. Handle only the insulated portion of the screwdriver. You will hear a popping sound and may see a spark. This indicates that the charge has been at least partially removed. Part of the charge can still be present so exercise caution. To remove as much of the charge as possible, ground the flyback lead repeatedly until there is no spark or pop.



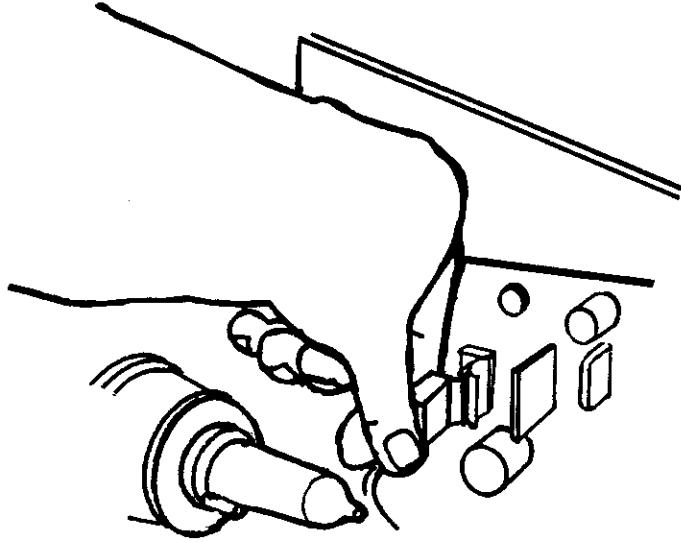
2. Use the same grounded screwdriver to compress the flyback lead spring and remove the lead and the rubber boot. Reconnecting this lead during reassembly is easier if you fold the rubber boot back on the lead wire and compress the spring lead with a screwdriver while reinserting it into the CRT.
3. Remove the ground wire that connects the monitor board to the CRT DAG clip. It is connected with a spade connector.



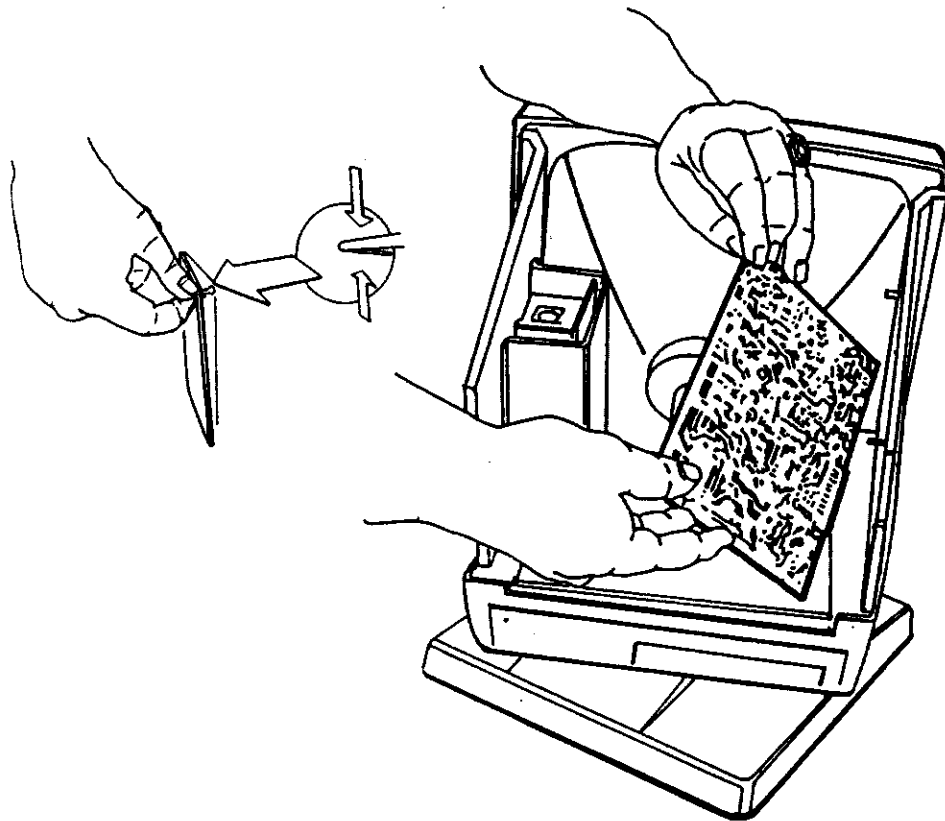
4. Remove the connector from the neck of the CRT. The neck is very fragile; take care not to damage it. Heed the warning about flying glass.



5. There are several wires from the CRT yoke to a connector on the monitor board. Remove the connector from the monitor board.

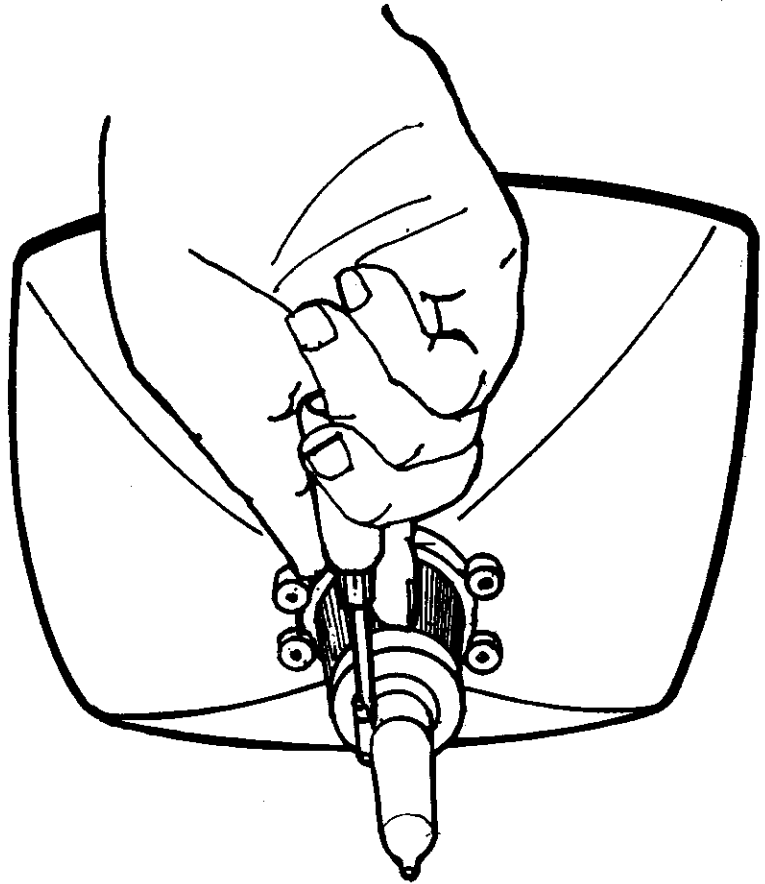


6. The monitor board is supported by two flanges on the lower corners and by two plastic standoffs on the upper corners. Pinch the standoffs as shown,



tilt the monitor board away from the side support and remove it, taking care not to tangle the ground and neck connector wires. If you are only removing the monitor board and do not need to remove the yoke, this is the final step.

7. Loosen the yoke clamp screw (the larger of the two screws on the yoke assembly). Slide the yoke off of the neck of the CRT.



The monitor board is reinstalled by reversing this procedure. Take care when replacing the neck connector. Reinstall the flyback lead by folding the rubber boot back on itself as much as possible and insert one side of the spring in the CRT, then press the spring together with the screwdriver and push it into the CRT.

When reinstalling the yoke, it will be necessary to adjust it with power on so that the raster is properly aligned. This is done by placing the yoke on the neck, aligning it visually and tightening the clamp slightly so that the yoke may still turn on the neck. Make all connections and turn on the terminal. While watching the screen, turn the yoke until the raster is horizontal and tighten the clamp. Take care not to over-tighten the clamp — remember the fragility of the neck. You only need to tighten the clamp enough to prevent the yoke from turning.

Removing and Replacing the Monitor CRT

This procedure requires the following tools:

- Long flat-bladed screwdriver with grounding jumper
- Phillips screwdriver
- Nut driver set
- Adjustable wrench
- Pliers
- Safety goggles

This section assumes prior removal of the cover. Removal of other sub-assemblies is not required; however, the monitor board must be disconnected from the CRT. This is accomplished by undoing all connections between the monitor board and the CRT as described in the previous procedure *Removing and Replacing the Monitor Board and Yoke*. The connections that must be removed are the flyback lead, DAG ground wire, neck connector, and CRT yoke connector.

DANGER



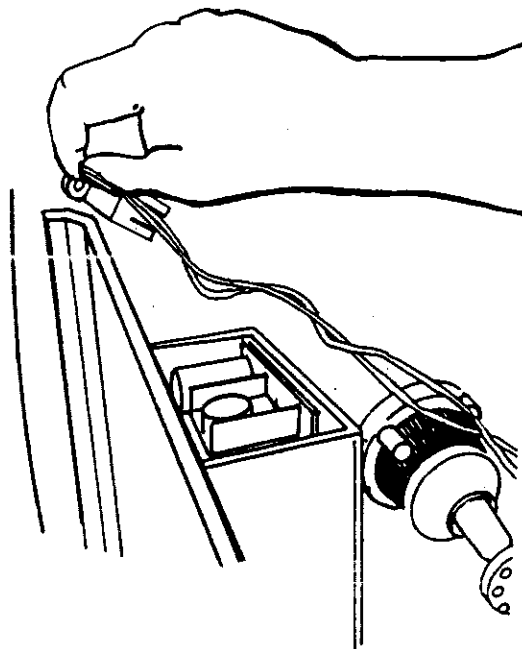
This procedure involves dealing with the high-voltage connection between the monitor board and the CRT. On ATL terminals, this connection carries about 14KV. This voltage is stored in the CRT even after the terminal has been turned off and the power cord has been removed. Unless you have just removed the charge, assume it to be present.

DANGER

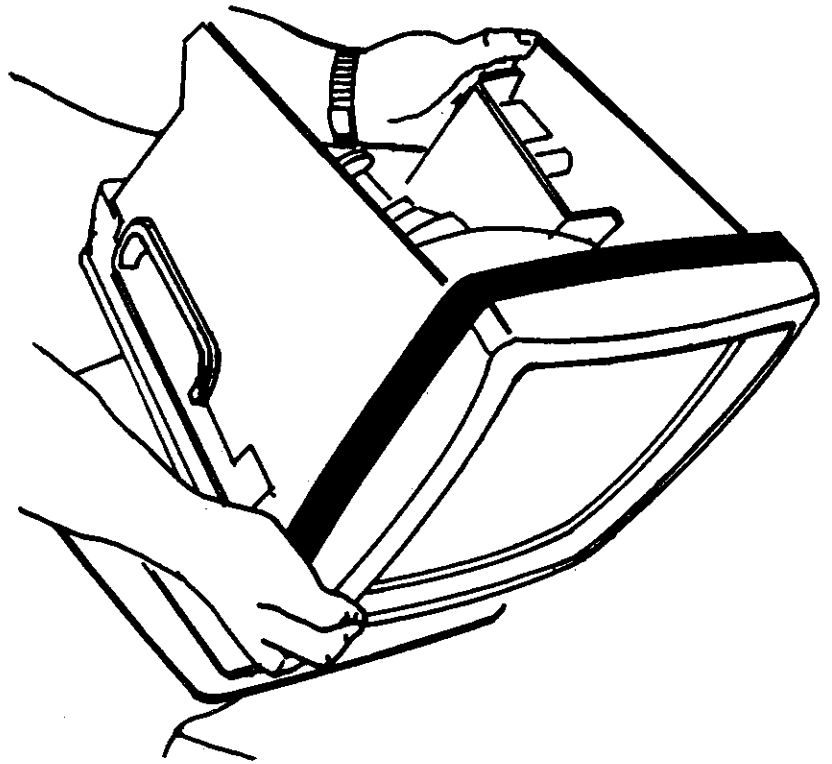


If the glass case of the CRT is damaged, the CRT may implode, resulting in danger from flying glass. Wear safety goggles during this procedure.

1. After disconnecting the monitor board from the CRT, remove the ground wire between the power supply and the CRT. It is connected with a spade connector.

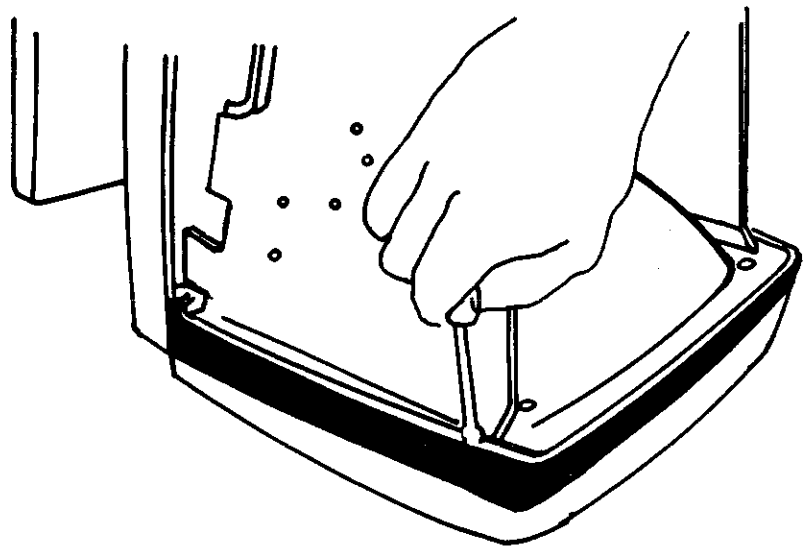


2. Place the screen face down on a soft pad, like this:

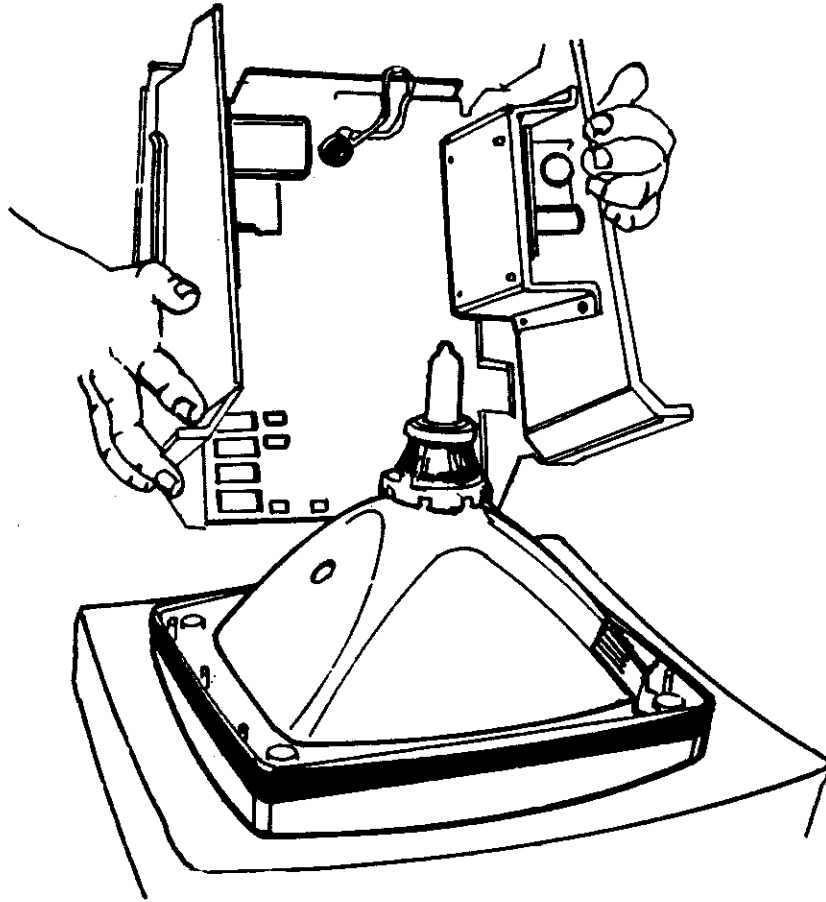


FOR

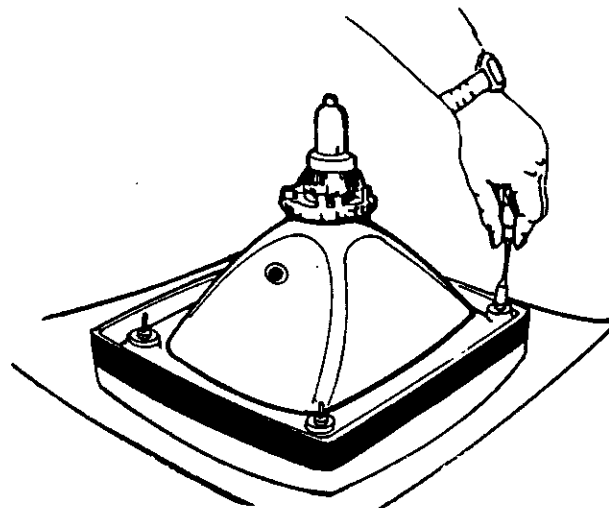
3. Remove the six screws that hold the CRT frame to the side supports.



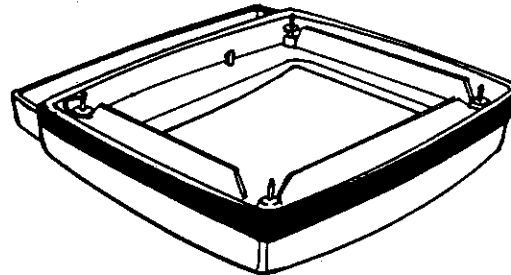
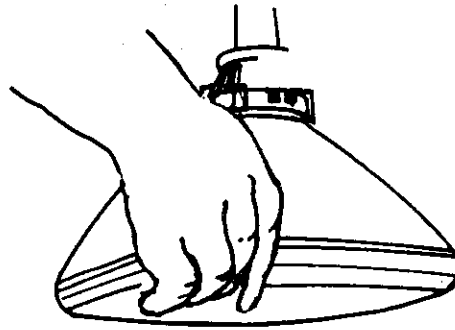
4. Lift off the chassis leaving the CRT and frame on the pad.



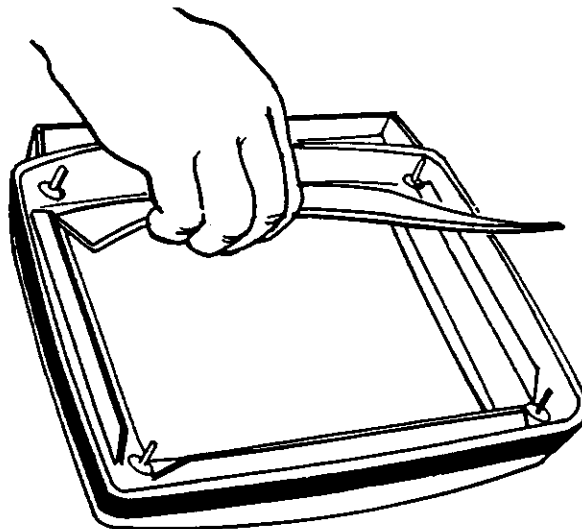
5. Remove the four nuts that hold the CRT frame to the front bezel. Note the position of the DAG clip relative to the flyback connector hole; this will serve to orient the new CRT to the rest of the terminal. Remove the DAG clip. When reinstalling the CRT, be sure to put the DAG clip on the same corner. If the studs turn when you use a nut driver on the nuts, use an adjustable wrench instead of the nut driver and hold the end of the stud with pliers or a special socket.



6. Lift the CRT out of the bezel.



7. The nylon anti-glare screen may be removed from the bezel for cleaning if necessary. During reassembly, be sure that the new CRT screen is clean and that no dirt is trapped between the nylon screen and the CRT glass surface. Dirt trapped between them causes the nylon screen to wrinkle.



There are two possible problems associated with replacing the CRT. They both have to do with the nylon anti-glare screen. The first problem is that of dirt trapped between the nylon mesh and the glass CRT screen. This may be avoided by cleaning the CRT immediately prior to installation.

The second problem involves adjusting the distance between the two screens. This problem usually occurs only when the bezel is being replaced; normally the factory adjustment is adequate. The four mounting studs that fasten the CRT to the front bezel are used for this purpose. The studs are threaded on both ends. The larger end fits into the bezel. The smaller end fits through a mounting tab on the CRT and has a star-shaped end. This star-shaped portion allows you to turn the entire stud with special socket or a pair of pliers.

It also allows you to hold the stud while tightening the nut that fastens the CRT tab to the bezel (this is why the tool list includes the pliers and an adjustable wrench). Turn all four studs completely into the bezel, then back them out half a turn, and attach the CRT. The remainder of the reassembly is the reverse of the removal procedure.

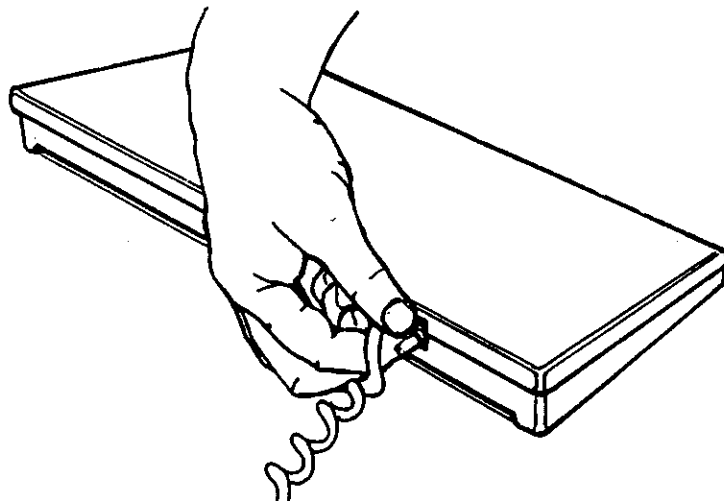
If the replacement CRT does not have a yoke assembly you will also have to remove the yoke from the malfunctioning CRT and replace it on the new CRT. The preceding section, *Removing and Replacing the Monitor Board and Yoke*, shows how to do this.

Removing and Replacing the Keyboard

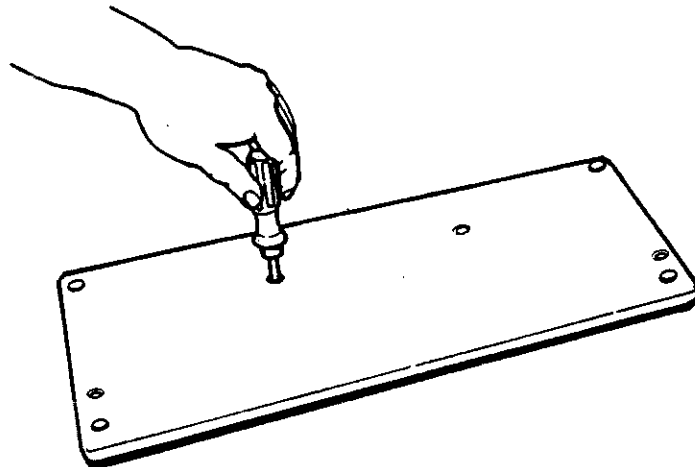
You will need a medium Phillips screwdriver for this procedure.

The keyboard enclosure is held together with four screws through the bottom of the case. It comes apart as follows:

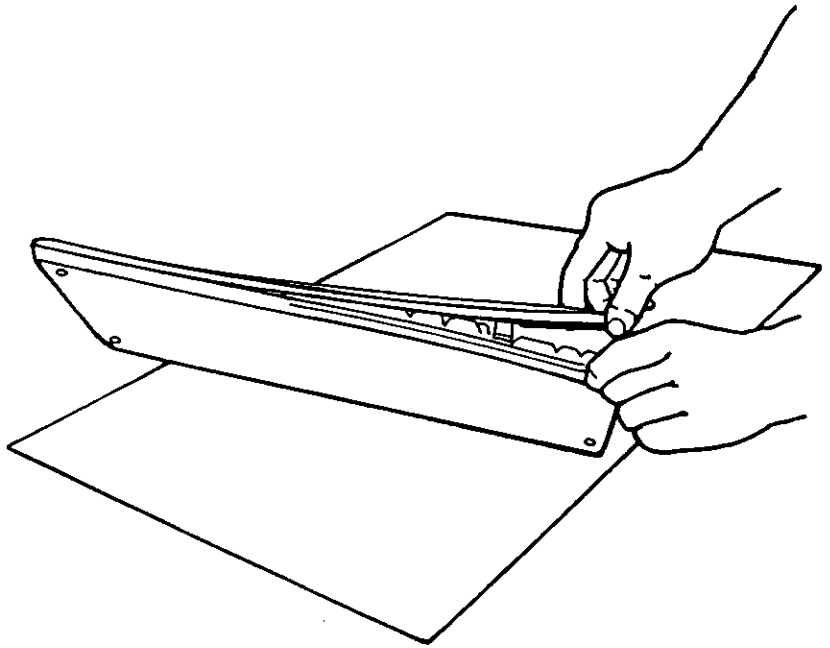
1. Unplug the keyboard cord. It works like a telephone jack.



2. Turn the keyboard over and remove the four screws. Then turn the case right side up.

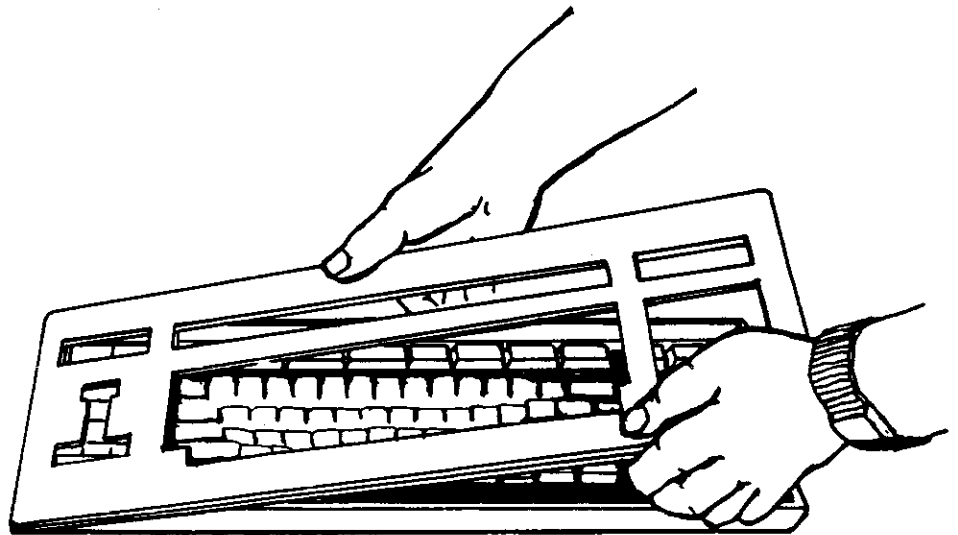


3. At this point, the keyboard is still held together by plastic catches inside the case. Carefully pry the cover open.

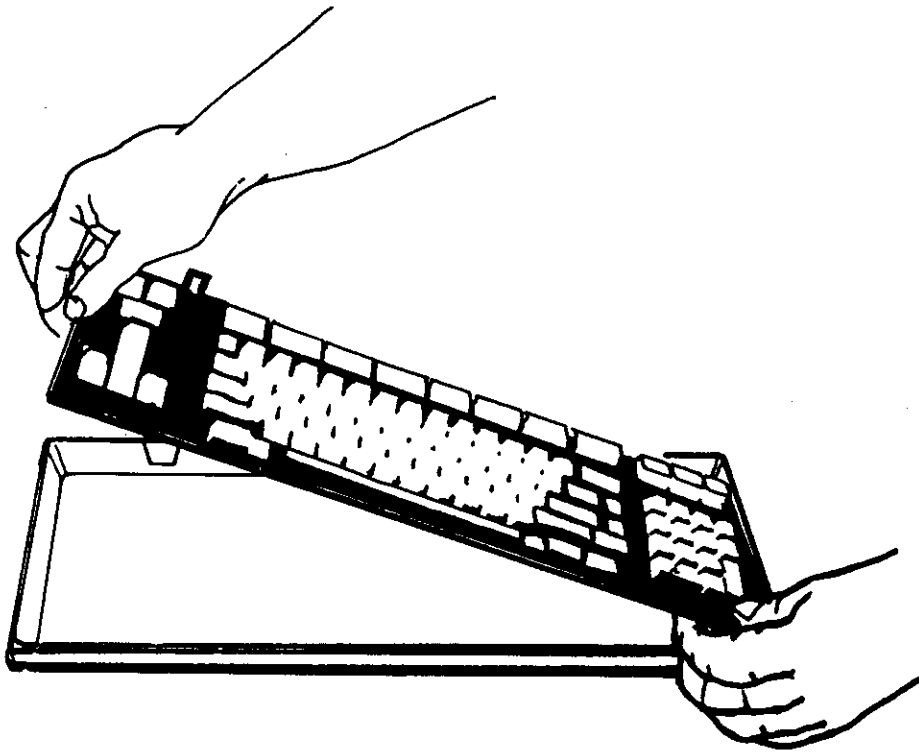


M
E
R

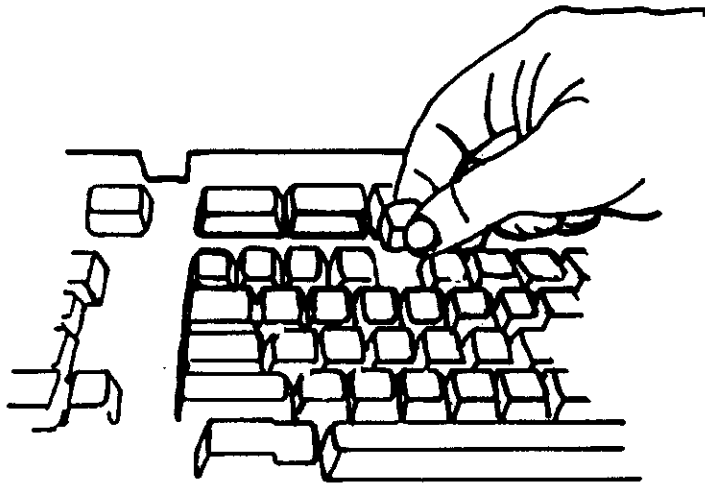
4. Lift off the top cover.



5. Lift out the keyboard printed circuit. Some keyboards have a sheet of insulating paper under the printed circuit. Take care not to damage it so that it may be reassembled intact.



6. Most keycaps pull off easily. Larger ones are fastened with a wire clip.



Reverse this process to replace the keyboard. Take care to adjust the keyboard printed circuit board in the case so that the keys do not bind on the edges of the openings in the top cover, then tighten the four screws.

3

ATL POWER SUPPLY FUNCTIONAL DESCRIPTION

GENERAL

The 40W ATL power supply is an offline flyback converter that provides three DC outputs—+5V at 2.5 amps, +12V at 2.0 amps, and -12V at 0.25 amps—from a single 115V/230V AC line. The power supply is constructed on a single PC board measuring 6.0 in. × 3.7 in. × 1.7 in. It is designed to be cooled by convection in an operating range of 0°C to 60°C.

The power supply should not be left connected to the input line voltage without a load on the outputs. Some sort of load should be maintained during testing to prevent burning out the power supply.

FUNCTION

Offline input voltage is applied to the power supply by line, neutral, and ground inputs. A 2-ohm fuse resistor provides primary over-current protection and limits the primary input surge current during cold start-up. An EMI filter consisting of four capacitors and a ballun provides common and normal filtering between the supply and the AC line. The input line at this point is rectified and filtered to provide a nominal ± 160 VDC primary rail voltage.

Q1, Q2, and T1 form the major components of a self-excited blocking oscillator. An RCL diode network provides sufficient base current to start the main switch transistor Q1 into conduction. Regenerative feedback is derived from a tertiary winding in phase with the primary of transformer T1 and applied through an RC network to saturate Q1 during 50% of the cycle. Q1 is turned off by either the over-current protection circuit or the opto-coupler depending on whether the supply is in initial start-up or normal operation. Once Q2 is turned off, the secondary rectifier diodes become forward biased and the energy stored in the transformer is delivered to the secondary output filters and load.

Secondary voltage control is sensed off the 5VDC output. This voltage is divided down and applied to the sense pin of a 2.5V shunt regulator. When the 5V output reaches the threshold, the regulator conducts causing the photodiode to conduct which in turn causes Q1 to turn off. The PNP transistor then shunts the shunt regulator, insuring that during start-up, the photo-transistor is conducting when Q1 is turned off.

Over-voltage protection is provided in the event that the loop fails to regulate the 5V output. A crowbar SCR conducts between the 5V output Zener threshold voltage and the SCR gate to the cathode threshold to prevent damage to the logic load. This in turn causes an over-current condition and resets the power supply. If the condition persists, the power supply will again reset.

4

ATL-008 MONITOR FUNCTIONAL DESCRIPTION

GENERAL

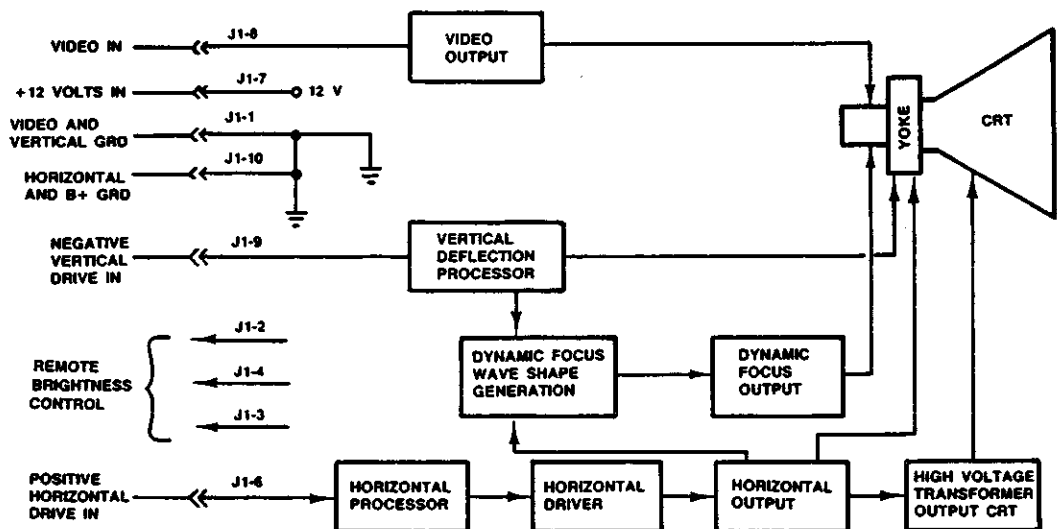
The ATL-008 terminal uses a 90°/20MM, TTL-compatible display requiring separate video, horizontal sync and vertical sync inputs. The +12V monitor operating voltage is supplied through the input signal connector. There is also a provision to connect an external brightness control through the same input signal connector on Pins 2, 3 and 4. The monitor consists of two major assemblies:

1. Printed Circuit Board (PCB) Assembly
2. Cathode Ray Tube (CRT) Assembly

PRINTED CIRCUIT BOARD ASSEMBLY

The PCB contains all the monitor electronics. The PCB assembly consists of a video amplifier, a vertical processing stage and a four-stage horizontal deflection circuit. Refer to Figure 4-1, ATL-008 Monitor Board Block Diagram, for the relationship between these four sections. Refer to Drawing EL112-2919-*, ATL-008 Monitor Schematic, for component identification.

Figure 4-1
Monitor Board
Block Diagram



Video Amplifier

The two-stage video amplifier consists primarily of Q101 and Q102. Q101 is connected in the common base configuration; Q102 is connected in the common emitter configuration. Together they form a cascode arrangement. This minimizes the Miller effect input capacitance and the breakdown voltage parameter of Q101.

The video amplifier accepts a TTL-compatible, non-composite, positive-going video input signal to produce the CRT cathode signal. R102 and R106 fix the gain of the amplifier at about 20dB. C103 and L101 are used for high frequency peaking to give a bandwidth of about 26MHz. R103 and R104 are limiting resistors to protect Q101 and Q102 from source spikes. R105 is a terminating resistor used to minimize frequency limiting effects of input cable capacitance. A buffering resistor is used in the CRT socket assembly.

In the absence of a video signal, transistor Q101 is non-conducting, thereby turning transistor Q102 off. This gives the same voltage at the CRT cathode as the video supply voltage. The threshold voltage needed to turn on Q101 is one PN-junction voltage (approximately 0.6V). Once this threshold is passed, the amplifier operates in linear mode. 3.6V P-P at the input results in a CRT drive voltage of approximately 28V P-P. This drive voltage provides a video light output of approximately 15 foot-lamberts. Adjusting this voltage adjusts the screen intensity. R101 and C102 provide additional filtering of the video supply voltage.

Horizontal Deflection

The horizontal deflection circuit consists of four distinct sections:

- Horizontal Processor
- Horizontal Driver
- Horizontal Output
- High Voltage Transformer

Horizontal Processor - The horizontal processor circuit consists of a monostable multivibrator circuit (a one-shot) in Q301 and Q302 and an MC1391 horizontal processor, A301, along with their associated circuitry. The horizontal sync pulse is coupled to the base of Q301 through C301 and R301. The output of the multivibrator is differentiated by R310 and C304 and fed to the sync input of A301. R305, R306, C302 and R302 control the timing of the multivibrator pulse between 1 and 12 microseconds.

A301 contains an oscillator, a predriver and a phase detector. R326, R327, R328 and C321 control the RC type oscillator. The sawtooth output of the oscillator goes through a predriver in the MC1391 and comes out on Pin 1 of A301 as a rectangular pulse. This output is coupled through R322 to the base of Q303.

A negative-going sync pulse at the sync input (Pin 3) of A301 allows the phase detector of A301 to compare the phase relationship of the sync pulse at Pin 3 and the sawtooth waveform at Pin 4 (which is derived from Pin 6 of the flyback transformer). When a phase offset occurs, current will flow either in or out of Pin 5. Pin 5 is connected to Pin 7 via R319 and thus controls the oscillator. The ratio of R320 with respect to R319 controls the damping of the feedback loop.

R314 and R323 control the output pulse width of the A301 and ensure stability in the pulse width. R311 and C309 provide ripple rejection.

Horizontal Driver - The horizontal driver circuit consists of Q303, R324, C323, R325 and CR202. When the output of A301 is high, Q303 is biased on. It conducts and develops its signal across R324. This signal is coupled through C323 to the base of Q304.

Horizontal Output - The horizontal output stage performs two main functions. It generates the necessary drive current for the horizontal yoke and develops supply voltages to drive the CRT.

Transistor Q304 acts as a switch, which is turned on and off at the horizontal scan rate by the drive signal at the base. When Q304 is turned on, the supply voltage causes the yoke current to increase linearly and moves the scanning beam from near the center of the screen to the right side of screen. At this time, transistor Q304 is turned off, which causes the output inductor and the tuning capacitor C314 to oscillate for half a cycle before diode CR303 takes over. A high reactive voltage in the form of a half-cycle positive voltage pulse is developed by the yoke and flyback transformer inductances. The peak magnetic energy which is stored in the yoke during scan time is then transferred to C314 and the yoke's distributed capacitance. During this cycle, the beam is returned to the left of the screen and then to the center again. This cycle repeats during the next scan line.

Capacitor C311 is a DC blocking capacitor which also serves to provide the "S" shaping of the yoke current waveform. "S" shaping is needed to avoid stretching of displayed video at the left and right side of the tube because the CRT face and deflected beam do not have the same arc.

Horizontal width coil L302 is a variable inductor placed in series with the horizontal deflection yoke. This inductor controls the amount of scan current through the deflection coils, thus controlling the horizontal size. L303 is a magnetically-biased inductor to introduce a changing impedance in series with yokes depending on current direction to improve horizontal scan linearity. C312 and R315 are damping components for horizontal width and linearity coils L302 and L303 respectively.

High Voltage Transformer - This stage is a part of the horizontal output stage and consists of the horizontal output transformer (flyback transformer) along with the rectifiers and filter capacitors needed to generate the required supply voltages to drive the CRT.

The induced voltage produced during the switch-off of Q303 is stepped up and rectified to produce the required high voltage that is applied to the second anode of the CRT. The other auxiliary voltages that are produced by the flyback transformer include the negative voltage for control grid bias (G1), the cathode (K) drive voltage, the screen grid (G2) voltage, and the focus grid (G4) voltage.

Vertical Deflection Processor

A201, a TDA 1170S chip, incorporates all the functions for providing the vertical deflection current to the monitor yoke. C201 and R203 differentiate the negative vertical sync pulse. Resistors R201, R202, and R203 limit the input current for the IC. As a safety feature, CR201 acts to short the input sync pulses if the supply voltage to the monitor exceeds a predetermined value. CR202 is a clamping diode and allows only negative triggering of the IC. R204 and C203 determine the free running frequency of the internal oscillator. In order for the oscillator to be triggered by either 50 or 60 Hz pulses, the free running frequency is fixed at about 46 Hz. The signal from the oscillator is applied to the ramp generator whose slope and amplitude are

determined by R206 and R207. C204 is a high frequency bypass capacitor. The ramp voltage signal is applied to the buffer stage, which isolates the ramp generator from the output stage and reduces any loading on the previous stages. R208, R209, R210, C207 and C208 reshape the ramp to compensate for vertical non-linearity and vertical "S" correction.

The buffer stage output is applied to the pre-amplifier. The pre-amplifier output is applied to the power amplifier stage, which drives the vertical deflection yoke via C212. R216, C210 and R218 provide damping to prevent oscillation in the output stage. R211, R212, R213, R214, R215, R217, and C211 provide the proper AC and DC feedback for the output stage to maintain proper gain and linearity. C209 is used as a high frequency bypass.

Dynamic Focus

Because of the geometry of a CRT, the distance that the scanning electron beam must travel is not uniform on the whole screen. The distance the beam must travel increases when scanning the sides and the corners. This distance determines the focus voltage required at the various parts of the screen. For an average 12"/90° or 14"/90° CRT, the manufacturer's specified focus voltage requirements at the corners is about 200V higher than at the center.

The dynamic focus correction circuit has two stages. The first stage performs all the waveshaping functions required for dynamic focus and consists of an operational amplifier IC401. The frame input is derived from the current feedback resistor of the vertical deflection circuit. R401, C402, and one-half of the dual operational amplifier, IC401, integrate the frame input. The result of this integration is a periodic parabola recurring at the vertical refresh rate. The line input is derived from C311 (the "S" correction capacitor of the horizontal output stage). The other half of IC401 is used for inverting the frame parabola and adding the line parabola to the vertical parabola. Thus a combined line and frame parabola is available on Pin 7 of IC401.

The second stage of the dynamic focus circuit, linear amplifier Q401, is coupled to the first stage through C403. It provides a gain of about 26 dB to give about 200V P-P combined trace and line parabolas to be applied to the focus electrode of the CRT through C405. Diode CR401 protects Q401 from reverse bias. Capacitor C407 provides some high frequency compensation as well as some phase shift to position the parabolas in the right time slot during horizontal scanning. The dynamic focus voltage is AC coupled to the variable static focus voltage derived from the focus control R415.

CATHODE RAY TUBE ASSEMBLY

The cathode ray tube (CRT) assembly consists of a CRT and yoke assembly. The yoke comes prealigned to a bogey tube. Correct yoke alignment will depend on how much a particular CRT differs from the bogey tube. The yoke may be rotated on the CRT neck and the individual magnets may be adjusted to provide proper screen alignment.

MONITOR ADJUSTMENTS

Holes are provided in the mounting bracket to facilitate monitor adjustments. Each hole is labeled with the name of its adjustment pot. Tweak these pots to align and adjust the visual display.

Adjust the brightness pot so that the raster is visible, then decrease the brightness until the raster barely disappears. This will allow the TCM brightness setting to function properly.

5

KEYBOARD FUNCTIONAL DESCRIPTION

GENERAL

The keyboard is a sculptured, low-profile, detachable, intelligent serial unit. As required by DIN specifications, the home row keys are 30mm above the working surface and the keyboard is inclined at an angle between 7 and 11 degrees.

The capacitive keyswitches are basically small variable capacitors formed by a fixed plate on the circuit board and by movable plates controlled by the switches. These switches are connected in a matrix like many other keyboard switches. The design of the matrix can accommodate a maximum of 128 switch stations, although only 94 are used in the ATL keyboard. The keyboard exhibits true N-Key rollover and phantom key lockout.

A coiled cable supplies +12VDC to the keyboard circuitry. A regulator provides +5VDC regulation at the keyboard. The cable attaches to the keyboard on the back edge of the keyboard enclosure near the left corner.

Scanning circuitry is based on a P8039-6 microprocessor and an external 2716 ROM located on the keyboard PCB. The single-chip microprocessor implements the keyboard controller functions and communicates bi-directionally with the main terminal processor via a half duplex serial link. Serial data integrity is end-to-end error controlled with a minimum rate of 9600 baud.

8039 MICRO-COMPUTER

The 8039-6 is a 40-pin, 6 MHz, single-chip microcomputer with 128×8 RAM. It provides 27 I/O lines, an internal timer/event counter, a 2.5 μ sec cycle and a single 5V power supply requirement. The 8039-6 (Z5) communicates serially with the 8041 Universal Peripheral Interface (UPI) located on the main logic board in the terminal.

CRYSTAL FREQUENCY

Drive for the microcomputer is provided by a 5.76 MHz crystal Y1. The selection of this frequency was made to accommodate standard baud rates for several transmission and reception rates up to 19.2K baud.

INTERFACE TO TERMINAL

The 8039-6 (Z5) microcomputer communicates serially with the terminal via J1, an 8-pin miniature telephone jack and an 8-conductor coiled telephone cable. All signal lines have 0.001 μ fd capacitors connected to chassis ground at connector J1 to provide RF noise suppression. See Table 5-1 for J1 pin assignments.

Keyboard Receive Data

Data from the terminal KRXD to the keyboard is received on Pin 3 of J1 where it is pulled up by a 4.7K resistor to +5VDC and buffered by inverter Z4 before being received at INT(N) (Pin 6) and T1 (Pin 39) on the microcomputer Z5. INT(N) on the microcomputer is an interrupt input. A low level at this input signals the microcomputer that a serial byte from the 8041 UPI on the main logic board has started. The low-going edge is seen as the start bit of the serial data.

T1 on the 8039 is a test input. It is used to test the signal state. This line is tested one half-bit time period after the interrupt occurs and then every bit time period thereafter until the incoming serial data is completely received.

Keyboard Transmit Data

Data is transmitted serially from P27 (Pin 38) of the 8039, buffered by inverter Z4 and sent out to the terminal via J1 Pin 5 (KTXD). This will become keyboard receive data on the terminal logic board. See Table 5-1 for J1 pin assignments.

POWER SUPPLY

A voltage of +12VDC is supplied from the terminal via the keyboard cable to Pin 7 of J1 and regulated to +5VDC by regulator Q1. This five-terminal regulator provides a reset output to the reset input of the 8039. For proper heat dissipation, a heat sink is attached to the switch support plate.

GROUNDING

There are separate chassis and logic grounds to minimize the effects of electrostatic discharge. The keyboard switch support plate must remain isolated from the logic common on the keyboard. The switch support plate is connected to chassis ground at a point near connector J1. See Table 5-1 for J1 pin assignments.

Table 5-1
J1 Data Jack
Pin Assignments

PIN #	ASSIGNMENT
Pin 1	CHASSIS GND
Pin 2	LOGIC GND
Pin 3	KRXD (KBD RECEIVE DATA)
Pin 4	LOGIC GND
Pin 5	KTXD (KBD TRANSMIT DATA)
Pin 6	LOGIC GND
Pin 7	+12VDC
Pin 8	CHASSIS GND

MATRIX SCANNING

The keyswitches are small variable capacitors formed by a fixed plate on the circuit board and by movable plates controlled by the switches. These switches are connected in a matrix like many other keyboard switches. The design of the matrix can accommodate a maximum of 128 switch stations although only 94 are used in the ATL keyboard. Scanning circuitry is based on a P8039-6 microprocessor and an external 2716 ROM.

Byte-Wide Interface

Byte-wide interface chip Z6 is a custom IC by General Instruments that satisfies the interface requirements between the switch array and microprocessor Z5. This chip basically provides the required drive and sense circuits for up to 128 capacitive keys in a 16 × 8 matrix. It also provides mechanical hysteresis and debouncing. This chip allows the 8039 microprocessor to control scanning and encoding. Figures 5-1 and 5-2 illustrate the pinouts and timing for this chip. Table 5-2 gives the AC characteristics.

Pinouts and Signal Functions - The circuit is placed in a 40-pin DIP package. Twenty-four of the 40 pins are used to interface to the matrix—twelve are used to interface to the processor; the remainder are used for setup of the sense amplifiers and power. The following is a list of the pins and their function.

Y-lines (Y0-Y7)	These are the 8 sense lines. The small current pulses caused by the X-lines are detected here. Two thresholds are provided, individually controlled by the processor, which are used to give the switches hysteresis.
X-lines (X0-X15)	These are the 16 matrix drive lines. The line to be active during the read cycle is selected by writing an address to the chip while the ALE pin (Pin 6) is hi. The selected output is active while the RD* line is active (lo).
Data bus (DB0-DB7)	These lines form a bidirectional port which receives the address and threshold data from the processor and returns the key data requested. DB0 through DB7 all have passive pullups. The load is equivalent to a 2.3 K-ohm resistor returned to 4V.
Write strobe (WR*)	A low level on this pin gates the data bus to the threshold control latches. The data is latched on the rising edge.
Read strobe (RD*)	When this line goes lo, the selected X-line goes lo and the data output drivers are enabled. If the resulting signal on the Y-line exceeds the threshold, the output is latched hi. The data and decoder outputs return to the inactive state when this line goes hi.
Address latch enable (ALE)	When hi, the lower half of the data bus is connected to the decoder latch. The data is latched when this pin goes lo.
Chip select (CS)	When this pin is hi, the circuit is enabled. It can be left open if not used. It has an internal pullup, as do the RD*, WR* and ALE inputs.
Sensitivity node (Iset)	A resistor tied from this node to Vcc is used to set the relative sensitivity. Decreasing the value will lower the thresholds.
Common node (CM)	A bypass capacitor is required on this node to ground. A resistor tied to Vcc is also used to program the relative threshold levels. The resistors on this and the Iset nodes interact considerably.
Power (Vcc, Gnd)	Requires single 5.0V \pm 10% supply.

* For more detailed specifications, consult General Instruments Byte-Wide Interface Application Note 715-115.

Figure 5-1
Byte-Wide Pinouts

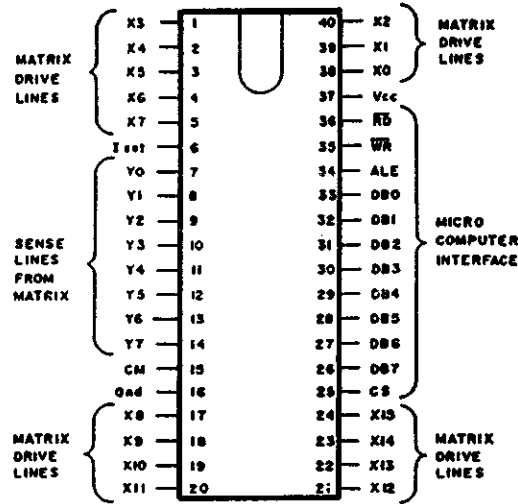


Figure 5-2
Byte-Wide
Timing Diagram

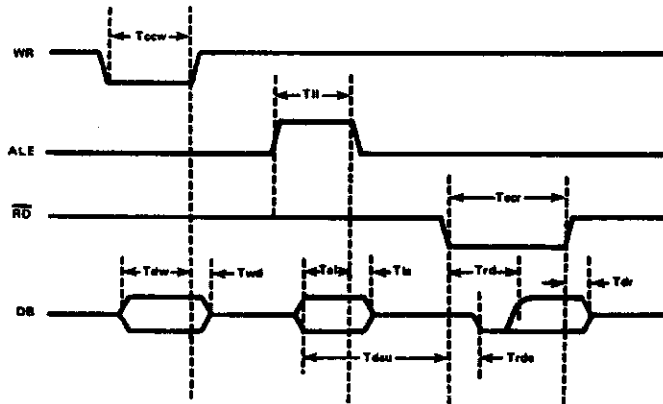


Table 5-2
Byte-Wide AC
Characteristics

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_{ccw}	Write pulse width	250		nSec
T_{dw}	Data setup to Write	250		nSec
T_{wd}	Data hold to Write	0		nSec
T_{H1}	ALE pulse width	250		nSec
T_{al}	Address setup to ALE	120		nSec
T_{la}	Address hold to ALE	0		nSec
T_{ccr}	Read pulse width	700		nSec
T_{rd}	Read to data ready		450	nSec
T_{dr}	Data hold to Read	10	200	nSec
T_{dsu}	Address setup to Read	240		nSec
T_{rde}	Bus enable from Read	10	200	nSec

Scanning Levels

The capacitive matrix is scanned by the microprocessor by byte-wide interface Z6. One of 12 scan lines is selectively addressed by the microprocessor and internal circuitry causes a negative pulse on that line. Current is coupled through a closed capacitive switch and enters one of eight sense amplifiers. If the current pulse is of sufficient magnitude, an internal latch is set for that particular bit, and is read off the data bus with a standard read instruction. The threshold of current required to set the internal latch can be individually set at one of two levels by the use of a write instruction from the microprocessor. This makes it possible to provide hysteresis to debounce keys.

Keyboard Encoding

The keyboard is encoded to provide N-key rollover (NKRO), which means that each key can be encoded independently of the status of the other keys.

In general, NKRO routines reserve a bit in RAM for each key in the array. As the keyboard is scanned, the key data and RAM are compared on a byte-by-byte basis. If there is no change in status, nothing needs to be done, and the processor can return to other tasks. If there is a change in status, the key is processed up or down, depending on the data. The bit in RAM would be set after the key is processed down (encoded), and cleared otherwise. While encoding, the processor must make sure that the proper threshold has been crossed and that the data is not caused by random noise. The problem with extraneous data is easily solved by reading the switch twice to confirm its condition; there is a 1.5 msec period between these two scans. When the data is validated, the processor then selects the proper code for the key and formats it for sending to the host.

MEMORY

The keyboard has external memory capability. External memory Z7 is selectable between 2716 EPROM/2316 ROM (2K × 8) and 2732/2332 ROM (4K × 8) by means of jumpers A and B. Internal program memory may be selected by jumper C as listed in Table 5-3.

Table 5-3
**Keyboard Internal/
External Memory
Strapping**

JUMPER	A	B	C	D
EXT PROG MEMORY				X
INT PROG MEMORY			X	
2716		X		
2732	X			

X = strap is in


AUDIO ALARM

The keyboard is capable of generating five sounds: two different tone beeps (600 Hz and 1200 Hz), a ring, a warble and a click. A ring is a signal alternating between 600 Hz and 1200 Hz for a duration of 750 msec. A warble is the same as a ring but with a continuous duration. A keyswitch click is a DC pulse with a duration of 5 msec. The microprocessor provides a dual-level volume control. These sounds and the volume control are under program control.

The keyboard has an on-board audio oscillator consisting of Z3 and associated circuitry that can produce 600 Hz and 1200 Hz independently. The oscillator is a dual timer/osc 556. One half of the device provides a 1200 Hz square wave while the other half can provide a 600 Hz square wave. The microprocessor (Z5) is capable of enabling either tone by asserting EN1200 and EN600 respectively. Outputs from the 556 (Z3) Pins 9 and 5 are ORed by Z2. This signal is buffered by Z1 which drives audio transducer L1. A keyswitch key

click is obtained with the microprocessor asserting keyclick, which is only a DC pulse and does not have the 1200 and 600 Hz tones. The microprocessor provides a higher volume by asserting EN HI VOL which allows more drive for the audio transducer.

RESET CIRCUIT

 1, a five-volt regulator, provides a reset output to the reset input of the 8039 microprocessor. When the keyboard is powered on, the reset output is held lo for 30 msec after the supply voltage reaches 4.85 V and then goes hi. This 30 msec delay is needed by the microprocessor for its internal biasing requirements. Capacitor Cd at Pin 4 controls the length of this delay. When the voltage drops below 4.85 V, the processor is reset.

6

ATL-008 LOGIC BOARD FUNCTIONAL DESCRIPTION

GENERAL

The ATL-008 terminal logic board contains the terminal microprocessor, communications circuitry, memory, and video control circuitry. The 68008 microprocessor allows the use of an 8-bit data bus. It controls the system operation by executing instructions read from the program memory. The 8530 Serial Communications Controller (SCC) is a dual channel, full duplex, multi-protocol data communications peripheral which functions as a serial-to-parallel, parallel-to-serial converter/controller. The 8041/8741 is a Universal Peripheral Interface (UPI) designed as a general purpose programmable interface device compatible with a variety of microprocessor systems. It functions basically as an intelligent UART to reduce overhead for the 8039 microprocessor on the keyboard and to provide certain status information about the main and aux ports. The ATL-008 memory consists of dynamic RAM, static RAM, ROM, and EEPROM. The standard ATL-008 has 32K bytes of DRAM, which is upgradable to 128K bytes. The video section is comprised of a CRT controller, a video attribute controller, four 1K × 4 bit static RAMs, and a clock generation circuit.

NOTE

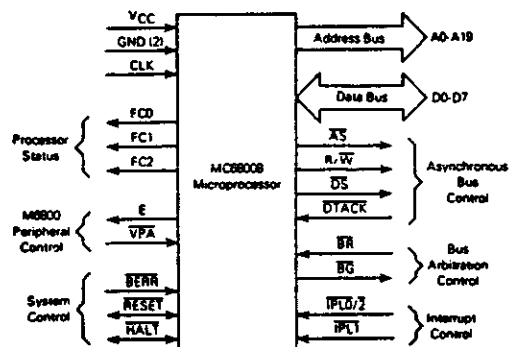
The ATL-008 terminal uses a variety of programmable array logic (PAL) chips. Refer to Appendix C for PAL equations and state diagrams.

68008 MICRO-PROCESSOR

The central processing element of the ATL-008 terminal is the 68008, a member of the 68000 family of 16-bit microprocessors. The 68008 allows the use of an 8-bit data bus. The microprocessor controls the system operation by executing instructions read from the program memory.

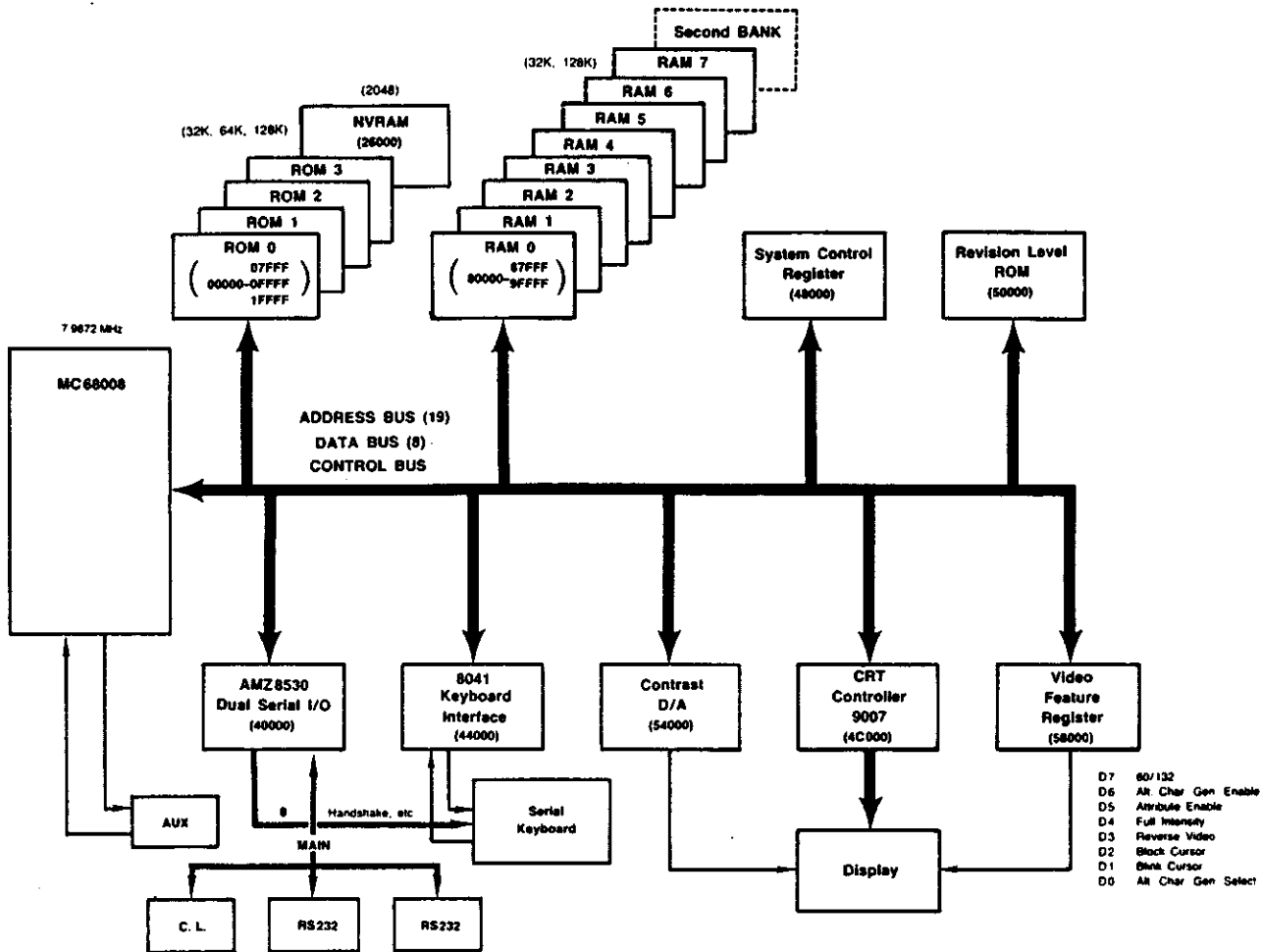
Figures 6-1 and 6-2 show the busing arrangements and device assignments of the 68008 system.

Figure 6-1
68008 Input/Output
Signal Configuration



L
E

Figure 6-2
68008 System
Block Diagram



Address Bus (A0 - A19)

The address bus (A0 - A19) is a three-state, 20-bit wide bus which can be driven by the 68008 microprocessor, the 9007 video controller, and the refresh controller. The address bus provides the addresses for bus operation during all cycles except interrupt acknowledge cycles. During interrupt acknowledge cycles, address lines A1, A2 and A3 provide the interrupt level while the remainder of the address lines are driven hi.

The primary devices and logic sections connected to the address bus are: I/O select decode logic, ROM select decode logic, ROM array and EPROM memory section, RAM timing and control logic, RAM array, 8041 peripheral interface, 8530 serial communications controller, and 9007 video controller.

Data Bus (D0 - D7)

The 68008 allows the use of an 8-bit data bus while providing the benefits of 32-bit microprocessor architecture. The bidirectional, three-state data bus is the general purpose data path for the ATL-008 system.

The devices and registers that are connected to the data bus are as follows:

- 8530 Serial Communications Controller
- 8041 Universal Peripheral Interface
- 9007 CRT Controller
- Revision Level PROM
- Contrast Control Register
- Video Feature Select Register
- System Control Register
- ROM Array and EEPROM
- Dynamic RAM Array

Clock Generator

CPU Clock - CPUCLK is the clock input of the 68008 microprocessor (A69, Pin 34). It is generated by a 15.9744 MHz crystal, Y1, which is divided down to 7.9872 MHz by a D-Flop, A51. This clock drives only the microprocessor.

System Clock - SYSCLK, 7.9872 MHz, is generated the same way as CPUCLK, but is taken from a separate buffer to isolate the CPUCLK.

UPI Clock - The Universal Peripheral Interface Clock (UPICLK) is derived from the same 15.974 MHz crystal as CPUCLK and SYSCLK. The crystal frequency is divided by 4, resulting in a 3.9936 MHz signal. The UPICLK drives the 8041 Universal Peripheral Interface (A79).

Reset

The voltage comparator, A70, senses the power as it is coming up to the normal supply voltage of 5VDC. The output is driven hi when the supply voltage reaches about 4.7VDC. The output of the voltage comparator then triggers the monostable multivibrator, A53, causing RESET* to go lo. Reset stays lo for 225 msec before returning to the hi condition.

If the power supply voltage drops below approximately 4.7V, the output of the voltage comparator, A70, is driven lo, causing RESET* to go lo again for 225 msec.

The reset pin (Pin 37) of the microprocessor, A69, is bidirectional in that it can be an input or an output. During a software reset this pin becomes an output, therefore causing RESET* to go lo and the system to be reset.

Halt

The halt operation is derived from the same circuitry as RESET*. When A85 (Q*) goes lo, HALT* goes lo, causing the microprocessor to halt. When it goes hi, the processor goes into its run condition.

Bus Error

BERR*, the bus error signal, informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of non-responding devices, interrupt vector failure, and various other application dependent errors.

The bus error circuit consists of a retriggerable one-shot A85 triggered by Address Strobe AS*. AS* going lo retriggers the one shot so that its Q output, BERR* Input to the CPU, is asserted hi. BERR* will remain hi for 100 μ sec. If AS* is not asserted for more than 100 μ sec, BERR* will go lo, indicating to the microprocessor that a bus error has occurred.

L
B

Control Bus

WRITE* - The R/W output on the microprocessor provides write control. When R/W is lo, WRITE* is asserted lo and the selected device will be written into. The R/W is a three-state output on the microprocessor. When the processor is placed in the hold and halt modes and during reset, the R/W is placed into a tri-state condition.

Address Strobe AS* - Address Strobe AS* (Pin 28 on the microprocessor) is a tri-state signal that indicates a valid address on the address bus. It is also used to lock the bus during a read-modify-write cycle used by the test and set (TAS) instruction. When another bus master (the 9007 CRT controller or the refresh controller) controls the bus, it is responsible for asserting AS*. During the transition of bus control, a pullup resistor holds AS* inactive.

Data Strobe DS* - Data Strobe DS* on the microprocessor is a tri-state signal that controls the flow of data on the data bus as shown in Table 6-1. When the R/W line is hi, the processor will read from the data bus as indicated. When the R/W line is lo, the processor will write to the data bus as shown.

Table 6-1
Data Strobe Control
of Data Bus

DS*	R/W	DO - D7
1	-	No Valid Data
0	1	Valid Data bits 0 - 7 (Read Cycle)
0	0	Valid Data bits 0 - 7 (Write Cycle)

Data Transfer Acknowledge DTACK* - DTACK, Data Transfer Acknowledge (Pin 31 of the processor), is an input that indicates that the data transfer is completed. When the processor recognizes DTACK during a read cycle, data is latched and the bus cycle is terminated by the CPU. When DTACK is recognized during a write cycle, the bus cycle is also terminated.

Bus Request BR* - BR*, Bus Request, comes from the Bus Arbiter/Refresh Controller PAL A35. The arbiter will arbitrate control of the bus between the CRT Controller and the Dynamic RAM Refresher. The controller will assert BR* when either the CRT Controller or Refresher requests control of the bus. See the Bus Arbiter/Refresh Controller section for additional details.

Bus Grant BG* - BG*, Bus Grant (Pin 32 of the processor), indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle (AS* going hi).

Interrupt Priority Level IPL1* and IPL2* - Interrupt priority level inputs IPL1* and IPL2* indicate the encoded priority level of the device requesting an interrupt. The MC68000 MPU uses three pins to encode a range of 0 - 7, but due to pin limitations only two pins are available for the MC68008. By connecting the IPL2 pin to both the IPL0 and IPL2 inputs internally, the MC68008 encodes values of 0, 2, 5, and 7. Level zero is used

to indicate that there are no interrupts pending. Level seven is a non-maskable interrupt. Except for level seven, the requesting level must be greater than the level contained in the processor status register before the processor will acknowledge the request.

A satisfactory interrupt condition must exist for two successive clocks before triggering an internal interrupt request. An interrupt acknowledge sequence is indicated by the function codes being set all hi while A1 through A3 are set to indicate the interrupt level being responded to and subsequently AS* and DS* being asserted.

Function Code FC0, FC1, FC2 - The processor status pins FC0, FC1, and FC2 are function code outputs that indicate the state (user, supervisor or interrupt acknowledge) and the cycle type currently being executed, as shown in Table 6-2. The information indicated by the function code outputs is valid whenever address strobe AS* is asserted.

Table 6-2
Function Code
Outputs

FUNCTION CODE OUTPUT				CYCLE TYPE
FC2	FC1	FC0		
0	0	0		(Undefined, Reserved)
0	0	1		User Data
0	1	0		User Program
0	1	1		(Undefined, Reserved)
1	0	0		(Undefined, Reserved)
1	0	1		Supervisor Data
1	1	0		Supervisor Program
1	1	1		Interrupt Acknowledge

Valid Peripheral Address VPA - The VPA input indicates that the device addressed is an M6800 family device. In the ATL-008 there are no M6800 family peripherals, so VPA* is used to slow the cycle time when accessing a peripheral. Normally, the M6800 peripherals are synchronized to the enable (E) signal. However, this feature is not used by this design.

VPA* is also used to indicate to the CPU that the autovector for the acknowledged interrupt should be used. Most interrupting devices respond with a VPA or autovector. The single exception is the Serial Communications Controller (SCC) which uses the vectored interrupt mode and puts the vector number assigned to it on the data bus.

Interrupt Structure

Interrupt Controller PAL - The 68008 microprocessor has only three levels of interrupt inputs. A fourth is required in this design. A programmable array logic (PAL) chip, Interrupt Controller A88, provides another method of prioritizing the interrupts.

L
B

The interrupt controller PAL has all interrupt request inputs and assigns the following priority level to the devices:

LEVEL	MEANING
7	CRT Controller
5a	Serial Communications Controller*
5b	Universal Peripheral Interface*
2	5 millisecond Timer
0	No interrupts requested

*The SCC and the UPI are essentially daisy chained, with the SCC being the first device on the chain.

When the CPU acknowledges a level 5 interrupt the PAL further arbitrates between the SCC and UPI. If the SCC does not have an active request the interrupt acknowledge goes to the UPI.

When the interrupt request from the SCC is acknowledged by the 68008 the interrupt controller first asserts SCCIACK* (SCC Interrupt Acknowledge) which signals the SCC to put the vector number onto the data bus. It then asserts DTACK* signaling to the 68008 that the vector number is on the data bus. After the CPU receives the vector number it goes to the address in low memory reserved for that vector and reads the address of the service routine.

The UPI is an autovector-type device and VPA* is asserted by the PAL at the time UPIIACK* (UPI Interrupt Acknowledge) is asserted. The CPU then reads the address reserved for AUTOVECTOR #5 and goes to that address to begin servicing the interrupt request.

When the 68008 acknowledges an interrupt, it will:

1. Place the interrupt level on A1, A2, A3.
2. Assert A0, A4 - A19 to a hi condition.
3. Set WRITE* = hi (READ).
4. Set function code to interrupt acknowledge FC0 = FC1 = FC2 = hi.
5. Assert AS*.
6. Assert DS*.

PERIPHERALS

Serial Communications Controller

The 8530 Serial Communications Controller (SCC) is a dual channel, full duplex, multi-protocol data communications peripheral which functions as a serial-to-parallel, parallel-to-serial converter/controller. This microprocessor peripheral provides vectored interrupts, polling and simple handshaking as well.

Main Port Control - The SCC supports a main port which consists of 20 mA current loop (J7), RS422 (J8), and RS232 (J3) external port connections. Selection of these ports is under TCM control. The receive data lines from each external port are selected by A47 and sent to the RXDA input (Pin 13) of the SCC.

For local loopback testing, the main port can be disabled to stop data from going out. Incoming data is then intercepted by the multiplexer A47. Local loopback is selected by setting $O/232^* = 422ENBL = 10$.

Aux Port - The SCC also supports an external auxiliary port J4 with RS232 only. The data and control lines are connected directly to the B side of the SCC and are not multiplexed with any other external port. The aux port is disabled when the main port is put in local loopback mode.

Transmit and Receive Clocks - The 8530 has basically two internal USARTS, each of which has two clock inputs. These clock ports are programmable for several modes of operation. TRXCA*, Pin 14 of the SCC, can be programmed as either a clock input or an output. In this application it is used as an input. RXTCA*, Pin 12, can be used only as an input.

The clock inputs for the other internal USART consists of SCCCLK (Pin 28) and AUXEXTCLK (Pin 26). Pin 26 can be programmed either as an input or output. In this application it is used as an output to provide an external clock for the Auxiliary RS232 Interface J4. SCCCLK is an input only.

The SCC PAL, A80, selects the proper internal or external clock for either the RS422 or RS232 ports.

The SCC PAL also interprets the state of $O/232^*$ and 422ENBL to select local loopback mode or a main port interface as shown in Table 6-3.

**Table 6-3
Main/Auxiliary
Port Selection**

$O/232^*$ 422ENBL FUNCTION

0	0	Inhibit main and aux port data transfer (local loopback mode)	
0	1	Main = RS232	Aux = enabled
1	0	Main = Current Loop	Aux = enabled
1	1	Main = RS422	Aux = enabled

Interrupts - See Interrupt Structure and Interrupt Controller PAL equations.

Reset - The SCC interprets the coincidence of RD* (Pin 36) and WR* (Pin 35) going lo as a reset. This is accomplished by the microprocessor asserting RESET*, which becomes an input to the SCC PAL, which drives WDDS* and RDDS* lo at the same time, causing the SCC to reset.

**Universal
Peripheral
Interface**

The 8041/8741 is a Universal Peripheral Interface (UPI) designed as a general purpose programmable interface device compatible with a variety of microprocessor systems. It contains a microcomputer with program and data memory, I/O ports, etc.

This device functions basically as an intelligent UART to reduce the overhead of the 68008 CPU when communicating with the 8039 microprocessor on the keyboard. It also functions to provide certain status information about the main and aux ports.

L
B

Port 1 - Port 1 consists of eight bidirectional I/O lines P10 through P17 (used as inputs) as described below:

P10	DSRA*	Data Set Ready modem signal from main port RS232
P11	CIA*	Speed mode indication modem signal from main port RS232
P12	RIA*	Ring indicator from modem on main port RS232
P13	TMA*	Test mode from modem on main port RS232
P14	ADEV RD4*	A lo indicates aux device ready
P15	N/C	Pulled up to +5
P16	CLINST*	Asserted lo if current loop option is installed
P17	422INST*	Asserted lo if RS422 interface is installed

Port 2 -

Keyboard Interface - Keyboard Receive Data (KBRXD*) from the keyboard goes to keyboard connector J6 (Pin 5), is buffered by A21 and becomes Keyboard Receive Data (KBRXD) at Test 1, Pin 39, input of the UPI A24. This data signal will contain information as to what key has been activated on the keyboard.

Keyboard Receive Data, KBTXD, from Port P20 of the UPI is buffered by A21 connecting to J6 (Pin 3), becoming Keyboard Receive Data (KBTXD*). This data line carries such information as ACK and NACK (acknowledge and not acknowledge for byte error checking), audio control, initialization sequences and keyboard selftest information.

TCM Override Strap - When this jumper E1 – E2 is inserted it pulls P21 (Pin 22) to ground. This strap allows a manual means to override the TCM password.

UPI Interrupt Request - When the UPI receives a data byte from the keyboard, an interrupt is requested from the microprocessor by asserting P24 (Pin 35) to a hi. This clocks D flip-flop, A19, asserting UPIIRQ* to a lo which is an input to the Interrupt Controller PAL A88. The controller decodes the UPIIRQ* to level 5 if its the highest level interrupt input. The PAL decodes the outputs IPL1* and IPL2* to a hi and a lo respectively. These signals become the interrupt level inputs IPL1 (Pin 41) and IPL2 (Pin 42) of the processor. The processor responds, after any active cycle is completed, by placing a hi on the three function code outputs, FC0, FC1, FC2, and drops AS*. Interrupt Acknowledge, IACK, is asserted hi which is an input to the Interrupt Controller PAL.

Up until now, the controller has been in a loop looking for an interrupt acknowledge from the processor. IACK going hi and DS* going lo causes the controller to jump out of this loop. If A3 = 1 and A2 = 0, a level 5 interrupt is being acknowledged by the CPU. If the SCC's interrupt request is not asserted (SCCIRQ* = hi), then VPA* and UPIIACK* are both asserted lo until IACK goes lo or DS* goes hi. This signals the end of the interrupt acknowledge cycle. UPIIACK* going lo clears the D-type flip-flop, returning UPIIRQ* to a hi state.

UPI Clock - The UPICLK is derived from Y1, a 15.9744 MHz crystal and is divided down by four to produce 3.9936 MHz which drives the XTAL1 and XTAL2 inputs of the UPI.

Reset - When RESET* (Pin 4) goes lo, the internal status flip-flops are reset and the program counter is set to zero.

CRT Controller

The 9007 CRT Controller is a programmable video processor and controller which provides the central control of the video section. For detailed information see the Video Section.

Board Revision Level

The etch and circuit version of the logic board can be determined by reading the contents of the Revision Level PROM A86. Revision Level Select (REVSEL*), at the output of the I/O select decoder A51, is asserted to enable the contents of the PROM onto the data bus (D0 – D7). Address bit A1 from the CPU is used to select between two bytes in the ROM. The four highest order address bits of the PROM are connected in etch to indicate the etch level. When the low order byte is read, the least significant four bits (D3 – D0) are programmed to reflect the etch level. The next byte contains an 8-bit code to indicate the circuit revision level.

Contrast Control

The contrast control consists of an octal latch, op amps and an output transistor. The data byte is latched from the data bus D0 – D7 into the D-latch (A92) when CONSEL* goes lo to hi. Output enable (OE) of the latch is grounded so that the output of the latch is always enabled. The latched data bits D0 – D3 are input to the summing resistor network. This network is connected to a common node at the negative input (Pin 2) of the amplifier. The positive input is referenced to +5VDC. The output of the amp, A105-A, will swing from +5 to +10VDC in 16 increments. This circuit constitutes the D/A section of the contrast control. The output of the D/A section feeds the positive input of A105-B which drives the base of transistor Q2. Contrast is taken from the emitter of Q2 in an emitter follower configuration. The output will vary from 4.3 to 9.3VDC.

Video Features Register

The Video Features Register, A61, consists of an octal latch that latches the proper data byte from the data bus D0 – D7 when Video Register Select (VREGSEL*) goes lo to hi. This register latches in the following video controls:

80/132*	80 columns is selected when hi, 132 columns when lo.
ALTCHARGENEN	When hi, the alternate character generator is enabled.
ATTRLATEN	Latched attributes are enabled when hi.
FULLINTSCRN	Full intensity screen is enabled when hi.
REVVIDSCRN	Reverse Video screen is enabled when hi.
BLINKCURS	Blinking cursor when hi, steady cursor when lo.
BLOCKCURS	Block cursor when hi, underscore cursor when lo.
ALTCHARGENSEL	When hi, the alternate character generator is selected.

The above signals operate in conjunction with various I/O lines not shown here. For more detailed information see the Video Section.

L
B

System Control Register

The system control register, A64, is an octal latch that latches the proper data byte from the data bus D0 – D7. This provides some system control as described below:

TIMERENBL	Enables the 5 msec timer interrupt request, TIMERIRQ*.
INT/EXT*	Selects between internal and external clocks via SCC PAL.
AUXDSR*	Data set ready to aux port.
RDLOOP	When hi, a remote digital loop for RS232 is selected via main Port, J3.
ANALOOP	When hi, a remote analog loop for RS232 is selected via main Port, J3.
SPEEDSEL	Selects baud rate of modem via RS232 main port, J3.
OTHER/RS232*	When lo, RS232 is selected via SCC PAL.
CL/RS422*	When hi, current loop is selected. When lo, RS422 is selected via SCC PAL.

MEMORY

The memory system within the ATL-008 consists of: dynamic RAM A17 – A24, A2 – A9; static RAM A10 – A13; ROM A93 – A96; EEPROM A98. The standard ATL-008 will have 32K bytes of DRAM, which is upgradable to 128K bytes with the availability of the extra sockets.

Two sockets of the ROM array are upgradable to stacked sockets, allowing two ROMs in the same footprint as one. Pin 20 of each device is brought out separately to allow selecting of one or the other.

Memory Map

Figure 6-3 illustrates the allocation of memory within the ATL-008. Appendix B contains additional details.

Dynamic RAM Array

The RAM array is 16 data bits wide divided into two 8 bit banks: the lower byte (RAM D0 – RAM D7) and the upper byte (RAM D8 – RAM D15). Each bank is addressed by eight address bits which are buffered by a tri-state buffer/driver A53 and A72. This buffer allows a row in the array to be addressed at one time and then a column to be addressed. CRTCAS* (from the CRT controller in the video section) or DRAMSEL* can assert MEMSTRT, which generates the start of a RAM cycle. MEMSTRT is delayed 45nsec via delay line A1 before driving the control inputs of the buffer to the proper conditions to output the column address. Both Row Address Strobe RAS* and Column Address Strobe CAS* are derived from MEMSTRT via delay line A1. RAS* is delayed 15nsec and CAS* is delayed 60nsec. Data is multiplexed onto the data bus D0 – D7 by A38 and A37 tri-state octal transceivers. The outputs of these transceivers are enabled by RBHE* and RBLE*.

NOTE

The Dynamic RAM requires refreshing at predetermined intervals. This is accomplished by the DRAM Refresher. For detailed information see Bus Arbiter/Refresher Controller.

DRAM Write Cycle - During a write cycle, the processor sends data to either the memory or some peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor

writes both bytes serially. When the instruction specifies a byte operation, the processor uses A0 to determine which byte to write and then issues the data strobe.

Refer to Figures 6-4 and 6-5. During a write cycle to DRAM the micro-processor places the function codes on FC0 – FC2 and the address on A1 – A19, sets A0 = 1 to write the high byte and then asserts address strobe AS*. AS* going lo causes DRAMSEL* to go lo, creating MEMSTRT. MEMSTRT generates the start of another RAM cycle which propagates through the delay line A3 to assert RAS*.

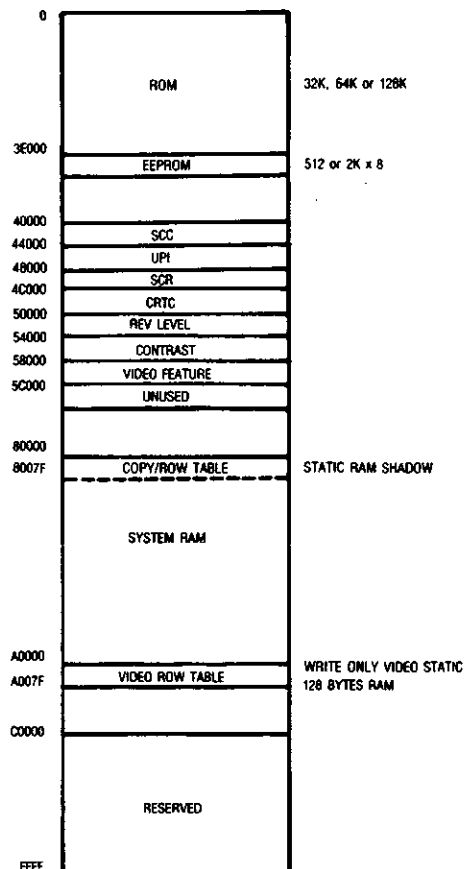
The processor sets WRITE* to a lo, which causes WE1* on PAL chip A36 to go lo. This is connected to write enable lines WE A5 – A12 (Pin 3 of the RAM). The high byte of the RAM is now enabled for a write condition.

A37 and A38 are bidirectional driver/receiver chips that control the direction and byte selection between the data bus D0 – D7 and RAM data RAM D0 – RAM D15. WRITE* is asserted, and the direction of data flow is to the RAM memory. The processor places data on D0 – D7. Data strobe DS* is asserted lo, causing CASEBL to go hi. CASEBL allows CAS* to go lo. CAS* clocks the data into the RAM.

Data transfer acknowledge, DTACK*, is asserted when CAS* is active. DS* and DTACK* are negated when CAS* goes hi, indicating the end of that cycle.

The same cycle follows in order to write the low byte of the word. The only differences are that the processor sets A1 = 1 for a low byte, and A37 and A38 place data at D0 – D7 to the low byte RAM D0 – RAM D7.

**Figure 6-3
ATL-008
Memory Map**



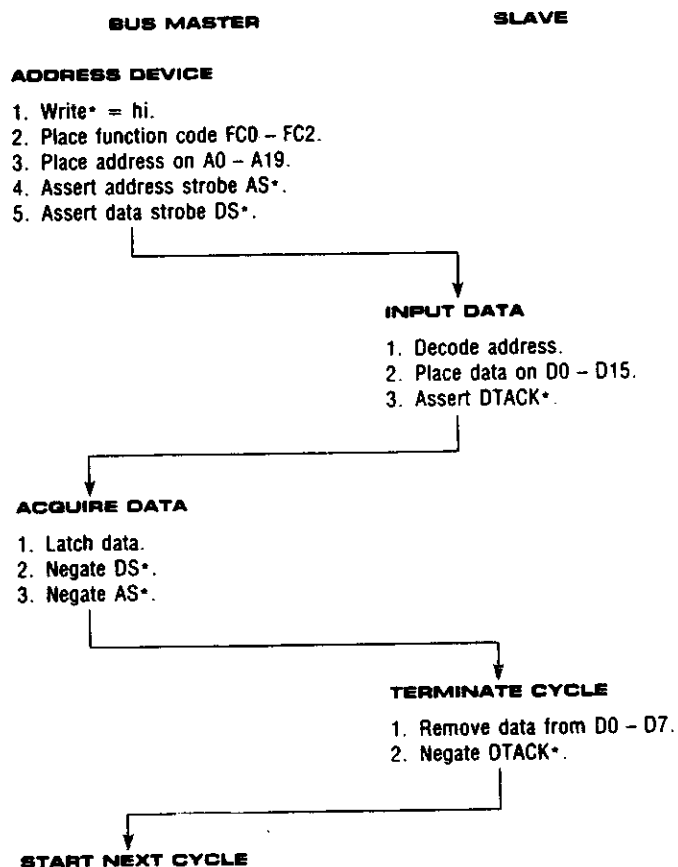
L
B

DRAM Read Cycle - During a read cycle, the processor receives data from the memory or some other device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads the appropriate number of bytes (2 or 4). When the instruction specifies byte operation, the processor uses A0 to determine which byte to read.

Refer to Figures 6-6 and 6-7. The processor sets WRITE* to a hi, places the function codes on FC0 – FC2. The address is placed on A1 – A19. The processor sets A0 = 0 for read of the high byte. Address strobe (AS*) is asserted lo by the microprocessor, indicating that a valid address is present on the bus. AS* going lo asserts DRAMSEL* lo, causing RAS* to go lo via delay line A3.

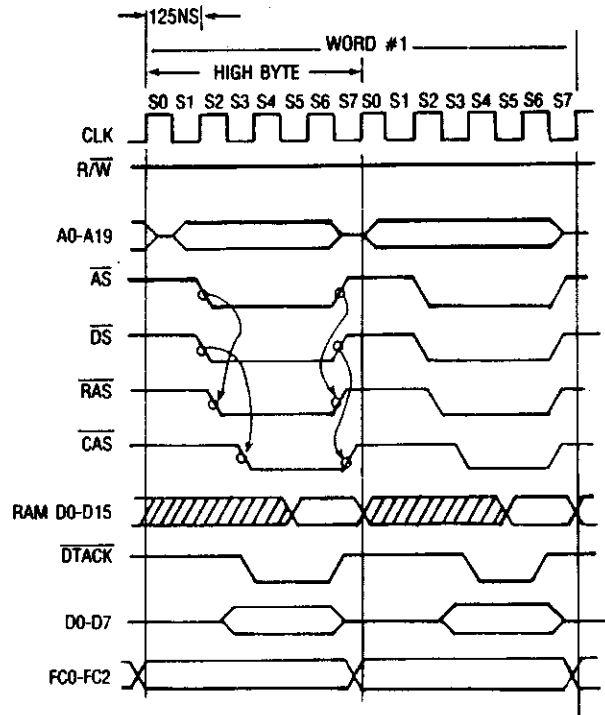
DS* going lo to the RAM causes CASEBL to go hi, allowing CAS* to be asserted lo. CAS* is now asserted lo, the RAM decodes the address and places data on bus D0 – D7. Data transfer acknowledge, DTACK*, is asserted lo. The processor latches the data, negates DS* and AS*. The RAM then removes data from data bus D0 – D7 and negates DTACK*, indicating an end to that bus cycle. When the next byte (low byte) of the word is read, A0 is asserted hi. The same sequence of events now follows as the first byte.

**Figure 6-6
DRAM Byte
Read Cycle
Flow Chart**



L
B

Figure 6-7
DRAM Read Word
Timing Diagram



Static RAM

In order to reduce overhead for the 68008 microprocessor, four 1K × 4, 70nsec static RAMs A10 – A13 are employed within the video section as temporary row character storage buffers. The intent of these static RAMs is to allow control of the bus to be returned as soon as possible to the microprocessor. This buffer also acts as pointer for locating character information within the dynamic RAM, thus avoiding sequential addressing for all rows.

Two 4-bit RAMs are stacked to form an 8-bit data bus, I/O 8 – I/O 15. For attribute storage and for two additional devices, character data is stored on I/O 0 – I/O 7. These chips are addressed by a common address bus CA0 – CA7. See the Video Section for more details.

Read Only Memory Array

The read only memory in the ATL-008 consists of from one to six ROMs and one EEPROM. There are two sites designed for sockets that allow the ICs to be stacked vertically; the other two sites accept single ROM sockets. All ROM sites are configured to accept the Intel universal site pinout. These ROMs are addressed by address bus A0 – A19 and share the same data bus ROM D0 – ROM D7. The terminal algorithm normally resides in the ROM while the terminal configuration manager (TCM) setup parameters reside in the EEPROM. (See Figure 6-3 for Memory Map.)

ROM Section - The read only memory array consists of from one to six ROMs and one EEPROM. There are four ROM sites on the board and two of them are upgradable to stacked sockets with Pin 20 separated to allow individual device selection. The ROM and EEPROM sites are configured in the Intel standard site (or JEDEC) pinout. This allows ROM sizes of from 8K × 8 to 32K × 8, or EEPROMs from 512 × 8 to 16K × 8.

The terminal algorithm normally resides in the ROMs while the EEROM is used to store TCM parameters. (See Figure 6-8 for timing diagram.)

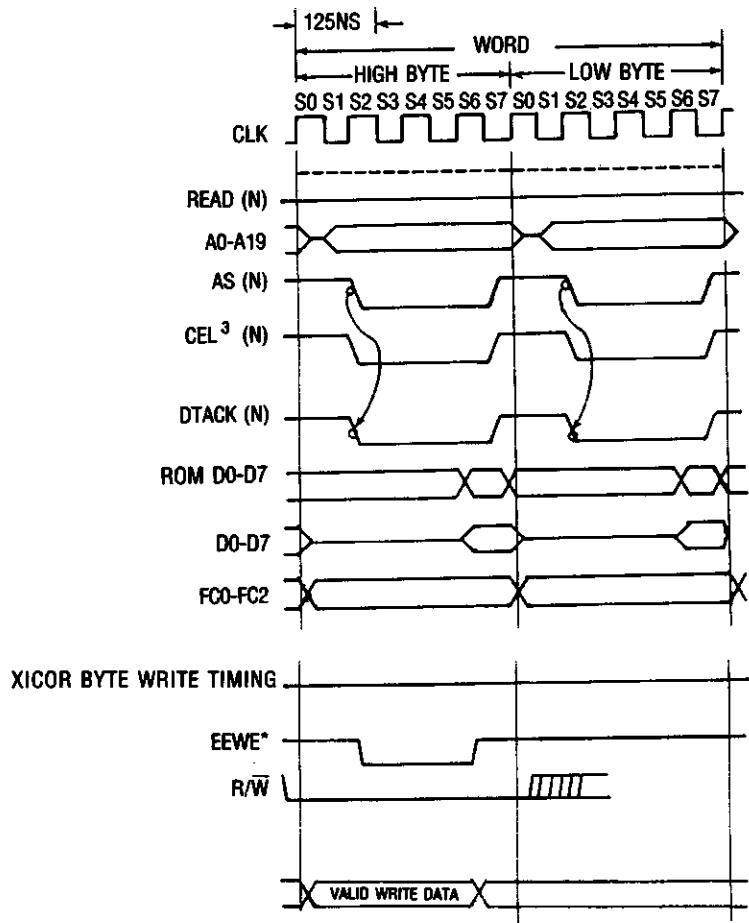
ROM decode is done by ROM Decode PAL A67. The ROM Control PAL controls the write enable line to the EEROM, enabling bidirectional buffer, A87. When ROM is accessed, it asserts DTACK*; when a peripheral is addressed, it asserts VPA*.

The EEPROM write line (EWE*) is latched in one state or another. Either RESET* = lo or a dummy read to the EEPROM will set EWE* = hi. A write to the EEPROM will assert EWE* = lo.

EEPROM - The ROM Array utilizes one Electrically Erasable PROM (EEPROM), A98. The socket can accommodate from 512 × 8 to 16K × 8 devices. The write enable line (EWE*) is controlled by the ROM Control PAL as described above. The firmware is responsible for the timing of the EWE* pulse width.

The EEPROM site accept both Xicor and Seeq type EEPROMs. The Xicor can write data with only a 200 nsec write pulse. The Seeq EEPROM requires firmware to assert WRITE ENABLE for 1 msec. The control PAL program is different for these two devices. (See Figures 6-8 and 6-9 for timing diagrams.)

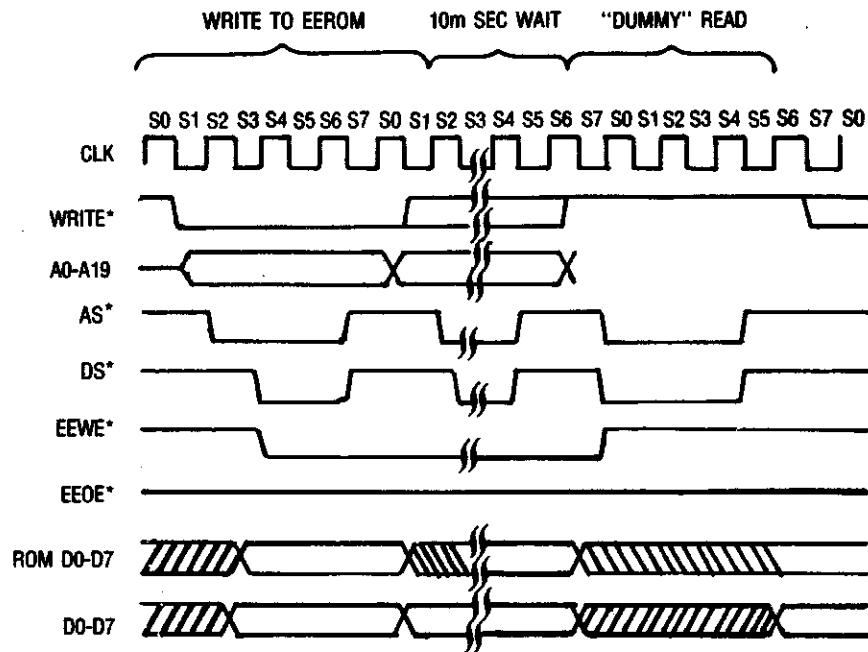
Figure 6-8
ROM/EEPROM
Read Word
Timing Diagram



AS and DTACK are the same as above.

J
B

Figure 6-9
EEPROM
Write Word
Timing Diagram



NOTE:

During the 10 millisecond wait normal bus activity does take place. The address and data are latched internally on the EEPROM chip. This releases the external signals (except EEWE* which must be low during the 10 millisecond period) for normal activity.

VIDEO SECTION

The video section reads character information to be displayed on the CRT from dynamic RAM, converts the character and attribute information into dot patterns, and sends this information to the monitor electronics to be displayed. The video section can be divided into four major blocks:

1. The CRT 9007, a CRT controller made by Standard Microsystems Corporation.
2. The CRT 9021, a video attribute controller also made by Standard Microsystems Corporation.
3. Four 1K × 4 bit static RAMs which store the character information for the active display row as well as the row table for the CRT 9007.
4. The clock generation circuit which produces the important timing waveforms.

When it is time to access dynamic RAM to obtain character information for a display row, the CRT 9007 will request the control of the system address and data bus from the 68008 processor. When the bus has been granted, the CRT 9007 will read two bytes from the static RAM which contain the main memory address of the row data. The CRT 9007 will then access this location in dynamic RAM and read either 80 or 132 consecutive locations for the row. The character data read from dynamic RAM is immediately displayed as well as written into the static RAM row buffers. This will allow the rest of the display row scan lines to display the data contained in the static RAM and return control of the system bus back to the 68008. Character data to be displayed is used to address the character generator, an 8K × 8 ROM. The character generator converts the ASCII character code into a dot pattern to be

9007 CRT Controller

displayed. The dot pattern on a parallel bus is loaded into the CRT 9021, as is the visual attribute information which selects reverse video, underline, half intensity, blink, and double high/wide. The CRT 9021 will combine the parallel dot information with the selected attributes and shift the resulting data out serially. This serial data is then amplitude-adjusted to provide the selected contrast level and is presented to the monitor electronics for display.

The ATL-008 video section is designed to display 27 rows of characters, each 13 scan lines in height. The vertical retrace period is 24 scan line times. This produces a horizontal scan frequency of 22.5 KHz. Each character is 9 dots wide in the 80 character mode and 7 dots wide in the 132 character mode. This produces a dot frequency of 25.9878 MHz for the 132 character mode and 20.2500 MHz in 80 column mode.

The CRT 9007 is a programmable video processor and controller which provides the central control of the video section. The CRT 9007 generates all the necessary timing to produce horizontal sync, vertical sync, and composite blanking. It also determines the correct times during the video display to request the system bus for a data transfer from dynamic RAM to the static RAM row buffers. The CRT 9007 generates the memory addresses for the dynamic RAM to access each of the 27 rows. It also outputs the scan line number for each of the 13 lines on a data row as well as generating a cursor pulse during the character time when the cursor should be displayed.

Two 74S374 octal latches and a 74LS245 bus buffer are used to interface the CRT 9007 to the system address bus. The latches are clocked by CCLK* to place the valid character address on the bus during the character time following the period when the address is valid. This allows the dynamic RAM section one full character time to access memory. The 74LS245 places the valid row table address on the bus during the character time when it becomes valid and without the latching delay. It also presents the 68008 address lines to the CRT 9007 at all times other than when the dynamic RAM is being accessed so that the CPU can address the read/write registers inside the CRT 9007. This method of interfacing the CRT 9007 to the system address bus allows the CRT 9007 to operate one character ahead of the character being read from dynamic RAM. Since the row table address must be read without delay, it is always obtained from the static RAM, which is much faster.

The CRT 9007 requests the system bus when it asserts DRB*, the Data Row Boundary indicator. This signal, as well as Visual Line Time (VLT), is synchronized to the video address latches through a 74S174 hex latch. When the 68008 grants the bus control to the CRT 9007 the signal CRTCBG* goes hi. This is tied to TSC*, the Tri-State Control input to the CRT 9007. When the TSC* input goes hi, the CRT 9007 will take the address bus out of tri-state and begin to drive valid addresses. The data bus is never driven by the CRT 9007 but is used by the 68008 to program the internal operational setup registers and allows the CRT 9007 to read the static RAM and obtain the two bytes which determine where the next data row is contained in dynamic RAM.

The scan line number for the next raster scan is output by the CRT 9007 during horizontal blanking. The signal SLG*, Scan Line Gate, indicates when SLD, Scan Line Data, contains the serial pattern forming the binary scan line number. When SLG* goes to the character clock will clock the contents of SLD into a serial-to-parallel shift register. The parallel outputs contain the binary scan line number for the next raster scan.

The horizontal and vertical sync signals are buffered from the CRT 9007 by an LS-type gate before being driven to the monitor electronics by an S-type gate.

The S gates are required to provide rapid state transitions and current sink capability. The CRT 9007 can display three different types of data rows which include normal high/normal wide, normal high/double wide, and double high/double wide. The display of either kind of double wide row requires that the video data is shifted out of the CRT 9021 at half the normal dot rate. Dividing the dot rate in half is done automatically by the CRT 9021 when the CRT 9007 indicates that the scan line is double wide. The CRT 9007 indicates this during the horizontal blanking period before the scan line by turning on the cursor signal for one character time. Except to indicate double wide, the cursor signal will only go hi when the position of the raster on the screen matches the x- and y-axis coordinates programmed into the CRT 9007 registers.

Double high character rows are generated by displaying each scan line number twice. The CRT 9007 is told what type of data row is to be displayed by the pattern on the two high order bits of the second byte read from the static RAM when it obtains the data row start address.

Smooth scrolling is another feature performed entirely by the CRT 9007. The start and stop boundaries of the smooth scrolling region are written into two registers of the CRT 9007. The number of scan lines this region is offset from normal is also programmable. When a frame interrupt occurs, the CPU will adjust the offset value to make the region scroll smoothly. The rate of scrolling is determined by the amount of offset which is added each frame interrupt.

Since the CRT 9007 has many modes of operation, it is best to clarify the way it is used in the ATL-008. The CRT 9007 is used in single row buffer mode. This means that the controller will take the system bus during scan line 0 of each of the 27 data rows on the screen. Each 8-bit character code has an 8-bit attribute with it in the dynamic RAM memory. The CRT 9007 will perform a continuous DMA burst of 80 or 132 cycles. Each cycle will access 16 bits of data to be simultaneously displayed on the screen during the scan line 0 and written into either the character row buffer for the low order 8 bits or the attribute row buffer for the high order 8 bits. The row data is addressed in a continuous block of dynamic RAM. The starting point of the row is determined by the CRT 9007 when it reads the row table data from the static RAM during the blanking period before the start of a new row. The row table is stored in static RAM in a contiguous format, which means that two bytes for each row are stored in a continuous table for the 27 rows. The starting address of this table is loaded by the CPU into a register of the CRT 9007.

9021 Video Attributes Controller

The second important component of the video section is the CRT 9021 video attributes controller. This is the mating part to the CRT 9007 and is used to create the effects of the video attributes, generate graphics characters, create the cursor form, shift out a video dot stream, and blank the video during monitor retrace periods.

The following chart shows which attributes are controlled by the dynamic RAM data bits:

RAM D15	alternate character set
RAM D14	latches the current attribute
RAM D13	unused (software flag)
RAM D12	underline
RAM D11	reverse video
RAM D10	blink
RAM D9	secure (blank)
RAM D8	half intensity

The reverse video and half intensity attributes are exclusive-ORed with control lines set up by the CPU in the video feature register. This is done to permanently turn on the attributes and reverse the effects of the memory bits. The attribute latch bit is ANDed with a control line which can turn off the effect of this memory bit so that no attributes will appear on the display. The alternate character set memory bit is also ANDed with a control line to prevent the bit from selecting the alternate set. This output is also ORed with another control bit so that the alternate set can be permanently turned on. The Mode Select inputs (MS0 and MS1) of the CRT 9021 determine the operating mode. The mode can be changed for each character and can include wide graphics, thin graphics, character mode with underline, and character mode without underline. The normal operational mode is character mode without underline (MS0, MS1 = 01), although thin line graphics mode can be selected in 80 column displays when the character code has bits 7 through 4 set to 1. Character mode with underline is selected when dynamic RAM bit 12 is set to 1. The block mode graphics are not used in the ATL-008.

Four different cursor styles are selected for display by using the BLC (BLink Cursor) and BKC (BlocK Cursor) inputs to the CRT 9021. The selection is made by two control lines BLINK CURS. and BLOCK CURS. which are set up by the CPU in the video feature register. The four selections are non-blinking block, blinking block, non-blinking underline, and blinking underline. The block cursor will fill the entire character cell while the underline will always be on the last raster line of the cell.

A unique dot pattern is output by the character generator for each scan line of a character. This parallel dot data is latched into the CRT 9021 on the rising edge of the LOAD* pulse. The corresponding attribute for the character is loaded into the CRT 9021 one LOAD* pulse before the character data. This feature of the CRT 9021 makes up for the extra character time embedded in the character data path as opposed to the attribute path because of the character generator access time. After a one character period internal delay through the CRT 9021, the dot data which is now combined with the attribute information is serially shifted out at the rate of the dot clock input, VDC. Although the parallel dot data loaded into the CRT 9021 is eight dots wide, the number of dots shifted out can be greater than eight. The mechanism to do this is called backfill. The number of dots to be shifted is determined by the number of dot clock cycles between load pulses, since shifting will continue until the next load pulse. Every dot shifted out beyond eight will be a duplicate of the first dot in character mode or the last dot in graphics mode. This allows for a nine-dot wide character cell using an eight-dot wide character generator.

Dot patterns are output from the character generator to create graphics characters in 132 column mode in the same way alphanumerics are generated. In 80 column mode, however, the graphics are produced by first placing the CRT 9021 in thin line graphics mode and then allowing the character generator to output a graphics segment number instead of a dot pattern. In this manner the graphic character is composed of thin line graphics segments defined inside the CRT 9021 and not by shifting out a dot pattern from the character generator.

The attribute enable input to the CRT 9021 allows the part to ignore all attributes except those which are valid when this input is hi. The CHABL (CHAracter BLank) input provides the effect of secure video by blocking the display of character data while continuing to display visual attributes and underline. The VSYNC (Vertical SYNC) input to the CRT 9021 is divided internally to provide the character blink rate of 1.875Hz with a 75/25 duty

L
B

cycle and the cursor blink rate of 3.75 Hz with a 50/50 duty cycle. The SLG+ and SLD inputs are the control lines from the CRT 9007 which allow the CRT 9021 to determine the scan line number for the next raster scan by using an internal serial-to-parallel shift register. CBLANK (Composite BLANK), which is input to the CRT 9021 from the CRT 9007, is the ORed state of horizontal and vertical blanking. This line is used to prevent any video from going to the monitor electronics during retrace periods. The cursor signal from the CRT 9007 tells the CRT 9021 when to display the cursor form on the display or go into double wide mode.

The half intensity input (INT IN) of the CRT 9021 has no function internally but is propagated through the CRT 9021 in sync with the other attributes until it is output as INT OUT. Outside the CRT 9021, it is used in an open collector gate arrangement to reduce the amplitude of the video waveform by about one-half. The video output of the CRT 9021 is buffered by an LS gate and then supplied as the D input to a 74S74. This latch will synchronize the dot data with the dot clock so that if the half-dot modulation is enabled, a full half dot clock wide pulse will be produced and no shaving of the dot will occur. A protective diode is placed on the video output to the monitor electronics so that the amplitude cannot exceed +5V.

The CRT 9021 is a mask programmed device which is set up with parameters specifically for Beehive.

1K × 4 Static RAMs

The video design uses four 1K × 4 static RAMs to provide a storage area for the row data as well as an area where the row table data can be kept. Since the static RAMs have two uses in the design, the addressing modes and data paths are fairly complex.

The static RAMs are filled with the character and attribute data coming out of the dynamic RAM main memory during the first scan line of each data row. As the static RAM is being filled, the character and attribute data are simultaneously being displayed on the monitor. For all the subsequent scan lines of the data row, the character codes to be displayed are read out of static RAM. This allows the CRT 9007 to return the bus control back to the 68008 until the first scan line of the next row. No accesses to main memory are required during vertical retrace.

During the horizontal blanking period before each display row, the static RAMs are used for a second purpose. During this time the CRT 9007 requests the system bus in preparation for the upcoming row transfer. As soon as the bus is granted the CRT 9007 will read two bytes of data from the static RAMs. This provides the starting address of main memory of the row data.

The row data can only be written during the DMA transfer which occurs during the first scan line of each row. The contiguous row table can only be written by the CPU during the vertical retrace period when the RAMs are not being used as a row data buffer. The CPU cannot read the row table data but only write it. The CRT 9007, on the other hand, cannot write to the row table but only read it.

When the static RAMs are used as a character and attribute row buffer, the addresses for reading and writing are generated by a 74LS393 octal binary counter. This counter increments its count by one for each character on a row and will count 0 to 79 or 0 to 131 depending on the row size. There is a 74LS244 in the design to keep this row address off the static RAMs when the address is being generated by the CPU to write the row table or by the CRT

9007 to read the row table. The high order address bit A9 on the static RAMs is hi during row table accesses and lo during use as a row buffer. This keeps the row data and row table data in separate blocks of memory.

A 74LS245 is used on the static RAM data bus so that data will only be driven from the system bus to the static RAM during scan line 0 of a data row or when the CPU writes the row table during vertical blanking. The 74LS245 is turned around to drive data out of the static RAMs onto the system bus when the CRT 9007 is reading the row table.

The 15 bits of row data read out of main memory to be displayed are divided into both character and attribute information. Data bits D0 – D7 represent the character code and are placed in one pair of $1K \times 4$ RAMs which effectively form a $1K \times 8$ device. Data bits D8 – D15 represent the attribute information and are placed in a second pair of static RAMs.

A 74LS174 and a 74S174 are used on the outputs of the character code static RAM buffer so that a full character clock period is allowed for accessing the RAM before the data is latched. The next character clock period is used to access the character generator ROM. The attribute buffer static RAM does not have this latch in the data path. The CRT 9021 accepts the attribute data one clock period before the corresponding character data and internally combines the two.

The WE* (Write Enable) input to the static RAMs is generated from two sources. Either 80 or 132 write pulses are created as a function of the character clock during the first scan line of each data row. This writes the data coming out of dynamic RAM into the static RAM buffers. The 68008 can also generate write pulses as a function of its DS* output when it is writing the row table into the static RAMs.

BUS ARBITER/ REFRESH CONTROLLER

The bus arbiter/refresh controller, PAL A35, provides two distinct separate functions:

- Bus arbitration between the DRAM refresher and the CRT controller, with the refresher having the highest priority.
- DRAM refresher, which provides a row address strobe (RAS*) pulse at a predetermined interval to refresh the contents of the dynamic RAM.

Bus Arbitration

Because the 68008 microprocessor has only one bus request input, a means to provide arbitration between the refresh controller and the CRT controller is required.

The Bus Arbiter/Refresh Controller State Map illustrates the states in which the controller operates. When the bus arbiter/refresh controller is in state A, it is in a loop waiting for a bus request from either the CRT controller or the refresher. In this state, bus request BR* of the controller is hi. When a refresh request (REFA AND REFB AND REFC) or a CRT controller bus request CRTRQ-L* (NREFA OR UREFB OR NREFC) occurs, the BARC transitions to state B where BR* is asserted lo. The BARC will remain in state B until the bus is granted by the CPU. It will then decide which request is present and go to stage C (if it is a refresh request) or state F (if it is a CRT request and there is not a refresh request). If it is a refresh request, the BARC will transition to state C and assert BR* = REFAEN* = lo, then will transition to state D (asserting REFAS* = lo). On the next clock the BARC will go to state A.

If, when in state B, there is no refresh request and the CRT bus request is active, the BARC will transition to state F after the CPU grants the bus. The BARC will stay in state F until the CRT controller is finished with the data transfer and will then go to state C to perform a refresh. It does this because data transfers are known to be long enough to always have a refresh request waiting at the end. This eliminates the extra arbitration cycle.

Dynamic RAM Refresher

Data retention in the dynamic RAM is achieved by means of a single transistor dynamic storage cell. The basic storage element is a capacitor which provides both low power consumption and high speed data access time. These storage cells, however, require refreshing for data retention. Refreshing is provided by performing a RAS* only memory cycle while addressing each combination of address inputs within a 2.4 msec time period.

The basic clock drive for the refresher is a 3.99 MHz signal from UPICLK, from A51. This drives the clock input of the bus arbiter/refresh controller, PAL A35. REFCLK* drives the binary counter A49. This counter counts up until a value of 76 is reached (REF A = REF B = REFC = hi). The clock to the counter is turned off until the refresh request is recognized and the bus is granted to the refresher. When REFAEN* is brought lo, the counter outputs are cleared and the cycle starts over again.

Refer once again to the state map and assume the controller begins again from state A where it is looking for a bus request either from the CRT controller or the refresher. Assume the CRT controller is not requesting the bus, CRTCBR* is not asserted. However, the refresher is not requesting the bus after the divided-by-76 counter outputs REFA, REFB and REFC have all been asserted hi. The controller now drops into state B where BR* is asserted lo. At this time the controller must arbitrate between the CRT controller or the refresher. The arbitrator gives priority to the refresher by looking for REFA, REFB and REFC all to be asserted hi. The controller drops to state C when input BG* is asserted lo and AS* returns to a hi. Refresh Address Enable, REFAEN*, is now asserted lo. REFAEN* gates A17, A18, A19 and the refresh address bits A1 – A8 from A40 onto the address bus.

Refreshing each address within the DRAM is accomplished by an 8-bit counter, A41, and an octal buffer, A40. The counter will sequence through all 256 addresses within a 4.8 msec period. The counter is clocked to the next address by REFAEN*, Pin 1, going lo.

REFAEN* is asserted lo when the controller drops to state C, thus clocking one of the 256 address combinations onto the bus. The controller then drops to state D where refresh address strobe REFAS* is asserted lo. This signal is buffered by a 3-state buffer/driver A33 and becomes AS*. (This AS* is wired OR-ed to AS* from the microprocessor.) AS*, A20 going lo with A17 = 0, A18 = 0, and A19 = 1 at the PAL, generate the output signal DRAMSEL* at Pin 18. DRAMSEL* causes RAS* to be asserted lo after a 15 nsec delay via delay line A3. RAS* going lo strobes the row address into the RAM, thus performing a refresh for that address.

The controller now jumps back to state A where it waits until another refresh request and then initiates another refresh sequence. The refreshing of the RAM is distributed over the 2.4 msec refresh period (4.8 msec for 64K × 1 RAMs) occurring on 19 μsec intervals.

APPENDIX

A

**ASCII CODE
CHART**

ASCII CHARACTER CHART

DEC	HEX	OCT	BINARY	CHR	DEC	HEX	OCT	BINARY	CHR	DEC	HEX	OCT	BINARY	CHR	DEC	HEX	OCT	BINARY	CHR	
000	00	000	00000000	NUL	C/A @	032	20	040	00100000	SP	064	40	100	01000000	@	096	60	140	01100000	`
001	01	001	00000001	SOH	C/A A	033	21	041	00100001	!	065	41	101	01000001	A	097	61	141	01100001	a
002	02	002	00000010	STX	C/A B	034	22	042	00100010	"	066	42	102	01000010	B	098	62	142	01100010	b
003	03	003	00000011	ETX	C/A C	035	23	043	00100011	#	067	43	103	01000011	C	099	63	143	01100011	c
004	04	004	00000100	EOT	C/A D	036	24	044	00100100	\$	068	44	104	01000100	D	100	64	144	01100100	d
005	05	005	00000101	ENQ	C/A E	037	25	045	00100101	%	069	45	105	01000101	E	101	65	145	01100101	e
006	06	006	00000110	ACK	C/A F	038	26	046	00100110	&	070	46	106	01000110	F	102	66	146	01100110	f
007	07	007	00000111	BEL	C/A G	039	27	047	00100111	'	071	47	107	01000111	G	103	67	147	01100111	g
008	08	010	00001000	BS	C/A H	040	28	050	00101000	(072	48	110	01001000	H	104	68	150	01101000	h
009	09	011	00001001	HT	C/A I	049	29	051	00101001)	073	49	111	01001001	I	105	69	151	01101001	i
010	0A	012	00001010	LF	C/A J	042	2A	052	00101010	*	074	4A	112	01001010	J	106	6A	152	01101010	j
011	0B	013	00001011	VT	C/A K	043	2B	053	00101011	+	075	4B	113	01001011	K	107	6B	153	01101011	k
012	0C	014	00001100	FF	C/A L	044	2C	054	00101100	,	076	4C	114	01001100	L	108	6C	154	01101100	l
013	0D	015	00001101	CR	C/A M	045	2D	055	00101101	-	077	4D	115	01001101	M	109	6D	155	01101101	m
014	0E	016	00001110	SO	C/A N	046	2E	056	00101110	.	078	4E	116	01001110	N	110	6E	156	01101110	n
015	0F	017	00001111	SI	C/A O	047	2F	057	00101111	/	079	4F	117	01001111	O	111	6F	157	01101111	o
016	10	020	00010000	DLE	C/A P	048	30	060	00110000	0	080	50	120	01010000	P	112	70	160	01110000	p
017	11	021	00010001	DC1	C/A Q	049	31	061	00110001	1	081	51	121	01010001	Q	113	71	161	01110001	q
018	12	022	00010010	DC2	C/A R	050	32	062	00110010	2	082	52	122	01010010	R	114	72	162	01110010	r
019	13	023	00010011	DC3	C/A S	051	33	063	00110011	3	083	53	123	01010011	S	115	73	163	01110011	s
020	14	024	00010100	DC4	C/A T	052	34	064	00110100	4	084	54	124	01010100	T	116	74	164	01110100	t
021	15	025	00010101	NAK	C/A U	053	35	065	00110101	5	085	55	125	01010101	U	117	75	165	01110101	u
022	16	026	00010110	SYN	C/A V	054	36	066	00110110	6	086	56	126	01010110	V	118	76	166	01110110	v
023	17	027	00010111	ETB	C/A W	055	37	067	00110111	7	087	57	127	01010111	W	119	77	167	01110111	w
024	18	030	00011000	CAN	C/A X	056	38	070	00111000	8	088	58	130	01011000	X	120	78	170	01111000	x
025	19	031	00011001	EM	C/A Y	057	39	071	00111001	9	089	59	131	01011001	Y	121	79	171	01111001	y
026	1A	032	00011010	SUB	C/A Z	058	3A	072	00111010	:	090	5A	132	01011010	Z	122	7A	172	01111010	z
027	1B	033	00011011	ESC	C/A [059	3B	073	00111011	;	091	5B	133	01011011	[123	7B	173	01111011	{
028	1C	034	00011100	FS	C/A \	060	3C	074	00111100	<	092	5C	134	01011100	\	124	7C	174	01111100	
029	1D	035	00011101	GS	C/A]	061	3D	075	00111101	=	093	5D	135	01011101]	125	7D	175	01111101	}
030	1E	036	00011110	RS	C/A ^	062	3E	076	00111110	>	094	5E	136	01011110	^	126	7E	176	01111110	~
031	1F	037	00011111	US	C/A _	063	3F	077	00111111	?	095	5F	137	01011111	_	127	7F	177	01111111	DEL

* C/A = CONTROL/ALT

EXPLANATION OF CONTROL CODES

- | | | | |
|---------------------------|------------------------|---------------------------------|-----------------------|
| NUL = Null | HT = Horizontal Tab | DC2 = Device Control 2 | ESC = Escape |
| SOH = Start of Heading | LF = Line Feed | DC3 = Device Control 3 | FS = File Separator |
| STX = Start of Text | VT = Vertical Tab | DC4 = Device Control 4 | GS = Group Separator |
| ETX = End of Text | FF = Form Feed | NAK = Negative Acknowledge | RS = Record Separator |
| EOT = End of Transmission | CR = Carriage Return | SYN = Synchronous Idle | US = Unit Separator |
| ENQ = Enquiry | SO = Shift Out | ETB = End of Transmission Block | SP = Space |
| ACK = Acknowledge | SI = Shift In | CAN = Cancel | DEL = Delete |
| BEL = Bell | DLE = Data Link Escape | EM = End of Medium | |
| BS = Backspace | DC1 = Device Control 1 | SUB = Substitute | |

B

ATL-008 MEMORY MAP

INTRODUCTION

Only hardware information is given in this listing of the ATL-008 memory map. A summary of address duplications and a list of which devices are accessed by what address ranges are followed by a detailed description of the ATL-008 memory map.

LOW	HIGH	DESCRIPTION
\$00000	\$17FFF	System ROM - 96K (6 - 16K × 8 bit, 27128 type)
\$3E000	\$3E1FF	EEROM - 512-byte Configuration - XICOR
\$3E000	\$3E800	EEROM - 2048-byte Configuration - SEEQ
\$40000	\$40007	Serial I/O - Zilog 8530
\$44000	\$44000	8041 Keyboard and Input Line Device (Data Register)
\$44002	\$44000	8041 Keyboard and Input Line Device (Command/Status Register)
\$48000	\$48000	System Control Register (write only)
\$4C000	\$4C07F	CRT Controller - SMC 9007
\$50000	\$50000	PC Board Revision Level ROM
\$54000	\$54000	CRT Contrast Adjustment Register
\$58000	\$58000	Video Features Register Device (write only)
\$5C000	\$5C000	Unused device register
\$80000	\$87FFF	System RAM - (32K RAM Configuration)
\$80000	\$9FFFF	System RAM - (128K RAM Configuration)
\$A0000	\$A3FFF	CRT Controller Row Buffers

The addresses from \$A0000 to \$A3FFFF require some explanation: processor writes to RAM locations \$80000 through \$801FF are also writes to corresponding locations \$A0000 through \$A01FF. However, only the CRT controller may read from \$A0000 through \$A01FF.

Device Address Duplications

Due to the address decoding technique used, some devices appear to be addressed in several different places. The following is a summary of those duplications, as well as a list of which devices (by "A" number) are accessed by what address ranges.

A

1. PROM

LOGICAL ADDRESS RANGE	PHYSICAL MEMORY ADDRESSED
000000-003FFF	0000-3FFF of PROM #1, A98 (bottom)
004000-007FFF	0000-3FFF of PROM #2, A98 (top)
008000-00BFFF	0000-3FFF of PROM #3, A99 (bottom)
00C000-00FFFF	0000-3FFF of PROM #4, A99 (top)
010000-013FFF	0000-3FFF of PROM #5, A100
014000-017FFF	0000-3FFF of PROM #6, A101
018000-01FFFF	Decoded but not used

2. EEPROM

A. 512 × 8 EEPROM, XICOR

LOGICAL ADDRESS RANGE	PHYSICAL MEMORY ADDRESSED
020000-025FFF	None
026000-0261FF	000-1FF EEPROM, read, write
026200-0263FF	000-1FF EEPROM, read, write
026400-0265FF	000-1FF EEPROM, read, write
026600-0267FF	000-1FF EEPROM, read, write
026800-0269FF	000-1FF EEPROM, read
026A00-026BFF	000-1FF EEPROM, read
026C00-026DFF	000-1FF EEPROM, read
026E00-026FFF	000-1FF EEPROM, read
027000-0271FF	000-1FF EEPROM, read, write
027200-0273FF	000-1FF EEPROM, read, write
027400-0275FF	000-1FF EEPROM, read, write
027600-0277FF	000-1FF EEPROM, read, write
027800-0279FF	000-1FF EEPROM, read
027A00-027BFF	000-1FF EEPROM, read
027C00-027DFF	000-1FF EEPROM, read
027E00-027FFF	000-1FF EEPROM, read
028000-02DFFF	None
02E000-02E1FF	000-1FF EEPROM, read, write
02E200-02E3FF	000-1FF EEPROM, read, write
02E400-02E5FF	000-1FF EEPROM, read, write
02E600-02E7FF	000-1FF EEPROM, read, write
02E800-02E9FF	000-1FF EEPROM, read
02EA00-02EBFF	000-1FF EEPROM, read
02EC00-02EDFF	000-1FF EEPROM, read
02EE00-02EFFF	000-1FF EEPROM, read
02F000-02F1FF	000-1FF EEPROM, read, write
02F200-02F3FF	000-1FF EEPROM, read, write
02F400-02F5FF	000-1FF EEPROM, read, write
02F600-02F7FF	000-1FF EEPROM, read, write
02F800-02F9FF	000-1FF EEPROM, read
02FA00-02FBFF	000-1FF EEPROM, read
02FC00-02FDFF	000-1FF EEPROM, read
02FE00-02FFFF	000-1FF EEPROM, read

A. 512 × 8 EEPROM, XICOR (cont.)

LOGICAL ADDRESS RANGE	PHYSICAL MEMORY ADDRESSED
030000-035FFF	Decoded but not used
036000-0361FF	000-1FF EEPROM, read, write
036200-0363FF	000-1FF EEPROM, read, write
036400-0365FF	000-1FF EEPROM, read, write
036600-0367FF	000-1FF EEPROM, read, write
036800-0369FF	000-1FF EEPROM, read
036A00-036BFF	000-1FF EEPROM, read
036C00-036DFF	000-1FF EEPROM, read
036E00-036FFF	000-1FF EEPROM, read
037000-0371FF	000-1FF EEPROM, read, write
037200-0373FF	000-1FF EEPROM, read, write
037400-0375FF	000-1FF EEPROM, read, write
037600-0377FF	000-1FF EEPROM, read, write
037800-0379FF	000-1FF EEPROM, read
037A00-037BFF	000-1FF EEPROM, read
037C00-037DFF	000-1FF EEPROM, read
037E00-037FFF	000-1FF EEPROM, read
038000-03dFFF	Decoded but not used
03E000-03E1FF	000-1FF EEPROM, read, write
03E200-03E3FF	000-1FF EEPROM, read, write
03E400-03E5FF	000-1FF EEPROM, read, write
03E600-03E7FF	000-1FF EEPROM, read, write
03E800-03E9FF	000-1FF EEPROM, read
03EA00-03EBFF	000-1FF EEPROM, read
03EC00-03EDFF	000-1FF EEPROM, read
03EE00-03EFFF	000-1FF EEPROM, read
03F000-03F1FF	000-1FF EEPROM, read, write
03F200-03F3FF	000-1FF EEPROM, read, write
03F400-03F5FF	000-1FF EEPROM, read, write
03F600-03F7FF	000-1FF EEPROM, read, write
03F800-03F9FF	000-1FF EEPROM, read
03FA00-03FbFF	000-1FF EEPROM, read
03FC00-03FDFF	000-1FF EEPROM, read
03FE00-03FFFF	000-1FF EEPROM, read

B. 2048 × 8 EEPROM, SEEQ

LOGICAL ADDRESS RANGE	PHYSICAL MEMORY ADDRESSED
020000-021FFF	Decoded but not used
022000-0227FF	000-7FF EEPROM, write
022800-022FFF	000-7FF EEPROM, write
023000-0237FF	000-7FF EEPROM, write
023800-023FFF	000-7FF EEPROM, write

A

B. 2048 × 8 EEPROM, SEEQ (cont.)

LOGICAL ADDRESS RANGE	PHYSICAL MEMORY ADDRESSED
024000-025FFF	Decoded but not used
023000-0237FF	000-7FF EEPROM, write, read
023800-023FFF	000-7FF EEPROM, write, read
024000-0247FF	000-7FF EEPROM, write, read
024800-024FFF	000-7FF EEPROM, write, read
028000-029FFF	Decoded but not used
02A000-02A7FF	000-7FF EEPROM, write
02A800-02AFFF	000-7FF EEPROM, write
02B000-02B7FF	000-7FF EEPROM, write
02B800-02BFFF	000-7FF EEPROM, write
02C000-02DFFF	Decoded but not used
02E000-02E7FF	000-7FF EEPROM, write, read
02E800-02EFFF	000-7FF EEPROM, write, read
02F000-02F7FF	000-7FF EEPROM, write, read
02F800-02FFFF	000-7FF EEPROM, write, read
030000-031FFF	Decoded but not used
032000-0327FF	000-7FF EEPROM, write
032800-032FFF	000-7FF EEPROM, write
033000-0337FF	000-7FF EEPROM, write
033800-033FFF	000-7FF EEPROM, write
034000-035FFF	Decoded but not used
036000-0367FF	000-7FF EEPROM, write, read
036800-036FFF	000-7FF EEPROM, write, read
037000-0377FF	000-7FF EEPROM, write, read
037800-037FFF	000-7FF EEPROM, write, read
038000-039FFF	Decoded but not used
03A000-03A7FF	000-7FF EEPROM, write
03A800-03AFFF	000-7FF EEPROM, write
03B000-03B7FF	000-7FF EEPROM, write
03B800-03BFFF	000-7FF EEPROM, write
03C000-03CFFF	Decoded but not used
03E000-03E7FF	000-7FF EEPROM, write, read
03E800-03EFFF	000-7FF EEPROM, write, read
03F000-03F7FF	000-7FF EEPROM, write, read
03F800-03FFFF	000-7FF EEPROM, write, read

3. Dynamic RAM

A. 32K RAM

**LOGICAL ADDRESS
RANGE**

080000-087FFF
088000-08FFFF
090000-097FFF
098000-09FFFF
0A0000-0A7FFF
0A8000-0AFFFF
0B0000-0B7FFF
0B8000-0BFFFF

**PHYSICAL MEMORY
ADDRESSED**

0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write
0000-7FFF 32K RAM, read, write

B. 128K RAM

**LOGICAL ADDRESS
RANGE**

080000-09FFFF
0A0000-0BFFFF

**PHYSICAL MEMORY
ADDRESSED**

00000-1FFFF 128K RAM, read, write
00000-1FFFF 128K RAM, read, write

4. Static RAM (Even Addresses Only)

**LOGICAL ADDRESS
RANGE**

0A0000-0A01FE

0A0200-0A03FE

.
.
.

0BFC00-0BFDFE

0BFE00-0BFFFE

**PHYSICAL MEMORY
ADDRESSED**

00-FF Static RAM Row Table, write
080000-0801FE DRAM, write

00-FF Static RAM Row Table, write
080200-0803FE DRAM, write

.
.
.

00-FF Static RAM Row Table, write
09FC00-09FCFE DRAM, write

00-FF Static RAM Row Table, write
09FE00-09FFFE DRAM, write

5. I/O Decodes

**LOGICAL ADDRESS
RANGE**

040000-043FFF
044000-047FFF
048000-04BFFF

**PHYSICAL MEMORY
ADDRESSED**

SCC, Serial Comm. Controller (8530)
UPI, Universal Peripheral Interface (8041)
SCR, System Control Register (74LS374)



**Detailed
Memory Map
Description**

Zilog 8530 SIO

Interrupt Type: Vectored
Interrupt Level: 5

_siodv	equ	\$40000	serial i/o device
_sioacm	equ	_siodv	aux port command register
_siomcm	equ	_siodv+2	main port command register
_sioadt	equ	_siodv+4	aux port data register
_siomdt	equ	_siodv+6	main port data register

Indices to Registers Inside the Serial I/O Device

_siow1	equ	1	xmit/rcv interrupt and data transfer mode
_siow2	equ	2	interrupt vector
_siow3	equ	3	receive parameters and control register
_siow4	equ	4	transmit/receive misc and control
_siow5	equ	5	transmit parameters and control
_siow6	equ	6	first byte of 16 bit sync character
_siow7	equ	7	second byte of 16 bit sync character
_siow8	equ	8	alternate data register
_siow9	equ	9	master interrupt control
_siow10	equ	10	misc transmit/receive control bits
_siow11	equ	11	clock mode control
_siow12	equ	12	low order byte - baud rate counter
_siow13	equ	13	high order byte - baud rate counter
_siow14	equ	14	miscellaneous control bits
_siow15	equ	15	interrupt enables
_ioxtal	equ	36864	frequency of serial i/o crystal in `khz

Intel 8041 Equates

UPI-8041a Keyboard and I/O Level Interface Defines

_upidt	equ	\$44000	8041 keyboard and input line device - data
_upics	equ	\$44002	8041 keyboard and input line device - command/status

Bits with Status Byte (given by UPI-8041a)

_uioerr	equ	\$80	there has been a serial i/o failure
_u26in	equ	\$40	p 26 input
_u22in	equ	\$20	p 22 input
_upin	equ	\$10	data byte is parallel input from p 10-p 17
_utxbsy	equ	\$02	upi transmitter is busy and unable to accept data
_urxrdy	equ	\$01	upi receiver has serial or parallel data

Bits Within the Command Byte (given to the UPI-8041a)

_update	equ	\$80	the next data byte is parallel data (in or out)
_upout	equ	\$40	the parallel direction is out
_uerrst	equ	\$20	reset the i/o error flag
_ustst	equ	\$08	send the self-test report
_uloop	equ	\$04	enter loop-back mode
_u21out	equ	\$02	p 21 output
_u27out	equ	\$01	p 27 output

Bits Within the Parallel Data Byte (given by the 8041a)

_ioindsra	equ	0	\$01 - 8041 main - dsr status
_ioincia	equ	1	\$02 - 8041 main - data signal rate sel
_ioinrta	equ	2	\$04 - 8041 main - ring indicator
_iointma	equ	3	\$08 - 8041 main - test mode
_ioinadr	equ	4	\$10 - 8041 aux - aux dev rdy
_ioinadr	equ	5	\$20 - 8041 aux - data terminal ready
_ioincl	equ	6	\$40 - 8041 422 - c lead installed
_ioin422	equ	7	\$80 - 8041 422 - 422 interface

Keyboard Defines

_kalck	equ	\$80	alpha lock mode bit
_klock	equ	\$40	shift lock mode bit
_kshlk	equ	\$10	bit for shift lock key
_klfcn	equ	\$08	bit for left control key
_krtc	equ	\$04	bit for right control key
_klfsh	equ	\$02	bit for left shift key
_krtsh	equ	\$01	bit for right shift key
_klvl	equ	_kshlk+ _klfcn+ _krtc+ _klfsh+ _krtsh	all level keys

Commands Which Can Be Sent to the Keyboard

_ks1200	equ	\$20	turn on short 1200 Hz tone
_kc1200	equ	\$21	turn on continuous 1200 Hz tone
_kc600	equ	\$24	turn on continuous 600 Hz tone
_kcwarb	equ	\$27	turn on continuous warble
_kcring	equ	\$2A	turn on continuous ring
_ktoff	equ	\$2C	turn off all tones
_khivol	equ	\$2D	turn on high volume
_klovol	equ	\$2E	turn on low volume
_kclik	equ	\$2F	click once
_kenscn	equ	\$31	enable keyboard scan
_kdiscn	equ	\$32	disable keyboard scan
_kinit	equ	\$33	reinitialize keyboard
_ksrprt	equ	\$34	send the selftest report and version data
_kreset	equ	\$35	reset the keyboard
_kldsta	equ	\$36	this is the start of the status key matrix numbers
_kstcrc	equ	\$37	send me the level key crc

Defines for the Keyboard Audio Functions

```

_audof    equ    0        turn off all tones
_s1200    equ    1        short 1200 Hz tone
_c1200    equ    2        continuous 1200 Hz tone
_s600     equ    3        short 600 Hz tone
_c600     equ    4        continuous 600 Hz tone
_swarb    equ    5        short warb Hz tone
_cwarb    equ    6        continuous warb Hz tone
_sring    equ    7        short ring Hz tone
_cring    equ    8        continuous ring Hz tone

```

Dead Key Code (for key table)

```

_kdead    equ    $FF

```

KEY MATRIX NUMBER CHART

-F8-	-A0-	—A1-	—A2-	—A3-	—A4-	—A5-	—A6-	—A7-	—C7-	—C6	—C4	—C1
-BD-	B8 B5 B0	AD A8 CD C8	D5 D0 DD D8	F5 F0 ED	—E8-	E5 E0	C5 C0					
BB	-BA B3 B2	AB AA CB CA	D3 D2 DB DA	F3 F2	-EB- EA	E2 E3	C3 C2					
BF	-BE- B7 B6	AF AE CF CE	D7 D6 DF DE	F7	—F6— EF	EE E7	E6 E4					
FD BC B9	—B4- B1 AC	A9 CC C9 D4	D1 DC D9 F4	—F1— -EC-	—E9- E1 E4							
	-FB-		FA	—FC- -F9-								

System Control Register

```

_scrdv    equ    $48000    system control register device - output bits

_sc42b    equ    $01        current loop/rs422 serial i/o mode selection
_sco3b    equ    $02        other/rs232 serial i/o mode selection
_sspdb    equ    $04        modem speed selection bit
_sanlb    equ    $08        modem analog selection bit
_srdlb    equ    $10        modem readback loop bit
_sadsb    equ    $20        aux port dsr signal (negative)
_sinex    equ    $40        i/o clock internal/external line
_stmeb    equ    $80        5 millisecond timer interrupt enable

```

SMC 9007 CRT Controller Defines

```

_crt dv    equ    $4C000    crt controller device

```

Registers in CRT Controller (expressed as offsets from _crt dv)

```

_vr00w    equ    $00*2    r0 - characters per horizontal period
_vr01w    equ    $01*2    r1 - characters per data row (-1)
_vr02w    equ    $02*2    r2 - characters per horizontal delay period

```

<code>_vr03w</code>	<code>equ</code>	<code>\$03*2</code>	r3 - characters per horizontal sync width
<code>_vr04w</code>	<code>equ</code>	<code>\$04*2</code>	r4 - scan lines per vertical sync width
<code>_vr05w</code>	<code>equ</code>	<code>\$05*2</code>	r5 - scan lines per vertical delay period (-1)
<code>_vr06w</code>	<code>equ</code>	<code>\$06*2</code>	r6 - pin configuration/skew bits register
<code>_vr07w</code>	<code>equ</code>	<code>\$07*2</code>	r7 - visible data rows per frame (-1)
<code>_vr08w</code>	<code>equ</code>	<code>\$08*2</code>	r8 - scan lines/vertical period (hi 3 bits)
<code>_vr09w</code>	<code>equ</code>	<code>\$09*2</code>	r9 - scan lines/vertical period (lo 8 bits)
<code>_vr0aw</code>	<code>equ</code>	<code>\$0A*2</code>	rA - dma control register
<code>_vr0bw</code>	<code>equ</code>	<code>\$0B*2</code>	rB - control register
<code>_vr0cw</code>	<code>equ</code>	<code>\$0C*2</code>	rC - table start address (lo 8 bits)
<code>_vr0dw</code>	<code>equ</code>	<code>\$0D*2</code>	rD - table start address (hi 6 bits)
<code>_vr0ew</code>	<code>equ</code>	<code>\$0E*2</code>	rE - auxiliary address register (lo 8 bits)
<code>_vr0fw</code>	<code>equ</code>	<code>\$0F*2</code>	rF - auxiliary address register (hi 6 bits)
<code>_vr10w</code>	<code>equ</code>	<code>\$10*2</code>	r10 - sequential break register 1
<code>_vr11w</code>	<code>equ</code>	<code>\$11*2</code>	r11 - data row start register
<code>_vr12w</code>	<code>equ</code>	<code>\$12*2</code>	r12 - data row end/sequential break reg 2
<code>_vr13w</code>	<code>equ</code>	<code>\$13*2</code>	r13 - auxiliary address register 2 (lo 8 bits)
<code>_vr14w</code>	<code>equ</code>	<code>\$14*2</code>	r14 - auxiliary address register 2 (hi 6 bits)
<code>_vr15w</code>	<code>equ</code>	<code>\$15*2</code>	r15 - start command
<code>_vr16w</code>	<code>equ</code>	<code>\$16*2</code>	r16 - reset command
<code>_vr17w</code>	<code>equ</code>	<code>\$17*2</code>	r17 - smooth scroll offset register
<code>_vr18w</code>	<code>equ</code>	<code>\$18*2</code>	r18 - vertical cursor register
<code>_vr19w</code>	<code>equ</code>	<code>\$19*2</code>	r19 - horizontal cursor register
<code>_vr1aw</code>	<code>equ</code>	<code>\$1A*2</code>	r1A - interrupt enable register
<code>_vr38r</code>	<code>equ</code>	<code>\$38*2</code>	r38 - vertical cursor register (read only)
<code>_vr39r</code>	<code>equ</code>	<code>\$39*2</code>	r39 - horizontal cursor register (read only)
<code>_vr3ar</code>	<code>equ</code>	<code>\$3A*2</code>	r3A - status register (read only)
<code>_vr3br</code>	<code>equ</code>	<code>\$3B*2</code>	r3B - vertical light pen register (read only)
<code>_vr3cr</code>	<code>equ</code>	<code>\$3C*2</code>	r3C - horizontal light pen register (read only)

Character Attribute Bits for the Video Attribute Controller

<code>_ahalf</code>	<code>equ</code>	<code>\$01</code>	half intensity bit
<code>_ablak</code>	<code>equ</code>	<code>\$02</code>	blank video bit
<code>_abljk</code>	<code>equ</code>	<code>\$04</code>	blinking video bit
<code>_arevs</code>	<code>equ</code>	<code>\$08</code>	reverse video bit
<code>_aulin</code>	<code>equ</code>	<code>\$10</code>	underline video bit
<code>_aflag</code>	<code>equ</code>	<code>\$20</code>	unused bit - possible use as character flag
<code>_altch</code>	<code>equ</code>	<code>\$40</code>	attribute latch bit
<code>_aalcg</code>	<code>equ</code>	<code>\$80</code>	alternate character generator bit

Defines for Double High/Wide Flags

(correspond to bits 14, 15 in 9007 format)

<code>_dblht</code>	<code>equ</code>	<code>\$80</code>	double high/wide top row
<code>_dblhb</code>	<code>equ</code>	<code>\$C0</code>	double high/wide bottom row
<code>_dblw</code>	<code>equ</code>	<code>\$40</code>	double wide row
<code>_dbls</code>	<code>equ</code>	<code>\$00</code>	the usual single high/wide row

Video Features Register

_viddv	equ	\$58000	video features register device - output bits
_vacgb	equ	\$01	video alternate character generator selection
_vblcb	equ	\$02	video block cursor selection
_vnbkcb	equ	\$04	video non-blinking cursor selection
_vrvr	equ	\$08	video reverse selection
_vfish	equ	\$10	video full intensity screen selection
_valeb	equ	\$20	video attribute latch enable selection
_vagbb	equ	\$40	video alternate character generator bit enable
_vcolb	equ	\$80	video oscillator 80/132 column selection

C

PAL EQUATIONS & STATE TABLES

INTRODUCTION

The Programmed Array Logic ICs are identified by their reference designators as indicated on the logic board and on the schematics.

A35 PAL

Bus Arbiter/Refresh Controller PAL

PAL type 16R4

13 July 1983 Revision 2.0

Inputs

2	upicl	3.9936 MHz clock
3	refa	
4	refb	refresh request when
5	refc	refa=refb=refc=hi
6	as_l	address strobe, negative true
7	bg_l	bus grant from the 68008, negative true
9	crtrq_l	crt bus request, negative true

Controls

12	enb12
13	enb13
18	enb18
19	enb19

Outputs

19	a19	address bit 19
18	a18	address bit 18
17	br_l	bus request to 68008, negative true
16	rfas_l	refresh address strobe, negative true
15	rfae_l	refresh address enable, negative true
14	crtg_l	crt controller bus grant, negative true
13	refclk	refresh timer clock, goes lo on terminal count
12	a17	address bit 17

Equations

$$\text{enb12} = \sim \text{rfae_l}$$

$$\text{enb13} = 1$$

$$\text{enb18} = \sim \text{rfae_l}$$

$$\text{enb19} = \sim \text{rfae_l}$$

$$\text{refclk} = (\text{upicl} \& \sim \text{refa}) + (\text{upicl} \& \sim \text{refb}) + (\text{upicl} \& \sim \text{refc})$$

$$\text{a19} = \text{rfae_l}$$

$$\text{a18} = \sim \text{rfae_l}$$

$$\text{a17} = \sim \text{rfae_l}$$

$$\text{rfae_l} = (\text{rfas_l} \& \sim \text{br_l} \& \text{crtg_l} \& \sim \text{bg_l} \& \text{as_l} \& \text{refc} \& \text{refb} \& \text{refa}) + (\sim \text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \text{crtg_l} \& \sim \text{bg_l})$$

$$\text{rfas_l} = (\sim \text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \text{crtg_l} \& \sim \text{bg_l})$$

$$\text{br_l} = (\text{rfae_l} \& \text{rfas_l} \& \text{crtg_l} \& \text{bg_l} \& \text{refc} \& \text{refb} \& \text{refa}) + (\text{rfae_l} \& \text{rfas_l} \& \text{crtg_l} \& \text{bg_l} \& \sim \text{crtrq_l}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \text{crtg_l}) + (\text{rfas_l} \& \sim \text{br_l} \& \text{crtg_l} \& \sim \text{bg_l}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{bg_l} \& \text{as_l} \& \sim \text{crtrq_l}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{bg_l} \& \text{as_l} \& \text{refc} \& \text{refb} \& \text{refa})$$

$$\text{crtg_l} = (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{bg_l} \& \text{as_l} \& \sim \text{crtrq_l} \& \sim \text{refc}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{bg_l} \& \text{as_l} \& \sim \text{crtrq_l} \& \sim \text{refb}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{bg_l} \& \text{as_l} \& \sim \text{crtrq_l} \& \sim \text{refa}) + (\text{rfae_l} \& \text{rfas_l} \& \sim \text{br_l} \& \sim \text{crtg_l} \& \sim \text{bg_l} \& \text{as_l} \& \sim \text{crtrq_l})$$

State Table

Bus Arbiter/Refresh Controller PAL
12 July 1983 Revision 2.0

SIGNAL VALUES											NOTES	
s t a t e	r f a e - i	r f a s - i	b r - i	c r t g - i	b g - i	a s - i	c r t r q - i	r e f c	r e f b	r e f a	n e x t	
a a a a	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	x x x x	x 0 0 0	1 0 x x	1 x 0 x	1 x x 0	b b b b	Wait in state "a" until refresh or the CRT controller requests the bus.
b b b b b	1 1 1 1 1	1 1 1 1 1	0 0 0 0 0	1 1 1 1 1	0 0 0 0 x	1 1 1 1 x	x 0 0 0 x	1 0 x x x	1 x 0 x x	1 x x 0 x	c f f f b	Arbitrate between refresh and the CRT controller requests. The CRT controller has highest priority. Wait in state "b" until the CPU grants the bus. Refresh grant CRT controller bus grant CRT controller bus grant CRT controller bus grant Wait until bus grant
c d	0 0	1 0	0 0	1 1	0 0	x x	x x	x x	x x	x x	d a	Refresh request service. First, assert refresh address enable. Second, assert refresh address enable and address strobe. Go back to state "a".
f f	1 1	1 1	0 0	0 0	0 0	1 1	0 1	x 1	x 1	x 1	f b	CRT controller request service. Assert CRT bus grant. Due to the length of a CRT controller bus grant, a refresh request will always be waiting when done with the CRT bus grant; thus, when done with the CRT bus grant, service the refresh request.

A

A36 PAL

RAM Decode PAL
PAL type 10L8
13 July 1983 Revision 2.0

Inputs

1	write _I	read = hi, write = lo
2	a19	address bit 19
3	a18	address bit 18
4	a0	address bit 0
5	as _I	address strobe, active lo
6	ds _I	data strobe, active lo
7	crtcse _I	crt controller select, active lo
9	a17	address bit 17
11	crtcbs _I	crt controller bus grant, active lo

Outputs

12	we1 _I	ram write enable bank 1, active lo
13	we0 _I	ram write enable bank 0, active lo
14	dramse _I	dram select, active lo
16	casenb _I	column address strobe enable, active hi
17	sramse _I	static ram select, active lo
18	rble _I	ram Bbffer low enable, active lo
19	rbhe _I	ram buffer hi enable, active lo

Equations

$$\text{dramse}_{I} = a19 \& \sim a18 \& \sim as_{I}$$

DRAM starts at address \$80000.
A write to \$A0000 will also write to \$80000.

$$\text{sramse}_{I} = a19 \& \sim a18 \& a17 \& \sim a0 \& \sim write_{I} \\ \& \sim ds_{I} \& \sim as_{I}$$

Static RAM starts at \$A0000.
A copy of data written to SRAM is simultaneously written to DRAM.

$$\text{casenb}_{I} = ds_{I} \& \text{crtcbs}_{I}$$

Allow CAS+ only if the CPU or the CRT controller accesses DRAM.

$$\text{we1}_{I} = a19 \& \sim a18 \& \sim as_{I} \& \sim write_{I} \& a0$$

Write to odd byte.

$$\text{we0}_{I} = a19 \& \sim a18 \& \sim as_{I} \& \sim write_{I} \& \sim a0$$

Write to even byte.

$$\text{rbhe}_{I} = a19 \& \sim a18 \& \sim as_{I} \& a0$$

Enable odd byte data buffer on access to DRAM.

$$\text{rble}_{I} = (a19 \& \sim a18 \& \sim as_{I} \& \sim a0) + (\sim \text{crtcse}_{I})$$

Enable even byte data buffer on access to DRAM.

A67 PAL

ROM Decode PAL
PAL type 10L8
19 October 1983 Revision 3.0

This PAL decodes six 16K × 8 ROMs. The first four are in stackable sockets. The total address range is 96K. This decode program is suitable for use on either *C or later revision ATL-008 logic boards.

Inputs	1	nc1	pulled up *
	2	nc2	pulled up *
	3	a11	address bit 11
	4	a13	address bit 13
	5	a14	address bit 14
	6	a17	address bit 17
	7	a15	address bit 15
	8	a16	address bit 16
	9	a19	address bit 19
	11	a18	address bit 18

Outputs	12	romen3_l	rom enable output, active lo
	13	nc13	not used
	14	romen2_l	rom enable output, active lo
	15	nc15	not used
	16	romen1_l	rom enable output, active lo
	17	romen1a_l	rom enable output, active lo
	18	romen0_l	rom enable output, active lo
	19	romen0a_l	rom enable output, active lo

Equations

$\text{romen0_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \sim\text{a16} \& \sim\text{a15} \& \sim\text{a14}$	Start Address \$00000 A98 (bottom ROM)
$\text{romen0a_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \sim\text{a16} \& \sim\text{a15} \& \text{a14}$	Start Address \$04000 A98 (top ROM)
$\text{romen1_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \sim\text{a16} \& \text{a15} \& \sim\text{a14}$	Start Address \$08000 A99 (bottom ROM)
$\text{romen1a_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \sim\text{a16} \& \text{a15} \& \text{a14}$	Start Address \$0C000 A99 (top ROM)
$\text{romen2_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \text{a16} \& \sim\text{a15} \& \sim\text{a14}$	Start Address \$10000 A100
$\text{romen3_l} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{a17} \& \text{a16} \& \sim\text{a15} \& \text{a14}$	Start Address \$14000 A101

A80 PAL

Communications PAL
PAL type 16L8
19 Sept 1983 Revision 2.0

This PAL is used to select the baud clock for the SCC and to select the interface for the main port (RS232, RS422, or Current Loop).

Inputs	1	write_l	read = hi, write = lo
	2	sccclk	3.7125 MHz clock
	3	rs422_l	select RS422 or current loop (hi = current loop, lo = RS422)
	4	rs232_l	select other or RS232 (hi = other, lo = RS232)
	5	reset_l	reset input, negative true
	6	ext_l	select internal or external clocks (hi = internal, lo = external)
	7	clk422	external RS422 baud clock



8	rx	external RS232 receive baud clock
9	ds_l	data strobe, negative true
11	txc	external RS232 transmit baud clock

Controls

12	enb12
13	enb13
14	enb14
15	enb15
16	enb16
17	enb17
18	enb18
19	enb19

Outputs

12	enbaux_l	enable aux port I/O, negative true
13	rdds_l	read data strobe, negative true
14	wrds_l	write data strobe, negative true
15	enb422	enable RS422 interface, positive true
16	rtxca	transmit clock to SCC
17	enb232_l	enable RS232 interface, negative true
18	enbcl	enable current loop I/F, positive true
19	trxca	receive clock to SCC

Equations

enb12 = 1

enb13 = 1

enb14 = 1

enb15 = 1

enb16 = 1

enb17 = 1

enb18 = 1

enb19 = 1

trxca = (~rx & ~ext_l & ~rs232_l) +
 (~clk422 & ~ext_l & rs232_l) +
 (~sccclk & ext_l)

Select clock source for SCC
 TRXCA clock input.

rtxca = (~txc & ~ext_l & ~rs232_l) +
 (~clk422 & ~ext_l & rs232_l) +
 (~sccclk & ext_l)

Select clock source for SCC
 RTXCA clock input.

wrds_l = (~ds_l & ~write_l) + (~reset_l)

Generate write data strobe for SCC and UPI.
 Reset to SCC by asserting both the read
 and the write data strobes.

rdds_l = (~ds_l & write_l) + (~reset_l)

Generate read data strobe for SCC and UPI.
 Reset to SCC by asserting both the read
 and the write data strobes.

MAIN AND AUXILIARY PORT SELECT TABLE

INPUTS		OUTPUTS				SELECTION
rs232_l	rs422_l	enb422	enb232_l	enbcl	enbaux_l	
0	0	0	1	0	1	loopback mode, no interfaces enabled
0	1	0	0	0	0	RS232 and aux port
1	0	1	1	0	0	RS422 and aux port
1	1	0	1	1	0	20 mA C.L. and aux port

In the above table, a 0 is less than or equal to 0.8 volts, while a 1 is greater than 2.4 volts.

$$\text{enb422} = \text{rs422_l} + \sim\text{rs232_l}$$

$$\text{enbcl} = \sim\text{rs422_l} + \sim\text{rs232_l}$$

$$\text{enb232_l} = \sim\text{rs232_l} \& \text{rs422_l}$$

$$\text{enbaux_l} = \text{rs232_l} + \text{rs422_l}$$

A82 SEEQ PAL

ROM Control PAL
PAL type 16L8
20 Oct 1983 Revision 1.0

This PAL is used to control the EEROM and ROM data buffer. The EEPROM write enable line is toggled by writing to EEPROM and subsequently writing to an address \$2000 less. Provision is made to be able to use Intel EEPROMS in the future if needed. *This PAL works only with SEEQ-type EEPROMS.*

Inputs

- | | | |
|----|---------|--|
| 1 | a19 | address bit 19 |
| 2 | reset_l | reset input to reset ee_wl to hi level |
| 3 | a18 | address bit 18 |
| 4 | a17 | address bit 17 |
| 5 | a14 | address bit 14 |
| 6 | a11 | address bit 11 |
| 7 | a13 | address bit 13 |
| 8 | wr_l | read = hi, write = lo |
| 9 | ds_l | data strobe, active lo |
| 11 | as_l | address strobe, active lo |

Controls

- | | |
|----|-------|
| 12 | enb12 |
| 13 | enb13 |
| 14 | enb14 |
| 15 | enb15 |
| 16 | enb16 |
| 17 | enb17 |
| 18 | enb18 |
| 19 | enb19 |



Outputs			
	12	vpa_l	valid peripheral address, active lo
	13	e2oe_l	eeeprom output enable, active lo
	14	dtack_l	data transfer acknowledge, active lo
	15	nc15	no connect
	16	e2we_l	eeeprom write enable, active lo (address bit 11 if using intel eeeproms)
	17	ieewe_l	intel write enable
	18	romoe_l	rom output enable, active lo
	19	nc19	address bit 11 or 12 (depending on pgm)

Equations

$$\text{enb12} = 1$$

$$\text{enb13} = 1$$

$$\text{enb14} = \sim\text{a19} \& \sim\text{a18} \& \sim\text{as}_l \quad \text{Assert DTACK* for ROM/EEPROM access.}$$

$$\text{enb15} = 1$$

$$\text{enb16} = 1$$

$$\text{enb17} = 1$$

$$\text{enb18} = 1$$

$$\text{enb19} = 1$$

$$\begin{aligned} \text{e2we}_l = & (\text{nc15} \& \text{a19} \& \text{reset}_l) + \\ & (\text{nc15} \& \text{a18} \& \text{reset}_l) + \\ & (\text{nc15} \& \sim\text{a17} \& \text{reset}_l) + \\ & (\text{nc15} \& \text{a13} \& \text{reset}_l) + \\ & (\text{nc15} \& \text{wr}_l \& \text{reset}_l) + \\ & (\text{nc15} \& \text{ds}_l \& \text{reset}_l) \end{aligned}$$

e2we_l and nc15 are cross coupled to form a flip-flop. The flop is used to turn on e2we_l when a write to EEROM (starting at \$3E000) is performed. The write pulse is turned off by a dummy write to an address \$2000 less.

$$\begin{aligned} \text{nc15} = & (\text{e2we}_l \& \text{a19}) + \\ & (\text{e2we}_l \& \text{a18}) + \\ & (\text{e2we}_l \& \sim\text{a17}) + \\ & (\text{e2we}_l \& \sim\text{a13}) + \\ & (\text{e2we}_l \& \text{wr}_l) + \\ & (\text{e2we}_l \& \text{ds}_l) \end{aligned}$$

Enable the EEROM output when reading data from it. Due to a previous decode method (using a strapped 74LS138), the EEROM address was chosen to be \$3E000 because this address was common to all strapable options. Address \$3E000 works here, too, but note that not all the address bits are decoded. This results in several copies of EEROM in memory space, but it provides a good copy at address \$3E000.

$$\text{e2oe}_l = \sim\text{a19} \& \sim\text{a18} \& \text{a17} \& \text{a14} \& \text{a13} \& \text{wr}_l \& \sim\text{ds}_l \& \sim\text{as}_l$$

$$\text{romoe}_l = \sim\text{a19} \& \sim\text{a18} \& \sim\text{as}_l$$

$$\text{dtack}_l = 1$$

$$\text{vpa}_l = \sim\text{a19} \& \text{a18} \& \sim\text{as}_l \quad \text{Assert VPA* for peripheral accesses.}$$

$$\text{ieewe}_l = 1 \quad \text{Reserved for future use with Intel EEPROMs.}$$

A82 XICOR PAL

ROM Control PAL
PAL type 16L8
20 Oct 1983 Revision 1.0

This PAL is used to control the EEROM and ROM data buffer. Provision is made to be able to use Intel EEPROMS. *This only works with Xicor-type EEPROMS.*

Inputs	1	a19	address bit 19
	2	reset_	reset input to reset eeve_ to hi level
	3	a18	address bit 18
	4	a17	address bit 17
	5	a14	address bit 14
	6	a11	address bit 11
	7	a13	address bit 13
	8	wr_	read = hi, write = lo
	9	ds_	data strobe, active lo
	11	as_	address strobe, active lo
	Controls	12	enb12
13		enb13	
14		enb14	
15		enb15	
16		enb16	
17		enb17	
18		enb18	
19		enb19	
Outputs		12	vpa_
	13	e2oe_	eprom output enable, active lo
	14	dtack_	data transfer acknowledge, active lo
	15	nc15	no connect
	16	e2we_	eprom write enable (xicor and seeq), active lo (address bit 11 if using intel eeproms)
	17	ieewe_	intel write enable
	18	romoe_	rom output enable, active lo
	19	nc19	address bit 11 or 12 (depending on pgm)

Equations

$$\text{enb12} = 1$$

$$\text{enb13} = 1$$

$$\text{enb14} = \sim a19 \ \& \ \sim a18 \ \& \ \sim as_ \quad \text{Assert DTACK* for ROM/EEPROM access.}$$

$$\text{enb15} = 1$$

$$\text{enb16} = 1$$

$$\text{enb17} = 1$$

$$\text{enb18} = 1$$

$$\text{enb19} = 1$$

e2we_l = $\bar{a}19 \& \bar{a}18 \& a17 \&$
 $a14 \& a13 \& \bar{a}11 \&$
 $\bar{a}s_l \& \bar{d}s_l \& \bar{w}r_l$

Xicor write enable is a pulse the same width as the data strobe pulse width. This is different from the Seeq parts where the write pulse is held lo for 10 milliseconds. The EEPROM starts at address \$3E000.

e2oe_l = $\bar{a}19 \& \bar{a}18 \& a17 \&$
 $a14 \& a13 \& w_r_l \&$
 $\bar{d}s_l \& \bar{a}s_l$

Enable the EEROM output when reading data from it. Due to a previous decode method (using a strapped 74LS138), the EEROM address was chosen to be \$3E000 because this address was common to all strapable options. Address \$3E000 works here, too, but note that not all the address bits are decoded. This results in several copies of EEROM in memory space, but it provides a good copy at address \$3E000.

romoe_l = $\bar{a}19 \& \bar{a}18 \& \bar{a}s_l$

dtack_l = 1

vpa_l = $\bar{a}19 \& a18 \& \bar{a}s_l$

Assert VPA* for peripheral accesses.

ieewe_l = 1

Reserved for future use.

nc15 = 1

This output is reserved for use in the cross flip-flop used in the SEEQ version PAL.

A86 PROM

The following is the data pattern for the Revision PROM at location A86 of a *B assembly of the 112-2831 ATL-008 logic board.

NOTE

The pattern here is positive true data. A 1 is represented by a voltage output of ± 2.4 volts; a 0 is an output voltage of ± 0.8 volts. For PROMs programmed with inverted data, it will be necessary to invert the data. (For example, Monolithic Memories' 6331 has inverted data BI #604-B00S-8578.)

HEX ADDRESS	HEX DATA	INVERTED HEX DATA
00	00	FF
01	02	FD
02	02	FD
03	02	FD
04	02	FD
05	02	FD
06	03	FC
07	02	FD
08	04	FB
09	02	FD
0A	05	FA
0B	02	FD
0C	06	F9
0D	02	FD
0E	07	F8
0F	02	FD
10	08	F7
11	02	FD
12	09	F6
13	02	FD
14	0A	F5
15	02	FD
16	0B	F4
17	02	FD
18	0C	F3
19	02	FD
1A	0D	F2
1B	02	FD
1C	0E	F1
1D	02	FD
1E	0F	F0
1F	02	FD

ABB PAL**Interrupt Controller PAL**

PAL type 16R6

13 July 1983 Revision 2.0

Inputs	2	iack	interrupt acknowledge from 68008, pos. true
	3	a3	address bit 3 from 68008
	4	srql	SCC interrupt request, active lo
	5	ds_l	data strobe from 68008, active lo
	6	urql	upi interrupt request, active lo
	7	trql	timer interrupt request, active lo
	8	a2	address bit 2 from 68008
	9	crql	crt controller interrupt request, active lo
	Controls	12	enb12
19		enb19	
Outputs	12	ipl1	interrupt priority level 1, active lo
	13	dtackl	data transfer acknowledge, active lo
	14	sccackl	SCC interrupt acknowledge, active lo
	15	cackl	crt controller interrupt acknowledge, active lo
	16	tackl	timer interrupt acknowledge, active lo
	17	vpal	valid peripheral address, active lo
	18	uackl	upi interrupt acknowledge, active lo
19	ipl2	interrupt priority level 2, active lo	

Equations

$$\text{enb12} = 1$$

$$\text{enb19} = 1$$

$$\text{ipl1} = (\sim\text{crql}) + (\sim\text{trql} \& \text{srql} \& \text{urql} \& \text{crql})$$

$$\text{ipl2} = \sim\text{crql} + \sim\text{srql} + \sim\text{urql}$$

$$\text{tackl} = (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \sim\text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack}) + (\sim\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \sim\text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack})$$

$$\text{sccackl} = (\text{tackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \sim\text{srql} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack}) + (\text{tackl} \& \sim\text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack})$$

$$\text{uackl} = (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \text{srql} \& \sim\text{urql} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack}) + (\text{tackl} \& \text{sccackl} \& \sim\text{uackl} \& \text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack})$$

$$\text{cackl} = (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack}) + (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \sim\text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack})$$

$$\begin{aligned} \text{vpal} = & (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \text{a2} \& \sim\text{ds_l} \& \text{iack}) + \\ & (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{dtackl} \& \text{srql} \& \sim\text{urql} \& \text{a3} \& \sim\text{ds_l} \& \text{iack}) + \\ & (\text{tackl} \& \text{sccackl} \& \text{uackl} \& \sim\text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack}) + \\ & (\text{tackl} \& \text{sccackl} \& \sim\text{uackl} \& \text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack}) + \\ & (\sim\text{tackl} \& \text{sccackl} \& \text{uackl} \& \text{cackl} \& \sim\text{vpal} \& \text{dtackl} \& \sim\text{a3} \& \text{a2} \& \sim\text{ds_l} \& \text{iack}) \end{aligned}$$

$$\text{dtackl} = \text{tackl} \& \sim\text{sccackl} \& \text{uackl} \& \text{cackl} \& \text{vpal} \& \text{a3} \& \sim\text{a2} \& \sim\text{ds_l} \& \text{iack}$$

State Table

Interrupt Controller PAL
4 Oct 1983 Revision 2.1

This PAL arbitrates between interrupt requests. The timer, UPI and CRT controller are 6800-type peripherals and generate VPA(n) responses, causing the CPU to perform an autovector interrupt acknowledge. The SCC responds with a DTACK(n) to operate as a vectored interrupt. This controller controls the timing to the SCC interrupt acknowledge and the DTACK(n) to the CPU. After the state machine gets into one of the acknowledge states, it remains there until the condition which kept it there ceases to exist. It then returns to state "a".

Revision 2.1 incorporates making only one output line transition to if an asynchronous input is used to cause the transition. This eliminates the possibility that one output will "see" the signal change and the other will not.

SIGNAL NAMES														NOTES	
s t a t e	t a c k i	s c c a c k i	u a c k i	c a c k i	v p a i	d t a c k i	r t q i	r s q i	r u q i	r c q i	g a	u a	d i s c k	n e x t	
a	1	1	1	1	1	1	x	x	x	x	1	1	0	1	g
a	1	1	1	1	1	1	x	0	x	x	1	0	0	1	c
a	1	1	1	1	1	1	x	1	0	x	1	0	0	1	h
a	1	1	1	1	1	1	x	x	x	x	0	1	0	1	i
g	1	1	1	1	0	1	x	x	x	x	1	1	0	1	b
b	1	1	1	0	0	1	x	x	x	x	1	1	0	1	b
c	1	0	1	1	1	1	x	x	x	x	1	0	0	1	d
d	1	0	1	0	1	1	x	x	x	x	1	0	0	1	j
j	1	0	1	0	1	0	x	x	x	x	1	0	0	1	j
h	1	1	1	1	0	1	x	x	x	x	1	0	0	1	e
e	1	1	0	1	0	1	x	x	x	x	1	0	0	1	e
i	1	1	1	1	0	1	x	x	x	x	0	1	0	1	f
f	0	1	1	1	0	1	x	x	x	x	0	1	0	1	f

Interrupt level 7 (Video)

Interrupt level 5a (SCC). First, the SCC is sent an acknowledge. Then, after waiting for the SCC to put its vector on the data bus, VPA* is asserted.

The assertion of cakl is for "place keeping" only, to differentiate state "c" from state "d".

Interrupt level 5b (UPI). If the SCC does not have its request asserted, then the UPI will get the interrupt acknowledge.

Interrupt level 2 (Timer)



ASO PAL

Video Clock/Address Strobe Generator PAL

PAL type 16R6

19 Sept 1983 Revision 2.0

Inputs			
	2	crtcbg_l	crt controller bus grant, active lo
	3	nc3	pulled down
	4	nc4	pulled down
	5	clk132	25.9878 MHz dot clock for 132 col. mode
	6	sel80	80 or 132 column select (hi = 80 column)
	7	clk80	20.25 MHz dot clock for 80 col. mode (hi = 80 col. mode, lo = 132 col. mode)
	8	3stcntrl	this input is not used
	9	vlt	visual line time, hi when the 9007 is painting the CRT screen
Control	19	enb19	
Outputs	19	dotclk	dot clock selected from clk132 or clk80
	18	s1	state counter bit 1
	17	cclk_l	character clock, active lo
	16	s0	state counter bit 0
	15	load_l	character load pulse, active lo
	14	lvlt	latched vlt, latched on lo-hi edge of cclk_l
	13	crtcas_l	crt controller address strobe, active lo
	12	nc12	not used

Equations

$$\text{enb19} = 1$$

$$\text{dotclk} = (\text{sel80} \& \sim\text{clk80}) + (\sim\text{sel80} \& \sim\text{clk132})$$

$$\begin{aligned} \text{crtcas}_l = & (\sim\text{sel80} \& \text{lvlt} \& \sim\text{crtcbg}_l \& \text{crtcas}_l \& \text{cclk}_l \& \text{s1} \& \text{s0}) + \\ & (\sim\text{sel80} \& \text{lvlt} \& \sim\text{crtcbg}_l \& \sim\text{crtcas}_l \& \text{cclk}_l) + \\ & (\text{sel80} \& \text{lvlt} \& \sim\text{crtcbg}_l \& \text{crtcas}_l \& \text{cclk}_l \& \text{s1} \& \sim\text{s0}) + \\ & (\text{sel80} \& \text{lvlt} \& \sim\text{crtcbg}_l \& \sim\text{crtcas}_l \& \text{load}_l) \end{aligned}$$

$$\text{lvlt} = (\sim\text{load}_l \& \sim\text{vlt}) + (\sim\text{lvlt} \& \text{load}_l)$$

$$\text{load}_l = (\text{s1} \& \sim\text{s0} \& \sim\text{cclk}_l \& \text{load}_l \& \sim\text{sel80}) + (\sim\text{s1} \& \sim\text{s0} \& \sim\text{cclk}_l \& \text{load}_l \& \text{sel80})$$

$$\begin{aligned} \text{cclk}_l = & (\sim\text{s1} \& \sim\text{s0} \& \text{cclk}_l \& \text{load}_l) + \\ & (\text{s1} \& \sim\text{cclk}_l \& \text{load}_l) + \\ & (\sim\text{cclk}_l \& \text{load}_l \& \text{sel80}) \end{aligned}$$

$$\begin{aligned} \text{s0} = & (\text{s0} \& \text{cclk}_l \& \text{load}_l) + \\ & (\text{s1} \& \text{s0} \& \text{load}_l) + \\ & (\text{s0} \& \text{load}_l \& \text{sel80}) \end{aligned}$$

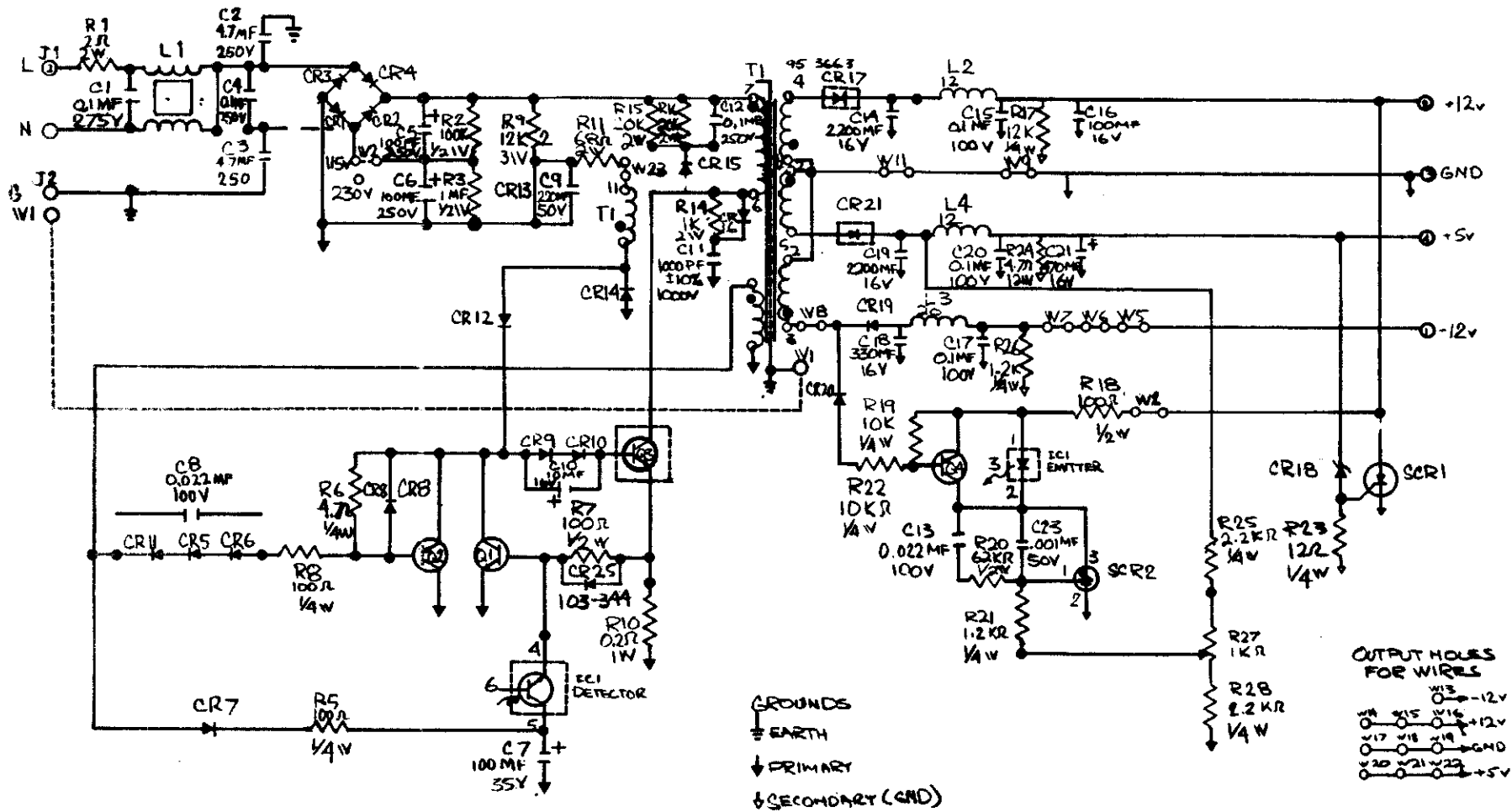
$$\begin{aligned} \text{s1} = & (\text{s1} \& \sim\text{s0} \& \text{load}_l) + \\ & (\sim\text{s1} \& \text{s0} \& \text{cclk}_l \& \text{load}_l) + \\ & (\sim\text{s1} \& \text{s0} \& \text{load}_l \& \text{sel80}) \end{aligned}$$

SCHEMATIC DRAWINGS

INDEX

This section contains assembly and schematic drawings for the keyboard, monitor board, and logic board. The drawings are in the order given below. The page numbers in the list refer to the sheet numbers printed in the lower right corner of each page.

DRAWING NAME	DRAWING NUMBER
Zenith Power Supply Schematic	123-5661-02
ATL-008 Schematic	EL1015-*
Keyboard Assembly	607-MF-****
Keyboard Schematic	607-MF-****
Monitor Board Assembly	112-2919
Monitor Board Schematic	EL112-2919
Logic Board Assembly	112-2831-000*
Logic Board Schematic	EL112-2831-*



ZENITH POWER SUPPLY SCHEMATIC

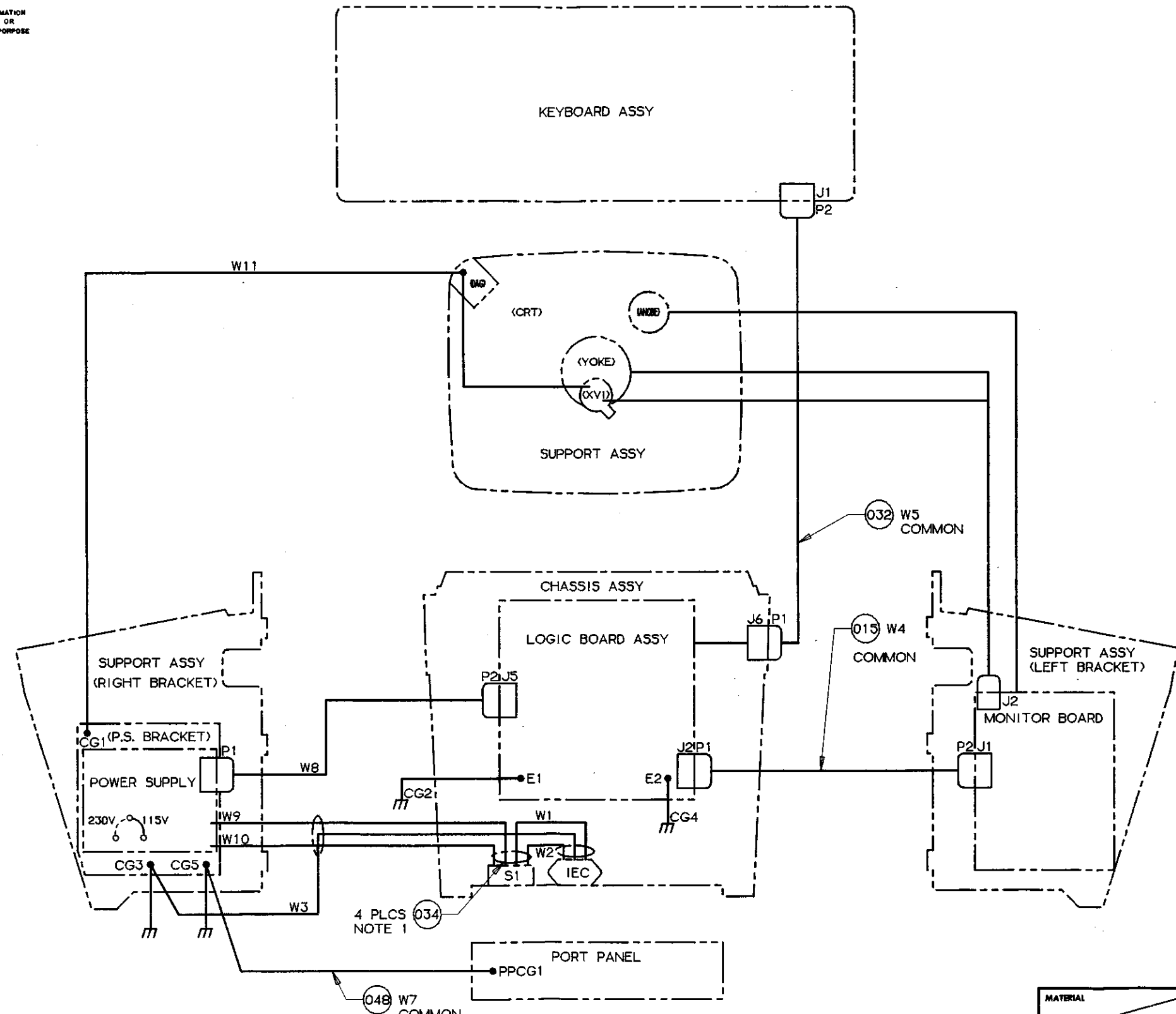
123-5661-02

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

THIS DOCUMENT, SUBMITTED IN CONFIDENCE, CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF BEEHIVE INTERNATIONAL.

DO NOT SCALE

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE
AA	RELEASED PER ECD 17240 TAPE 0903-01	RP	RP		2-16-81



NOTES:
1. SECURE WIRES WITH ITEM (034) (TIEWRAP) 1.5" ± .5" FROM COMPONENT OR TERMINATION.

STANDARD HOLE TOLERANCES UNLESS NOTED	
HOLE SIZE	TOLERANCE
.000-.250	+ .003 - .002
.250-.500	+ .005 - .003
OVER .500	+ .010 - .005

MATERIAL	FINISH	DRAWN R. HILL	DATE 1-31-81	APPROVED L.O. TN	DATE 2-16-81
		CHECKED R. Parr	DATE 3/16/81	APPROVED PM	DATE 2-16-81
		APPROVED SAH	DATE 2-16-81	APPROVED RGP	DATE 2-16-81
TITLE		TOP ASSEMBLY			
		(WIRING DIAGRAM)			
DWG. SIZE	CODE IDENT. NO.	NUMBER	REV		
D	52541	WD1015-*	AA		
SCALE	N/A		SHEET 1 OF 1		

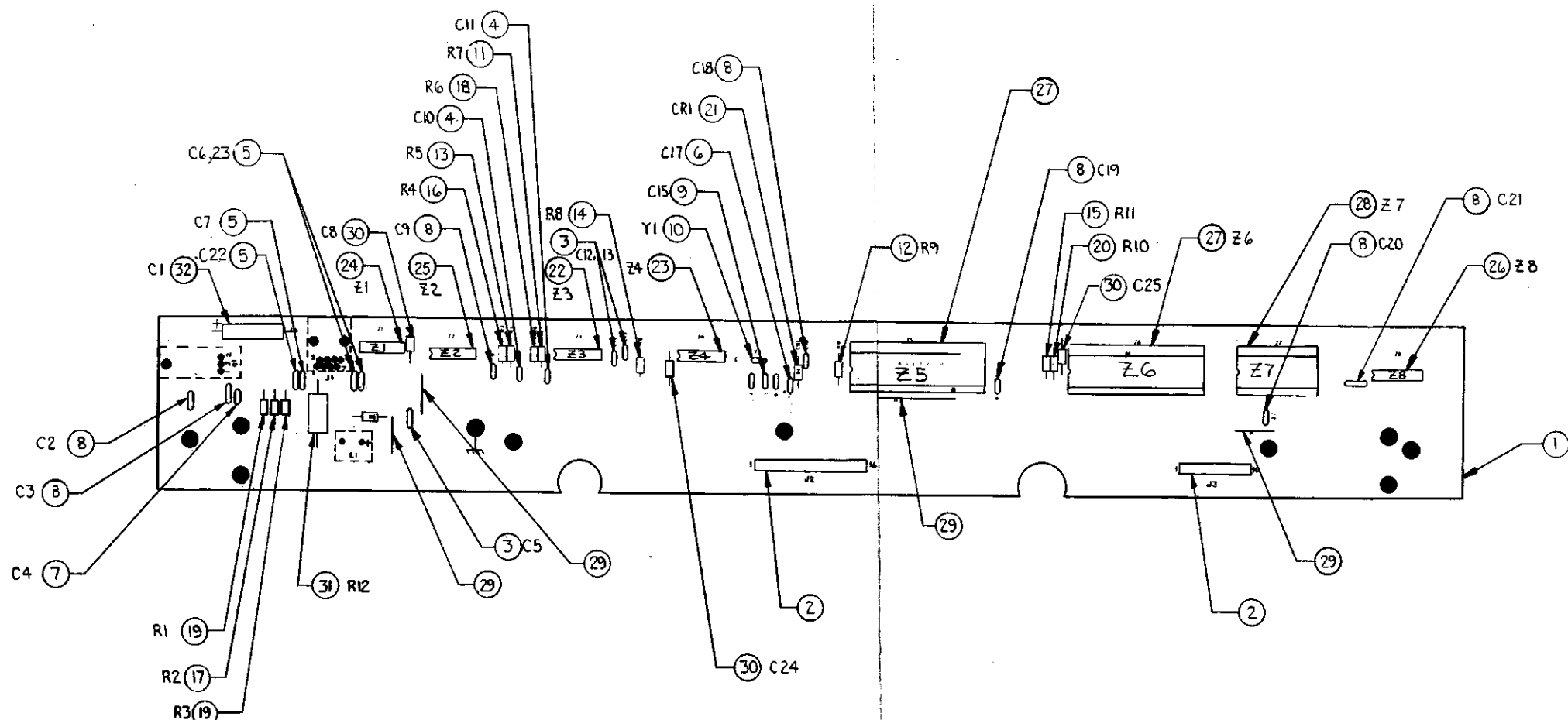
BEEHIVE INTERNATIONAL
4910 AMELIA EARHART DR.
SALT LAKE CITY, UTAH

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

DWG. NO. WD1015-*

DO NOT SCALE

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE
-----	-----------------------	--------	------	------	------



BILL OF MATERIAL

ITEM NO.	QTY	ITEM DESCRIPTION	G.I. PART NUMBER
1	1	PWB	900207-401
2	2	CONNECTION, HEADER (J2, J3)	321350
3	3	CAPACITOR, .1UF (C6, 12, 13)	321215U1042J
4	2	CAPACITOR, .1UF, PLUS/MINUS 10% (C10, 11)	321215M104KJ
5	4	CAPACITOR, .001UF (C6, 7, 22, 23)	321320U102ZJ
6	1	CAPACITOR, .1UF (C17)	3212161010ME
7	1	CAPACITOR, 10UF (C4)	321216T100ME
8	7	CAPACITOR, .01UF (C2, 3, 9, 10-21)	321320U103ZJ
9	1	CAPACITOR, SIP, 30PF X 2 (C15)	321242-001
10	1	RESONATOR, CERAMIC, 5.76MHZ (Y1)	321201-007
11	1	RESISTOR, 12K (R7)	321213M123JB
12	1	RESISTOR, 10K (R9)	321213M103JB
13	1	RESISTOR, 6.2K (R5)	321213M622JB
14	1	RESISTOR, 4.7K (R8)	321213M472JB
15	1	RESISTOR, 2K, RV (R11)	321213R202JB
16	1	RESISTOR, 430 OHM (R4)	321213M431JB
17	1	RESISTOR, 110 OHM (R2)	321213M111JB
18	1	RESISTOR, 620 OHM (R6)	321213M621JB
19	2	RESISTOR, 56 OHM (R1 & 3)	321213M560JB
20	1	RESISTOR, 10K (R10)	321213R 10
21	1	DIODE, 1N4148 (CR1)	321058-002
22	1	I.C., NE566 (Z5)	321219-015
23	1	I.C., 74LS14 (Z4)	32121807414002
24	1	I.C., 7406 (Z1)	32121807406A02
25	1	I.C., 74LS02 (Z2)	32121807402D02
26	1	I.C., 74LS373 (Z8)	321218074373D04
27	2	SOCKET, DIP, 40 PIN	321204-001
28	1	SOCKET, DIP, 28 PIN	321204-003
29	4	JUMPER	324018
30	3	CAPACITOR, .01UF (C8, 24, 25)	321335U103ZJ
31	1	RESISTOR, 10 OHM, 2W (R12)	321213R100JE
32	1	CAPACITOR, 470UF (C1)	321051-E471GG

DWG. NO. 607-MFOO-XXXX

DWG. SIZE	CODE IDENT. NO.	NUMBER	REV
D	52541	607-MFOO-XXXX	AA
SCALE	N/A	SHEET	80 OF 91

REV	DESCRIPTION OF CHANGE	DRN. BY	CHKD.	APPR.	DATE
-----	-----------------------	---------	-------	-------	------

DO NOT SCALE

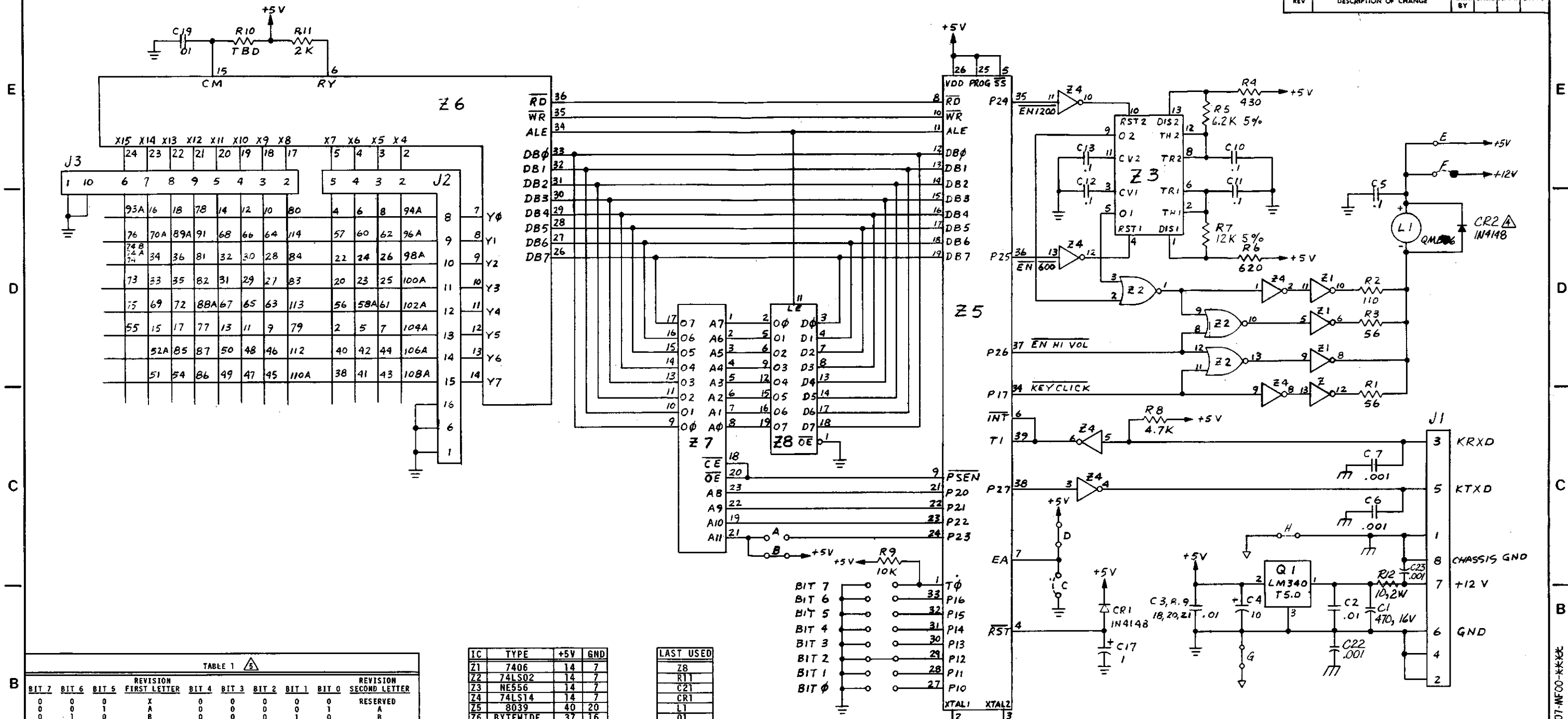


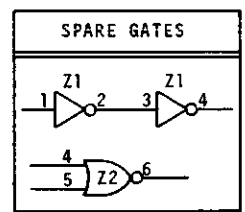
TABLE 1

BIT 7	BIT 6	BIT 5	REVISION FIRST LETTER	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REVISION SECOND LETTER
0	0	0	A	0	0	0	0	0	RESERVED
0	0	1	B	0	0	0	0	0	A
0	0	1	C	0	0	0	0	1	B
0	1	0	D	0	0	0	0	0	C
0	1	0	E	0	0	0	0	1	D
0	1	1	F	0	0	0	0	0	E
1	0	0	G	0	0	0	0	0	F
1	0	0	H	0	0	0	0	1	G
1	0	0	I	0	0	0	0	1	H
1	0	0	J	0	0	0	0	1	I
1	0	0	K	0	0	0	0	1	J
1	0	0	L	0	0	0	0	1	K
1	0	0	M	0	0	0	0	1	L
1	0	0	N	0	0	0	0	1	M
1	0	0	O	0	0	0	0	1	N
1	0	0	P	0	0	0	0	1	O
1	0	0	Q	0	0	0	0	1	P
1	0	0	R	0	0	0	0	1	Q
1	0	0	S	0	0	0	0	1	R
1	0	0	T	0	0	0	0	1	S
1	0	0	U	0	0	0	0	1	T
1	0	0	V	0	0	0	0	1	U
1	0	0	W	0	0	0	0	1	V
1	0	0	X	0	0	0	0	1	W
1	0	0	Y	0	0	0	0	1	X
1	0	0	Z	0	0	0	0	1	Y
1	0	0	RESERVED	0	0	0	0	1	Z
1	0	0	RESERVED	0	0	0	0	1	RESERVED
1	0	0	RESERVED	0	0	0	0	1	RESERVED
1	0	0	RESERVED	0	0	0	0	1	RESERVED
1	0	0	RESERVED	0	0	0	0	1	RESERVED
1	0	0	RESERVED	0	0	0	0	1	RESERVED

IC	TYPE	+5V	GND
Z1	7406	14	7
Z2	74LS02	14	7
Z3	NE556	14	7
Z4	74LS14	14	7
Z5	8039	40	20
Z6	BYTEWIDE	37	16
Z7	2716/2732	24	12
Z8	74LS373	20	10

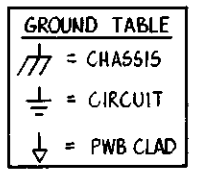
LAST USED

Z8
R11
C21
CR1
L1
Q1
J3



JUMPER

	A	B	C	D
EXT PROG MEMORY				X
INT PROG MEMORY			X	
2716		X		
2732	X			

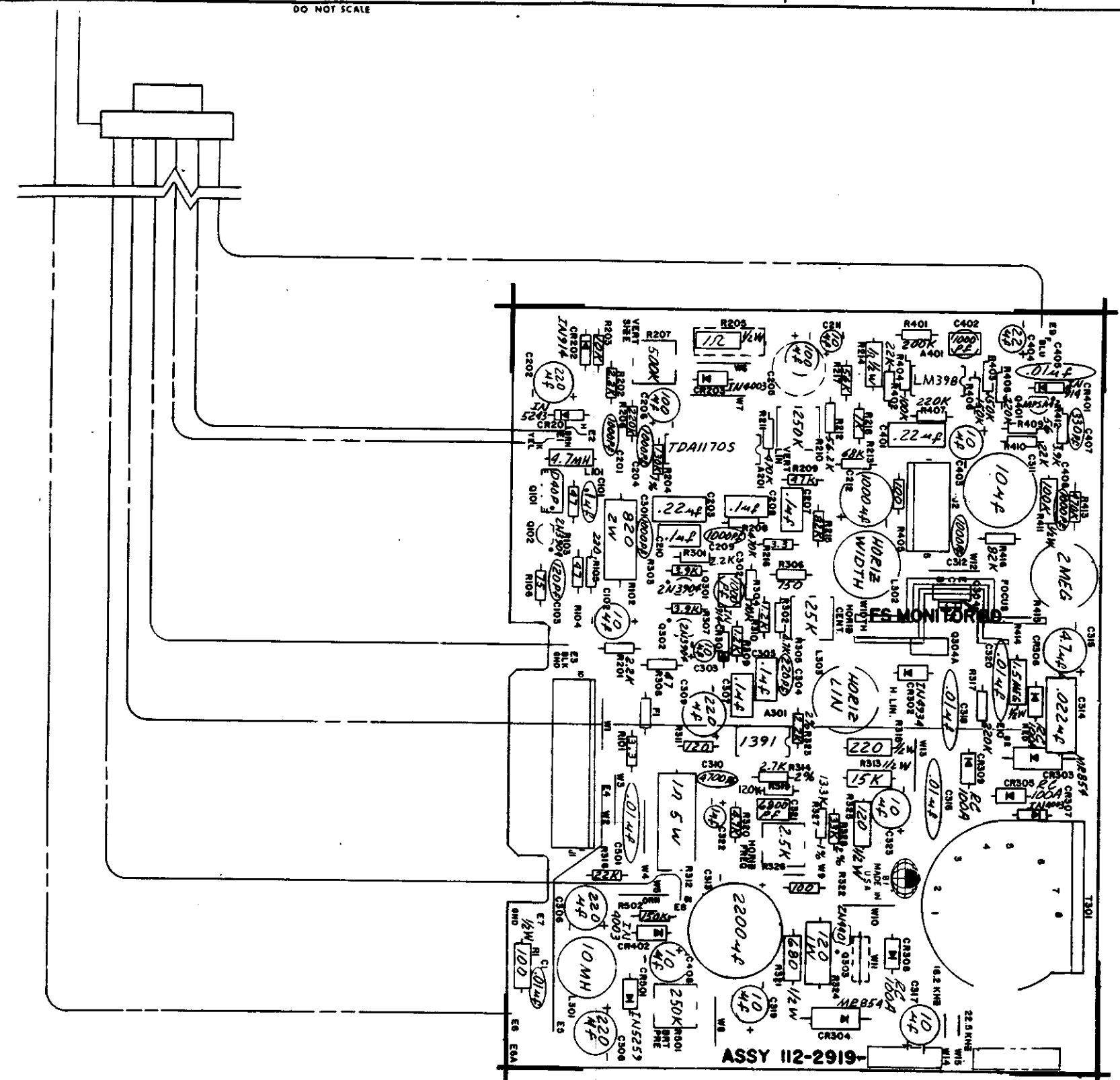


- NOTES: (UNLESS OTHERWISE SPECIFIED)
- ALL CAPACITOR VALUES ARE IN MICROFARADS (μf).
 - ALL RESISTOR VALUES ARE IN OHMS (Ω), 1/4 WATT, ±5%.
 - C16 IS SUBSTITUTED FOR C15 WHEN CRYSTAL IS USED IN PLACE OF RESONATOR (Y1).
 - NOT INSTALLED.
 - SEE TABLE 1 FOR FUTURE CONNECTIONS FOR JUMPERS 0 THRU 7. THESE JUMPERS INDICATE THE REV LEVEL OF THE CIRCUIT BOARD AND MUST BE UPDATED ALONG WITH THE PWB REV LEVEL. A 1 MEANS THE JUMPER IS PRINTED.

EXAMPLE BOARD REVISION
 XA = 00000001
 AA = 00100001

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE
RA	RELEASED PER ECO 17137	LB	RP	RP	11/11/83
RB	REVISED PER ECO 17216	LB	RP	RP	11/11/83
RC	REVISED PER ECO 17252	LB	RP	RP	11/11/83
RD	REVISED PER ECO 17275	LB	RP	RP	11/11/83

THIS DOCUMENT, SUBMITTED IN CONFIDENCE, CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSMITTED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF BEEHIVE INTERNATIONAL.



STANDARD HOLE TOLERANCES UNLESS NOTED	
HOLE SIZE	TOLERANCE
.000-.250	+.003 -.002
.250-.500	+.005 -.003
OVER .500	+.010 -.005

UNIT OR MODEL	NEXT ASSEMBLY
ATL-008	

BREAK ALL SHARP EDGES AND CORNERS UNLESS OTHERWISE SPECIFIED
Tolerance unless otherwise specified
2 PLACE DECIMAL ±
3 PLACE DECIMAL ±
ANGULAR ± 0° 30'

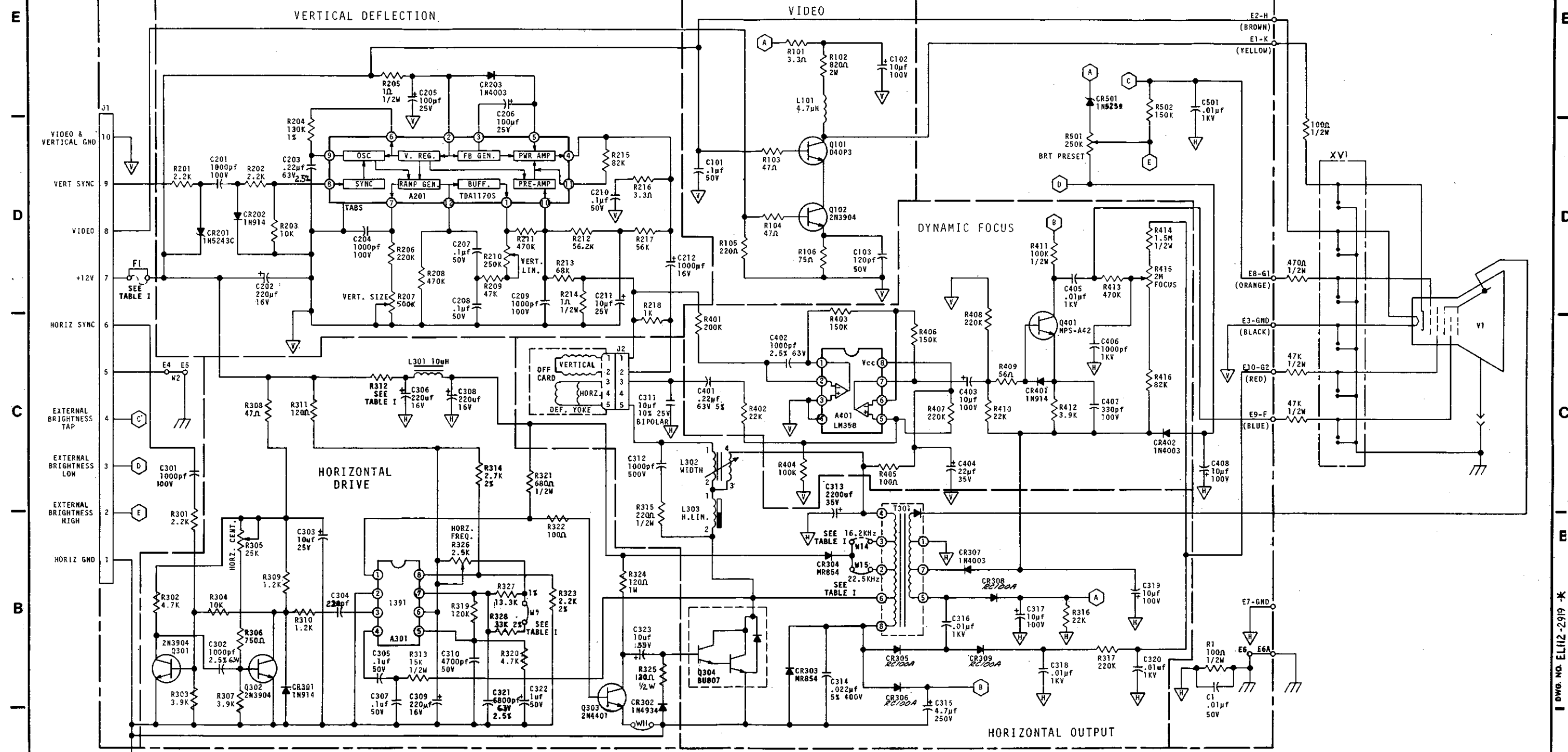


DRAWN	R Hill	DATE	7 Jul 83	APPROVED	[Signature]	DATE	11/11/83
CHECKED	[Signature]	DATE	12/27/83	APPROVED	[Signature]	DATE	11/11/83
APPROVED	[Signature]	DATE	11/11/83	APPROVED	[Signature]	DATE	11/11/83
TITLE BOARD, MONITOR							
DWG SIZE	CODE IDENT. NO.	NUMBER	REV				
D	52541	112-2919-*	RD				
SCALE	NONE	SHEET 1 OF 1					

DWG. NO. ELI12-2919-*

THIS DOCUMENT, SUBMITTED IN CONFIDENCE, CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF BEEHIVE INTERNATIONAL.

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE
AA	RELEASED PER ECO 17137	L.B.	W.P.	W.P.	10-12-83
AB	REVISED PER ECO 17216	L.B.	W.P.	W.P.	10-12-83
AC	REVISED PER ECO 17252	L.B.	W.P.	W.P.	10-12-83
AD	REVISED PER ECO 17275	L.B.	W.P.	W.P.	10-12-83



NOTES:
1. GROUND SYSTEMS ∇ AND ∇ ARE TIED TOGETHER ON THE P.C. BOARD AT A SINGULAR POINT.

TABLE I

DASH NO.	F1	R312	W9	W14	W15	W11
0000	WIRE JUMPER	10 5W	WIRE JUMPER	---	WIRE JUMPER	WIRE JUMPER
0001	WIRE JUMPER	10 5W	---	WIRE JUMPER	---	WIRE JUMPER
0002	3A	125V	WIRE JUMPER	---	WIRE JUMPER	---

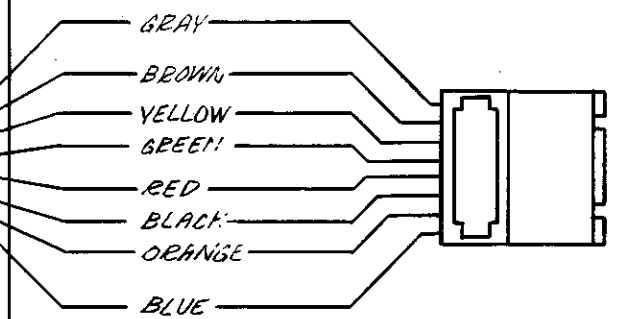
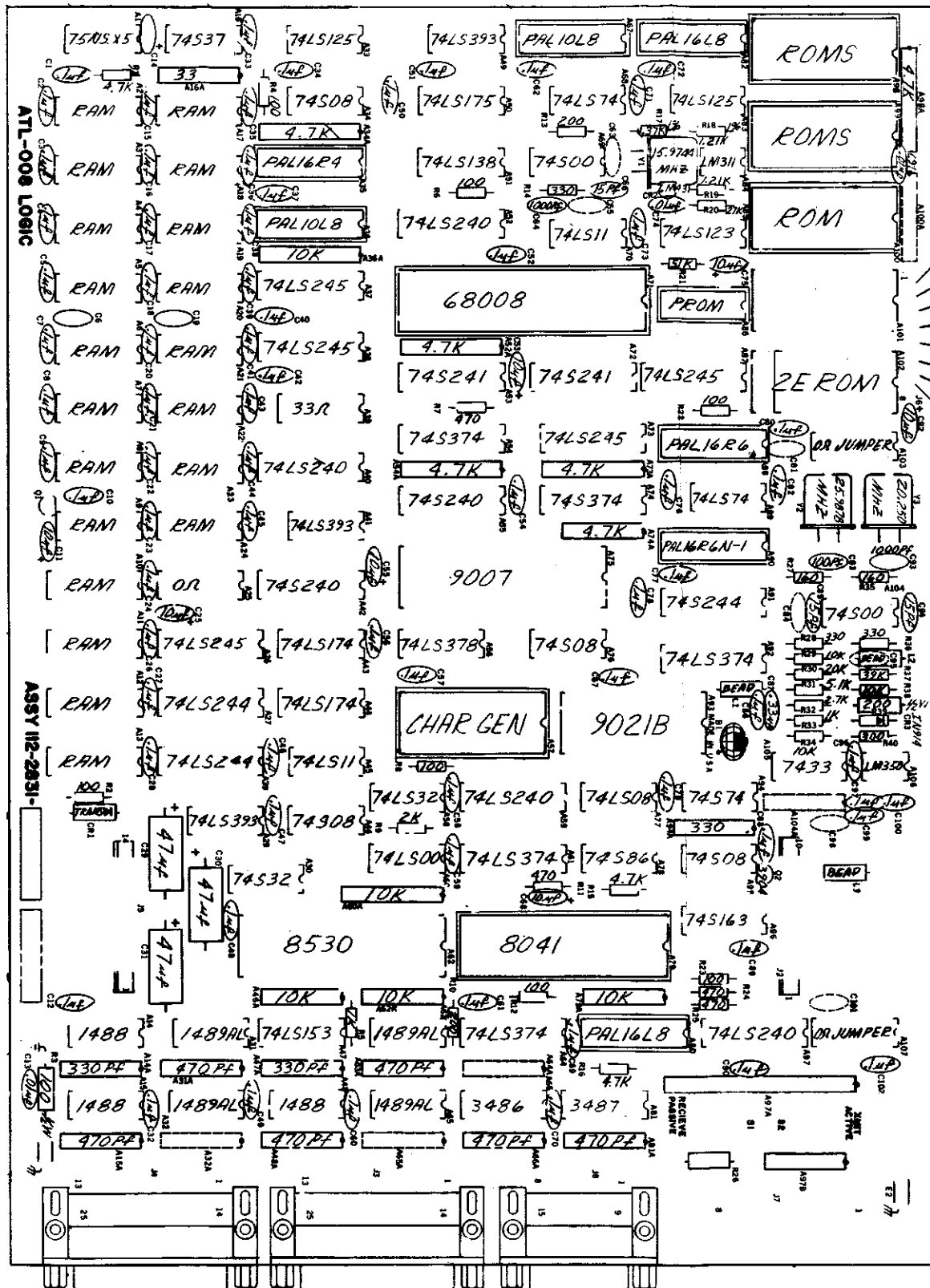
STANDARD HOLE TOLERANCES UNLESS NOTED		UNIT OR MODEL	
HOLE SIZE	TOLERANCE	UNIT OR MODEL	NEXT ASSEMBLY
.000-.250	+.003 -.002	BEEHIVE INTERNATIONAL	
.250-.500	+.005 -.003	4910 AMELIA EARHART DR. SALT LAKE CITY, UTAH	
OVER .500	+.010 -.005	BEEHIVE INTERNATIONAL	

MATERIAL	DATE	APPROVED	DATE
FINISH	7 Jun 83	W.P.	10-12-83
DRAWN		APPROVED	
CHECKED		APPROVED	
APPROVED		APPROVED	
TITLE			
BOARD, MONITOR W/FAILSAFE CIRCUIT (SCHEMATIC)			
DWG. SIZE	CODE IDENT. NO.	NUMBER	REV
D	52541	ELL12-2919-*	AD
SCALE	NONE	SHEET	1 OF 1

DO NOT SCALE

THIS DOCUMENT, SUBMITTED IN CONFIDENCE, CONTAINS PROPRIETARY INFORMATION WHICH SHALL NOT BE REPRODUCED OR TRANSFERRED TO OTHER DOCUMENTS OR DISCLOSED TO OTHERS OR USED FOR MANUFACTURING OR ANY OTHER PURPOSE WITHOUT PRIOR WRITTEN PERMISSION OF BEEHIVE INTERNATIONAL.

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE
RA	RELEASED PER ECO 17240	LB	RP	[Signature]	11 MAR 84
RB	REVISED PER ECO 17270	LB	RP	[Signature]	11 MAR 84
RC	REVISED PER ECO 17281	LB	RP	[Signature]	11 MAR 84
RD	REVISED PER ECO 17301	LB	RP	[Signature]	11 APR 84
RE	REVISED PER ECO 17282	LB	RP	[Signature]	20 JUN 84
RF	REVISED PER ECO 17339	LB	RP	[Signature]	3 JUL 84



E
D
C
B
A

E
D
C
B
A

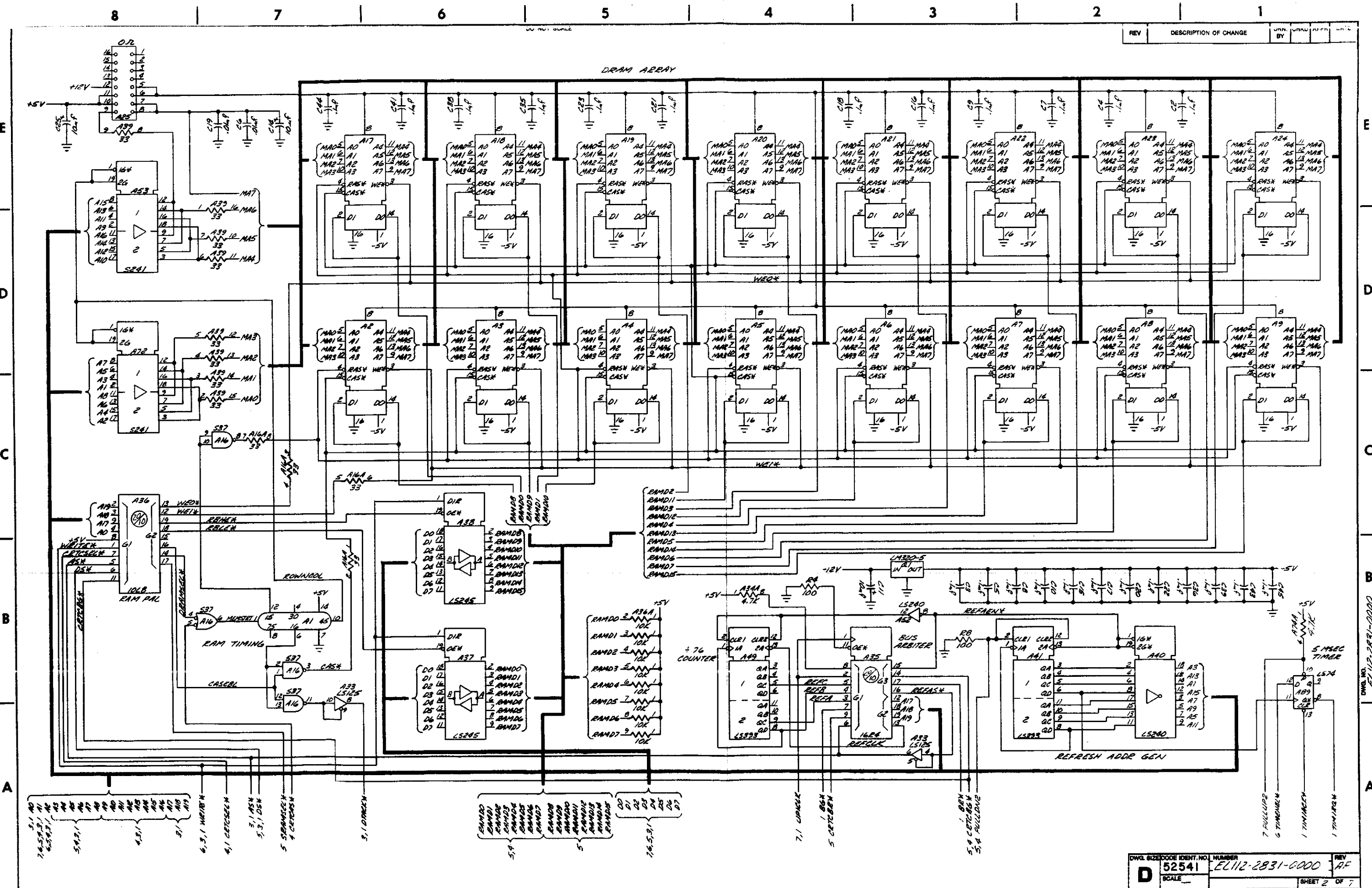
STANDARD HOLE TOLERANCES UNLESS NOTED	
HOLE SIZE	TOLERANCE
.000-.250	+ .003 - .002
.250-.500	+ .005 - .003
OVER .500	+ .010 - .005

UNIT OR MODEL: ATL 008
NEXT ASSEMBLY: [Blank]
BREAK ALL SHARP EDGES AND CORNERS UNLESS OTHERWISE SPECIFIED
Tolerance unless otherwise specified:
2 PLACE DECIMAL ±
3 PLACE DECIMAL ±
ANGULAR ± 0° 30'

MATERIAL	DRAWN: R. PARR	DATE: 11/2/83	APPROVED: [Signature]	DATE: 10/2/83
FINISH	CHECKED: R. PARR	DATE: 11/2/83	APPROVED: [Signature]	DATE: 10/2/83
TITLE: LOGIC BOARD				
DWG. SIZE: D		CODE IDENT. NO.: 52541	NUMBER: 112-2831-0000	REV: [Blank]
BEEHIVE INTERNATIONAL 4910 AMELIA EARHART DR. SALT LAKE CITY, UTAH				

DWG. NO. E112-2831-0000

REV	DESCRIPTION OF CHANGE	DATE	BY



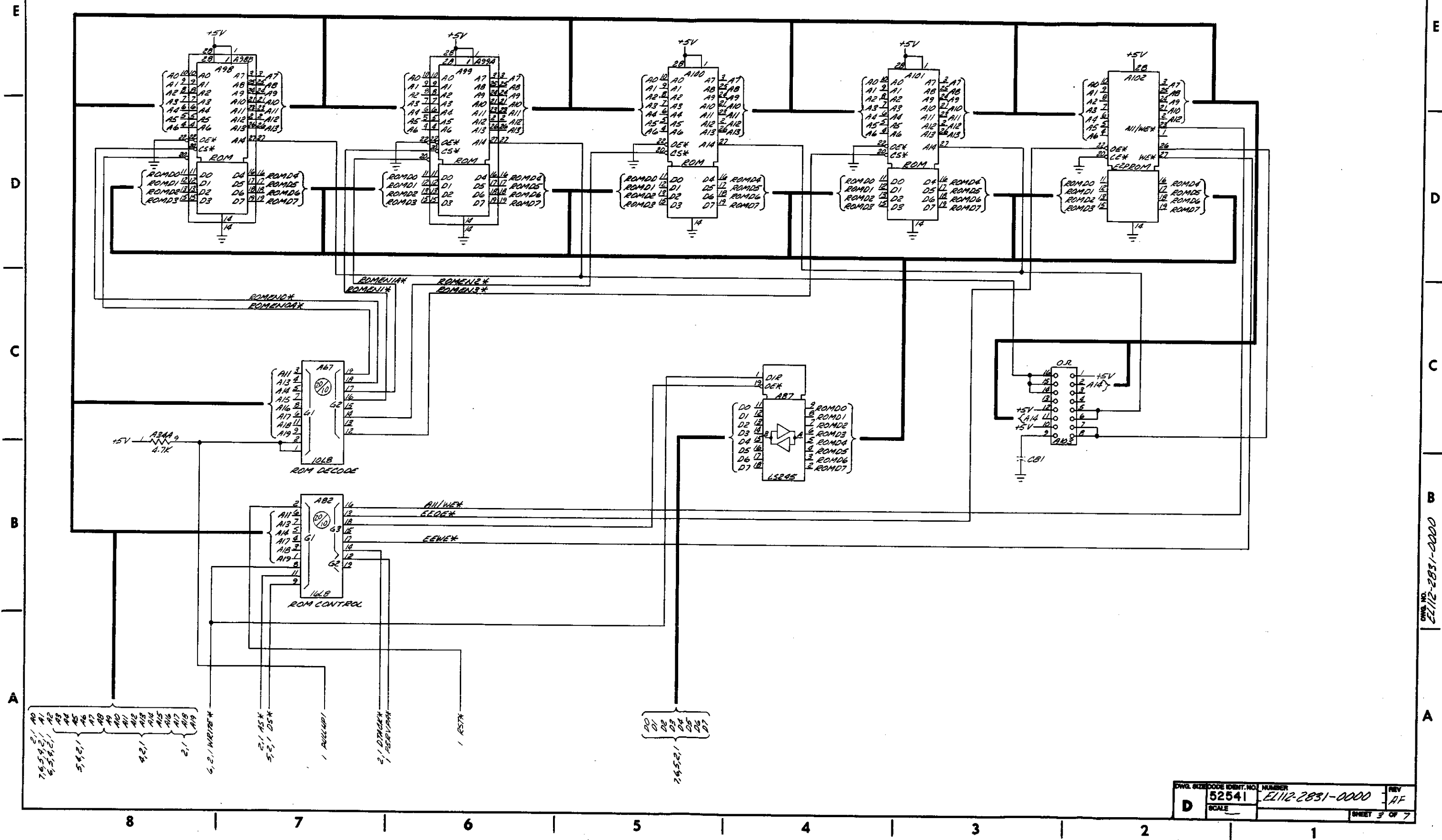
D	52541	EL112-2831-0000	REV AF
SCALE		SHEET 2 OF 7	

0000-1802-21123

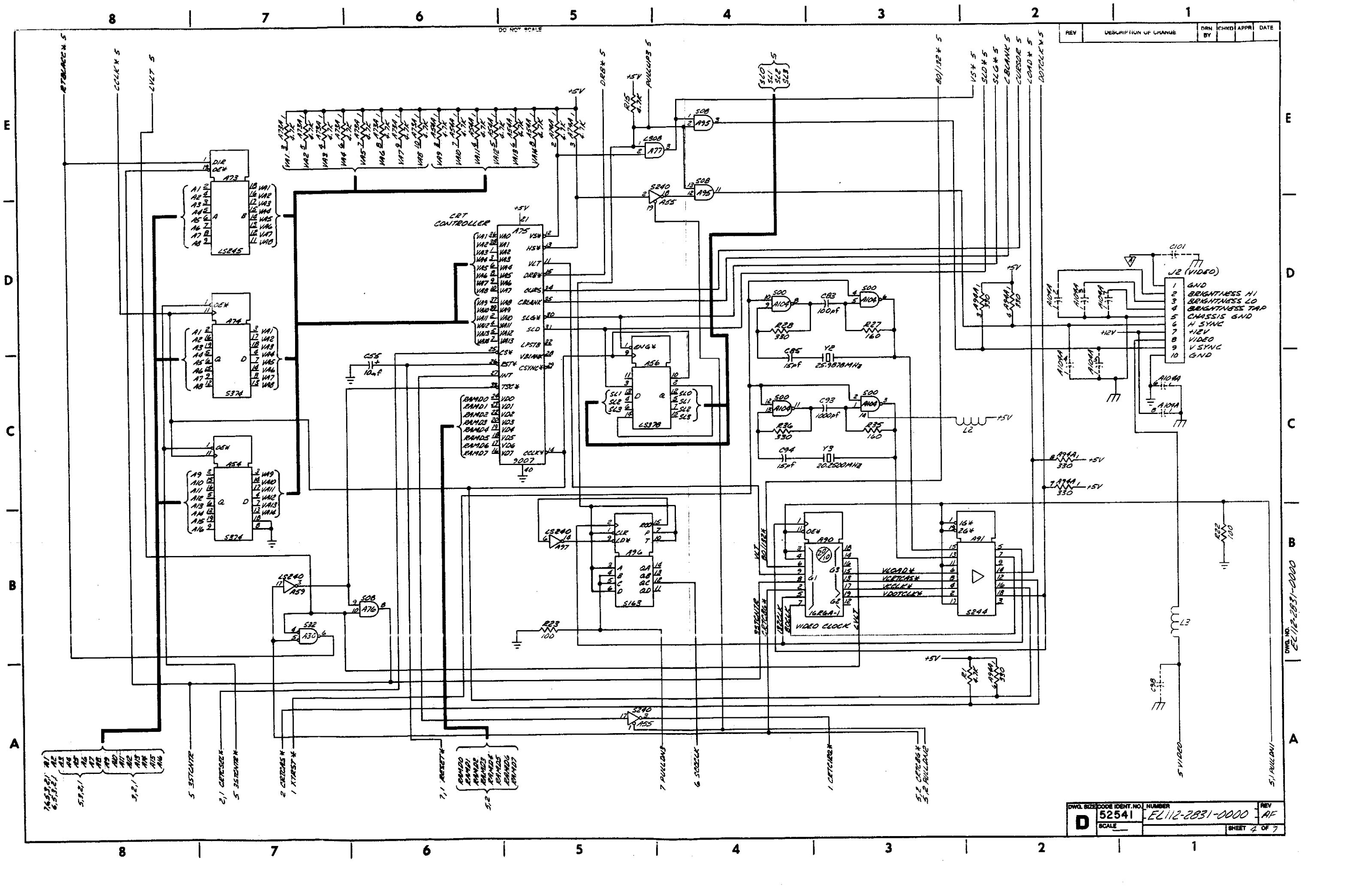
DO NOT SCALE

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE

NOTE:
 A98B AND A99A ARE PLACED ABOVE A98 AND
 A99 RESPECTIVELY. A STACKED SOCKET WITH
 PIN 20'S BROKEN OUT WILL BE USED.



DWG. NO. EL112-2831-0000



REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE

DWG. SIZE	CODE	IDENT. NO.	NUMBER	REV
D	52541	EL112-2831-0000	AF	
SCALE				

DWG. NO. EL112-2831-0000

SHEET 4 OF 7

DO NOT SCALE

REV	DESCRIPTION OF CHANGE	DRW. BY	CHKD	APPR	DATE

E

E

D

D

C

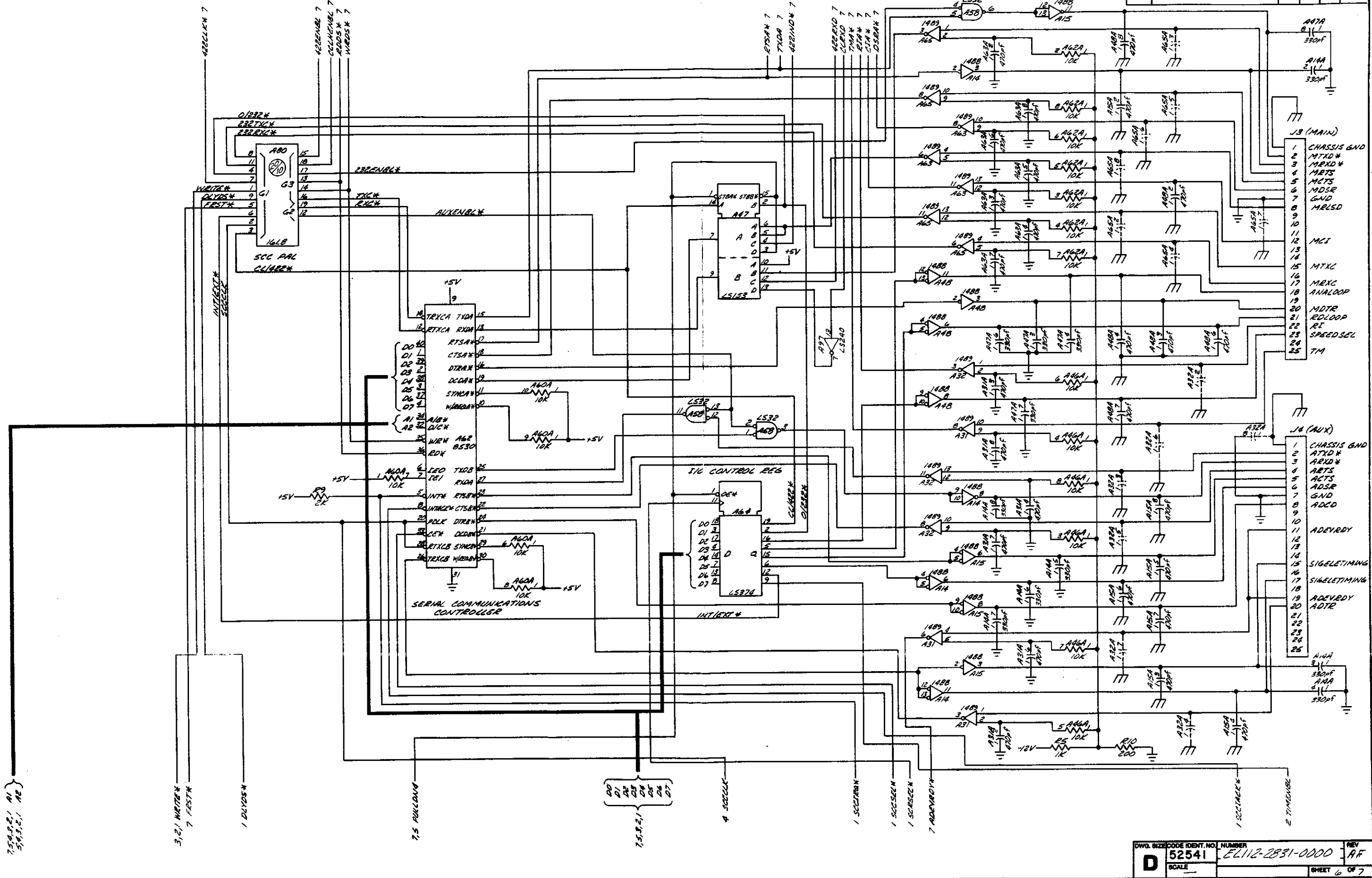
C

B

B

A

A



- 13 (MAIN)
- 1 CHASSIS GND
 - 2 MTKD*
 - 3 MTKD*
 - 4 MTS
 - 5 MTS
 - 6 MDSR
 - 7 GND
 - 8 MRLSD
 - 9
 - 10
 - 11 MCI
 - 12
 - 13
 - 14
 - 15 MTKC
 - 16 MTKC
 - 17 MEXC
 - 18 ANALOOP
 - 19
 - 20 MDTR
 - 21 EDLOOP
 - 22 RT
 - 23 SPEEDSEL
 - 24
 - 25 TM

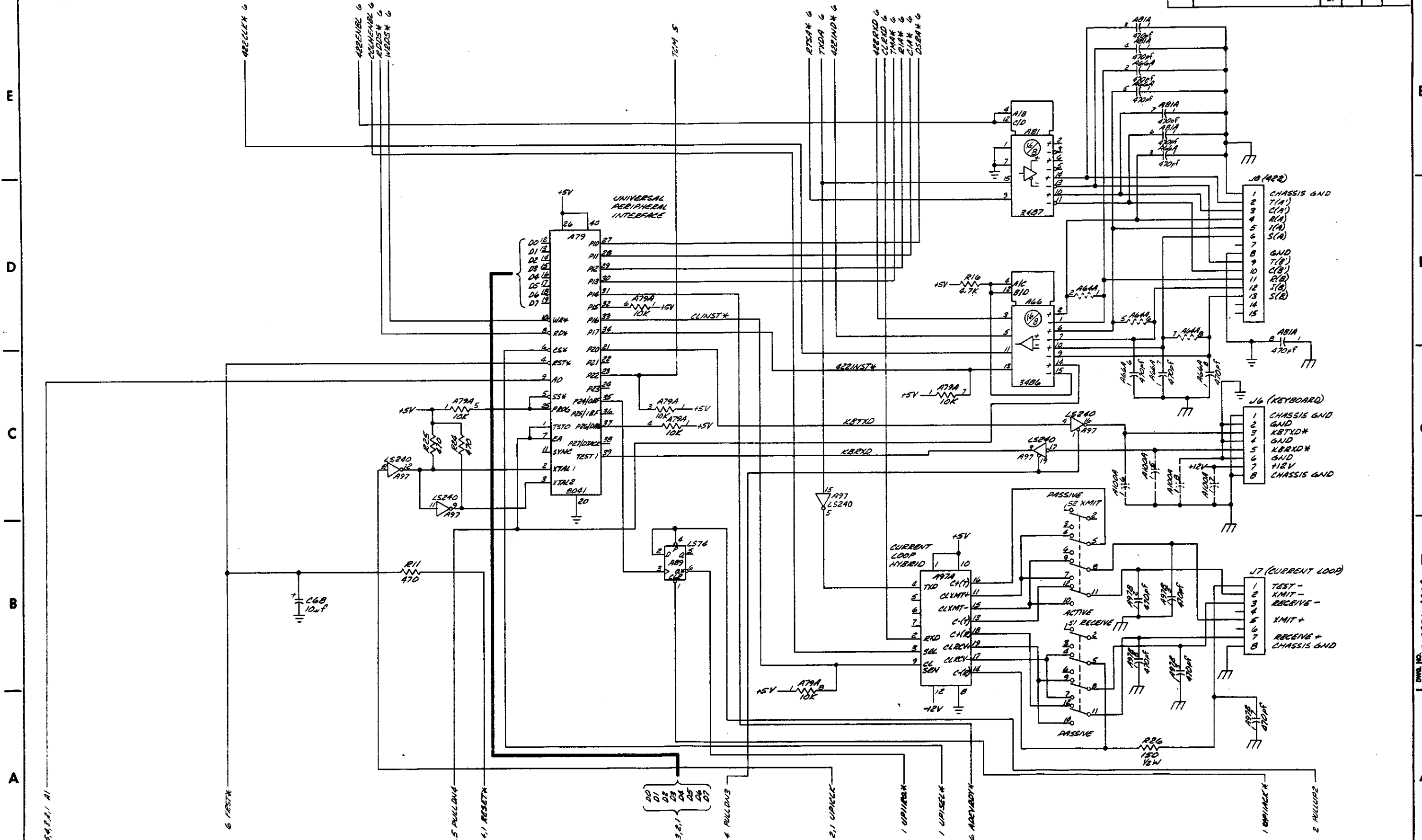
- 14 (AUX)
- 1 CHASSIS GND
 - 2 MTKD*
 - 3 MTKD*
 - 4 MTS
 - 5 MTS
 - 6 MDSR
 - 7 GND
 - 8 ADGD
 - 9
 - 10
 - 11 ADEVRDY
 - 12
 - 13
 - 14
 - 15 SIGLETTIMING
 - 16 SIGLETTIMING
 - 17
 - 18 ADEVRDY
 - 19 ADTR
 - 20
 - 21
 - 22
 - 23
 - 24
 - 25

DWG NO. EL112-2831-0000

DWG. SIZE	CODE IDENT. NO.	NUMBER	REV
D	52541	EL112-2831-0000	AF
SCALE	SHEET 6 OF 7		

REV	DESCRIPTION OF CHANGE	DRN BY	CHKD	APPR	DATE

DO NOT SCALE



6.5, 7, 2, 1 A1
 6. FRS7X
 6.5, 7, 2, 1
 4. PULLDN3
 2.1. UP/CLK
 1. UP/RSK*
 1. UP/SEL*
 6. ADV/ADYN
 1. UP/INCK*
 2. PULLUP2