How to maintain the CONSUL 980

ADDS
Applied Digital Data Systems, Inc., 100 Marcus Boulevard, Hauppauge, N.Y. 11787

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1. INTRODUCTION

This manual is intended for use by personnel who must perform fault diagnosis and repair of the Consul 980. The reader should be familiar with ADDS publication number 98-3000, HOW TO USE THE CONSUL 980, which presents complete operating instructions and interface information. Before proceeding with the Theory of Operation, salient terminal features are described below.

1.1 General Description

The Consul 980 is a low cost TTY compatible CRT display terminal. It is designed for users who wish to take advantage of a CRT's silent operation, fast transmission speed and inherent reliability. It is a self-contained desktop unit.

The 980 displays data in a format of 24 lines with 80 character per line - making a total of 1920 characters. Data is displayed as black characters on a white background. Communications with the data processing system or a minicomputer takes place a character at a time on a conversational basis, or in the form of message blocks.

1.2 Salient Terminal Features

EIA and Current Loop Interface
An EIA RS232C voltage interface and a 20 milliampere current loop interface are standard. Both are operational over the full speed range of the terminal up to 9600 baud.

Five Transmission Speeds
Transmission rates of 110, 300, 1200, 2400 or 9600 baud are selectable by means of a switch on the rear panel.

Half/Full Duplex
A DPDT switch on the rear panel permits selection of full or half duplex operation.

Cursor Control
Cursor controls to position the cursor up, down, forward, backward and home are available. Home is the lower left corner in CONV mode, and upper left corner in non-conversational mode.

Hard Copy Interface
Allows attachment of a serial or parallel printer. The operator can control the flow of data to the printers by using the PRINT ON, PRINT LOCAL and PRINT OFF keys on the 980 keyboard.

Audible Alarm
The BEL code causes an audible alarm in the 980 to be activated.

Remote Control
The 980 is a completely remotely controllable terminal. The CPU can directly address any cursor position on the screen, insert or delete lines, read the current cursor location, ring an audible alarm and control the flow of data to the peripherals.

Editing Features
The 980 has some powerful editing features. Besides the five cursor movements mentioned, the 980 can insert/delete a character at a time or insert/delete an entire line of characters, do horizontal tabbing and erase the screen.

Graphics
A graphics capability is available on the 980 which provides a matrix of 11,520 "graphic" elements. These elements can be used to generate business-level graphs such as bar-charts and trend curves.

Formatting
A formatting feature which can be used in either the Page or Message mode permits simultaneous display of both fixed and variable data. This feature not only makes data entry easier and faster, but also helps assure complete entry of all required data.

1.3 General Specifications

a)	MEMORY Size:	1920 Characters
b)	SCREEN Size:	12" Diagonal
c)	SCREEN PRESENTATION:	
	# of lines	24
	Character/Line	80
	Character size	0.1" wide (Typ.) by 0.2" high (Typ.)
	Color	Black Characters on a a White background
	Character Set	96 Upper/Lower case ASCII characters
	Refresh Rate	60 frames/second
d)	COMMUNICATIONS INTERFACE:	
	EIA	Conforms to RS232C; operates at 110, 300, 1200, 2400, 9600 baud
	Current Loop	20 milliamperes; operates at 110, 300, 1200, 2400 9600 baud
	Mode	Full/Half Duplex
	Code	USASCII
	Parity	Odd, Even, Marking or Spacing

e) OPERATING MODES:

Conversational	Character at a time
Message	Line at a time
Page	Full screen at a time
f) EDITING FEATURES:	Character and line insert/ delete, character overwrite, horizontal tabbing, cursor movements
g) WEIGHT:	52 lbs. maximum
h) PHYSICAL DIMENSIONS:	21" x 14" x 23"
i) POWER:	110V at 60 Hz, 165VA 220V at 50 Hz
j) TEMPERATURE:	0° to 50°C (operating) 0° to 85°C (storage)
k) HUMIDITY:	0° to 95% RH, non-condensing

2. THEORY OF OPERATION

A block diagram overview of the Consul 980 electronics is presented in this section. It is followed by a detailed circuit description at the circuit level.

2.1 General Summary

The Consul 980 electronics package is made up of five basic blocks. They are the Front End, the Control, the Memory, the Video Generator and the Option. Each block is wholly contained on one printed circuit card. A single input/output data buss architecture is used to ease system design.

2.1.1 Front End

The Front End block contains the Universal Asynchronous Receiver/Transmitter (UAR/T), EIA level shifters, 20 ma current loop converters, keyboard interface, the RS232C control logic, the Output Encoder, the Read Logic and the switch-selectable baud rate clock for asynchronous communication.

2.1.2 Control

The Control block contains the code Decoder, the Cursor Control Logic, the Data Access Logic, the scroll logic and the Transparent Mode Logic. It also contains the master oscillator along with a divide by 8 counter, the three character generators and the video shift register.

2.1.3 Memory

The Memory block contains the Display Buffer Memory and its associated 2-phase clock generator, the one line Refresh Buffer Memory, the access logic to control input to the Display memory, the "look ahead" compression logic and the output multiplexer. The buffer for the parallel printer is also on this block.

2.1.4 Video Generator

The Video Generator contains the timing chain counters for controlling all video signals, the video amplifier and mixer, sync and blanking generator, display select and cursor generators, the blink circuit, the 1 of 3 ROM's enable circuit, the Address Registers and the Tracking Registers. It also contains the multiplexer to output the current cursor address.

2.1.5 Option

This block contains all the options offered with the Consul 980. These include line insert/delete, charachter insert/delete, graphics mode and serial and parallel printer interface.

2.2 Block Diagram Description

The overall system block diagram Figure 2.1 shows the four major sections, the Front End, the Control, the Memory and the Video Generator, divided by dashed lines.

A single 7-bit wide data buss runs through the whole system. All output data rides on this buss. The Front End accepts this parallel data, converts it to serial data, and sends it out on the communication lines. All incoming data has to enter the system through the Front End. The serial input data is converted to parallel data, 7-bit wide. These bits are then used on the Control, the Memory and the Video Generator for specific purposes.

The Control section decodes the 7-bit data. Depending on whether it is a control code or not it activates the Access and Control Logic, to perform the corresponding control function if it were a control code or to load the data into the Display Memory if it were a message character.

The Display Memory is modular in organization. It is made up of both dynamic and static shift registers whose contents are continuously recirculated at a rate of 1.6 MHZ. The entire Display Memory has a storage capacity of 1920 x 8 bits. The Display Memory feeds a Refresh Memory of 80 x 8 bit capacity. It provides the 6 refresh bits for the character generator to generate a 5-dot pattern for every scan line. A total of 7 such 5-dot patterns are required to display a character on the screen. These 5-dot patterns from the character generator are applied to the video mixer. Here it is mixed with other timing signals. The composite signal is then amplified and applied to the video monitor.

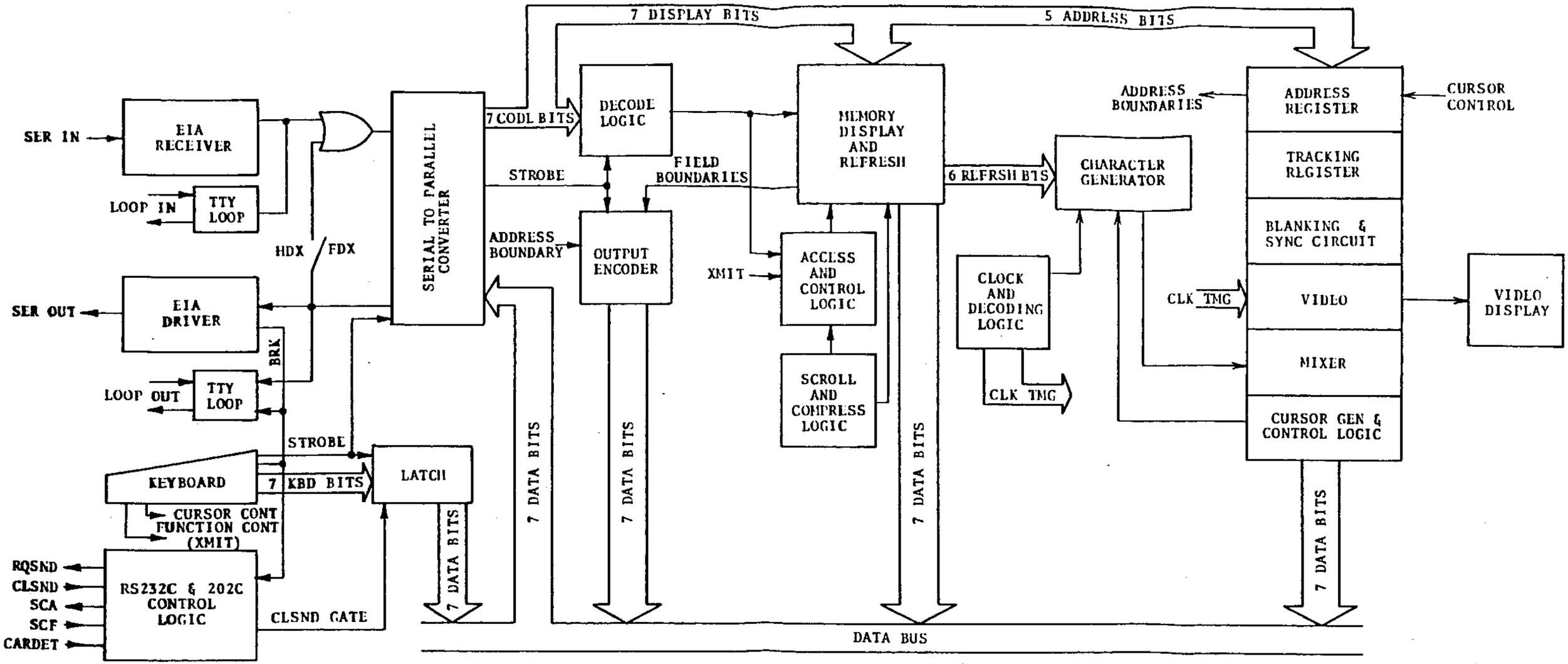
The 980 system consists of one more section - the Option Card. It provides all the Options available on the Consul 980.

2.2.1 Front End

2.2.1.1 Input Data Path

Input data to the Front End can be either current loop or EIA serial data. The serial data stream [Figure 2.2] is converted to TTL levels and applied to the UAR/T which converts the serial data to parallel data. The parallel data, together with a strobe pulse, is presented to the decoding logic on the Control block. If the character is displayable it is also presented to the Display Buffer Memory on the Memory block. All illegal characters and RUBOUT are ignored by the CRT.

SYSTEM BLOCK DIAGRAM - 980
Fig.2-1



2.2.1.2 Output Data Path

Output data rides on a single 7-bit data buss. It is generated in one of the following ways: the keyboard, the memory (during read operation), the output encoder (outputting the active control characters like LF, CR, SO, SI, GS, ESC, ETC) or in response to the external request for current cursor position. The ASCII code together with a strobe is then presented in parallel, if proper conditions exist at the RS232C control logic, to the UAR/T for parallel to serial conversion. The serialized data is then converted from TTL levels to EIA levels, or current loop signals, and sent to the modem or the CPU.

2.2.1.3 Full/Half Duplex Modes

Full/Half Duplex is controlled by a SPDT switch on the rear panel. In FDX, conversational mode the serial TTL output goes only to the level converters for output. In HDX mode the serial output data is also routed to the UAR/T. This causes the output character to be treated as an input character from the CPU.

2.2.1.4 RS232C Control Logic

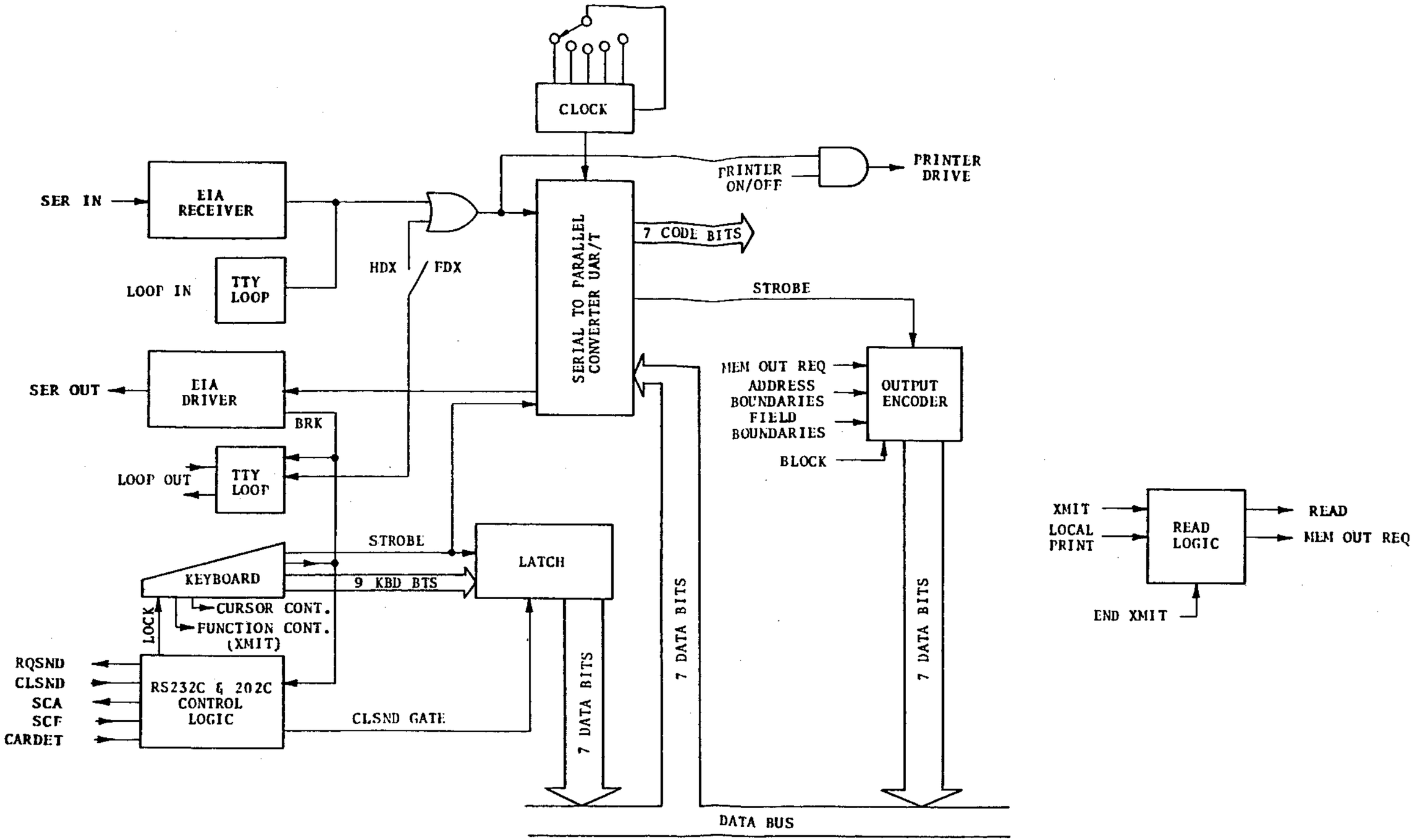
This logic handles all the necessary control lines to and from the EIA connector. The first character of a message transmitted, or keyed out live in conversation mode, raises Request to Send. As soon as Clear to Send (from the CPU) goes true the character riding on the output buss is loaded into the UAR/T for transmission. The reverse channel signals SCF and SCA are also controlled by this logic.

2.2.2 Control

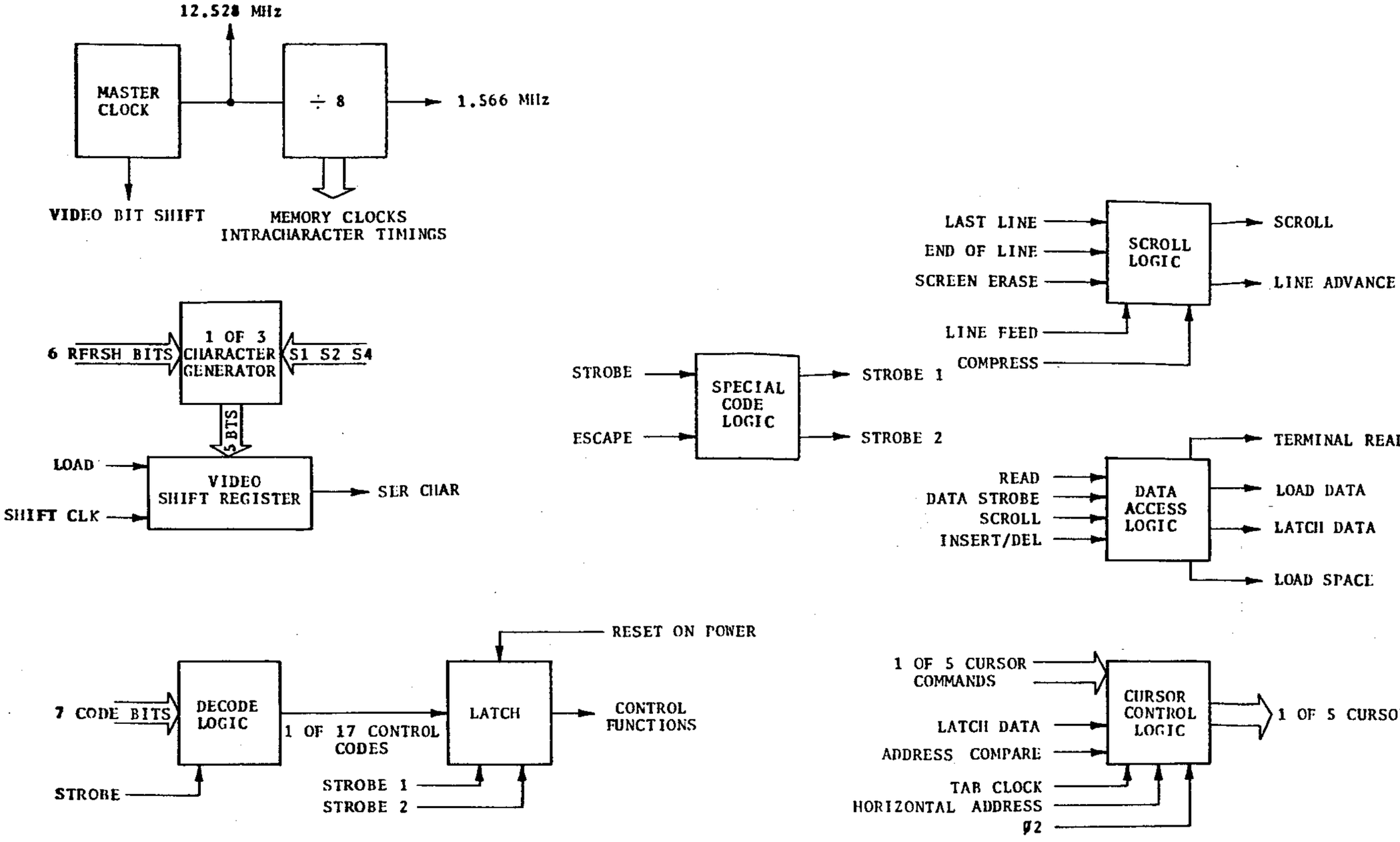
2.2.2.1 Decode Logic

The parallel data from the UAR/T on the Front End block is presented to the decoding logic on the control block [Figure 2.3]. If the 7-bit code is a Control code it is decoded into one of 17 control codes. These are then latched to form control functions, each performing a specific task. All illegal control codes are ignored. Non-Control characters are written into the memory.

FE/ASYNC BLOCK DIAGRAM
Fig. 2-2



CONTROL BLOCK DIAGRAM
Fig. 2-3



2.2.2.2 Access Control

The Access Control accepts the control functions from the decoder, and performs the task requested. These tasks include data input, erase functions and scrolling.

2.2.2.3 Cursor Control Logic

This logic accepts 1 of 5 cursor commands from the keyboard and causes the corresponding cursor movements. It also handles horizontal addressing and tab functions.

2.2.2.4 Character Generator

The character generator accepts one character at a time from the Refresh Memory and then outputs the proper portion of the character to be displayed.

The line of characters in the Refresh Memory is presented to the generator seven times to complete the display of that data line.

2.2.3 Memory

2.2.3.1 Display Buffer

The Display Buffer memory is composed of shift registers that recirculate their contents at a 1.6 MHz Shift rate. The memory is modular [Figure 2.4] in that it is divided into three sections. Each section has a capacity of 5120 bits or 640 8-bit characters.

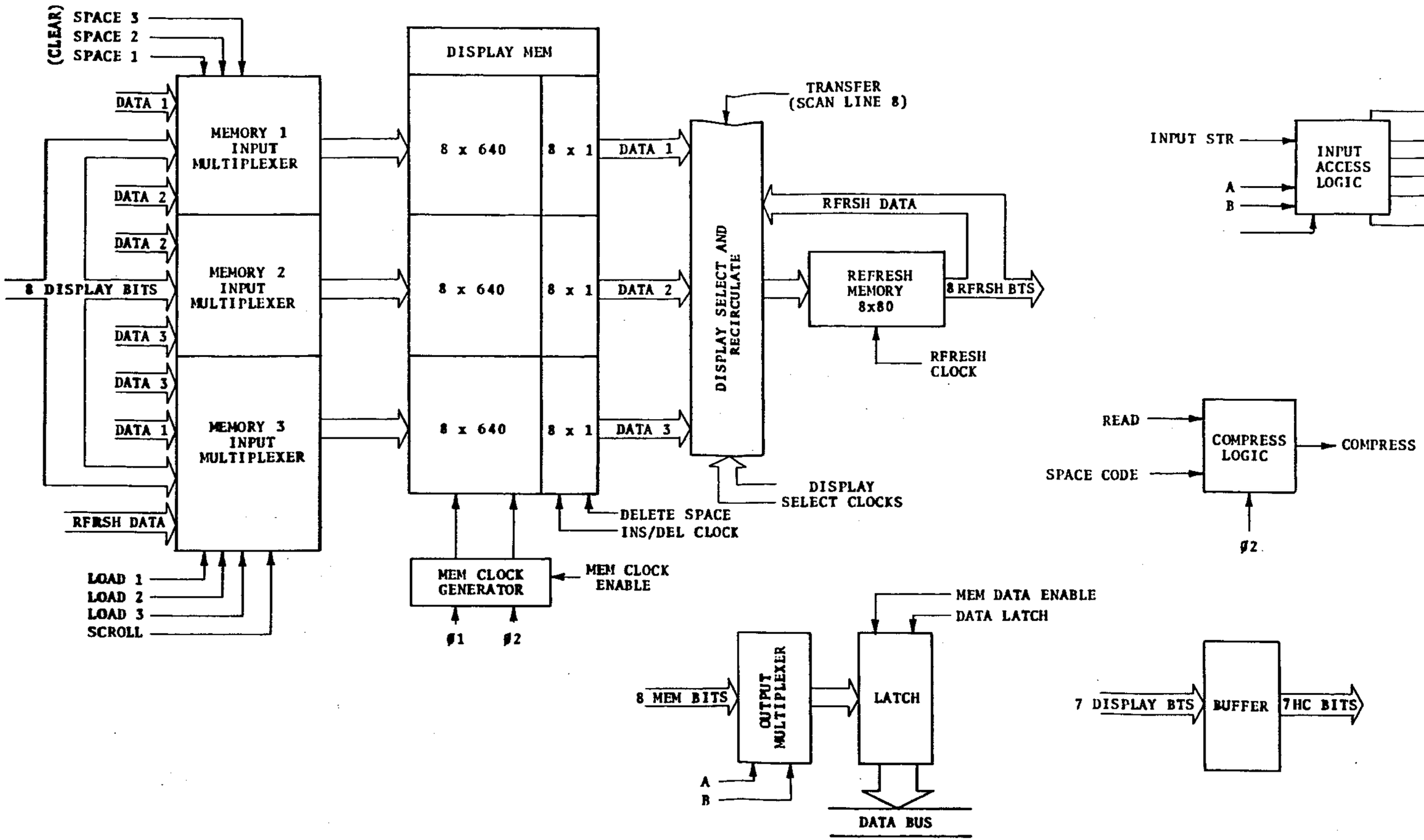
2.2.3.2 Refresh Buffer

This is made up of a static shift register which has a capacity to hold 100 8-bit characters. However, only 80 characters of a particular data line are used for display. The Refresh Buffer holds one line of characters during the time the character generator is generating that particular line of data on the Consul screen. It is updated after every 9th scan line or at the end of every logic line by one of the 640 character modules.

2.2.3.3 Compression Logic

This logic incorporates the "look ahead" feature in the terminal. During the read operation this logic scans ahead in each line.

MEMORY BLOCK DIAGRAM
Fig. 2-4



If the remainder of the current line is blank, (i.e., filled with SPACE codes), one space code is output and the line is then terminated by sending the proper codes. If in Page mode, the next line is output following the CR/LF codes. If in message, the transmission is terminated with a CR.

2.2.3.4 Output Multiplexer

During transmission this circuit accepts data from the memories and outputs it on the data buss through a tri-state latch.

2.2.4 Video Generator

2.2.4.1 Clock and Timing Chain

This consists of the Master clock followed by a countdown chain and its associated decoding logic [Figure 2.5]. This chain generates all the timing signals required for video presentation and memory timing.

2.2.4.2 Video Amplifier & Mixer

The blank and sync signals and the video display signals are mixed by the mixer to form composite signals. These are then amplified by the amplifier to the level required to drive the CRT.

2.2.4.3 Address Register

The Address Register contains the address of the location in which a character may be entered into or fetched from the Display Memory module.

2.2.4.4 Tracking Register

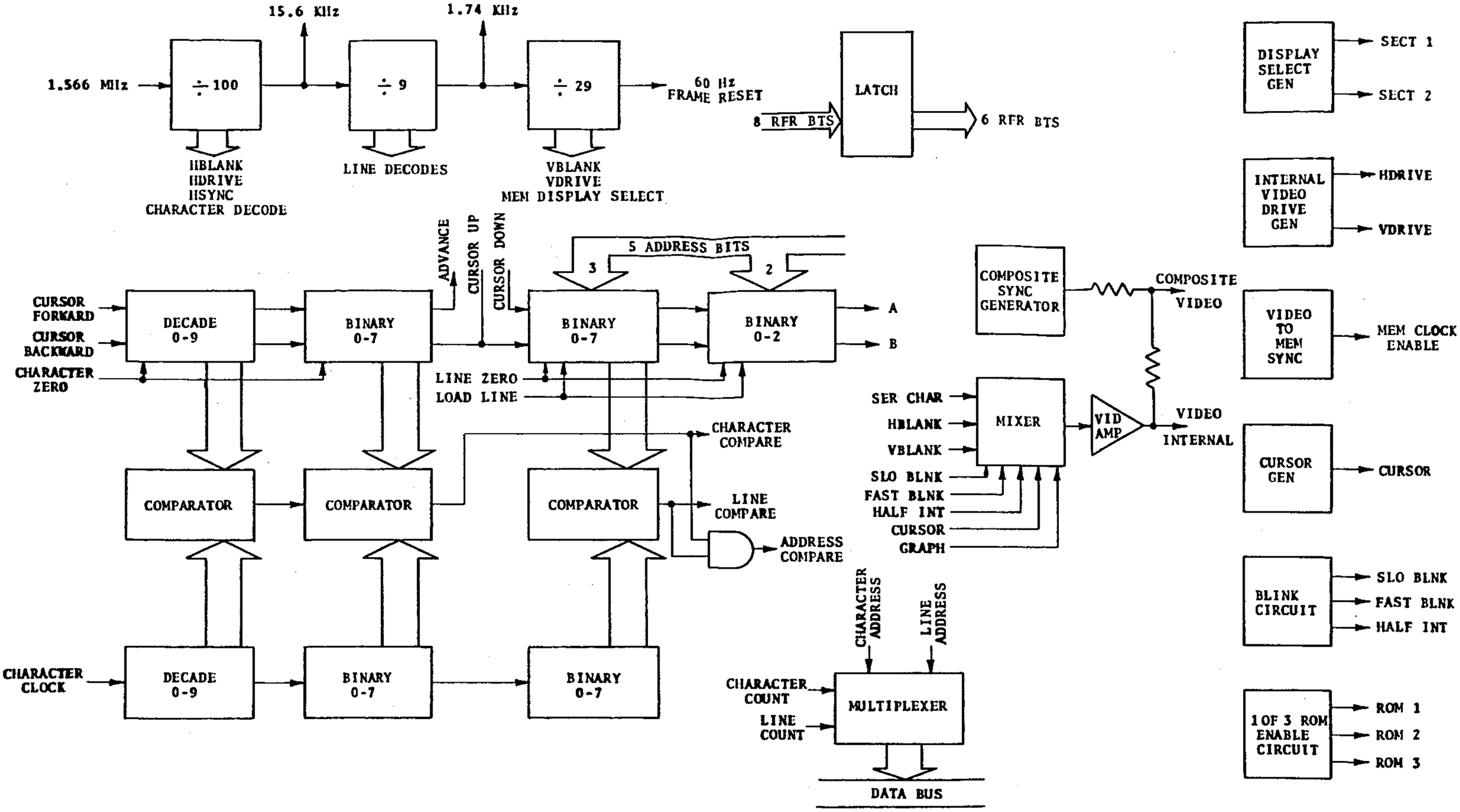
The Tracking Register tracks the Memory Registers by counting the shift pulses to the Display Memory. Its contents at any given time represents the address of the memory location that is available for access.

2.2.5 Option

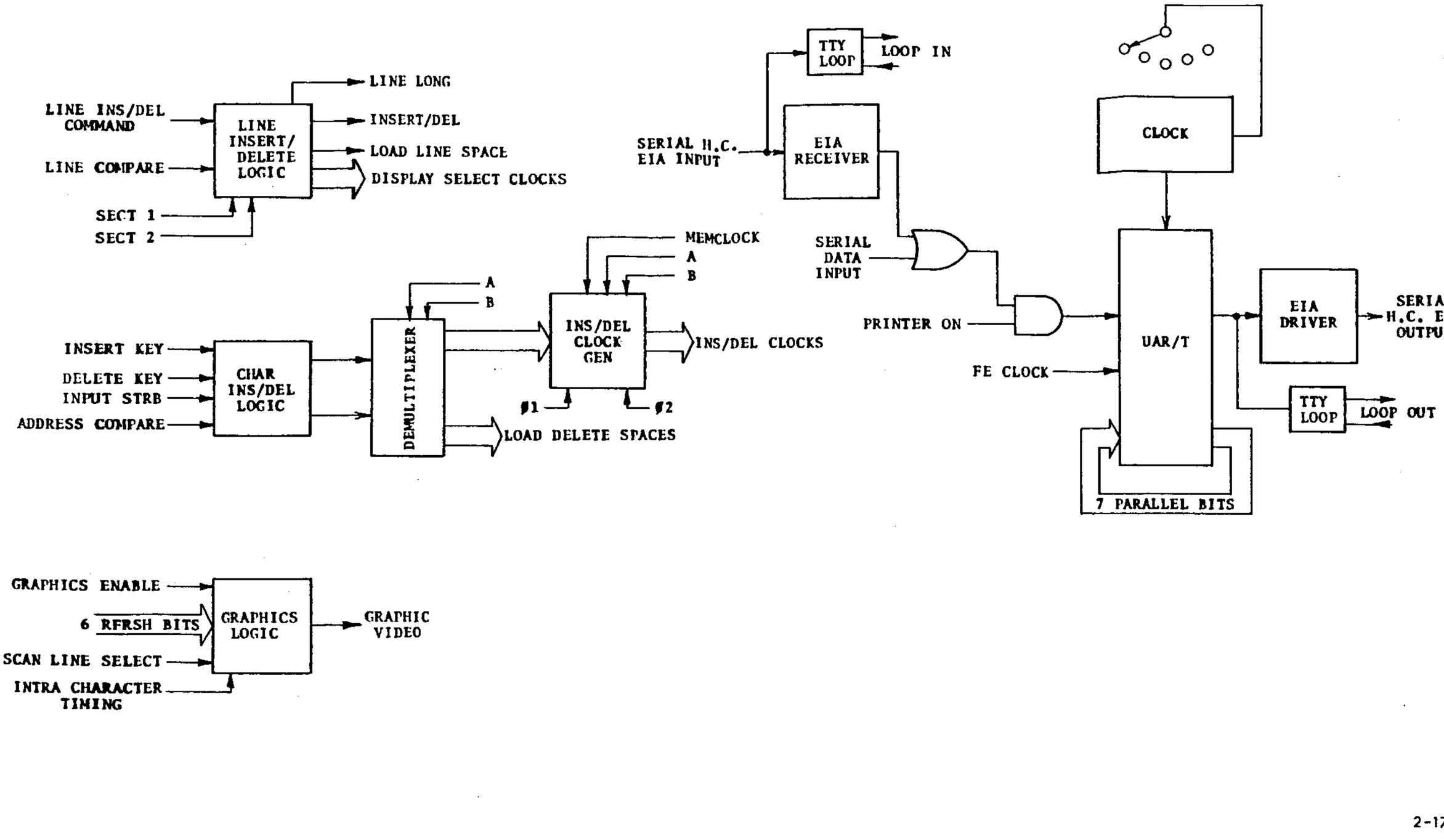
2.2.5.1 Insert/Delete Logic

This is a powerful editing feature that enables insertion or deletion of a single character or a complete line of characters at any memory location [Figure 2.6].

VIDGEN BLOCK DIAGRAM
Fig. 2-5



OPTION CARD BLOCK DIAGRAM
Fig. 2-6



2.2.5.2 Graphics Logic

This logic enables the 980 to present display video in both graphical and/or alphanumeric mode.

2.2.5.3 Hard Copy Interface

This consists of a UAR/T and its associated logic. It helps to channel, and control, the flow of data to both the serial and parallel printers.

2.3 Detailed Circuit Description

2.3.1 Front End - Schematic #135-088

2.3.1.1 Serial to Parallel & Parallel/Serial Conversion

The serial to parallel and parallel to serial conversion of data is handled by the Universal Asynchronous Receiver/Transmitter or UAR/T in section 2C and 2D. This UAR/T is an LSI subsystem which accepts binary characters from either a terminal device or a computer, and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 1 to 7 bits, a parity bit and one/two stop bits.

2.3.1.1.1 Receiver Operation: On applying power, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud rate. The previous conditions will set data available (DA, Pin 19) to a logic "0".

After initialization is completed, data reception starts when serial input (Pin 20) signal changes from marking (logic "1") to spacing (logic "0"). This initiates the start bit. The start bit is valid if, after transition from logic "1" to logic "0" the SI line continues to be logic "0", when centre sampling occurs. If the SI input is not at logical zero, the start bit verification process will be reset. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s) reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits previously set on switches K1-0, K1-7, L1-6 & L1-7. If a Framing Error or a Parity Error is detected, it will be indicated by raising the corresponding lines (Pines 14, Framing Error and 13 Parity Error) to a logic "1". This error can be displayed on the screen as a RUBOUT code by closing switch E1-1.

Once a full character is received, internal logic looks at the data available signal (DA, Pin 19) to determine if data has been received. If DA is at logic "1" it means that data has been received and is ready to be accessed. When this occurs signal DA goes true, and the rising edge of the clock produces the strobe INS which forms the input strobe INST to the system. At the same time the DA signal is reset by the signal RDA (Pin 18) [Section C-3]. The receiver is now ready to transfer the next character received to its output register.

2.3.1.1.2 Transmitter Operation: In order to output a character it has to be presented in parallel to the UAR/T and be given a strobe. Due to the single data buss architecture of the system, data can be presented to the UAR/T either from the keyboard or from the memory (during read operation). In either case, the signal DS* [see Section B2, B3] Data Strobe is generated which strobes the data into the UAR/T. Once DS* is pulsed, the TBMT signal [Section D2] will change from a logical "1" to a logic "Ø" indicating that the data bits holding register is filled with a character, and is unable to receive new data bits. The parallel data is then converted to serial data within the UAR/T and appears as SDOT [Section C2]. When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that a new character is ready for transmission. It is assumed that Clear to Send - CLSND [Section B2] is true. If CLSND is false the data strobe F/F A7 will be held reset and no data can be output.

2.3.1.1.3 Receiver/Transmitter Timing Clock: The clock to the receiver and the transmitter is SCLK [Section B3]. It is generated by a differential comparator J7 [Section A4]. The output FCOM is returned to the negative input via any one of the 5 switch selectable paths. These provide the five baud rates: 110, 300, 1200, 2400 and 9600. When the output swings from 0 to 5V (referenced by the zener D9), the positive input swings from 3.3V to 1.65V. Alternate charging and discharging of the timing capacitor C6 causes the output to provide a stable clock.

2.3.1.2 Read Operation

We have seen that when a character is loaded into the UAR/T, the UAR/T flags us with the signal EIARDY (which is the same as FERDY)-[Section B2]. FERDY is then used to produce an input strobe INST [Section C3]. INST is used within the system during both the read and the write operations. During write operation INST is used (On Control Card) to load data into the memory, and during the read operation it is used to fetch characters from the memory. In either case INST generates a flag signal TRDY - Terminal Ready, which is self-explanatory.

At the start of the READ operation, READT [Section D4] pulses low and sets the READ F/F. At the same time INST goes true and fetches the first character from the memory. When TRMRDY goes true, Memory Out-Put Request (MOTRQ) is set true which in turn produces the Data Strobe DS to the UAR/T. Once the character is transmitted FERDY goes true. This resets the circuit and produces the second input strobe to go fetch the second character. This continues till the READ F/F is turned off by TEND (End of Transmission).

When reading, the UAR/T has to output not only the data in the memory but also codes like End of Page Code or End of Message Code and other special codes like SO, SI, GS, LF, and ESC. These codes are all generated by their respective circuits [as shown in Sections D1, D2 and D3]. Upon generation of any of these codes a signal BLK (Block) goes true and blocks the INST. At the same time it outputs these special codes via the output encoder. [Section B4 and C4]. The output encoder rides on the output buss. Proper logic is used to put the respective codes on the line. Switches K1 and L1 can be used by the customer to generate his choice of End of Page and End of Line Codes respectively.

2.3.1.3 Write Operation

The Write function can be performed either from the keyboard or through the serial interface. In either case the serial data received by the UAR/T causes the flag DA to go true. This then forms INST [Section C3] which is used by the Control Card to load data into the memory.

When coming from the keyboard the 9-bit ASCII code is presented in parallel to the Front End. These bits are then latched [Section D4] and output on the data buss. They are converted to serial data in the UAR/T, turned around and fed back to the receiver. Thus to the receiver the keyboard looks like the CPU, and it treats it so in Half-Duplex mode. However, in Full-Duplex mode the data from the keyboard is blocked by FDXRQ (Full-Duplex Request) [Section B1].

2.3.1.4 RS232C Interface

The voltage swing for the standard EIA RS232C interface is +3V to +25V for a logic "0" on the data line and -3V to -25V for a logic "1" on the data line. Control signals Request to Send (EIARTS) and Clear to Send (EIACLS) have the same voltage swing with + V being on and - V being off. (In this system the swing is limited within -13V to +13V).

The SDOT (Serial Data), which is at TTL levels, is level shifted to EIA levels by the EIA driver A1 [Section B1] to form SEIAOT (Serial EIA Output).

Similarly SEIAIN (Serial EIA Input) [Section C1] is at EIA levels and is shifted to TTL levels by the EIA receiver A3 to form SDIN (Serial Data Input) which in turn is applied to the UAR/T.

The Request to Send Circuit is in Section C1. Whenever OUTEN (Output Enable) is true it sets the RQSND (Request to Send) F/F C7. RQSND is then converted to EIARTS (EIA Request to Send) by the driver A1.

The EIACLS (EIA Clear to Send) [Section C1] is likewise received by the receiver A3 and delayed for about 2 msecs. to form CLSND (Clear to Send).

2.3.1.5 Current Loop

The current loop interface is in Section B1. A0 and A2 are isolators. The input stage is A0. When current is present A0, 4 and 5 present a low impedance. Q1 is turned ON and holds the EIA input at about 0V- (Switch E1-2 is closed). When the loop breaks, A0, 4 and 5 present high impedance turning Q1 OFF. This pulls the EIA input to +5V. Thus the presence or absence of current swings the EIA voltage between 0V and +5V. Diodes D4 and D5 work as speedup diodes insuring the Q1 does not get over saturated.

The output stage is A2. For a Mark condition on the data line A2, 4 and 5 present a low impedance. Q3 is turned ON thus closing the loop. When a Space condition occurs Q3 gets turned OFF thus breaking the loop. Diodes D3 and D6 are for reverse voltage protection.

2.3.1.6 Generation of Special Codes

During the READ operation the Front End has the responsibility to insert special codes such as SO, SI, GS, LF, CR, ETX in the data stream. It does this by means of the output encoder -[Section B, C-4]. In this Section it will be shown how these codes are generated.

The Shift Out and Shift In codes are generated by the F/F pair F5 [Section D3]. TAGL (Tag Latch) is a signal that latches true at the first tag bit latched for output in the memory. F6, 11 pulses low for a 100 nanosecond and sets F5, 8 false. SO* (Shift Out*) going low is encoded on the encoder to give the Shift Out code SO. When SO is transmitted FERDYB resets F5, 8 true again. At the end of the tag field, TAGL goes low. This causes a 100 nanosecond pulse on F6, 6 and sets F/F F5, 6 low. This time the Shift In code SI is sent out on the encoder. The F/F is reset by FERDYG. Note that SO and SI are not allowed to go out if the non-variable fields are in protected mode, i.e., FON is true.

If FON is true a Group Separator code GS is sent out before each protected field. GS is generated by the F/F pair B6 [Section D-2]. When FON is true, and the first tag bit is at the output of the memory B6, 5 goes true. GSEN (Group Separator Enable) going true causes C6, 8 to pulse low (since TAGL is true). This sets B6, 9 true and the Group Separator code GS is output on the buss via the encoder. Also B6, 5 is reset by GS* going false and this resets the circuit.

The Carriage Return and Line Feed circuit is in Section D-3. CRSND* (Carriage Return Send*) is made on the Memory card. During READ operation, if CRSND* pulses false, its trailing edge sets up F4, 5 true. CREN (CR Enable) resets the latch J4, 8 true. A6, 6 goes true and the trailing edge of the previous FERDYB sets up F4, 9. EOL (End of Line) is a signal that can be coded as any code by switch Module L1. Normally it is coded as a CR. This then puts the CR code on the buss. EOL* resets F4, 1, and the trailing edge of FERDYB resets F4, 9 low. In Message mode the transmission chain dies here and the READ F/F is reset. However, in Page mode, when EOL goes true it sets up LFEN (Line Feed Enable) and a LF code is output on the buss after a CR code. This will continue till the READ F/F is reset by TEND* (End of Transmission*).

The EOM (End of MEMORY) code is normally an ETC code, however, the customer has the option to select his own code by proper switch settings on the switch module K1. METX* (Memory End of Text*) [Section D-3] goes false whenever an ETX code buried in the memory is read out. When the ETX code is at the output of the memory, METX* pulses low setting the latch A4, 3 true. F6, 8 goes low and thus sets up H6, 5 true. ETXEN (ETX Enable) going true causes C5, 12 to go false provided the CR and LF codes have been sent out. FERDYB sets C4, 8 true and puts the EOM code on the buss. EOM* going low causes RSEOM* (Reset EOM*) low and this resets the latch A4, 3 false. This inserts an ETX code at the end of a partial transmission. ETXEN is also set true by the fact that the cursor has gone through the last line. At this time LSTLNE (Last Line) goes true and its trailing edge sets up ETXEN true.

There is one more special code generated by this card. It is the ESC code. Before we go into the generation of this code here is a brief description of how information is input from the keyboard. Whenever a coded key on the keyboard is depressed, a nine-bit parallel code is provided to the system along with KBSTB* (Keyboard Strobe*). The leading edge of KBSTB* causes KBRQ (Keyboard Request) to go true and this is then used to generate the signal DS* (Data Strobe*) to the UAR/T. KBRQ is also used to form KBL* (Keyboard Latch) [Section C-4] which is a strobe used to latch the keyboard bits onto the output buss. J6, 9, i.e., KBRQ is reset by FERDY going low. B1KB* through B7KB* represent the 7-bit ASCII code. B8KB* and B9KB* are used internally to perform two different functions. Whenever a particular code has B8KB* also low, an ESC code precedes that code. The ESC code is generated in Section B-3. If B8KB* from the keyboard (i.e., KBRQ is true) goes low E51 goes true and the leading edge of TRTS (X-mit strobe) sets D4, 5 true. ESCIN goes true and outputs the ESC code. At the same time, ESCIN* causes BLK to go high and prevents the INST associated with that code. This helps to delay the transmission of the required code and insert and ESC code before it. KBRQ going low resets the F/F D4, 5 low. B9KB* appended to any code puts the terminal momentarily into a full-duplex mode. The latched bit B9KBL* going low causes D3, 6 [Section B-1] to go low. FDXRQ* (Full Duplex Request*) goes low and thus puts the system in FDX mode, for that character only. B8KB* and B9KB* are low together when the 10 key numeric pad is optioned for function codes.

2.3.1.7 Miscellaneous

The Carrier Light Circuit is in Section A-3. Carrier Light ON indicates that the terminal is receiving the carrier signal from the modem.

The alarm circuit is in Section B-1. The one-shot E6 can be activated either by the BEL code, by crossing the 75th character position or by the reception of the first error in a chain of errors.

Section A-1 contains the (Power-On Reset) circuit. RST1 is a pulse train of 60Hz frequency. This is divided to provide the 30Hz, 4Hz and 2Hz clocks which are used within the system. RST is the master reset used to reset the entire system.

2.3.2 Control - Schematic #135-090

2.3.2.1 Decoding Logic

The 7-bit parallel output from the UAR/T is fed into the decoder [Section G, H - 7, 8). The decoded outputs are logically combined to obtain the 17 allowable codes as shown [Section G, H - 6]. All other coding combinations are ignored by the terminal. These are then latched to form control functions, each performing a specific task. To mention a few of these control functions: Vertical tabbing [Section D-6], Shift In and Shift Out [Section C-6], Record and Unit Separators [Section FH], Graphics Mode [Section F-3], Alarm [Section H-3].

Besides these standard ASCII codes, there are 7 special codes each preceeded by ESC. They perform the following special functions: Local Print (LPCOD), Line Insert (LNINS), Line Delete (LNDEL), Keyboard Lock (KBLOK), Print On Line (PRONLN), Character and Line Address of the Cursor (CHADR, LNADR). These special functions help make the terminal a remotely controllable device. The format of the special is ESC X. Where X is one of the allowable codes.

INST (Input Strobe) from the ASYNC/FE is used to latch all these codes to form the control functions. The normal codes are strobed with INST1 while the special codes are strobed with INST2, ESC is used to generate INST2 from INST [Section D-7].

2.3.2.2 Access Logic

From INST (Input Strobe) is derived INSD (Data Input Strobe) [Section E-6]. INSD is responsible both for loading data into the memory and for accessing the memory during READ operation. INSD strobes only for that data to which the memory is accessible. For all other data, INSD is disabled by the NAND gate F5. The leading edge of INSD sets up the F/F E2 and at the same time puts the terminal in the Busy state (TRDY* goes true) [Section E-4]. The next MEMCLK (Memory Clock) anded with ADDCOM produces the signals DLACH (Data Latch) and LOAD [Section F-4]. LOAD is used to load data into the Buffer, and DLACH is used to latch the memory data onto the output buss. DLACH also causes the cursor to advance by one character position thus updating ADDCOM (Address Comparison). The entire cycle is reset by DLACH, and the terminal returns to the READY state.

The Access Logic also contains the Transparent Mode circuit. This feature allows one to load, and store control characters in the memory. To enter the Transparent mode the terminal must receive the DLE code. Reception of DLE sets up the F/F H6 [Section F-7], thus enabling the D input of the BCD-to-Decimal Converter J6 [Section G-7]. CO* and C1* are, therefore, held high for the following control character. This enables the NAND gate F5 and thus allows INSD for that control character. At the same time, the terminal comes out of the Transparent mode. It is, therefore, necessary that all control characters to be stored in the memory be preceded separately by the DLE code.

F/F E5 [Section E-5] causes the SPACE code to be loaded into the memory during the Carriage Return and the Form Feed functions. It also enables the terminal to come up with a blank screen when power is first applied.

2.3.2.3 Scroll Logic

In Message and Page modes when the cursor crosses the page boundary it wraps around and starts again at the top of the page. However, in Conversation mode, when the cursor crosses the page boundary, the following things happen:

(i) All information is shifted upwards by one line;

(ii) The cursor goes to the beginning of the last line;

(iii) The last line is filled with SPACES.

(iv) The top most line is lost.

All these four steps make up the "scroll" function which very closely simulates the paper-feeding function in a typewriter.

The scroll logic [Section C2, 3, 4, 5] handles the scroll function. Normally switch E7, 3 is closed. Hence, in Mess./Page Modes D7, 8 is enabled while C5, 10 (Scroll Circuit) is disabled. Whenever the cursor crosses the line or page boundary LNADV (line Advance) goes true and the cursor advances by one line. However, in conversation mode, when the cursor crosses the page boundary C5, 10 goes true and produces SCROL (Scroll). This signal is then used on the Memory card to cascade the three 8-line memory blocks to form one 24-line block. All information is then shifted up by one logic line. When SCROL goes away the memories return to their original form.

In order to understand the scroll operation in a little more detail, refer to Figure 2.7. Figure (a) represents the three memory modules of 8 lines each. Just before the scroll ooperation (SCROL* goes low) the memories are tied together as one shift register of length 1920 characters. SPACE code is inserted in the last line (Line 7) of the bottom memory while the first line (Line 0) of the top memory is lost.

Returning to Figure 2.7, the registers are shifted for 80 counts in the long configuration. After 80 shifts SCROL* returns true and the memories are returned to their normal configuration as shown in Figure (b). Note that if during scroll operation the Tracking Counter (on Vidgen card) was allowed to shift then the SPACE code, instead of being inserted in the last line of the bottom memory would appear in line zero of that memory. The same would be true of the other two memories.

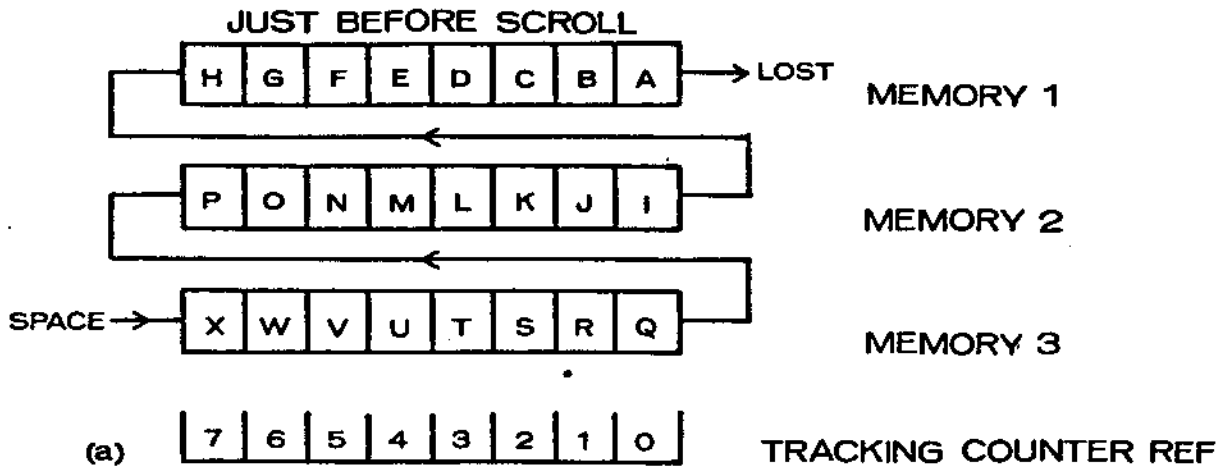
In order to correct this the Tracking Counter is disabled during scrolling. This is done on the VIDGEN card.

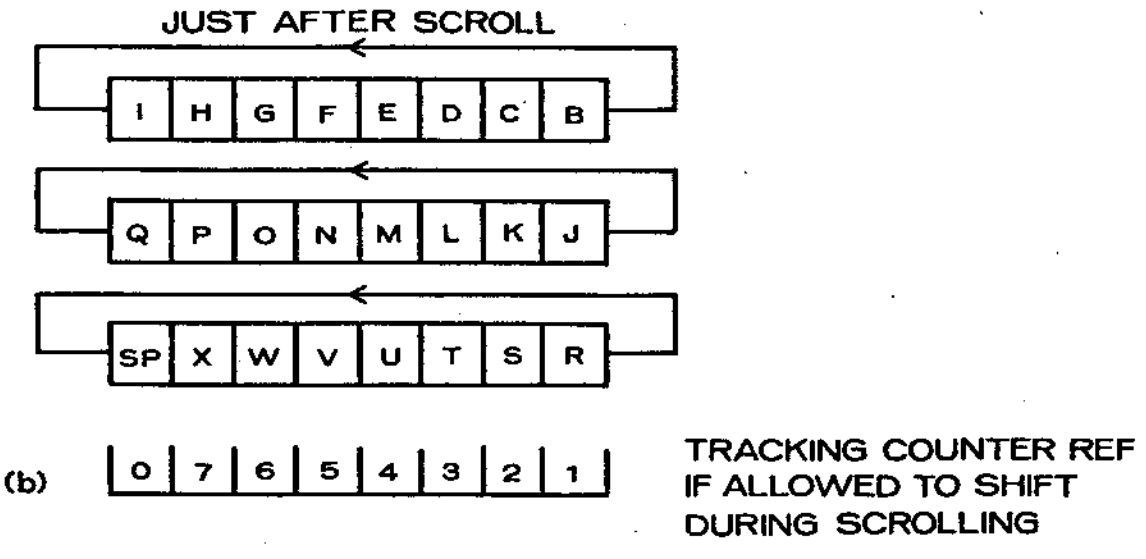
In general, if the SCROLL operation occurs any time but when the Tracking Counter is at count 0, SPACE code would be inserted in the wrong line and by the same token the wrong line would be lost. Elaborating a little more, note that the SCROLL operation should not be enabled until the Tracking Counter reaches a character count of zero, otherwise part of the lines will get mixed up. From this it is easy to appreciate the importance of having both the character and the line count of the Tracking Counter at zero before the information is shifted during scrolling.

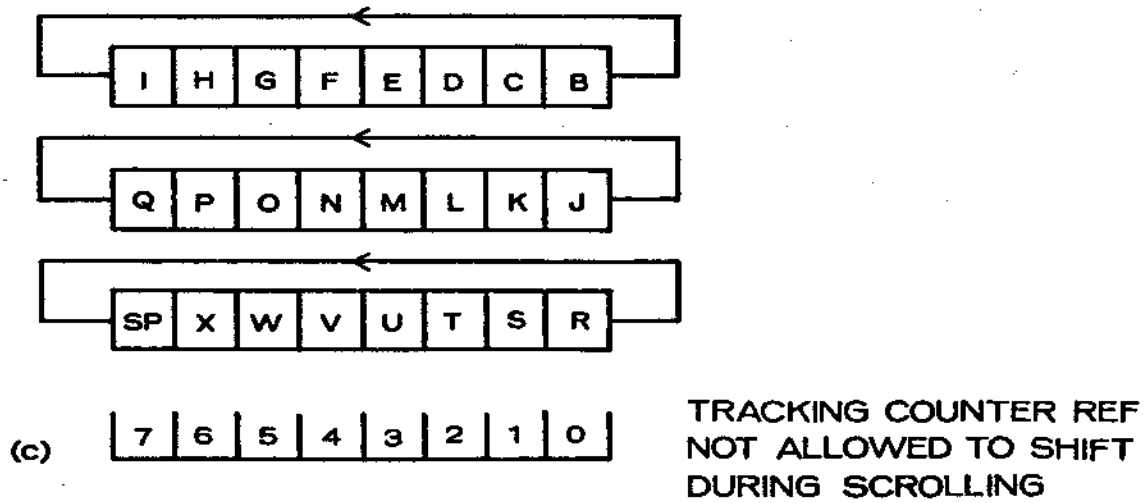
In practice, this is achieved as shown in Section C-2. When the right conditions are met for scrolling C5, 10 goes true and sets up F/F B5, 9. (Note that scrolling is prevented during screen erase.) ADDCOM going true indicates that the character sitting on the cursor (assumed to be in line 7 of bottom memory) is at the output of memory 3. This assures us that the Tracking Counter is somewhere on line 7 of the third memory. ADDCOM and the clock PH1B is, therefore, used to set up F/F B6, 5. To make sure that the Tracking Counter has crossed the end of the last line MCLEN* (Memory Clock Enable Not) is then used to set up F/F B6, 8. This causes SCROL* to go false and initiates the shift operation on the Memory Card.

SCROLLING OPERATION

Fig. 2·7







CR code on A6, 12 is used to cause prompt scrolling. This helps to speed up the scrolling operation necessary at high baud rates.

2.3.2.4 Cursor Control Logic

The cursor control logic [Section C-6, 7, 8] handles all the cursor movements, i.e., up, down, backward, forward and home position. One way to initiate these movements is by enabling any one of the 5 cursor function keys on the keyboard [Section C & D-8]. These signal levels (as their names imply) are converted to a strobe called FKYST (Function Key Strobe) by the F/F E4 [Section C-7]. Depressing the REPEAT key on the keyboard will generate a repetitive FKYST with a frequency of 30 Hz. FKYST is generated by the rising edge of control functions. It is then ANDED with the control functions to generate the respective cursor control strobes. [Section B & C-6]. These are used on the VIDGEN card to update the Address Register and ADDCOM.

CURFR* (Cursor Forward Not) goes low either for CURFOR (From the Keyboard) or for any one of the following four signals:

PFCLK*	(Protected Field Clock)
DLACH*	(Data Latch)
TABCL*	(Tab Clock)
HADRC*	(Horizontal Address Clock)

PFCLK runs at the speed of PH2B (1.6MHz) whenever the cursor is in a protected field, i.e., whenever ADDCOM and TAGM and FON are true.

DLACH* pulses low whenever a character has been entered into the memory.

TABCL* is generated by the horizontal tab circuit [Section A-5]. This circuit helps to place the cursor in specific character positions (e.g., multiples of 5) at a rate faster than possible if done manually. This helps to speed up data entry. On receipt of HT code (Horizontal tab), F/F D4, 5 is set on the trailing edge of its input strobe. This enables the NAND gate C6 causing TABCL* to run at the speed of PH2B whenever ADDCOM is true. The cursor continues to move forward till the F/F is reset by the signal TAB (goes true for character positions that are multiples of 5) when in Format OFF mode. If in Format ON mode the F/F is reset whenever the cursor goes through the entire page.

If during tabbing the cursor happens to enter a protected field, F/F D4 is promptly reset and the cursor is moved forward by PFCLK* to the first non protected position following the protected field.

HADRC* is generated by the Horizontal Address Circuit [Section A & B-3, 4, 5]. As its name implies, this circuit allows one to address the cursor in the horizontal direction upto a maximum of 166 positions. The special sequence needed to initiate the HADRC* is ESC, ENQ, X, Y, where X is the tens digit in decimal and Y is the unit digit in binary. For instance, to place the cursor in the 78th position, the sequence is ESC ENQ 7 8.

ESC ENQ cause B3, 3 to pulse high and the trailing edge of INST sets the F/F B4, 9. At the same time, BSY1* (Busy 1) goes low. When 7 is depressed LDY* (Load Y) goes false and the code for 7 presets the up/down decode counter J5 to count 7. At the same time, the trailing edge of INST associated with 7 sets up F/F B4, 5 while BSY1* is held low. Next when 8 is depressed F6, 8 strobes low and the code for 8 presets the counter J4 to a count of 8.

During both characters 7 and 8 BSY1* was held low and hence INSD was disabled. This prevents 7 and 8 from being loaded into the memory. When 8 is depressed B4, 6 goes true again and this sets up F/F B2, 9 [Section A-4]. The next PH2 sets up F/F B2, 5 and allows CLKD* and HADRC* to run. Counters J4 and J5 start to count down from the count of 78. HADRC* likewise runs at the speed of PH2B causing the cursor to move forward. When the counters are cleared to zero STP* (Stop) resets the F/F B2 and thus disables CLKD* and HADRC*. The cursor is now in the 78th character position.

Signals CURBK and CURUP [Section B-6] are self-explanatory. When HOME key is depressed signal HOME* is generated. This causes the cursor to go to the start of page (in Mess. and Page Modes) since the signals CHRZ* (Character Zero) and LNZR* (Line Zero) [Section F-3] go false. However, in CONV mode HOME is at the beginning of the last line. To achieve this we first make the cursor go home as if the system were in Mess. mode. The trailing edge of the HOME function strobe is then used to set up the F/F C2 [Section B-6] and after a delay of one clock time CURP is generated which kicks the cursor upwards by one. This makes the cursor come to rest in the last line.

2.3.2.5 Character Generation

Character generation on the 980 is obtained by using the horizontal scanning technique. A 5 x 7 dot matrix is used to generate all displayable characters. [Refer Figure 2.8]. The character field is an 8 dot wide by 9 scan line high "window". The character is generated within this field in dot positions 2 through 6 and scan lines 1 through 7. Characters R and S are shown in the Figure 2.8 (a) to illustrate the point.

It can be seen from the above figure that each character is generated from seven slices each of maximum 5-dot length. Each time a scan line is swept across, a 5-dot portion of the character is generated.

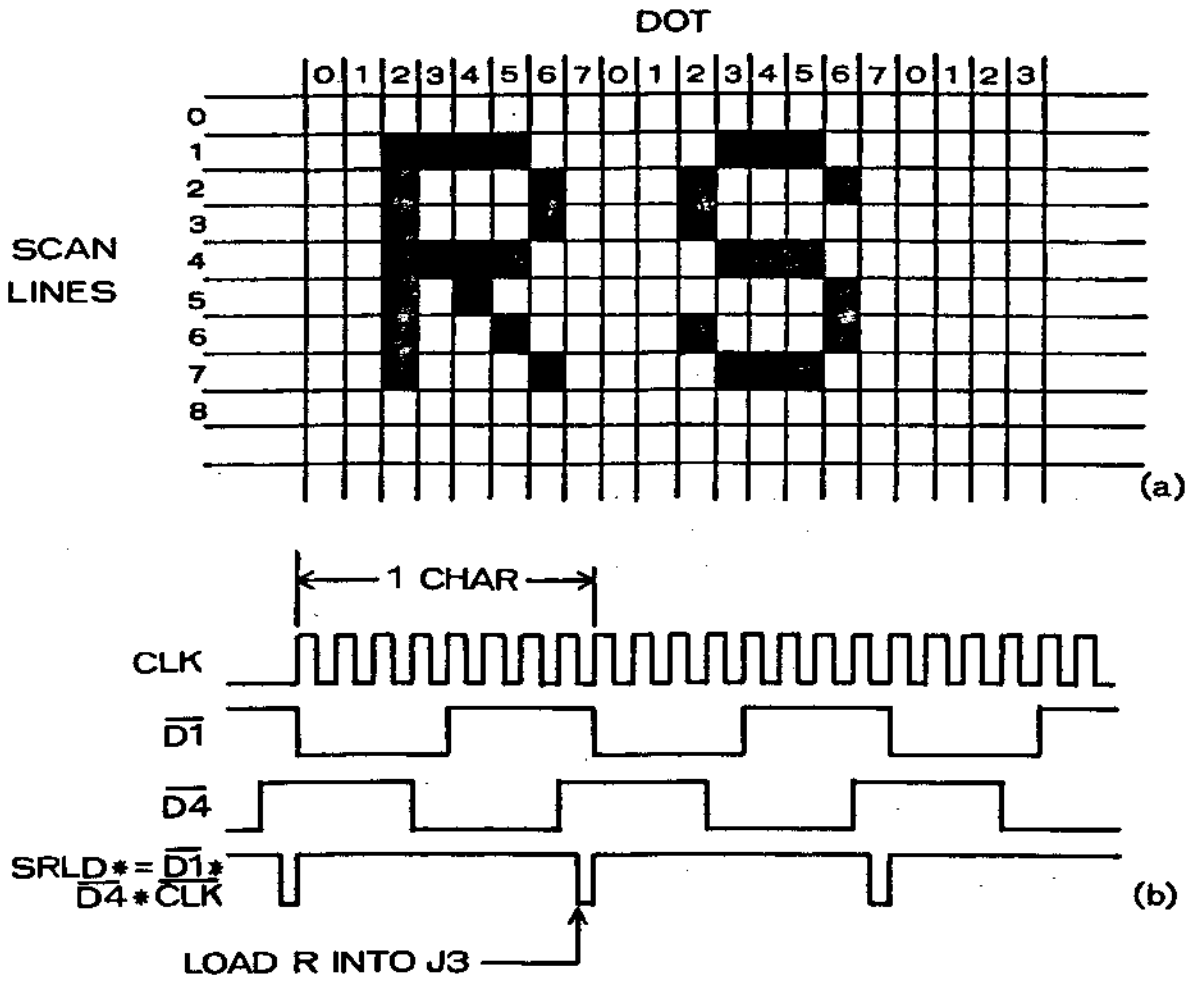
The data line consists of 81 such windows. 80 of these are used to display characters. The remaining 1 is used at the beginning and at the end (1/2 at each end) of the line to form a margin for the white page.

The seven 5-dot patterns that make up a single character are pre-coded and stored in a cell in a Read Only Memory (ROM). L1, L2 and L3 [Section B, C, D-1] form a bank of 3 ROMS. Each of the ROMS has a total capacity to store 64 characters, i.e., it has 64 cells each of which can accommodate seven 5-dot patterns. L1 is called the Upper Case ROM since it stores 64 upper case characters. Likewise L2 is the Lower Case ROM. L3 is a special ROM offered as an Option (64 character set). L1 and L2 together store the 128 character set on the ASCII CHART.

To obtain the 5-dot slice from the ROM, we have to go through two levels of addressing. In the first step, we have to address the cell where the particular character is located. In the second step, we have to address the correct 5-dot slice. It is easy to see that for proper character generation, the seven slices must be accessed in the right sequence. Each of the 64 cells is associated with a 6-bit address (0-63). This address is chosen the same as the ASCII code for the character. Refresh bits R1 through R6G [Section G. H-2] are used as address bits. For example, the ASCII code for an R is 010010. This indicates that cell #18 contains the seven 5-dot patterns that make up the character R.

CHARACTER GENERATION

Fig. 2·8



Each of these seven patterns is then addressed by 3 bits (0-7). The scan line counter S1, S2, S4 are used to address the correct word within the cell. For example, the third 5-dot word of R is 10001 and is addressed by S1 = 1, S2 = 1, S4 = 0 which is the state of the Scan Line Counter during the 3rd scan line. These 5-dot patterns are then available in parallel at the output of the ROMS.

Because of the nature of horizontal scanning technique, the 5-dot parallel output has to be first converted into a serial form before being applied to the video mixer. This conversion is done by J3 [Section A-1]. It is an 8-bit parallel-in-serial-out shift register. Of these only 5-bits are used the others being tied to +5 Volts. Refer to Figure 2.8 (b) for timing diagram. Note that ample time is provided for the 5-bit pattern to become stable on the output lines before being loaded into the shift register. SRLD* (Shift Register Load) is decoded on the Vidgen card, and electrically it is a logical AND function of SRSTR (Shift Register Strobe) [Section G-4] and DATA GT (Data Gate). SER (Serial) represents the serial output obtained from the shift register. It is then mixed on the Vidgen card and applied to the video amplifier. Figure 2.8 (c) shows the seven serial slices of the character R one for each scan line.

2.3.2.6 Miscellaneous

The Master Oscillator for the video is in [Section H-4 & 5]. It is a crystal Oscillator consisting of a common base amplifying stage Q3, driving an emitter follower, Q2, Q2 drives the crystal in the feedback path. The output is picked off the collector of Q2 to avoid disturbing the Oscillator circuit. This drives Q1 in switching mode. The D1 is a load on Q2 and also used to protect the base of Q1 from excessive negative voltage. The collector of Q1 drives a Schottky inverter H1 to provide the main clock signal, CLK. This is a 12.528 MHz (12.6 MHz for 50 Hz units) clock which provides the video bit shift rate.

The signal, CLK, drives the first stage of the timing chain J7 [Section E-4] J7 is a SN74175 used as a Ring Counter. This causes the register to sequentially fill with ones and then with zeros. An entire period takes eight clock pulses. E3 is used to insure that no illegal state, such as 1010 may exist for more than one period. All intra-character timing is derived from this counter which is also called the DOT counter. D4* (1.566 MHz or 639 n.sec.) represents one character time and drives the rest of the timing chain on the VIDGEN card.

The last thing on this card is the Read Trigger circuit [Section B-7 & 8]. This circuit provides READT* (Read Trigger*) which sets the READ F/F on the ASYNC/FE card. F/F D4 can be reset either by depressing XMIT key on the keyboard, or when the terminal receives the commands DC1 or SLOC (Start Local Print). It is set again by RTRST* (Read Trigger Reset*). Note that READT* cannot pulse low in CONV mode. Hence, no information can be read out of the memory in CONV mode.

Finally, the discrete components around the ROMS [Section F, G, H-2] are needed to supply the proper levels to the ROMS. Input levels must be between ground and +13V. The output drives must be sinked to a negative voltage and caught at +5V by the diodes D2-D6 [Section C-1] to operate properly with TTL circuits.

2.3.3 Memory — Schematic #135-091

The Memory Section of the 980 is made up of two parts - the Display Memory and the Refresh Memory.

2.3.3.1 Display Memory

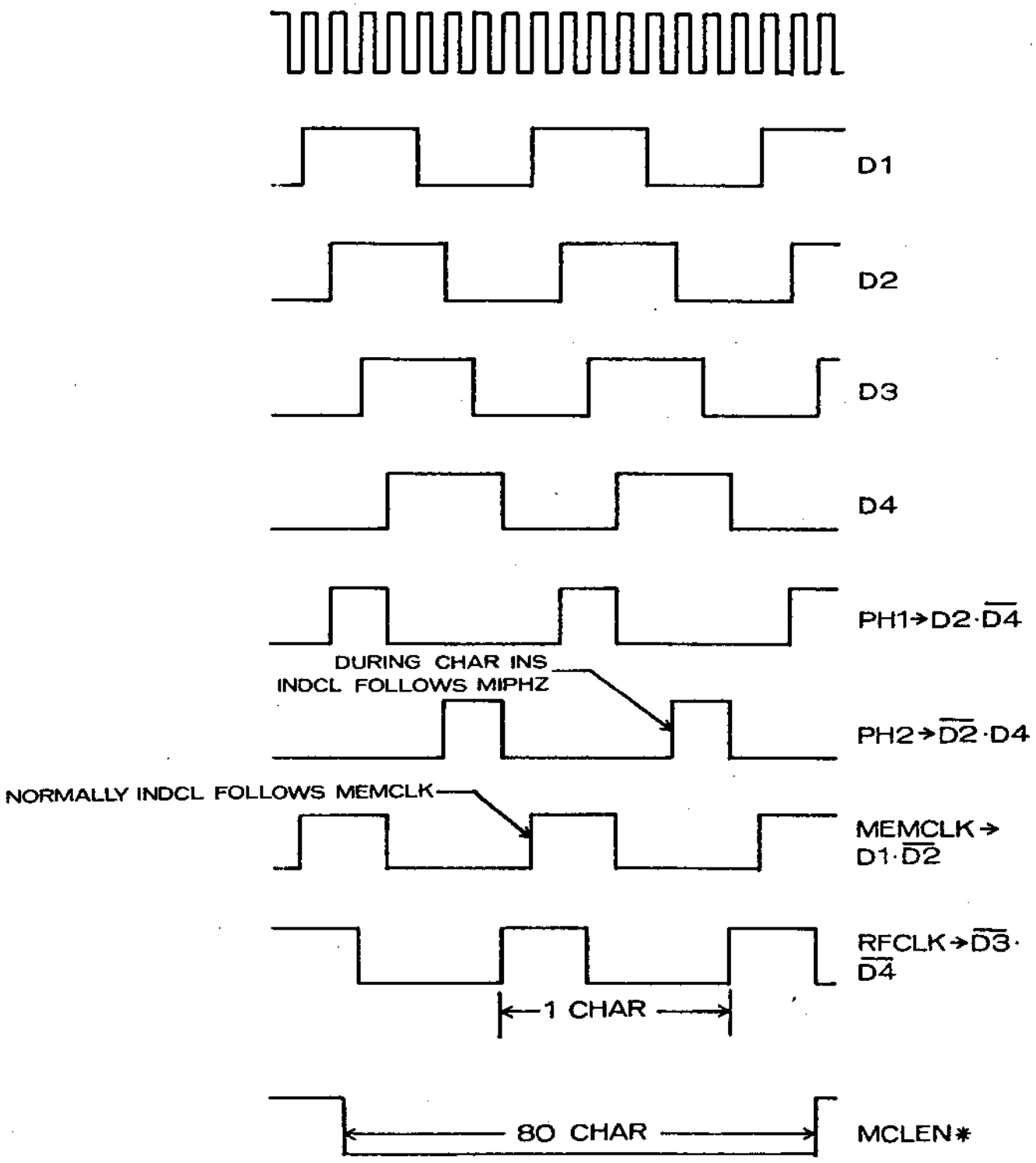
The Display Memory [Section A, B, C, D-3] organization is modular in nature. It consists of a group of shift registers running in parallel and recirculating their contents from the output back to the input. A single bit, of the 7-bits that form a character, is composed of a 128-bit static register in series with a 512-bit dynamic shift register 640-bits long. There are 7 such 640-bit long shift registers. In addition to this, there is another bit appended to characters. This bit is called the tag-bit, and it also has a 640-bit long shift register associated with it. This bank of 8 640-bit long shift registers form one module. It has a total storage capacity of 5120 bits (8x640) or 640 8-bit long characters. Since each line accommodates 80 characters, 8 such lines can be stored in a single memory module. Three such modules cover the entire screen of 24 lines or 1920 characters. Since the 3 modules are identical only one of them will be described in detail.

Shift registers K6, H6, L7, K7, J7, H7 [Section C, D-3] make up one module. K6 and H6 are quad 128-bit static shift registers and L7, K7, J7 and H7 are dual 512-bit dynamic shift registers. The contents of these registers are shifted at a rate of 1.566 MHz or 639 nanosec. which is one character time. The clocks MEMCL1, M1PH1 and M1PH2 are AND functions of MCLEN* (Memory Clock Enable*) and PH1 and Ph2 (Refer Timing Diagram for clarity) [Figure 2.9]. L6 and J6 are quad buffers whose function will be explained shortly. The outputs of L6 and J6 are returned again to the input of the registers via the multiplexers L5, K5, J5 and H5.

This enables us to recirculate the contents and run in parallel. Hence at any time an entire character appears at the output of the shift registers. The 4:1 multiplexers (only 3 inputs are used) allow us to enter data into the memory or to scroll data. Depending on the states of the address lines of the multiplexer (pins 2 & 14) one of the three inputs is enabled. Normally both the lines are low. This enables input pin 6 and hence the memory contents are recirculated. However, when a character has to be entered into the memory, A1 [Section D-4] momentarily goes true. This state of the address lines allows the output to follow input pin 5. Hence for one character time the recirculation path is broken and the character of interest is inserted into the memory. Still another manipulation of the memory occurs during the Scroll operation.

TIMING DIAGRAM

Fig. 2-9



During scrolling, we have to stretch out the entire memory as one long memory. This is achieved as follows. During scroll SCROL* [Section G-4] goes low and BMEMI goes high. The address on the address lines is now 1.0. This address enables the third input (pin 4) of the multiplexer. But this input is the output of the corresponding bit from the second module. This suggests that all the bits of the 2nd module get tied to the corresponding bits of the 1st module. Likewise all the bits of the 3rd module get tied to their corresponding bits in the 2nd module. Hence, during scrolling all the three modules are cascaded to form one memory of 1920 characters. Also note that BMEMI goes true when we do Line Insert/Delete - ID12* [Section C-4]. Thus the 3 modules are tied together during line Insert/Delete. Also SP3 (SPACE 3) goes true and causes SPACE code to be inserted during line delete operation.

The quad D-flip-flops 74175's are used during character insert/delete operation. These are clocked by INDCL 1,2,3. (Insert/Delete Clock). Normally, INDCL1 follows MEMCL1. However, during character insert operation INDCL1 follows M1PH2. From the timing diagram we note that the rising edge of these two signals is almost one character time apart. This has the affect of making the shift register 1-bit longer, i.e., making it 641-bits long. The character to be inserted now has the place available in the memory. Without overwriting any characters that may have been present. Once the character is inserted INDCL1 follows MEMCL1 and the memory returns to its original form. During character delete DSP1, 2,3* (Delete Space 1,2,3*) goes false and resets the 74175's. This introduces a SPACE code to appear at the output of the memory.

C3, D3 and J3 [Section A, B-4] are MOS clock drivers for the memory. They convert the TTL level clocks and swing it between +5V and -12V which are MOS logic levels.

2.3.3.2 Refresh Memory

The Refresh Memory consists of two quad shift registers. Each of these 8 registers is a 100-bit static shift register. L3 and M3 [Section C, D-2] are the quad 100-bit registers. The entire refresh memory has a capacity of holding 100, 8-bit characters at any one time. However, only 80 of these positions are used to store the 80 characters of a logic line.

Consider that all the 80 characters of a particular line have been transferred into the registers. Each of the 8-bits of the characters are recirculated within the register at a shift rate provided by RFCLK (Refresh Clock). From the timing diagram we see that RFCLK occurs once every character time. Hence, the outputs of the shift registers represent a character at any time. This information is sent to the character generator on the CONTROL card. Once the entire line of 80 characters has been generated, the contents of the refresh memory has to be updated. This happens after every 9th scan line at the end of every logic line. At this time S8* (Scan line 8*) goes false causing pin 1 on H3 and L3 to go low. This disables the recirculate path and enables the output to follow the input. As soon as the next logic line is filled into the memory S8* goes true again and the recirculation process begins.

2.3.3.3 Compression Logic

This logic [Section B-2] incorporates the "Look Ahead" feature in the terminal. During the READ operation, this logic "looks ahead" at the current logic line, and if the remainder of the line is blank, (i.e., filled with SPACE codes), it terminates the line. This name "compression" logic suggests that if the number of characters on a particular line is less than 80, the circuit compresses the normal line to the length of the number of characters on the line, and treats the compressed line as a normal line of 80 character length. It, therefore, immediately terminates the line, as it would do a normal line, by sending proper codes. This function of compressing the line prevents trailing blanks (which has no information value) from being transmitted and thus greatly increases throughput.

Referring to the circuit [Section B-2] we see that the SPACE code in the memory is decoded at D2, 6. Normally D2, 6 is true causing F/F F2 to be clamped reset. During READ (A1, 4 is true) if no SPACE code is detected F2 is still held reset. However, if a SPACE code is detected at the output of the memory A1, 6 goes true and the trailing edge of DLACH* sets the F/F F2. If while scanning the current line no further SPACE code is detected, A1, 6 goes false and clamps F2. But if the remainder of the line is filled with blanks F2 is held set till MEOLN* (Memory End of Line*) sets up H2, 5. One character later PH2 causes COMPR* (Compress*) to go false. Normally jumper J3 is in activating CRSND* (Carriage Return Send*) and the line is terminated. Note that a protected SPACE code is treated as information and does not enable COMPR*.

2.3.3.4 Output Multiplexer

During the READ operation, the information in the memory has to be put on the output buss. This is achieved through the output multiplexer. [Section B, C-2] C4, D4, E4 and F4 are dual 4:1 multiplexers. Depending on where the cursor is, the output bits B1M through TAGM follow the output of the corresponding memory module. The selection of the correct memory module is done via the level of signal A and B on the address lines (pins 2 and 14). This information is output on the data buss via 2 tri-state quad buffers E3 and F3. The information is clocked on the trailing edge of DLACH*. Normally MDEN* (Memory Data Enable*) is low thus keeping the memory tied to the output buss. However, when special codes like CR, LF, SI, . . . etc., have to be inserted in the data stream MDEN* pulses true and momentarily disables the memory from the buss.

2.3.3.5 Miscellaneous

In the 980 we have available to us a feature that permits us to store control characters in the memory. METX* (Memory ETX*) [Section A-2] is a decode of ETX code stored in the memory. It is used on the ASYNC/FE card to cause short transmission.

B1HC through B7HC [Section B, C-1] are buffered output bits that go to the parallel printer port.

MEMCLG (Memory Clock Gates) [Section A-2] is the clock to be used instead of MEMCL1, 2, 3 and INDCL1, 2, 3 on the 920. Likewise PH1LR* and PH2LR* [Section D-4] are clocks to be used on the 920 instead of M1PH1* M2PH1*, M3PH1* and M1PH2*, M2PH2* and MBPH2* respectively.

The two signals DATTRY (Data Terminal Ready) and LBIAS (Loop Bias) [Section A-2] go to the output connector. DATTRY is needed by a modem when EIA levels are used. DATTRY and LBIAS may be used in a current loop connection to supply the necessary current.

2.3.4 Video Generator - Schematic #135-089

As its name implies, this P.C. Board contains a large portion of the overall timing signals.

2.3.4.1 Clocking and Timing Chain

The heart of the video generator is a 12.528 MHz crystal oscillator. This was discussed on the CONTROL Card. The Master Clock, CLK, is divided by 8 on the CONTROL card, by the Dot Counter. This produces the signal D4*. D4* has a 639 nanosecond period and this represents one character time. D4* is further counted down on the VIDGEN card by the rest of the timing chain.

The timing chain is in Section D-3 & 4. D4* represents one character time. This signal is divided by 100 to give the video scan line rate. K6 and J7 are quad D-flip-flops K6 and J7 form a pair of 5 bit flip-flops, and are so connected as to divide D4* by 10. The second divide by 10 counter (J6 & J7) produces the signal C50* that is 100 times slower than D4*. C50* represents one video scan line. It has a repetition rate of 15.66 KHz and a time period of 63.9 microsecond. The various outputs of the divide by 100 counter are used to obtain horizontal blanking and horizontal sync timings.

C50* is applied to the input of J2, a synchronous decade counter. This chip is wired such that the output S8 is inverted and fed back to the synchronous clear input on pin 1. When S8 goes high, the next clock signal at pin 2 will clear the chip to all zeros resulting in a divide by 9 function. This is the Scan Line Counter and its outputs S1, S2, S4 and S8 are used for timing within one data line of characters.

Finally the output S8 drives a binary ripple-through counter D6 together with a couple of J-K flip-flops wired in toggle mode. This is the Data Line Counter. For 60 Hz devices it counts 29 data lines (261 scan lines) and then is reset to zero. For 50 Hz the count is 35 data lines (315 scan lines). The crystal frequencies of 12.528 MHz and 12.6 MHz for 60 Hz and 50 Hz devices respectively were picked to provide a 60 Hz or 50 Hz refresh rate, while keeping the number of scan lines an integral of 9.

The outputs of the Data Line Counter are used to generate vertical blank, vertical drive and memory display select timings.

The signal RST1 is the reset signal for the Data Line Counter. It is generated by the cross-coupled latch A6 [Section D-3]. The latch is set by the four input NAND gate C6, 8. RST1 goes true when the Data Line Counter reaches a count of 29 (or 35 for 50 Hz devices) and goes false again half a character count later when D4* goes true. This resets the latch.

2.3.4.2 Horizontal Timing

2.3.4.2.1 Horizontal Blank

The horizontal blank signal determines the size of the white page on the screen in the horizontal direction. Half a character space is left at each end of the 80 character line to form a border resulting in a 19 character time blank signal. HBLNK (Horizontal Blank) is generated by the J-K flip-flop L3 [Section C-1]. For a character decode of 97, L6, 6 goes true and sets L3, 13. HBLNK resets at the end of count 15 since at this time SHFTGT (Shift Gate) goes true. This results in a blank of 19 characters. Refer to the timing diagram for clarity.

2.3.4.2.2 Horizontal Drive

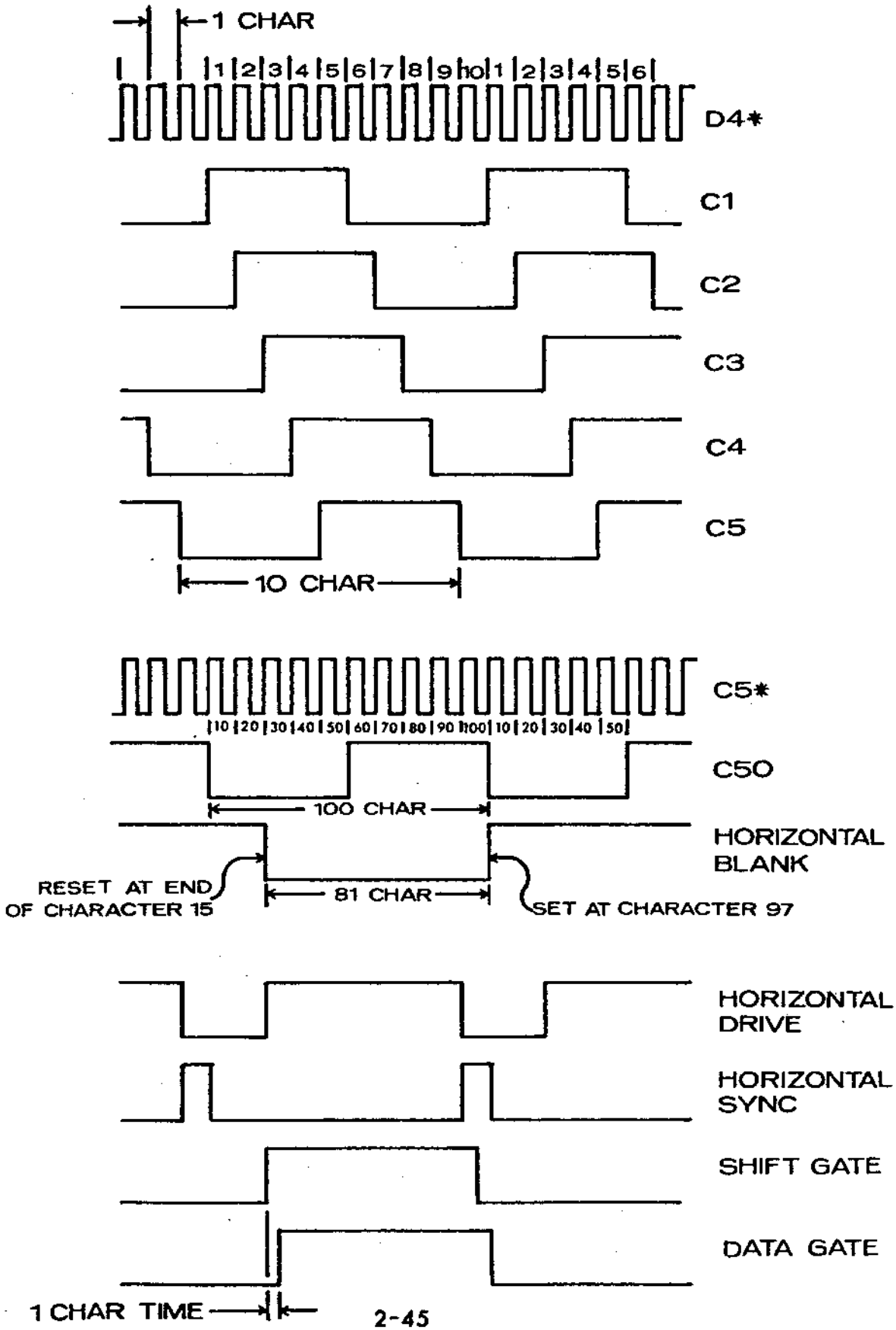
HDRIVE (Horizontal Drive) [Section C-1] is used by the internal monitor to develop the horizontal sweep. It begins at character position 90 and ends at character position 20. [Refer to Figure 2.11].

2.3.4.2.3 Horizontal Sync

This signal is needed by an external monitor in order to synchronize its horizontal oscillator [Figure 2.10]. It is contained within the combined sync circuit [Section C-1]. CMBSN* (Combined Sync*) goes false when C10 and C50 are both high, (i.e., at count 90) and goes true again when C10 goes false (at count 100). This results in a horizontal sync pulse lasting for 10 character times.

HORIZONTAL TIMING

Fig. 2-10



2.3.4.2.4 Data Gate

DATAGT is a signal lasting for 80 characters. This period is the time during which the Display Buffer Memory shifts. SHFTGT [Section C-1] is also 80 characters long but occurs one character earlier than DATAGT. SHFTGT is used to begin the shifting and also to gate one line of data from the Display Buffer to the one line Refresh Memory. SHFTGT and DATAGT are generated by the J-K flip-flops K4 [Section C-1]. K4 is set at a count of 15 and reset at a count of 95. DATAGT is delayed from SHFTGT by one character count. DATAGT goes true at 16 and goes false at count 96. The falling edge of D4 is used to insure no false clocking. Refer to the timing diagram for clarity.

2.3.4.3 Vertical Timing [Refer to Figure 2.11]

2.3.4.3.1 Vertical Blank

The vertical blank signal, VBLNK, [Section D-1] is generated by a cross-coupled latch A6, 8. This signal determines the top and bottom borders of the white page. To allow for one scan line under the cursor in the bottom line, one scan line is added to the page after the last data line. To keep the page symmetrical, a scan line is also added to the top of the page.

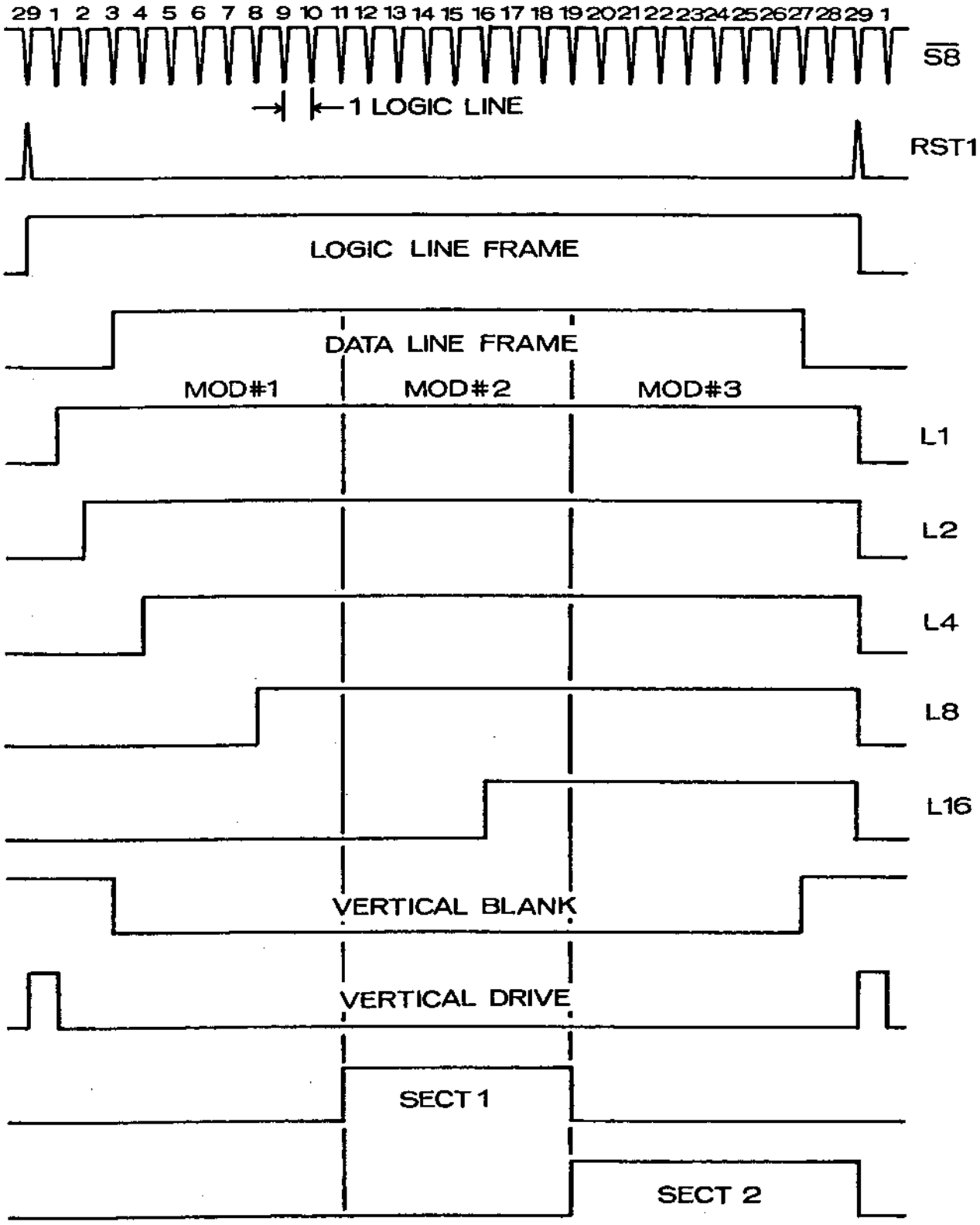
VBLNK goes true when SL1, (Scan Line 1) of logic line 28 goes true and it goes false at the beginning of logic line 4. Hence the 24 data lines of the screen lie between logic lines 4 through 27. This is for 60 Hz devices. For 50 Hz devices VBLNK goes true with SL1 of logic line 32 and resets with logic line 8.

2.3.4.3.2 Vertical Drive

VDRIVE* [Section D-1] is used by the internal monitor, and as a part of combined sync by the external monitor, to initiate the vertical fly-back. It starts with the reset pulse RST1 and ends when L1 returns true 9 scan lines later.

VERTICAL TIMING

Fig. 2-11



2.3.4.3.3 Memory Module Selection

Since the three modules of the Display Buffer are multiplexed at their outputs, the proper section must be selected for input to the one line Refresh Memory. The signals SECT1 and SECT2 control this gating and are generated by the F/F pair F6 [Section D-2]. When both SECT1 and SECT2 are low, the 1st module is selected. SECT1 true selects the 2nd module and SECT2 true selects the 3rd module.

VDRV* is used to set both F/F to zero which selects Display Buffer Module 1. After 8 data lines have been displayed, i.e., the line counter counts 11, E6, 8 goes true and sets F6, 9. This selects the 2nd module. After the next 8 data lines are displayed, i.e., the line count is now 19, E6, 8 again pulses high. This resets F6, 9 and sets F6, 5, and the 3rd module is now selected. For 50 Hz devices, these decodes are all increased by 4 logic lines to center the display.

Refer to vertical timing diagram in Figure 2.12 for further clarification.

2.3.4.4 Address 8 Tracking Registers

We have seen that the contents of the memory modules are shifted continuously at a shift rate of 1.566 MHz. Whenever a character has to be inserted in the shift registers, the recirculation path is momentarily broken and the character is "written" into the memory. To enable us to write the character in the correct memory location, we must be provided with the correct address of that location. Also to obtain the correct address, the memory as it shifts must be tracked continuously. Both these functions are performed by the Address and Tracking registers [Section C, D-2,3,4].

The Memory Address Register holds the address of the next Display Memory location to be accessed. It consists of chips B2, A2, C1 and F/F pair D5. B2 is a synchronous up/down decimal counter. This drives A2 which is a four-stage synchronous up/down binary counter. The two in tandem count from 0 to 79 (only the first 3 stages of A2 are used) or one 80 character line.

The count of B2 and A2 together indicates the horizontal position of the character. The up and down inputs to B2 are CURFR* (Cursor Forward*) and CURBK (Cursor Back) respectively. These lines are used to update the contents of these registers as the cursor is moved across the screen. The outputs CA0 through CA6 are decoded to obtain signals like TAB, CH75 and ADV.

The next counter, C1, is also a synchronous up/down binary counter. It is used to indicate which of the eight lines in one memory module contains the character of interest. Finally the F/F pair D5 is wired to obtain a count of 3. It indicates in which of the three memory modules the current line of interest lies. B2 and A2 form the character counter while C1 and D5 form the line counter. The line counter can be preset to any count by the five lower bits of a character TIN1 through TIN5. This is used for vertical tabbing at which time signal LDLNE* (Load Line*) pulses low and loads the present count into the counter. The outputs of C1 are decoded to form signals LSTLNE (Last Line), A and B. When the Cursor is in the top module A and B are both zero. In the middle module A=1, B=0 and in the bottom module A=0, B=1. Signal A+B is high in module 1.

The Tracking Register is counted by the shift pulse PH2 of the Display Memory and indicates which location in any given module is available for access. Its output is stable for one character time and increments at 1.566 MHz rate. This register is constructed in the same way as the Address Register. The first stage is a decade counter B4, followed by a binary counter A4. Since the three memory modules are shifting in parallel, only eight lines of 80 characters need be tracked. The last stage of A4 and the F/F pair D4 make up the 0-7 counter for the line count. B4 and A4 make up the character counter. B4 is shifted by CCLK* (Character Clock*). CCLK* is enabled only when MCLEN (Memory Clock Enable) is true, i.e., when the memories are not pausing for line end or memory synchronization. Also note that, as per the discussion for scrolling the Tracking Counter is not allowed to shift during scroll operation. The outputs of the Tracking Register are decoded to obtain the signals MEOLN* (Memory End of Line*) which indicates the end of 80 character line, and TR7* (Track 7*) which indicates the end of a memory module.

The three chips B3, A3 and C2 are dual four-bit comparators. These three comparators are used to generate a signal that indicates when the memories are at the location held by the address counter. This is done by comparing the contents of the Address Register with that of the Tracking Register. B3 and A3 compare the character portion and generate a signal named CHCOM (Character Compare). Likewise C2 generates the signal LNCOM (Line Compare). The two signals are then ANDED by E3 [Section C-3] to generate ADDCOM (Address Compare). When ADDCOM is true it indicates that the character sitting atop the cursor is at the output of the Display Memory Buffer.

2.3.4.5 Memory to Video Synchronization

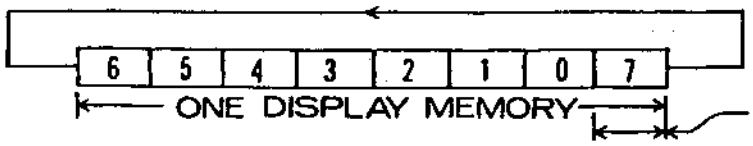
In order to explain why synchronization is necessary, a discussion of the method used to transfer data from the Display Memory to the one-line Refresh Memory will be given.

As mentioned before, the Display Buffer Memory is divided into 3 modules of 640 characters each. These modules are shifting together with their inputs and outputs multiplexed for access and display. At the top of the white page the first memory module must be ready to transfer the first line of 80 characters to the Refresh Memory. This indexes the memory by one line of 80 characters. During the next eight scan lines the Display Memory shifts for 8 more lines. It is then back to the same relative position as when it completed the transfer of the first line to the Refresh. The first line was transferred when the Scan Line Counter J2 was at count of 8. After the bottom scan of the characters the Display Memory is ready to shift the next line of characters to the Refresh Memory. This process continues until all 8 lines have been transferred. Now the Display switches to the second module for 8 more lines of characters and then to the third module for the bottom 8 lines.

Referring to Figure 2.12, the last line transfers during scan line 8 of logic line #26. (Or data line #23). The memories continue to shift as if they were loading for two more lines. At the end of these two lines the video begins the vertical flyback.

MEMORY SYNCHRONIZATION

Fig. 2-12



MEMORY POSITION AT BEGINNING OF SCAN LINE								SCAN LINE	DATA LINE	
7	6	5	4	3	2	1	0	0		
0	7	6	5	4	3	2	1	1		
1	0	7	6	5	4	3	2	2		
2	1	0	7	6	5	4	3	3		
3	2	1	0	7	6	5	4	4	27	LAST DATA LINE DISPLAY
4	3	2	1	0	7	6	5	5		
5	4	3	2	1	0	7	6	6		
6	5	4	3	2	1	0	7	7		
7	6	5	4	3	2	1	0	8		
0	7	6	5	4	3	2	1	0		VERTICAL BLANK BEGINS
1	0	7	6	5	4	3	2	1		
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		
4	3	2	1	0	7	6	5	4	28	
5	4	3	2	1	0	7	6	5		
6	5	4	3	2	1	0	7	6		
7	6	5	4	3	2	1	0	7		
0	7	6	5	4	3	2	1	8		RST1 PULSES LOW
1	0	7	6	5	4	3	2	0		
2	1	0	7	6	5	4	3	1		PAUSE IN SHIFTING
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		PAUSE IN SHIFTING
3	2	1	0	7	6	5	4	4	0	MEMORIES IN SYN
4	3	2	1	0	7	6	5	5		
5	4	3	2	1	0	7	6	6		
6	5	4	3	2	1	0	7	7		
7	6	5	4	3	2	1	0	8		PAUSE IN SHIFTING
7	6	5	4	3	2	1	0	0	1	
0	7	6	5	4	3	2	1	1		PAUSE DURING SCAN LINE 8 OF DATA LINES 1&2
1	0	7	6	5	4					
2	1	0	7							
3								6		
				2	1	0	7	7	3	VERT BLNK END
		5	4	3	2	1	0	8		FIRST LINE OF DISPLAY SHIFTED INTO REFRESH
0	7	6	5	4	3	2	1	0		
1	0	7	6	5	4	3	2	1		
2	1	0	7	6	5	4	3	2		
3	2	1	0	7	6	5	4	3		
4	3	2	1	0	7	6	5	4	4	
5	4	3	2	1	0	7	6	5		
6	5	4	3	2	1	0	7	6		
7	6	5	4	5	2	1	0	7		
0	7	6	5	6	5	2	1	8		SECOND LINE LOADED

BALANCE OF 1, 2 AND START OF 3

When the video generator is ready to display the first line on the screen, line 0 of memory module 1 must be ready to transfer to the Refresh Memory. In order to achieve this the Display Memories must be in synchronism with the Scan Line Counter, i.e., line 0, in the Display Memory must shift through the output during scan line 0, memory line 1 with scan line 1 and so on, in order for memory line 0 to be ready to shift into the Refresh Memory during scan line 8.

When RST1 pulses, the synchronization circuit [Section B-4] begins to lock the memory to the video generator. This is done by causing the memories to pause every other scan line until memory line 0 is shifting during scan line 0. The memories are always shifting in groups of 80 shifts in sync with the video scan line so only the line portion must be brought back into lock.

When the Scan Line Counter outputs S1, S2, S4 and S8 and the Tracking Register outputs TR1, TR2 and TR4 are the same, the memory is in sync with the video. By not allowing the memories to shift during scan line 8, the memories will remain in sync until the first line is needed, at which time the memories will shift during scan line 8 again.

Referring to the schematic, the signal RST1* pulses low at the vertical flyback time setting the F/F E5, 5 true. [Section B-4] One effect of this is to enable NAND gate H7, 12 allowing S8 when true to go high. SHFTGT goes true at the start of the 80 character shift group allowing #3, 8 to go low. During synchronization H6, 10 is enabled. Also the comparator H4, causes inverter F2, 12 to be true when S1, S2, S4 are not the same as TR1, TR2 and TR4. This causes H3, 11 to go low when S1 is true. The result is that the memory clocks are disabled during the time S1 is true until a true comparison is achieved. It takes two pauses to sync back because the memories were out of sync by 2 lines when RST1* pulsed low. When synchronization occurs H4 causes F2, F12 to be low which disables H3, 11 allowing H3, 10 to go true every scan line for 80 shifts. From this point on the memories pause only during scan line 8 to maintain sync. Vertical blank goes true at the start of scan line 8 in Logic line 3. This signal SYNCL (Sync Clock) is used to set E5, 5 low allowing the Display Memories to shift during Scan line 8.

2.3.4.6 Fast and Slow Blink Circuits

All protected information in format off mode blinks at a 4Hz rate. This is the fast blink. Besides this all information enclosed between the symbols { } blinks at 2Hz rate. This is the slow blink.

The fast blink circuit [Section B-1] generates a signal FSBLNK (Fast Blink). Whenever the refresh memory outputs a tagged character, L4, 9 is set. At this time if DATAGT is also true FSBLNK goes true and the tagged character blinks at 4Hz rate. Note that FSBLNK is disabled when the tagged characters are put into protected field mode, i.e., when FON is true. The protected characters do not blink but appear at half intensity since FON going true enables K3, 9 and sets signal, HALF, true. Also FSBLNK is disabled in graphics mode. Hence graphs cannot blink.

The slow blink circuit is in Section C-1. When the Refresh Memory puts out the code for the symbol { , L2, 6 goes true and sets L3, 9 true. One character later L4, 5 goes true and the signal SBLNK (Slow Blink) activates the slow blink rate of 2Hz. L3, 9 can be reset in two ways. When the output of the Refresh Memory is the symbol } , then L2, 8 goes true and resets L3, 9. The other way L3, 9 can be reset by crossing character position 15. (Note that the page margin starts from actual character position 16). Thus all information enclosed between the symbols { } or between { and the end of the line blinks at 2Hz rate.

2.3.4.7 Cursor Generation Circuit

A cursor is an underscore over which a character sits. It appears in scan line 8. The cursor is generated as follows: When ADDCOM is true during scan line 8 it means that the character of interest is being loaded into the Refresh Memory. The next time S8 (Scan line 8) goes true the cursor must be generated in order to place it under this character. The cursor generation circuit is in Section B2 and 3. CUREN (Cursor Enable) is true whenever the Display Select Signals SECT1 AND SECT2 are the same as signals A and B. When ADDCOM goes true during S8 it sets L7, 5 true, and the trailing edge of S8* sets 1&, 9 true. The next time S8 goes true with CHCOM, E5, 9 goes true after one character delay, and generates the cursor signal, CURS (Cursor). CURS is mixed in the mixer, and inverts the background level causing the underline mark.

2.3.4.8 Video Amplifier and Mixer

The video amplifier and mixer is in Section A, B-3, 4. Video presentation is obtained by controlling the output of the transistor Q1. If the collector of Q1 is high it generates a white dot on the screen and if it is low it generates a black dot. The collector of Q1 swings between 10V 5.2V and GND. (D3 is a 10V Zener, R15, R17, R6 divide the 10V down to 5.2V when Q1 is off. Q3 is an emitter follower that produces VIDINT (Video Internal) that drives the internal monitor. VIDINT is resistively mixed with CMBSN* (Combined Sync) to generate VIDEXT (Video External) that goes out to BNC connector in the rear panel.

Normally Q1 is in cut off mode causing its collector to be at +10V + 5.2V. Whenever F1, 4 or F1, 5 goes low, F1, 6 goes true. This causes Q1 to switch to the ON state, and the collector of Q1 is pulled to ground. Hence any serial video (SER) on F1, 4 or HBLNK and VBLNK on F1, 5 causes the screen to be dark. We, therefore, get black characters on a white screen. To present protected data in half intensity Q1 is OFF (since F1, 1 is disabled by the signal HALF), and F1, 8 goes high. Q2 turns ON and its collector is pulled to ground. This acts as a voltage divider causing the collector of Q1 to be at

$$10 \text{ (volts)} \times \frac{R17}{R_{15} + R_{17}} = 4 \text{ Volts}$$

This makes the protected field appear at half intensity.

2.3.4.9 1 of 3 ROM Enable Circuit

This circuit is in Section B-1. It generates the signals ROM1*, ROM2* to enable the respective ROMS. For ASCII chart columns 2,3,4 and 5, which contain the upper case characters together with numbers and symbols, R6 & 7 are never equal. Hence H1, 8 is low. This disables J1, 1 or ROM2 and enables ROM1 by making the signal, ROM1*, low. However, if the character is from columns 0,1, 6 & 7, then R6 and R7 are same. H1, 11 is low and H1, 8 is true. This causes ROM2* to be low and ROM1* to be high. For lower case characters the lower case ROM is enabled. ROM3 is a special character set ROM. It is enabled when the signal, Kanen, [Section C-1] is set true by the symbol and reset by the symbol . This special ROM allows the user to have 64 more characters or symbols displayed inplace of the slow blink feature.

2.3.4.10 Miscellaneous

Chips A1 and B1 [Section a, B-2] are tri-state quad buffers. They are used to output the LNADR (Line Address) and the CHADR (Character Address), of the current cursor position, on the data buss.

L1 and K1 are quad latches for the refresh bits, RR1 through RRT from the Refresh Memory. The outputs R1 through R5 & R6G are fed to the ROMS for character generation.

SRLD* (Shift Register Load*) [Section C-1] is a strobe to the video shift register on the Control card. Note that Control codes stored in the memory can be displayed only if the CONTROL key on the keyboard is depressed.

CBKEN (Cursor Back Enable) [Section C-3] is a signal that enables the cursor to be moved backwards. When the cursor comes to the zero character position on any line, it is decoded by the four-input NAND gate A5. In this position, all the inputs are high causing A5, 8 to be low. This prevents the cursor from going back any more.

The switches in Section B-4 allow us to select various video presentations, such as black characters on a white background, white characters on a black background and so on.

J3 [Section D-2] is a BCD-to-Decimal decoder. Its outputs generate signals, SLO-2 and SL3-5. These are used on the OPTION card to create picture elements for graphs.

2.3.5 Option - Schematic #135-092

The Option Card contains all the options offered on the 980. These options are listed below.

2.3.5.1 Character Insert/Delete

The character insert/delete logic enables one to insert or to delete a character at any memory location. Whenever a character is inserted or deleted, the change only affects the characters, to the right of the cursor, in that particular line. To be more specific, the change affects only that variable field in which the character is inserted or deleted.

Character insert logic is in Section A, B-4. To initialize the character insert function, Insert key on the keyboard is depressed. This holds the signal INSKEY [Section B-4] true. Now the character to be inserted is keyed in. The rising edge of the INSD sets the F/F H2, 5. When ADDCOM goes true it indicates that the character sitting over the cursor is at the output of the Display Memory. The rising edge of ADCOMG is used to set H2, 9 true. The signal, CINSL* (Character Insert Load*) goes false causing the strobe line on chip E-3, a dual 2:4 demultiplexer [Section A-4] to go low. Depending on the address lines (pins 3 and 13) drops low. This has the effect of shifting the location in time of the clock INDCL (Insert/Delete Clock). Normally INDCL follows MEMCLK. However, during character insert INDCL follows PH2 causing the memory to be one character longer. This clock is then used on the Memory card to insert the character as explained earlier. When H2, 9 goes true it removes the clamp from the F/F J3, 13. MEOLN* (Memory End of Line*) pulsed low when the video crosses the page boundary (after a maximum period of 63.9 microsecond) and resets the entire circuit. CINSL* returns true causing the output of E3 to go high. INDCL once again follows MEMCLK and the memories return to their original form. If a second character has to be inserted, the whole process repeats itself. If we have a protected field somewhere to the right of the cursor, then the character insert operation is not allowed to proceed till MEOLN* pulses low. Instead the operation is shut down earlier as explained below. M1TP, M2TP and M3TP are tagged bits, associated with tagged characters, in memory modules 1,2, & 3 respectively.

In protected field mode FON is true, thus enabling the gate H6. When the first tag bit to the right of the cursor is scanned, B12, 12 goes true and sets H6, 12 true. The rising edge of H6, 12 is then used to shut down the character insert operation. By so doing, we do not disturb any other fields except the one in which the change is to be made. Also note that the character insert process is disabled during the READ operation.

The character delete operation enables one to delete a character from any memory location. This change will only affect the field in which the character is deleted. To delete a character, the cursor has to be placed under that character and the DEL key on the keyboard depressed. The effect produced is to delete that character, shift the rest of the characters in the field one position to the left, and introduce a blank at the end of that field. The character delete logic [Section A, B-3, 4] handles all these functions as described below.

When the DEL key is depressed, the signal, DELKEY sets up the F/F F3, 5. The leading edge of ADCOMG sets F3, 9 true and enables the NAND gate F2, 1. When MEOLN goes true at the end of the video line F2, 3 pulses low and sets up the two latches H3 and F2. One of the effects of DSP (Delete Space) going low is to activate one of the 3 signals, DSP1*, DSP2*, and DSP3*. These go to the Memory Card and insert a SPACE code at the end of the line. After a slight delay DSP* going low resets the F/F pair F3. The other effect is that H3, 6 goes low causing H1, 8 to go low and thus making INDCL1, INDCL2 or INDCL3 long by one character time. These make the Display Memory one-character longer to accommodate the SPACE code. The trailing edge of MEOLB* sets up E2, 5. This disables the gates E1, 9 or D1, 9 or C1, 9. As a result MCLEN* has no effect on MEMCL1, 2, 3 or M1PH1*, M1PH2*, M2PH2, M3PH1* or M3PH2*. One set of these clocks follow the clocks MEMCLK, PH1 and PH2 for one character time till E2,5 is reset by E2, 8. This is to adjust the memory that was one character longer for 640 counts. Next time when ADCOMG* goes false it resets the latch H3 returning the INDCL1, 2 or 3 to their original form losing the character in the latch, i.e., (replaced by the character after it). All this has the effect of shifting all characters to the left by one character position and replacing the last character in the line with a space. If there was a protected field before the end of the line the entire process would be identical except that now DSP would go false with H6, 12 going true instead of MEOLN going true. Hence character deletion would not affect any other fields.

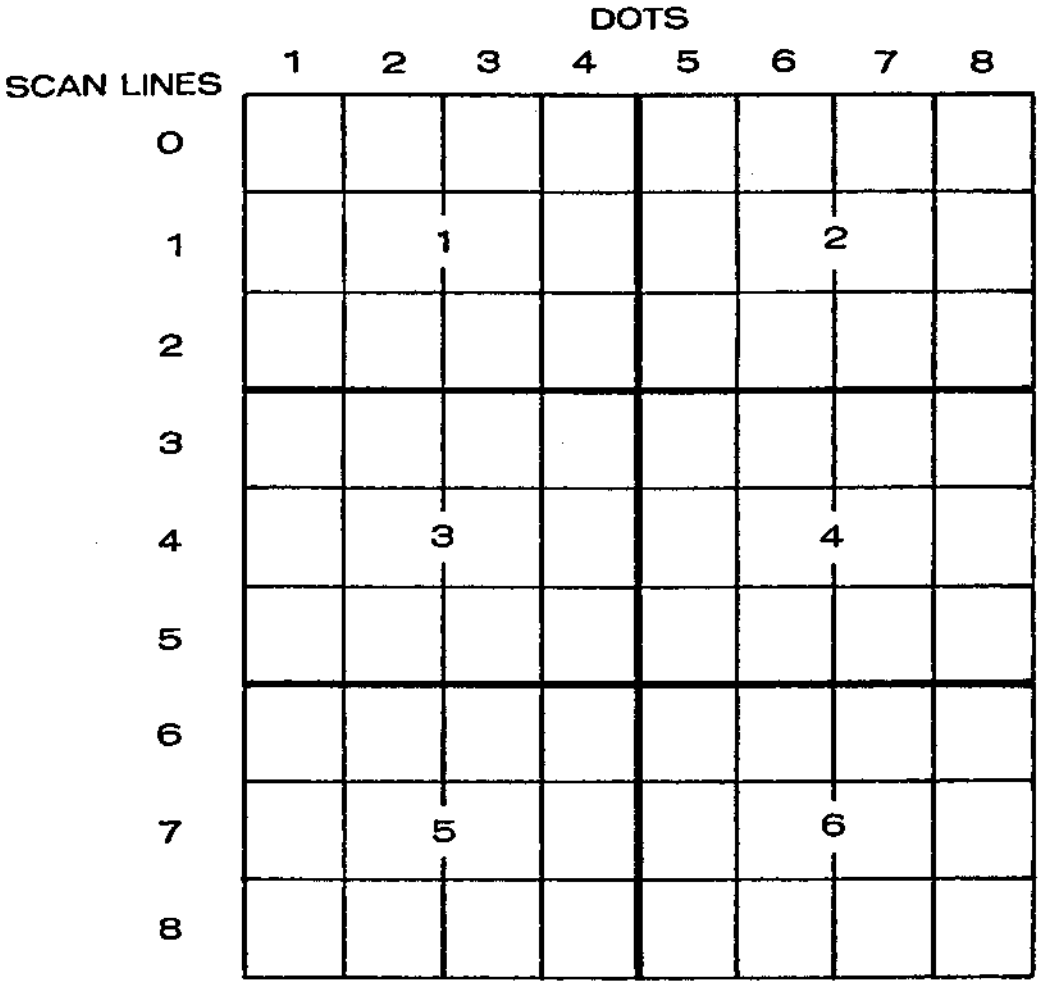
2.3.5.2 Graphics

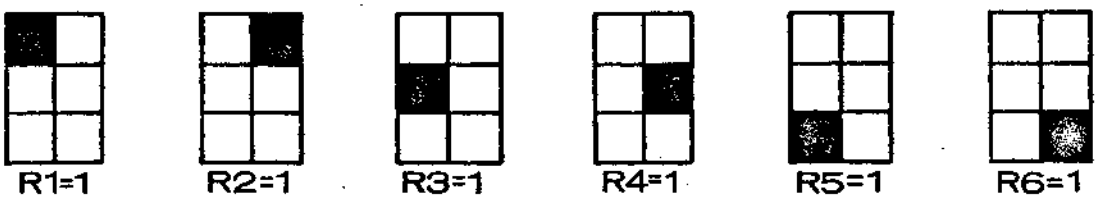
The Graphics mode on the 980 enables one to display the information in a graphics mode besides the regular alphanumeric mode. The technique of video representation in both these cases is the same, i.e., horizontal scanning technique; however, the "graphic" characters are generated in a different way. The normal alphanumeric characters are generated by a 5 x 7 dot-matrix in a field of 7 x 9 dots. As opposed to this, "graphic" characters are generated by a combination of six video elements each of which is a 4 x 3 dot-matrix. Refer to Figure 2.13. The six elements are numbered as shown. They are addressed by the 6 Refresh bits R1 through R6G. Each of the bits having a value of logical "1" in a character code causes the corresponding element to appear black on the screen [Figure 2.13 illustrates the point]. By using the proper codes, a total of 64 "graphic" characters can be displayed on the screen. These characters can be used to generate graphs as shown in the figure. A vertical column of the letter U can generate a vertical bar while a string of the letter L can generate a horizontal bar. The symbol can similarly be used in graphics mode to obtain thick bars. Since two "graphic" characters are not separated, by any dots, the vertical and horizontal bars remain continuous and can form sharp and crisp graph patterns on the screen. To put it in a more concise form, we divide the entire screen into 1920 x 6 = 11,520 elements and a group of six elements everytime we write a "graphic" character.

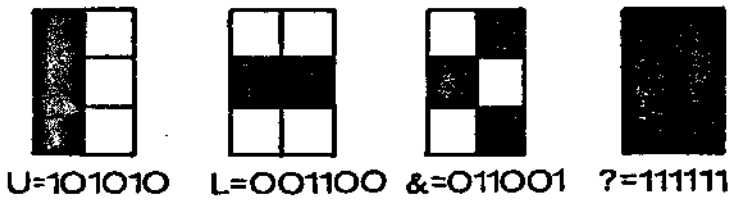
The way this is achieved is explained below. Refer to the schematic drawing. The graphics logic is in Section D-2. R1 through R6G are the Refresh bits that also go to the character generation circuit. SL0-2 is a signal that stays true for scan lines 0,1 and 2 and SL3-5 is a signal that stays true for scan lines 3,4 and 5.

From the figure we see that R1, R3 & R5 cause the 3 elements in the left column to appear black while R2, R4 and R6G cause the other 3 elements to appear black. This decoding is done by the NAND gates K1 J1 and the 3-input NAND gate K2. K2, 6 or K2, 12 going true sets the F/F pair K3, 9 or K3, 5. The left or the right column of elements is selected by the state of D4* and D4. Either of these causes K4, 11 to go true. D4, D4* is a pulse occurring at every half character interval. It is generated by the circuit in Section C-2.

Fig. 2-13


DOTS
1 2 3 4 5 6 7 8
SCAN LINES
0
1
2
3
4
5
6
7
8
1
2
3
4
5
6


R1=1
R2=1
R3=1
R4=1
R5=1
R6=1


U=101010
L=001100
&=011001
?=111111

The first pulse sets J3, 6 low and half a character later the second pulse resets J3, 6 true. This generates the signal VGRF* (Video Graphics*) that goes to the VIDGEN card where it is mixed with the other video signals before applying it to the monitor. Note that the graphics mode cannot be enabled until GRAPH* goes low. It goes low when the terminal receives the control code EM (End of Medium), i.e. Y^C.

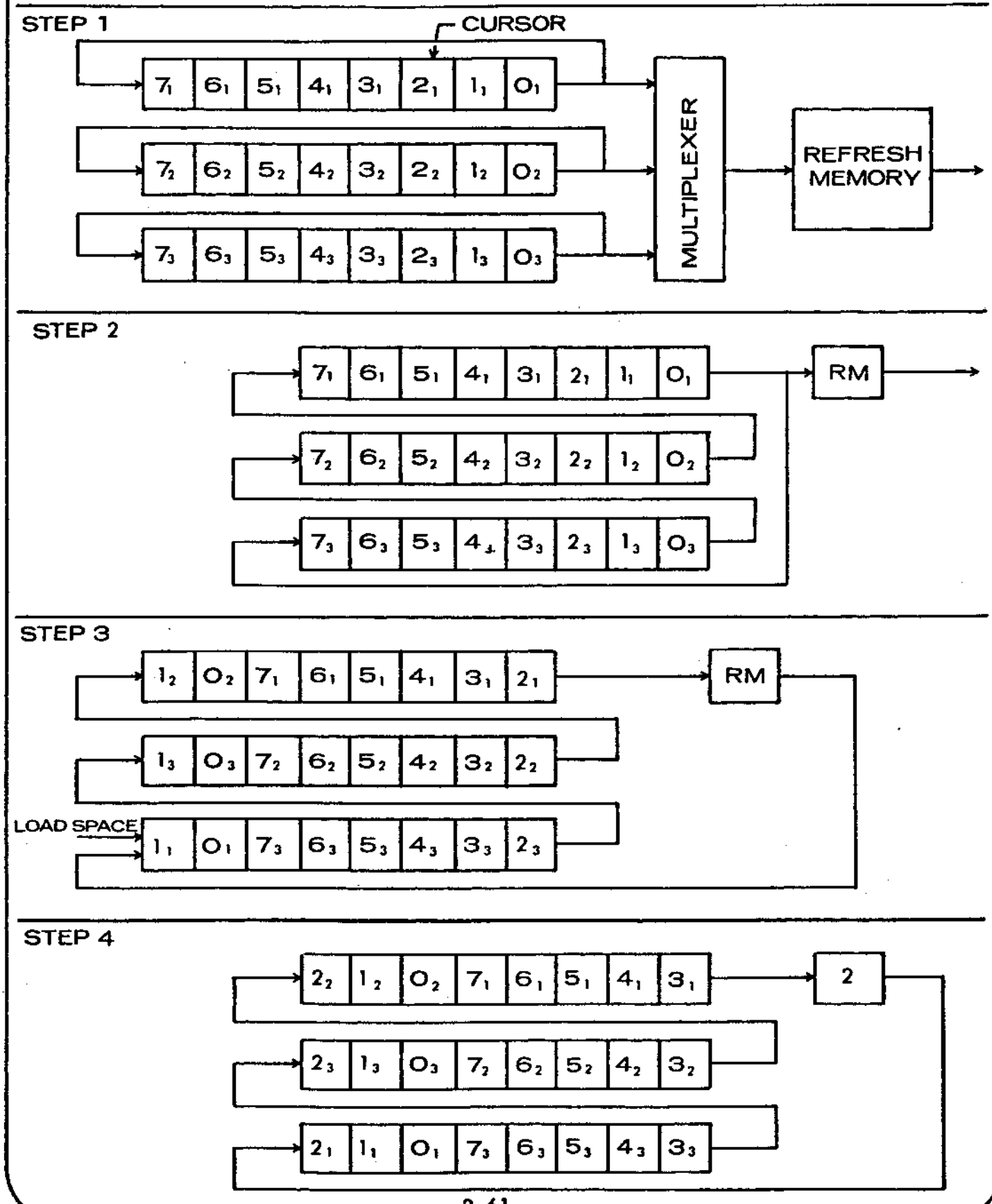
2.3.5.3 Line Insert/Delete

This is a powerful editing feature which allows one to insert or delete a whole line of 80 characters anywhere on the screen. When we do a line insert operation the line in which the cursor is sitting is filled with spaces, all the other lines below this line, and including this line, are moved one line down and the last line of the page is lost. When we do a line delete operation the line in which the cursor is sitting is deleted, all the lines below this line move up by one and the last line of the page is filled with spaces. As far as the system is concerned, the line delete operation is the same as the line insert operation since in both these operations a full line of 80 spaces is inserted. The difference, however, lies in when the line of SPACES is inserted and when the operation is reset. Since an entire line of 80 SPACES has to be accommodated temporarily, the memories consisting of 24 lines have to be extended to 25 lines. This extra line of memory is provided by the one-line Refresh Memory. All the signals required to manipulate the memories are generated by the Line Insert/Delete logic [Section C, D-3, 4].

The line insert operation will now be explained in detail. Refer to Figure 2.14. It shows in 7 steps the entire line insert operation. Normally the three memory modules recirculate their contents on themselves. Their outputs are multiplexed and fed to the one-line Refresh Memory. For the sake of discussion assume that the cursor is in line 3 of memory module #1. This is shown in Step 1. Now when the terminal receives a line insert command, the individual modules have to be first cascaded to form a single 24 line memory. This should be done only when all the memory modules are at the start of the next recirculating cycle.

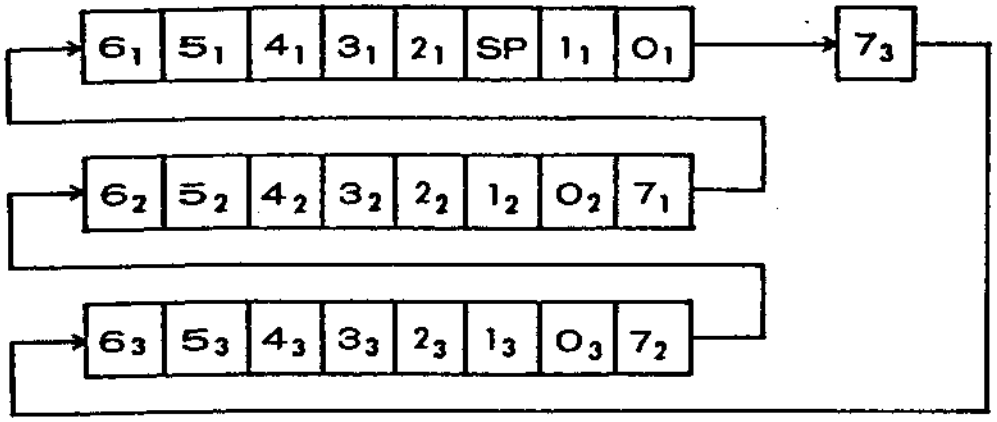
LINE INSERT

Fig. 2·14

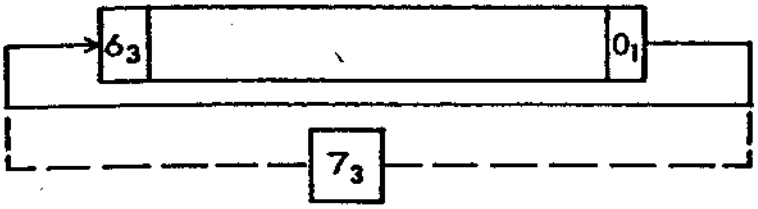


LINE INSERT
Fig.2-14 (Sht.2)

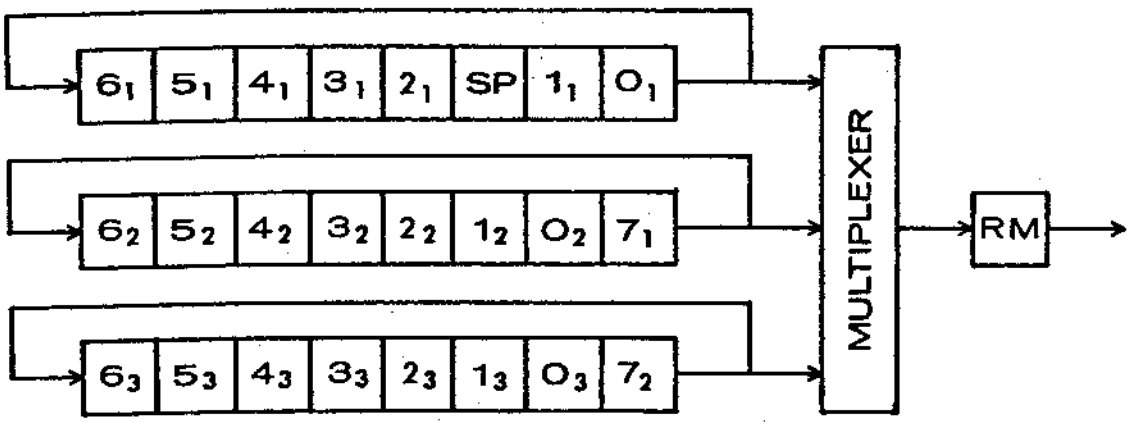
STEP 5



STEP 6



STEP 7



Also the Refresh Memory should be tied only to the output of memory module #1. Step 2 illustrates the memory configuration. Now before the Refresh Memory is included in the path, we have to wait until the line of interest is at the output of module #1. Once this is attained, the recirculation path between the 1st and the 3rd modules is broken. The output of the 1st module is now tied to the input of the 3rd module via the Refresh Memory. At the same time, SPACES are loaded into the 3rd memory as shown in Step 3. Step 4 illustrates the memory configuration at this point. The next time the memories are back with line 0 of module 1 about to shift into the Refresh and the last line is in the refresh as shown in Step 5. At this point in time, the Refresh Memory has to be removed from the path, and the memories tied back as they were in Step 1. Step 6 shows that the last line in the Refresh Memory is lost and the SPACES are between line 1, and 2. All the other lines have shifted down by one, and the last line of the page will be lost. This completes the line insert operation. The memories, as they appear after the line insert operation, is completed and are shown in Step 7.

Refer to the schematic [Section C, D-4]. When the line insert command is received, the signal, LNINS sets the F/F L2, 9 true. This also makes K4, 3 to go low and thus releases the clamp on the count of 3 counter E5. At the same time INDEL* (Insert/Delete*) goes low thus indicating to the terminal that the line insert or delete operation is being performed. L3, 2 is true. When TR7* and MEOLN* pulse low it indicates that the memories have their first line of data at their outputs. The AND function of TR7* and MEOLN* is then used to set L3, 5 true on its trailing edge. LD1 (Insert/Delete 1) is now true causing ID12* to go false. This produces two effects. One it goes to the Memory card and cascades the memory modules to form one long 25-line memory. Secondly, it forces AMEMO and BMEMO [Section C-3] low, thus connecting the Refresh Memory to the output of the 1st module only. The memories are now as shown in Step 2. The AND function of TR7* and MEOLN* also clocks the counter E5. Once the right count is reached and the line comparison for the entire 24-line memory is made, the signal COMP* (Compare*) goes false. This indicates that the line of interest (line 3 in our case) is at the output of module 1.

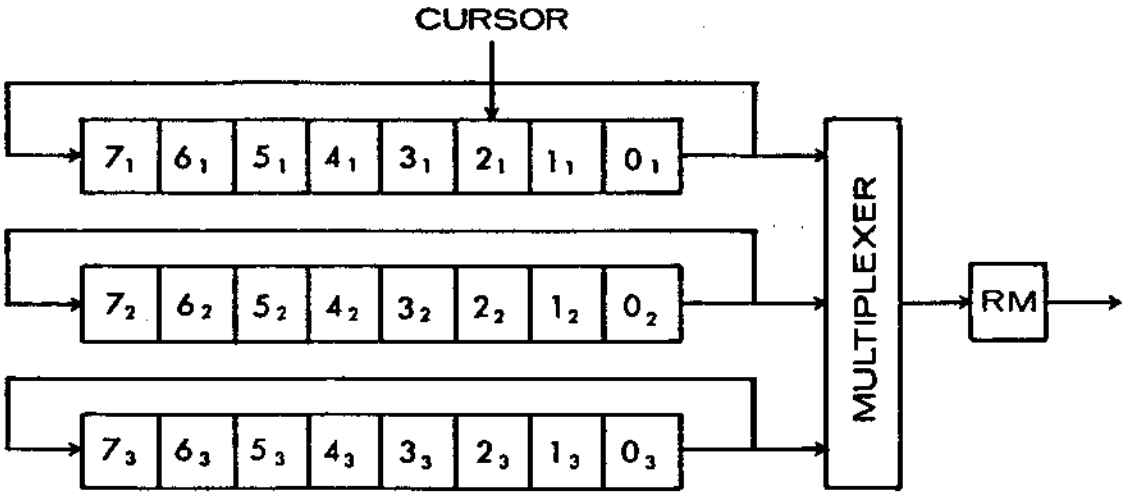
Since LI (Line Insert) is true, the leading edge of COMP* sets ID2 true and at the same time resets ID1. ID2 (Insert/Delete 2) going true causes two things. Firstly, it causes the signal LL* (Line long*) [Section C-3] to go low. This signal goes to the Memory card and causes line 3 to be loaded into the Refresh Memory and ties the output of the Refresh Memory to the input of the 3rd module. Secondly, ID2 also causes the signal LIDSP* (Load Insert/Delete Space*) to go low, thus forcing the memory to load a line of SPACES in the bottom memory. This is shown in Step 3, and the memory configuration at this point is shown in Step 4. When the signal CNT3, (Count 3) goes true again indicating that line 0 is again about to shift out of the top memory, RSTCL* (Reset Clock*) goes low, resets the F/F L4, 8. LNRST* (Line Reset*) goes low resetting L2, 9. The counter is now held reset. This causes the signal LL* and ID12* to go low. The effect of this is to remove the Refresh Memory from the path and also to separate the individual modules so that they recirculate on themselves. Step 6 shows that when the Refresh Memory is broken from the path, the last line is lost and the spaces inserted between 1 and 2. The memories return to their original form as shown in Step 7 with a line of SPACES being inserted in the 3rd line of module #1.

The line delete operation is explained below. Refer to Figure 2.15. It shows the 5 steps through which the memories have to go through in order to successfully complete the operation. The 1st step shows the normal mode in which the memories operate. When the terminal receives a line delete command, the signal LNDEL goes true and set up LD (Line Delete), L2, 5 true. This causes K4, 3 to go true and release the clamp on the counter. When the memories have circulated once, i.e., their first line is now at the output,TR7* and MEOLN* causes L3, 5 to go true. ID1 going true immediately causes the memories to be cascaded (since ID12* goes low) and also ties in the Refresh Memory (since LL* goes low) as shown in Step 2.

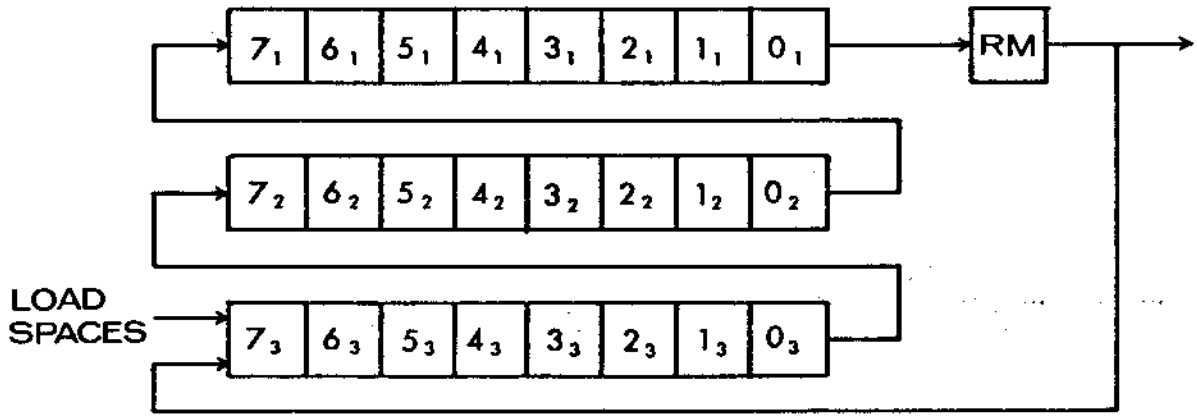
At the same time, a full line of 80 SPACES is inserted in the bottom memory since LIDSP* goes false. When COMP* goes false at comparison, the memories are as shown in Step 3. Also since LI is low L3, 9, (ID2)goes true on the leading edge of COMP. The 3rd line of module #1 is shifted into the Refresh Memory. ID2 going true resets ID1, and removes the Refresh Memory from the path, though still keeping the Display modules cascaded. [Step 4].

LINE DELETE
Fig. 2-15

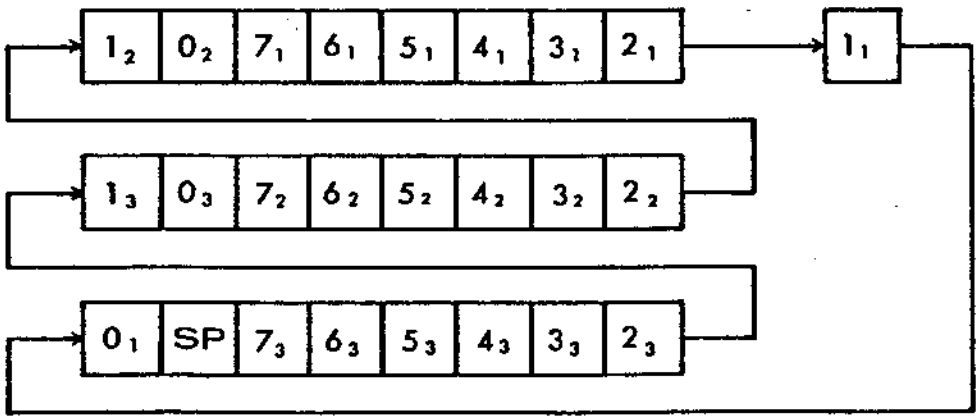
STEP 1



STEP 2

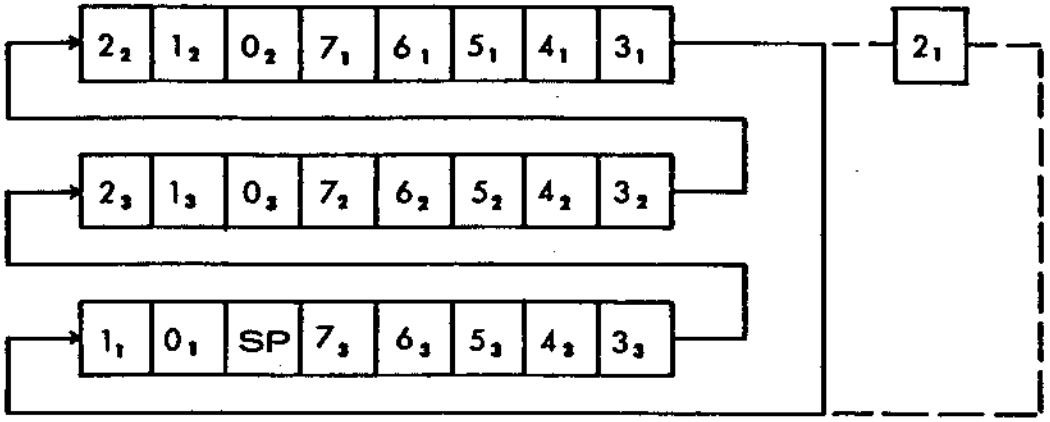


STEP 3

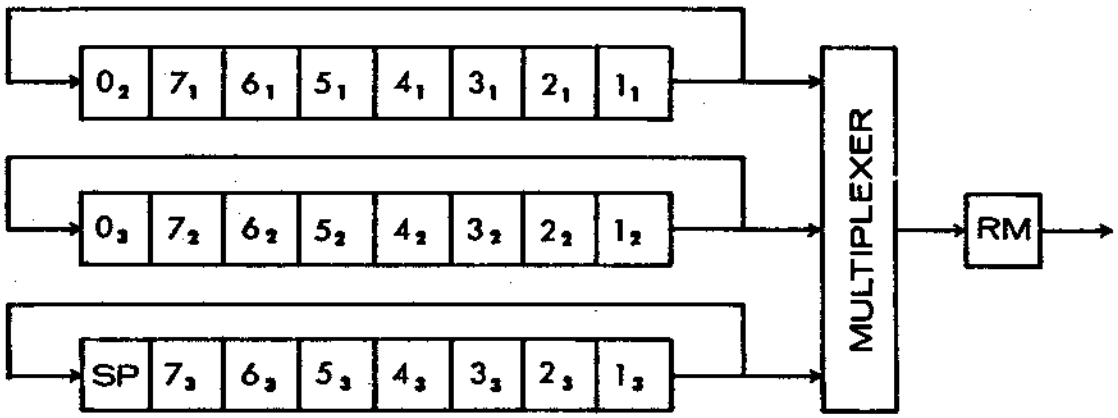


LINE DELETE
Fig. 2-15 (Sht. 2)

STEP 4



STEP 5



When the signal CNTD3 (Count 3 delayed) goes true, and the memories are in sync, RSTLK* goes low. LNRST* goes low and resets the entire logic. The memories return to their original form as shown in Step 5. This completes the line delete operation.

2.3.5.4 Hard Copy Interface

The 980 provides both serial and parallel hard copy interfaces. The serial port can support a serial printer, or a cassette, and is capable of operating at baud rates as high as 9600 baud. The parallel port supports a parallel printer, and the communication interchange between the 980 and the parallel printer is strictly on a handshake basis. As such the parallel printer dictates the speed of transmission. If both the serial and the parallel printer are connected to the 980 at the same time, the slowest of the three devices determines the speed of information interchange.

To start with consider the serial interface. Assume that the CPU and the 980 are operating at a higher baud rate (this is fixed by the speed of the Front End card) than the serial printer. This provides us with the flexibility of exchanging information with the CPU at a faster rate, thus freeing it to perform other duties and transmitting this information to the printer at a slower rate. This is achieved by using a UAR/T in the interface logic. The UAR/T is not used in its traditional form, (i.e., a serial-to-parallel converter). Instead it is used as a serial-to-serial converter. The speeds of the two streams of serial data is determined by two different clocks, one for the receiver and the other for the transmitter. The receiver clock is the same as the Front End clock. Thus the hard copy UAR/T receives data at the same speed as the Front End UAR/T. However, it transmits the data at a rate fixed by the transmitter clock. It should be noted that the UAR/T is not a character buffer. The reception and the transmission of data is done a character at a time. That is to say the 980 will not accept another character from the CPU until the current character is fully transmitted to the printer. In other words, the rate of character flow is the same between the CPU and the 980 as it is between the 980 and the printer. The difference lies in the rate of bit flow. This is achieved by controlling the signal FERDY (Front End Ready) on the ASYNC/FE card.

Refer to the schematic drawing. The UAR/T is in Section B-1. SDIN (Serial Data In) represents the serial data input to the Front End. If the serial port is enabled, (i.e., SENBL is true) and also HDCEN (Hard Copy Enable) is true, the signal SDIN is applied to the input line (Pin 20) of the UAR/T. When a full character has been received (at a bit rate determined by SCLKIN), DA gives true and after a minimum delay of 1 clock DS* pulses low. This is generated by the F/F pair C5. DS* is used to reset the data available flag, DA and also provide a data strobe, DS* to the transmitter. The received parallel bits are turned around and applied to the transmitter to be converted to serial data. As soon as DS* pulses low TBMT (Transmitter Buffer Empty) signal goes low causing HCRDY (Hard Copy Ready) to go low. This signal is a flag to the Front End that the hard copy interface is busy. HCRDY on the ASYNC/FE card holds the data strobe to that UAR/T reset thus preventing any input from the CPU. Once the entire character has been serially transmitted TBMT goes true again. HCRDY goes true and removes the reset on the ASYNC/FE card, and the next character is input to both the UAR/TS. The serialized data appears on line 25 of the UAR/T as SHCOT (Serial Hard Copy Out). It is converted to EIA levels by B5 [Section C-1], and output to the serial printer as SHEIOT (Serial Hard Copy EIA Out). The same signal is also provided in current loop mode HCLPOT (Hard Copy Current Loop Out). Data from the serial printer or cassette to the 980 appears as SHEIN (Serial Hard Copy EIA In) [Section C-1]. It is converted to TTL levels by B5 to form HCSIN (Hard Copy Serial In). This is used on the ASYNC/FE card to access the system. Thus data from a serial peripheral device can be displayed on the 980 screen. If PRONL (Print On Line) is true HCSIN (Hard Copy Serial in Gated) follows HCSIN and is also transmitted to the CPU via the ASYNC/FE card. HCLPIN (Hard Copy Current Loop In) is the current loop option that can be used by closing switch 2.

Now consider the parallel printer. When HDCEN is true, and INS pulses true on the ASYNC/FE card, the signal PRTST (Printer Strobe) [Section D-1] pulses true. This goes to the parallel printer with the seven parallel hard-copy bits (buffered on the MEMORY card). The printer then raises PRTBSY (Printer Busy).

Section B-1 true. This holds HCRDY and thus in turn FERDY false till such time as the parallel printer has finished processing the parallel character. It then returns to the ready state by forcing PRTBSY low. In this manner, it accepts information by hand-shaking with the 980.

Sometimes it is desirable to have a local dump of the information displayed on the 980 screen. For this we have the local print mode. The local print mode can be entered into via the keyboard or on receiving the proper command from the CPU. In either case, the printers have to be off-line, i.e., PRONLN (Print On Line) should be low. LPCOD (Local Print Code).

Section B-1 is the command from the CPU and LPRKY (Local Print Key) is the signal from the keyboard. When either goes true and the printers are off-line SLOC* (Send Local*) goes low. This signal goes to the CONTROL card and triggers the READ flip-flop D5, 5 [Section C-2] true. The signal, LPRT* (Local Print*) goes false. This does a couple of things. It holds MESSG and CONV low thus forcing the 980 into the Page Mode. Secondly, it enables the hard copy interface by forcing HDCEN true [Section B-1], and finally it goes to the ASYNC/FE card and disables the SEIAOT line, thus preventing the information to go the CPU during a local dump. Once the dump is completed, READB* goes true again and resets the LPRT flip-flop D5. Note that local print mode is disabled when the printers are On Line since PRONL* is low.

2.3.5.5 Miscellaneous

The four NAND gates B1 [Section C-2] help to select the mode in which the device operates. Signals MESSIN (Message In) and CONVIN (Conversation In) are from the mode switch bracket on the front panel. In message mode MESSIN is high causing the signal MESSG to be high and CONV to be low. In conversation mode CONVIN is also high and thus CONV and MESSG are high. In page mode both MESSG and CONV are low.

If the printers are faster than the CPU, this could be taken advantage of during the local dump by the circuit in Section B, C-3. During the dump LPRT is true thus disabling C3, 2 and enabling C3, 10. In this case, SCLKIN does not follow the Front End clock FCOM but follows a much faster clock derived from PH1.

3. GLOSSARY OF SIGNAL NAMES

A, B, A+B	-		-	Select Address for memory module.
ACCESS	-	Access	-	Loads SPACES in the memory during power-on-reset and on receipt of CR & FF codes.
ADDCOM	-	Address Comparison	-	Character and Line Counter Comparison.
ADV	-	Advance	-	Cursor crossed line boundary
AMEMO, BMEMO	-	A or B Memory output	-	Selects Memory module for Refresh memory.
B1KB* - B7KB*	-	Keyboard bits	-	Represent the 7-bit ASCII code.
B8KB*	-	Keyboard bit	-	Causes ESC code to be inserted before the character
B9KB*	-	Keyboard bit	-	Causes the terminal to momentarily enter FDX mode.
B10-B70	-	Data bits	-	The main data buss.
B1HC-B7HC	-	Hard Copy bits	-	Used for parallel printer.
BEL	-	Bell	-	Alarm code
BELDR	-	Bell Drive	-	Drives the alarm.
BMEMI	-	Buffered Memory Input	-	Cascades the memory modules to form one 24-line memory.
BSY1*, BSY2*	-	Busy 1, Busy 2	-	Terminal busy during horizontal addressing.

BSY3*	-	Busy 3	-	Terminal busy during horizontal tabbing.
BLK	-	Block	-	Blocks data flow to insert special codes like SO, SI, GS, CR.
CA0-CA6	-	Character count bits	-	Horizontal position of the cursor.
CHCOM	-	Character Comparison	-	The contents of the character tracking and address counters are equal.
CHADR	-	Character Address	-	Transmits the character address of the cursor.
CLK	-	Clock	-	Video shift clock (12.528 MHz)
COMBSN	-	Combined Sync	-	To sync the external video.
CNTLKY	-	Control key	-	Function key from the keyboard.
CHRZ	-	Character Zero	-	Cursor is in the zeroeth character position.
CONV	-	Conversation	-	Conversation mode.
COMPR*	-	Compress	-	Compresses a line of SPACES during fast-read.
CONVIN	-	Conversation IN	-	From the mode switch bracket
CR	-	Carriage Return	-	Decode from keyboard.
CRSND*	-	Send Carriage Return	-	Transmits the End of Line code (CR).
CR + FF	-	Carriage Return or Form Feed	-	CR or FF code received

CURDWN	-	Cursor Down	-	Keyboard function.
CUREN	-	Cursor Enable	-	A,B equals SECT1, SECT2.
DA	-	Data Available	-	Flag from the UAR/T.
DS*	-	Data Strobe	-	Strobes parallel data B10-B70 into the UAR/T.
DATAGT	-	Data Gate	-	Gates data. Set at character count 16, reset at count 96.
DATTRY	-	Data Terminal	-	Flag to the modem for EIA operation.
DC1	-	Device Control 1	-	ASCII code. X-mits data.
DLACH*	-	Data Latch	-	Latches data on the output buss.
DSP	-	Delete Space	-	Loades SPACES during charachter delete.
EIACLS	-	Clear to Send (EIA Level)	-	Allows terminal to input characters.
EIARDY	-	EIA Ready	-	Indicates that the UAR/T is ready to accept a character.
EIARTS	-	Request to Send (EIA LEVEL)	-	Signal to modem indicating terminal ready to send.
ENOLN	-	End of Line	-	Cursor has just crossed the line boundary.
ENQ	-	Enquire	-	ASCII Control Code (E^C)
EOM	-	End of Memory Code	-	Inserts ETX after a block of message.

EOL	-	End of Line Code	-	Inserts CR after a line of message.
ERR	-	Error	-	Framing or Parity Error
ESC	-	Escape	-	ASCII control code (^{C})
EXTRQ*	-	External Request	-	The current character/line address of the cursor is sent out on the buss.
CARLT	-	Carrier Light	-	Terminal commands the carrier.
CINSL*	-	Char. Insert Load Strobe	-	Inserts the required character in the line.
CNTD3	-	Count 3 delayed	-	The video has once again scanned module 1 after having scanned all the 3 modules.
CRALOW	-	Allow Carriage Return	-	Sends CR code before GS code.
FDXRQ*	-	Full Duplex Request	-	Terminal is in FDX mode.
FERDY	-	Front End Ready	-	Front End is ready to accept the next character.
FF	-	Form Feed	-	ASCII Control Code (L^{C}).
FFENB	-	Enable Form Feed	-	Enables FF code from the keyboard only.
FKYSTB	-	Function Key Strobe	-	Strobe for cursor movements.

FOFF	-	Format OFF	-	Disables field protection.
FON	-	Format ON	-	Enables field protection.
FSBLNK	-	Fast Blink	-	Enables data to blink at 4 Hz rate.
GRAPH*	-	Graphics	-	Terminal enters graphics mode.
GRPHEN	-	Graphics Enable	-	Enables graphic mode on receipt of EM code (Y^C)
GSALOW	-	Allow Group Separator	-	Enables GS code to go before CR.
GSEN	-	Group Separator Enables	-	Enables GS code to go out on the buss.
HADR	-	Horizontal Address	-	Enables horizontal address clock.
HADRC	-	Horizontal Address Clock	-	Clocks the cursor forward by the required address.
HALF	-	Half Intensity	-	Enables half intensity.
HBLNK	-	Horizontal Blank		Set at character count 97, reset at count 16.
HCLPIN	-	Hard Copy Current Loop Input		Current Loop in for Hard copy.
HCLK	-	Hard Copy Clock	-	Transmitter clock for hard copy.
HCLPOT	-	Hard Copy Current Loop Output		Current Loop out for hard copy.
HCRDY	-	Hard Copy Ready	-	Both serial and parallel printers ready to accept the next character.

HCSIN	-	Hard Copy Serial Input	-	Goes only to the terminal.
HCSING	-	HCSIN Gated	-	Goes to terminal and CPU.
HDCEN	-	Hard Copy Enable	-	Enables data to go to the printers.
HDRIVE	-	Horizontal Drive	-	Used by internal monitor Sets at character count of 100.
HOME	-	Home position	-	Function key.
HT	-	Horizontal Tab	-	ASCII control code (I^C).
ID1, ID2, ID12	-	Insert/Delete 1, 2, 1 or 2	-	Cascade the memory modules during line insert/delete.
INDCL1,2,3	-	Insert/Delete Clocks 1,2, 3	-	Clocks used to insert/ delete a character.
INDEL*	-	Insert or Delete	-	Indicates that line insert/ delete is being performed.
INSD	-	Data Input Strobe	-	Strobes whenever data is to be entered in memory.
INSR	-	Received Input Strobe	-	When data is received by the UAR/T.
INST	-	Input Strobe	-	Used for both READ and WRITE Operations.
INST1	-	Input Strobe 1	-	Strobe for usual codes.
INST2	-	Input Strobe 2	-	Strobe for special codes
KANEN	-	Kannen	-	Enables the Katakana ROM.
KBINP	-	Keyboard Input	-	Indicates that the input is from the keyboard.

KBL*	-	Keyboard Latch	-	Latches keyboard data onto the buss.
KBLOK*	-	Keyboard Lock	-	Locks the keyboard.
KBRQ	-	Keyboard Request	-	Requests input from the keyboard.
KBSTB*	-	Keyboard Strobe	-	Strobe from the keyboard
LA-LA2	-	Line Count Bits	-	Vertical position of the cursor.
LBIAS	-	Loop Bias	-	Supplies current in current loop modes.
LDLNE*	-	Load Line	-	Loads the vertical address during vertical tabbing.
LF	-	Line Feed	-	ASCII Control Code (J^C)
LIDSP*	-	Load Insert/ Delete Space	-	Loads SPACES during line insert/delete.
L1-L32	-	Logic Line	-	Counts the logic lines scanned by the video.
LL*	-	Long Line	-	Makes the memory longer by one line during line insert/ delete.
LNADR	-	Line Address	-	Outputs the line address of the cursor.
LNADV*	-	Line Advance	-	Causes the cursor to advance by one line.
LNDEL	-	Line Delete	-	Code to delete a line.
LNINS	-	Line Insert	-	Code to insert a line.
LNZR	-	Line Zero	-	Cursor is in the zero line.

LOAD*	-	Load	-	Loads data into memory.
LOT - LOT	-	Loop Out	-	Current loop output.
LPCOD	-	Local Print Code	-	Code to perform a load dump.
LPRKY	-	Local Print Key	-	Function key from the keyboard.
LPRT*	-	Local Print	-	Causes local print operation.
LSTLNE	-	Last Line	-	When cursor is in the last line of the page.
LDY*	-	Load Y	-	Loads the horizontal address in the counter.
MCLEN*	-	Memory Clock Enable	-	Allows for synchronization during vertical flyback.
MDEN*	-	Memory Data Enable	-	Enables the memory data to go to the buss.
MEMCLK	-	Memory Clock	-	Provides clock to the static shift register.
MEMCLG	-	Memory Clock Gated	-	Used on 920 in lieu of MEMCLK1, 2, 3 & INDCL1, 2, 3.
MEOLN*	-	Memory End of Line	-	Display memories have shifted 80 counts.
MESCR*	-	Message-CR	-	Sends ETX code after CR in Mess mode.
MESSG	-	Message	-	Message mode.
MESSIN	-	Message IN	-	From the mode switch bracket.

METX*	-	Memory ETX	-	Decode of ETX code buried in memory.
M1PH1, M1PH2, M2PH1, M2PH2, M3PH1, M3PH2,	- - -	Buffered PH1, PH2 for the memories	-	Clocks to the dynamic shift registers.
M1-1-M3-7	-	Memory Bits	-	Display memory bits Ma-b = Bit b in module a.
MOTRQ*	-	Memory Output Request	-	Requests the output of memory data.
MRST*	-	Memory Reset	-	Resets MOTRQ*
M1TP, M2TP, M3TP	-	Memory Tag Prompt	-	Tab bit available one clock earlier.
OUTEN	-	Output Enable	-	Enables the serial data to go to the CPU
PAGE	-	Page	-	Page Mode
PFCLK*	-	Protected Field Clock	-	Clocks the cursor forward through the protected field.
PH1, PH2	-	ϕ_1 , ϕ_2	-	Two phase clocks for one character period.
PRONLN	-	Print On Line	-	Function key from the keyboard.
PRTBSY	-	Printer Busy	-	Flag from the parallel printer indicating it is busy.
PRTST	-	Printer Strobe	-	Strobe to the parallel printer.
RDA*	-	Reset Data Available	-	Resets DA line on the UAR/T.

READ*	-	Read	-	Terminal is in READ mode.
READB*	-	Read Buffered	-	Buffered READ signal.
READT*	-	Read Trigger	-	Triggers the READ circuit.
REPEAT	-	Repeat	-	Function key from the keyboard.
RFCLK	-	Refresh Clock	-	Clock to the Refresh Memory.
R1-R6G	-	Refresh Bits	-	Used to generate characters.
ROM 1,2,3	-	ROM 1,2,3	-	Enables ROM 1,2 or 3.
RQSND	-	Request to Send	-	Indicates that the terminal is ready.
RR1-RRT	-	Refresh Memory BITS	-	Latched to form R1-R6G
RSEOM*	-	End of Memory Reset		Resets the circuit after sending the EOM code.
RS	-	Record Separator	-	ASCII Control Code (↑C)
RST	-	Power-On-Reset	-	Resets the system when power is applied.
RST1	-	Reset 1	-	Provides a refresh rate of 60 frames per second.
RST2	-	Reset 2	-	Resets the RQSND circuit.
RSTCL*	-	Reset Clock	-	Resets the Line Insert/ delete circuit.
RUBOUT	-	Rub Out or Delete	-	ASCII Control Code.
SPACE	-	Space	-	Loads SPACE code in the memories.

SRSTRB	-	Shift Register Strobe	-	Strobes the video shift register.
SRLD*	-	Shift Register Load	-	Gated SRSTRB
STP*	-	Stop	-	Stops the horizontal address clock.
SPEC*	-	Special	-	Enables special codes
SYNCL	-	Sync Clock	-	Used for video to memory synchronization.
SER	-	Serial	-	Serialized video data.
SLBLNK	-	Slow Blink	-	Enables data to blink at 2Hz rate.
SDOT	-	Serial Data Out	-	Serialized data out of the UAR/T
SENBL	-	Serial Enable	-	Enables serial printer.
SECT 1,2	-	Section 1,2	-	Select memory module.
SHFTGT	-	Shift Gate	-	Shifts gated data into the video shift register. Set at character count 15 and reset at count 95.
SDIN	-	Serial Data In	-	Serial input to the UAR/T
SHEIN	-	Serial Hard Copy In (EIA Level)	-	Input from the serial printer.
SEIAIN	-	Serial EIA Input (EIA Level)	-	Serial input from the CPU.
SEIAOT	-	Serial EIA Output (EIA Level)	-	Serial output to the CPU

SLOC*	-	Send Local Printer-		Sets the Local Print Circuit
TIN1-7	-	Input Bits	-	Used internally in the terminal.
TRDY*	-	Terminal READY	-	Indicates that the terminal is ready to accept data.
TABCL*	-	Tab Clock	-	Clocks the cursor forward during tabbing.
TBMT	-	Transmitter Buffer Empty	-	Data bits holding register in the UAR/T is ready to receive the data bits.
TR7*	-	Track 7	-	Video is scanning through the last line of the module.
TRINH*	-	Transmit Inhibit	-	Inhibits transmission of data.
TRMRDY	-	Terminal Ready	-	Delayed TRDY
TEND	-	End of Transmission	-	Stops transmission by resetting the READ circuit.
VERTAB	-	Vertical Tab	-	Latched vertical tab command
VGRF*	-	Graphics Video	-	Serial video for graphics mode.
XMIT	-	Transmit	-	Function key from the keyboard.

4. UNIT TEST PROCEDURE

The off-line test procedure described in this section provides assurance that the terminal is operating properly. We shall assume, before the steps below are followed, that no cables are plugged into the data connectors on the rear panel, and that the unit is set up for EIA operation. Also make sure that the serial and parallel printer switches are in the OUT position.

a. Depress the POWER switch to the ON position. The red indicator should light, and the screen should show a clear white rectangular "page" after approximately a 30-second warm-up. The cursor should be at the top left corner of the page unless the terminal is in CONV mode in which case the cursor will be at the bottom left corner. If so, go to PAGE mode.

b. Check all the cursor movements with and without REPEAT function. Move the cursor across the entire screen. Check that HOME is at the top left corner.

c. Check the keyboard by writing every letter on the screen in both lower and upper case. Note the character generation and formation on the screen. CHAR INS key is a lighted alternate-action key. Also PRINT ON is a lighted key. Check the lights under both these keys. PRINT ON light goes OFF by depressing the PRINT OFF key. Erase the screen and check that CONTROL key has to be depressed along with the ERASE key to clear the screen.

d. Write ABDHP ␣ 'ØØ in the top line (where ␣ = SPACE :'Q'= Shift Out mode). $K_C K$ will move the cursor down to the beginning of the 12th line. Write ABDHP ␣ 'Ø'Ø in this line. $K_C W$ will put the cursor at the start of the bottom line. Write ABDHP ␣ 'Ø 'Ø in this line also. Check for correct data in all three memories.

e. Do the character insert and delete test in all the three memories. Go into protected mode by keying in ↑C. The tagged field will appear non-blinking at half intensity. Again do the character insert and delete test. Check that only that variable field in which the cursor is positioned is affected by character insert and delete. Get out of protected mode by keying in ←C.

f. Depress the TAB key and check the horizontal tabbing function. Now go into protected mode and do the horizontal tab. Check that the cursor tabs to the start of the next variable field, and after it has gone through all the variable fields it tabs HOME before going to the next field.

g. Go to CONV mode. Check that the device is in Half-duplex mode. In this mode you should be able to key data on the screen. Check that HOME is at the bottom left corner. Hit NEWLINE and check the scrolling. Also check that protected data wraps around and is saved while the variable data is lost. Scroll the last line through all three memory modules and check that the data is not changed. Hit the TAB key and note that data scrolls upwards and the protected data wraps around. go the FDX mode and check that data keyed in cannot be displayed on the screen. Go back to HDX mode. Get out of protected mode and clear the screen. The cursor should be at the top left corner of the screen. Go to PAGE mode.

h. Key in some data on the top line. Depress the LINE INS key. The cursor should go back to the start of the line, the present line should scroll down by one line, and a line of SPACES will appear in its place. Scroll the line down to the bottom of the page. Now depress the LINE DEL key. The line of data will scroll up by one line, and its place will be taken by a line of SPACES. Scroll the line up through the entire page. Clear the screen.

i. Go to the center of the page. Key in 'ABDHPØ U*'. Now depress Y^C. The terminal will go into graphics mode. Check the graph pattern.RS or US will take the terminal out of graphics mode.

j. Key in {ABDHØP. The letters will blink at a slow rate of 2Hz. Move the cursor in the blank position, and key in}. Note that ABDH will keep blinking at the slow rate. However, P will have now stopped blinking. Check that any data enclosed by the symbols { } blinks at 2Hz.

k. Go to MESS mode. Key some data in the top line. Hit XMIT. The terminal should read that data and the cursor should come to rest at the start of the next line. Go to PAGE mode and check that Q^C also causes the screen to be read. Check that trailing blanks are not transmitted. Also note that READ is inhibited in CONV mode.

l. Go to the centre of the screen and hit $P^C C^C$. This will bury an ETX code in the memory. Also check that C^C is displayed as c only if the CONTROL key is depressed. Now hit XMIT and see that the cursor reads the data and stops at the ETX code on the screen. Depress the PRINT LOCAL key and note that the cursor reads till the ETX code. Clear the screen.

m. Check horizontal addressing by keying the sequence ESC, ENQ,M, N (where M, N form the address). In particular key in ESC, ENQ,/,/. The cursor will come to rest at the 166th position. Now key in ESC, ENQ, Ø, Ø. The cursor should not move.

If all of the above steps are operative, you are ready to start the on-line operation.

5. PHYSICAL ACCESS FOR TEST & REPAIR

5.1 Controls, Indicators and Connectors

A detailed description of the function of all controls and of interface connections is given in ADDS publication 98-3000, HOW TO USE THE CONSUL 980. At this point we shall simply summarize those components.

Controls and indicators on the front of the Consul 980 are:

- An ON-OFF pushbutton power switch.
- A POWER indicator lamp. (Red) This is in series with the fuse in the primary of the power supply transformer.
- A CARRIER indicator lamp. (Yellow) This lamp indicates that the 980 is in command of the carrier.
- Three mode select pushbuttons. These switches permit selection of MESS, PAGE or CONV mode.

Located on the panel [Fig. 5.1] are:

- Parallel and Serial printer ports and their respective IN-OUT DPDT switches. The printer connectors are 25-pin female Cinch or Cannon type DB25-S.
- BNC video output connector. This is used to connect 75-ohm ciaxial cable (RG59/U or equivalent) for driving slaved external monitors.
- EIA and Current Loop Data Connector. This is a 25-pin female Cinch or Cannon type DB25-S.
- A 1.5A "SLO-BLO" fuse.
- A 3-pin power cord connector.

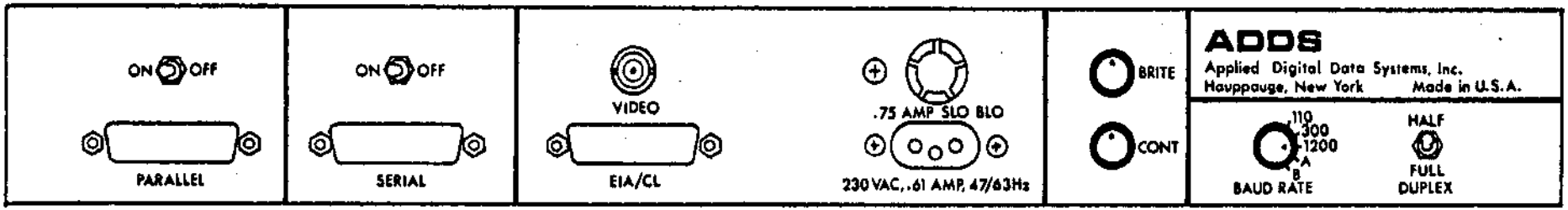
DO NOT PLUG 115 VOLT TERMINAL INTO A 230 V OUTLET

- BRITE control knob. Sets TV screen brightness.
- CONT control knob. Sets TV screen contrast.
- A 5-position BAUD RATE switch. This switch is used to select the desired serial baud rate for the Front End. Speeds of 110, 300, 1200, 2400 and 9000 are standard on the Consul.
- HALF/FULL DUPLEX switch. This is a DPDT switch. It helps to select the Half or Full Duplex mode of transmission.

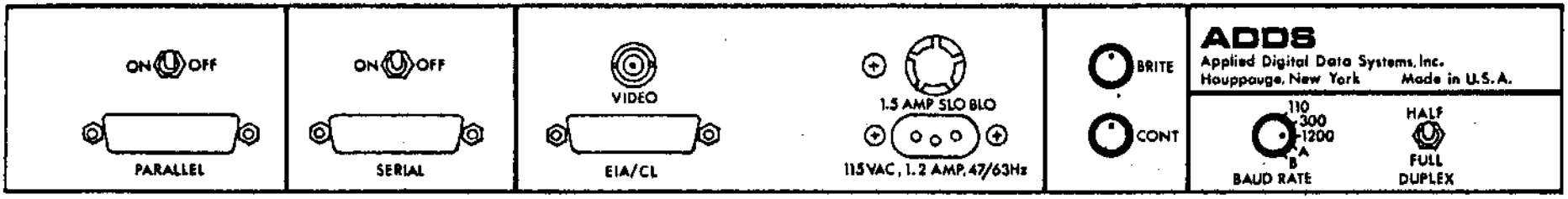
REAR PANEL 980

Fig. 5-1

FOREIGN MODELS



DOMESTIC MODELS



5.2 Access to P.C. Cards and Subassemblies

The top shroud of the Consul is removed to service the PC cards and subassemblies. To take the shroud off, remove four Phillips head screws; two at the lower front corners of the terminal and two at the top rear corners. Then tilt the shroud slightly to the rear and left it off. [See Figure 5.2]

Figure 5.3 shows the 980 with its shroud removed. The item numbers in Figure 5.3 are referenced in the following paragraphs.

Note the four fasteners (#8) by which the shroud is attached.

The majority of service problems involve only removal and replacement of PC cards. The layout of PC cards within the card cage (#6) is show in Figure 5.4. The two hold-down brackets (#5) must be removed before PC cards can be changed. Cards may be removed by grasping the end firmly and working the card up and down while exerting a pulling force. For those personnel who must remove cards frequently a "card puller is recommended. (ADDS service personnel use the "Wire-Grip" puller, part #1733, made by E.H. Titchener and Co., 1 Titchener Place, Binghamton, New York.)

When cards are inserted they should be pushed in until the card shoulder firmly seats against the backplane connector. Cards will not come loose in normal shipment and use since they are firmly seated with long fingers and held in place.

However, if the performance of the device is erratic after shipment (or very rough handling is suspected) the cards should be inspected to insure that all are firmly seated.

When the terminal is "unbuttoned" as in Figure 5.3 power may be applied and the device operated if one wishes to check signals in the cabling, the PC card backplane, connector terminations, etc.

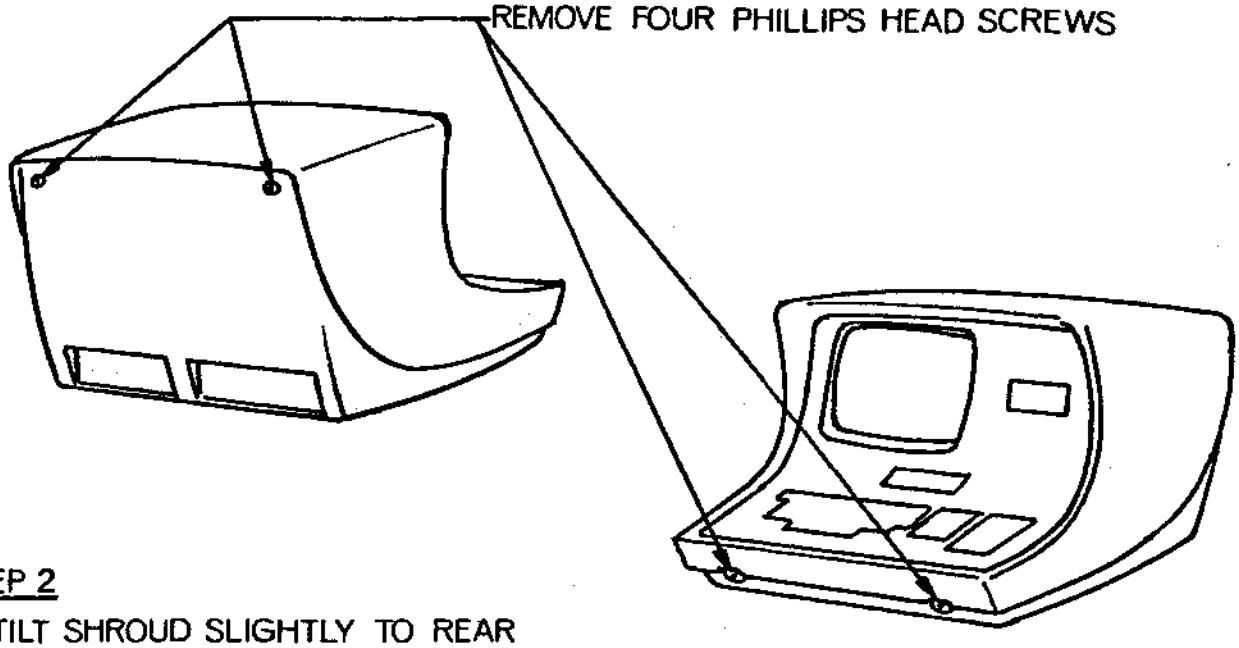
If circuitry is to be checked with an oscilloscope as the terminal is operated, an ADDS extender board should be plugged into a card slot and the card plugged into the end of the extender card. The ADDS extender card has a center ground plane to prevent signal pickup and interference between signals on the two sides of the extender. The extender card is almost a necessity if one wishes to diagnose faults to the chip level, rather than the card level. The alternative for chip-level repair is to sequentially replace the suspect chips on a card, if fault isolation is performed only to a card level.

SHROUD REMOVAL

Fig 5-2

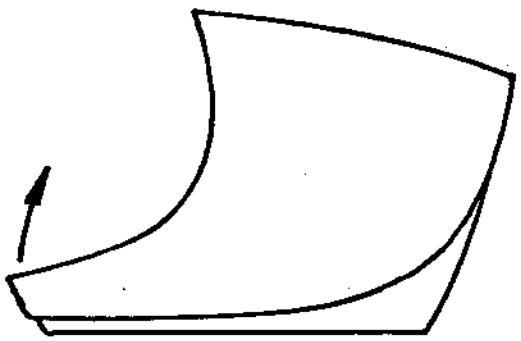
STEP 1

REMOVE FOUR PHILLIPS HEAD SCREWS



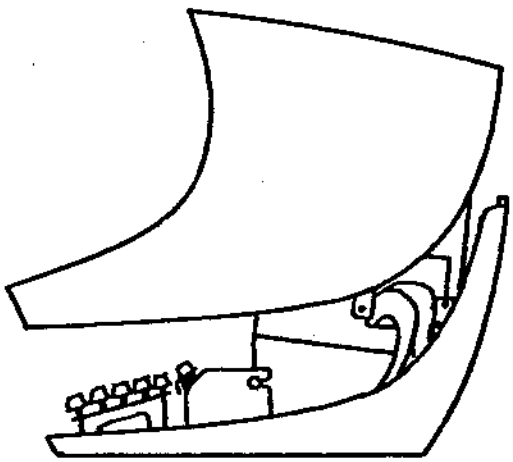
STEP 2

TILT SHROUD SLIGHTLY TO REAR



STEP 3

LIFT SHROUD OFF



980 WITH SHROUD REMOVED

Fig.5-3

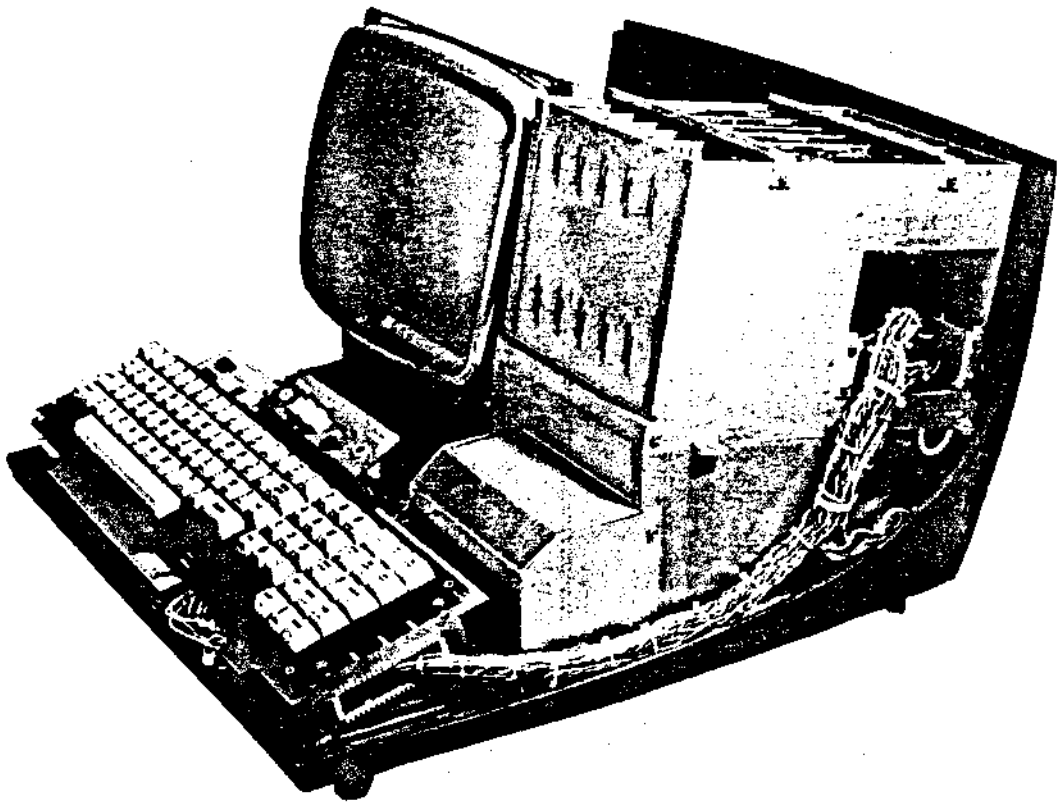
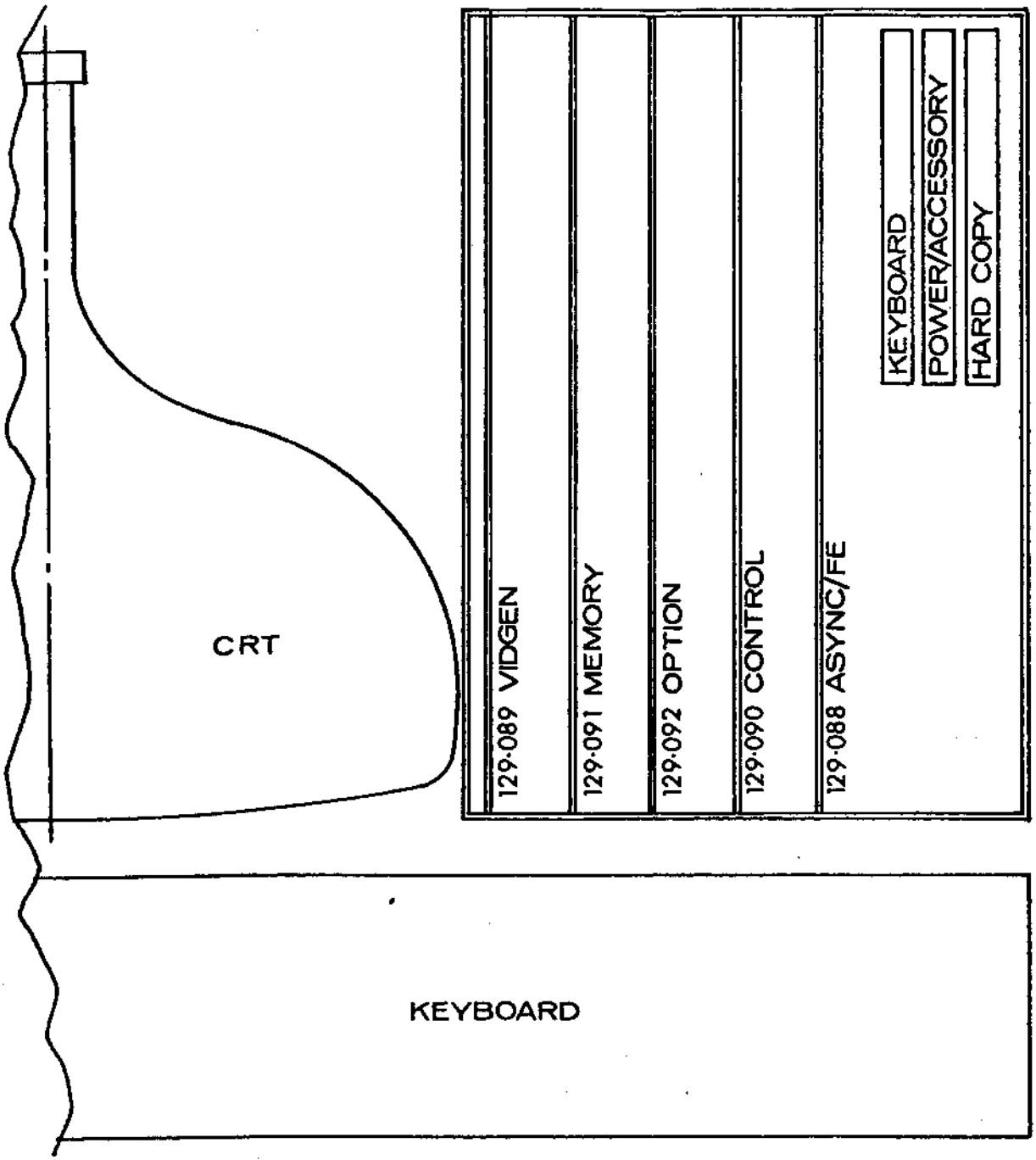


Figure 5.4 - LAYOUT OF P.C. CARDS IN THE CARD CAGE

LAYOUT OF PC BOARDS IN CARD CAGE

Fig. 5-4



Occasionally subassemblies must be removed, rather than simply changing PC cards. Various subassemblies are discussed below, with item numbers referencing Figure 5.3.

CRT monitor To remove, undo 3 nuts (#1) and disconnect the connector on the back edge of the monitor P.C. card, and the "Molex" connector which brings power to the monitor subassembly. The monitor can now be lifted out.

Keyboard (#2) To take the keyboard out remove the screws at each end which secure it to the mounting brackets. Next disconnect the P.C. Board connector on the front of the unit. The keyboard can now be removed.

If when you replace the shroud on your unit any of the keys on the periphery of the keyboard bind on the opening in the shroud, lift the front of the terminal up and loosen the 4 keyboard mounting screws. Now position the keyboard so that there is an even clearance between the keytops and the opening and then tighten the 4 mounting screws. This adjustment should not normally be necessary unless a new shroud is installed.

Power Supply (#3) To remove, take off the power supply cover (#10), the card cage (#6), and remove the keyboard (#2), and disconnect the harness from the terminal strip on the power supply. Now lift up the front of the terminal so that you can see the underside of the unit. Remove the 4 countersunk screws near the hole for the fan and set the unit down. You may now slide the power supply out the front, twisting it slightly as you do to clear the keyboard mounting bracket.

Card Cage (#6) To remove, take out the 2 screws on the outside of the card cage and loosen the 2 screws on the side closest to the monitor. Now slide card cage forward and lift up. The harnesses are long enough so that the card cage can be laid next to the terminal with the backplane accessible. To disconnect the harness from the card cage remove hold down brackets on either side of the access window and pull out connectors.

Lamp and Switch Bracket (#4) To remove, lift up the front of the terminal until you can see the bottom. Remove 3 screws and the mounting plate and set the unit back down. Now lift the bracket up and lay it on top of the keyboard. Disconnect the harness from the terminal strip and remove the assembly.

Backpanel (#9) The chassis supporting the CRT and the card cage must be removed. Five screws, 2 on each end and one in the middle must be removed; then disconnect the CRT connector and the connectors to the card cage. Then lift the entire chassis assembly out. You can now access the back panel.

6. TROUBLE-SHOOTING CHART

A trouble-shooting chart is presented, at the module replacement level. All possible faults can obviously not be listed, but fault diagnosis to the suspect module(s) or subassembly will be facilitated by reference to the chart.

In cases where the cause of a symptom cannot be summarized in a brief phrase the column labeled "Probable Cause" has no entry, but the module(s) or subassembly to be replaced is listed.

> Turn Power OFF before
>
> removing or inserting
>
> a Printed Circuit card.

It is essential that, if a defective card has apparently been found, it be reinserted to verify that the symptoms reappear. If the symptoms do not reappear, the fault could have been corrosion on edge connector contracts or a temperature sensitive I.C. chip. It may be necessary to bring the device back to the operating temperature at which symptoms were first observed to find such chips.

On page 6-2a list of equipment and parts for servicing at both the module replacement level and the chip level is given.

SERVICE EQUIPMENT AND PARTS

Minimum and Optional

Spare Parts

1. P.C. Cards (Card complement per Locator Chart in Section 5).
2. 1 1/2 amp SloBlow fuse.
3. Power Supply - optional.
4. Spare chips - optional.

Tools

1. Phillips head screw driver, medium and small, w/long shank.
2. Flat screw driver, medium and small.
3. Card extractor
4. Video monitor
5. Extender card - optional
6. Cutters - optional
7. Pliers - optional
8. Soldering iron/solder -optional
9. Solder wick - optional
10. Oscilloscope - optional
11. Trouble lite - optional
12. VOM - optional
13. Frequency counter - optional

TROUBLE-SHOOTING CHART

Trouble	Probable Cause	Remedy or Bad Board
Power Light fails to come on when Power ON switch pressed	a) AC power b) fuse c) faulty switch d) faulty light	a) check receptacle b) replace 1 1/2 amp-ere "slo-blo" fuse c) replace switch d) replace lamp
Fan fails to come on when Power lamp is ON.	a) faulty fan	a) replace fan
Picture fails to appear after warm-up time. Power light and fan OK.	a) poorly adjusted contrast or brightness b) poorly seated P.C. cards c) d) power supply faulty	a) adjust contrast and/ or brightness b) remove shroud and check card seating c) VIDGEN card d) check for shorts or replace supply
Picture fails to appear on screen but does appear on external monitor	a) poorly adjusted contrast or brightness b) c) faulty Bright-ness or Contrast pots d) loose connector on monitor e)	a) adjust controls b) remove shroud (Consul series) and replace P.C. card on internal monitor chassis c) replace pots d) remove shroud and check connector on rear of monitor (Consul series) e) VIDGEN card
Screen comes up blank after Power ON and no characters may be entered, but cursor moves with cursor movements		a) ASYNC/FE b) CONTROL

Trouble	Probable Cause	Remedy or Bad Board
Screen comes on full of random characters	a) Power on reset circuitry faulty b) Power down too short	a) replace ASYNC/FE b) cycle power Sw.
Unit gets hot and shuts down	a) blocked fan b) stopped fan c) power supply malfunction or thermal cutoff	a) clear b) clear or replace c) replace power supply
All " " on screen "?" or "@" on 1/3 or more of screen		a) MEMORY b) CONTROL c) OPTION
Characters distorted by extra dots in character field	b) low +5V supply	a) CONTROL card b) adjust +5V or replace
Characters aren't recognizable but may be altered by keying from keyboard	b) low +5V supply	a) CONTROL card b) adjust +5V or replace
All positions on screen appear black w/narrow white boarders		a) CONTROL card
Certain groups of characters can't be entered on screen		a) ASYNC/FE b) MEMORY c) Keyboard replacement
Black vertical line appears in middle of screen with data running up screen		a) VIDGEN card
Screen torn and distorted	b) faulty monitor c) 50 or 60 cycle operation jumpers incorrect	a) VIDGEN card b) replace monitor c) correct as per description on VIDGEN schematic

Trouble	Probable Cause	Remedy or Bad Board
Characters have missing horizontal lines		a) VIDGEN b) CONTROL
Characters appear in Right or Left Margin		a) VIDGEN
Page on screen wrong in horizontal or vertical size		a) VIDGEN b) adjust TV monitor
Cannot move cursor		a) replace keyboard b) CONTROL c) VIDGEN
Cursor moves erratically	b) noisy keyboard c) +5V supply low	a) VIDGEN b) keyboard replacement c) adjust +5V
One cursor control fails to work	c) faulty keyboard	a) VIDGEN b) CONTROL c) check cable, replace keyboard if faulty
REPEAT key fails to operate	b) faulty keyboard	a) CONTROL b) check cable, replace keyboard if faulty
No cursor visible, but data on screen		a) VIDGEN b)
Cannot enter data	a) full duplex switch in FDX position b) modem off line but plugged into EIA connector c) faulty keyboard d) switch 2 on e) ASYNC/FE	a) switch to HDX (release switch) c) keyboard replacement d) turn switch off e) ASYNC/FE

Trouble	Probable Cause	Remedy or Bad Board
CR or ERASE fills rest of line or whole screen with some characters other than space		a) MEMORY
Data from keyboard is entered in wrong lines sometimes		a) VIDGEN b) MEMORY
Characters sometimes not entered on screen or missing from words		a) keying in too fast
Characters appear to be entered incorrectly in 1/3 of screen		a) MEMORY
Characters appear to be entered incorrectly in all of screen		a) MEMORY b) ASYNC/FE c) Keyboard
Cursor address operates but cursor goes to wrong location		a) CONTROL
Cursor Address function fails to operate		a) CONTROL
Line Address operates but cursor goes to wrong line		a) VIDGEN
Line Address function fails to operate		a) VIDGEN

Trouble	Probable Cause	Remedy or Bad Board
Carriage Return fails to operate properly		a) CONTROL
Characters don't scroll up screen		a) MEMORY b) CONTROL
Once data scrolls it doesn't stop; keeps scrolling		a) CONTROL
Data changes when shifting from bottom 1/3 to middle third or from middle third to top third of screen		a) MEMORY
Printer fails to	a) Power-ON indicator will show "ON" even though Printer is not plugged into AC outlet. Check by pushing LF button b) Not in PRINT ON mode c) not plugged into terminal d) faulty printer	a) plug in and check printer b) press PRINT ON c) plug into terminal d) replace printer
Characters to Printer not the same as on screen		a) MEMORY b) bad printer
Printer fails to CR after printing only one character on a line when new line sent from terminal	a) printer out of adjustment	a) refer to Printer Manual
Printer returns to next line before the terminal has finished sending a given line	a) printer out of adjustment	a) refer to Printer Manual

Trouble	Probable Cause	Remedy or Bad Board
EIA output data doesn't operate	a) bad cable b) wrong baud rate	a) repair cable b) correct setting c) ASYNC/FE d) "Clear to Send" false
EIA data input doesn't operate but output operates	a) cable wrong b) wrong baud rate	a) replace cable b) correct setting c) ASYNC/FE
EIA interface operates but current loop doesn't	a) cable wrong b) wrong baud rate c) SW E1,2 ON ASYNC/FE d) loop polarities reversed	a) replace b) correct setting c) ASYNC/FE Switch ON d) reverse polarity
Data to EIA device or from EIA device has high error rate but EIA device check OK	a) baud rate wrong b) frequency of baud rate incorrect	a) correct setting b) replace ASYNC/FE card or adjust frequency
Terminal is hung up and one can't enter anything on screen	a) EIA cable plugged in with no device attached or power off	a) unplug cables
CARRIER light fails to come on but EIA appears to function	a) lamp bad b) EIA cable wrong c) ASYNC/FE	a) replace lamp b) check Carrier Detect signal c) replace ASYNC/FE
" " written on screen	a) parity error b) framing error	a) set switches on ASYNC/FE as per schematic b) check EIA device

Trouble	Probable Cause	Remedy or Bad Board
Character insert/ Delete do not work at all		a) OPTION b) Keyboard
Character Insert/ Delete do not work in 1/3 screen		a) MEMORY
Line Insert/Delete do not work		a) OPTION b) MEMORY c) CONTROL
Horizontal tabbing does not work	a) No tab clock (TABCL*)	a) CONTROL
Cursor does not tab to the correct tab positions		a) VIDGEN
Terminal does not enter graphics mode with Y^C		a) CONTROL
Graphic elements are of different size or are placed wrong		a) OPTION
Data does not slow blink between the symbols { and }		a) VIDGEN
XMIT or Q^C does not cause the terminal to READ		a) ASYNC/FE b) CONTROL
Terminal does not stop transmitting in either MESS or PAGE mode		a) ASYNC/FE

Trouble	Probable Cause	Remedy or Bad Board
Trailing blanks are not suppressed by the terminal during READ		a) MEMORY
Terminal does not enter into transparent mode, i.e., control codes cannot be written into the MEMORY		a) CONTROL
Buried control codes remain displayed even if CONTROL key is not depressed		a) VIDGEN
Terminal does not top transmitting : C^C buried in the MEMORY		a) MEMORY b) ASYNC/FE
Terminal hangs when the hard copy interface is connected	a) No "Printer Busy" signal from the Printer	a) Put Printer ON b) Parallel switch on the rear panel ON c) OPTION
No data flow to serial printer	a) Printer is not enabled b) No hard copy clock	a) Put the "serial" switch on the rear panel ON b) OPTION
Incorrect data to the serial printer	a) Wrong baud rate	a) OPTION
No hard copy current loop	a) Loop is open	a) Close switch 2 on OPTION card
No local Print mode		a) OPTION

7. POWER SUPPLY SUBASSEMBLY

This section describes the power supply used in the ADDS Consul series of desktop terminals and the MRD series of rack-mountable equipment. Except for minor variations, the same power supply is used in all Consul and MRD units.

The variations are:

a) Power Transformer - The type of transformer used in the power supply depends on whether the supply is to be installed in a Consul or an MRD.

b) Fan Placement - An exhaust fan is mounted integrally in power supply subassemblies used in Consul terminals. For MRD equipment the exhaust fan is not on the power supply subassembly but is mounted on the rear panel of the MRD instead.

7.1 Power Supply Specifications

7.1.1 Input Voltage

105-125 VAC/210-250 VAC (strapping option)

7.1.2 Input Frequency

47-63, 400 Hz

7.1.3 Input Breakout

Below 100/195 VAC

7.1.4 Outputs

(a)	+5.2 VDC ±10%	@ 6.75 A continuous
(b)	+13.2 VDC	@ 0.5 A continuous
(c)	-13.2 VDC	@ 1.0 A continuous

7.1.5 Regulation

Line: ±0.5% Low Line to High Line for both 115V and 230 VAC

Load: ±0.5% No Load to Full Load

7.1.6 Ripple

10 mV RMS max

30 mV Peak to Peak max.

7.1.7 Overload Protection

All outputs protected by individual foldback circuits against continuous overloads and short circuits. Automatic recovery upon removal of overload condition.

7.1.8 Overvoltage Protection

Individual crowbars for each output: +5.2 VDC output to be preset between +6.50 and +7.5 VDC.
The +13.2 VDC and -13.2 VDC outputs will be preset between 15.0 and 17.0 VDC.

7.1.9 DC Output Adjust

The 5.2 VDC output is settable by means of a Cermet potentiometer to ±10% of nominal. The +13.2 VDC and -13.2 VDC outputs are set by fixed resistors to ±2% of nominal.

7.1.10 Temperature Coefficient and Stability

T.C.: 0.02%/°C

Stability: 0.1% for any 8 hour period after 30 min. stabilization.

7.1.11 Operating Temperature

-20°C to +85°C

7.1.12 Storage Temperature

-55°C to +85°C

7.1.13 Overtemperature Protection

Thermostat protection provided to turn off AC input in the event ambient temperature goes beyond 75°C. Heatsink temperature protected at 100°C to 108°C.

7.1.14 Fusing

To protect the power supply from internal faults an input fuse should be used. For 115V input a 1.5 A Slo-Blow fuse is recommended. A 0.75 A Slo-Blow fuse must be used for 230V input.

7.1.15 P.C. Boards

P.C. Boards should be easily field replaceable without desoldering.

7.1.16 Humidity

The operating range is 0-95% R.H., non-condensing.

7.2 Theory of Operation

7.2.1 General Power Supply Description

The power supply consists of three separate series regulators obtaining their power from a common transformer. All three regulators are basically the same in design and operation. Only the sensing, drive and series-pass circuit vary slightly. Each circuit has a full wave rectifier, filter capacitor, complete IC regulator, pass transistor, driver and overvoltage SCR crowbar.

Fold out the power supply schematic drawing, Figure 7.5 on pages 7- before proceeding to the circuit description below.

7.2.2 Circuit Description

7.2.2.1 Input Transformer

Input voltage of 115 or 230 VAC is applied to transformer T1; see schematic for proper jumper connection on transformer for 115 or 230 VAC operation. All input and output connections are made through terminal board TB1.

7.2.2.2 5 Volt Regulator Circuit

The center tapped transformer winding feeds rectifiers CR2 and CR3 and the rectified DC is filtered by capacitor C6. The filtered unregulated DC is then fed to the collector of series-pass transistors Q4, Q5 which product the proper voltage drop to keep the output regulated at the preset voltage. IC regulator A1 consists of voltage reference, error amplifier series-pass transistor and current limit circuit. The output voltage is connected directly to the inverting input. The referenced voltage is connected to a voltage divider R7, R8 and R9. The reference voltage is divided down to 5 V with potentiometer R8 and fed to the non-inverting input. The regulator will then automatically adjust and maintain the output voltage at the voltage set with potentiometer R8. R8 allows to vary the output voltage at least $\pm$ 10%. The output of the IC regulator feeds driver Q1 which controls passing transistors Q4 and Q5. Overload protection is provided by sensing the voltage drop across emitter resistor R18, R19 plus base-emitter voltage of Q4 and Q5. The sense voltage is picked up through voltage divider R5, R6 and is fed to the IC regulator in such a manner that drive to Q1 is removed in case excessive current is drawn.

In case of a short circuit only a fraction of the nominal output current can be drawn. The input to A1 is fed from the +13.2 V output, because the IC regulator requires a voltage several volts greater than its output. Therefore, the +5 V circuit depends on the presence of the +13.2 V output.

7.2.2.3 +13 and -13 V Regulator Circuit

Both circuits are identical except for the pass transistor drive circuits. The transformer secondary winding feeds rectifiers CR6 and CR7 and the rectified DC is filtered by capacitor C7. The filtered, unregulated DC is then fed to the collector of series-pass transistor Q6 which produces the proper voltage drop to keep the output regulated at the preset voltage.

Except for the sensing bridge, the 13V circuits operate exactly like the 5V circuit described above. The reference voltage from pin 4 of IC A1 is fed directly at the non-inverting input pin 3. R9, 10 and 11 is a voltage divider, dividing the output voltage down to same level as the reference voltage (approx. 7.15V). This sample of the output voltage is then fed to the inverting input pin 2. Jumpers J2 and J3 across R11 are used to set the output voltage to within ±2%. The -13.2 output has its own rectifier-filter circuit (CR10-CR13, C8). The positive output terminal is connected to the output common.

7.2.2.4 Overvoltage Crowbar Circuit

Silicon controlled rectifiers Q8, Q9 and Q10 are connected across the outputs of each of the three regulators. Zener diode VR2, R14, R15 and R17 form a sensing bridge to detect an overvoltage. Q2 is normally not conducting. In case of an overvoltage Q2 will turn on and fire the SCR which causes the output voltage to drop. All three overvoltage circuits work in the same fashion.

7.3 Operating Notes

Connections to the power supply are made through the appropriate terminals on the terminal board. The output voltages are factory pre-set. (The +5V output can be adjusted with potentiometer R8.)

The power supplies are designed to operate with forced air. Should the fan fail or airflow be severely restricted, the heatsink will get excessively hot and the thermostat K1 will open, interrupting input power. Operation will continue after the power supply has sufficiently cooled off. If this should occur, operation should be discontinued until proper air flow is restored.

Similarly, a short in the terminal backplace wiring could cause the power supply to shut down. If this is suspected disconnect the output leads (+5.2 VDC, +13 VDC, -13 VDC) from the barrier strip on the power supply and observe whether or not the output voltages at the barrier strip come up to the correct value with the harness to the terminal electronics disconnected. If so, there is a short fault in the power supply itself.

7.4 Maintenance

7.4.1 General

This section describes trouble analysis routines and test procedures that are useful for servicing the power supply. A chart is provided for trouble shooting. Refer to section 7.1 for minimum performance standards.

7.4.2 Trouble Analysis Procedures

Whenever a problem develops, systematically check all fuses, primary power connections, external circuit elements, and external wiring before trouble shooting the equipment. Failures and malfunctions often can be traced to simple causes such as improper jumpers and supply load connections or fuse failure. Use the schematic diagram as an aid to locating trouble causes. The voltage chart contains various circuit voltages that are averages for normal no-load operation. Use measuring probes carefully to avoid causing short circuits and damaging circuit components.

7.4.3 Checking Transistors and Capacitors

Check transistors with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohm-meter that has a highly limited current capability. Observe proper polarity for NPN transistors. The forward transistor resistance is low but never zero; backward resistance is always much higher than the forward resistance.

When soldering semi-conductor devices, hold the lead being soldered with pliers on a heat sinking device placed between the component and the solder joint.

NOTE: The leakage resistance obtained from a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most cases the capacitors are shunted with resistances some of which have low values. Only a dead short is a true indication of a shorted capacitor.

7.4.4 Printed Circuit Board Maintenance Techniques

Voltage measurements can usually be made from both sides of the board. Use a needle point probe or another suitable measuring probe.

Broken or damaged printed wiring is usally the result of an imperfection or strain. To repair small breaks, tin a short piece of hook-up wire to bridge the break and holding the wire in place, flow solder along the length of wire so that it becomes a part of the circuit.

When unsoldering components from the board never pry or force the part loose, use a solder-sucker to remove solder before loosening a component. If a solder-sucker is not available, use tinned copper braid or stranded wire (AWG 14 or 16).

7.4.5 Trouble Chart Description

The trouble chart is intended as a guide for locating trouble causes, and is used along with the schematic.

The operating conditions assumed for the trouble chart are as follows:

(a) AC power of proper voltage and frequency is present at the input terminals.

(b) All loads have been removed.

7.4.6 Typical Voltages

Voltage readings taken at nominal AC line voltage and no load.

T1	7-12	18.5 VAC
	5-6, 5-11	10.4 VAC
	8-13	19.2 VAC
C6		14.3 VDC
C7		24.5 VDC
C8		26.2 VDC
C1		-
Com. output -	PC1/A1-4	6.8- 7.5 VDC
" "	PC2/A1-4	6.8- 7.5 VDC
-13 output -	PC3/A1-4	6.8- 7.5 VDC
	PC1/VR2	3.3 VDC
	PC2/VR2	5.6 VDC
	PC3/VR2	5.6 VDC
Com. output -	PC1/Q1 base	6.35VDC
" " -	PC2/Q1 base	14.45VDC
-13V output -	Q7 base	13.8 VDC
Com. output -	Q4 base	5.6 VDC
" "	Q6 base	13.8 VDC

7.4.7 Trouble Chart

Symptoms	Probable Cause	Remedy
1. No output voltage	K1 open	Replace K1 if it does not reset when cool.
	T1 defective	Check T1 for proper output voltage; replace.
	A1 defective	Replace if no output on pin 6 or no reference voltage on pin 4.
2. Low Output Voltage	Q1 open	Check & Replace.
	Q4,5 Q6 Q7 open	Check & Replace.
	CR2,3 CR6,7 (8,9) defective CR10-13	Check & Replace.
	C4 shorted	Check & Replace
	SCR fired	Raise input voltage slowly and check if OV ckt. crowbars at the right voltage. If yes, check output too high. Check for shorted SCR.
3. Output Voltage too High. Note: High output may activate OV-circuit	Q4,5, Q6,Q7 shorted	Check & Replace
	A1 defective.	Check & Replace
4. High Ripple & Unregulated DC.	AC input voltage too low.	Check AC line voltage.
	Open Rectifier CR2-13	Check & Replace
	Excessive Load.	Check Load Current.

Notes:

(a) The +5 Volt output depends on +13 Volt. Check +13V output before trouble shooting +5V output.

(b) High output may activate OV. crowbar. Trouble shoot with reduced input voltage. (Use variable transformer to keep output voltage below trip voltage.)

(c) If trouble is suspected to be on PC board, replace entire board if one is available.

7.4.8 Power Supply Drawings/Photographs

Presented on following pages are:

Figure 7.1 - A photo of the Consul power supply.

Figure 7.2 - A photo of the MRD power supply.

Figure 7.3 - Photos of the three P.C. boards on the power supply.

Figure 7.4 - Diagram of harness connection to power supply barrier strip.

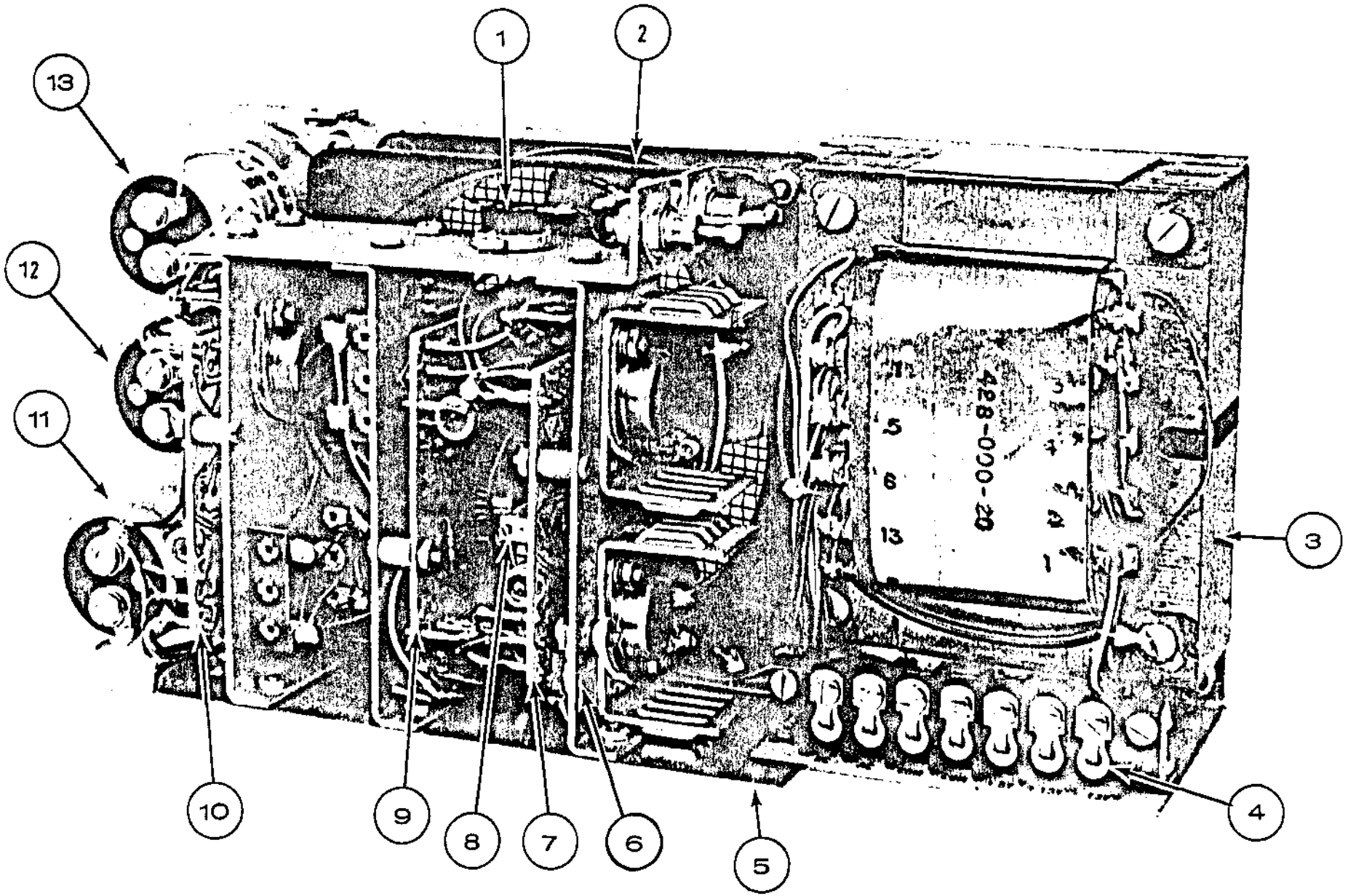
Figure 7.5 - Power Supply schematic drawings.

In Figures 7.1 and 7.2, the major components identified are as follows:

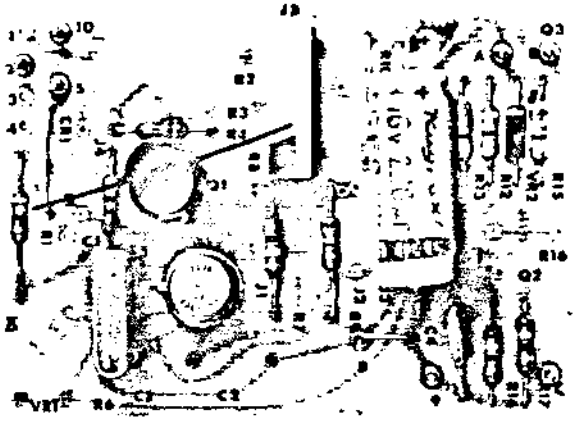
1. Thermostat
2. Fan
3. Power Transformer (T1)
4. Terminal board (TB1)
5. Chassis
6. Heat sink bracket
7. +5 VDC P.C. board (PC1)
8. Potentiometer (+5V adj)
9. -13.2 VDC P.C. Board (PC3)
10. +13.2 VDC P.C. Board (PC2)
11. Filter capacitor (C6)
12. Filter capacitor (C7)
13. Filter capacitor (C8)

CONSUL SERIES POWER SUPPLY, 285-002

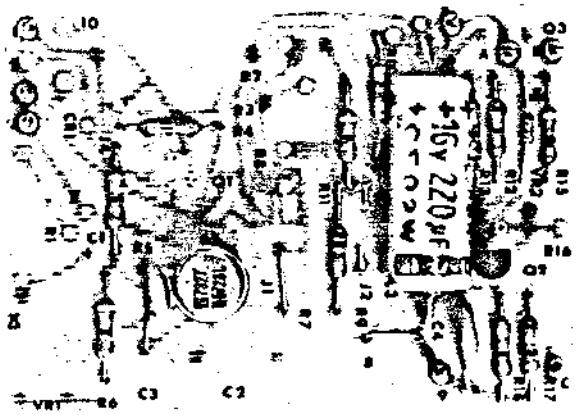
Fig. 7-1



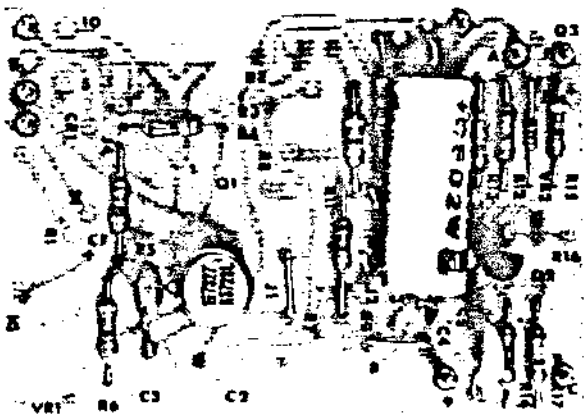
P.C. BOARDS, POWER SUPPLY
Fig.7·2



+5VDC · PC1 · 360·110



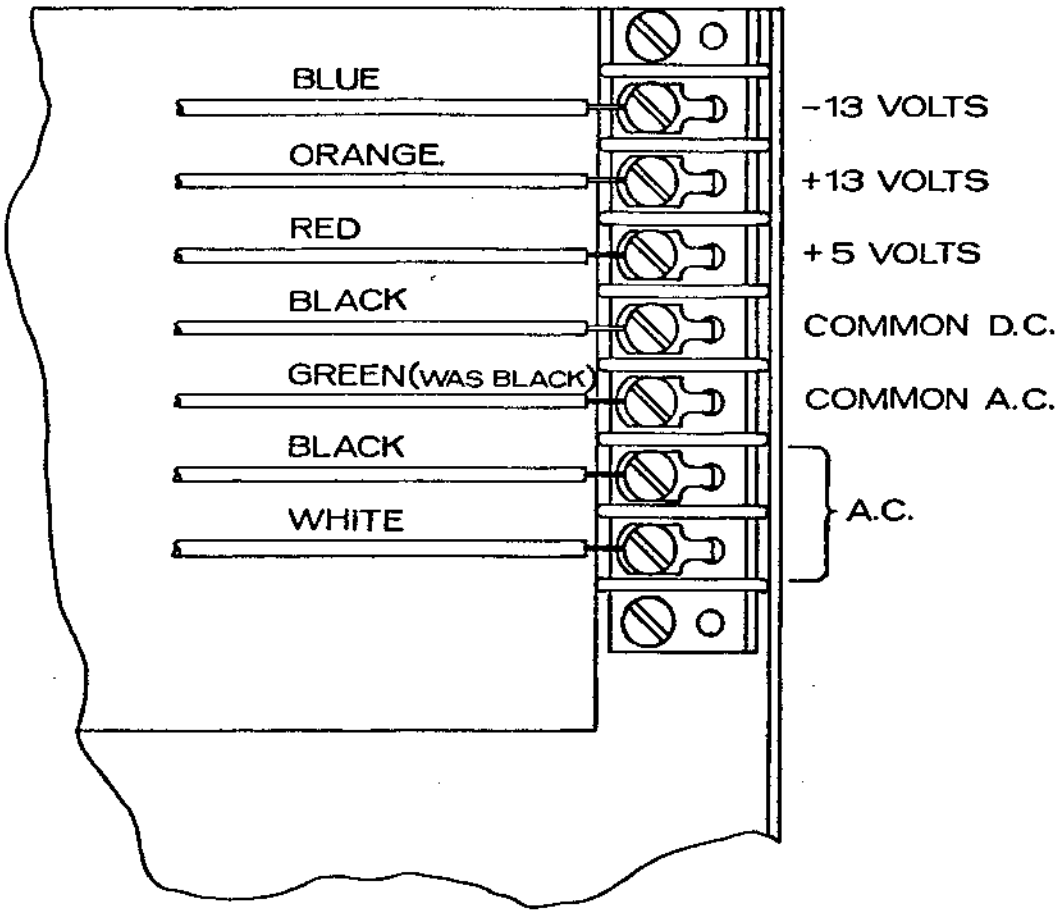
+13.2VDC · PC2 · 360·132



−13.2VDC · PC3 · 360·115

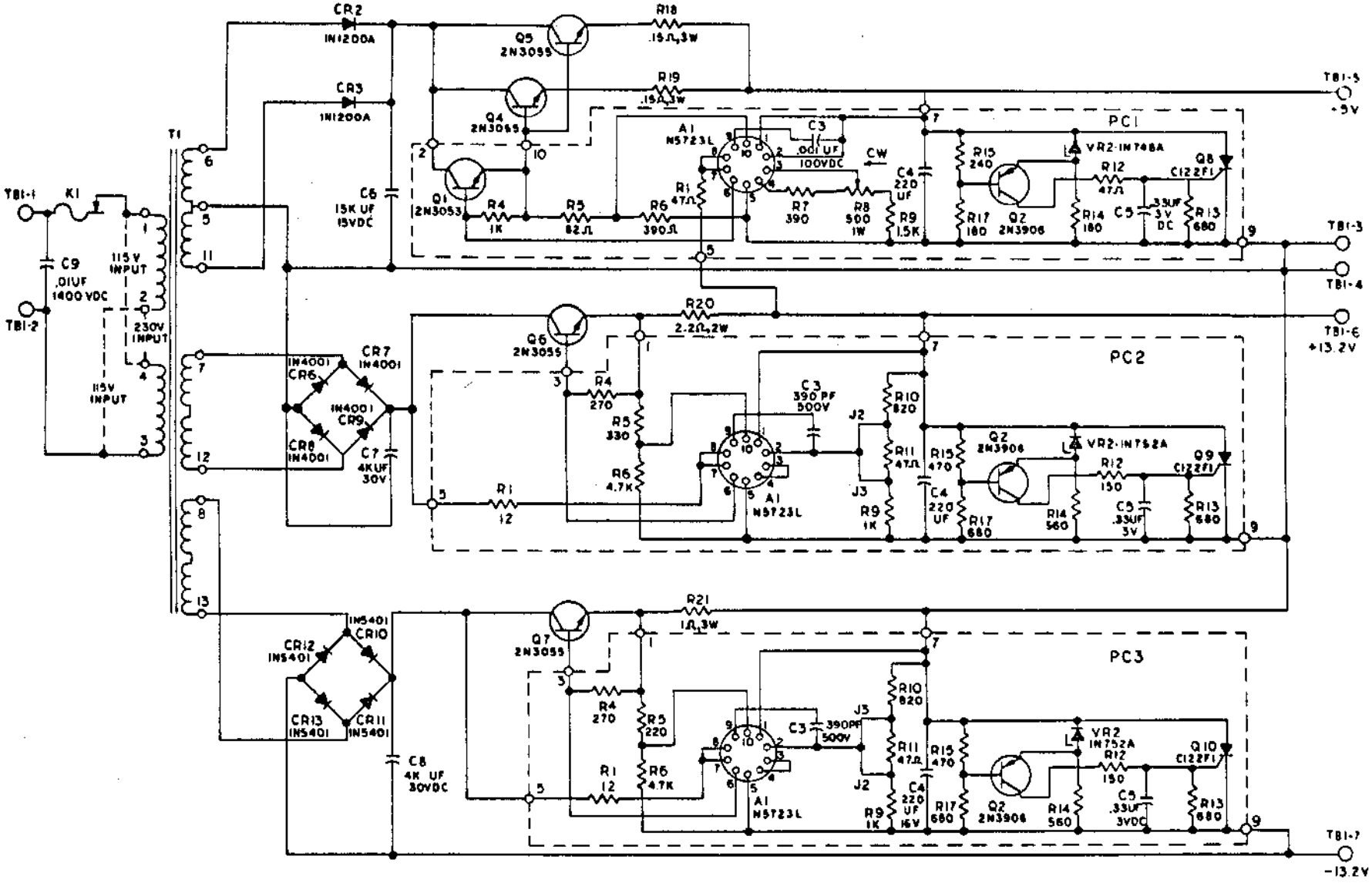
POWER SUPPLY TBI CABLE HOOK-UP

Fig. 7-3



SCHEMATIC DIAGRAM, POWER SUPPLY, 285-002

Fig. 7-4



NOTE
UNLESS OTHERWISE SPECIFIED
RESISTORS ARE 1/4W, 5%

7.5 Power Supply Bill of Material

A complete B.O.M. of the Power Supply is given in following pages.

Note that for certain parts, ADDS is the sole supplier. However, most parts are "off-the-shelf" and have a standard manufacturer's part number listed.

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	NOTES.
1	502-010	1	ASS'Y. POWER SUPPLY		
2	285-002	1	POWER SUPPLY ASSEMBLY	POWER PAC 417-000-91	
3	502-003	1	ASS'Y. PLENUM		
4	502-714	1	COVER, POWER SUPPLY		
5	502-733		SCREEN, FAN		
6	825-0012	1	FAN	IMC-WS2107FL-2R	
7	810-005	11	6-32 x 5/16 SCREW	SEMS	
8	810-010	4	6-32 x 3/4 SCREW, P.H. PHILLIPS,	SEMS	
9	790-008	2	6-32 FLAT WASHER, CRS, CAD PLATE		
10	360-089	AR	CATERPILLAR INSULATOR TRACK		
11	360-023	1	CABLE CLAMP	WECKESSER #5/32J	

PREPARED	P. George	11-7-73	TITLE ASS'Y. POWER SUPPLY			ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 502-010	REV. A	SHEET 2 OF 2	
APPROVED						

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	285-002	1	TOP ASSY. POWER SUPPLY +5.0 VDC ADJUSTABLE,	POWER PAC 417-000-91	
			+13.2 VDC AND -13.2 VDC		
2		1	MAIN CHASSIS		
3	360-110	1	P.C. BOARD +5.0V	ADDS	PC-1
4	360-115	1	P.C. BOARD -13.2V	ADDS	PC-2
5	360-132	1	P.C. BOARD +13.2V	ADDS	PC-3

PREPARED			TITLE TOP ASSY - POWER SUPPLY		
CHECKED			DWG. NO. 285-002	REV. A	SHEET 1 OF 5
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	CHASSIS		
2		2	BRACKET-P.C. BOARD		
3		1	BRACKET-P.C. BOARD		
4		1	BRACKET RECTIFIER		
5		2	HEAT SINK - T03	STAVER 65	
6		3	TERMINAL STRIP	CINCH-JONES 52A	
7		4	TERMINAL STRIP	CINCH-JONES 52	
8		3	CAPACITOR CLAMP	SPRAGUE 4586-97A	
9		1	TERMINAL BLOCK	CINCH-JONES 7-140Y	TB1-1
10	350-008	1	TRANSFORMER	ADDS	T1
11		2	RIGHT ANGLE BKT'S	H.H. SMITH 1446	
12		6	FIBER STANDOFF	H.H. SMITH 8886	
13	140-087	1	ELECT. CAP 15K uf, 15 VDC	SPRAGUE 36DX153G015AB2	C6
14	.140-088	2	ELECT. CAP 4K uf, 30 VDC	SPRAGUE 36DX402G030AA2	C7,C8
15		2	RECTIFIER-STUD MOUNT	INT. RECT. CORP. 1N1200A	CR2,CR3
16		4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N4001	CR6 thru CR9
17		4	RECTIFIER-AXIAL LEAD	PWR. COMP. 1N5401	CR10 thru CR13
18		1	THERMOSTAT	KLIXON 20700	K1
19	330-010	4	TRANSISTORS-T03	MOTOROLA 2N3055	Q4 thru Q10
20		1	CAPACITOR-AC .01 uf, 1400 VDC	DIELECTRON ULR1400DC	C9
21		3	SCR	G.E. C122F1	Q8 thru Q10
22		2	RESISTOR W.W. .15ohm 3W	CLAROSTAT CC3L	R18,R19
23		1	RESISTOR W.W. 2.2 ohm 2W	IRC BWH	R20
24		1	RESISTOR W.W. 1.0 ohm 3W	CLAROSTAT CC3L	R21
25		1	MARKING STRIP-VOLTAGE DESIGNATION		
26					

PREPARED	I.C. Serra	11/3/73	TITLE MAIN CHASSIS - POWER SUPPLY			ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO.	REV. A	SHEET 2 OF 5	
APPROVED						

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	360-110	1	PRINTED CIRCUIT BOARD, +5 V	ADDS	PC-1
2		1	CAPACITOR .001 uf 100VDC	SPRAGUE 225	C3
3		1	CAPACITOR 220 uf 16VDC	RAYREX RADY 220 PY01605	C4
4		1	CAPACITOR .33 uf 3VDC	DIELECTRON RT3	C5
5		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R1
6		1	RESISTOR 1K ohm 1/4W ± 5%	ALLEN BRADLEY EB	R4
7		1	RESISTOR 82 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R5
8		1	RESISTOR 390 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R6
9		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
10		1	RESISTOR 680 ohm 1/4W ± 5%	ALLEN BRADLEY EB	R13
11		1	RESISTOR 180 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
12		1	RESISTOR 390 ohm 1/4 W	R-OHM R-25	R7
13		1	RESISTOR 270 ohm 1/4 W	R-OHM R-25	R15
14		1	RESISTOR 180 ohm 1/4 W	R-OHM R-25	R17
15		1	RESISTOR 1.5K ohm 1/4W	R-OHM R-25	R9
16		1	POT 500 ohm 1 W	AMPHENOL 6034P-501-7310	R8
17	330-018	1	TRANSISTOR TO-5	RCA 2N3053	Q1
18	330-005	1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2
19		1	ZENER DIODE	MOTOROLA 1N746A	VR2
20		1	REGULATOR	SIGNETICS N5723L	A1
21		1	TO-5 HEAT SINK	WAKEFIELD 296-1-AB	

PREPARED	I.C. Serra	11/3/73	TITLE	CONSUL POWER SUPPLY		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 360-110	REV. A	SHEET 3 OF 5	
APPROVED						

BILL OF MATERIAL

ITEM	AD /N	QTY.	DESCRIPTION	MFR. P/N	ES.
1	360-110	1	PRINTED CIRCUIT BOARD, +13.2 V	ADDS	PC-2
2		1	CAPACITOR 390 pf 500V	DIELECTRON X5F	C-3
3		1	CAPACITOR 220 uf 16V	RAYREX RADY 220PY01605	C-4
4		1	CAPACITOR .33 uf 3 Volt	DIELECTRON RT3	C5
5		1	RESISTOR 270 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R4
6		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R11
7		1	RESISTOR 150 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
8		1	RESISTOR 680 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R13
9		1	RESISTOR 560 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
10		1	RESISTOR 4.7K ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R6
11		1	RESISTOR 330 ohm 1/4 W	R-OHM R-25	R5
12		1	RESISTOR 1.K ohm 1/4 W	R-OHM R-25	R9
13		1	RESISTOR 470 ohm 1/4 W	R-OHM R-25	R15
14		1	RESISTOR 680 ohm 1/4 W	R-OHM R-25	R17
15		1	RESISTOR 820 ohm 1/4 W	R-OHM R-25	R10
16		1	ZENER DIODE	MOTOROLA 1N752A	VR2
17		1	REGULATOR	SIGNETICS N5723L	A1
18		1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2

PREPARED	J.C. SERRA	11/3/73	TITLE CONSUL-POWER SUPPLY			ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 360-132	REV. A	SHEET 4 OF 5	
APPROVED						

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	Ref. DES.
1	360-110	1	PRINTED CIRCUIT BOARD -13.2 V	ADDS	PC-3
2		1	CAPACITOR 390 pf, 500VDC	DIELECTRON X5F	C3
3		1	CAPACITOR 250 uf, 16 VDC	RAYREX-RADY 220PY01605	C4
4		1	CAPACITOR .33 uf, 30 VDC	DIELECTRON RT3	C5
5		1	RESISTOR 270 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R4
6		1	RESISTOR 4.7K ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R6
7		1	RESISTOR 47 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R11
8		1	RESISTOR 150 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R12
9		1	RESISTOR 680 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R13
10		1	RESISTOR 560 ohm 1/4 W ± 5%	ALLEN BRADLEY EB	R14
11		1	RESISTOR 220 ohm 1/4 W	R-OHM R-25	R5
12		1	RESISTOR 1K ohm 1/4 W	R-OHM R-25	R9
13		1	RESISTOR 820 ohm 1/4 W	R-OHM R-25	R10
14		1	RESISTOR 470 ohm 1/4 W	R-OHM R-25	R15
15		1	RESISTOR 680 ohm 1/4 W	R-OHM R-25	R17
16		1	TRANSISTOR TO-92	NATIONAL 2N3906	Q2
17		1	ZENER DIODE	MOTOROLA 1N752A	VR2
18		1	REGULATOR	SIGNETIC N5723L	A1

PREPARED	I.C. Serra	11/3/73	TITLE	CONSUL POWER SUPPLY	ADDS	Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 360-115	REV. A	SHEET 5 OF 5	
APPROVED						

8. TV MONITOR SUBASSEMBLY

8.1 General Description

The TV monitor is a solid-state unit intended for use in industrial and commercial installations where reliability and high quality video reproduction are desired. It is packaged as a self-contained subassembly, complete with a power supply. The only electrical connections required to the monitor subassembly are AC power and horizontal and vertical video drive signals.

The monitor subassembly can easily be removed from your terminal by removing three nuts which old the unit on mounting studs and disconnecting the 10-pin edge connector and the AC power "Molex" connector. Note that re-centering the picture may be necessary when installing a new monitor. See Section 8.4.4 for details.

8.2 Specifications

8.2.1 Input Data Specifications

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory-Available) Printed circuit board card edge connector - Viking #2VK10S/1-2 or Amphenol #225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 47 to 63 pulses per second	Pulse Rate: 15,000 to 16,500 pulses per sec
Amplitude	Low = Zero $^{+0.4}_{-0.0}$ volts High = 4 + 1.5 volts		
Signal Rise & Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Figure 8.1		

8.2.2 Display Specifications

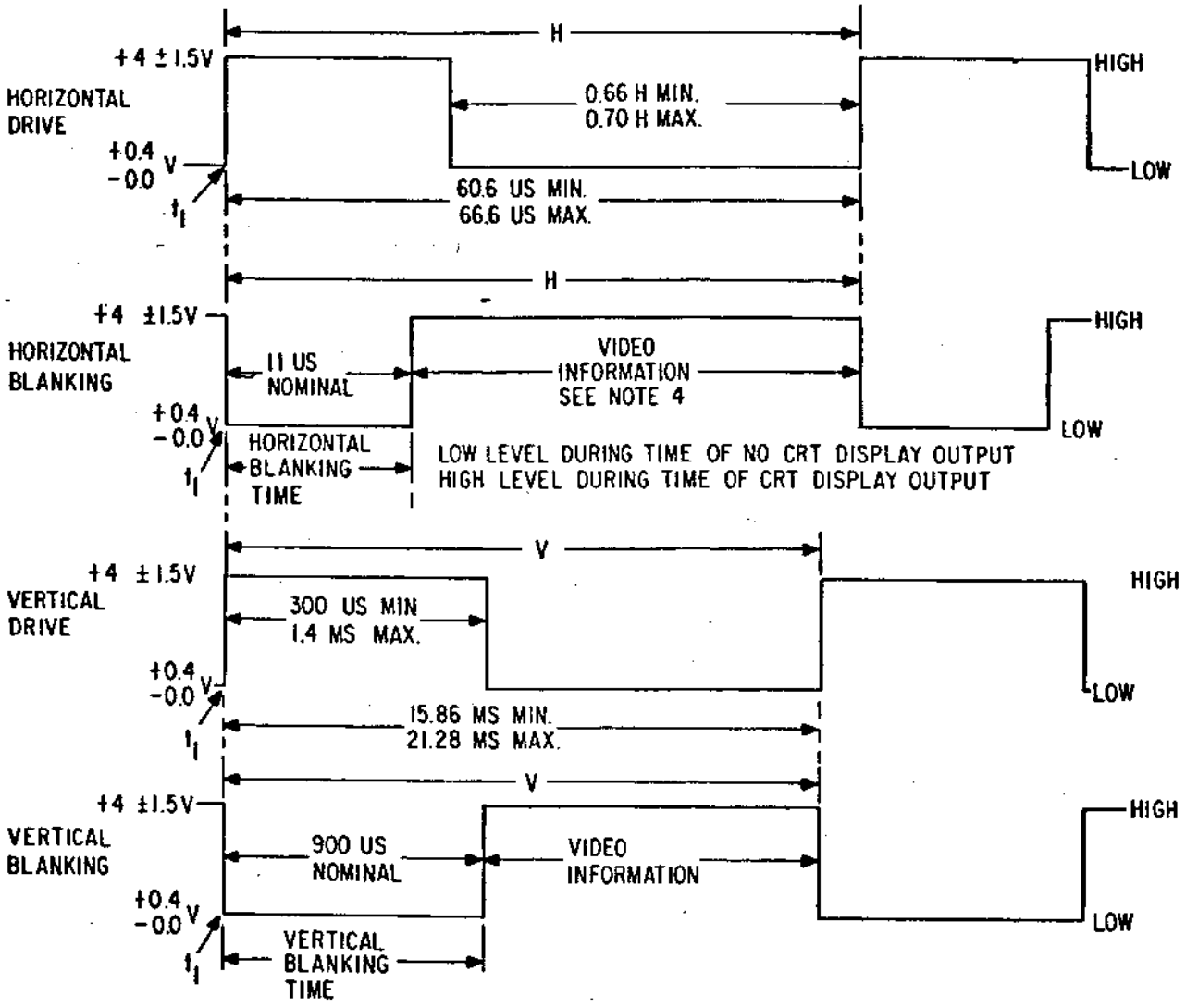
(a) Cathode Ray Tube

Nominal Diagnal Measurement: 12 inches

Phosphor: P4

SYNCHRONIZATION AND BLANKING SIGNALS

Fig. 8-1



NOTES

1. The leading edges of Drive and Blanking waveforms must start at time t_1. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

* Resolution (TV Lines): at center - 900 at 40 fL
at corner - 800 at 40 fL

*Resolution is measured in accordance with EIA RS 375, except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

b) Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within ± 1.5% of the rectangle height.

8.2.3 Power Requirements

Input Connector:	Receptacle, Molex #03-06-1041 supplied with unit. Mating plug is Molex #03-06-2041.
Input Voltage:	105 to 130 V rms (120V nominal; 50/60 HZ)
	Optional: 220/240 V rms ± 10%; 50/60 HZ.
Input Power:	24 Watts (nominal)
Output Voltages:	+15VDC (short circuit protected)
	+12 kV DC;

8.2.4 Environmental Specifications

a) Temperature

Operating Range: 5°C to 55°C
Storage Range: -40°C to 65°C

b) Humidity

5 to 80 percent R.H. (noncondensing)

c) Altitude

Operating Range: Up to 10,000 feet

8.2.5 X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78.

8.2.6 Controls

a) External Controls

(1) Contrast, 500 ohm potentiometer carbon composition 1/4 Watt.

(2) Brightness, 100 kilohm potentiometer 1/4 Watt.

b) Internal Set Up Controls

(1) Height

(2) Vertical Linearity

(3) Vertical Hold

(4) Focus

(5) Width

(6) Low Voltage Adjust

8.3 Theory of Operation

Fold out the monitor schematic drawing, Figure 8.2, before proceeding with the theory of operations. Figure 8.2 is located at the end of this section, on page 8- .

8.3.1 Video Amplifier

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101, operating as a class B amplifier, and its components comprise the video output driver with a gain of about 17.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

8.3.2 Vertical Deflection

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and capacitors C105 and C106 form an RC network providing proper timing.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CPT.

The vertical output stage. Q104, uses a power transistor which operates as a class A amplifier. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscilations by providing damping across the vertical deflection coils.

8.3.3 Horizontal Deflection

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. A positive going pulse is coupled through R127 to the base of Q105.

The driver stage is either cut off or driven into saturaction by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near to center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to change C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12kV, "C" VDC, and "B" VDC respectively. 12kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No.2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

8.3.4 Low Voltage Regulated Supply

The series-pass low voltage regulator is designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VAC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on.

Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition.

8.4 Adjustments

8.4.1 Vertical Adjustments

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

(1) Set the vertical frequency control, R116, near the mechanical center of its rotation.

(2) Adjust the vertical height control, R124, for desired height.

(3) Adjust the vertical linearity control, R121, for best vertical linearity.

(4) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

(5) Readjust the vertical frequency control, R116, until the picture rolls up slowly.

(6) Restore vertical drive to the monitor.

(7) Recheck height and linearity.

8.4.2 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

(1) Adjust the horizontal width coil, L101, for the desired width.

(2) Adjust the linearity sleeve under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

(3) Readjust L101 for proper width.

(4) Observe final horizontal linearity and width, and touch up either adjustment if needed.

8.4.3 Focus Admustment

The focus control, R107, provides an adjustment for maintaining best overall display focus.

8.4.4 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

8.5 Troubleshooting and Maintenance

8.5.1 List of Symptoms and Remedy

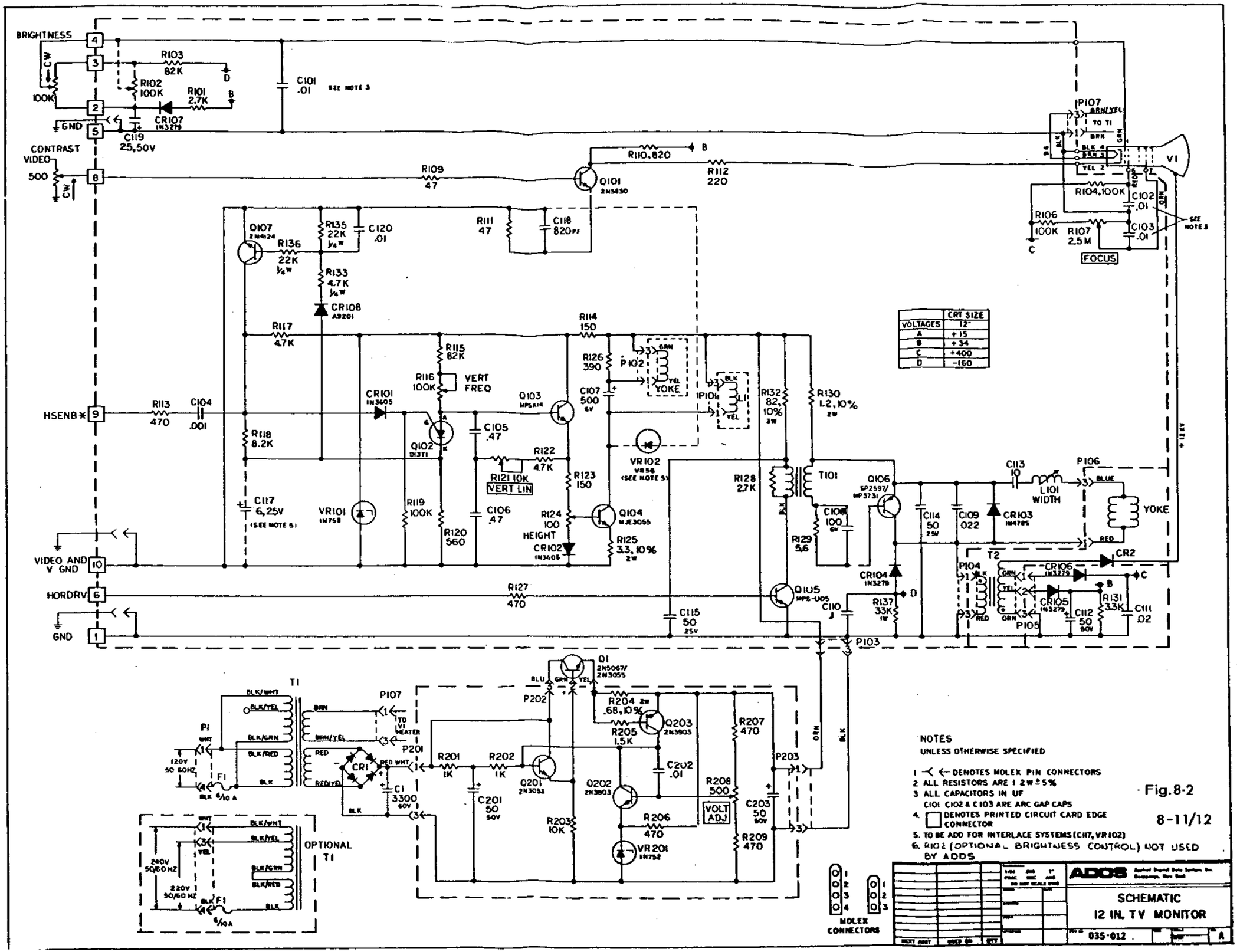
SYMPTOM	POSSIBLE REMEDY
a) Screen is dark	If an external monitor is available, plug it into the video connector at the rear of the terminal. If no picture appears on that monitor check the P.C. cards in the terminal bucket which generate horizontal and vertical drive (The VGA and VGB in the 800/700 series; the VG/GT card in the 580/380 series) If external monitor shows picture (or if you cannot check P.C. cards in terminal) proceed to step below. Check "A" bus Q106, Q105, CR2

b)	Loss of Video	CR105, Q101
c)	Power consumption is too high	Check horizontal drive waveform; Check proper placement of horizontal linearity sleeve; Q106, Q105
d)	Low voltage bus incorrect	Q202, Q203, Q1 Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

8.5.2 Supplementary Drawings

The following four pages show

- A schematic drawing
- Interconnecting cabling
- Important waveforms in the monitor subassembly
- Location of Circuit Board Components



	CRT SIZE
VOLTAGES	12"
A	+15
B	+34
C	+400
D	-160

NOTES
UNLESS OTHERWISE SPECIFIED

1. ⊣ ← DENOTES MOLEX PIN CONNECTORS
2. ALL RESISTORS ARE 1 2W ±5%
3. ALL CAPACITORS IN UF
   C101 C102 & C103 ARE ARC GAP CAPS
4. ☐ DENOTES PRINTED CIRCUIT CARD EDGE CONNECTOR
5. TO BE ADD FOR INTERLACE SYSTEMS (CII7, VR102)
6. R102 (OPTIONAL BRIGHTNESS CONTROL) NOT USED BY ADDS

Fig. 8-2

8-11/12

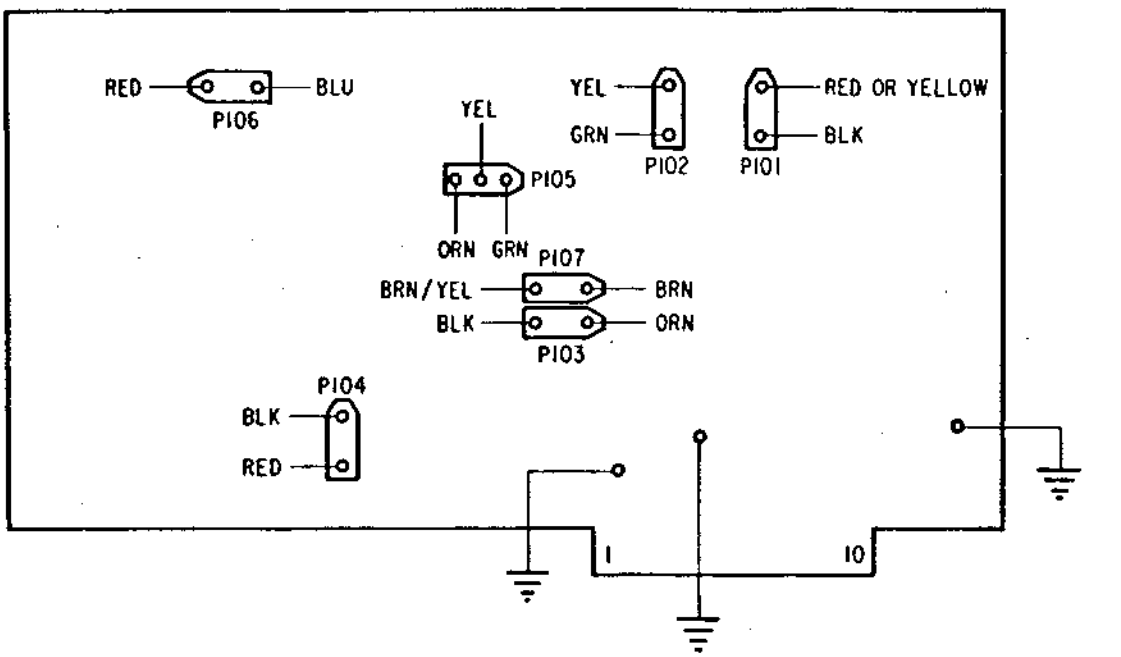
ADDS

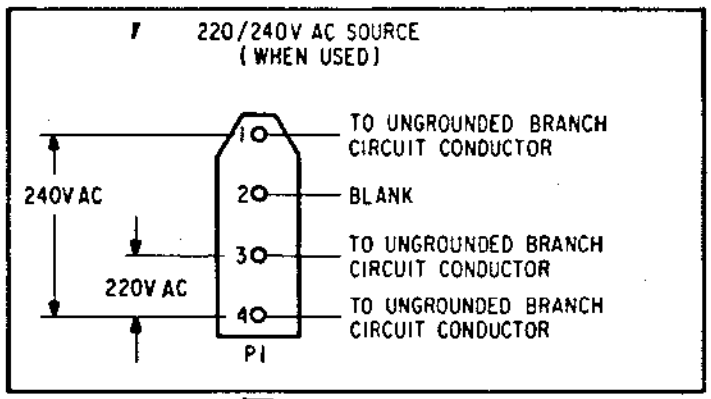
SCHEMATIC
12 IN. TV MONITOR

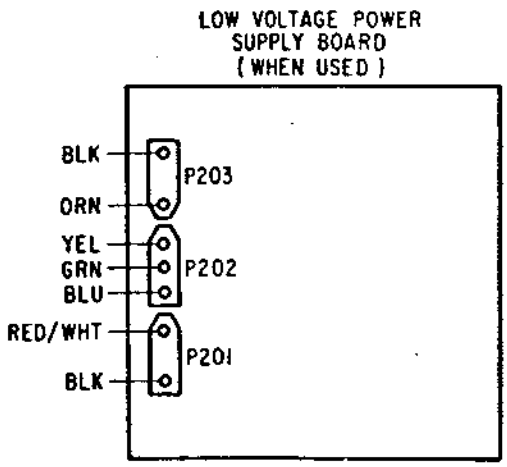
035-012 A

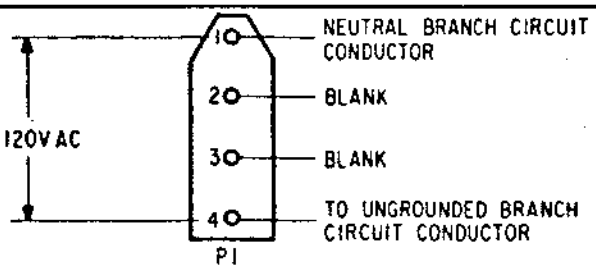
INTERCONNECTING CABLING

Fig. 8.3



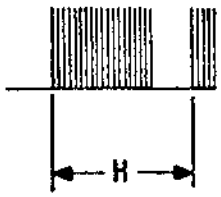




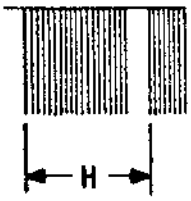


VOLTAGE WAVEFORMS
Fig. 8.4

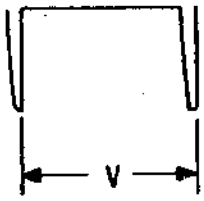
WAVEFORMS



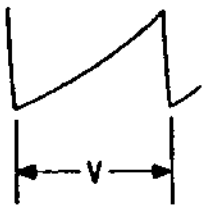
Q101-B
2.5V P-P



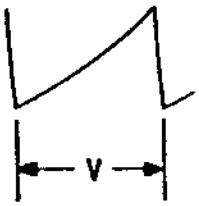
V1-CATHODE
20V P-P



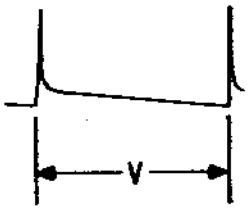
CR101-ANODE
3V P-P



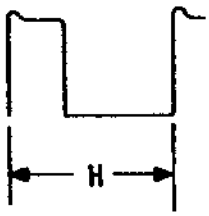
Q103-B
4.5V P-P



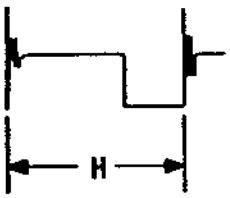
Q104-B
1.2V P-P



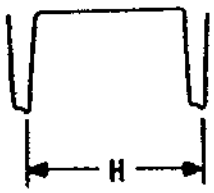
Q104-C
45V P-P



Q105-B
3V P-P



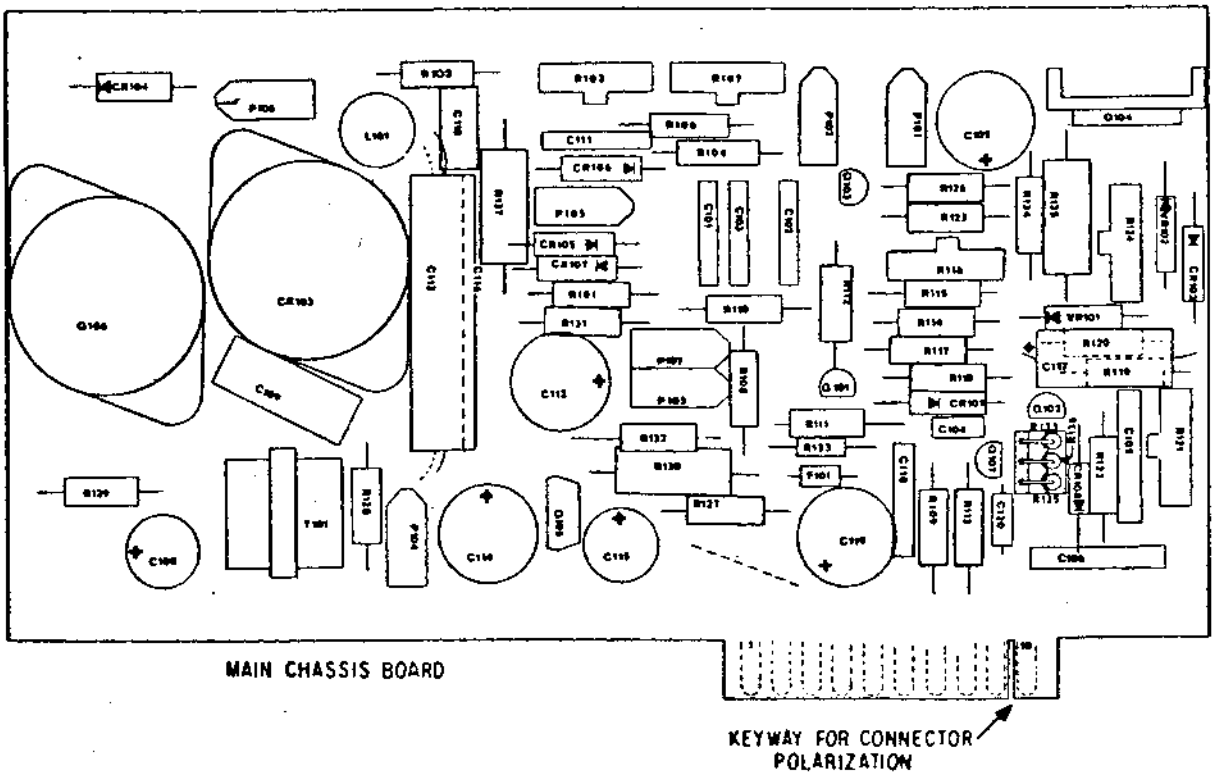
Q105-C
30V P-P



Q106-C
170V P-P

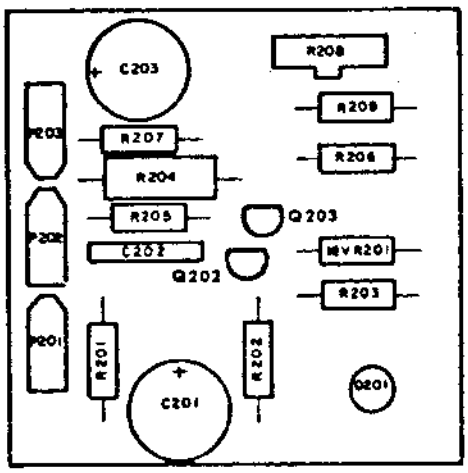
CIRCUIT BOARD COMPONENTS LOCATION

Fig.8.5



MAIN CHASSIS BOARD

KEYWAY FOR CONNECTOR POLARIZATION



LOW VOLTAGE POWER SUPPLY BOARD

8.6 TV Monitor Bill of Material

A complete B.O.M. of the TV Monitor is given in the following pages.

Note that for certain parts, ADDS is the sole supplier. However, those parts which are "off-the-shelf" have a standard manufacturer's part number listed.

EM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	CRT 12 INCH 90° P4 BONDED LONG NECK	1-014-0737	
2					
3		1	SLEEVE LINEARITY	1-023-5035	
4					
5		7	CONTACT 20-22 AWG FEMALE	1-034-0289	
6		3	CONNECTOR SHELL 1 CONTACT MALE	1-034-0300	
7		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
8					
9		1	CLAMP LOOP .187 x .287	2-050-0170	
0					
1		1	SPRING DAG 1/4 OD 6-1/2 LG	3-015-0105	
2					
3		1	TERMINAL LUG SOLDER # 6	3-016-0140	
4					
5		8	STANDOFF PCB HEIGHT 3/8	3-019-0143	

PREPARED			TITLE MONITOR 12" TV-A12 MISC.		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 1-014-0737	REV.	SHEET 1 OF 1

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	RIVET ASSEMBLY FRAME	6-006-0225	
2					
3		1	FRAME TV-A12	2-017-0638	
4					
5		2	GUSSET CORNER 1 FRAME	2-017-0585	
6		2	GUSSET CORNER 2 FRAME	2-017-0586	
7					
8		1	PLATE FRAME	2-017-0636	
9					
10		1	WIRE FORMED SUPPORT	2-022-0101	
11		1	WIRE FORMED U SHAPE	2-022-0131	
12		2	WIRE FORMED U SHAPE	2-022-0132	
13		1	WIRE STRAIGHT 9.5 Lg.	2-022-0133	
14		2	WIRE STRAIGHT 1.580	2-022-0134	
15					
16					
17		4	NUT CLINCH 8-32 STLCAD	3-019-0115	
18		3	NUT CLINCH 6-32 STLCAD	3-019-0119	

PREPARED			TITLE	RIVETED ASSEM. FRAME, CRT	
CHECKED			DWG. NO. 6-006-0225	REV.	SHEET 1 OF 1
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY DEFLECTION COIL	6-004-0314	
2					
3		1	COIL DEFLECTION	1-023-0205	
4					
5		4	CONTACT 20-22 AWG FEMALE	1-034-0289	
6					
7		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	

PREPARED			TITLE ASSEMBLY DEFLECTION COIL, CRT		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 6-004-0314	REV.	SHEET 1 OF 1

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	RIVETED ASSEM. PWR. TRANSFORMER BKT.	6-006-0226	
2					
3		1	SOCKET TRANSISTOR POWER TO-3	1-022-0230	
4		1	SOCKET CAP. ELYTIC 1-3/8 PHEN.	1-022-0404	
5					
6		1	TERMINAL STRIP 7 LUG-2 GND #6 MTG	1-029-0145	
7					
8		1	BRACKET, POWER SUPPLY	2-017-0658	
9					
10		6	RIVET .120 x 7/32 STLCAD	3-014-0135	
11					
12		5	NUT CLINCH 8-32 STLCAD	3-019-0115	

PREPARED			TITLE RIVETED ASSEM. PWR. TRANSFORMER BKT.CRT	ADDS	Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 6-006-0226 REV.	SHEET 1 OF 1	

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY 120V POWER SUPPLY MODULE	6-003-0371	
2					
3		1	CAP ELECTROLYTIC 3300 uF 60V	1-012-2156	C1
4					
5		1	TRANSISTOR 2N3055	1-015-1134	Q1
6		1	INSULATOR MICA TO-3	2-015-5010	
7					
8		1	TRANSFORMER 120/220 VAC 50/60Hz	1-017-5390	T1
9					
10		1	DIODE BRIDGE ZA VS148	1-021-0413	CR1
11					
12		1	FUSEHOLDER 1/4 x 1-1/4	1-028-0210	
13		1	FUSE .6A-250V SLO-BLO	1-028-0244	
14					
15		7	CONTACT 20-22 AWG FEMALE	1-034-0289	
16		3	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
17		4	CONTACT 20-22 AWG MALE	1-034-0295	
18		1	CONNECTOR SHELL 4 CONTACT FEMALE	1-034-0297	
19					
20		2	INSULATOR BUSHING NYLON .5 MTG HOLE	2-046-0230	
21					
22		1	MCH SCR 6-32 x 1/2 STLCAD PHLPAN	3-011-0352	
23		2	TPG SCR CHS CAD 6 x 1/2 PHL PAN	3-011-0408	
24		2	MCH SCR 8-32 x 1/2 STLCAD PHLPAN	3-011-0555	
25		1	NUT HEX 6-32 STLCAD 5/16 FLATS	3-012-0160	
26		1	WASHER LOCK #6 INT STLCAD	3-013-0160	
27		2	WASHER LOCK #6 INT STLCAD	3-013-0182	

PREPARED			TITLE ASSEMBLY 120V POWER SUPPLY MODULE, CRT		
CHECKED					
APPROVED			DWG. NO. 6-003-0371	REV.	SHEET 1 OF 1

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY VERTICAL CHOKE	6-003-0321	L1
2					
3		1	CHOKE VERTICAL	1-031-0131	
4					
5		2	CONTACT 20-22 AWG FEMALE	1-034-0289	
6					
7		1	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	

PREPARED			TITLE ASSEMBLY VERTICAL CHOKE, CRT	ADDS	Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 6-003-0321	REV.	SHEET OF

TEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1		1	ASSEMBLY HIGH VOLTAGE TRANSFORMER	6-003-0320	T2
2					
3		2	CORE, FERRITE	1-017-5371	
4					
5		1	TRANSFORMER HIGH VOLTAGE	1-017-5372	
6					
7		1	COIL FORM	1-017-5387	
8					
9		1	DIODE H510	1-021-0424	
10					
11		1	LEAD ELEC. CRT 8.5 INCH	1-033-0163	
12					
13		5	CONTACT 20-22 AWG FEMALE	1-034-0289	
14		2	CONNECTOR SHELL 3 CONTACT MALE	1-034-0290	
15					
16		1	CLAMP FERRITE CORE 2.0 INCH	2-050-0168	
17					
18		1	INSULATION SLEEVING SHRINKABLE 2-3/8 x $\frac{1}{4}$	2-052-0187	
19					
20		2	NUT THREADING .094 STUD	3-012-0278	
21					
22		2	SHEET MYLAR 10MIL 1/4 SO	5-011-0124	

PREPARED			TITLE ASSEMBLY HIGH VOLTAGE TRANSFORMER, CRT		
CHECKED					
APPROVED			DWG. NO. 6-003-0320	REV.	SHEET 1 OF 1

ADDS Applied Digital Data System, Inc. Hauppauge, New York

ITEM	ADD'L P/N	QTY.	DESCRIPTION	MFR. P/N	REF DES.
1		1	ASSEMBLY LOW VOLTAGE CIRCUIT BOARD	6-002-0459	
2					
3		1	PRINTED WIRING BOARD LOW VOLTAGE	1-029-0367	
4					
5		1	RESISTOR WIREWOUND .068 ohm ZW 10%	1-011-2217	R204
6		3	RESISTOR CARBON 470 ohm 1/2W 5%	1-011-2262	R206,207,209
7		2	RESISTOR CARBON 1K ohm 1/2W 5%	1-011-2270	R201,202
8		1	RESISTOR CARBON 1.5K ohm 1/2W 5%	1-011-2274	R205
9		1	RESISTOR CARBON 10K 1/2W 5%	1-011-2294	R203
10					
11		1	RESISTOR VAR COMP. 500 ohm 1/8W	1-011-5604	R208
12					
13		1	CAP. CERAMIC .01uf 500V 20%	1-012-0740	C202
14		2	CAP. ELECTROLYTIC 50 uf 50V	1-012-2157	C201,C203
15					
16					
17		2	TRANSISTOR 2N3903	1-015-1132	Q202,Q203
18		1	TRANSISTOR 2N3053	1-015-1143	Q201
19					
20		1	DIODE ZENER 1N752 5 6V	1-021-0412	VR201
21					
22		7	CONTACT -20-22 AWP MALE	1-034-0288	
23					
24		1	INSULATOR-TRANSPAD TO-5	3-019-0134	

PREPARED			TITLE ASSEM. LOW VOLTAGE CIRCUIT BOARD, CRT		
CHECKED			DWG. NO. 6-002-0459	REV.	SHEET 1 OF 1
APPROVED					

ADDS Applied Digital Data System, Inc. Hauppauge, New York

EM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
		1	ASSEM PWP MAIN CHASSIS	6-002-0500	
1		1	PRINTED WIRING BOARD MAIN CHASSIS	1-029-0369	
2		1	RESISTOR WIREWOUND 1.2 ohm 2W 10%	1-011-1395	R130
3		1	RESISTOR WIREWOUND 3.3 ohm 2W 10%	1-011-1571	R125
4		1	RESISTOR COMP. 5.6 ohm ½ W 5%	1-011-2218	R129
5		2	RESISTOR CARBON 47 ohm ½ W 5%	1-011-2238	R111, R109
6		2	RESISTOR CARBON 150 ohm ½W 5%	1-011-2250	R114, R123
7		1	RESISTOR CARBON 220 ohm ½ W 5%	1-011-2254	R112
8		1	RESISTOR CARBON 390 ohm ½ W 5%	1-011-2260	R126
9		2	RESISTOR CARBON 470 ohm ½ W 5%	1-011-2262	R127, R113
10		1	RESISTOR CARBON 560 ohm ½W 5%	1-011-2264	R120
11		1	RESISTOR CARBON 820 ohm ½W 5%	1-011-2268	R110
12		2	RESISTOR CARBON 2.7K ohm ½W 5%	1-011-2280	R101, R128
13		1	RESISTOR CARBON 3.3K ohm ½W 5%	1-011-2282	R131
14		2	RESISTOR CARBON 4.7K ohm ½W 5%	1-011-2286	R117, R122
15		1	RESISTOR CARBON 8.2K ohm ½W 5%	1-011-2292	R118
16		2	RESISTOR CARBON 82K ohm ½W 5%	1-011-2316	R115, R103
17		3	RESISTOR CARBON 100K ohm ½W 5%	1-011-2318	R104, R106, R119
18		1	RESISTOR WIREWOUND 82 ohm 3W 10%	1-011-2375	R132
19		1	RESISTOR COMP. 33K ohm 1W 5%	1-011-2448	R137
20		1	RESISTOR VAR. COMP. 100 ohm ⅛W 20%	1-011-5095	R124
21		1	RESISTOR VAR. COMP. 10K ohm ⅛ W 20%	1-011-5312	R121
22		1	RESISTOR VAR. COMP. 100K ohm ⅛ W 20%	1-011-5435	R116
23		1	RESISTOR VAR. COMP. 2.5M ohm ⅛W 20%	1-011-5566	R107
24		1	ARC GAP CERAMIC .75pf 1000V	1-012-0110	C103

PREPARED			TITLE ASSEM. PWB MAIN CHASSIS, CRT	ADDS	Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 6-002-0500 REV. SHEET 1 OF 3		

26		1	CAP. MICA 820pf 500V 5%	1-012-0482	C118
27		1	CAP. CERAMIC .001uf 1000V 10%	1-012-0540	C104
28		1	CAP. CERAMIC .01uf 500V 20%	1-012-0740	C120
29		1	CAP. CERAMIC .02uf 500V 20%	1-012-0780	C111
30		1	CAP. MYLAR .022uf 400V 10%	1-012-0800	C109
31		1	CAP. METAL/MYLAR .1uf 200V 10%	1-012-0870	C110
32		2	CAP MYLAR .47uf 100V 10%	1-012-1005	C105, C106
33		1	CAP MYLAR 10uf 50V 10%	1-012-1130	C113
34		1	CAP ELECTROLYTIC 50uf 50V	1-012-2157	C112
35		1	CAP ELECTROLYTIC 500 uf 6V	1-012-2158	C107
36		1	CAP ELECTROLYTIC 200uf 25V	1-012-2159	C114
37		1	CAP ELECTROLYTIC 100uf 6V	1-012-2160	C108
38		1	CAP ELECTROLYTIC 50uf 25V	1-012-2165	C115
39		1	CAP ELECTROLYTIC 25uf 50V	1-012-2193	C119
40		1	TRANSISTOR 2N4124	1-015-1139	Q107
41		1	TRANSISTOR MJE3055	1-015-1156	Q104
42		1	TRANSISTOR PUT 2N6027CD1311	1-015-1157	Q102
43		1	TRANSISTOR MPS-A14	1-015-1158	Q103
44		1	TRANSISTOR MPS-V05	1-015-1159	Q105
45		1	TRANSISTOR SP2597/MP3791	1-015-1160	Q106
46		1	TRANSISTOR 2N5830	1-015-1172	Q101
47		1	HEAT SINK TO77	1-015-5032	
48		1	HEAT SINK TO3	1-015-5033	

PREPARED			TITLE ASSEM. PWB MAIN CHASSIS, CRT		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED					
APPROVED			DWG. NO. 6-002-0500	REV.	SHEET 2 OF 3

EM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
49		1	COIL ADJ WIDTH	1-016-0303	L101
50		1	TRANSFORMER HORIZ. DRIVE	1-017-5338	T101
51		1	DIODE ZENER 1N758 10V	1-021-0180	VR101
52		1	DIODE 1N4785	1-021-0360	CR103
53		4	DIODE 1N3279	1-021-0380	CR104,105,106,107
54		3	DIODE A9201/1N3605	1-021-0410	CR101,102,108
55		1	SOCKET CRT 7 PIN	1-022-0427	
56		18	CONTACT 20-22 AWG MALE	1-034-0288	
57		1	MCH SCR 4-40 x 1/2 PHLPAN	3-011-0140	
58		4	MCH SCR 6-32 x 3/8 PHLPAN	3-011-0330	
59		1	NUT HEX 4-40 STLCAD	3-012-0140	
60		4	NUT HEX 6-32 STLCAD 1/4 FLATS	3-012-0161	
61		4	WASHER LOCK #6 INT STLCAD	3-013-0160	
62		2	RESISTOR CARBON 22K 1/4 W 5%	70-16-0223	R135,R136
63		1	RESISTOR CARBON 4.7K 1/4W 5%	70-16-0472	R133

PREPARED			TITLE ASSEM. PWB MAIN CHASSIS, CRT		ADDS Applied Digital Data System, Inc. Hauppauge, New York
CHECKED			DWG. NO. 6-002-0500	REV.	SHEET 3 OF 3
APPROVED					

ITEM	ADD /N	QTY.	DESCRIPTION	MFR. P/N	RE ES.
1		1	ASSEMBLY PWB MAIN CHASSIS	6-002-0500	
2		1	ASSEMBLY LOW VOLTAGE CIRCUIT BOARD	6-002-0459	
3		1	ASSEMBLY HIGH VOLTAGE TRANSFORMER	6-003-0320	T2
4		1	ASSEMBLY VERTICAL CHOKE	6-003-0321	L1
5		1	ASSEMBLY 120V POWER SUPPLY MODULE	6-003-0371	
6		1	RIVETED ASSEMBLY POWER		
7			TRANSFORMER BRACKET	6-006-0226	
8		1	ASSEMBLY DEFLECTION COIL	6-004-0314	YOKE
9					
10		1	WELDED ASSEMBLY FRAME	6-006-0225	
11		1	MONITOR 12" TV-A12 MISC	1-014-0737	

PREPARED			TITLE TOP ASSEMBLY - MONITOR		
CHECKED					
APPROVED			DWG. NO. 035-012	REV.	SHEET 1 OF 1

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9. KEYBOARD SUBASSEMBLY

The keyboard is a subassembly which may be simply removed from a 980 for repair or replacement.

9.1 Keyboard Mechanical Package

Figure 9.1 is a mechanical drawing of the keyboard subassembly, giving overall dimensions.

Note that the keyboard can be removed from a 980 by disconnecting the edge connector at the front of the keyboard and removing four Phillips head screws at the corners of the keyboard which hold it on mounting brackets in the terminal. Field maintenance usually consists of removing a defective keyboard and replacing it with a spare unit.

Individual key modules can be replaced by desoldering two connections on the bottom P.C. Board, pulling the bad module up through the hole in the mounting frame, and then resoldering the new module to the P.C. board connections. Integrated circuits are located on the keyboard P.C. board such that they can be replaced without further board disassembly.

9.2 Keyboard Electronics

Refer to the schematics in Figure 9.2. The heart of the keyboard is an LSI chip that serves the purpose of both an encoder and a ROM. This chip is U1. It is a complete keyboard interface system capable of providing quad mode 90 key keyboard encoding.

A dynamic scanning technique is utilized to detect and pin point keyswitch activity on the keyboard. The chip uses two ring counters. A 9-bit X counter monitors the rows X_0 through X8 of the switch matrix while the 10 columns Y_0 through Y_9 are monitored by a 10-bit Y counter. Since there are 9 x 10 = 90 possible counter states, ninety data switches may be defined by their X-Y coordinates.

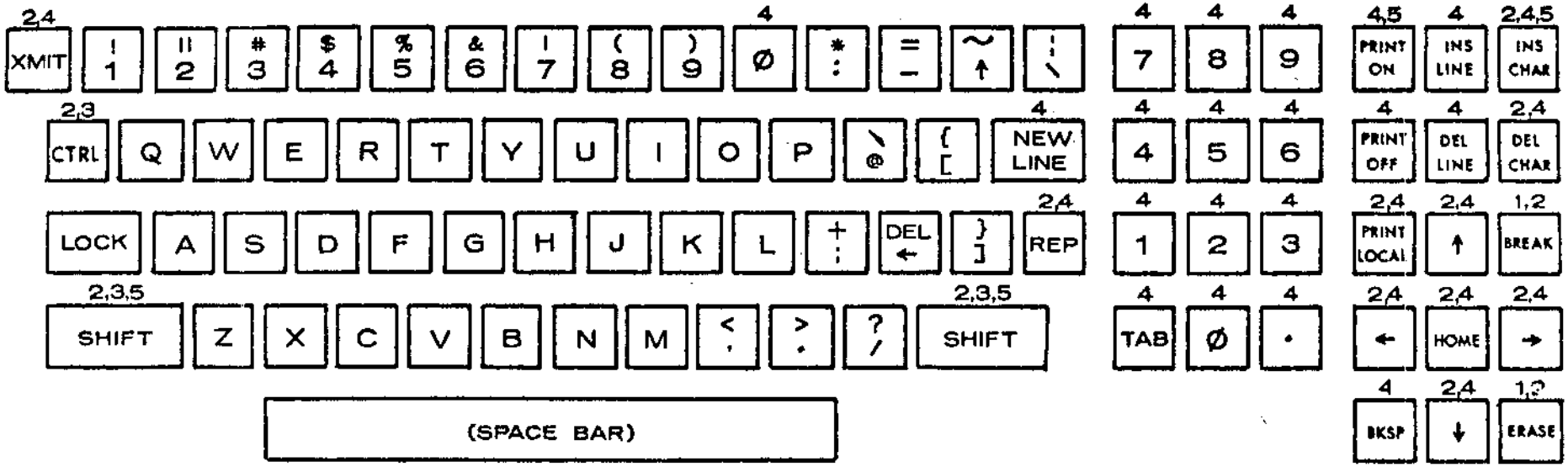
Every scan time (90-bit times), all keys are interrogated in turn to determine their status. Each particular key is interrogated every 90-bits or once each keyboard scan cycle. This is implemented by employing the X counter as drivers to drive each row of the switch matrix in turn. The Y counter enables the sensing of each column of the switch matrix. Therefore, if a switch is closed it will be detected if its row is driven and its column is sensed. This corresponds to the particular X-Y time (one of 90 time slots in the scan) defining the closed switch. A key detect pulse at the X-Y time in question is issued, and this is used to define the status of that particular key.

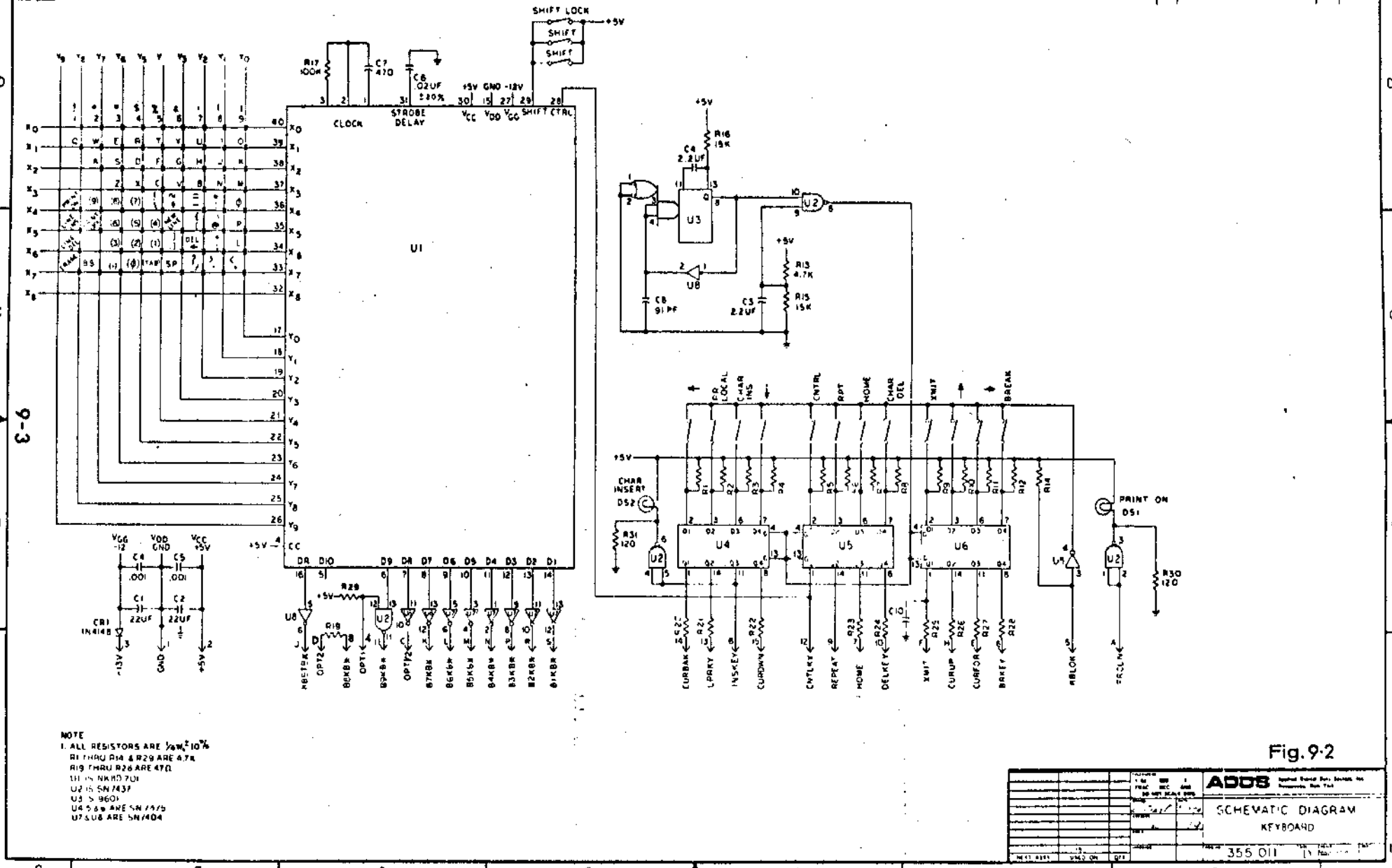
CONSUL 980 KEYBOARD

Fig. 9-1

NOTES:

1. Must be used in conjunction with "CTRL"
2. Produce D.C. level change, not coded.
3. Used to control keyboard operating modes.
4. Not affected by "SHIFT" or "CTRL"
5. Lighted keys





NOTE
1. ALL RESISTORS ARE ⅛W, ±10%
   R1 THRU R14 & R29 ARE 4.7K
   R19 THRU R26 ARE 470
   U1 IS NKB01
   U2 IS SN7437
   U3 IS 9601
   U4,5,6 ARE SN7495
   U7,U8 ARE SN7404

Fig. 9-2

ADDS

SCHEMATIC DIAGRAM
KEYBOARD

355 011

9-3

ASCII Codes Generated in Row 1 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE BITS 765	4321	SHIFTED MODE BITS 765	4321	CONTROL MODE BITS 765	4321	SHIFT & CONTROL MODE BITS 765	4321	
XMIT			FUNCTION KEY						
1 !	011	0001	010	0001	011	0001	010	0001	TYPING ARRAY
2 "	011	0010	010	0010	011	0010	010	0010	
3 #	011	0011	010	0011	011	0011	010	0011	
4 $	011	0100	010	0100	011	0100	010	0100	
5 %	011	0101	010	0101	011	0101	010	0101	
6 &	011	0110	010	0110	011	0110	010	0110	
7 '	011	0111	010	0111	011	0111	010	0111	
8 (	011	1000	010	1000	011	1000	010	1000	
9)	011	1001	010	1001	011	1001	010	1001	
Ø	011	0000	011	0000	011	0000	011	0000	
: *	011	1010	010	1010	011	1010	010	1010	
- =	010	1101	011	1101	010	1101	011	1101	
↑ ~	101	1110	111	1110	001	1110	111	1110	
\ ¦	101	1100	111	1100	001	1100	111	1100	
7	011	0111	011	0111	011	0111	011	0111	NUMERIC PAD
8	011	1000	011	1000	011	1000	011	1000	
9	011	1001	011	1001	011	1001	011	1001	
PRINT ON	000	1011	000	1011	000	1011	000	1011	CONTROL ARRAY
LINE INSERT	000	1110	000	1110	000	1110	000	1110	
CHAR INSERT	ALTERNATE ACTION KEY LIGHTED FUNCTION KEY								

ASCII Codes Generated in Row 2 of Keyboard

	UNSHIFTED MODE		SHIFTED MODE		CONTROL MODE		SHIFT & CONTROL MODE		
KEYTOP LEGEND	BITS 765	4321	BITS 765	4321	BITS 765	4321	BITS 765	4321	
CNTL	FUNCTION KEY								TYPING ARRAY
Q	101	0001	111	0001	001	0001	111	0001	
W	101	0111	111	0111	001	0111	111	0111	
E	100	0101	110	0101	000	0101	110	0101	
R	101	0010	111	0010	001	0010	111	0010	
T	101	0100	111	0100	001	0100	111	0100	
Y	101	1001	111	1001	001	1001	111	1001	
U	101	0101	111	0101	001	0101	111	0101	
I	100	1001	110	1001	000	1001	110	1001	
O	100	1111	110	1111	000	1111	110	1111	
P	101	0000	111	0000	001	0000	111	0000	
@ \	100	0000	110	0000	000	0000	110	0000	
[{	101	1011	111	1011	001	1011	111	1011	
NEW LINE	000	1101	000	1101	000	1101	000	1101	
4	011	0100	011	0100	011	0100	011	0100	NUMERIC PAD
5	011	0101	011	0101	011	0101	011	0101	
6	011	0110	011	0110	011	0110	011	0110	
PRINT OFF	000	1100	000	1100	000	1100	000	1100	CONTROL ARRAY
LINE DEL	000	1111	000	1111	000	1111	000	1111	
CHAR DEL	FUNCTION KEY								

ASCII Codes Generated in Row 3 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE BITS 765	4321	SHIFTED MODE BITS 765	4321	CONTROL MODE BITS 765	4321	SHIFT & CONTROL MODE BITS 765	4321	
LOCK	SHIFT LOCK								TYPING ARRAY
A	100	0001	110	0001	000	0001	110	0001	
S	101	0011	111	0011	001	0011	111	0011	
D	100	0100	110	0100	000	0100	110	0100	
F	100	0110	110	0110	000	0110	110	0110	
G	100	0111	110	0111	000	0111	110	0111	
H	100	1000	110	1000	000	1000	110	1000	
J	100	1010	110	1010	000	1010	110	1010	
K	100	1011	110	1011	000	1011	110	1011	
L	100	1100	110	1100	000	1100	110	1100	
; +	011	1011	010	1011	011	1011	010	1011	
← DEL	101	1111	111	1111	001	1111	111	1111	
[}	101	1101	111	1101	001	1101	111	1101	
REPEAT	FUNCTION KEY								
1	011	0001	011	0001	011	0001	011	0001	NUMERIC PAD
2	011	0010	011	0010	011	0010	011	0010	
3	011	0011	011	0011	011	0011	011	0011	
PRINT LOCAL	FUNCTION KEY								CONTROL ARRAY
↑	FUNCTION KEY								
BREAK	FUNCTION KEY INTERLOCKED WITH CONTROL								

ASCII Codes Generated in Row 4 of Keyboard

KEYTOP LEGEND	UNSHIFTED MODE BITS 765	4321	SHIFTED MODE BITS 765	4321	CONTROL MODE BITS 765	4321	SHIFT & CONTROL MODE BITS 765	4321	
SHIFT	KEYBOARD FUNCTION								
Z	101	1010	111	1010	001	1010	111	1010	TYPING ARRAY
X	101	1000	111	1000	001	1000	111	1000	
C	100	0011	110	0011	000	0011	110	0011	
V	101	0110	111	0110	001	0110	111	0110	
B	100	0010	110	0010	000	0010	110	0010	
N	100	1110	110	1110	000	1110	110	1110	
M	100	1101	110	1101	000	1101	110	1101	
, <	010	1100	011	1100	010	1100	011	1100	
. >	010	1110	011	1110	010	1110	011	1110	
/ ?	010	1111	011	1111	010	1111	011	1111	
SHIFT									
TAB	000	1001	000	1001	000	1001	000	1001	NUMERIC PAD
ø	011	0000	011	0000	011	0000	011	0000	
.	010	1110	010	1110	010	1110	010	1110	
←	FUNCTION KEY								CONTROL ARRAY
HOME	FUNCTION KEY								
→	FUNCTION KEY								

ASCII Codes Generated in Row 5 of Keyboard

SPACE	010	0000	010	0000	010	0000	010	0000
BS	000	1000	000	1000	000	1000	000	1000
↓	FUNCTION KEY							
ERASE	000	1100	000	1100	000	1100	000	1100

Once it is determined as to which key is closed, this information is taken and used to provide a coded bit pattern for that key. In addition to scanning the key switch matrix, the X and Y counters are used to scan the contents of a Read Only Memory (ROM) which contains the bit pattern for each key switch. For example, when switch X_1, Y_1 (letter I) is being interrogated (at X_1-Y_1 time), the counters are addressing the ROM location which contains the code for switch X_1-Y_1. If the key is closed, a key detect pulse is issued. At this time, the ROM contents are strobed into latches which then hold the code pattern D1 through D10 for the key X_1 Y_1 (i.e., letter I).

For each keyswitch it is possible to have four modes. These are determined by the status of the SHIFT and CONTROL keys which are inputs to U1. There are four possible code patterns for each key as determined by the mode switches.

The code pattern along with the strobe out of U1 is inverted by U7 and U8 to provide the signals B1 through B9 that are active low. To assure that the output code pattern is stable the strobe is delayed by the capacitor C6. The coding information for coded keys is given in Figure 9.3.

All the unencoded keys such as cursor movements, XMIT, etc., are generated to the right of U1. These function keys are debounced from a free running oscillator, U3 triggering three quad latches, U4, U5 and U6. When a function key is depressed, the corresponding interface pin goes from GND to +5 Volts, and remains at +5 Volts until the key is released.

The keyboard can be "disabled" by grounding the connector pin labeled "KBLOK" (Keyboard lock). This disables the "strobe" output signal, and all the function keys.

9.3 Keyboard Interface Signals

The edge connector on the keyboard is a 30-pin connector. The signals and their pins are listed below.

980 KEYBOARD

PIN ASSIGNMENT

Pin 1	GND	Pin A	Input pin for light
2	+5V	B	CHAR. INSERT (TTL +5V)
3	-13V	C	OPT 1/2
4	OPT1	D	OPT 2
5	KBLOK*	E	CURFWD
6	BREAK	F	XMIT
7	CURHOM	H	CURUP
8	B8KB*	J	KBSTB*
9	REPEAT	K	B7 KB*
10	CHAR. DELETE	L	B6 KB*
11	B9KB*	M	B5 KB*
12	CONTROL	N	B4 KB*
13	PRINT LOCAL	P	B3 KB*
14	CURBAK	R	B2 KB*
15	CURDWN	S	B1 KB*

NOTE: Pin A pertains to the PRINT ON light

OPT1 - Normal, Pin C strapped to Pin 4

OPT2 - Function Keys, Pin C strapped to Pin D

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	355-011	—	KEYBOARD ASSY - 980		
2	502-703	1	BRACKET, MTG. R.H.		
3	502-704	1	BRACKET, MTG. L.H.		
4	355-019	1	KEYBOARD 980 NCR		
5	360-178	4	WASHER		
6	810-005	4	SCREW 6-32 X 5/16	SEM	
7	810-008	4	SCREW 6-32 X 1/2	SEM	
8	790-008	4	WASHER, PLAIN #6		
9	360-089	AR	CATERPILLAR, TRACK		
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					
26					
27					

PREPARED	L. Ebert	3/27/75	TITLE	KEYBOARD ASSY 980	
CHECKED			DWG. NO.	355-011	REV.
APPROVED			SHEET / OF /		

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
1	355-019		KEYBOARD 980, NCR		
2	357-008	1	KEYCAP SET, NCR 980		
3	356-015	1	P.C. BOARD	CHERRY ELECT. 001-0699	
4	356-005	1	COVER PLATE	CHERRY ELECT. 022-0424	
5	356-006	9	SPACER	CHERRY ELECT. 013-0079	
6	356-007	1	MODULE, LIGHTED	CHERRY ELECT. M41-0100	
7	356-003	1	MODULE, SPACE BAR	CHERRY ELECT. M51-0106	
8	356-008	78	MODULE, T	CHERRY ELECT. M61-0120	
9	356-009	1	MODULE, SHIFT	CHERRY ELECT. M61-0300	
10	356-010	1	MODULE, LOCK	CHERRY ELECT. M61-0500	
11	356-002	1	MODULE, LIGHTED ALT. ACTION	CHERRY ELECT. M61-0800	
12	356-011	2	BULB	CHERRY ELECT. 022-0432	
13	356-012	1	SOCKET, 40 PIN DIP	CHERRY ELECT. 007-0378	
14	356-013	1	SPRING	CHERRY ELECT. 004-0656	
15	356-014	3	PAD	CHERRY ELECT. 012-0339	
16	360-126	2	PLUNGER	CHERRY ELECT. 004-0549	
17	360-131	1	BRACKET, PIVOT	CHERRY ELECT. 004-0550	
18	704-1025	2	SCREW, BH. 4-40 X 1/8 LG	CHERRY ELECT. 012-0324	
19	360-128	2	PIVOT	CHERRY ELECT. 012-0325	
20					
21					
22					
23					
24	190-005	1	DIODE 1N4148		CR1
25					
26					
27					

PREPARED	L. Ehst	3-27-75	TITLE	KEYBOARD 980,		
CHECKED			DWG. NO.	355-019	REV.	SHEET 1 OF 2
APPROVED						

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

ITEM	ADDS P/N	QTY.	DESCRIPTION	MFR. P/N	REF. DES.
28	302-021	15	RESISTOR 4.7 K		R1-R14,R29
29	302-086	2	RESISTOR 15 K		R15,R16
30	302-026	1	RESISTOR 100 K		R17
31	302-017	11	RESISTOR 47 OHM		R18-R28
32	302-103	2	RESISTOR 120 OHM		R30,R31
33					
34					
35					
36	140-092	3	CAPACITOR 22 UF	CHERRY ELECT. 034-0403	C1,C2,C3
37	140-084	2	CAPACITOR .001 UF	REC	C4,C5
38	140-091	1	CAPACITOR .02 UF	REC	C6
39	140-005	1	CAPACITOR 47 PF	REC	C7
40	140-002	1	CAPACITOR 91 PF	REC	C8
41	140-093	1	CAPACITOR 2.2 UF	CHERRY ELECT. 034-0268	C9
42					
43					
44	200-090	1	INTEGRATED CIRCUIT NKDB-701	G.I.	U1
45	200-077	1	INTEGRATED CIRCUIT SN7437N	N.S.	U2
46	200-091	1	INTEGRATED CIRCUIT 9601	N.S.	U3
47	200-016	3	INTEGRATED CIRCUIT SN7475N	N.S.	U4,U5,U6
48	200-019	2	INTEGRATED CIRCUIT SN7404N	N.S.	U7,U8
49					
50					
51					
52					
53					
54					

PREPARED	L. Eberle	3-27-75
CHECKED		
APPROVED		

TITLE KEYBOARD 980,

DWG. NO. 355-019 | REV. | SHEET 2 OF 2

ADDS Applied Digital Data System, Inc. Hauppauge, New York

BILL OF MATERIAL

10. SCHEMATICS & ASSEMBLY DRAWINGS

This section includes the schematics and assembly drawings listed below:

ASYNC/FE	135-088	Schematic
	129-088	Assembly
VIDGEN	135-089	
	129-089	
CONTROL	135-090	
	129-090	
MEMORY	135-091	
	129-091	
OPTION	135-092	
	129-092	

IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES
SN7400	A4,B2,C1,C6,D1,E2, F6,J4,L5	SN7430	H7	LM1488	A1
		SN7437	J5	LM1489	A3
SN7402	B3,E5,K4	SN7474	A7,B4,B6,B7,C4,C7, D2,D4,D7,E3,F3,F4, F5,H6,J6,K6	DM8810	F2,H2
SN7404	C2 D6 F7 H4 J2 L6				K3,L3
SN7405	J1,K2,L2			4N26	A0,A2
SN7408	A5,B1,B5,H3,H5,L4	SN7495	C3		
SN7410	C5,K5	SN74123	E6		
SN7411	A6,D3	SN74175	F1,H1		
SN7420	E4	LM311	J7		

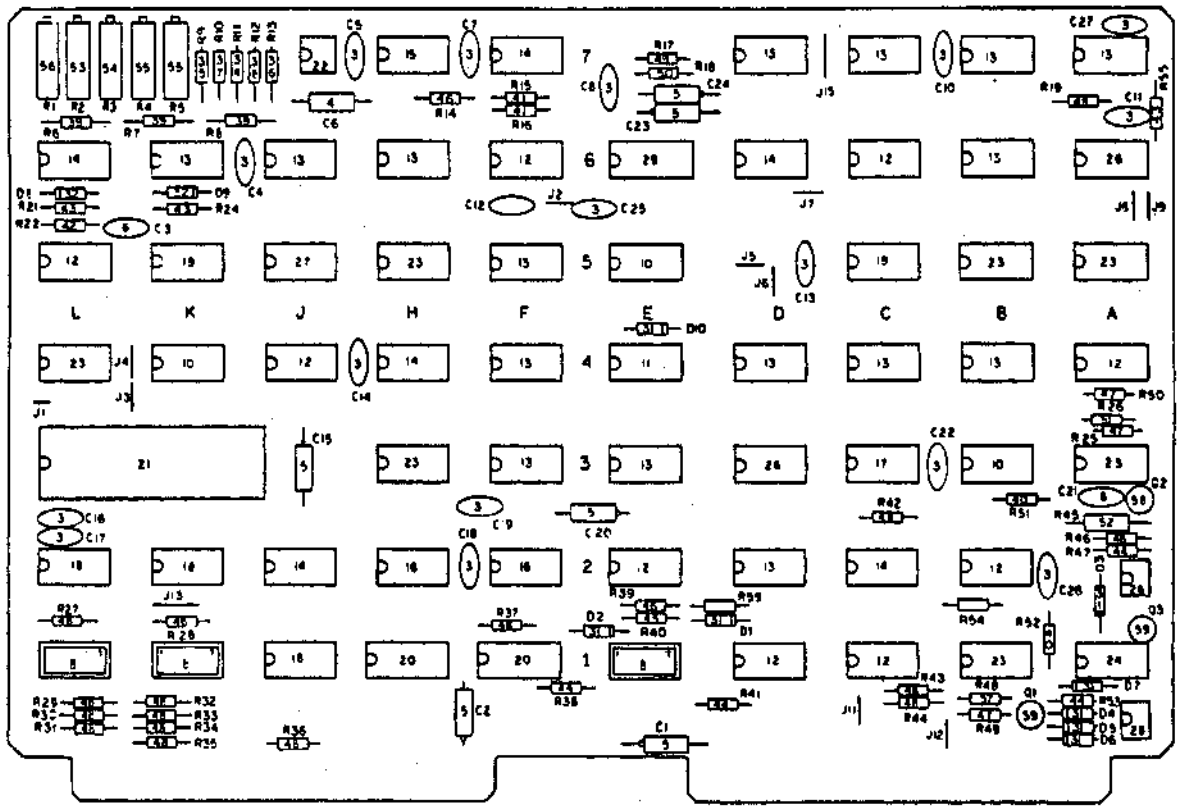
10-2/3

ADDS — SCHEMATIC DIAGRAM — ASYN/FE — 35-088

SEE NEXT P/G

IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES
SN7400	A4,B2,C1,C6,D1,E2, F6,J4,L5	SN7430	N7	LM1488	A1
		SN7437	J5	LM1489	A3
SN7402	B3,J5,K4		A7,B4,B6,B7,C4,E7,	DM881D	F2,M2
SN7404	C2 D6 F7 H4 J2 L6	SN7474	D2,D4,D7,E3,F5,F4,		K3,L3
SN7405	J4,K2,L2		F5,H6,J6,K6	4N26	A0,A2
SN7408	A5,B1,B5,H3,H5,L4	SN7494	C3		
SN7410	C5,K5	SN74123	E6		
SN7414	A6,D3	SN74175	F1,H1		
SN7420	E4	LM311	J7		

REVISIONS			
B	ECO 050-118		
C	ECO 050-121		



ADDS

ASSEMBLY
ASYN/FE

129-088 D C

DM8123	A1,B1	SN7473	Q7 of L3
SN74193	A2,A,C1	SN7442	J3
SN74192	B2,B4	SN7420	A5,B6,C6,H2
SN74175	A6, K4,6,L1	SN7411	E4,L2,6
SN74162	A3	SN7410	C4,F3,7,M
SN7493	B4	SN7408	E3,H5,J5,K5,5
SN7486	F3, M1	SN7404	A7,D2,E2,F2,M2
SN7485	A5,B3,C2,M4	SN7402	B5,C1,F4,M5
SN7476	D4,5,E5,F6,J2, L4,7,	SN7400	A6,D3,E6,FLK3,J4,5
IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES

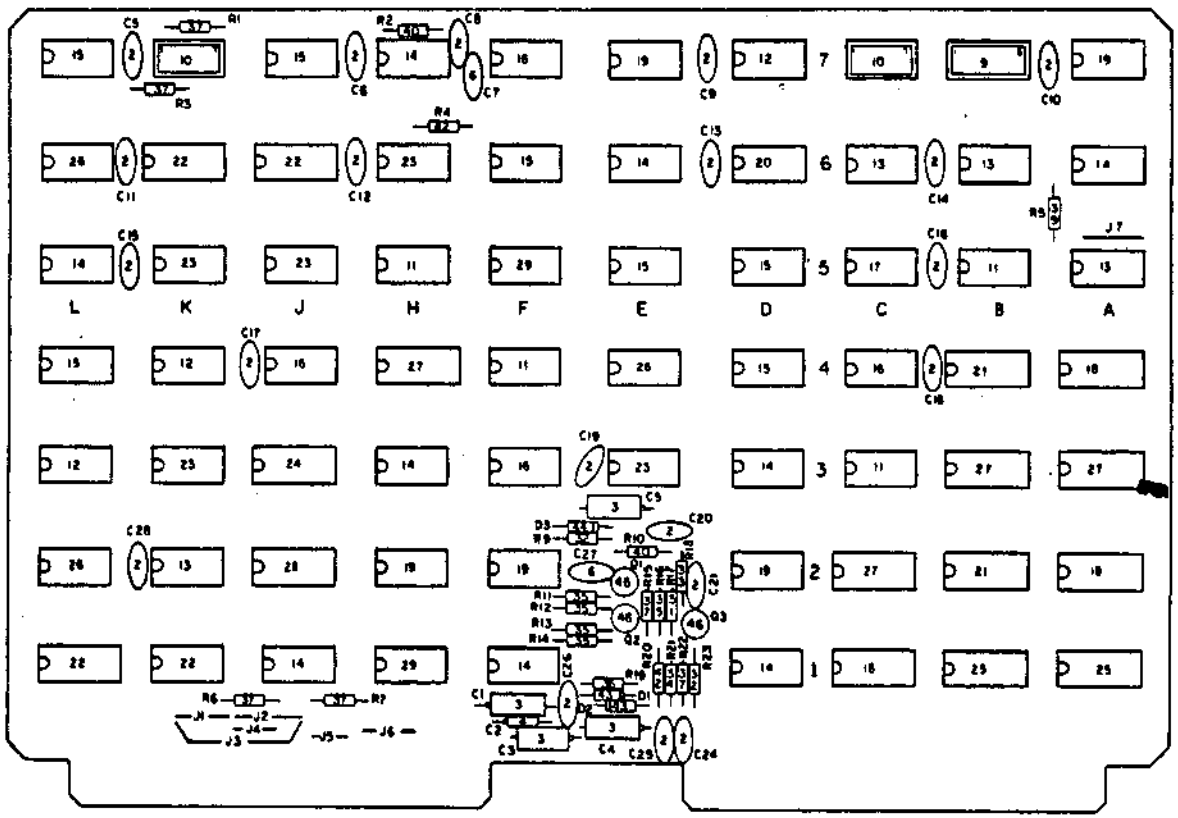
10 5/6

ADDS

SCHEMATIC DIAGRAM

VIDGEN

135-089 E



ASSEMBLY
VIDGEN

129-089 D

LOC. TYPE	LOC. COORDINATES	IC TYPE	IC COORDINATES
SN7400	A6,C3,D2,D7,F6,H3,B7	SN74154	L5
SN7402	A1,C5,F3,F7,H2,H7,K5	SN74165	J3
	K6,L5,L6	SN74192	J4,J5
SN7408	A3,B1,B5,D3,F4,H5,H7		
SN7410	C6,D6,E3		
SN7411	E6		
SN7416	A5,D5,H6,H4,J1,J2		
SN7420	C4,F2,F5		
SN7430	D1		
SN7437	B7		
SN7442	J6		
SN7473	C1,E2,L7		
SN7474	A2,A4,B2,B4,B5,B6,C2 D4,E4,E5,H6		

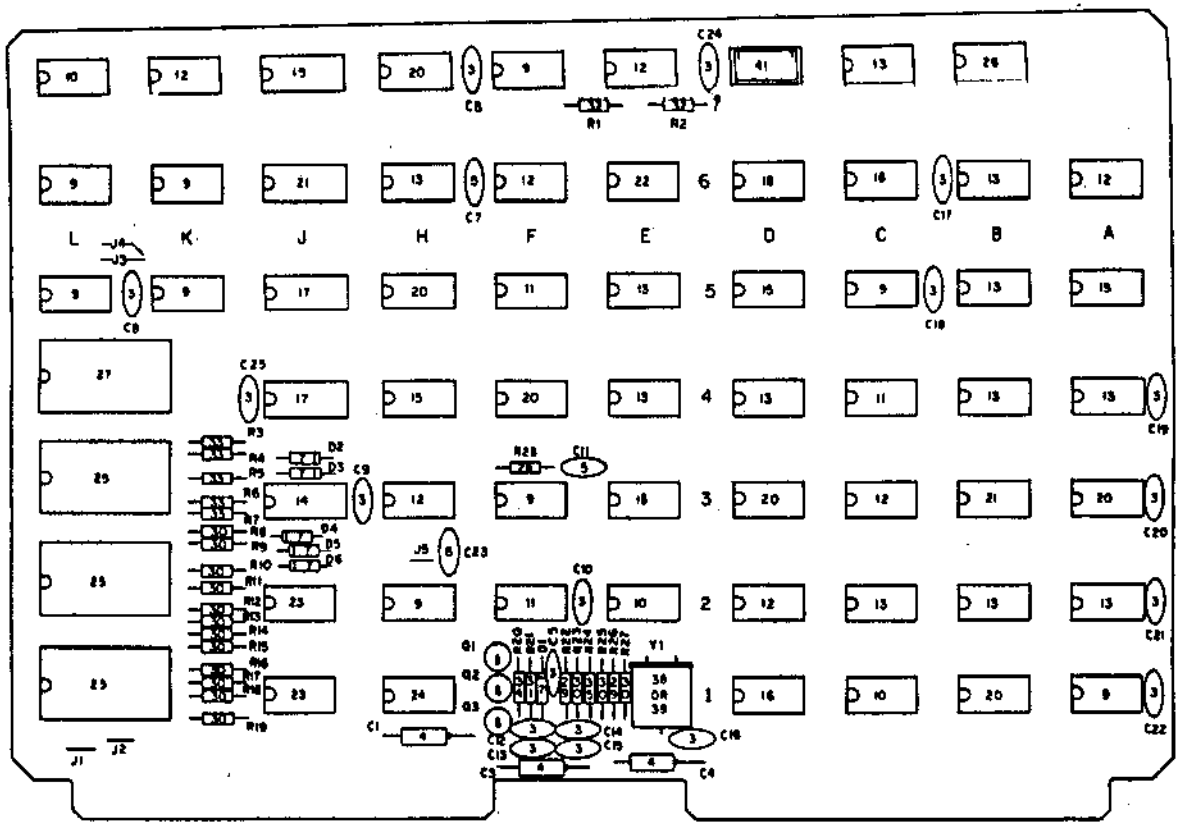
REV	DESCRIPTION	DATE
B	[illegible]	050-149
1	REVISED PER ECO 050 124	

10-8/9

ADDS

SCHEMATIC DIAGRAM
CONTROL

135-090 E C



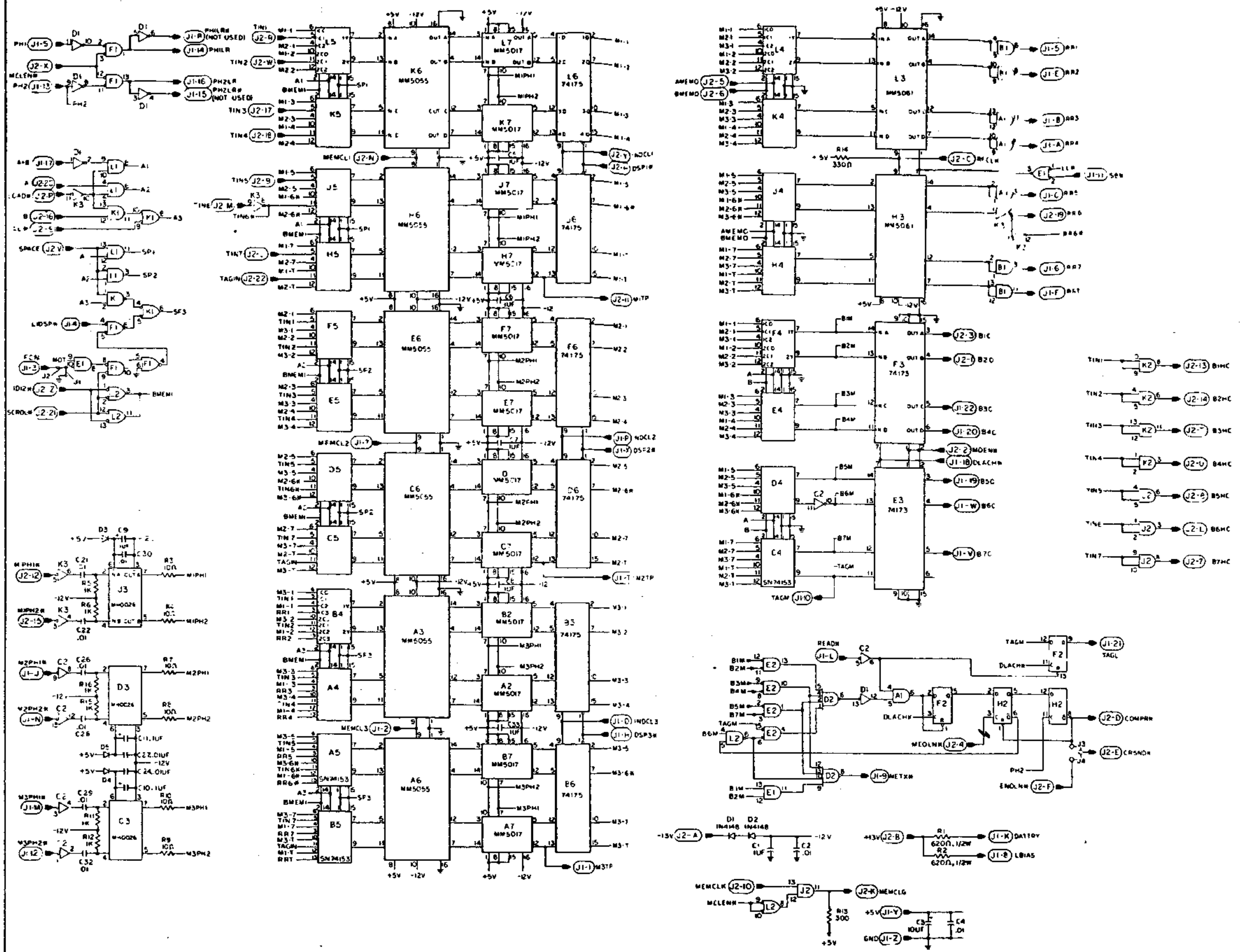
10-10

REVISIONS		
LTR	DESCRIPTION	DATE
B	ECO D90-110	

ADDS

ASSEMBLY
CONTROL

129-090 B



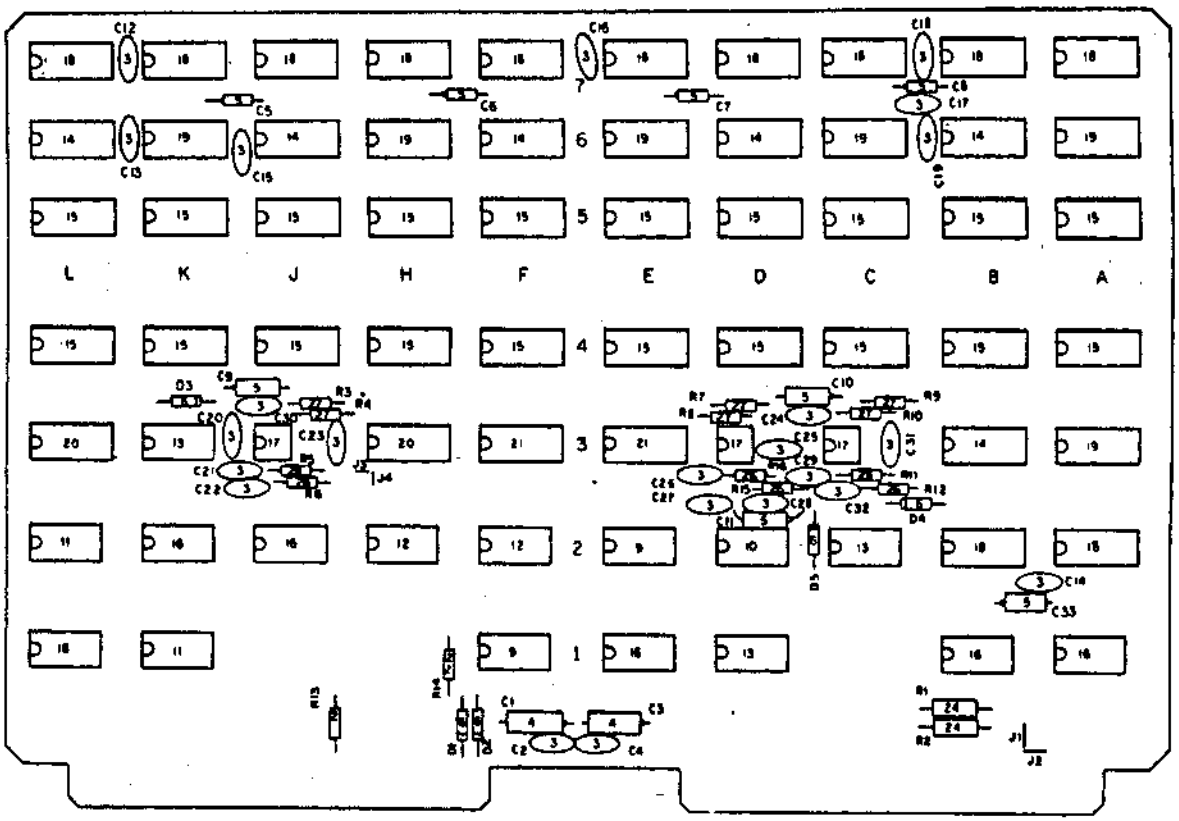
IC TYPE	IC COORDINATES
SN7474	F2,H2
SN742C	D2
SN7428	A1,D1,E1,J2,K2,L1
SN7404	C2,D1,K3
SN7402	E2,F1
SN7400	L2,K1

10-11/12

ADDS

SCHEMATIC DIAGRAM
MEMORY

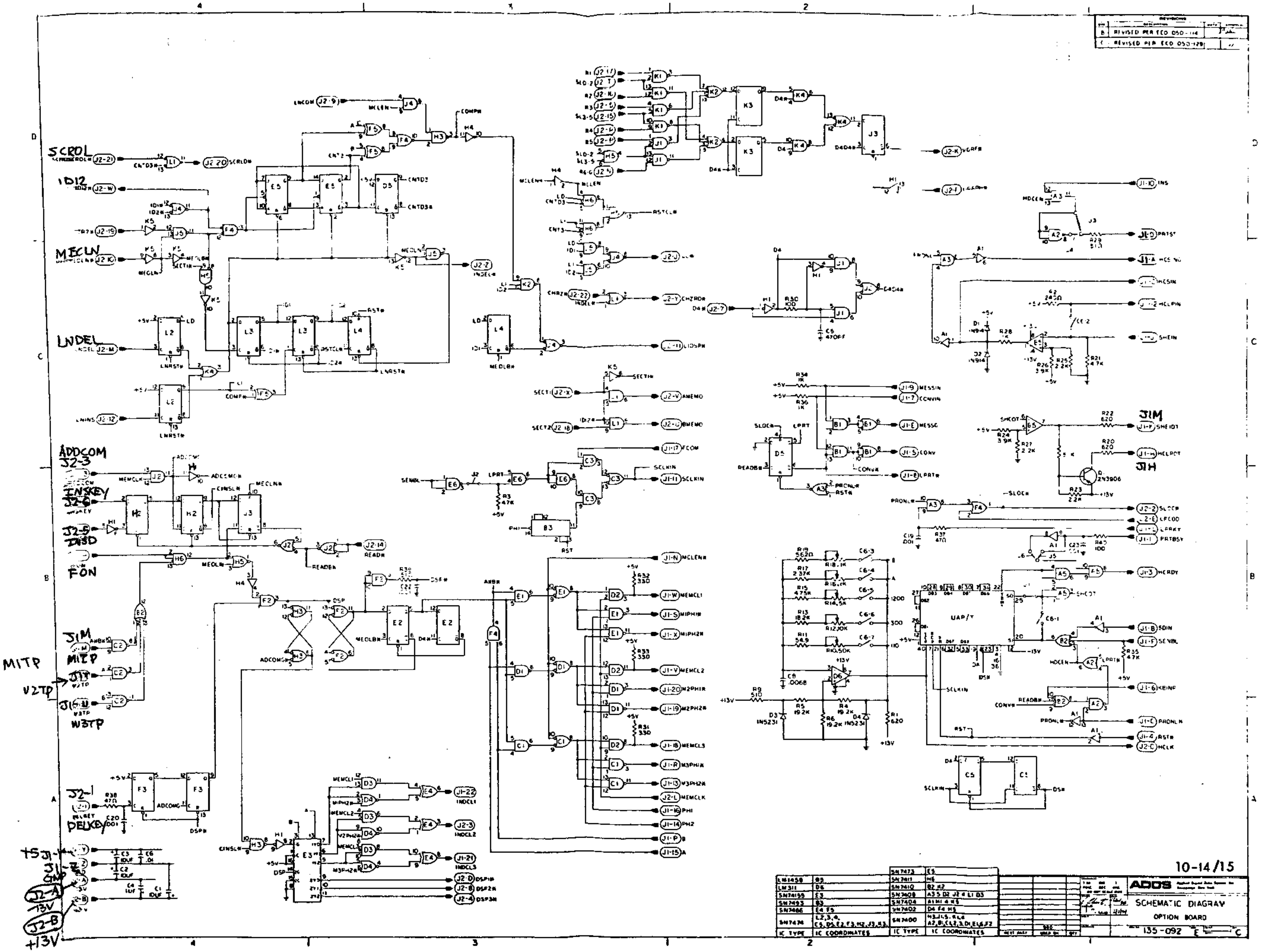
135-091 E



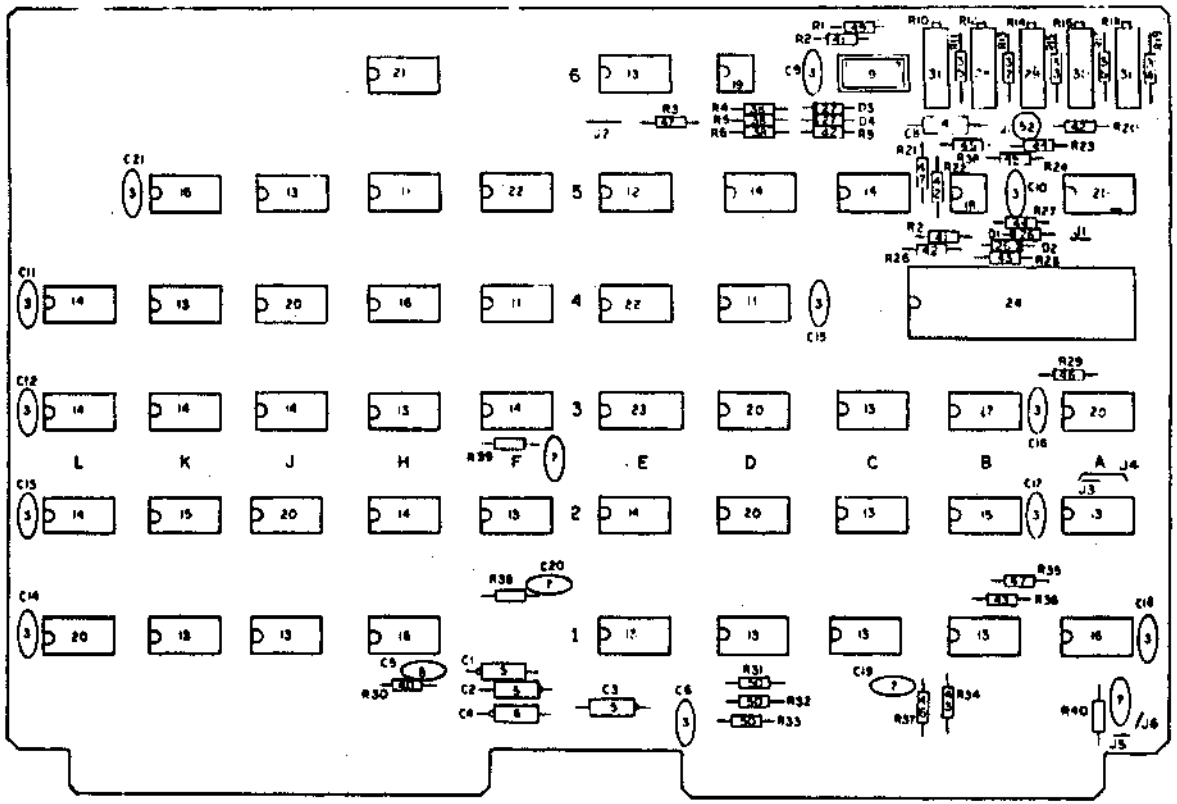
ASSEMBLY
MEMORY

129-091 D

10-13



IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES
		SN7473	E5
LM1458	B5	SN7411	H6
LM311	D6	SN7410	B2 K2
SN74155	E3	SN7408	A3 5 D2 J2 4 L1 D3
SN7493	B3	SN7404	A1 H1 4 K5
SN7486	E4 F5	SN7402	D4 F4 H5
SN7474	L2,3,4, C5, D5, E2, F3, H2, J3, K3,	SN7400	H3, J1, 5, K1, 4, A2, B1, C1, 2, 3, D1, E1, 6, F2



10-16

CO 040-179

ADDS

ASSEMBLY
OPTION

129-092 D C

11. WIRELIST AND HARNESS LIST

This section contains two types of information:

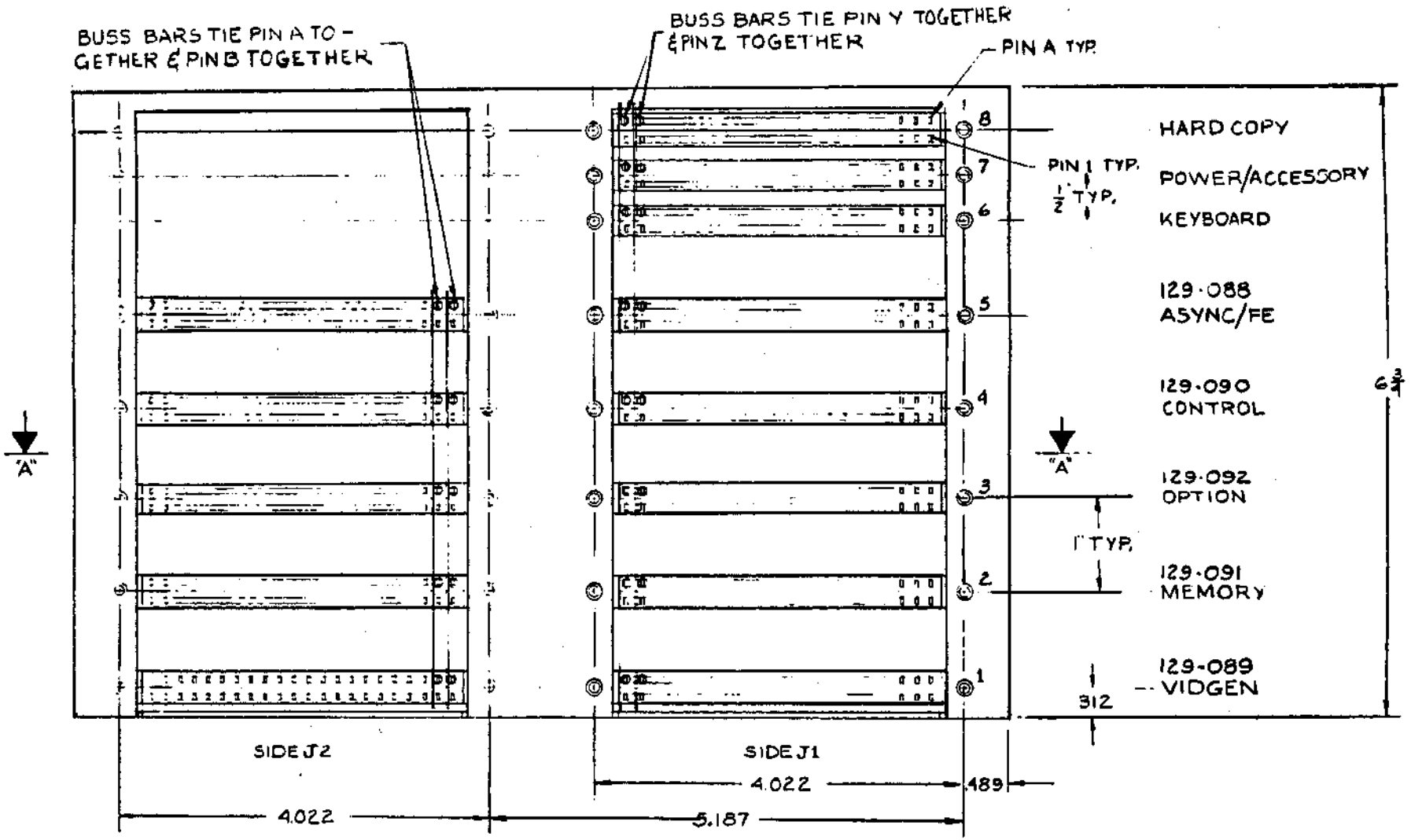
a) A point-to-point wire list of the 980 backplane wiring, with signal names.

b) A point-to-point wire list of the Complete 980 harness, with appropriate signal names.

A view of the 980 Card Cage, as seen from the wirewrap side, is shown in Figure 11.1.

980 CARD CAGE

Fig. 11-1



980 WIRE LIST

Signal Name		
A		
A FREQ	-5B-22, -7A-R	NET 212
A + B	-1A-K, -2A-17	NET 17
ADDCOM	-1A-15, -3B-13, -4A-F, -5A-21	NET 27
ADV	-1B-6, -4A-8	NET 50
AMEMO	-2B-5, -3B-V	NET 108
AUTO*	-4A-B, -7A-14	NET 165
B	-1A-T, -2B-16, -3A-P	NET 30
B FREQ	-5B-21, -7A-S	NET 210
BEL*	-4A-16, -5A-11	NET 171
BELDR	-5A-H, -7A-9	NET 195
BMEMO	-2B-6, -3B-U	NET 110
BRKEY	-5B-E, -6A-6	NET 199
B10	-1A-8, -2B-3, -5B-W	NET 14
B20	-1A-6, -2B-1, -5B-19	NET 10
B30	-1A-H, -2A-22, -5B-V	NET 13
B40	-1A-E, -2A-20, -5B-18	NET 09
B50	-1A-2, -2A-19, -5B-U	NET 03
B60	-1A-7, -2A-W, -5B-17	NET 12
B70	-1A-A, -2A-V, -5B-T	NET 02
B1HC	-2B-13, -8A-E	NET 121
B2HC	-2B-14, -8A-F	NET 123
B3HC	-2B-T, -8A-H	NET 126
B4HC	-2B-U, -8A-J	NET 127
B5HC	-2B-8, -8A-K	NET 114
B6HC	-2B-L, -8A-L	NET 116
B7HC	-2B-7, -8A-M	NET 112
B1KB*	-5B-S, -6A-U	NET 207
B2KB*	-5B-R, =6A-7	NET 205
B3KB*	-5B-15, -6A-S	NET 206
B4KB*	-5B-16, -6A-R	NET 208
B5KB*	-5B-13, -6A-P	NET 203
B6KB*	-5B-11, -6A-N	NET 201
B7KB*	-5B-12, -6A-M	NET 202
B8KB*	-5B-H, -6A-14	NET 200
B9KB*	-5B-14, -6A-10	NET 204
CARDT	-5A-E, -7A-E	NET 191
CARLT	-5A-A, -7A-7	NET 185
CHADR	-1A-4, -4A-D	NET 07
CHRZ*	-3B-22, -4A-W	NET 163
CHZRO*	-1A-21, -3B-Y	NET 39
CH75	-1B-E, -5A-U	NET 49
COMPR*	-2B-D, -4A-19	NET 107

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV
APPROVED			SHEET 1 OF 6

CNTLKY	-1A-12, -5A-T, -6A-15	NET 22
CONV	-3A-5, -4A-11, -5A-F	NET 141
CONVIN	-3A-7, -7A-11	NET 145
CR	-4B-19, -5A-K	NET 182
CRSND*	-2B-E, -5B-6	NET 109
CURBAK	-4B-E, -6A-18	NET 175
CURBK	-1A-U, -4A-6	NET 32
CURDWN	-4B-L, -6A-20	NET 181
CURFOR	-4B-3, -6A-C	NET 173
CURFR*	-1A-J, -4A-E	NET 15
CURUP*	-1A-17, -4A-4	NET 31
CURUP	-4B-10, -6A-H	NET 180
D4*	-1B-P, -3B-7, -4B-18	NET 65
D4	-1b-14, -4B-W	NET 66
DATTRY	-2A-K, -7A-L	NET 93
DELKEY	-3B-1, -6A-12	NET 156
DLACH*	-2A-18, -4B-F	NET 102
DSP1*	-2B-H, -3B-D	NET 113
DSP2*	-2A-X, -3B-8	NET 103
DSP3*	-2A-H, -3B-4	NET 89
EIACLS	-5A-D, -7A-D	NET 189
EIARTS	-5A-5, -7A-C	NET 190
ENOLN*	-2B-F, -4A-2	NET 111
ERR*	-4B-J, -5B-L	NET 177
EXTRQ*	-4A-5, -5B-7	NET 166
FCOM	-3A-17, -5A-9, -7A-W	NET 155
FDX	-5A-10, -7A-13	NET 197
FFENB	-4B-8, -5A-17	NET 176
FON	-1B-R, -2A-3, -3B-H, -4A-V, -5B-2	NET 67
GRAPH*	-1B-8, -3B-F	NET 54
GRPHEN	-1B-K, -4A-13	NET 57
HCLPIN	-3A-12, -8A-S	NET 154
HCLPOT	-3A-H, -8A-T	NET 146
HCRDY	-3A-3, -5A-2	NET 137
HCSIN	-3A-2, -5A-13	NET 135
HCSING	-3A-A, -5A-3	NET 134
HDRIVE	-1B-21, -7A-6	NET 80
HOME	-4A-N, -6A-8	NET 168
ID 12*	-2B-Z, -3B-W	NET 132
INDCL1	-2B-Y, -3A-22	NET 130
INDCL2	-2A-P, -3B-3	NET 99
INDCL3	-2A-D, -3A-21	NET 87
INDEL*	-3B-Z, -4A-U	NET 164
INS	-3A-10, -5A-N	NET 151
INSD	-3B-5, -4B-2	NET 158
INSKEY	-3B-6, -6A-B	NET 160

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED			
APPROVED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV SHEET 2 OF 6

BINP	-3A-6, -5A-15	NET 143
KBSTB*	-5A-8, -6A-K	NET 196
KBLOK*	-4A-R, -5A-14, -6A-4	NET 170
LBIAS	-2A-8, -7A-M	NET 90
LDLNE*	-1A-X, -4A-M	NET 38
LIDSP*	-2A-4, -3B-11	NET 86
LIN-	-5A-1, -7A-K	NET 184
LIN+	-5A-7, -7A-J	NET 194
LL	-2B-S, -3B-J	NET 125
LNADR	-1A-C, -4A-C	NET 06
LNADV	-1A-N, -4A-S	NET 23
LNCOM	-1A-P, -3B-9	NET 24
LNDEL	-3B-M, -4A-10	NET 161
LNINS	-3B-12, -4A-L	NET 162
LNZR*	-1B-F, -4A-15	NET 51
LOAD*	-2B-P, -4A-20	NET 122
LOT-	-5A-B, -7A-P	NET 186
LOT+	-5A-4, -7A-N	NET 188
LPCOD	-3B-E, -4A-J	NET 159
LPRKY	-3A-L, -6A-16	NET 152
LPRT*	-3A-8, -5A-M	NET 147
LSTLNE	-1A-F, -4A-3, -5A-22	NET 11
L1	-1A-S, -5B-F	NET 28
MCLEN*	-1B-4, -2B-X, -3A-N, -4A-7	NET 47
MDEN*	-2B-2, -5B-M	NET 105
MEMCLK	-1B-V, -2B-10, -3B-L, -4A-21	NET 75
MEMCL1	-2B-N, -3A-W	NET 120
MEMCL2	-2A-7, -3A-V	NET 88
MEMCL3	-2A-2, -3A-18	NET 85
MEOLN*	-1A-B, -2B-4, -3B-10	NET 04
MESSG	-3A-E, -4A-P, -5B-J	NET 142
MESSIN	-3A-9, -7A-12	NET 149
METX*	-2A-9, -5B-K	NET 92
MITP	-2B-11, -3A-M	NET 117
M1PH1*	-2B-12, -3A-S	NET 119
M1PH2*	-2B-15, -3A-X	NET 124
M2PH1*	-2A-J, -3A-20	NET 91
M2PH2*	-2A-N, -3A-19	NET 98
M2TP	-2A-T, -3A-T	NET 101
M3TP	-2A-1, -3A-U	NET 84
M3PH1*	-2A-M, -3A-R	NET 96
M3PH2*	-2A-12, -3A-13	NET 97
PH1	-2A-S, -3A-16, -4A-A	NET 100
PRONLN	-3A-C, -4B-22, -6A-A	NET 138
PRTBSY	-3A-1, -8A-A	NET 133
PRTST	-3A-D, -8A-C	NET 140
PH2	-1A-10, -2A-13, -3A-14, -4A-1,-5A-20	NET 18

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED			
APPROVED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV SHEET 3 OF 6

READ*	-2A-L, -3B-14, -4B-1, -5B-10	NET 95
READT*	-4A-14, -5B-P	NET 169
REPEAT	-4B-K, -5B-8, -6A-11	NET 179
RFCLK	-2B-C, -4A-X	NET 106
ROM 1*	-1B-9, - 4B-4	NET 56
ROM 2*	-1B-10, -4B-5	NET 58
ROM 3*	-1B-L, -4B-H	NET 59
RRT	-1B-U, -2A-F	NET 73
RR1	-1B-20, -2A-5	NET 78
RR2	-1B-19, -2A-E	NET 76
RR3	-1B-X, -2A-B	NET 79
RR4	-1B-Y, -2A-A	NET 81
RR5	-1B-16, -2A-C	NET 70
RR6	-1B-15, -2B-19	NET 68
RR7	-1B-T, -2A-6	NET 71
RST*	-3A-4, -4A-9, -5A-16	NET 139
RST 1	-1A -3, -5A-S	NET 05
R1	-1B-22, -3B-17, -4B-N	NET 82
R2	-1B-W, -3B-16, -4B-13	NET 77
R3	-1B-18, -3B-S, -4B-S	NET 74
R4	-1B-Z, -3B-R, -4B-15	NET 83
R5	-1B-13, -3B-P, -4B-R	NET 64
R6G	-1A-5, -3B-N, -4B-12	NET 08
SCA	-5A-C, -7A-F	NET 187
SCF	-5A-F, -7A-H	NET 193
SCLKIN	-3A-11, -5B-20	NET 153
SCRLO*	-1A-11, -3B-20	NET 20
SCROL*	-2B-21, -3B-21, -4A-17	NET 129
SDIN	-3A-B, -5A-J	NET 136
SECT 1	-1A-9, -3B-X	NET 16
SECT 2	-1A-1, -3B-18	NET 01
SEIAIN	-5A-L, -7A-B	NET 198
SEIAOT	-5A-6, -7A-A	NET 192
SENBL	-3A-F, -8A-U	NET 144
SER	-1B-17, -4B-11	NET 72
SHEIN	-3A-J, -8A-P	NET 148
SHEIOT	-3A-K, -8A-R	NET 150
SLOC*	-3B-2, -4B-M	NET 157
SLO-2	-1B-7, -3B-T	NET 52
SL3-5	-1B-J, -3B-15	NET 55
SRLD*	-1B-C, -4B-16	NET 46
SRSTRB	-1B-3, -4A-22	NET 45
SPACE	-2B-V, -4B-7	NET 128
S1	-1B-N, -4B-T	NET 63

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			
APPROVED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV
			SHEET 4 OF 6

S2	-1B-11, -4B-F	NET 60
S4	-1B-M, -4B-14	NET 61
S8	-1B-12, -2A-11	NET 62
TAB	-1A-W, -4A-H	NET 36
TAGIN	-2B-22, -4A-12	NET 131
TAGL	-2A-21, -5A-18	NET 104
TAGM	-2A-10, -4A-18, -5A-X	NET 94
TBMT	-4A-K, -5B-9	NET 167
TIN 1	-1A-R, -2B-R, -4B-Z, -5B-5	NET 26
TIN 2	-1A-14, -2B-W, -4B-21, -5B-4	NET 25
TIN 3	-1A-M, -2B-17, -4B-Y, -5B-D	NET 21
TIN 4	-1A-V, -2B-18, -4B-20, -5B-3	NET 34
TIN 5	-1A-20, -2B-9, -4B-U, -5B-C	NET 37
TIN 6	-2B-M, -4B-17, -5A-19	NET 118
TIN 7	-2B-J, -4B-V, -5A-W	NET 115
TRDY*	-4A-T, -5B-1	NET 172
TR7*	-1A-L, -3B-19	NET 19
VDRIVE*	-1B-2, -7A-5	NET 43
VGRF*	-1B-S, -3B-K	NET 69
VIDEXT	-1A-19, -7A-1	NET 35
VIDINT	-1A-18, -7A-3	NET 33
XMIT	-4B-C, -6A-E	NET 174
2Hz	-1B-H, -5A-V	NET 53
4Hz	-1B-D, -5A-R	NET 48
30Hz	-4B-9, -5A-12	NET 178
110	-5B-Z, -7A-V	NET 213
300	-5B-Y, -7A-U	NET 211
1200	-5B-X, -7A-T	NET 209

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			
APPROVED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV
			SHEET 5 OF 6

+5	6A,2 - 6A,Y 7A,15 - 7A,Y
GND	8A,D - 8A,B - 8A,Z 7A,10 - 7A,Z 6A,1 - 6A,D - 6A,5 - 6A,F - 6A,J - 6A,9 - 6A,L - 6A,13 - 6A,17 - 6A,19 - 6A,21
-13	7A,8 - 5B,A - 6A,3

Connectors	1A,Z thru 8A,Z tied with buss bar 1A,Y thru 8A,Z tied with buss bar 1B,A thru 5B,A tied with buss bar 1B,B thru 5B,B tied with buss bar

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED			
APPROVED		WIRE LIST, BACKPLANE, CONNECTORS	DWG NO 502-451 REV SHEET 6 OF 6

FROM 25 PIN FEMALE	TO	SIGNAL NAME
PIN 1	CHASSIS GROUND	GROUND
7	JUMPER	GROUND
18	JUMPER	GROUND
2	SER SW"ON" POS 3 (SEE DRAWING)	SHEIAN
3	14	SHEIOT
4	JUMPER	
5		
6	JUMPER	
8	JUMPER	
20		
11	A3,J1 PIN 15	HCLPIN
21	CHASSIS GND	
22	TO PIN 16 OF PARALLEL DATA CONN.	
23	TO PIN 17 OF PARALLEL	
25	A3,J1 PIN 16	HCLPOT
	A3,J1 PIN 17 TO SERIAL SWITCH - SENBL	
	A3,J1 PIN 13 TO SERIAL SW.WIPER-SHEIAN	

NOTE: INSTALL DUMMY PINS ON LETTERED SIDE FOR CONTACT PRESSURE.

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			
APPROVED		980 SERIAL HARDCOPY HARNESS	DWG NO / REV
			SHEET 1 OF 1

FROM	TO	
25 PIN FEMALE CONN.	A3,J1	SIGNAL NAME
14	PIN 3	PRTST
15	" 4	PRTST GND
16	SW. 6	PRTBSY
17	PAR. SW.4	PRTBSY GND
18	A3,J1 PIN 5	B1 HC
19	" " " 6	B2 HC
21	" " " 7	B3 HC
22	" " " 8	B4 HC
23	" " " 9	B5 HC
24	" " " 10	B6 HC
25	" " " 11	B7 HC

5-13 CHASSIS GROUND DAISY CHAN

ALSO ADD A3,J1 PIN 1 SW. 5 WIPER
" " " 2 SW. 4

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED			
APPROVED		980 PARALLEL HARDCOPY HARNESS	DWG NO / REV / SHEET 1 OF 1

FROM	TO	SIGNAL NAME
A.C. RECPT. 1	SW. BRKT, PWR WIPER, 5	A.C. HOT
FUSE HOLDER	SW. BRKT, PWR WIPER, 2	A.C. FUSED
TB2,1	TB1,1	A.C. HOT, SWITCHED
TB2,2	TB1,2	A.C. FUSE, SWITCHED
TB2,1	MONITOR MOLEX, 1	A.C. HOT, SWITCHED
TB2,2	MONITOR MOLEX, 4	A.C. FUSE, SWITCHED
UL GND, R.P.	TB1,3	UL CHASSIS GND
UL GND, R.P.	A.C. RECPT. 2	UL CHASSIS GND
UL GND, R.P.	MONITOR MOLEX, 2	UL CHASSIS GND
TB1,4	SW. BRKT.	UL CHASSIS GND
A.C. RECPT. 3	FUSE HOLDER	A.C. NEU. IN
A.C. RECPT.		FUSE HOLDER
A.C. RECPT. 1		SWITCH (RESISTOR LEAD)

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			
APPROVED		980 BASIC HARNESS	DWG NO / REV
			SHEET 1 OF 1

FROM		TO	
10 PIN MONITOR CONN.		BRITE, CONT. POTS	SIGNAL NAME
A		CHASSIS	UL GROUND
E	JUMP	CHASSIS	
B		BRITE POT 1	+ BRT
C		BRITE POT 3	- BRT
D		BRITE POT	BRT WIPER
J		CON POT 2 #2 MARKER	
L		CON POT 3	SHIELD

3 INSTALL DUMMY PINS FOR CONTACT PRESSURE

8

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			DWG NO / REV
APPROVED		980 MONITOR HARNESS	SHEET 1 OF 1

FROM EIA, 25 PIN FEMALE CONN.		FROM CONN. A2,J1	SIGNAL NAME
1	JUMPER	CHASSIS	GND
7		CHASSIS	GND
2		1	SEIAOT
3		2	SEIAIN
4		3	EIARTS
5		4	EIACLS
8		5	CARDET
11		6	SCA
12		7	SCF
17		8	LIN+
18		9	LIN-
20		10	DATTRY
22		11	LBIAS
24		12	LOT+
25		13	LOT-

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED		980 EIA CONNECTOR HARNESS	DWG NO / REV
APPROVED			SHEET 1 OF 1

FROM	TO	
CONN. A2,J1		SIGNAL NAME
PIN 15	BAUD SW, 1	"B"
14	BAUD SW, 2	"A"
16	BAUD SW, 3	"1200"
17	BAUD SW, 4	"300"
18	BAUD SW, 5	"110"
19	BAUD SW, 6	F-COM
21	TB1, 5	+5V
22	TB1, 4	GND
A	BNC	VIDEXT
B	BNC LUG	VIDEXT SHIELD
C	CONT. POT, 1	VIDINT
D	CONT. POT, 3	VIDINT SHIELD
E	MONITOR PIN K	V DRIVE
F	MONITOR PIN F	H DRIVE
H	TB2, 8	CARLT
J	TB2, 7	-13V
K	SONALERT +	BELDR
L	SONALERT -	GROUND
M	TB2, 6	CONVIN
N	TB2. 5	MESSIN
P	FDX SW, 2	FDX
S	TB2, 4	+5V
Y	TB1, 7	-13V
Z	TB1, 6	+13V

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			DWG NO / REV
APPROVED		980 POWER AND ACCESSORY HARNESS	SHEET 1 OF 1

FROM	TO	
KEYBRD., 30 PIN CONN.	A1, J1	SIGNAL NAME
1	X	GND
2	B	+5B
3	C	-13V
8	L	B8KB*
9	M	REPEAT
11	R	B9KB*
12	S	CONTROL
A	1	PRINT ON
B	2	INSKEY
K	11	B7KB*
L	12	B6KB*
M	13	B5KB*
N	14	B4KB*
P	15	B3KB*
R	16	B2KB*
S	17	B1KB*

ENG'R		ADDS Applied Digital Data Systems, Inc. Hauppauge, New York	
DRAWN			
CHECKED			
APPROVED		980 KEYBOARD HARNESS	DWG NO / REV
			SHEET 1 OF 1

FROM	TO	
30 PIN LEAF	A1, J1	SIGNAL NAME
5	D	KBLOK*
	E	GND
6	F	BREAK
	H	GND
7	J	CURHOM
	K	GND
10	N	DELKEY
	P	GND
13	T	LPRKY
	U	GND
14	V	CURBAK
	W	GND
15	X	CURDWN
	Y	GND
E	3	CURFWD
	4	GND
F	5	XMIT
	6	GND
H	7	CURUP
	8	GND
J	9	KBSTB*
	10	GND

ENG'R		ADDS	Applied Digital Data Systems, Inc. Hauppauge, New York
DRAWN			
CHECKED			DWG NO / REV
APPROVED			SHEET 1 OF 1

CONSUL 980

SCHEMATICS & ASSEMBLIES

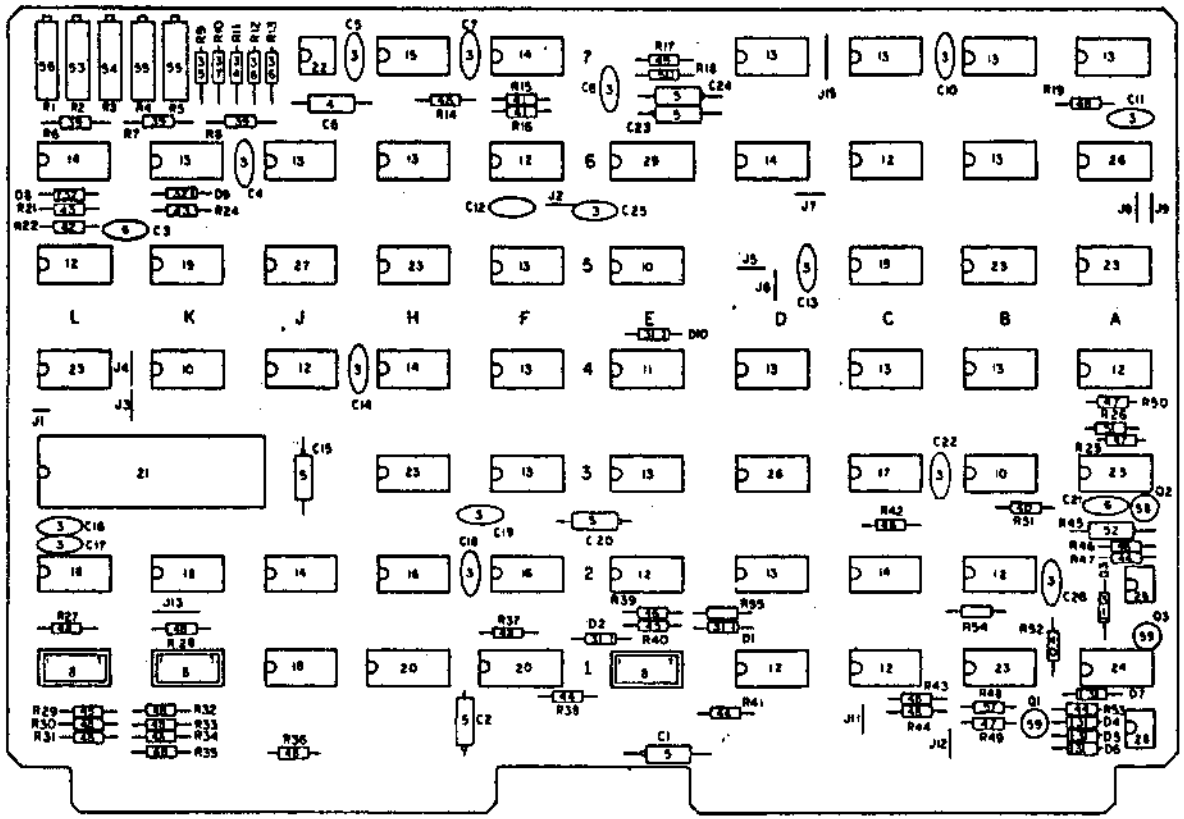
ADDS
Applied Digital Data Systems, Inc., 100 Marcus Blvd., Hauppauge, New York, 11787

IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES
SN7404	A4,B2,C1,C6,D1,E2, F6,J4,L5	SN7430	H7	LM1488	A1
		SN7437	J5	LM1489	A3
SN7402	B3,J 5,K4		A7,B4,B6,B7,C4,C7, D2,D4,D7,E3,F3,F4, F5,H6,J6,K6	DM8810	F2,H2
SN7408	C2 D6 F7 H4 J2 L6	SN7474			K3,L3
SN7405	J1,K2,L2			4N26	A0,A2
SN7408	A5,B1,B5,H3,H5,L4	SN7494	C3		
SN7410	C5,F5	SN74123	E6		
SN7411	A6,D3	SN74175	F1,H1		
SN7420	E4	LM311	J7		

ADDS

SCHEMATIC DIAGRAM
ASYN/FE

135-088 E B



REV	DESCRIPTION	DATE	APPROVED
B	ECO 650-115		

ADDS

ASSEMBLY
ASYN/FE

129-088 D

		SN7473	D7 K4 L3
DM8123	A1,B1	SN7450	C5
SN74195	A2,4, C1	SN7442	J3
SN74192	B2,B4	SN7420	A5,B6,C6,K2
SN74175	J6, K1,6, L1	SN7411	E4,L2,8
SN74162	J2	SN7410	C4,F3,7,M4
SN7493	D6	SN7408	E3,M6,J5,K3,5
SN7486	F5, H1	SN7404	A7,D2,E7,F2,M2
SN7485	A3,B3,C2,M4	SN7402	B5,C3,F4,M5
SN7474	D4,5,E5,F6,J7, L4,7,	SN7400	A6,D1,3,E6,F1,M3,J1,5
IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES

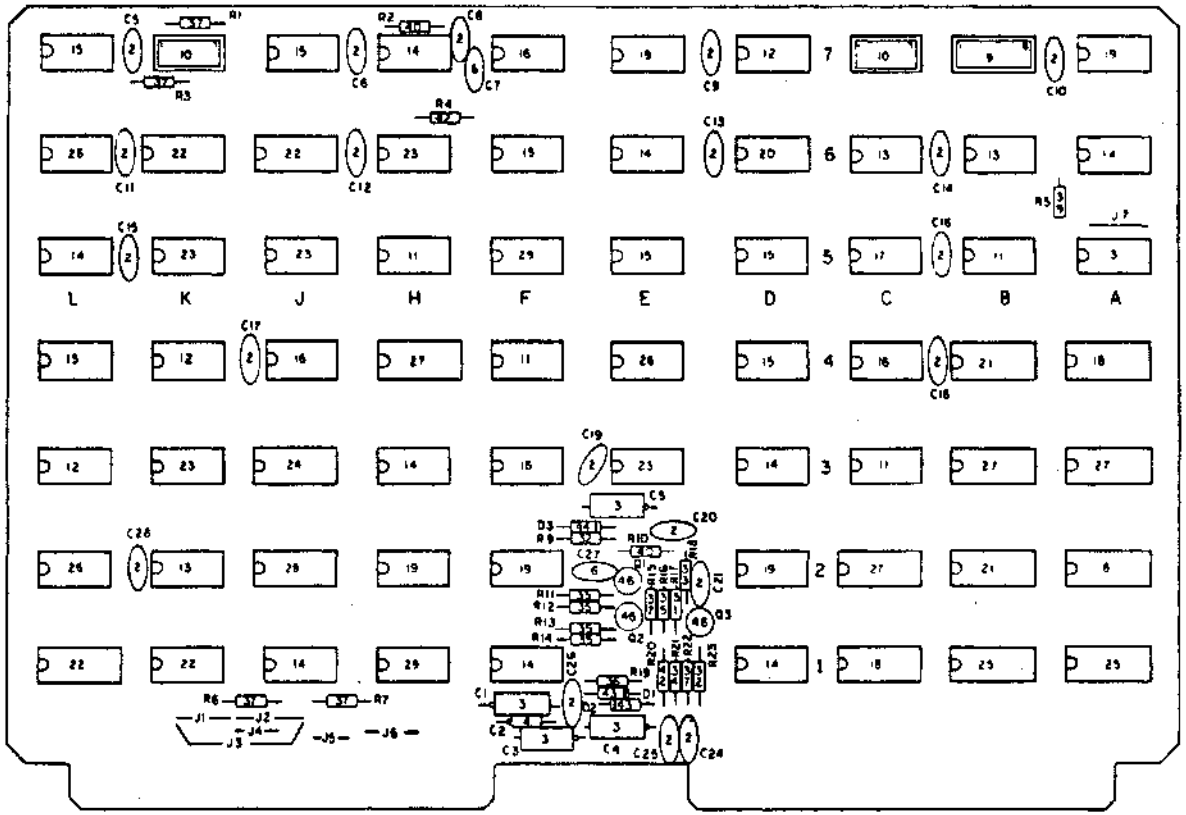
3

ADDS

SCHEMATIC DIAGRAM

VIDGEN

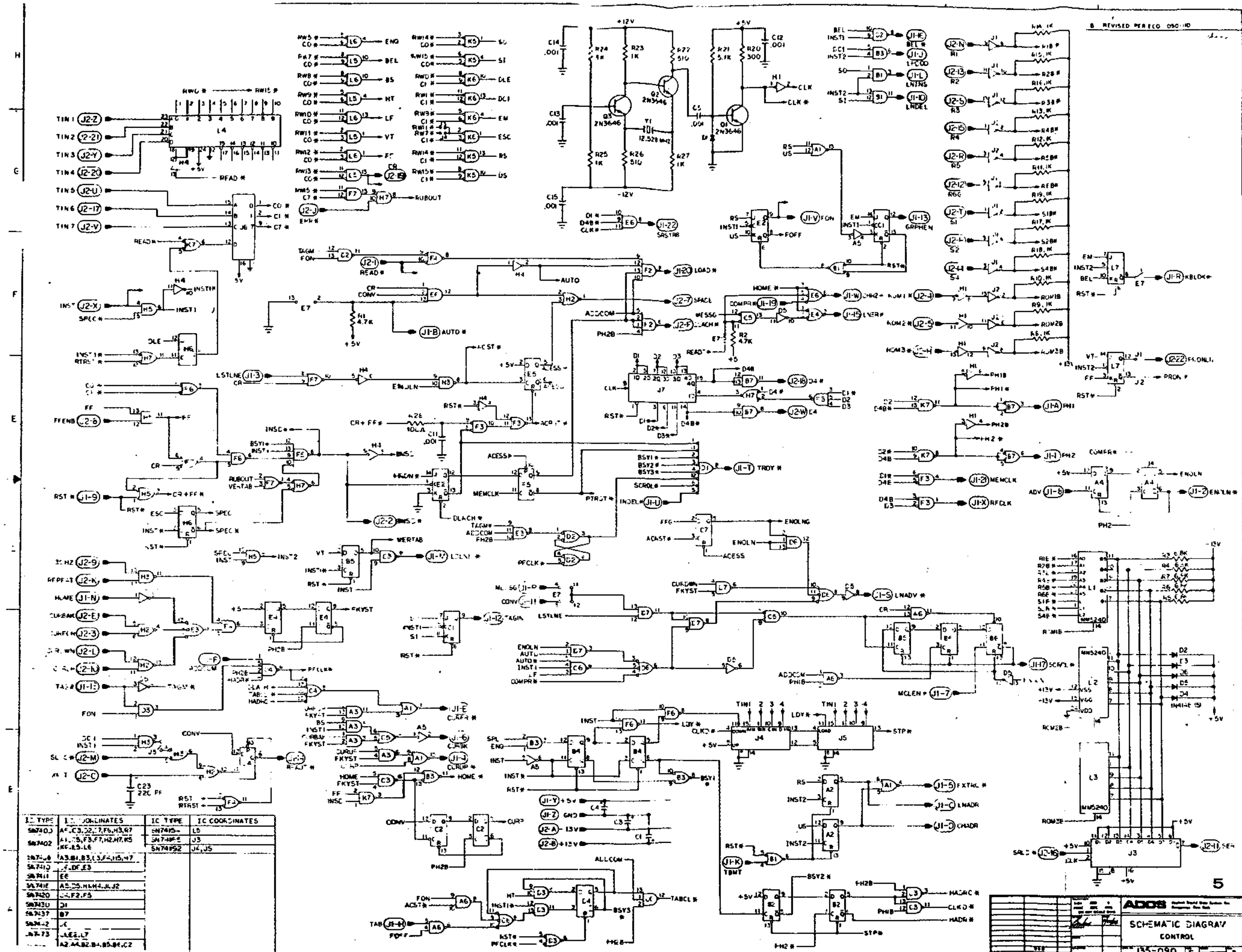
135-089



ADDS

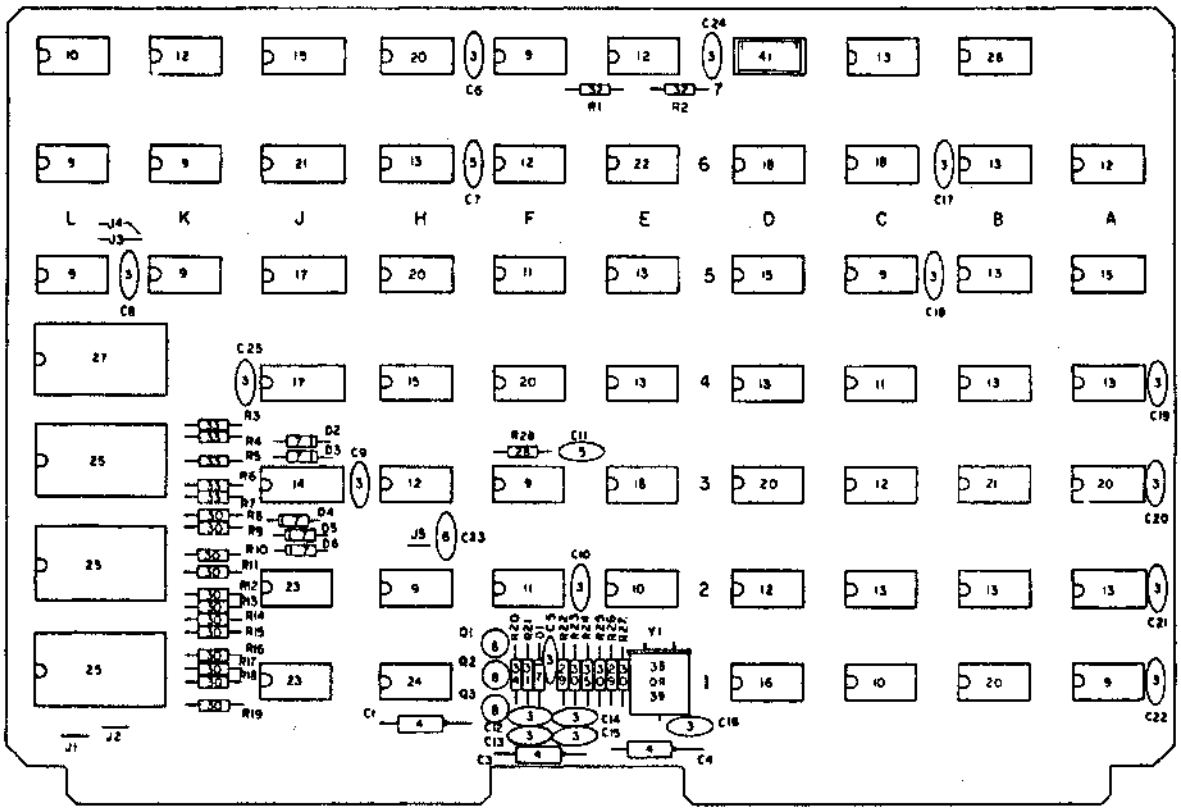
ASSEMBLY
VIDGEN

129-089 D



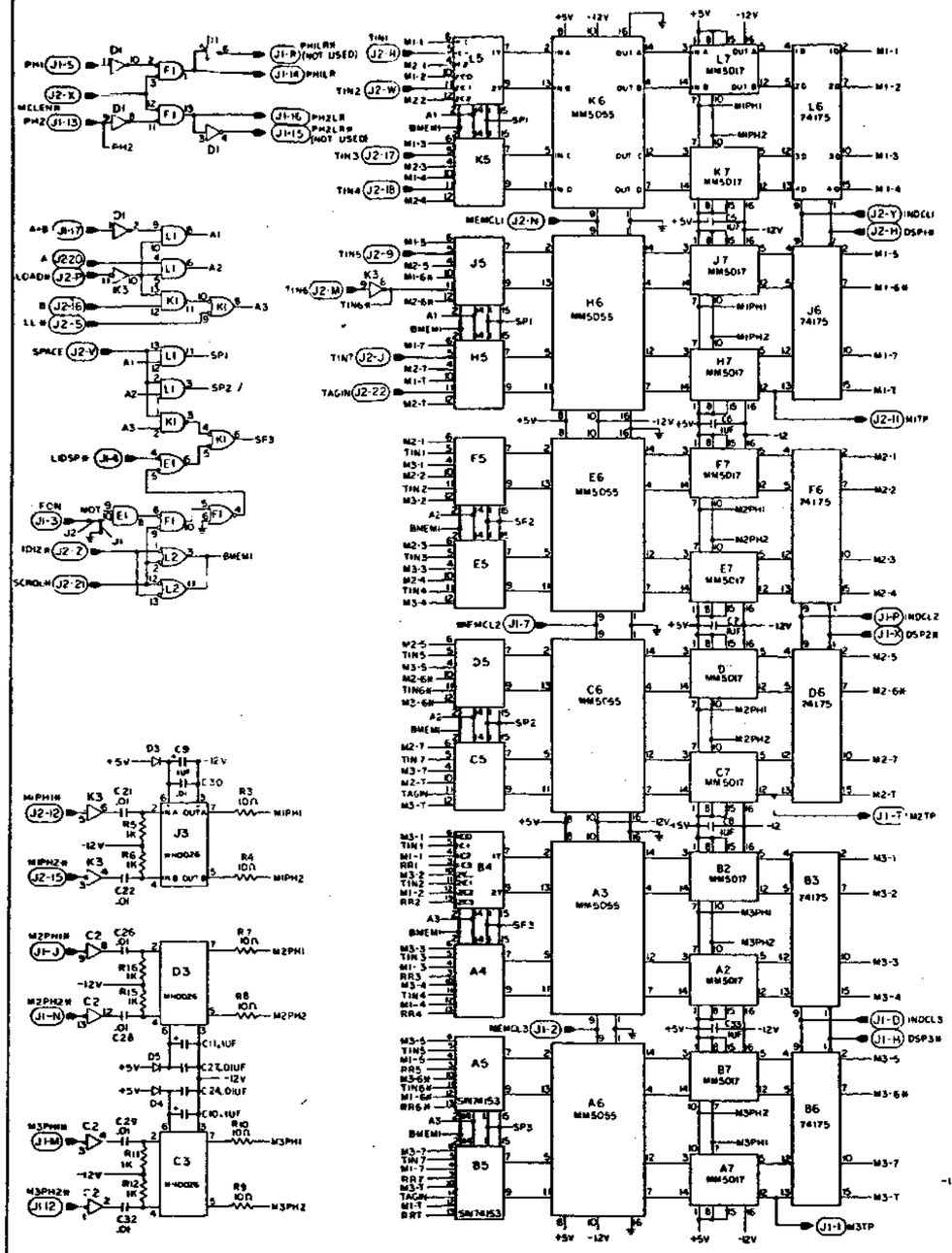
IC TYPE	IC COORDINATES
SN7400	A6,C3,D2,E7,F6,H3,K7
SN7402	A1,C5,F3,F7,H2,H7,K5,K6,E5,L6
SN7404	A3,B1,B3,C3,F4,H5,H7
SN7410	[illegible],D6,E3
SN7411	E6
SN7414	A5,D5,H1,H4,J1,J2
SN7420	C4,F2,F5
SN7430	D1
SN7437	B7
SN7442	L6
SN7473	C1,E2,L7
	A2,A4,B2,B4,B5,B6,C2

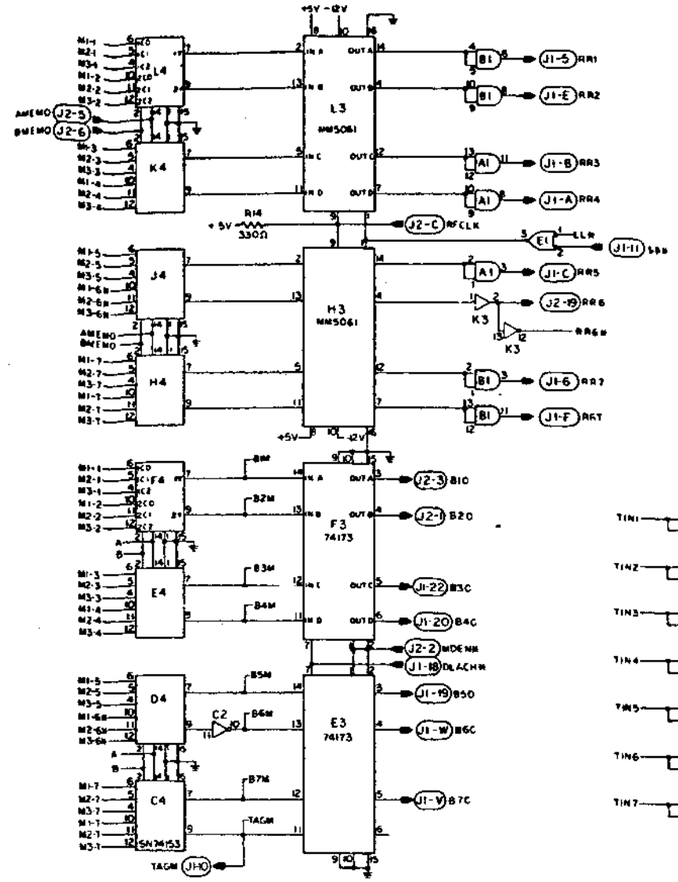
IC TYPE	IC COORDINATES
SN74154	L5
SN74165	J3
SN74192	J4,J5



ASSEMBLY
CONTROL

129-090 D



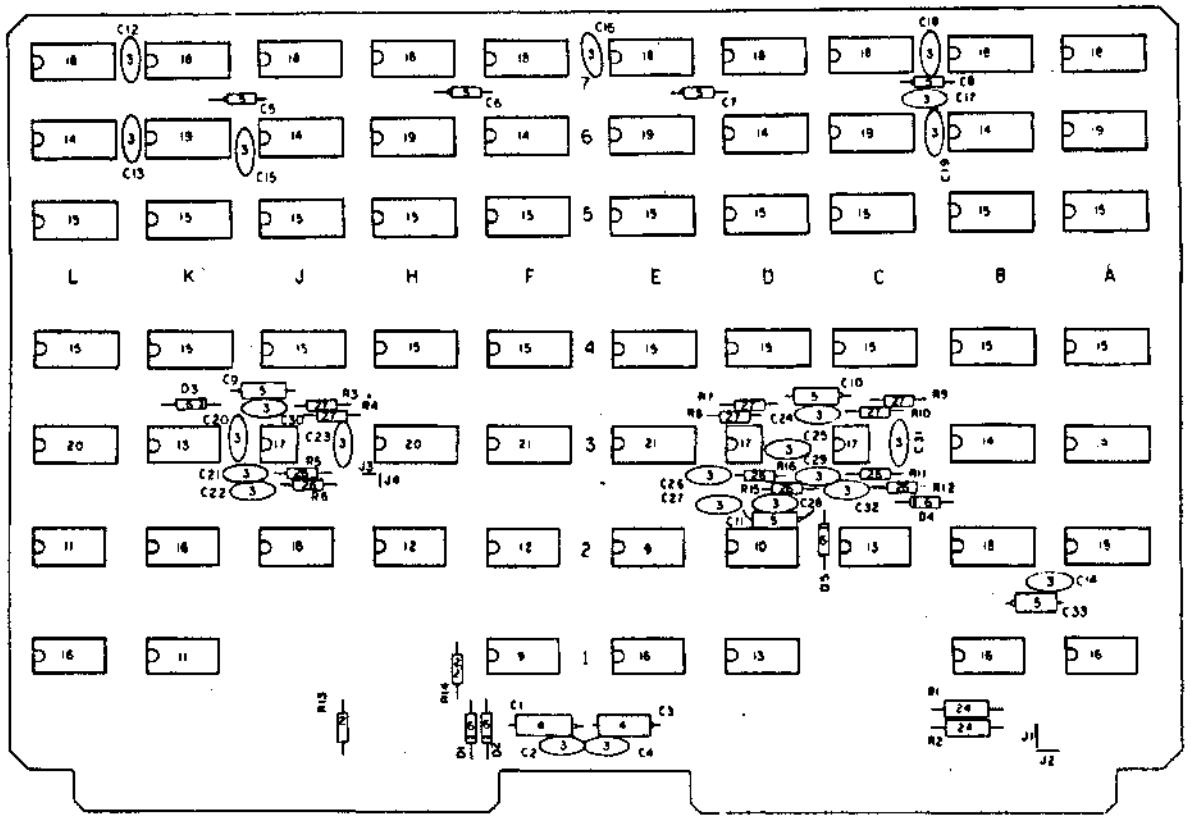


SN7474	F2, M2
SN7420	D2
SN7408	A1, B1, E1, G2, G2, L1
SN7406	C2, D1, K3
SN7402	E2, F1
SN7400	L2, E1
IC TYPE	IC COORDINATES

ADDS

SCHEMAT C DIAGRAM
MEMORY

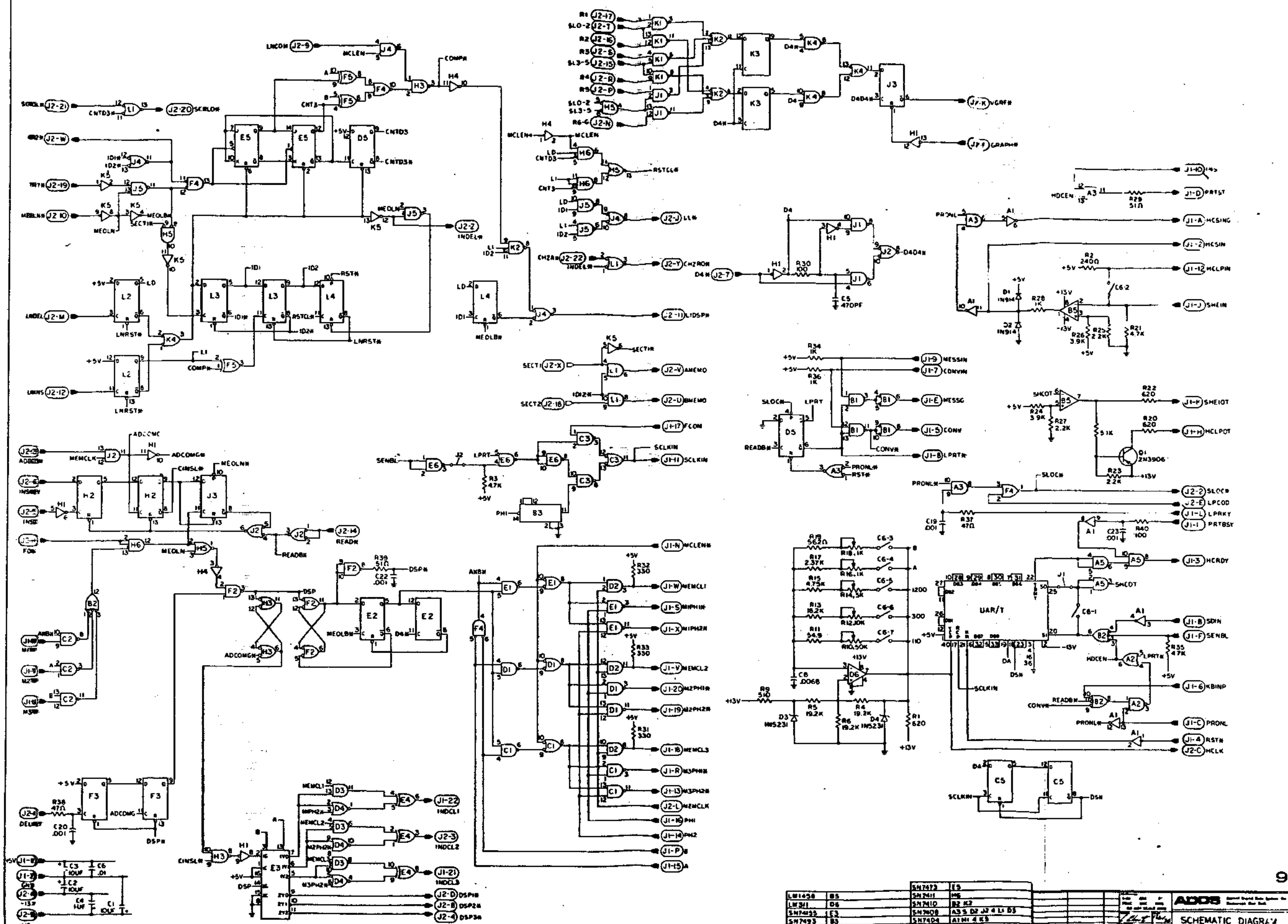
135-091 E



ADDS

ASSEMBLY
MEMORY

129-091 D



9

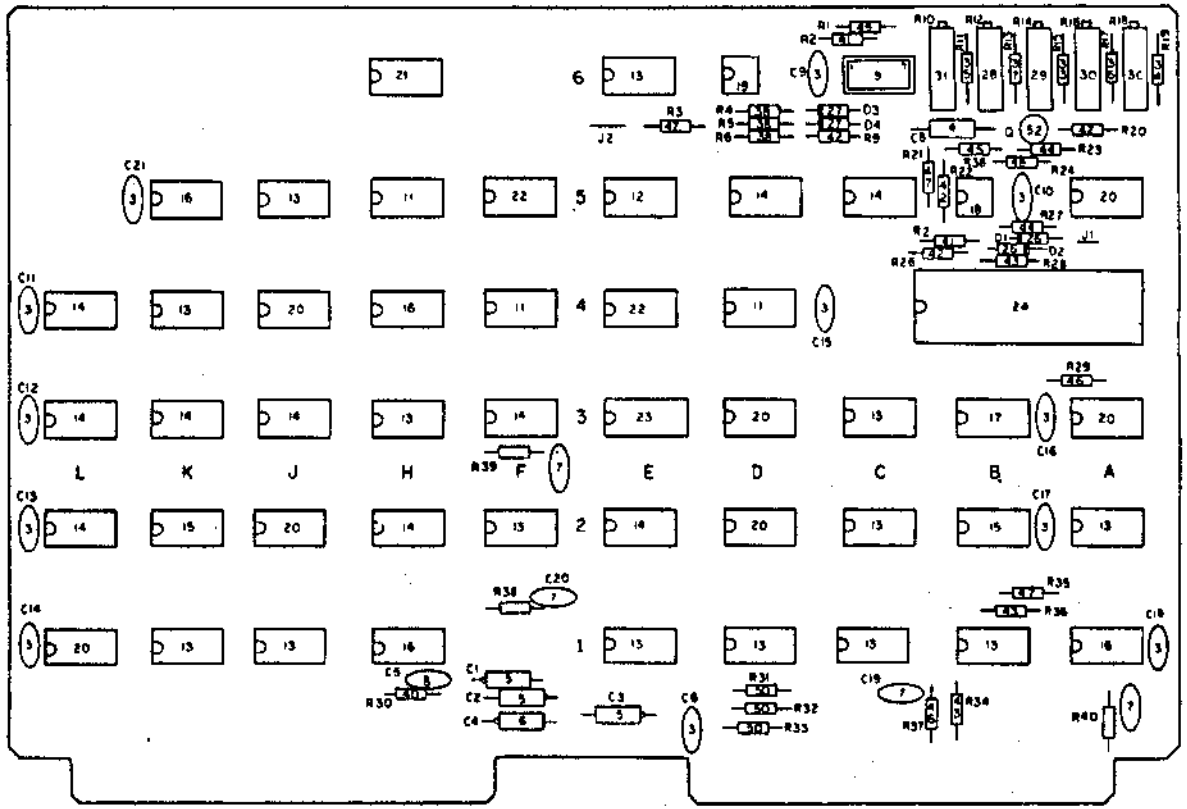
IC TYPE	IC COORDINATES	IC TYPE	IC COORDINATES
		SN7473	E5
LM1458	B5	SN7411	H5
LM311	D6	SN7410	B2 K2
SN74155	E3	SN7408	A3 5 D2 J2 4 L1 D3
SN7493	B3	SN7404	A1 H1 4 K5
SN7486	E4 F5	SN7402	D4 F4 H5
SN7474	L2,3,4, C5, D5, E2, F3, H2, J3, K3,	SN7400	H3, J1, 5, [illegible]

ADDS

SCHEMATIC DIAGRAM

OPTION BOARD

135-092 E



ASSEMBLY
OPTION

129-092