

**SA810/860**  
**Single/Double-Sided**  
**Half Height**  
**Diskette**  
**Storage Drive**

**Service Manual**

**Shugart**

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# SECTION I INTRODUCTION

## 1.1 GENERAL DESCRIPTION

The compact SA810 single-sided and SA860 double-sided half-height 8-inch floppy disk drives offer a reliable, low cost, high performance solution for OEM data storage applications which require maximum capacity in the smallest space possible. The SA810/860 drives are less than half the height of the Shugart SA801 and SA851 floppy disk drives, fit in comfortably with a CRT, require no ac voltage, and offer up to 1.6 megabytes of unformatted capacity.

The SA810/860 offers the following standard features:

- a. Half-height sizing: 2.31 in. (59 mm) high by 8.55 in. (217 mm) wide by 12.00 in. (305 mm) deep
- b. Interface and media compatibility with Shugart SA801/851 disk drives
- c. Low heat dissipation
- d. Fast access time (3 ms track to track)
- e. Quiet operation
- f. Low media wear due to low mass head
- g. Rapid start dc drive motor--less than one revolution (eliminates ac requirements)
- h. Phase-Locked Loop Crystal Referenced Motor Speed Control
- i. Media compatible with SA801/851 plus IBM 3740
- j. Single or double density
- k. 0.8/1.6M Bytes (unformatted capacity)
- l. Write protect and programmable door lock for improved data security
- m. Internal write current switching
- n. TRUE READY alerts the system that the drive is ready to send or receive data
- o. Buffered seek
- p. Single or multiple drive dc Motor On control
- q. Multiple jumper options
- r. Shugart's proprietary Bi-Compliant read/write heads with straddle erase elements
- s. Extended reliability
- t. Activity light
- u. Solid die cast chassis
- v. Light weight
- w. Inline dc and I/O connectors

The SA810/860 provides the best solution to the user looking for a compact, low cost, and reliable 8-inch floppy disk drive. The SA810/860 is the most versatile disk drive on the market. This drive is backed by an engineering department that is recognized as the largest, most experienced group in the entire floppy industry. The SA810/860 is the ultimate solution for small business systems, intelligent terminals, personal computer systems, and program storage equipment.

## 1.2 SPECIFICATIONS SUMMARY

### 1.2.1 Performance Specifications

	<b>SA810</b>	<b>SA860</b>
Capacity	Single/Double Density	Single/Double Density
Unformatted		
Per Disk	400/800 k bytes	0.8/1.6 M bytes
Per Surface	400/800 k bytes	400/800 k bytes
Per Track	5.2/10.4 k bytes	5.2/10.4 k bytes

	<b>SA810</b> Single/Double Density	<b>SA860</b> Single/Double Density
<b>IBM Format</b> (128 byte sectors)		
Per Disk	250/500 k bytes	500/1000 k bytes
Per Surface	250/500 k bytes	250/500 k bytes
Per Track	3.3/6.66 k bytes	3.3/6.66 k bytes
Transfer Rate	250/500 k bits/sec	250/500 k bits/sec
Latency (average)	83 ms	83 ms
<b>Access Time</b>		
Track to Track	3 ms	3 ms
Settle Time	13 ms	13 ms
One Track Seek & Settle	16 ms	16 ms
Average (including settle)	89 ms	89 ms
<b>Motor Start Time</b>		
Worst Case	165 ms	165 ms
Typical	120 ms	120 ms

### 1.2.2 Functional Specifications

Rotational Speed	360 ± 2 rpm	360 ± 2 rpm
Recording Density (inside track)	3268/6536 bpi	3408/6816 bpi
Flux Density	6536 fci	6816 fci
Track Density	48 tpi	48 tpi
Tracks	77	154
Index	1	1
Encoding Method	FM/MFM	FM/MFM
<b>Media Requirements</b>		
Soft Sector	SA100/102	SA150
32 Sector Hard Sector	SA101/103	SA151
Alignment Diskette	SA120	SA122

### 1.2.3 Physical Specifications

	<b>Operating</b>	<b>Shipping</b>
<b>Environmental Limits</b>		
Ambient Temperature:	50° to 115°F (9.9° to 46.1°C)	-40° to 144°F (-40° to 62.2°C)
Relative Humidity:	20% to 80%	1% to 95%
Maximum Wet Bulb:	85°F (29.4°C)	no condensation
	<b>Storage</b>	
	-8° to 122°F (-22.2° to 50°C)	
	1% to 95%	
	no condensation	

#### DC Voltage Requirements:

- +24.00 ± 2.4 V dc @ 1.0 A typ., 1.7 A max., 100 mV ripple.
- +5.00 ± 0.25 V dc @ 0.7 A typ., 0.7 A max., 50 mV ripple.

#### NOTE

If the stepper motor is energized by the controller during the single motor start-up time, the drive will exceed the +24 V dc current specification of 1.7 A max. Under this condition, the current specification is 2.2 A max.

#### Mechanical Dimensions

- Width = 8.55 in. (217 mm)
- Height = 2.31 in. (59 mm)
- Depth = 12.00 in. (305 mm)
- Weight = 7 lbs (3 kg)

## Mounting

- Top loading
- Diskette Horizontal Label Up/Down
- Diskette Vertical Label Left/Right

## Power Dissipation:

- 10 watts (34.2 BTU/hr) Standby
- 28 watts (94.0 BTU/hr) Typical
- 50 watts (171 BTU/hr) Maximum

### 1.2.4 Reliability Specifications

Mean Time Between Failure: 10,000 Power On Hours under typical usage.

Preventive Maintenance: Not required.

Mean Time to Repair: 30 Minutes

Component Life: 5 years

#### Error Rates:

- |                   |                           |
|-------------------|---------------------------|
| Soft Read Errors: | 1 per $10^9$ bits read    |
| Hard Read Errors: | 1 per $10^{12}$ bits read |
| Seek Errors:      | 1 per $10^6$ seeks        |

#### Media Life:

- Passes per Track:  $3.5 \times 10^6$
- Insertions: 30,000 +

## 1.3 FUNCTIONAL CHARACTERISTICS

The 810/860 floppy disk drives consist of:

- a. Read/Write and Control Electronics
- b. Drive Mechanism
- c. Precision Track Positioning Mechanism
- d. Read/Write Head(s)

### 1.3.1 Electronics

The electronics are packaged on one PCB which contains:

- a. Index Detector Circuits (Sector/Index for Hard Sector Media)
- b. Head Position Actuator Driver
- c. Read/Write Amplifier and Transition Detector
- d. Write Protect
- e. Drive Select Circuits
- f. Spindle Motor Control
- g. Data/Clock Separation Circuits (FM Only)
- h. Drive Ready Detector Circuit
- i. Drive True Ready Detector Circuit
- j. Side Select Circuit (Used on SA860 Only)
- k. In Use and Door Lock Circuits
- l. Internal and External Write Current Switching
- m. Power on Reset Circuit
- n. Activity LED

### 1.3.2 Drive Mechanism

The Head Positioning Actuator moves the read/write head(s) to the desired track on the diskette. The head(s) is loaded onto the diskette when the door knob is closed. If no diskette is inserted when the door knob is closed, the heads will not touch each other.

The dc drive motor under phase locked loop speed control (using an integral tachometer) rotates the spindle at 360 rpm. A contracting collet/spindle assembly provides precision media positioning and clamping to ensure data interchange. A diskette ejector places the diskette within reach of the operator when the diskette is unclamped.



### **1.3.3 Positioning Mechanism**

The read/write head assembly is accurately positioned through the use of a precision HeliCam V-groove lead screw with a flat nut follower which is attached to the head carriage assembly. Precise track location is accomplished as the lead screw is rotated in discrete increments by a stepping motor.

### **1.3.4 Read/Write Heads**

The proprietary head(s) is a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus, normal interchange tolerances between media and drives will not degrade the signal to noise ratio and diskette interchangeability is ensured.

The read/write head(s) is mounted on a carriage which is located on precision carriage ways. The diskette is held in a plane perpendicular to the read/write head(s) by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head(s). The read/write head(s) is in direct contact with the diskette. The head surfaces have been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette with minimum head/diskette wear due to the low mass suspension system.

### **1.3.5 Recording Formats**

The format of the data recorded on the diskette is totally a function of the host system. This format can be designed around the user's application to take maximum advantage of the total available bits that can be written on any one track.

Figure 1-2 provides a functional diagram of the SA810/860.

## **1.4 FUNCTIONAL OPERATIONS**

### **1.4.1 Power Sequencing**

Applying dc power to the SA810 or SA860 can be done in any sequence; however, during power up, the WRITE GATE line must be held inactive or at a high level. After application of dc power, a 90 ms delay should be introduced before a seek operation or before the control output signals are valid. After powering on, the initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on and internal write current switching at the proper track, a STEP OUT operation should be performed until the TRACK 00 line becomes active (recalibrate).

### **1.4.2 Drive Selection**

Drive selection occurs when the DRIVE SELECT line in the drive is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the DRIVE SELECT line enables the input and output lines, starts the spindle motor, locks the door, and lights the Activity LED on the front of the drive.

### **1.4.3 Motor On**

In order for the host system to read or write data, the dc drive motor must be turned on. In the standard configuration, this is accomplished by activating the line DRIVE SELECT. A 165 ms delay must be introduced after activating this line (or the TRUE READY line may be monitored) to allow the motor to come up to speed before reading or writing can be accomplished. All motors in a daisy chain configuration can be turned on with the optional MOTOR ON line or the spindle motor may be activated when both MOTOR ON and DRIVE SELECT are present.

In the standard configuration, the host system turns off the motor by deactivating the DRIVE SELECT line. This should be done if the drive has not received a new command within 2.6 seconds (16 revolutions of diskette) after completing the execution of a command. This will ensure maximum motor and media life. Also, the 2.6 second delay function may be performed by the drive by jumpering the optional MOTOR OFF delay.

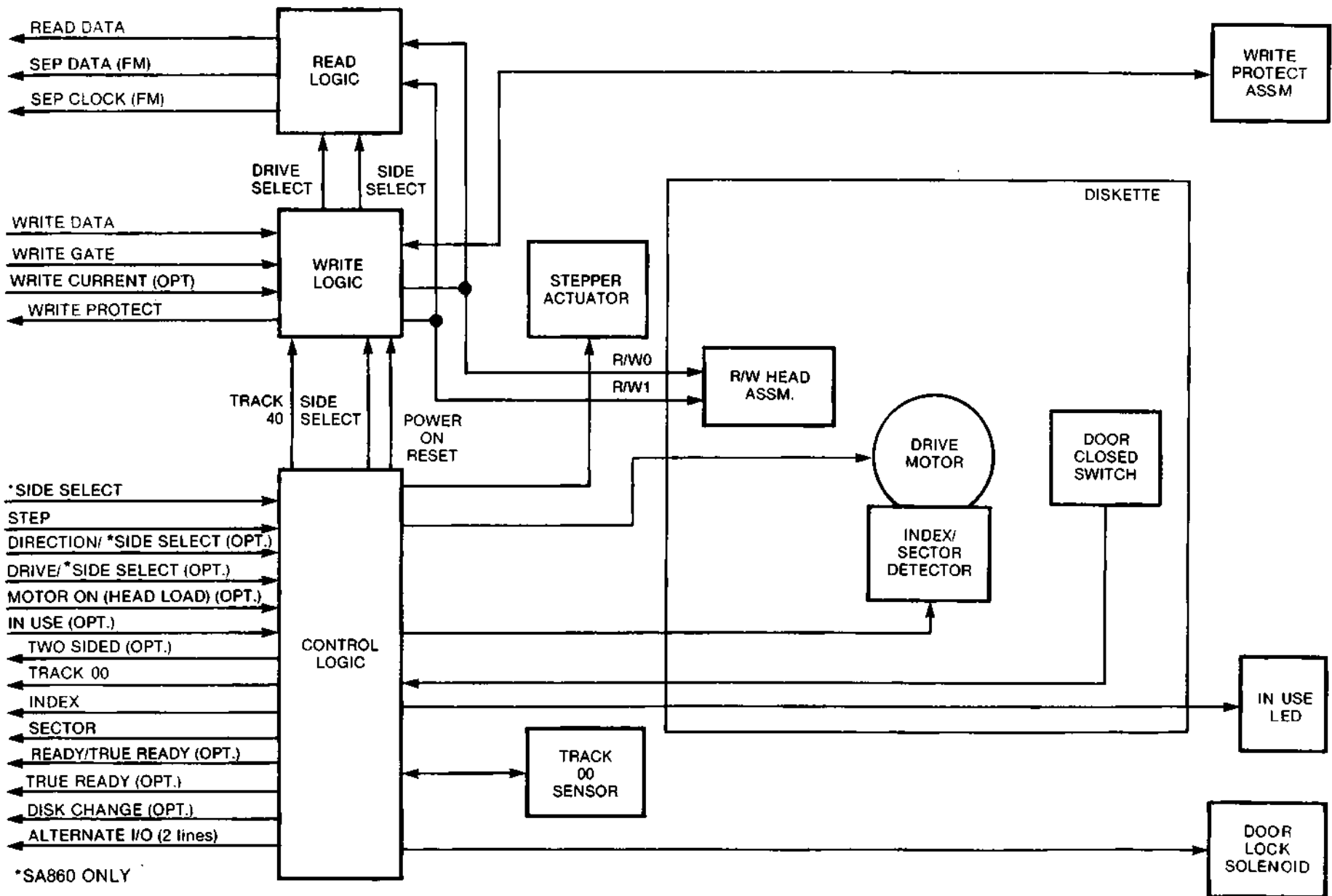


FIGURE 1-2. SA810/860 FUNCTIONAL DIAGRAM

### 1.4.4 Track Accessing

Seeking the read/write heads from one track to another is accomplished by:

- Activating DRIVE SELECT line.
- Selecting desired direction utilizing DIRECTION SELECT line.
- WRITE GATE being inactive.
- Pulsing the STEP line.

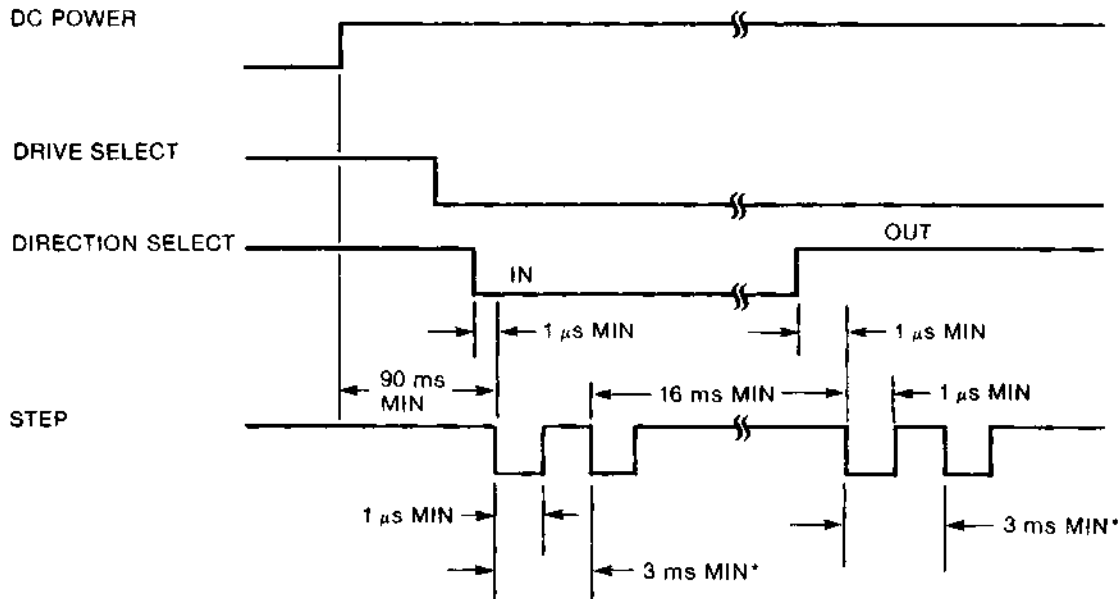
Multiple track accessing is accomplished by repeated pulsing of the STEP line until the desired number of steps have been input. Each pulse on the STEP line will cause the read/write heads to move one track either in or out depending on the DIRECTION SELECT line. Head movement is initiated on the leading edge of the STEP pulse. Pulses received at less than a 3 ms period, but greater than 15  $\mu$ s, will be stored in a buffer which will then issue step commands to the drive stepper motor at a 3 ms pulse rate. Pulses received at greater than a 3 ms period will step the drive at the same rate they are received. The first step begins upon receipt of the first step pulse.

### 1.4.5 Step Out

With the DIRECTION SELECT line at a plus logic level (2.5 V to 5.25 V), a pulse on the STEP line will cause the read/write heads to move one track away from the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in figure 1-3 or figure 1-4.

### 1.4.6 Step In

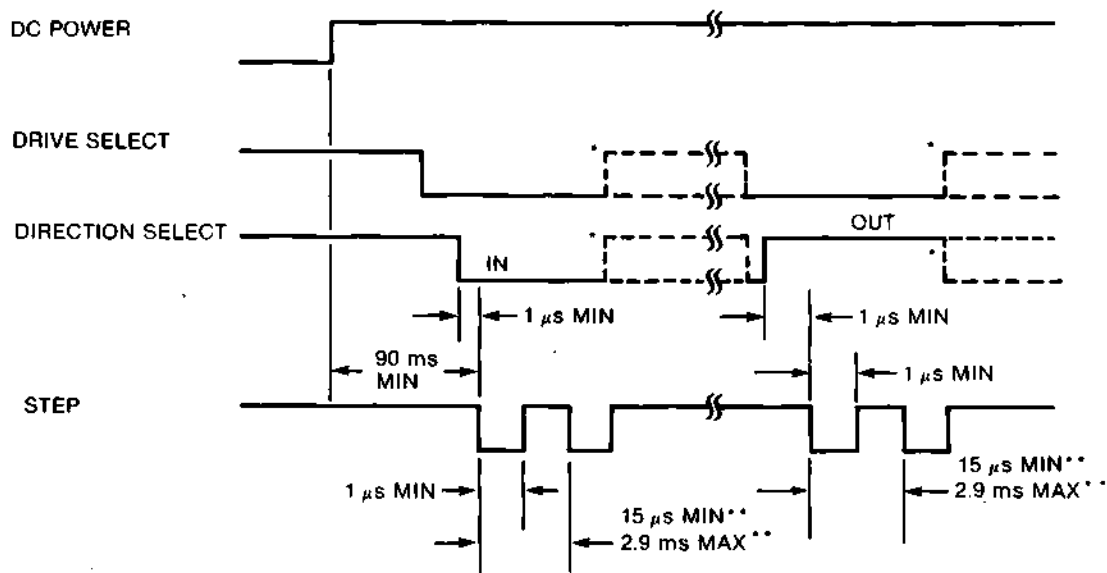
With the DIRECTION SELECT line at a minus logic level (0 V to 0.4 V), a pulse on the STEP line will cause the read/write heads to move one track closer to the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in figure 1-3 or figure 1-4.



\*3 ms is the minimum frequency for a standard seek. Pulses received at less than a 3 ms frequency will go into a buffered seek mode. See figure 1-4.

39216-03

**FIGURE 1-3. TRACK ACCESS TIMING, STANDARD SEEK**



\*After the last step pulse has been issued the drive may be deselected. The drive ignores any change to the DIRECTION SELECT line when no further step pulses are received. This frees the controller to issue instructions to other drives while the first drive completes the step commands stored in the buffer.

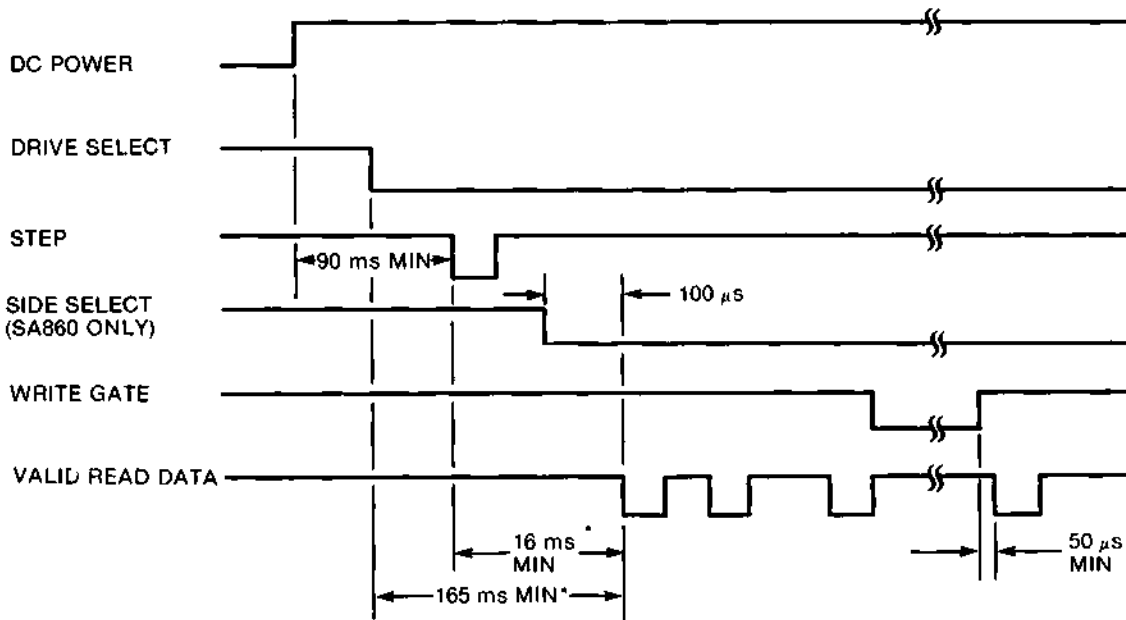
\*\*Pulses received at less than a 3 ms period will be stored in a buffer which will then issue step commands to the drive stepper motor at a 3 ms pulse rate. Pulses received at greater than a 3 ms period will step the drive at the same rate they are received. The first step begins upon receipt of the first step pulse.

39216-31

**FIGURE 1-4. TRACK ACCESS TIMING, BUFFERED SEEK**

**1.4.7 Side Selection (SA860 Only)**

Head selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the diskette. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100 μs delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Figure 1-5 shows the use of SIDE SELECT prior to a read operation.



\*Or when TRUE READY comes active.

39216-04

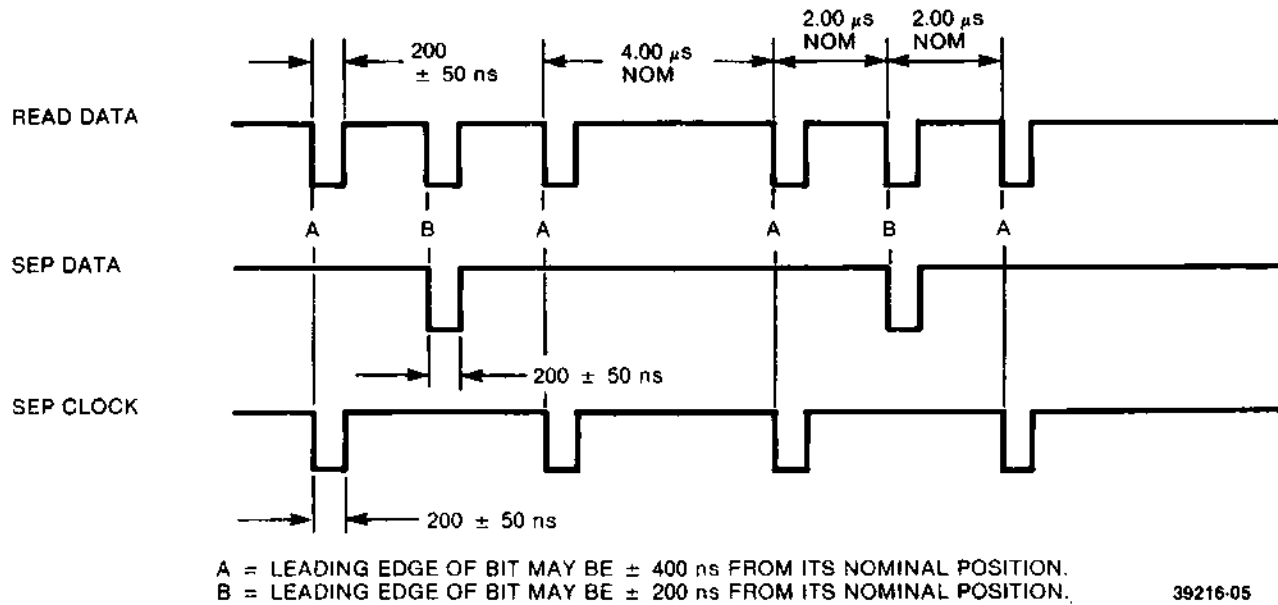
**FIGURE 1-5. READ INITIATE TIMING**

### 1.4.8 Read Operation

Reading data from the SA810/860 drive is accomplished by:

- a. Activating DRIVE SELECT line.
- b. Selecting head (SA860 only).
- c. WRITE GATE being inactive.

The timing relationships required to initiate a read sequence are shown in figure 1-5. These timing specifications are required in order to guarantee that the position of the read/write head has stabilized prior to reading. The timing of READ DATA (FM) is shown in figure 1-6.



**FIGURE 1-6. READ SIGNAL TIMING (FM ENCODING)**

The encoding scheme of the recorded data can be FM or MFM. The first of these, FM, provides single-density recording. The superior efficiency of MFM permits the bit cell period to be half that of the FM code, thereby providing double-density recording. Differences among FM and MFM encoding are concerned with the use of clock bits in the write data stream.

FM encoding rules specify a clock bit at the start of every bit cell. MFM encoding rules allow bits to be omitted from some bit cells, when either the preceding bit cell or the current bit cell contains a data bit. See figure 1-7.

In both of these encoding schemes, clock bits are written at the start of their respective bit cells and data bits at the center of their bit cells.

The timing of the read signals, READ DATA, SEPARATED DATA, and SEPARATED CLOCK are shown in figure 1-6 (FM encoding).

In the standard SA810/860, data separation of FM data is performed by the drive electronics. Data bits are presented to the controller on the SEP DATA line and clock bits are presented on the SEP CLOCK line. In systems using MFM encoding, data separation is performed outside the drive. In such cases, the READ DATA line carries both clock bits and data bits. Separation of MFM encoded read data should be controlled by a phase-locked loop circuit.

For additional information regarding the use of MFM encoding, refer to the SA810/860 OEM Manual (P/N 39216-2).

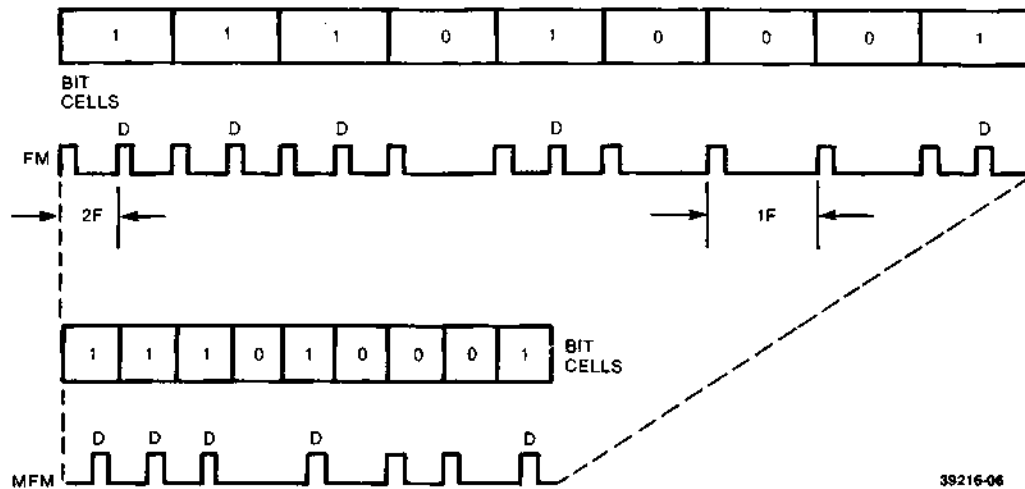


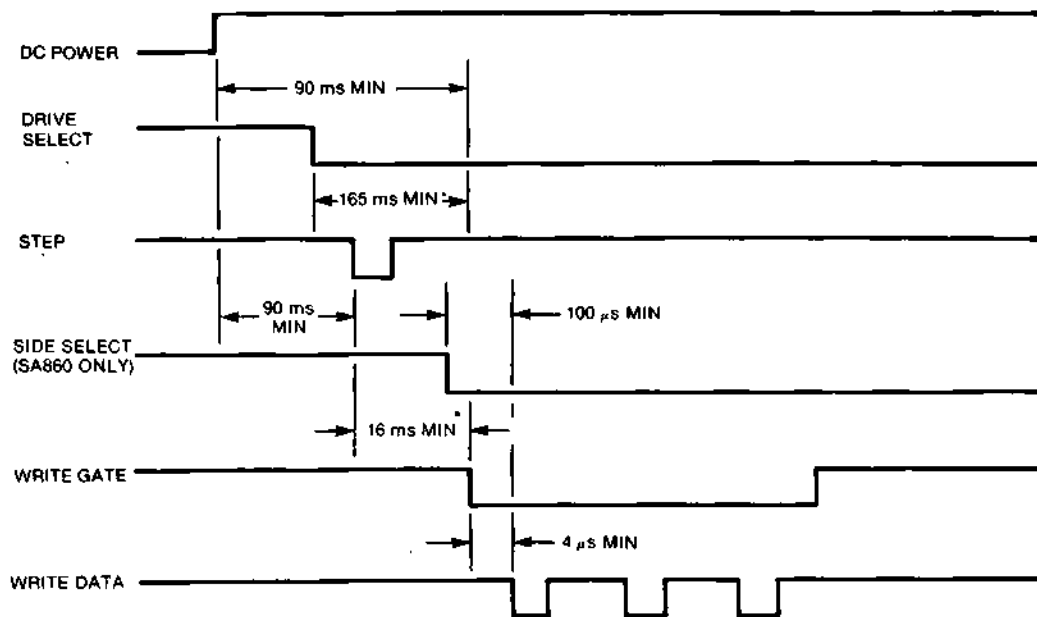
FIGURE 1-7. FM AND MFM CODE COMPARISONS

### 1.4.9 Write Operation

Writing data to the SA810/860 is accomplished by:

- a. Activating DRIVE SELECT line.
- b. Selecting head.
- c. Activating WRITE GATE line.
- d. Pulsing WRITE DATA line with data to be written.
- e. Head current switching.

The timing relationships required to initiate a write data sequence are shown in figure 1-8. These timing specifications are required in order to guarantee that the read/write head position has stabilized prior to writing.



\* Or when TRUE READY comes active

39216-07-A

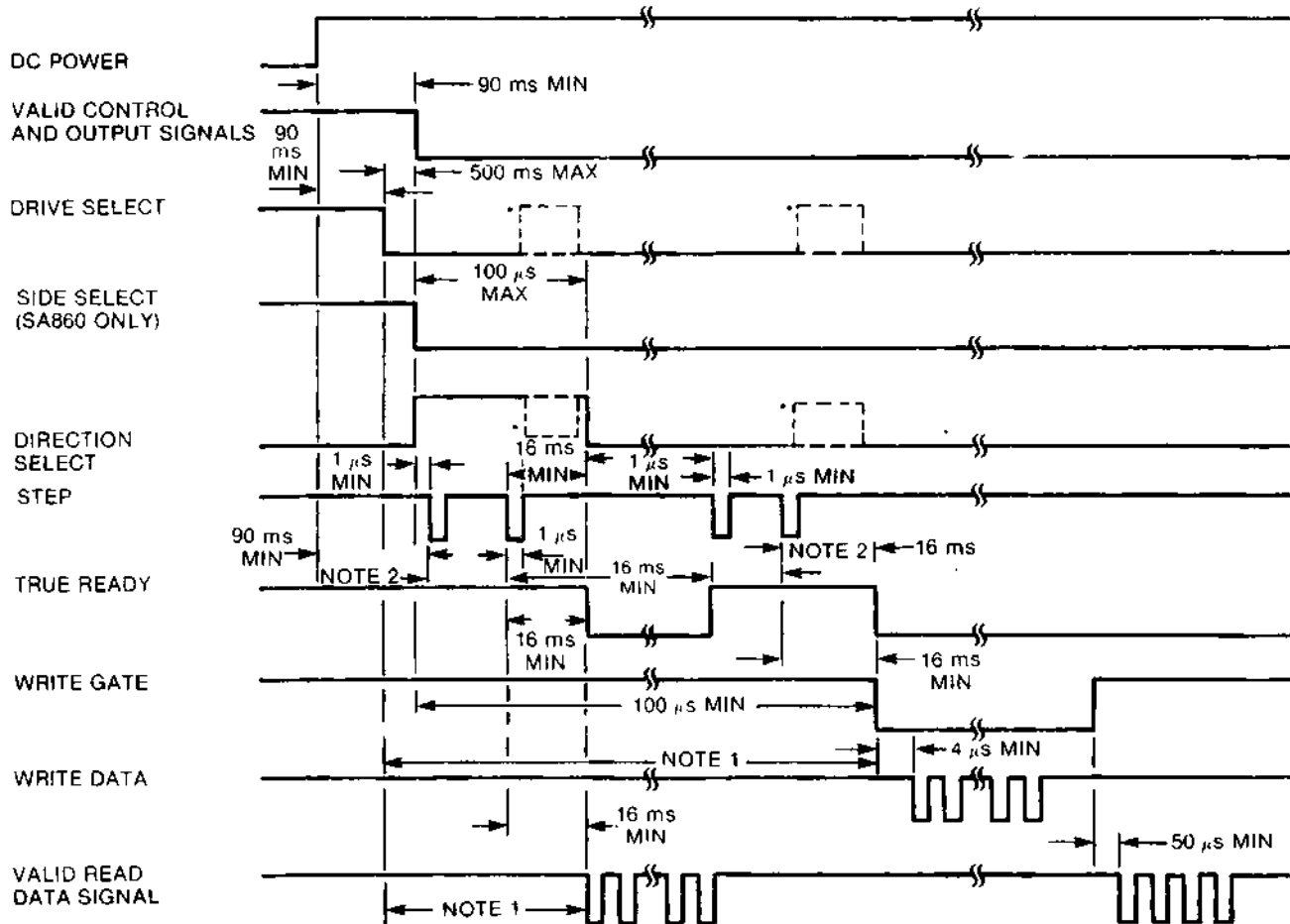
FIGURE 1-8. WRITE INITIATE TIMING

Write data encoding can be FM or MFM. If MFM is used, the write data should be precompensated to counter the effects of bit shift. The amount and direction of compensation required for any given bit in the data stream depends on the pattern it forms with nearby bits.

For more details regarding data encoding and formatting for SA810/860 drives, refer to the OEM manual (P/N 39216).

### 1.4.10 Sequence Of Events

The timing diagram shown in figure 1-9 illustrates the necessary sequence of events with associated timing restrictions for proper operation.



NOTE 1: 165 ms minimum delay must be introduced after DRIVE SELECT to allow time for the dc motor to reach 360 rpm or the optional TRUE READY line must be monitored.

NOTE 2: If performing standard seeks, the minimum frequency is 3 ms between steps. If utilizing the drive in the buffered seek mode of operation the frequency shall be 15 μs to 2.9 ms between pulses.

\*After the last step pulse has been issued, the drive may be deselected. The drive ignores any change to the DIRECTION SELECT line when no further step pulses are received. This frees the controller to issue instructions to other drives while the first drive completes the step commands stored in the buffer.

39216-08-A

**FIGURE 1-9. SA810/860 GENERAL CONTROL AND DATA TIMING REQUIREMENTS**

## **SECTION II ELECTRICAL INTERFACE**

### **2.1 INTRODUCTION**

The interface of the SA810/860 Diskette Drive can be divided into two categories:

- a. Signal Interface
- b. Power Interface

The following paragraphs provide the electrical definition for each line. See figure 2-1 for all interface connections.

### **2.2 SIGNAL INTERFACE**

The signal interface consists of two categories:

- a. Control Lines
- b. Data Transfer Lines

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

#### **2.2.1 Input Lines**

There are twelve signal input lines. Nine are standard and three are user installable options.

The input signals are of three types, those intended to be multiplexed in a multiple drive system, those not intended to be multiplexed, and those which will perform the multiplexing.

The input signals which are intended to do the multiplexing are:

- a. DRIVE SELECT 1
- b. DRIVE SELECT 2
- c. DRIVE SELECT 3
- d. DRIVE SELECT 4

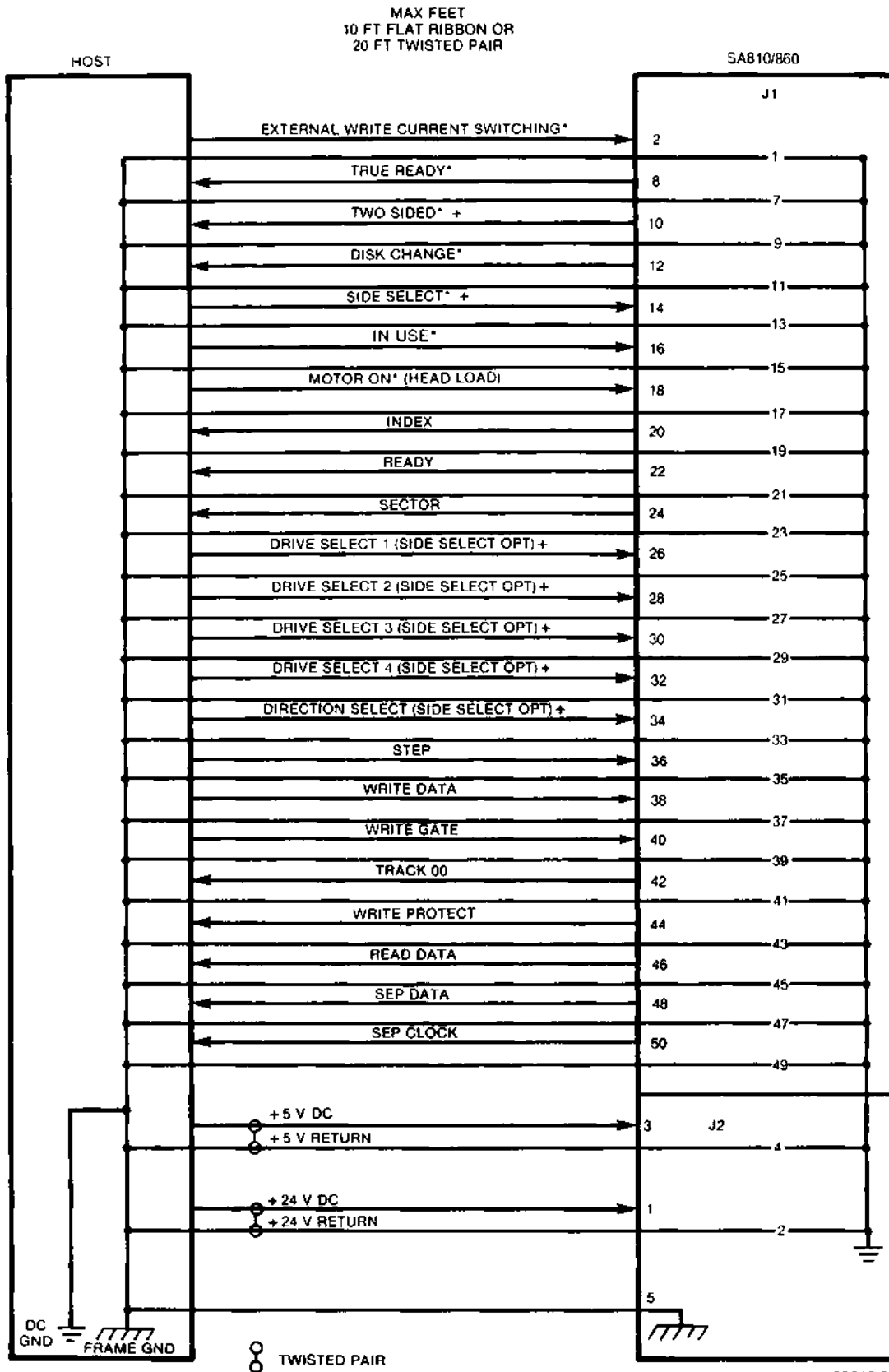
The input signals to be multiplexed are:

- a. SIDE SELECT
- b. DIRECTION SELECT
- c. STEP
- d. WRITE GATE
- e. WRITE DATA

The input signals which are not multiplexed are:

- a. MOTOR ON (May be optionally multiplexed.)
- b. IN USE
- c. EXTERNAL WRITE CURRENT SWITCH





\* JUMPER ENABLED ALTERNATE I/O LINES.  
+ SA860 ONLY

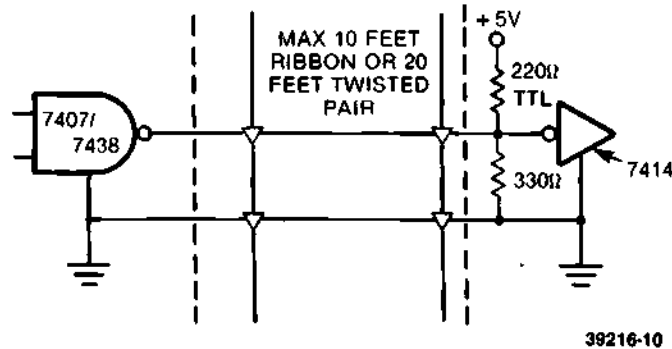
**FIGURE 2-1. SA810/860 INTERFACE CONNECTIONS**

The input circuit lines have the following electrical specifications. See figure 2-2 for the recommended circuit.

True = Logical zero =  $V_{in} \pm 0.0 \text{ V to } +0.4 \text{ V @ } I_{in} = 40 \text{ mA (max)}$

False = Logical one =  $V_{in} \pm 2.4 \text{ V to } + 5.25 \text{ V @ } I_{in} = 250 \mu\text{A (open)}$

Input Impedance = 220/330 ohms



**FIGURE 2-2. INTERFACE SIGNAL DRIVER/RECEIVER**

### 2.2.2 Input Line Termination

The SA810/860 has been provided with a removable resistor pack for terminating the eight input lines.

In order for the drive to function properly, the last drive on the interface must have these eight lines terminated. Termination of these lines can be accomplished by either of two methods:

- As shipped from the factory, the resistor pack is installed in location U9. These packs should be removed from all drives except the last one on the interface.
- External termination may be used provided the terminator is beyond the last drive. Each of the input lines should be terminated by using 220/330 ohm, 1/4 watt resistors pulled up to +5 V dc as shown in figure 2-2.

The same removable resistor pack is also provided for terminating the optional input lines.

### 2.2.3 Drive Select 1-4

DRIVE SELECT, when activated to a logical zero level, enables the multiplexed I/O lines, starts the spindle motor, locks the door, and lights the activity LED. In this mode of operation, only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4, are provided so that up to four drives may be multiplexed together in a system and have separate DRIVE SELECT lines. Traces "DS1," "DS2," "DS3," and "DS4" have been provided to select which DRIVE SELECT line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on "DS1." To select another DRIVE SELECT line, this plug should be moved to the appropriate "DS" pin.

### 2.2.4 Side Select (SA860 Only)

This interface line defines which side of a two-sided diskette is used for reading or writing. An open circuit, or logical one, selects the read/write head on the side 0 surface of the diskette. A short to ground, or logical zero, selects the read/write head on the side 1 surface of the diskette. When switching from one head to the other, a 100  $\mu\text{s}$  delay is required before any read or write operation can be initiated.

Two optional methods of side selection are available and can be implemented by the user through appropriate jumper connections.

### **2.2.5 Direction Select**

This interface line is a control signal which defines the direction of motion the read/write heads will take when the STEP line is pulsed. An open circuit, or logical one, defines the direction as "out" and if a pulse is applied to the STEP line, the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground, or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk. If buffered stepping is used, any changes to the DIRECTION SELECT line will be ignored by the drive during the time step pulse(s) are not input.

A jumper-selectable option is available which allows the DIRECTION SELECT line to be time shared for both the DIRECTION SELECT and SIDE SELECT functions. That is, during head positioning operations, the DIRECTION SELECT line controls direction of head motion. During read or write operations, the DIRECTION SELECT line determines which head is selected.

#### **NOTE**

A 16 ms delay must be introduced when changing direction (i.e., the last step-in pulse to the first step-out pulse or vice versa).

### **2.2.6 Step**

This interface line is a control signal which causes the read/write heads to move with the direction of motion as defined by the DIRECTION SELECT line.

The access motion is initiated on each logical one to logical zero transition or at the leading edge of the signal pulse. For a standard seek, step pulses may be received at a rate of 3 ms minimum time between pulses having a 1  $\mu$ s minimum pulse width. Any change in the DIRECTION SELECT line must be made at least 1  $\mu$ s minimum before the leading edge of the STEP pulse. Refer to figure 1-3 for these timings.

Buffered stepping may be done by issuing pulse(s) to the drive at a rate of 15  $\mu$ s minimum to 2.9 ms maximum time between pulses having a 1  $\mu$ s minimum pulse width. Pulses are stored in a buffer which will issue step commands to the drive stepper motor at a 3 ms pulse rate. The first step begins upon receipt of the first step pulse. Any change to the DIRECTION SELECT line during the time step pulse(s) are not input will be discounted by the drive. See figure 1-4 for these timings.

### **2.2.7 Write Gate**

The active state of this signal (logical zero) enables WRITE DATA to be written on the diskette. The inactive state (logical one) enables the read data logic (SEPARATED DATA, SEPARATED CLOCK, and READ DATA) and stepper logic. Refer to figure 1-8 for WRITE INITIATE timing information.

### **2.2.8 Write Data**

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level will cause the current through the read/write head to be reversed, thereby writing a data bit. This line is enabled by WRITE GATE being active. See figure 1-8 for timing information.

### **2.2.9 Motor On (Alternate Input)**

This customer installable option, when enabled by jumpering trace "MO" or "MMO" and activated to a logical zero level, will activate the dc spindle motor. Jumper trace "MMO" requires MOTOR ON and DRIVE SELECT to be active to start the dc spindle motor.

### **2.2.10 In Use (Alternate Input)**

This customer installable option will turn on the Activity LED and lock the door.

### **2.2.11 External Write Current Switch (Alternate Input)**

This option, enabled by jumpering trace "SE," permits write current switching via the optional WRITE CURRENT SWITCHING interface line (pin 2). When the interface signal is activated to a logical zero level, the lower value of the write current is selected. Selecting this option replaces internal write current switching at track 40.

### 2.2.12 Output Lines

There are nine standard output lines from the SA810/860 with two optional output lines and two alternate outputs available. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 mA at a logical zero level or true state with a maximum voltage of 0.4 V measured at the driver. When the line driver is in a logical one or false state, the driver is off and the collector current is a maximum of 250  $\mu$ A. See figure 2-2 for the recommended circuit.

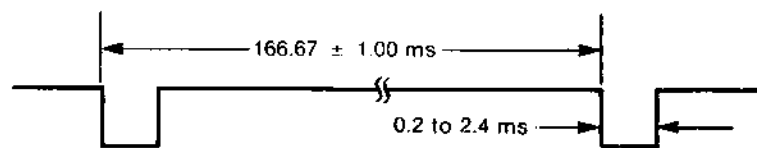
### 2.2.13 Track 00

The active state of this signal, or a logical zero, indicates when the read/write heads of the drive are positioned at track 00 (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the read/write heads of the selected drive are not at track 00.

### 2.2.14 Index

This interface signal is provided by the drive once each revolution of the diskette (166.67 ms) to indicate the beginning of the track. Normally, this signal is a logical one and makes the transition to the logical zero level for a period of 0.2 to 2.4 ms once each revolution. The timing for this signal is shown in figure 2-3.

To correctly detect INDEX at the control unit, INDEX should be false at DRIVE SELECT time; that is, the controller should see the transition from false to true after the drive has been selected. INDEX pulses will only be provided when the diskette is up to speed.

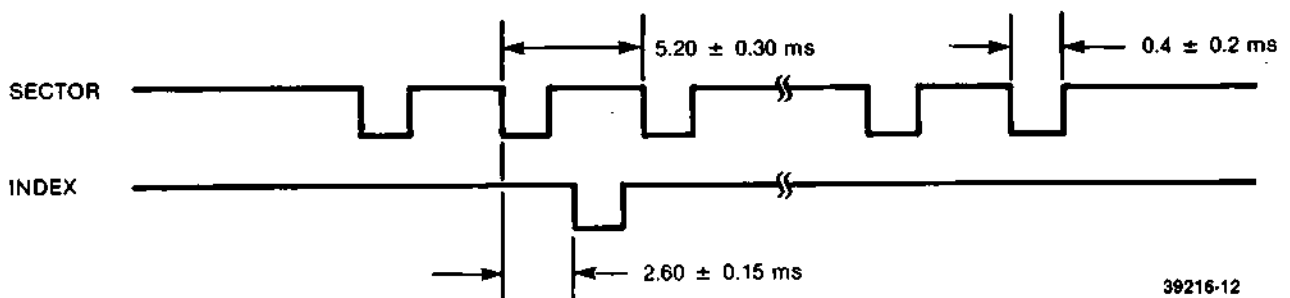


39216-11

FIGURE 2-3. INDEX TIMING

### 2.2.15 Sector (Hard Sector Only)

When a hard sectored diskette is inserted and up to speed, this interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4 ms each time a sector hole on the diskette is detected. Figure 2-4 shows the timing of this signal and its relationship to the INDEX pulse.



39216-12

FIGURE 2-4. SECTOR TIMING

### 2.2.16 Ready

This interface signal indicates that two index holes have been sensed after properly inserting and clamping a diskette. Three holes have to be sensed for two sided diskettes.

If a single sided diskette is installed, READY will be active (logical zero) when SIDE 0 is selected, but false (logical one) when SIDE 1 is selected. Conversely, if a two-sided diskette is installed, READY will be active when either side of the diskette is selected.

## NOTE

READ DATA, SEP DATA, and SEP CLOCK are only present when DRIVE SELECT and TRUE READY are active (low) and WRITE GATE is inactive (high).

### 2.2.17 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figure 1-6 for the timing and bit shift tolerance within normal media variations.

### 2.2.18 Sep Data

This interface line furnishes the data bits as separated from the raw data by use of the internal FM data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figure 1-6 for the timing.

### 2.2.19 Sep Clock

This interface line furnishes the clock bits as separated from the raw data by use of the internal FM data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figure 1-6 for the timing.

### 2.2.20 Write Protect

This interface signal is provided by the drive to give the user an indication when a write protected diskette is installed. This signal is a logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

### 2.2.21 True Ready

This output (pin 8) signals that the drive is ready to handle data. The line will come true (active low) when the diskette is up to speed, all seek functions have been completed, and the READY line is active (refer to paragraph 2.2.16). It is recommended that this signal be used in place of motor start and seek complete timers.

### 2.2.22 Disk Change (Optional Output)

This customer installable option is enabled by jumpering trace "DC." When DRIVE SELECT is activated, it will provide a true signal (logical zero) onto the interface (pin 12), if while deselected, the drive has gone from a READY to a NOT READY (door open) condition. This line is reset on the true to false transition of DRIVE SELECT if the drive has gone READY. Timing of this line is illustrated in figure 2-5.

TABLE 2-1. DC POWER REQUIREMENTS

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+ 24 V DC*	± 2.4 V DC	1.7 A MAX 1.0 A TYP	100 mV MAX ALLOWABLE
2	+ 24 V RETURN**			
3	+ 5 V DC	± 0.25 V DC	1.0 A MAX 0.7 A TYP	50 mV MAX ALLOWABLE
4	+ 5 V RETURN**			
5	FRAME GROUND			

\*If the stepper motor is energized by the controller during the spindle motor start-up time, the drive will exceed the + 24 V DC current specification of 1.7 A max. Under this condition, the current specification is 2.2 A max.

39216-13

\*\*Returns are tied together at the drive PCB.

### 2.2.23 Two Sided (Optional Output)

When the drive is selected and the diskette is spinning, this line will indicate a logical zero level for two sided media, and a logical one for single sided media.

To install this option on a standard drive, jumper trace "2S."

### 2.2.24 Alternate I/O Pins

These interface lines (pins 4 and 6) have been provided for use with customer installable options. Refer to the SA810/860 OEM Manual (P/N 39216-2) for methods of use.

## 2.3 POWER INTERFACE

The SA810 and SA860 require only dc power for operation. DC power to the drive is provided via P2/J2 located on the component side of the PCB near the stepper motor. The two dc voltages, their specifications, and their P2/J2 pin designators are outlined in table 2-1. The specifications outlined on current requirements are for one drive. For multiple drive systems, the current requirements are a multiple of the maximum current times the number of drives in the system. See figure 2-5 for the dc power requirement profile during various operations.

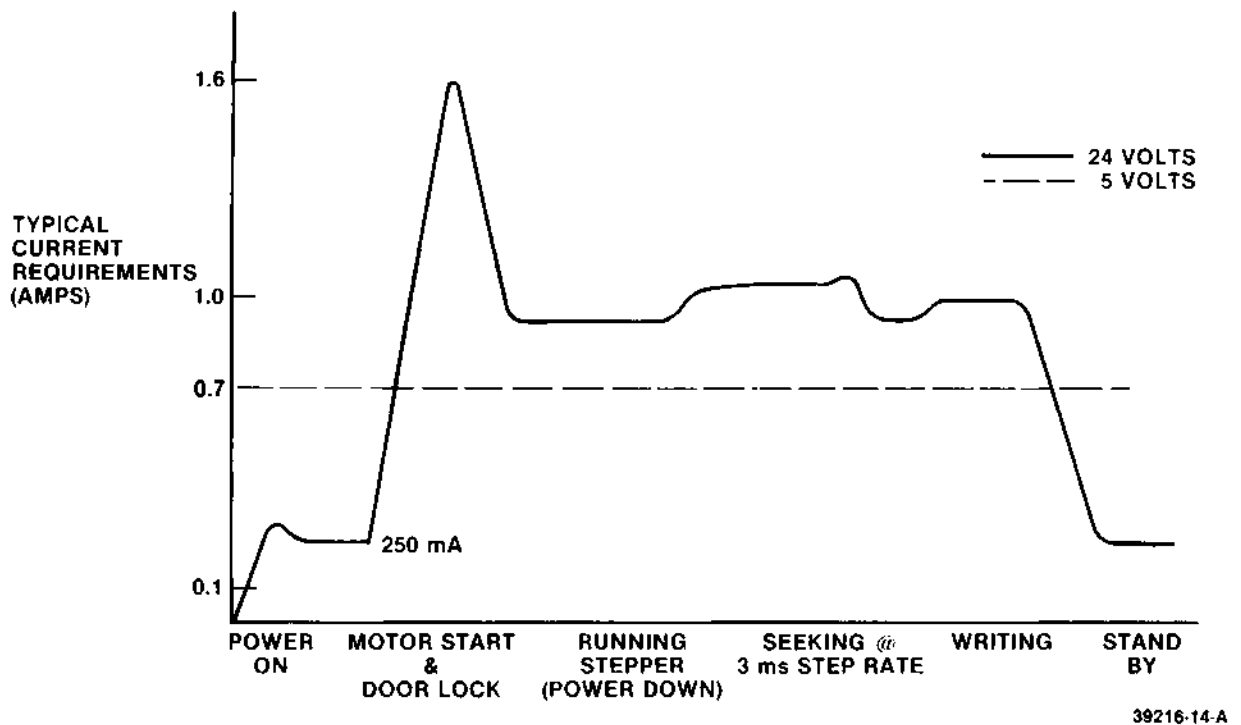


FIGURE 2-5. DC POWER PROFILE

## 2.4 FRAME GROUND

The drive must be frame grounded to the host system to ensure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good ac ground, a wire from the system ac frame ground must be connected to the drive. For this purpose, a faston tab is provided on the drive where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.

## SECTION III PHYSICAL INTERFACE

### 3.1 INTRODUCTION

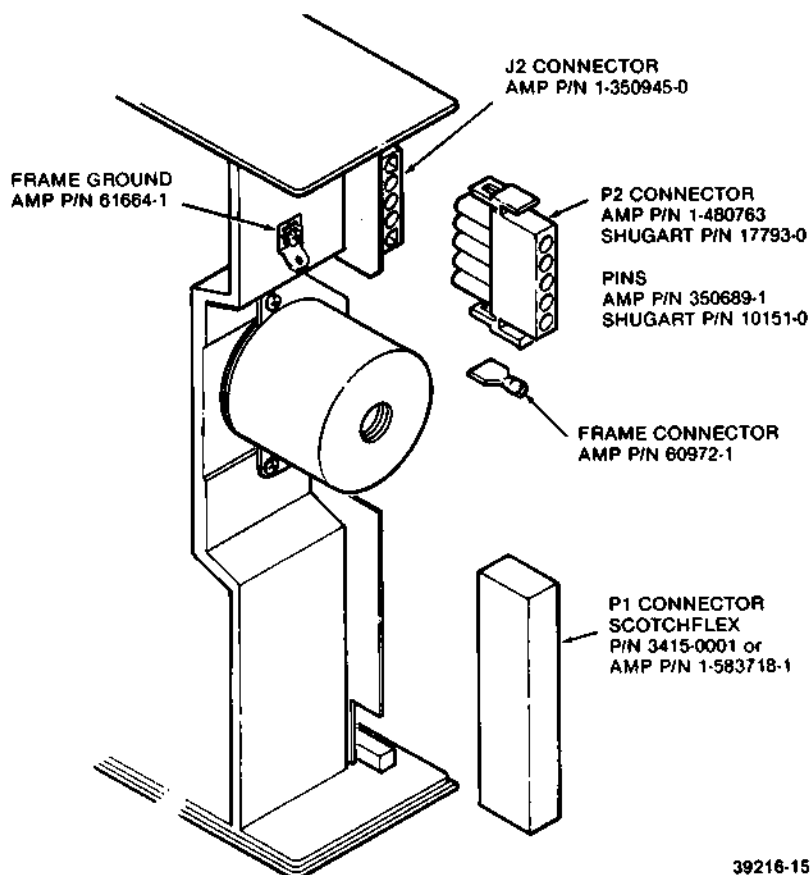
The electrical interface between the SA810/860 and the host system is via two connectors. The first connector, J1, provides the signal interface and the second connector, J2, provides the dc power.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to figure 3-1 for connector locations.

### 3.2 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge connector. The dimensions for this connector are shown in figure 3-2. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the dc connector and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are shown in table 3-1.



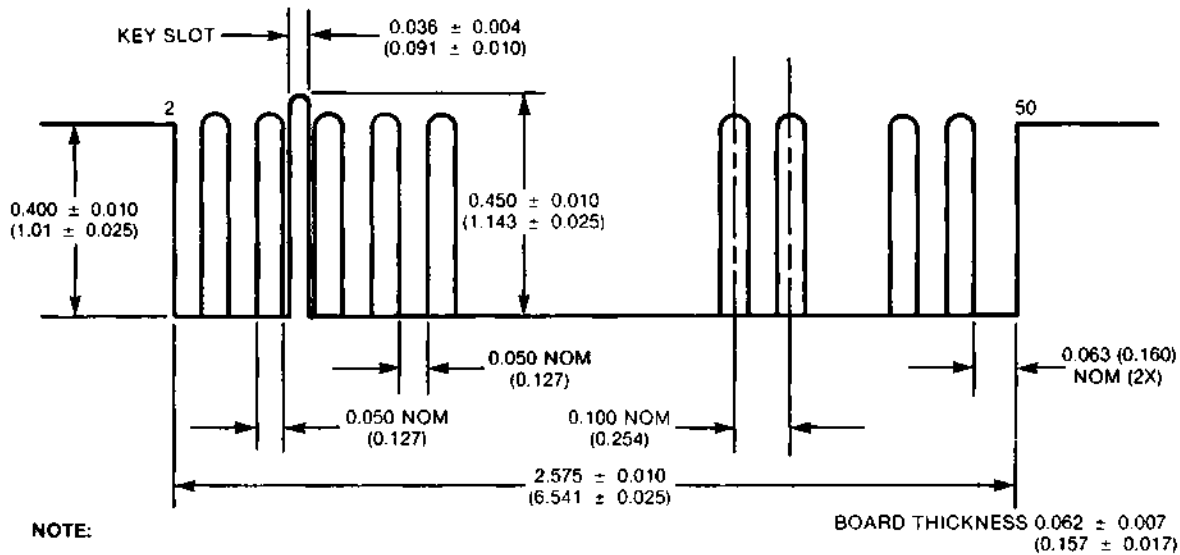
39216-15

FIGURE 3-1. INTERFACE CONNECTORS - PHYSICAL LOCATIONS

**TABLE 3-1. RECOMMENDED J1 CONNECTORS**

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
TWISTED PAIR, #18 (CRIMP OR SOLDER)	AMP	1-583718-1	583616-5 (CRIMP) 583854-3 (SOLDER)
TWISTED PAIR, #18 (SOLDER TERM.)	VIKING	3VH25/1JN-5	NA
FLAT CABLE	3M "SCOTCHFLEX"	3415-0001	NA

39216-16

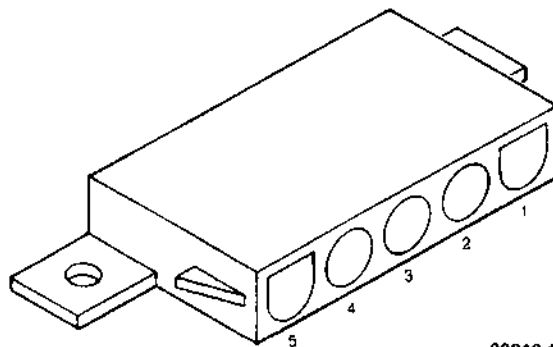


50574-19

**FIGURE 3-2. J1 CONNECTOR DIMENSIONS**

**3.3 J2/P2 CONNECTOR**

The dc power connector, J2, is mounted on the component side of the PCB and is located near the stepper motor. J2 is a 5 pin AMP Mate-N-Lok connector P/N 1-350945-0. The recommended mating connector (P2) is AMP P/N 1-480763 utilizing AMP pins P/N 350689-1. J2, pin 1, is labeled on the component side of the PCB. Figure 3-3 illustrates the J2 connector.



39216-17

**FIGURE 3-3. J2/P2 CONNECTOR**



## **SECTION IV THEORY OF OPERATIONS**

### **4.1 GENERAL OPERATIONS**

The SA810/860 floppy disk drives consist of:

- a. Read/Write and Control Electronics
- b. Drive Mechanism
- c. Precision Track Positioning Mechanism
- d. Read/Write Head(s)

The electronics are packaged on one PCB which contains:

- a. Index Detector Circuits (Sector/Index for Hard Sector Media)
- b. Head Position Actuator Driver
- c. Read/Write Amplifier and Transition Detector
- d. Write Protect
- e. Drive Select Circuits
- f. Spindle Motor Control
- g. Data/Clock Separation Circuits (FM Only)
- h. Drive Ready Detector Circuit
- i. Drive True Ready Detector Circuit
- j. Side Select Circuit (Used on SA860 Only)
- k. In Use and Door Lock Circuits
- l. Internal and External Write Current Switching
- m. Power On Reset Circuit

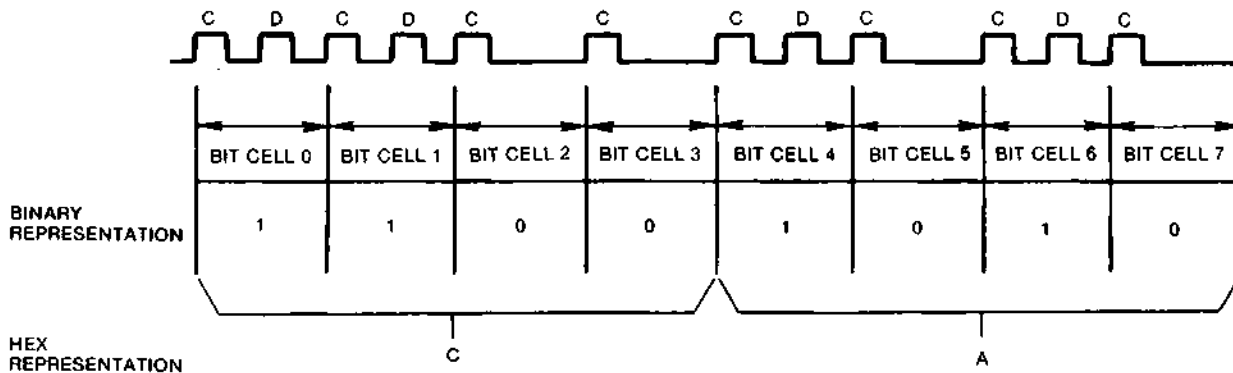
The Head Positioning Actuator moves the read/write head(s) to the desired track on the diskette. The head(s) is loaded onto the diskette when the door is closed.

The following information describes each of the above functions in detail.

### **4.2 READ/WRITE OPERATIONS**

- a. The SA810/860 uses double frequency non return to zero (NRZI) recording method.
- b. The read/write head, in general, is a ring with a gap and a coil wound at some point on the ring.
- c. During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil.
- d. During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface.

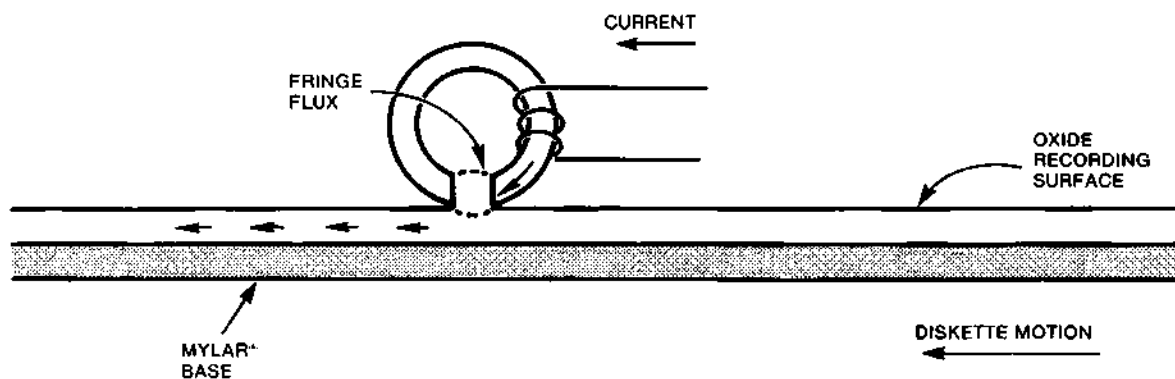
SA810/860 drives use the double-frequency (2F) longitudinal NRZI method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell, thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, is provided by the using system. See figure 4-1.



**FIGURE 4-1. BYTE**

39211-17

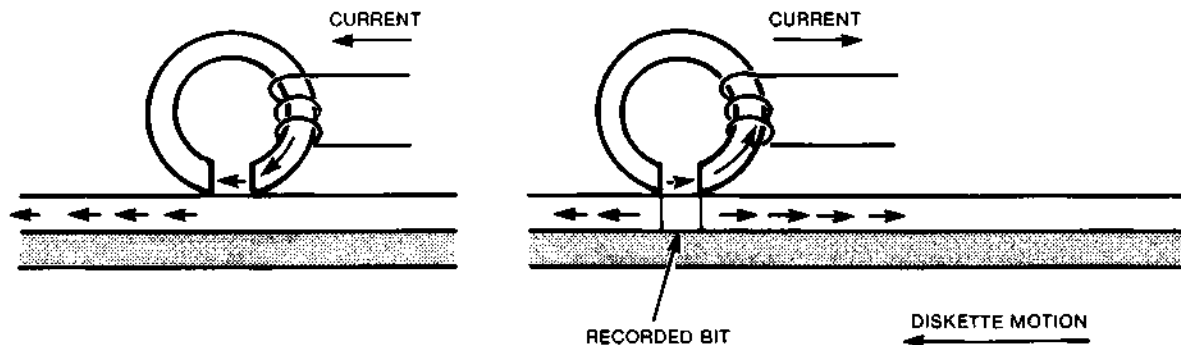
The read/write head is a ring with a gap and a coil wound some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a longitudinal direction. See figure 4-2.



**FIGURE 4-2. BASIC READ/WRITE HEAD**

39211-18

The drive writes two frequencies: 1F, 125 k Hz and 2F, 250 k Hz. During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized one direction while the portion under the gap is magnetized in the opposite direction. This flux reversal represents a bit. See figure 4-3.

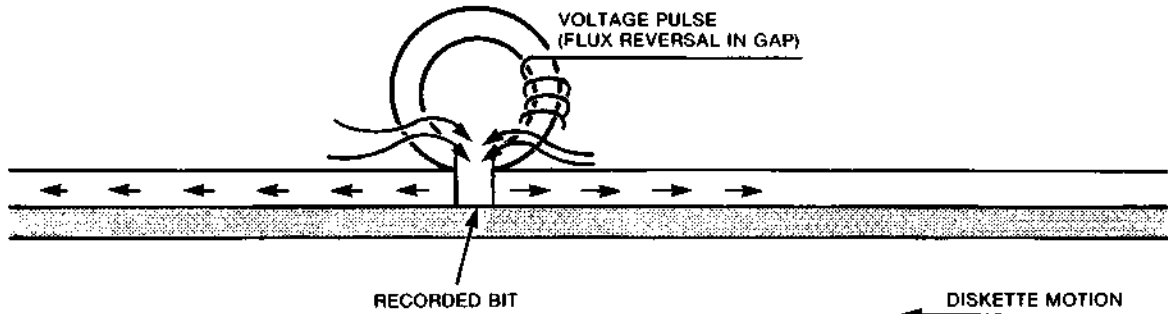


**FIGURE 4-3. RECORDED BIT**

39211-19

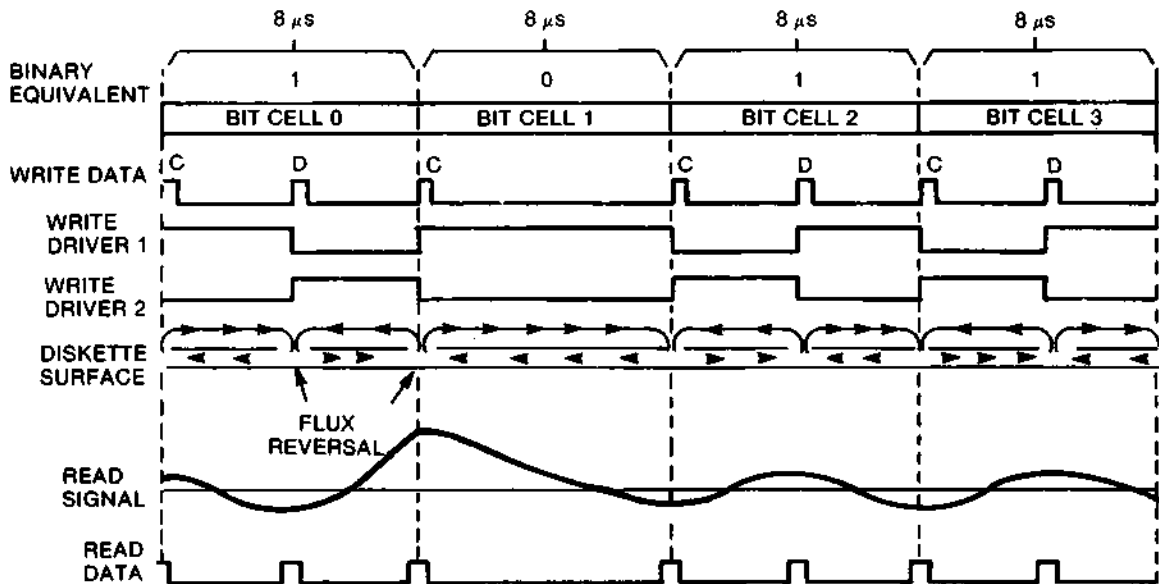
During a read operation, a bit is read when the flux direction in the ring is reversed as a result of flux reversal on the diskette surface. The gap first passes over an area that is magnetized in one direction and a constant flux flows through the ring and coil. The coil registers no output voltage at this point. When a recorded bit passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See figure 4-4.

These flux reversals produce an FM waveform which transmits data to and from the diskette. See figure 4-5.



39211-20

FIGURE 4-4. READING A BIT



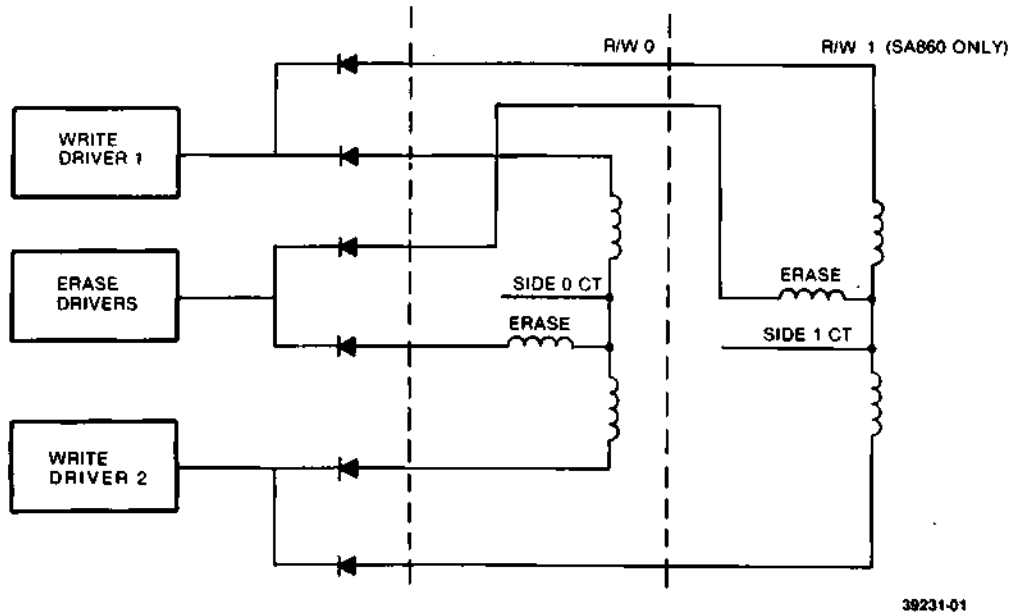
39231-30

FIGURE 4-5. 1F AND 2F RECORDING FLUX AND PULSE RELATIONSHIP

### 4.3 READ/WRITE HEAD

- a. The ceramic read/write heads each contain three coils.
- b. When writing, the head erases the outer edges of the track to ensure there are erased areas between adjacent tracks.

The read/write head contains three coils. Two read/write coils are wound on a single core, center tapped, and one erase coil is wound on a yoke that spans the track being written. The read/write and erase coils are connected as shown in figure 4-6.



**FIGURE 4-6. READ/WRITE HEADS**

During a write operation, the erase coil is energized. This causes the outer edges of the track to be trim erased to prevent the track being recorded from exceeding the 0.012 inch (0.508 mm) track width. Trim erasing allows for minor deviations in read/write head current so as one track is recorded, it will not splash over to adjacent tracks.

Each bit written will be directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. A change in the flux pattern for each bit results. The current through either of the read/write coils will cause the old data to be erased as new data is recorded.

During a read operation, the direction of flux changes on the diskette surface as it passes under the gap and current is induced into one of the windings of the read/write head. This results in a voltage output pulse. When the next data bit passes under the gap, another flux change takes place in the recording surface. Current is induced in the other coil, producing another voltage output pulse of the opposite polarity.

#### 4.4 WRITE CIRCUIT OPERATION

- a. The write data trigger flips with each pulse on the WRITE DATA line.
- b. The write data trigger alternately drives one or the other of the write drivers.
- c. Lower write current value is selected by grounding the EXTERNAL WRITE CURRENT SWITCH or -TRACK 40.
- d. WRITE GATE allows write current to flow to the write driver circuits if the diskette is not write protected.
- e. Write current sensed allows erase coil current.
- f. Heads are selected by raising the appropriate center tap to a logical high state.

WRITE DATA pulses (clock and data bits) are supplied by the using system. The write trigger flips with each pulse. The outputs are fed to alternate write drivers (see figure 4-7).

WRITE GATE and NOT WRITE PROTECT are ANDed together and will cause write current to flow to the write driver circuits. This causes the center tap switch to close and erase current to flow.

The output of one of the write drivers allows write current to flow through one half of the read/write coil. When the write trigger flips, the alternate write driver provides write current to the other half of the read/write coil.

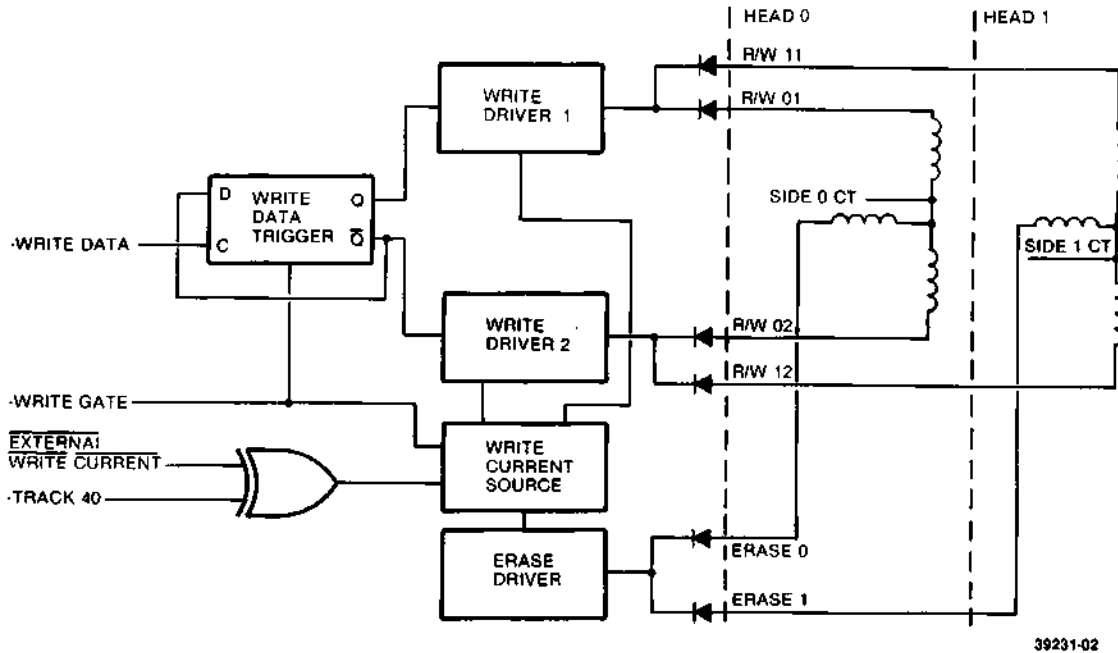


FIGURE 4-7. WRITE CIRCUIT FUNCTIONAL DIAGRAM

#### 4.5 READ CIRCUIT OPERATION

- Duration of all read operations is under control of the using system.
- As long as the drive is selected, TRUE READY is active, and WRITE GATE is not active, the read signal is amplified and shaped, and the square wave signals are sent to the interface as read data.
- The FM data separator divides the read data into clock pulses and data pulses.

When the using system requires data from the diskette drive, the using system must select the head (SA860 only) and disable WRITE GATE. The read signal is then fed to the amplifier section of the read circuit. After amplification, the read signal is fed to a filter where the out-of-band noise is removed. The read signal is then fed to the differentiator amplifier.

Since a clock pulse occurs at least once every  $4 \mu\text{s}$  and data bits are present once every  $2 \mu\text{s}$  (FM encoding only), the frequency of the READ DATA varies. The read signal amplitude decreases as the frequency increases. Note the signals in figure 4-8. The differential amplifier will amplify, differentiate, limit, and digitize the read signals (sine waves).

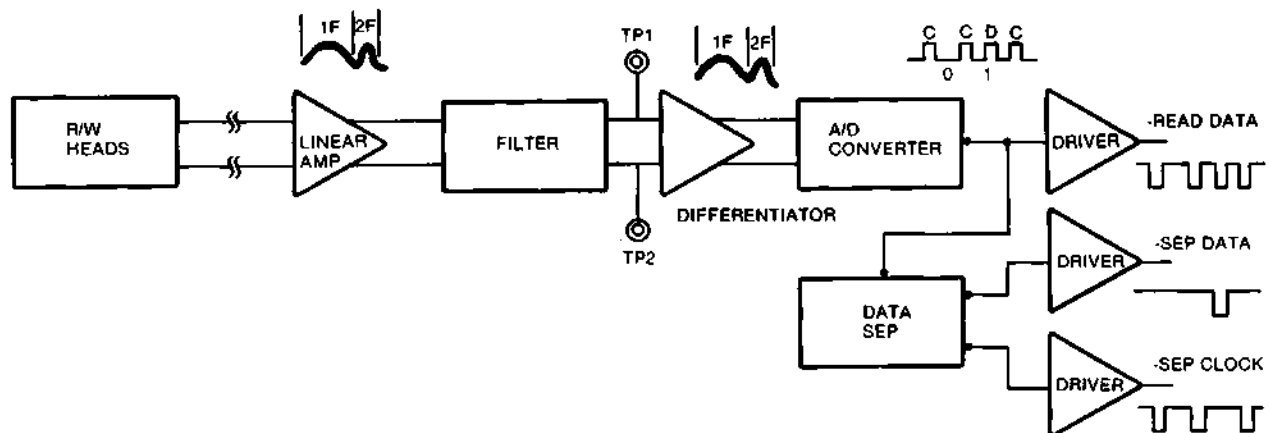


FIGURE 4-8. READ CIRCUIT FUNCTIONAL DIAGRAM

The FM data separator is a single time constant separator, that is, the clock and data pulses must fall within pre-specified time frames or windows.

#### 4.6 DRIVE MOTOR CONTROL

- a. Start/Stop
- b. Phase Control
- c. Speed Control

The motor used in the SA810/860 is a dc brushless direct drive motor. The motor may be turned on and off via DRIVE SELECT or the optional MOTOR ON line located on pin 18 of the interface. When activating the motor, a 165 ms minimum delay must be introduced to allow proper motor speed before reading or writing, or the TRUE READY line must be monitored. The typical time for a valid TRUE READY signal is 120 ms.

Figure 4-9 is a block diagram of the motor phase and speed control circuitry. The position of the 3 phase motor is detected by three Hall effect sensors which feed this information into the Motor Phase Control. The Motor Phase Control then decodes this information and activates the proper Motor Phase Drivers. The amount of current supplied to the motor windings is determined by comparing the output of the integral magnetic tachometer of the motor to a 360 Hz crystal reference. The difference is fed to the Motor Speed Control which adjusts the current flow to the Motor Phase Drivers via the Motor Power Driver, thus locking the phase of the motor to a crystal reference.

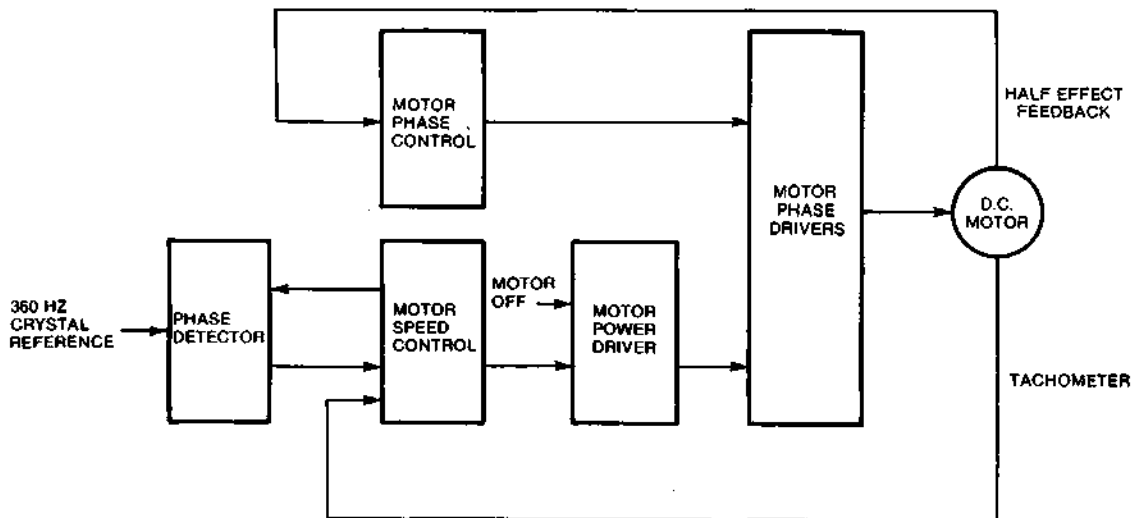


FIGURE 4-9. DRIVE MOTOR CONTROL

39231-03

#### 4.7 TRACK ACCESSING

- a. Carriage Actuator Motor
- b. Actuator Control Logic
- c. Reverse Seek
- d. Forward Seek
- e. Track 00 Flag

##### 4.7.1 Stepping

Seeking the read/write heads from one track to another is accomplished by selecting the desired direction utilizing the DIRECTION SELECT interface line, loading the read/write heads, and pulsing the STEP line. Multiple track accessing is accomplished by repeated pulsing of the STEP line until the desired track has been reached. Each pulse on the STEP line will cause the read/write heads to move one track either in or out depending on the DIRECTION SELECT line.

##### 4.7.2 Carriage Actuator

The Carriage Actuator Motor used on the SA810/860 is a four phase, 15° per step, variable reluctance stepper motor.

There are eight stator windings and a rotor with six teeth. The eight stator windings are wired together in groups of two, 180° apart. Each pair of stator windings is wired to one phase of the stepper control logic. The rotor has six teeth spaced 60° apart. The two windings per phase are those which, when energized, will magnetize the poles causing the rotor to move one-fourth of a gear tooth pitch or one step.

### 4.7.3 Actuator Control Logic

Figure 4-10 illustrates the logic of the following operations.

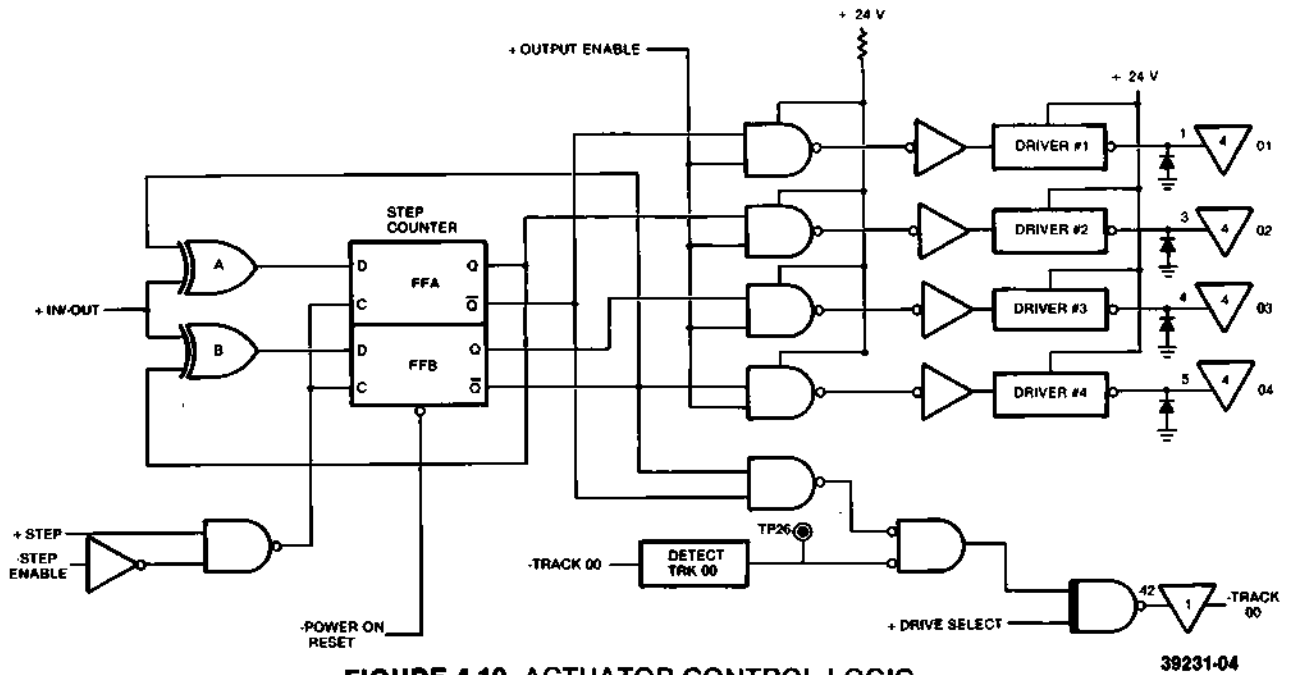


FIGURE 4-10. ACTUATOR CONTROL LOGIC

39231-04

The step counter (FF A and FF B) is a modified Gray Code counter that counts 0, 1, 3, and 2. At power on, the step counter is reset causing the Q outputs to be active. When dc power is applied and the drive is selected, the Q outputs activate the 2 and 3 drivers. With these drivers active, the position zero windings are excited causing the rotor to align as shown in figure 4-11.

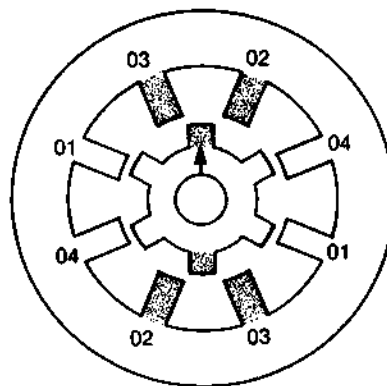


FIGURE 4-11. TRACK 00

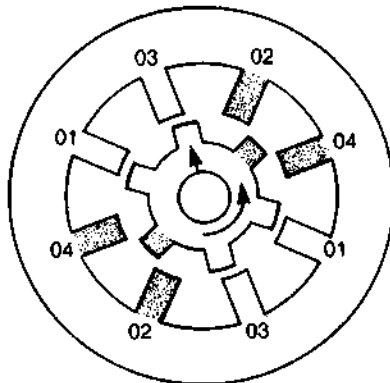
39231-05

### Forward Seek

- a. Seek forward five tracks.
- b. Assuming:
  - Present position of the read/write heads to be Track 00.
  - +IN/-OUT at a minus level.
  - -STEP ENABLE active.
  - Five step pulses to be received (from the host system).
  - Step Counter (drivers 2 and 3 active).

Minus DIRECTION SELECT is inverted and becomes +IN. Since the step counter is reset (low), a high is at one input of Exclusive OR A and a low at Exclusive OR B. +IN is high and inverts both signals present at Exclusive OR's A and B, causing the input to FF B to be high.

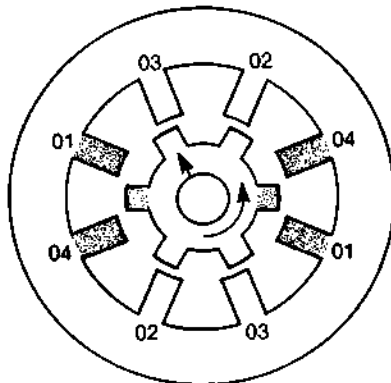
When the first step pulse is sent to the control logic, it is ANDed with +STEP ENABLE and clocks FF A off and FF B on. This enables drivers 2 and 4 causing the actuator motor to move 15° in a counter-clockwise direction. In turn, the carriage assembly moves one track towards the center of the diskette. See figure 4-12 (Track 01, Count 1).



39231-06

**FIGURE 4-12. TRACK 01**

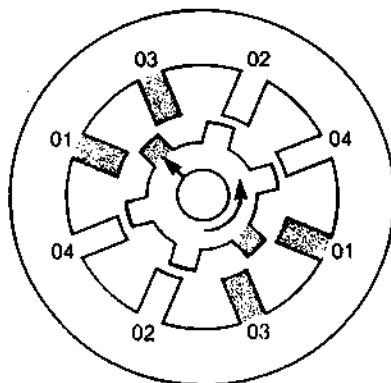
With FF A off and FF B on, a low is presented to Exclusive OR A and B allowing +IN to pass to both FF's. Upon receipt of the next step pulse, both FF's are clocked on, enabling drivers 1 and 4. See figure 4-13 (Track 02, Count 3).



39231-07

**FIGURE 4-13. TRACK 02**

With both FF's on, a low is at Exclusive OR A and a high at Exclusive OR B which presents +IN to FF A. The next step pulse clocks FF A on and FF B off enabling drivers 1 and 3. See figure 4-14 (Track 03, Count 2).



39231-08

**FIGURE 4-14. TRACK 03**

This process continues until the host system stops sending step pulses at track 05. At that time, FF A is off and FF B on enabling drivers 2 and 4. See figure 4-12 (Count 1).



## Reverse Seek

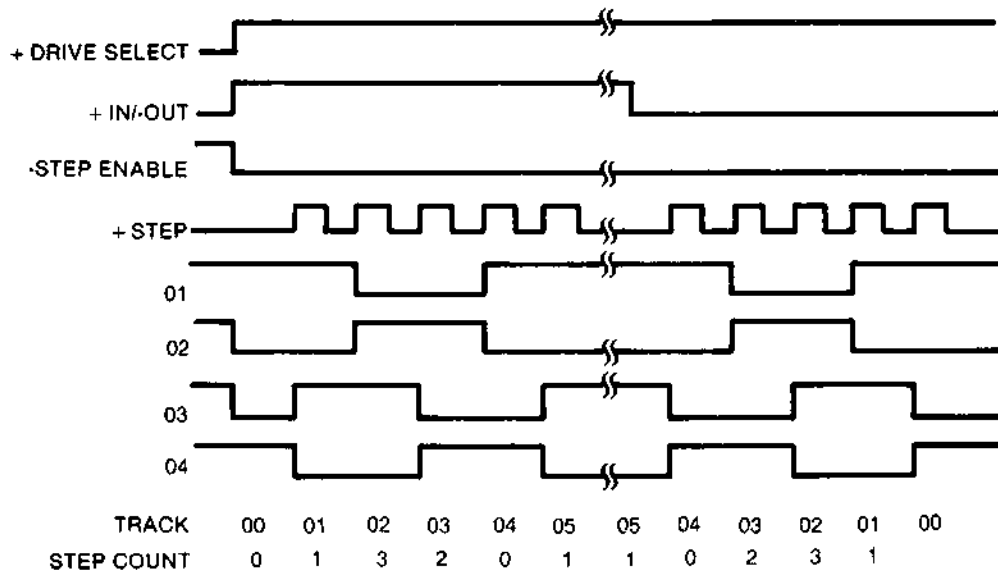
- a. Seek in a reverse direction five tracks.
- b. Assuming:
  - Present position of read/write heads to be track 05 and DIRECTION SELECT at a positive level (from the host system).
  - WRITE GATE inactive.
  - Five step pulses to be received.
  - FF A is off and FF B is on; drivers 2 and 4 active.

Plus IN is inverted and becomes OUT. With FF A off and FF B on, lows are presented to Exclusive OR's A and B. With the first step pulse, the FF's are clocked off enabling 2 and 3 drivers. This causes the actuator motor to move 15° in a clockwise direction, moving the carriage one track towards the outside of the diskette. See figure 4-11 (Track 04, Count 0).

With both FF's off, a high is presented to Exclusive OR A and a low to Exclusive OR B. The next step pulse clocks FF A on and FF B off enabling drivers 1 and 3. See figure 4-14 (Track 03, Count 2).

This process continues until the fifth step pulse. With lows at the Exclusive OR's, and FF's clocked off, drivers 2 and 3 are enabled. See figure 4-11 (Track 00, Count 0).

Figure 4-15 shows stepper timing for forward and reverse seeks.



39231-09

FIGURE 4-15. STEPPER TIMING

### 4.7.4 Track Zero Indicator

Track 00 Pin 42 is provided to the host system to indicate that the read/write heads are at track 00. The track 00 flag on the carriage assembly is adjusted so that the flag covers the photo transistor at track 01. When FF A and B are clocked off, the actuator moves to track 00, the Q outputs and track 00 defect are ANDed together and then ANDed with DRIVE SELECT to send the track 00 indication to the host system (see figure 4-10).

## SECTION V MAINTENANCE

### 5.1 MAINTENANCE EQUIPMENT

#### 5.1.1 Alignment Diskette

Two alignment diskettes are available for verifying and adjusting the SA810/860. The SA810 requires written information on one surface only and utilizes the SA120 alignment diskette. The SA860 has two read/write heads and requires written information on both surfaces. The SA122 alignment diskette is used to perform checks on the SA860. The following adjustments to the SA810/860 can be made using the SA120/122:

- a. Read/Write head radial alignment using track 38.
- b. Index photo-detector adjustment using tracks 01 and 76.

#### CAUTION

Caution should be exercised in using the SA120/122 Alignment Diskette. Tracks 00, 01, 36, 37, 38, 39, 40, 75, and 76 should not be written on. Doing so destroys pre-recorded tracks.

#### 5.1.2 SA809 Exerciser

The SA809 Exerciser is built on an 8-inch by 8-inch PCB. This Exerciser PCB can be used in a stand alone mode, built into a test station, or used in a tester for field service.

The Exerciser, when used with the SA120/122 Alignment Diskette, is designed to enable the user to perform all adjustments and checks required on the SA810/860 drives.

The Exerciser has no intelligent data handling capabilities but can write both 1F and 2F frequencies and can enable read in the drive to allow checking of read back signals.

#### 5.1.3 Special Tools

The special tools available for performing maintenance on the SA810/860 are listed in table 5-1.

**TABLE 5-1. MAINTENANCE EQUIPMENT**

DESCRIPTION	PART NUMBER
SA120 ALIGNMENT DISKETTE (SA810 ONLY)	50782
SA122 ALIGNMENT DISKETTE (SA860 ONLY)	51189
EXERCISER (SA810/860)	50619
SPINDLE MOTOR CENTERING TOOL	54650

39231-10

## 5.2 DIAGNOSTIC TECHNIQUES

Incorrect operating procedures, faulty programming, damaged diskettes, and soft errors created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment.

Unless visual inspection of the drive discloses an obvious misalignment or broken part, try to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

### 5.2.1 Soft Error Detection and Correction

Soft errors are usually caused by:

- a. Airborne contaminants that pass between the read/write heads and the disk. These contaminants can usually be removed by the cartridge self-cleaning wiper.
- b. Random electrical noise that usually lasts for a few microseconds.
- c. Small defects in written data and/or track not detected during a write operation may produce soft errors during a read.
- d. Improper grounding of power supply, drive and/or host system. Refer to the SA810/860 OEM manual (P/N 39216) for proper grounding requirements.
- e. Improper motor speed.

The following procedures are recommended to recover from soft errors:

- a. Reread track 10 times or until data is recovered.
- b. If data is not recovered after step (a), access head to adjacent track in same direction previously moved then return to desired track.
- c. Repeat step (a).
- d. If data is not recovered, error is not recoverable.

### 5.2.2 Write Errors

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a write check. To correct the error, another write and write check operation must be performed. If the write operation is not successful after 10 attempts, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error persists, replace the diskette and repeat the above procedure. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

### 5.2.3 Read Errors

Most read errors that occur will be soft errors. In these cases, performing the error recovery procedure in paragraph 5.2.1 will recover the data.

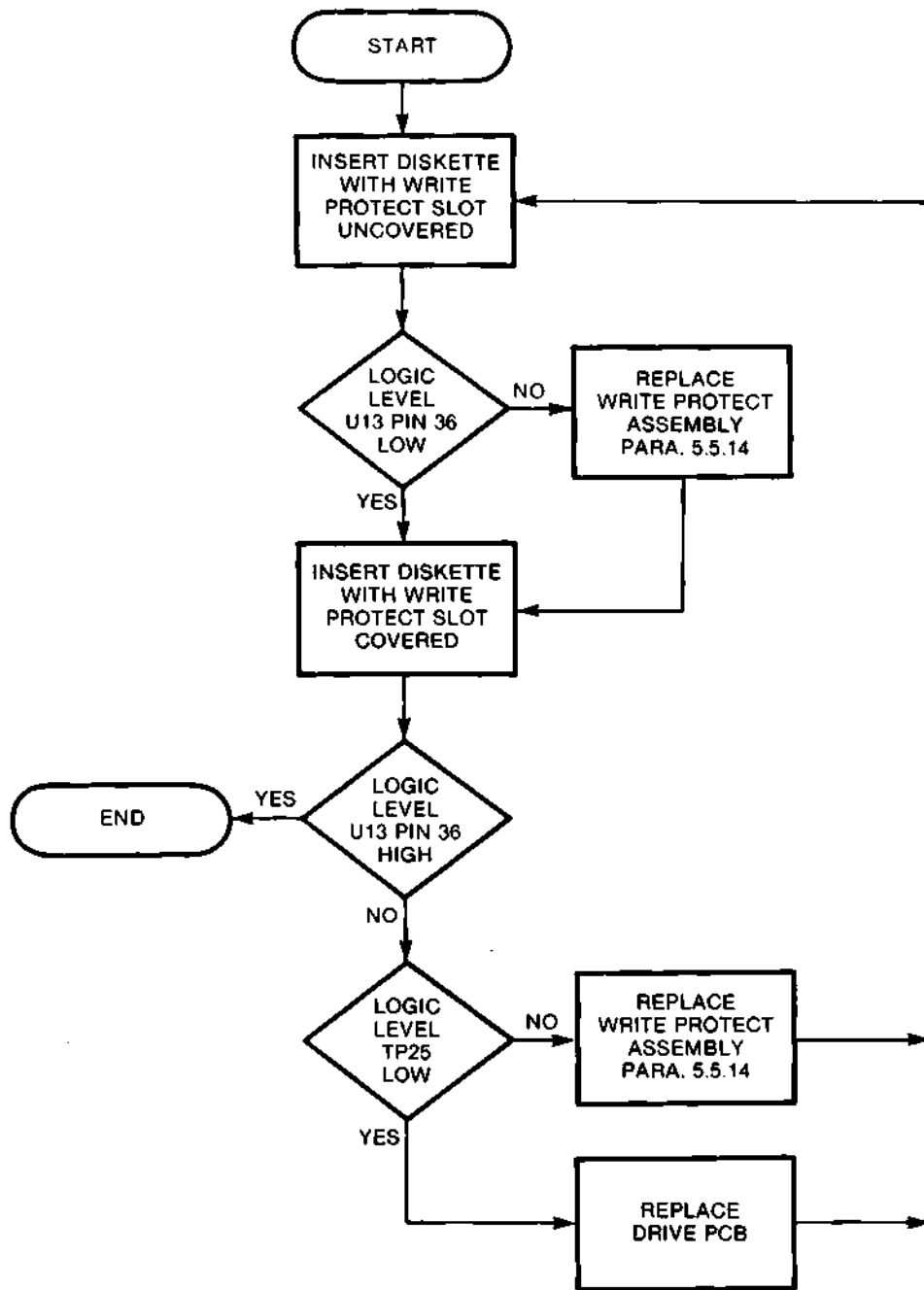
### 5.2.4 Seek Errors

Seek errors may be caused by stepper malfunctions or carriage binds.

To recover from a seek error, recalibrate to track 00 and perform another seek to the original track or perform a read ID to find which track the head is located on and compensate accordingly.

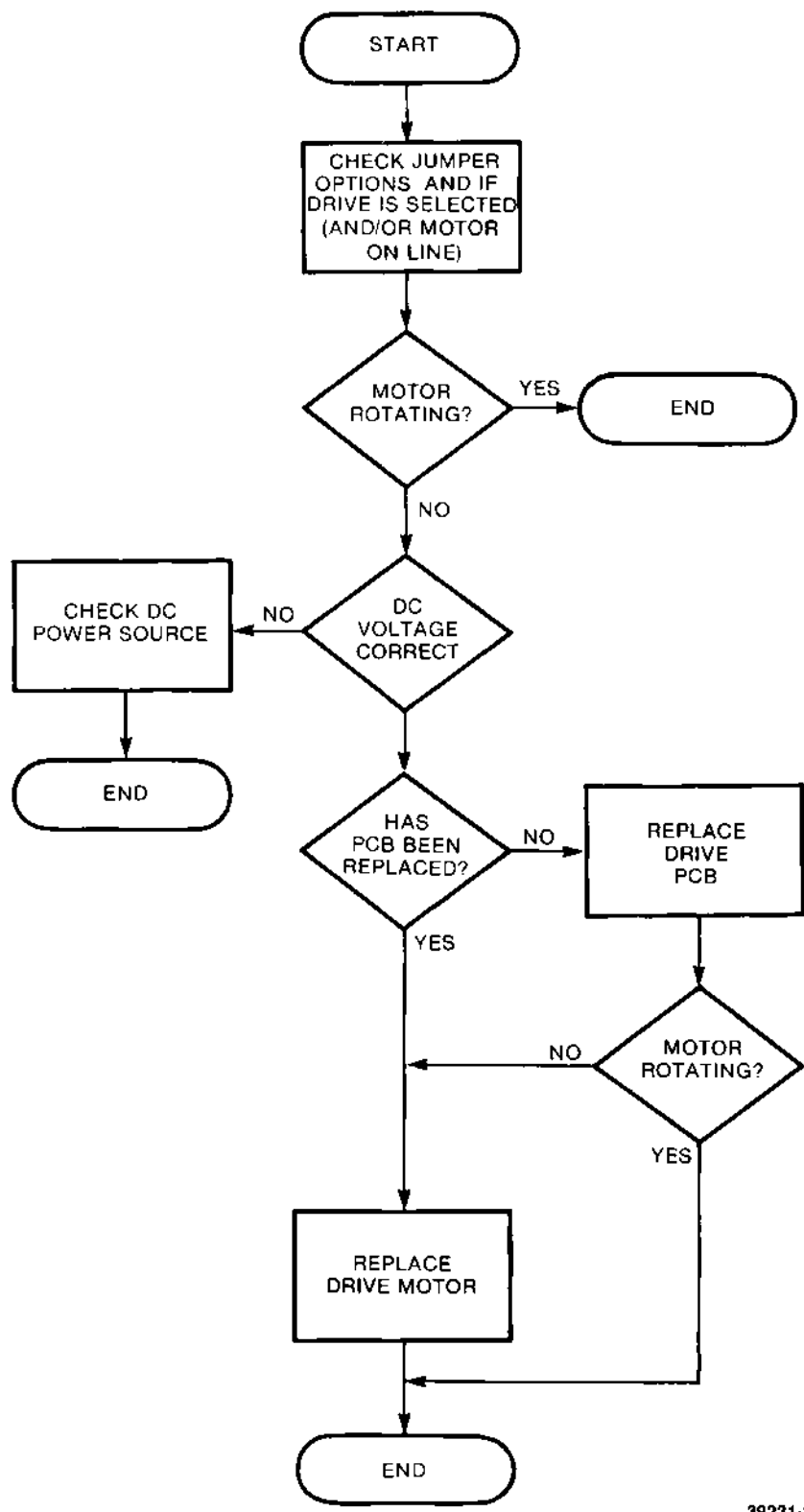
## 5.3 TROUBLE-SHOOTING

Figures 5-1 and 5-2 outline trouble-shooting procedures for the SA810/860.



39231-11

FIGURE 5-1. WRITE PROTECT INOPERATIVE



39231-12

FIGURE 5-2. DISKETTE NOT ROTATING

## 5.4 ADJUSTMENTS

### 5.4.1 Side 1 Downstop Adjustment (SA860 Only)

- a. Install good media. Ensure door knob is in fully closed position.
- b. Clearance of  $0.010 \pm 0.002$  inch ( $0.254 \pm 0.051$  mm) should be obtained between side 1 arm and flexure. To adjust clearance, turn allen screw located on top of side 1 arm. Clockwise turn decreases clearance. Counter-clockwise turn increases clearance. See figure 5-3.
- c. Eject and reinsert media several times and reverify required clearance.
- d. Verify head alignment (paragraph 5.4.2).

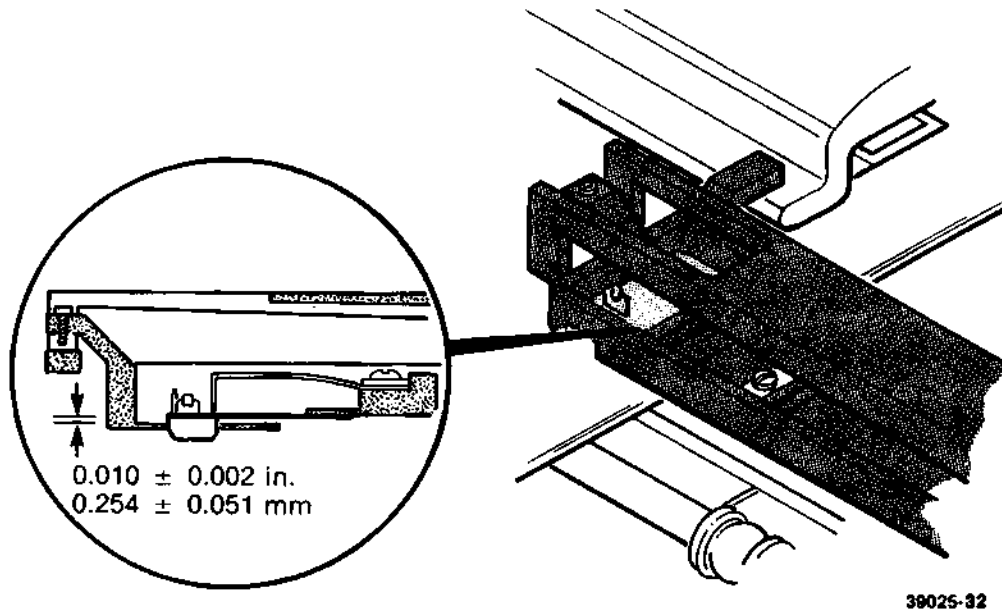


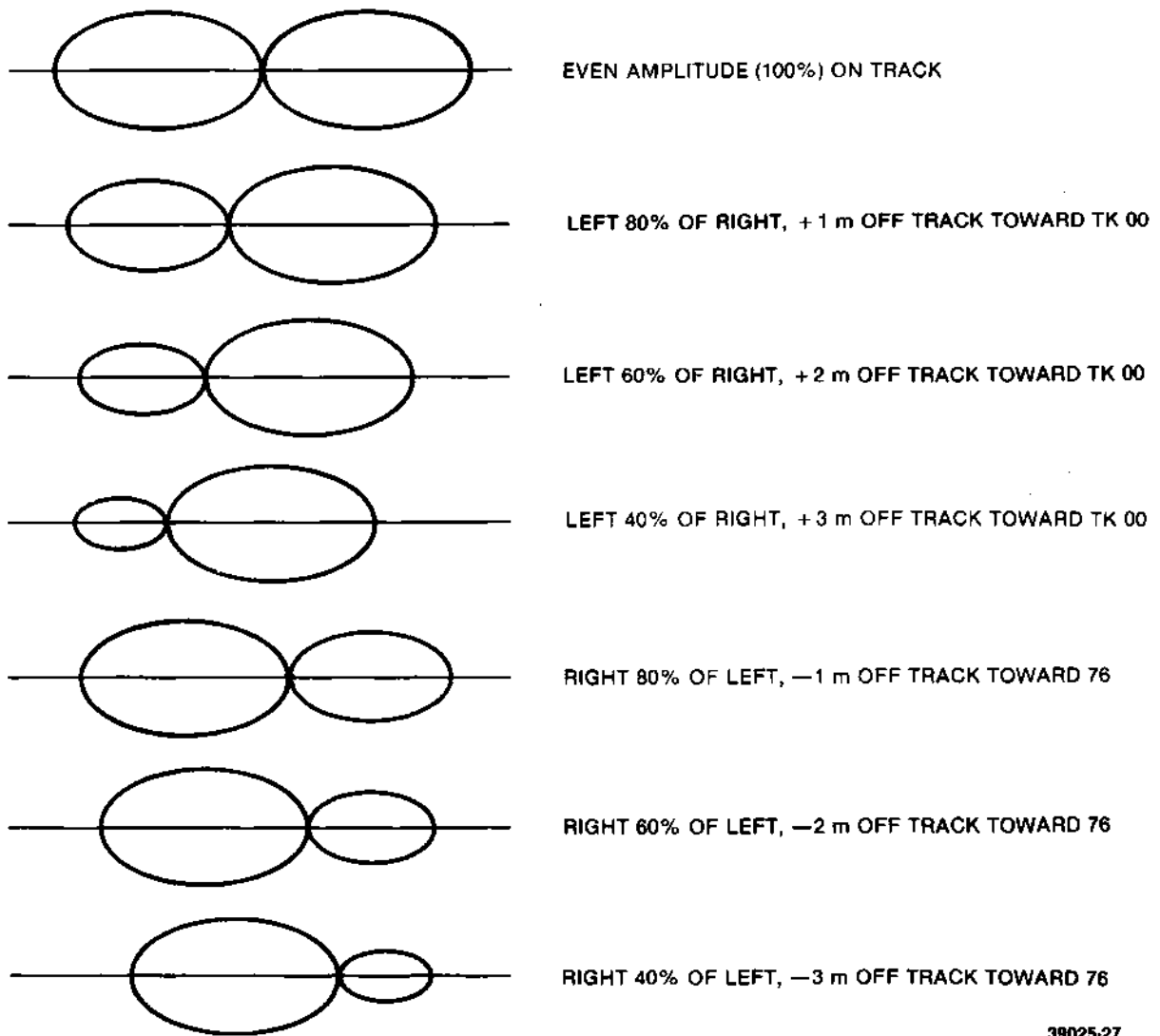
FIGURE 5-3. SIDE 1 DOWNSTOP ADJUSTMENT

### 5.4.2 Head Radial Alignment

#### NOTE

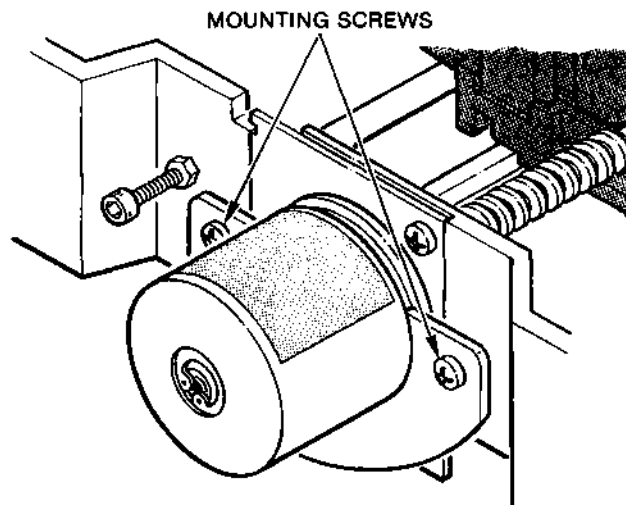
SA860 read/write head assembly is aligned at factory and adjustment of head-to-head alignment is not field adjustable. However, downstop adjustment may effect head-to-head alignment. If tolerances below cannot be maintained, downstop adjustment should be checked (paragraph 5.4.1).

- a. Insert alignment diskette (SA810 = SA120, SA860 = SA122). Alignment diskette should be at room conditions for at least 24 hours prior to alignment checks.
- b. Select drive and step head(s) to track 38.
- c. Sync oscilloscope external negative on TP12 (—INDEX). This will display over one revolution.
- d. Connect one probe to TP1 and other to TP2. Ground probes to PCB. Set inputs to ac, ADD, and invert one channel. Set vertical deflection to 100 mV/division.
- e. Amplitude of two lobes must be within 70% of each other. If lobes do not fall within specification, continue procedure (see figure 5-4).
- f. Loosen two mounting screws which hold motor plate to base casting. See figure 5-5.



**FIGURE 5-4. HEAD RADIAL ALIGNMENT**

- g. Rotate stepper motor.
- h. When lobes are of equal amplitude, tighten motor plate mounting screws (see figure 5-5).



**FIGURE 5-5. MOTOR PLATE MOUNTING SCREWS**

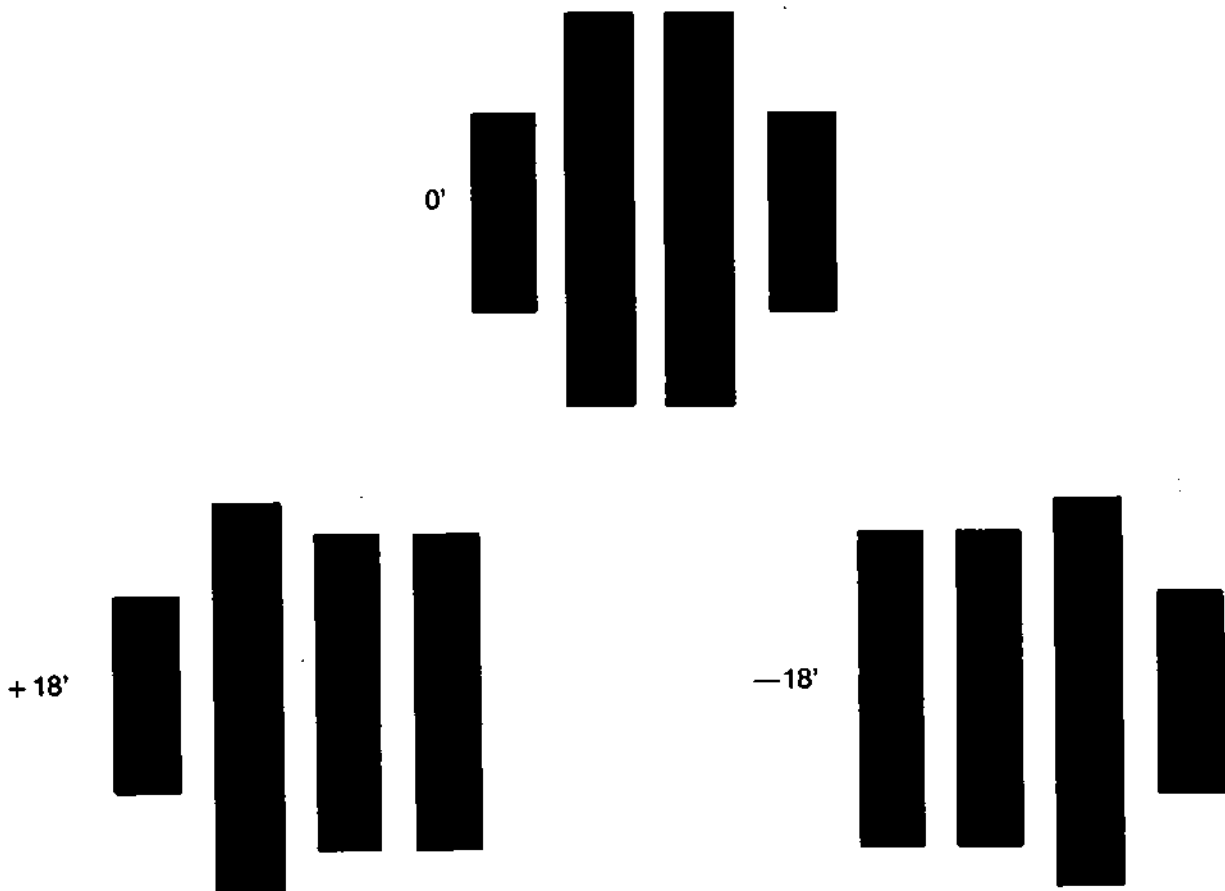
39231-13

- i. Check adjustment by stepping off track and returning. Check in both directions and readjust as required.
- j. Whenever head radial alignment has been adjusted, track 00 detector and limiter adjustment must be checked (paragraphs 5.4.5 and 5.4.6).

### 5.4.3 Read/Write Head(s) Azimuth Check

The azimuth is not field adjustable. If, after performing this check, the waveform on the oscilloscope is not within  $\pm 18'$ , replace the Head Carriage Assembly (paragraph 5.5.8).

- a. Install Alignment Diskette (SA810 = SA120, SA860 = SA122).
- b. Select drive and step to track 76.
- c. Sync the scope external negative on TP12 (-INDEX). Set time base to 0.5 Msec per division.
- d. Connect one probe to TP1 and other to TP2. Invert one channel and ground probes to TPG5 and TPG6. Set inputs to ac, ADD, and 50 MV per division.
- e. Compare waveform to figure 5-6. If not within range shown, replace Head Carriage Assembly (paragraph 5.5.8).



39231-14

FIGURE 5-6. AZIMUTH BURST PATTERNS



#### 5.4.4 Head Amplitude Check

These checks are only valid when writing and reading back as described below. If the amplitude is below the minimum specified, ensure that the diskette is not worn or otherwise shows evidence of damage on either side before re-writing and re-checking. Ensure that the head load downstop is properly adjusted (SA860 only).

- a. Install good media.
- b. Select drive and step to TK 76.
- c. Sync oscilloscope on TP12 (—INDEX) for single-sided diskettes, and TP13 for double-sided diskettes.
- d. Connect one probe to TP2 and one to TP1 on drive PCB.
- e. Ground probes to PCB and invert one input. Set volts per divisions to 50 mV and time base to 20 Msec per division.
- f. Write entire track with 2F signals (all 1's).
- g. Average minimum read back amplitude peak-to-peak should be 130 mV for side 1 (SA860 only).
- h. Repeat procedure for side 1 (SA860 only).

If the output is below minimum, and different media is tried but the output is still low, it will be necessary to install a new head assembly (paragraph 5.5.8).

#### 5.4.5 Track 00 Detector Assembly

- a. Check head radial alignment and adjust if necessary (refer to paragraph 5.4.2) before making following adjustment.
- b. Insert diskette.
- c. Connect oscilloscope to TP26. Set vertical deflection to 1 V/division and sweep to continuous.
- d. Step carriage to track 02. TP26 should go high. Adjust detector assembly towards actuator assembly if not low.
- e. Check adjustment by stepping heads between tracks 01 and 02, ensuring TP26 is high at track 02 and low at track 01.

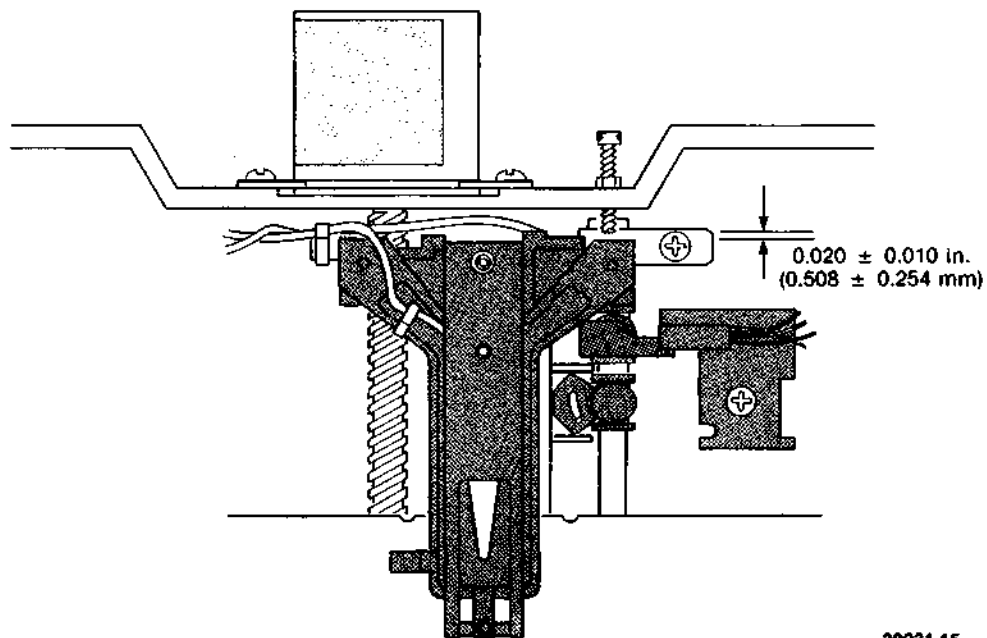
#### 5.4.6 Track 00 Carriage Limiter

- a. Step carriage to track 00. Verify carriage is at track 00 by checking J1 pin 42 is active (low).
- b. Check limiter clearance is  $0.020 \pm 0.010$  inch ( $0.508 \pm 0.254$  mm). See figure 5-7.
- c. If clearances are not within tolerance, loosen limiter nut. Rotate limiter screw until proper clearance is obtained.
- d. Tighten limiter nut and repeat steps (a) and (b) above.

#### 5.4.7 Index Sector Timing

- a. Insert Alignment Diskette (SA810 = SA120, SA860 = SA122).
- b. Step carriage to track 01.
- c. Sync oscilloscope external negative, on TP12 (—INDEX).
- d. Set time base to 50  $\mu$ sec/division.

- e. Observe timing between start of sweep and first data pulse. This should be  $200 \pm 100 \mu\text{sec}$ . If timing is not within tolerance, continue procedure.
- f. Loosen holding screw in index detector until detector is just able to be moved.
- g. Observing timing, adjust detector until timing is  $200 \pm 100 \mu\text{sec}$  for hard sector applications, and  $200 \pm 200 \mu\text{s}$  for soft sectored applications. Ensure detector assembly is against registration surface on top plate.
- h. Tighten holding screw.
- i. Recheck timing.
- j. Seek to track 76. Reverify timing.

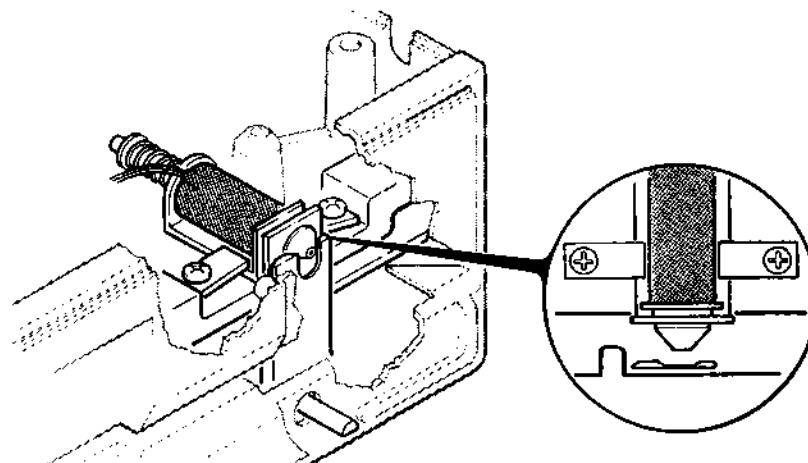


39231-15

**FIGURE 5-7. TRACK 00 CARRIAGE LIMITER CLEARANCE**

#### 5.4.8 Door Lock

- a. Rotate door knob counter-clockwise to fully closed position. Observe door lock plunger and door lock shutter. Door lock solenoid should not touch shutter. See figure 5-8.



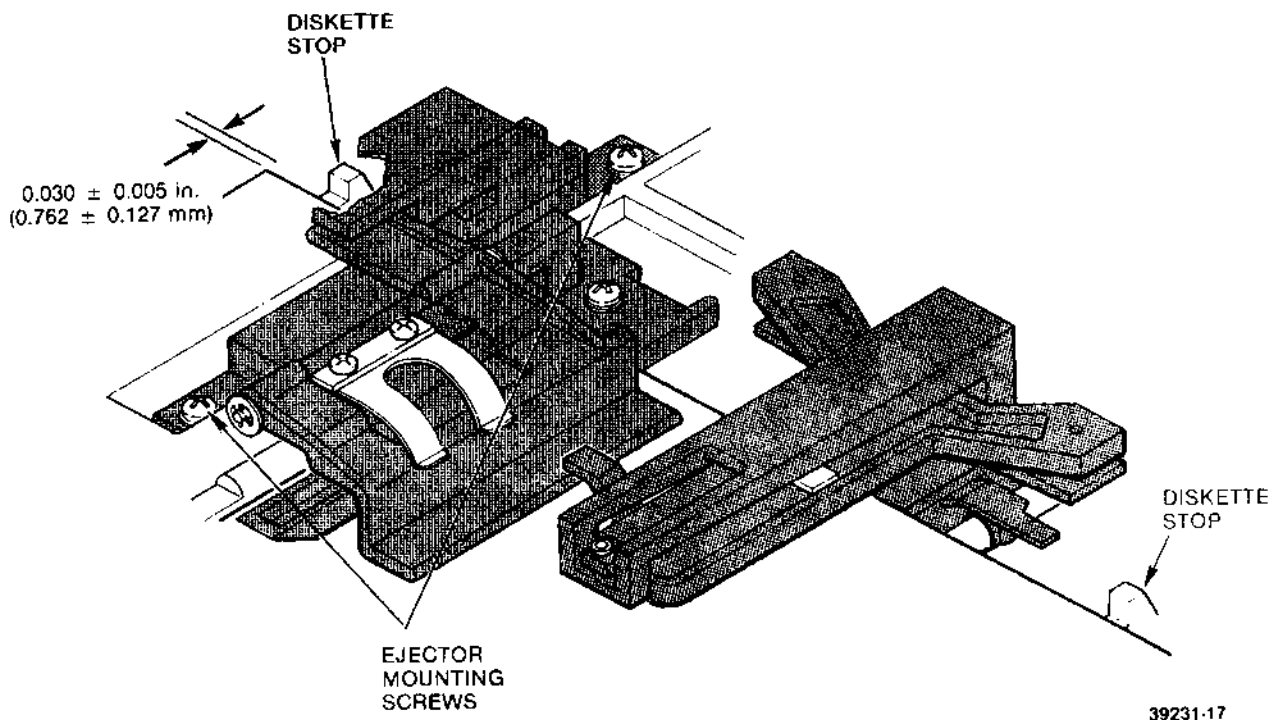
39231-16

**FIGURE 5-8. DOOR LOCK SOLENOID ADJUSTMENT**

- b. Select drive. Door lock plunger should extend so that it fully seats into shutter cavity.
- c. If proper clearances are not obtained, continue adjustment procedure.
- d. Remove drive PCB.
- e. Loosen two mounting screws securing door lock assembly.
- f. While fully extending door lock plunger, slide door lock assembly until plunger fully seats into shutter cavity.
- g. Secure mounting screws.

#### 5.4.9 Ejector/Bail

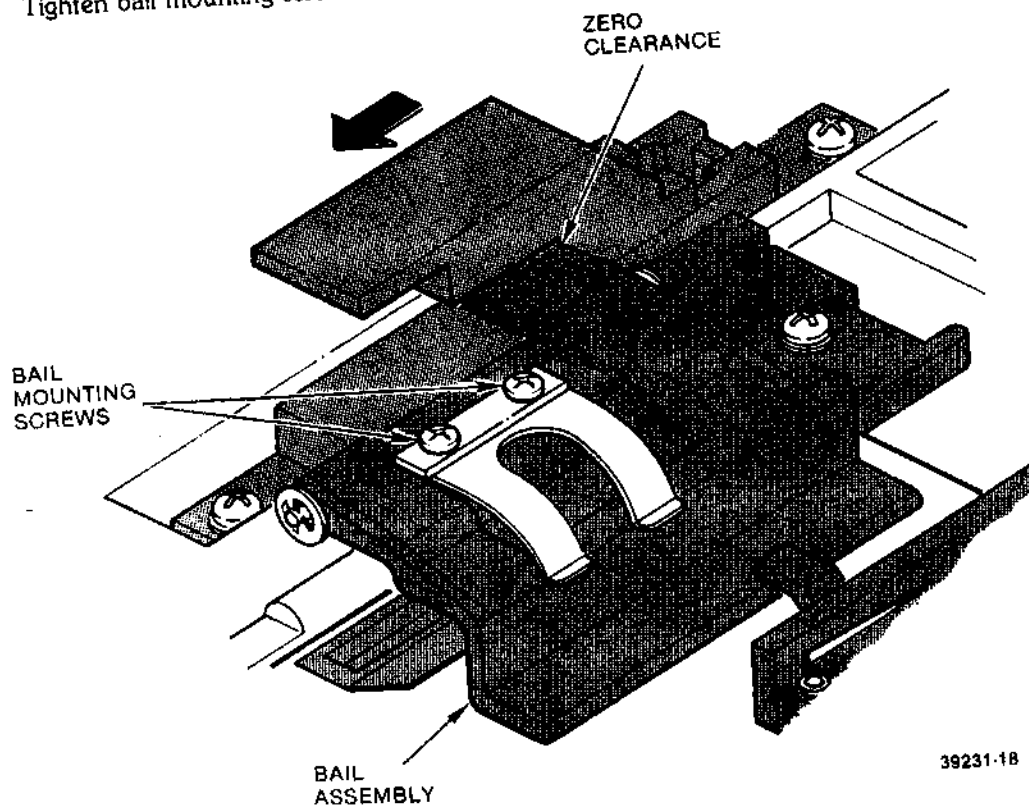
- a. Insert diskette.
- b. With rear edge of diskette jacket touching diskette ejector, there should be  $0.030 \pm 0.005$  inch ( $0.762 \pm 0.127$  mm) gap between rear of diskette jacket and diskette stops on casting. See figure 5-9.



**FIGURE 5-9. DISKETTE STOP CLEARANCE**

- c. If proper clearances are not obtained, loosen ejector mounting screws and slide assembly until proper clearance is obtained.
- d. Tighten ejector mounting screws and recheck clearance.
- e. Insert and eject media several times. If diskette fails to eject, continue procedure.
- f. Remove media.
- g. Loosen bail mounting screws.

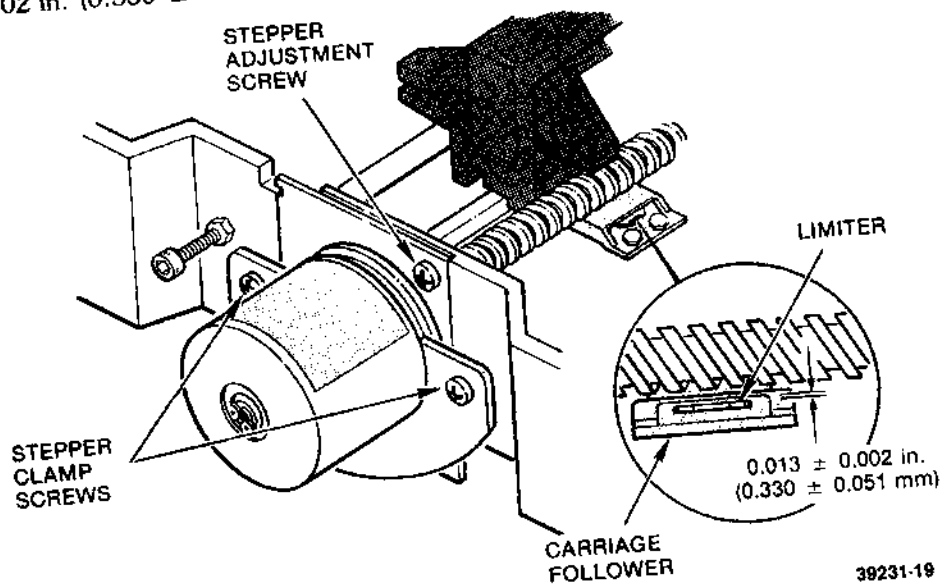
- h. With door knob in fully open (clockwise) position, rotate bail assembly so ejector slides over bail arm into forward or eject position. Slide bail assembly until bail arm is flush with ejector notch (figure 5-10).
- i. Tighten bail mounting screws.



**FIGURE 5-10. BAIL ASSEMBLY ADJUSTMENT**

**5.4.10 Stepper Motor**

- a. Check clearance between carriage follower and limiter (figure 5-11). Proper clearance is  $0.013 \pm 0.002$  in. ( $0.330 \pm 0.051$  mm). If clearance is not within specification, continue procedure.



**FIGURE 5-11. STEPPER MOTOR ADJUSTMENT**

- b. Loosen two stepper clamp screws and stepper adjustment screw. Move stepper motor until carriage follower just touches limiter. Tighten two stepper clamp screws until snug. Stepper adjustment screw remains loose.
- c. With screwdriver in slot in adjusting plate, move stepper motor up until clearance between follower and limiter is  $0.013 \pm 0.002$  in. ( $0.330 \pm 0.051$  mm). Tighten stepper adjustment screw and stepper clamp screws.

## **5.5 REMOVALS AND REPLACEMENTS**

### **5.5.1 Faceplate and Door Knob**

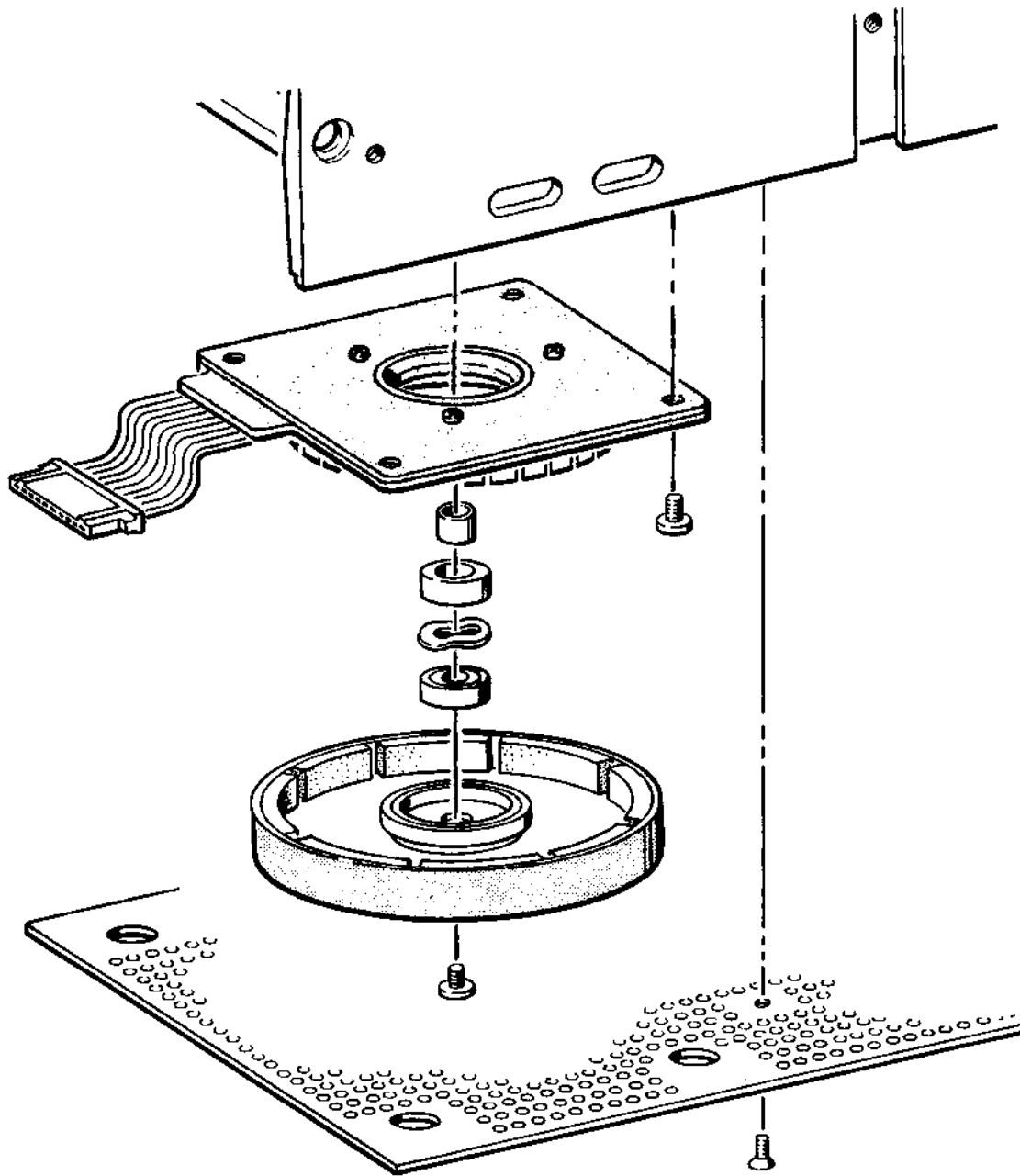
- a. Loosen two allen head set screws on door knob.
- b. Remove door knob. Pull door knob forward and away from faceplate.
- c. Remove screws retaining EMI/RFI bottom shield. Remove shield.
- d. From PCB side of drive, loosen two screws on back side of faceplate. Pull faceplate forward and away from drive casting.
- e. To reinstall, reverse above procedure.

### **5.5.2 Drive Motor Assembly**

- a. Remove screws retaining bottom EMI/RFI shield (see figure 5-12). Remove shield.
- b. Remove screw retaining rotor.
- c. Remove rotor.
- d. Disconnect motor power cable at PCB.
- e. Remove four screws retaining motor assembly.
- f. Lift motor assembly up and away from casting. Moderate force is required as there is an interference fit between motor assembly and spindle collar on drive casting.
- g. To reinstall:
  - Set motor assembly on casting.
  - Place spindle motor centering tool (P/N 54650) over motor assembly.
  - Secure four motor assembly retaining screws.
  - Perform steps (a) through (d) in reverse order.

### **5.5.3 Top Plate Assembly**

- a. Remove screws retaining top EMI/RFI shield. Remove shield.
- b. Remove front plate.
- c. Insert a clean piece of bonded paper between read/write heads to prevent the heads from touching when the top plate is removed.
- d. Remove screws on outside edges of top plate assembly. Remove top plate by lifting up and away from casting, lifting at front side of top plate. Ensure bail assembly is past side 1 arm lift tab before lifting top plate clear.
- e. To reinstall, reverse procedure.



39231-20

**FIGURE 5-12. DRIVE MOTOR ASSEMBLY**

#### **5.5.4 Spindle Hub Assembly**

- a. Remove top plate assembly (paragraph 5.5.3).
- b. Remove screws retaining bottom EMI/RFI shield. Remove shield.
- c. Remove screw retaining drive motor rotor.
- d. Withdraw spindle hub from opposite side of casting.
- e. To reinstall, reverse procedure.

### **5.5.5 PCB Assembly**

- a. Remove screws retaining bottom EMI/RFI shield. Remove shield.
- b. Disconnect all PCB connector plugs.
- c. Remove screws retaining PCB.
- d. Lift PCB up and away from casting being careful to feed through connector without damaging cables.
- e. To reinstall, reverse procedure.

### **5.5.6 Door Lock Assembly**

- a. Remove screws retaining bottom EMI/RFI shield. Remove shield.
- b. Remove PCB (paragraph 5.5.5).
- c. Remove screws retaining door lock. Remove door lock.
- d. To reinstall, reverse procedure.
- e. Perform door lock adjustment (paragraph 5.4.7).

### **5.5.7 Side 1 Arm Assembly (SA860 Only)**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Disconnect side 1 head connector (J7) from PCB.
- c. Remove tie wrap on carriage side of drive.
- d. Remove side 1 cable from rubber grommet cable retainer.
- e. Insert a clean piece of bond paper between read/write heads.
- f. Remove screw securing downstop arm..
- g. Remove downstop arm.
- h. Remove side 1 arm.
- i. To reinstall, reverse procedure.

### **CAUTION**

After installing head cable, ensure there is enough slack to allow full motion without causing binds.

- j. Check SA860 downstop adjustment (paragraph 5.4.1).
- k. Check head alignment (paragraph 5.4.2).

### **5.5.8 Head and Carriage Assembly**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Disconnect head connector(s) from drive PCB.
- c. Remove tie wrap on carriage side of drive.
- d. Remove head cable(s) from rubber grommet cable retainer.

- e. Remove stepper motor connector from drive PCB.
- f. Remove two screws retaining stepper motor.
- g. Remove stepper motor.
- h. Loosen screws at each end of guide rod.
- i. Withdraw carriage assembly.
- j. Slide guide rod out from carriage assembly.
- k. To reinstall, reverse procedure.

#### **CAUTION**

After installing head cable(s), ensure there is enough slack to allow full motion without causing binds.

- l. Check SA860 downstop adjustment (paragraph 5.4.1).
- m. Check head alignment (paragraph 5.4.2).

#### **5.5.9 Clamp Hub Assembly**

- a. Remove top plate.
- b. Ensure door knob is in closed (clamped) position.
- c. Lift clamp hub away from top plate then away from bail shaft.
- d. To reinstall, reverse procedure.

#### **5.5.10 Bail Assembly**

- a. Remove top plate.
- b. Loosen screws on bail arm.
- c. Slide bail assembly off shaft.
- d. To reinstall, reverse procedure.
- e. Perform ejector/bail adjustment (paragraph 5.4.8).

#### **5.5.11 Track 00 Detector**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Remove connector (J5) from drive PCB.
- c. Remove bracket holding track 00 cable.
- d. Remove detector mounting screw to free detector.
- e. To reinstall, reverse procedure.
- f. Check track 00 adjustment (paragraph 5.4.5).

#### **5.5.12 Index/Sector LED Assembly**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Remove connector from appropriate header (J8B).



- c. Remove top plate.
- d. Remove detector mounting screw to free LED assembly.
- e. To reinstall, reverse procedure.

#### **5.5.13 Index/Sector Detector Assembly**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Remove connector from appropriate header (J3D) on PCB.
- c. Remove tie wrap holding detector cable.
- d. Remove bracket holding detector cable.
- e. Remove top plate.
- f. Remove index detector mounting screw.
- g. To reinstall, reverse procedure.
- h. Check index timing adjustment (paragraph 5.4.7).

#### **5.5.14 Write Protect Detector**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Remove connector from appropriate connector (J3A).
- c. Remove tie wrap holding cable.
- d. Remove screw holding detector bracket and remove assembly.
- e. To reinstall, reverse procedure.
- f. Register Write Protect Assembly against rib in casting. Secure detector mounting screw.

#### **5.5.15 Ejector Assembly**

- a. Remove screws retaining top EMI/RFI shield. Remove shield.
- b. Remove ejector mounting screws to free ejector.
- c. To reinstall, reverse procedure.
- d. Perform Ejector/Bail adjustment (paragraph 5.4.8).

#### **5.5.16 Door Switch**

- a. Remove screws retaining top and bottom EMI/RFI shields. Remove shields.
- b. Remove connector from appropriate header on PCB.
- c. Remove tie wrap holding door switch cable.
- d. Remove bracket holding door switch cable.
- e. Remove top plate.
- f. Remove door switch mounting screws.

- g. To reinstall, reverse procedure.
- h. Rotate door knob. Single click should be heard from door switch.

## 5.6 RECOMMENDED INCOMING RECEIVING INSPECTION

All Shugart drives are 100% adjusted and tested before leaving the factory. It is only necessary to inspect for shipping damage on receipt of drives.

### 5.6.1 Test Equipment

Inspection should be simple and test equipment kept to a minimum. Shugart recommends the following equipment:

- a. SA810/860 Service Manual.
- b. SA809 Exerciser.
- c. Exerciser Instruction Manual.
- d. Power supply for Exerciser (+5 V, +24 V).
- e. Oscilloscope.
- f. Alignment Diskette (SA120 for SA810, SA122 for SA860).

### 5.6.2 Procedure

- a. Unpack drive.
- b. Make visual inspection for physical damage.
- c. Ensure all power is off. Attach Exerciser cables to appropriate drive connectors.
- d. Power up.
- e. Insert work diskette.
- f. Set track addresses of 00 and 76 into Exerciser. Select drive and seek automatically for 5 minutes. After 5 minutes, move address 76 to 00. Seeking should stop and track 00 indicator should be on.
- g. Using nominal force, attempt to rotate door knob while drive is seeking. Knob should not rotate.

#### NOTE

Excessive force can defeat the door lock function.

- h. With SA810/860 Service Manual, SA120/122 Alignment Diskette, and Exerciser Instruction Manual as guides, perform the following checks:
  - Azimuth Check (paragraph 5.4.3).
  - Index Sector Adjustment (paragraph 5.4.7). Soft sector applications do not require this check. If soft sector check is desired, timing specification is  $200 \pm 200$  msec.
  - Head Radial Alignment (paragraph 5.4.2).
- i. Remove SA120/122 alignment diskette. Insert work diskette.
- j. Seek to track 76 and write 2F on both sides. Minimum read back signal from each head should be 130 mV.
- k. Connect scope to TP I and verify index timing is  $166.7 \pm 1$  ms.
- l. Power off.
- m. Remove connectors and repack drive.

This procedure verifies that the critical functions of the drive are working properly, i.e., the file will read and write, the drive will access, the disk is rotating at the proper speed, and critical adjustments are within specifications.

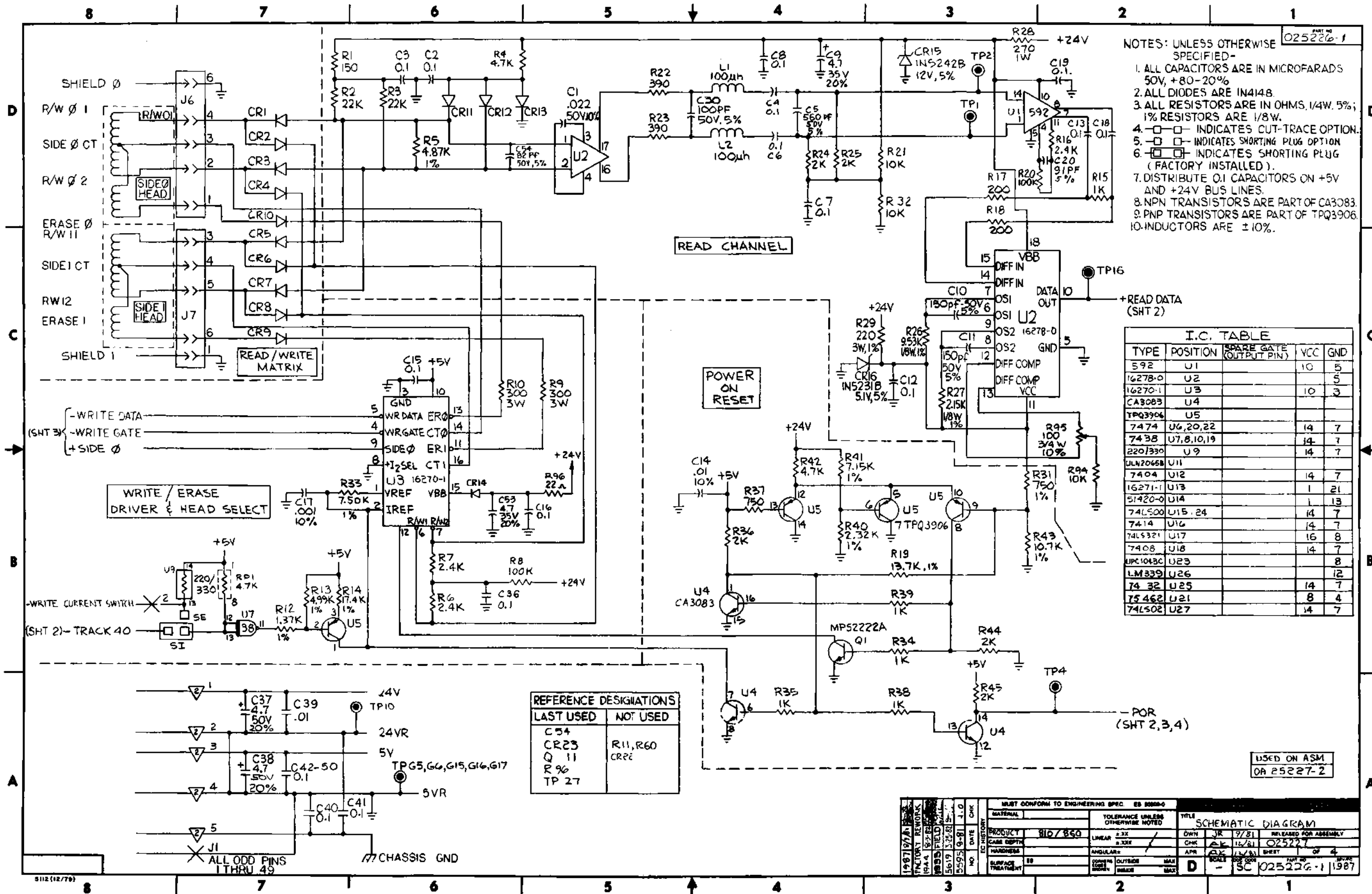
## SECTION VI SCHEMATIC DIAGRAMS

The following schematic diagrams are furnished as an aid to malfunction analysis. Table 6-1 shows the applicability of each diagram.

**TABLE 6-1. SCHEMATIC DIAGRAM APPLICABILITY**

FIGURE	TITLE	APPLICABILITY
6-1	SCHEMATIC DIAGRAM (4 SHEETS)	25227
6-2	SCHEMATIC DIAGRAM (4 SHEETS)	25247
6-3	SCHEMATIC DIAGRAM (4 SHEETS)	25249
6-4	LOGIC EQUIVALENT P/N 16271, LOCATION U13	25227, 25247, AND 25249
6-5	LOGIC EQUIVALENT P/N 51420, LOCATION U14	25227, 25247

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- NOTES: UNLESS OTHERWISE SPECIFIED-
1. ALL CAPACITORS ARE IN MICROFARADS 50V, +80-20%
  2. ALL DIODES ARE IN4148
  3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%; 1% RESISTORS ARE 1/8W.
  4. □ □ INDICATES CUT-TRACE OPTION.
  5. □ □ INDICATES SHORTING PLUG OPTION
  6. □ □ INDICATES SHORTING PLUG (FACTORY INSTALLED).
  7. DISTRIBUTE 0.1 CAPACITORS ON +5V AND +24V BUS LINES.
  8. NPN TRANSISTORS ARE PART OF CA3083.
  9. PNP TRANSISTORS ARE PART OF TPQ3906.
  10. INDUCTORS ARE ±10%.

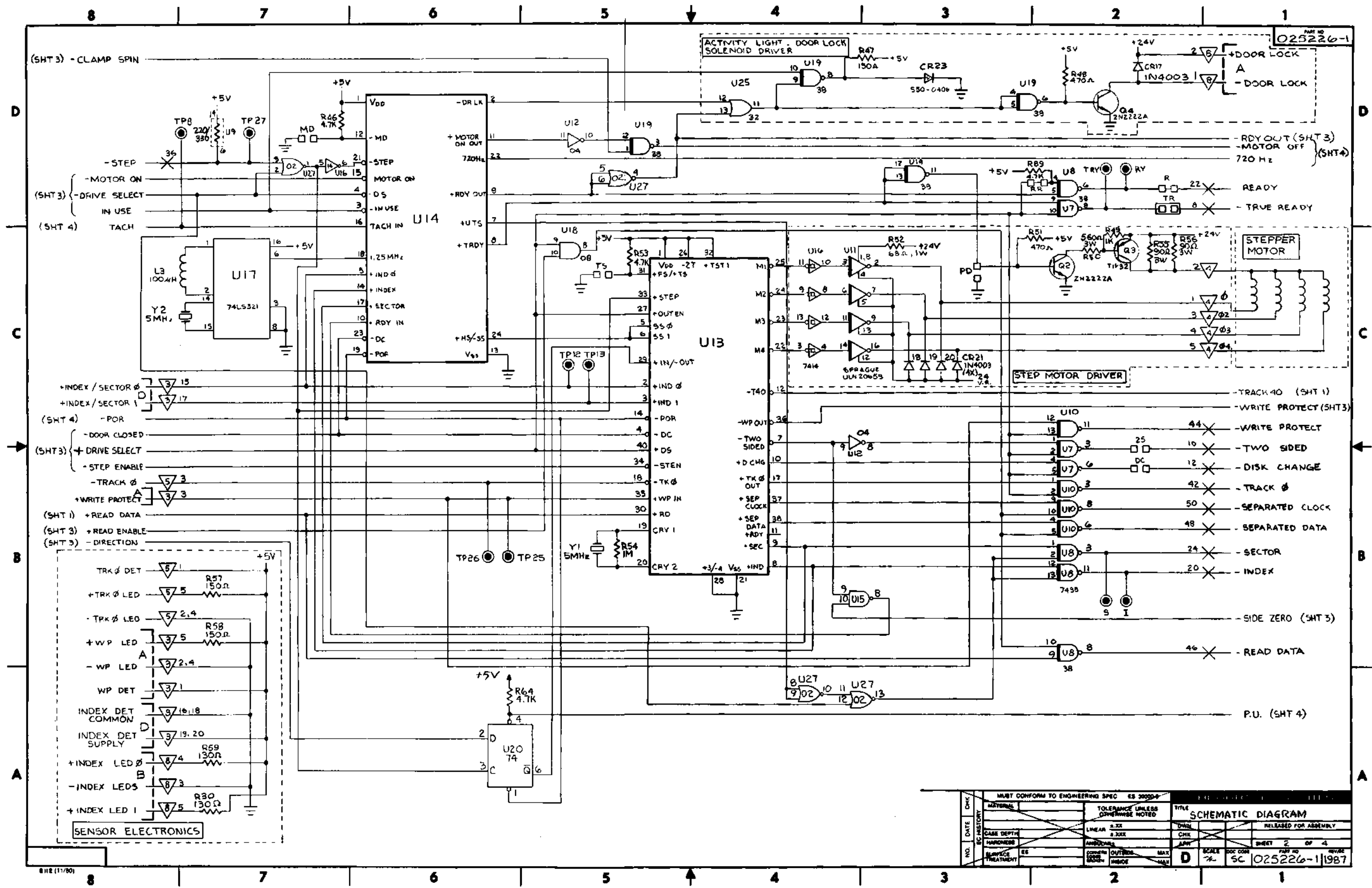
I.C. TABLE				
TYPE	POSITION	SPARE GATE (OUTPUT PIN)	VCC	GND
592	U1		10	5
16278-0	U2			5
16270-1	U3		10	3
CA3083	U4			
TPQ3906	U5			
7474	U6,20,22		14	7
7438	U7,8,10,19		14	7
2201330	U9		14	7
ULN2065B	U11			
7404	U12		14	7
16271-1	U13		1	21
51420-0	U14		1	13
74LS00	U15, 24		14	7
7414	U16		14	7
74LS371	U17		16	8
7408	U18		14	7
UPC1043C	U23			8
LM339	U26			12
7432	U25		14	7
75462	U21		8	4
74LS02	U27		14	7

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C54	R11, R60
CR23	CR2C
Q11	
R96	
TP27	

USED ON ASM  
OR 25227-2

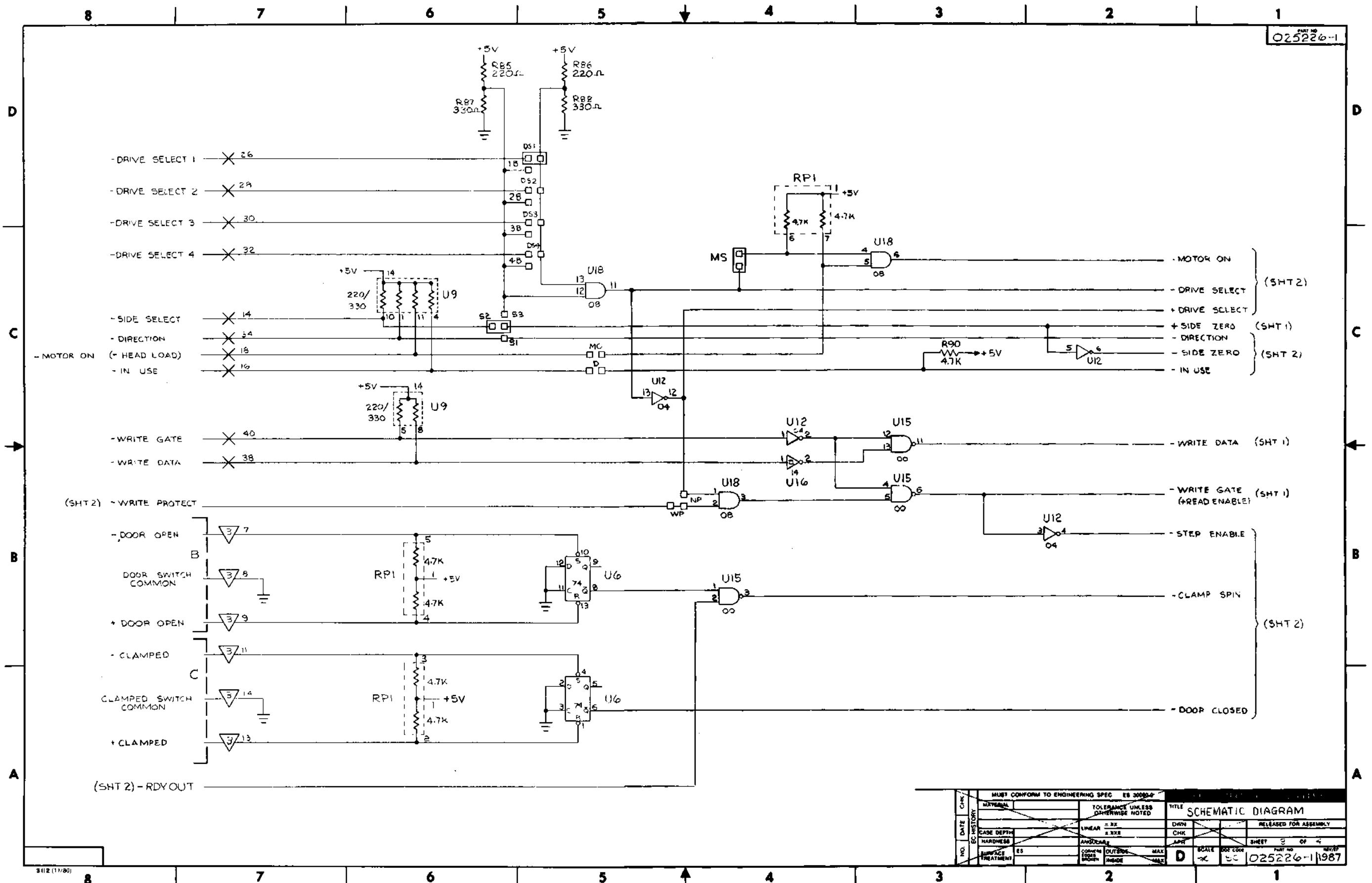
MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED		TITLE	
910/850		LINEAR 2:XX		SCHEMATIC DIAGRAM	
DWN		JK		9/81	
CHK		AK		11/81	
APR		OK		1/81	
SCALE		D		SC 025227-1	
DATE		1.0		1987	

FIGURE 6-1. SCHEMATIC DIAGRAM, PCB 25227 (SHEET 1 OF 4)



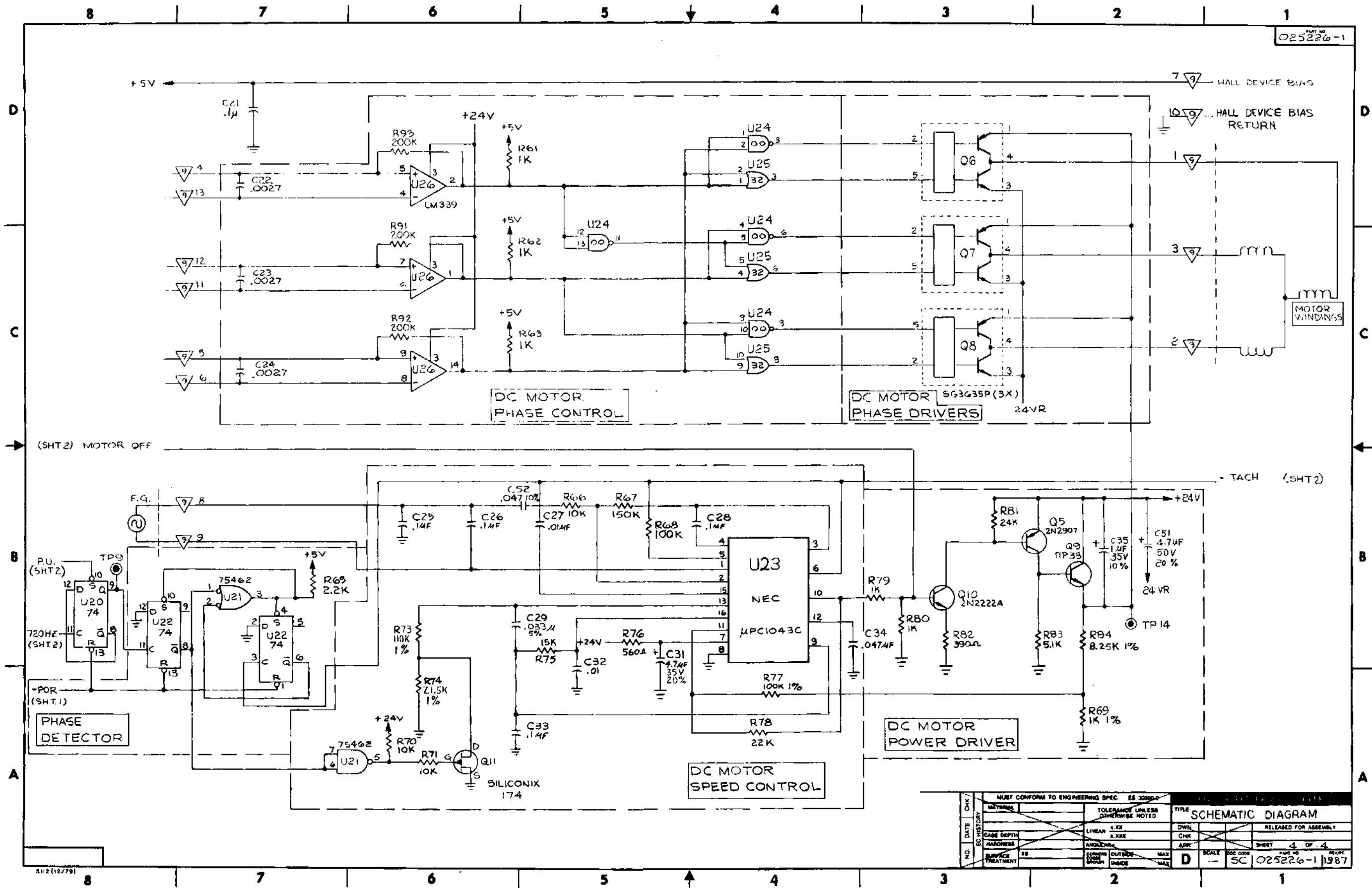
MUST CONFORM TO ENGINEERING SPEC ES 30004-4		TITLE	
MATERIAL	TOLEARNCE UNLESS OTHERWISE NOTED	SCHEMATIC DIAGRAM	
CAGE DEPTH	LINEAR & 2X	CHK	RELEASED FOR ASSEMBLY
HARDWARE	APW	APW	SHEET 2 OF 4
FINISH/TREATMENT	OUTSIDE MAX	SCALE	DOC CODE
	INSIDE MAX	D	SC 025226-11987

FIGURE 6-1. SCHEMATIC DIAGRAM, PCB 25227 (SHEET 2 OF 4)



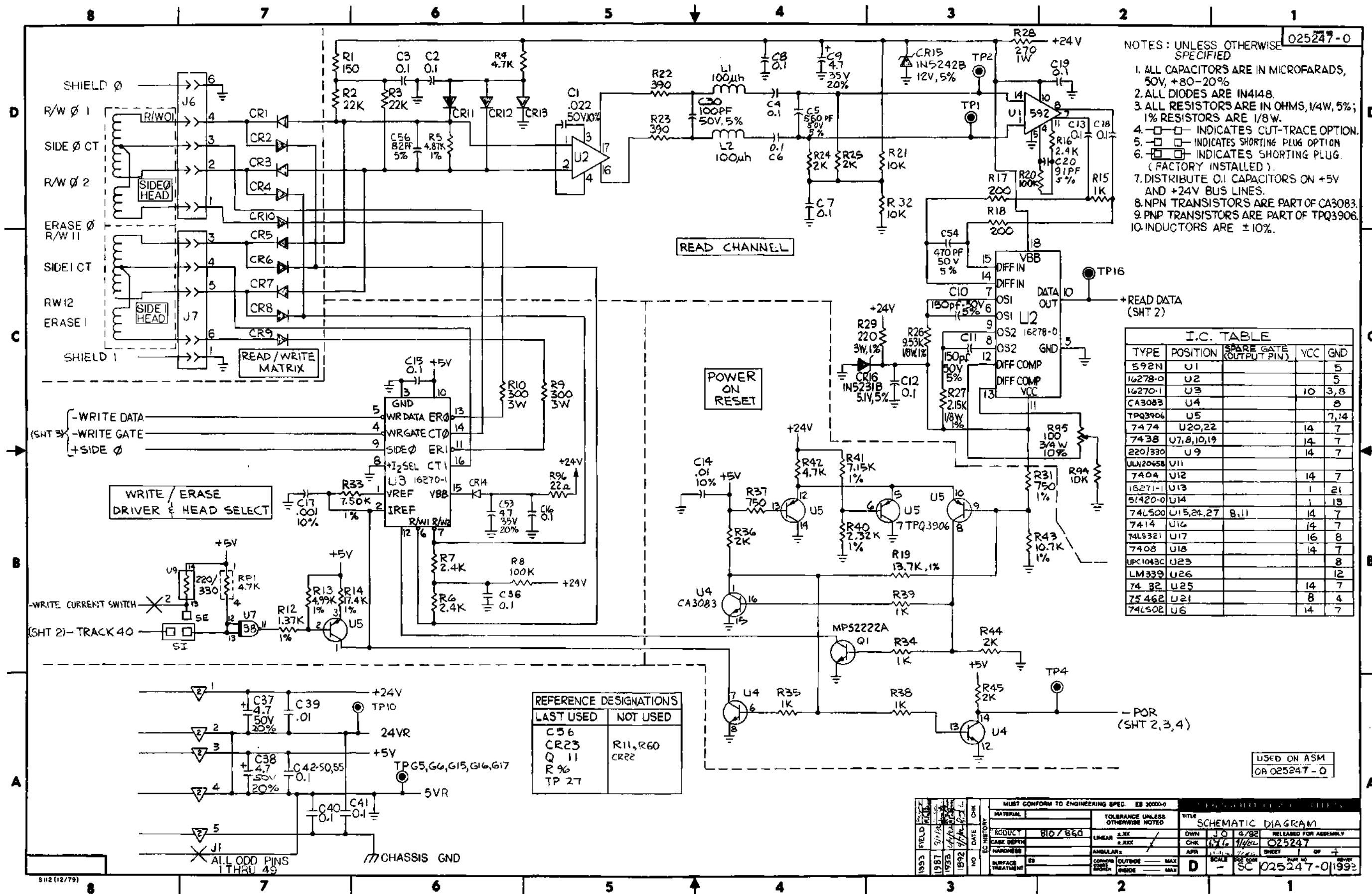
MUST CONFORM TO ENGINEERING SPEC ES 3000-6		TOLERANCE UNLESS OTHERWISE NOTED		TITLE SCHEMATIC DIAGRAM	
NO.	DATE	CHK	BY	SCALE	REV
1				D	1
SURFACE TREATMENT		FINISH		SCALE	
ES		OUTSIDE		D	
PART NO		REV		DATE	
025226-1		1987			

FIGURE 6-1. SCHEMATIC DIAGRAM, PCB 25227 (SHEET 3 OF 4) 6-7/6-8 (blank)



MUST CONFORM TO ENGINEERING SPEC. ES 3000-P		TOLERANCE UNLESS OTHERWISE NOTED		TYPE SCHEMATIC DIAGRAM	
ANYTHING		LINEAR	2.XX	DWN	RELEASED FOR ASSEMBLY
CASE DEPTH		ANGLED	2.XXX	CHK	
HARDNESS		CONTOUR	MAX	ARR	
SURFACE TREATMENT		OUTSIDE	MAX	SCALE	
		UNFINISH	MAX	D	
NO	DATE	CHK	BY	SCALE	SHEET 4 OF 4
				SC	025226-1 1987

FIGURE 6-1. SCHEMATIC DIAGRAM, PCB 25227 (SHEET 4 OF 4) 6-9/6-10 (blank)



- NOTES: UNLESS OTHERWISE SPECIFIED 025247-0
1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80-20%
  2. ALL DIODES ARE IN4148.
  3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%; 1% RESISTORS ARE 1/8W.
  4. INDICATES CUT-TRACE OPTION.
  5. INDICATES SHORTING PLUG OPTION
  6. INDICATES SHORTING PLUG (FACTORY INSTALLED).
  7. DISTRIBUTE 0.1 CAPACITORS ON +5V AND +24V BUS LINES.
  8. NPN TRANSISTORS ARE PART OF CA3083.
  9. PNP TRANSISTORS ARE PART OF TPQ3906.
  10. INDUCTORS ARE ±10%.

**I.C. TABLE**

TYPE	POSITION	SPARE GATE (OUTPUT PIN)	VCC	GND
592N	U1			5
16278-0	U2			5
16270-1	U3		10	3,8
CA3083	U4			8
TPQ3906	U5			7,14
7474	U20,22		14	7
7438	U7,8,10,19		14	7
820330	U9		14	7
ULA2045B	U11			
7404	U12		14	7
16271-1	U13		1	21
51420-0	U14		1	13
74LS00	U15,24,27	8,11	14	7
7414	U16		14	7
74LS32	U17		16	8
7408	U18		14	7
UKC1043C	U23			8
LM339	U26			12
7432	U25		14	7
75462	U21		8	4
74LS02	U6		14	7

FIGURE 6-2. SCHEMATIC DIAGRAM, PCB 25247 (SHEET 1 OF 4)



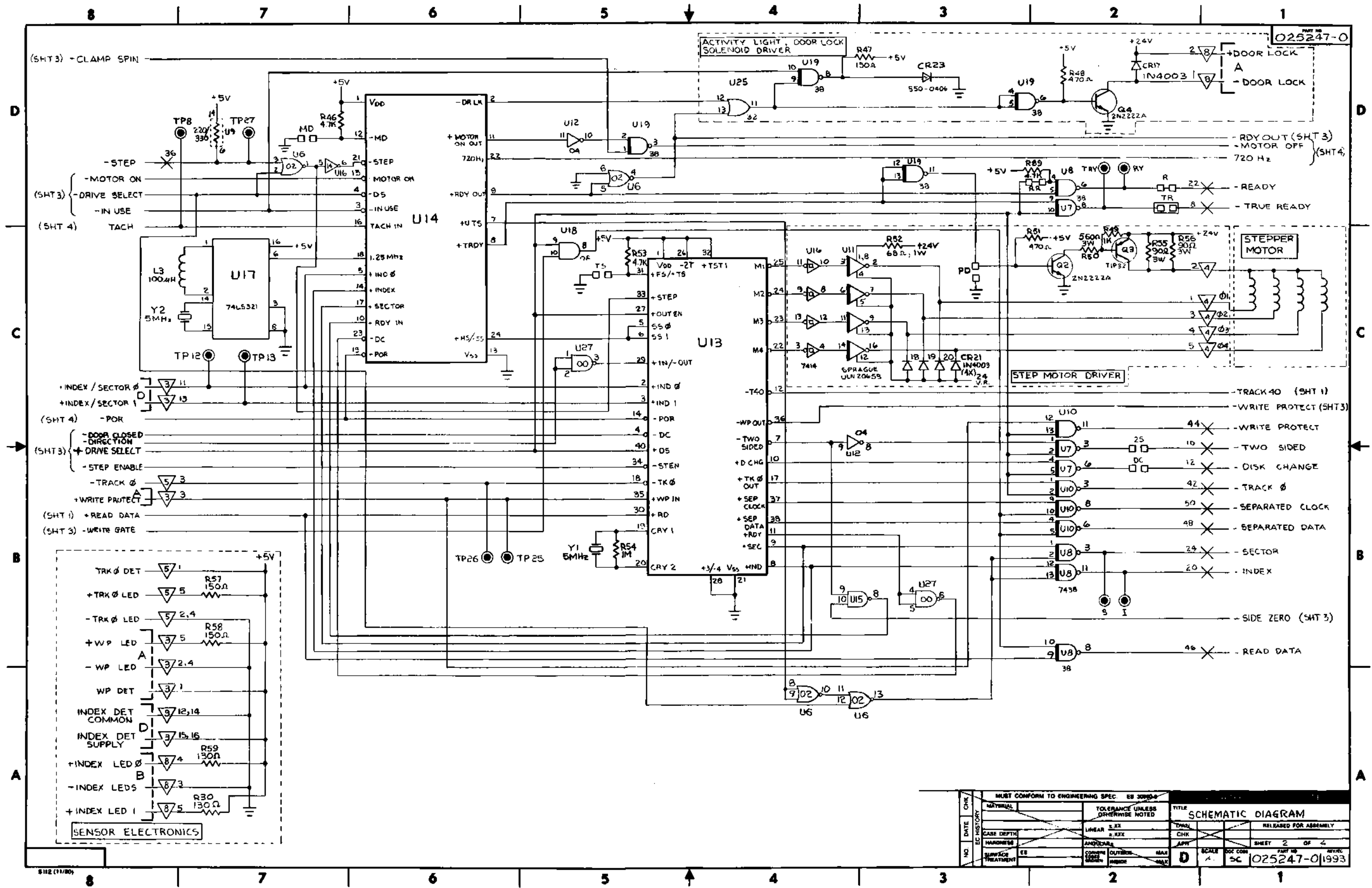


FIGURE 6-2. SCHEMATIC DIAGRAM, PCB 25247 (SHEET 2 OF 4)

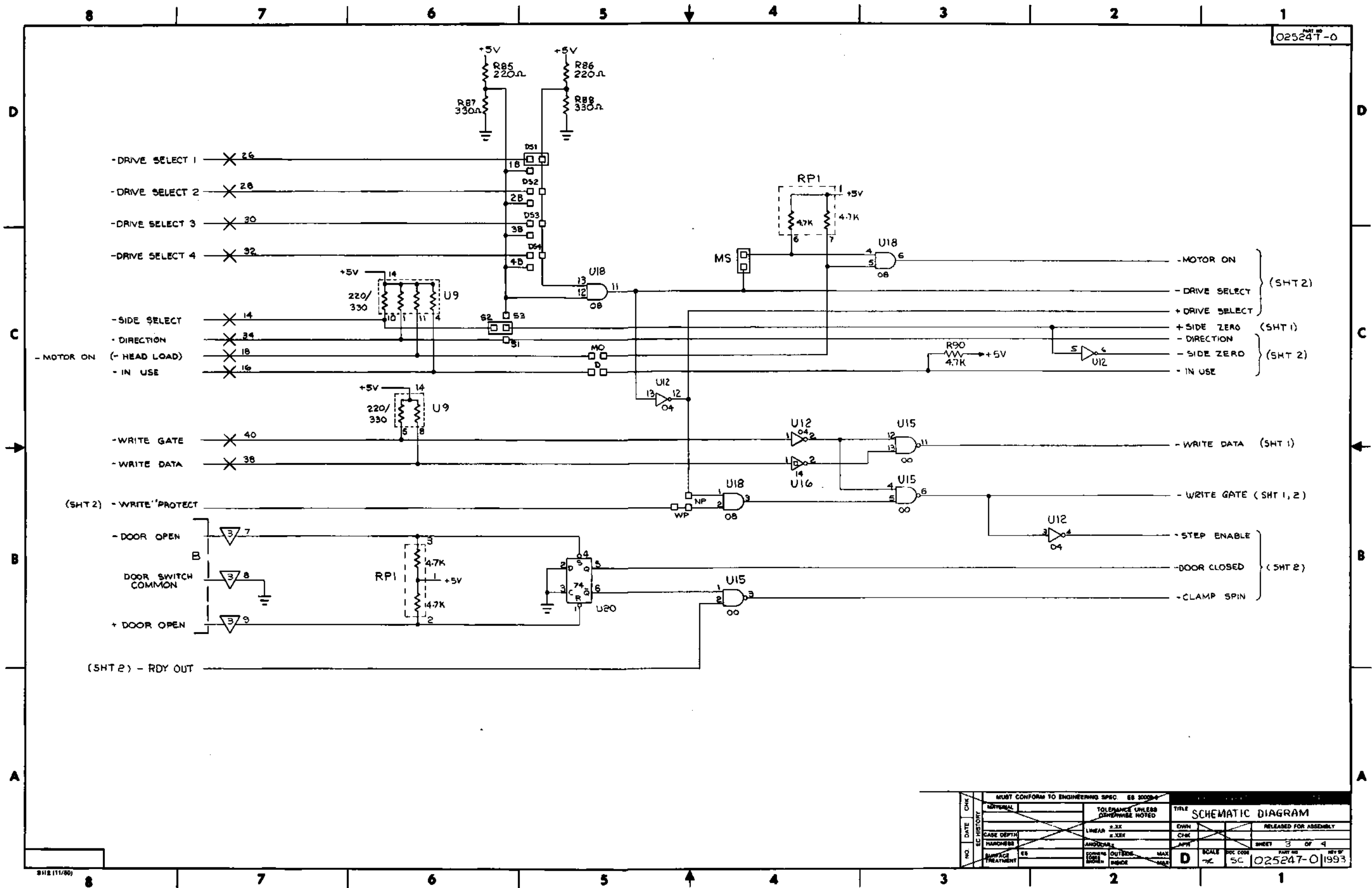


FIGURE 6-2. SCHEMATIC DIAGRAM, PCB 25247 (SHEET 3 OF 4)

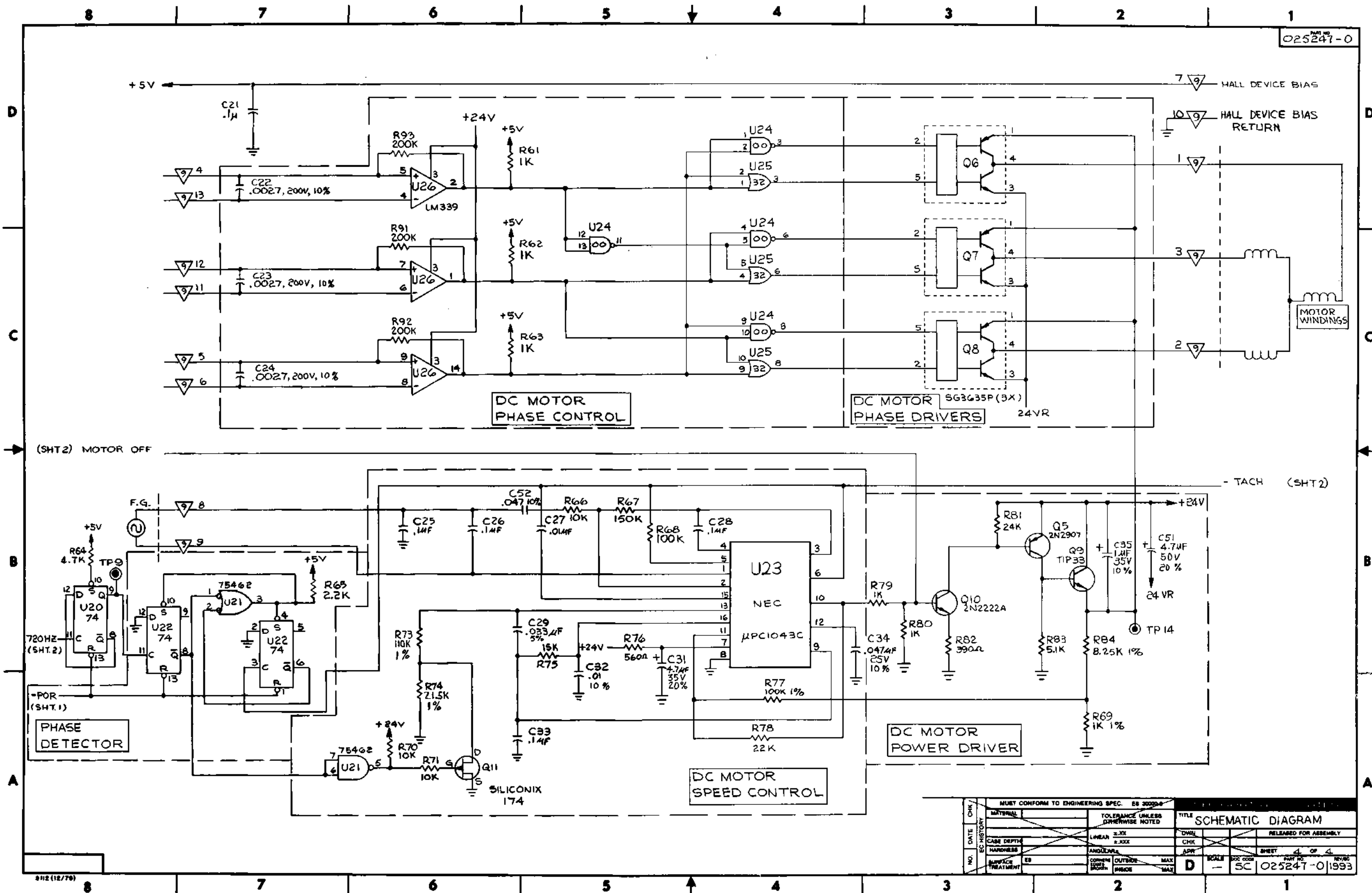
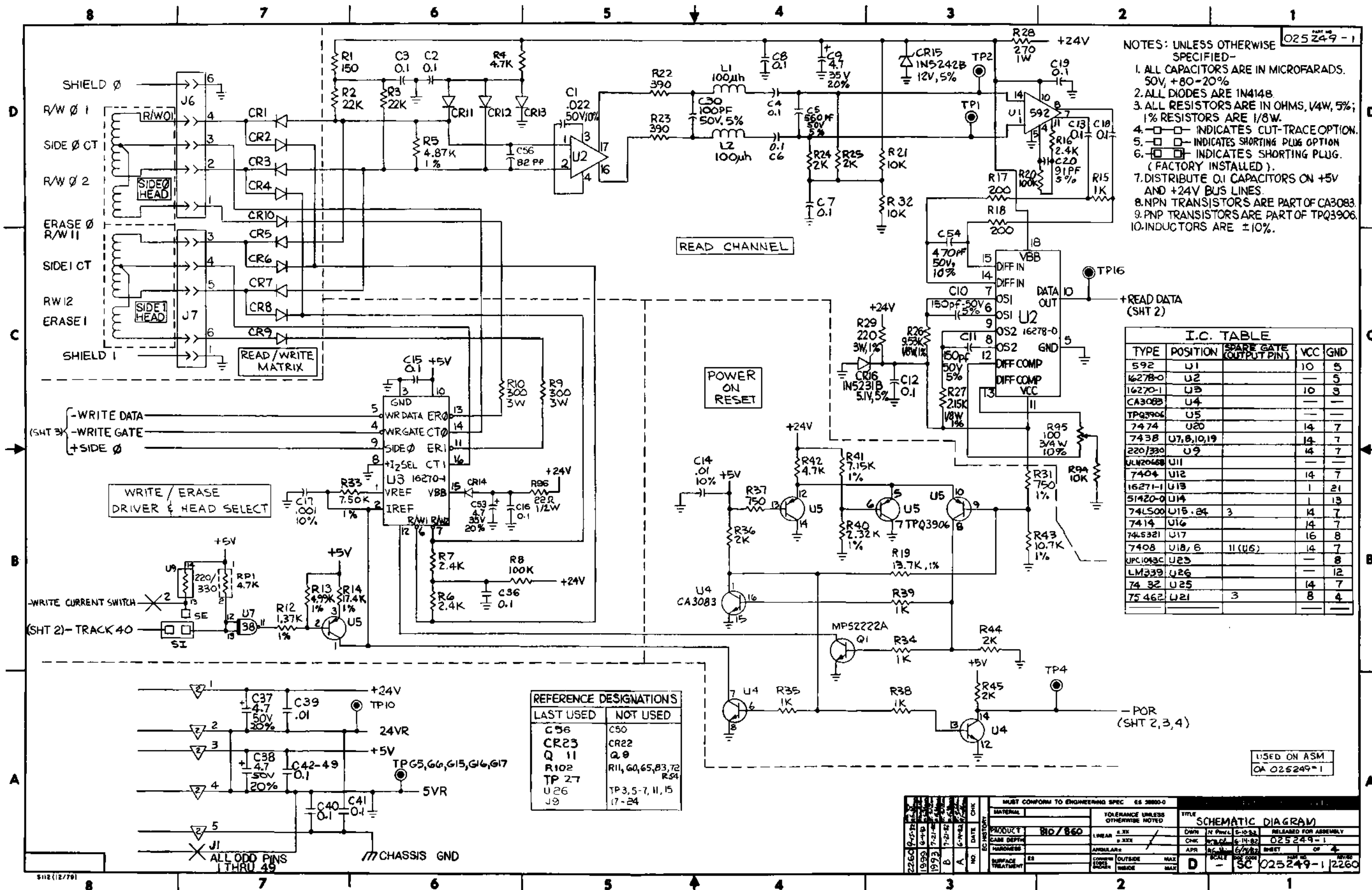


FIGURE 6-2. SCHEMATIC DIAGRAM, PCB 25247 (SHEET 4 OF 4)



- NOTES: UNLESS OTHERWISE SPECIFIED-
1. ALL CAPACITORS ARE IN MICROFARADS. 50V, +80-20%
  2. ALL DIODES ARE 1N4148
  3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%; 1% RESISTORS ARE 1/8W.
  4. □ □ INDICATES CUT-TRACE OPTION.
  5. □ □ INDICATES SHORTING PLUG OPTION.
  6. □ □ INDICATES SHORTING PLUG. (FACTORY INSTALLED).
  7. DISTRIBUTE 0.1 CAPACITORS ON +5V AND +24V BUS LINES.
  8. NPN TRANSISTORS ARE PART OF CA3083
  9. PNP TRANSISTORS ARE PART OF TPQ3906
  10. INDUCTORS ARE ±10%.

I.C. TABLE

TYPE	POSITION	SPARE GATE (OUTPUT PIN)	VCC	GND
592	U1		10	5
16278-0	U2			5
16270-1	U3		10	3
CA3083	U4			
TPQ3906	U5			
7474	U20		14	7
7438	U7,8,10,19		14	7
220/330	U9		14	7
LM2048	U11			
7404	U12		14	7
16271-1	U13		1	21
51420-0	U14			13
74LS00	U15, 24	3	14	7
7414	U16		14	7
74LS32	U17		16	8
7408	U18, 6	11 (U5)	14	7
UPC1043C	U23			8
LM339	U26			12
7432	U25		14	7
75462	U21	3	8	4

REFERENCE DESIGNATIONS

LAST USED	NOT USED
C56	C50
CR23	CR22
Q 11	Q 9
R102	R11, G0, 65, 83, 72, R54
TP 27	TP 3, 5-7, 11, 15
U26	(7-24)
J9	

MUST CONFORM TO ENGINEERING SPEC ES 3880-0

MATERIAL		TOLERANCE UNLESS OTHERWISE NOTED		TITLE	
PRODUCT	RD/860	LINEAR	±.3X	DWN	N Pw/L 5-10-82
CAM DEPTH		CNK	±.3X	RELEASED FOR ASSEMBLY	025249-1
HARDNESS		ANGULAR		APR	6/11/82
SURFACE TREATMENT	ES	CONVEX	OUTSIDE	SCALE	1/8" = 1"
		DEPTH	INSIDE	MAX	
				MIN	
				SCHEMATIC DIAGRAM	
				D	
				SC 025249-1	
				2260	

FIGURE 6-3. SCHEMATIC DIAGRAM, PCB 25249 (SHEET 1 OF 4)

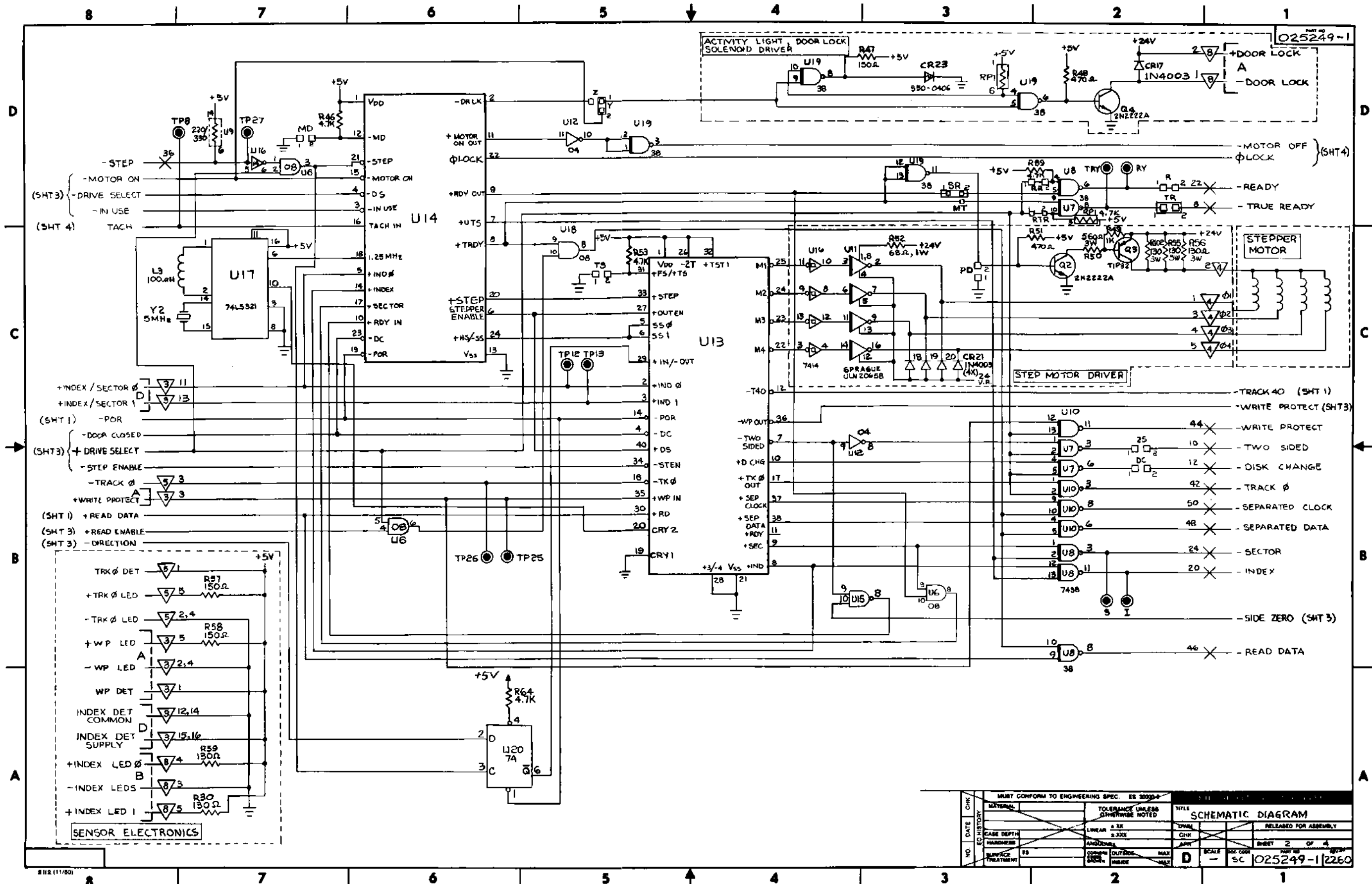
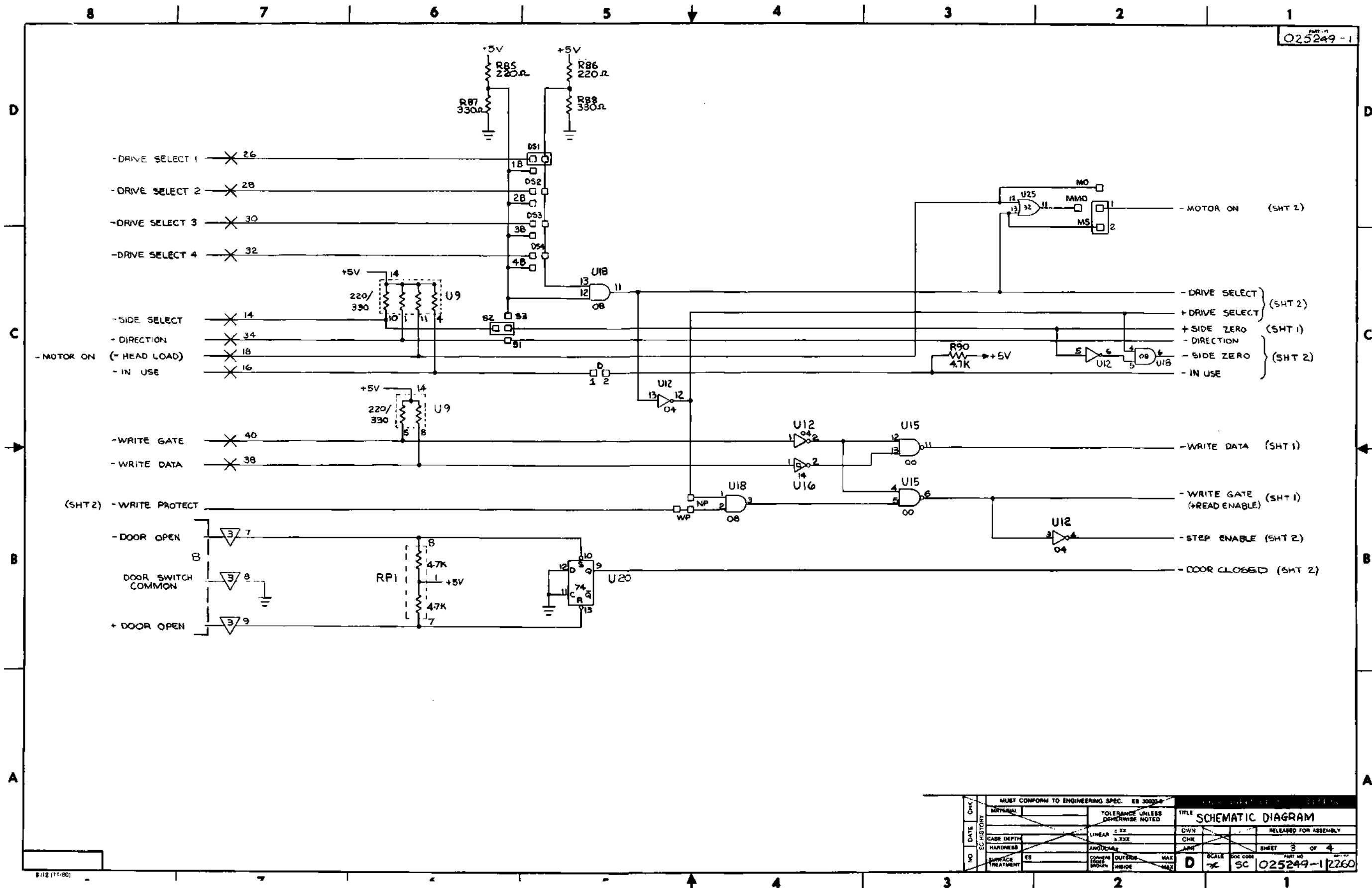


FIGURE 6-3. SCHEMATIC DIAGRAM, PCB 25249 (SHEET 2 OF 4)



MUST CONFORM TO ENGINEERING SPEC. EB 3000*				TITLE SCHEMATIC DIAGRAM			
NO	DATE	CHK	SCHEMATIC	TOLERANCE UNLESS OTHERWISE NOTED	LINEAR ±.XX	ANGULAR ±.XX	SCALE D
							SC 025249-1
							SHEET 3 OF 4
							2260

FIGURE 6-3. SCHEMATIC DIAGRAM, PCB 25249 (SHEET 3 OF 4)

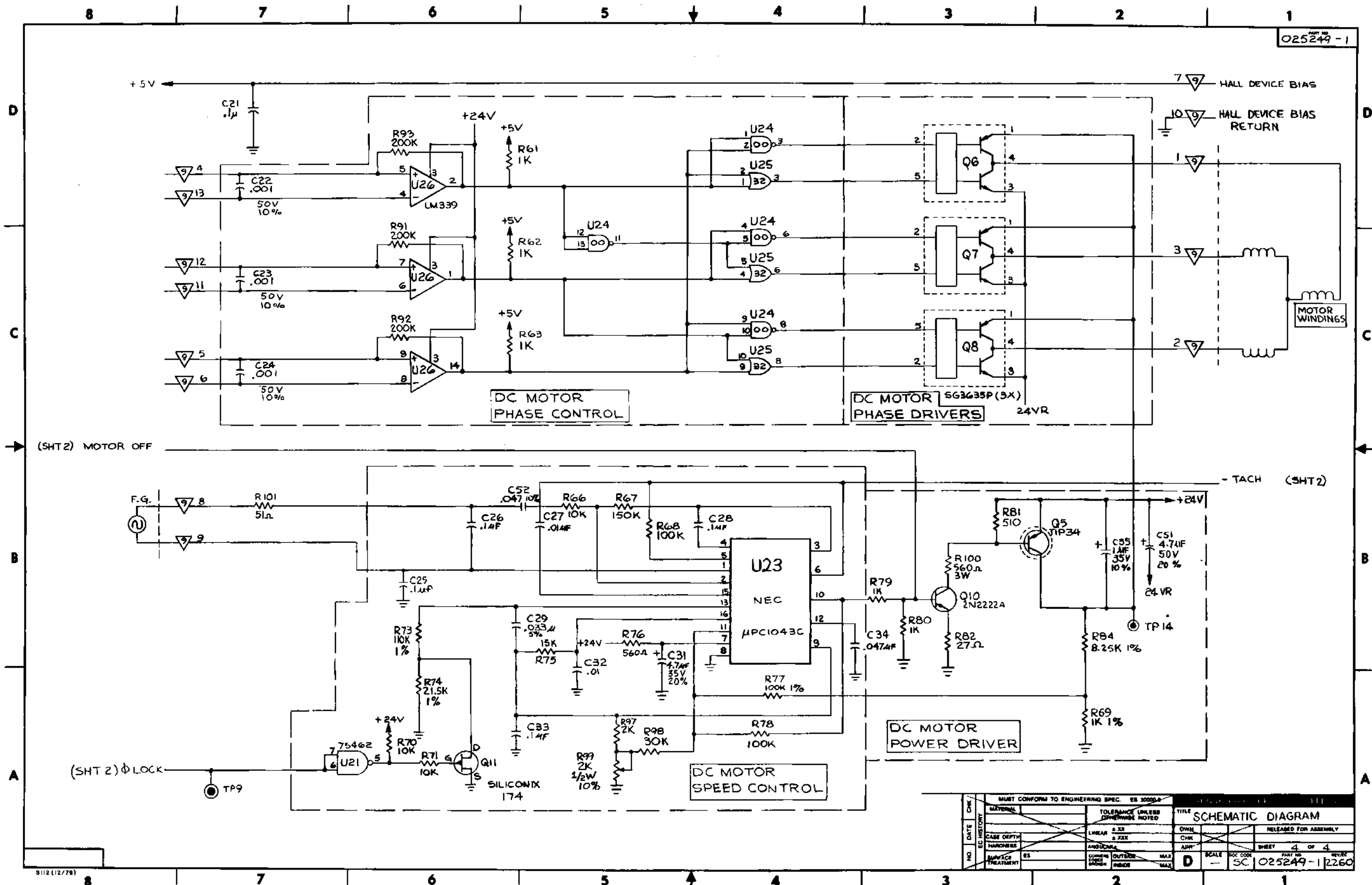


FIGURE 6-3. SCHEMATIC DIAGRAM, PCB 25249 (SHEET 4 OF 4)

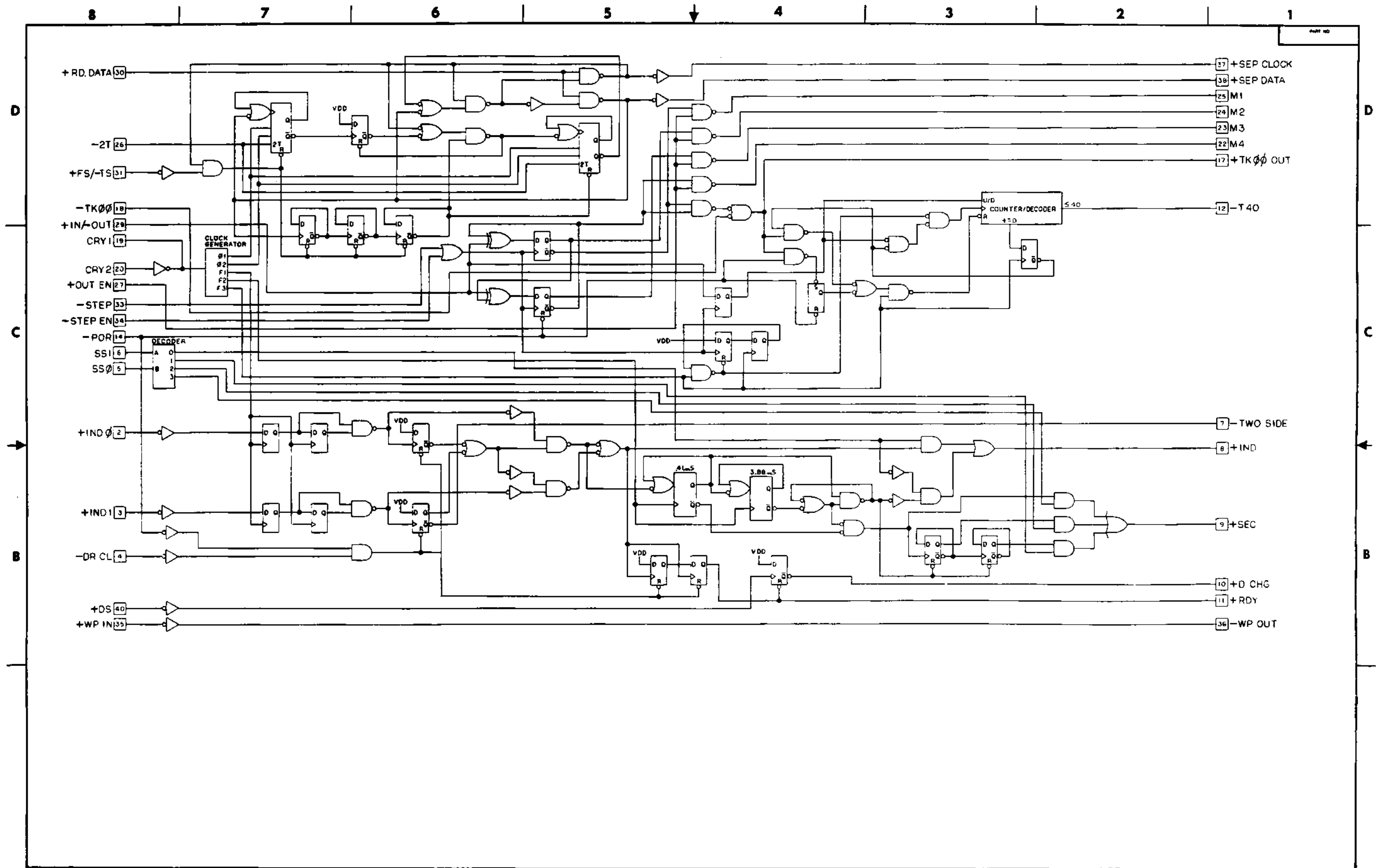
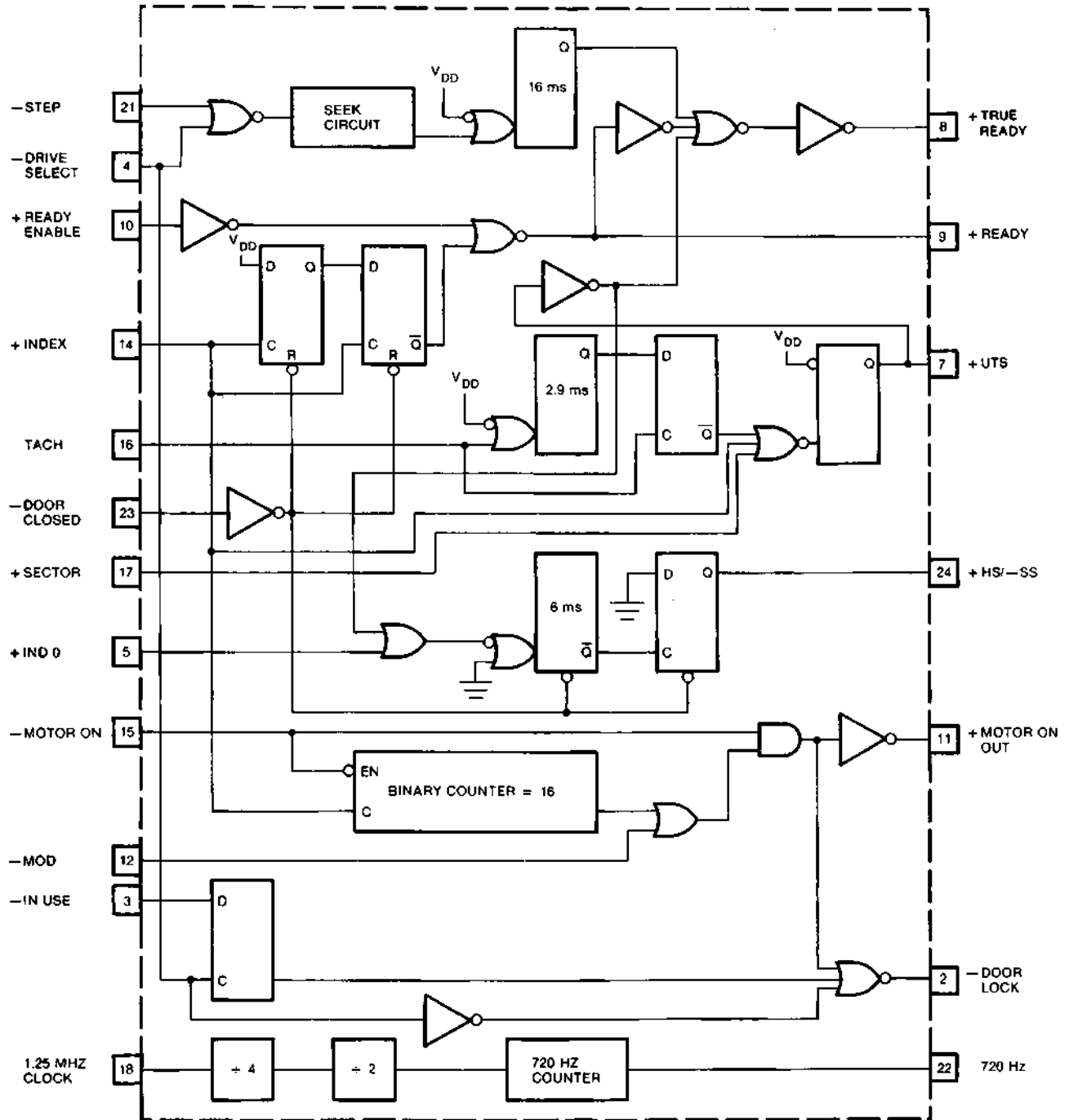


FIGURE 6-4. LOGIC EQUIVALENT,  
P/N 16271-X, LOCATION U13





NOTE: USED ON PCB ASSEMBLIES 25227-X AND 25247-X.

39231-21

FIGURE 6-5. LOGIC EQUIVALENT P/N 51420, LOCATION U14

## **SECTION VII ILLUSTRATED PARTS CATALOG**

### **7.1 DESCRIPTION**

The Illustrated Parts Catalog (IPC) is arranged so that the figure will always precede the parts listing and, when possible, will appear directly above the parts list or on the left hand page immediately preceding it.

The first number in the list will always refer to the figure number. The second number will refer to the reference number of the part within the figure.

Part numbers enclosed in parentheses refer to parts belonging to a Next Higher Assembly (NHA) and are of importance only to those customers with alternate assemblies. Following the descriptions of these parts, the designation NHA P/N \_\_\_\_\_ gives the part number of the assembly to which they pertain. When applicable to the customer's assembly, these alternate parts will be used in lieu of the part listed directly above them. Assume that the quantity per assembly for these alternate parts is the same unless otherwise listed.

When an assembly is referred to within a figure and a further breakdown is shown on another figure, then the referenced figure will be called out.

### **7.2 INDENTED LEVEL**

The parts list is indented to show the levels of assembly within a figure. The major assembly will always be unindented. All parts or assemblies that attach to the assembly will be indented one space. Parts within these assemblies will be indented two spaces and so on.

### **7.3 QUANTITY PER ASSEMBLY**

The quantity listed is the quantity used on the major assembly. Major assemblies themselves will never have a quantity listed.

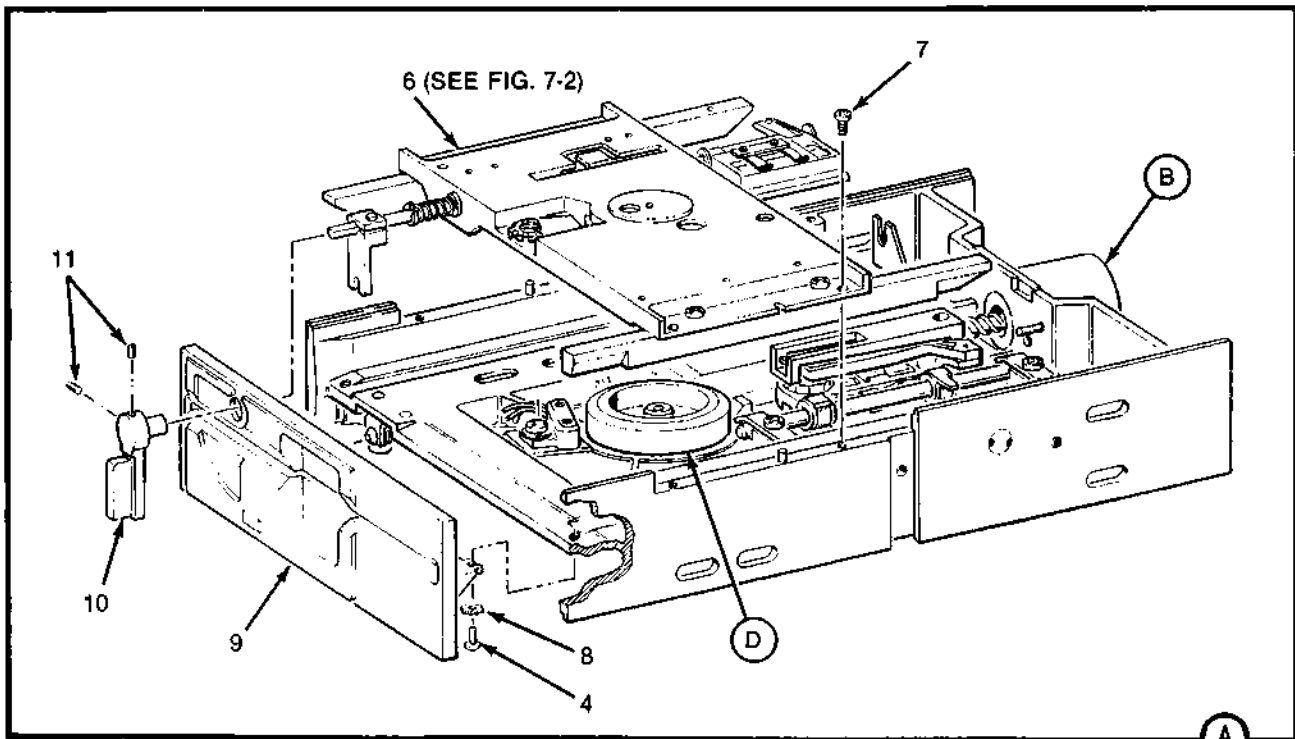
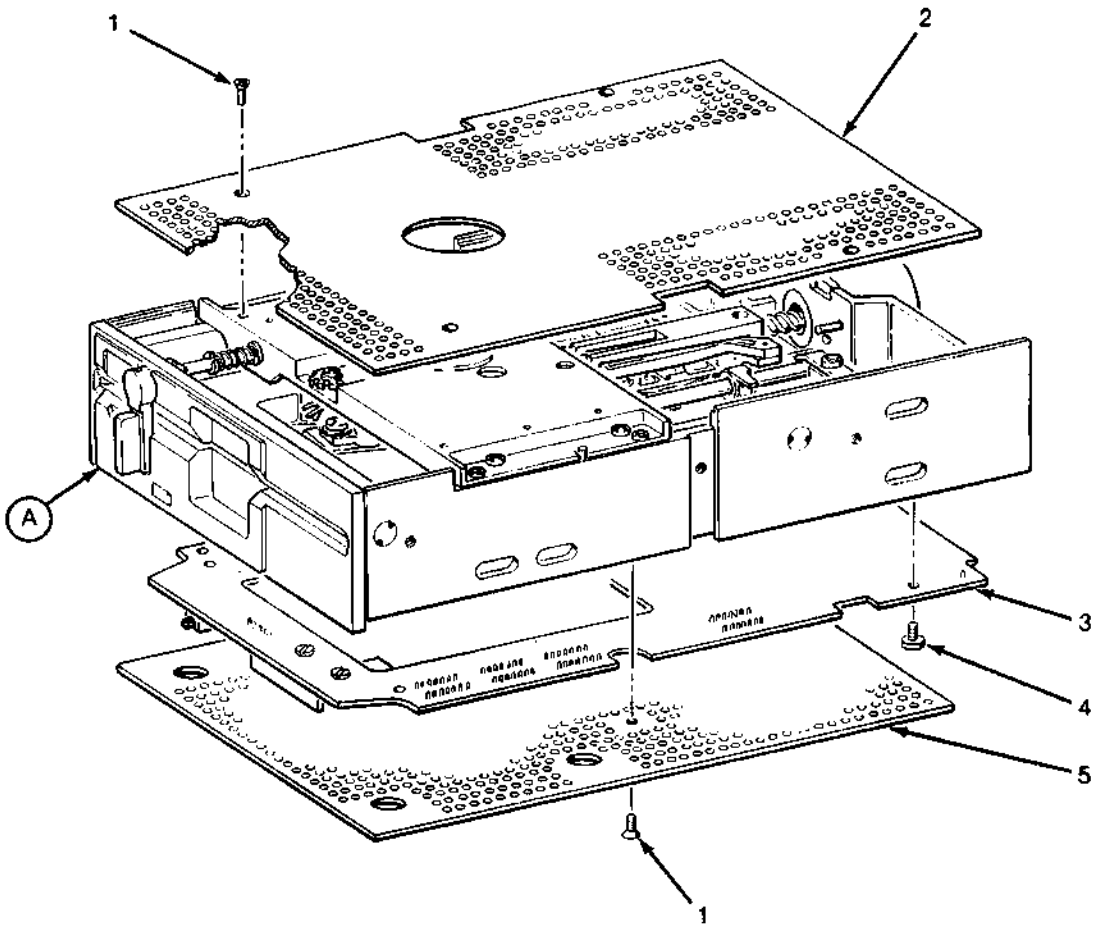
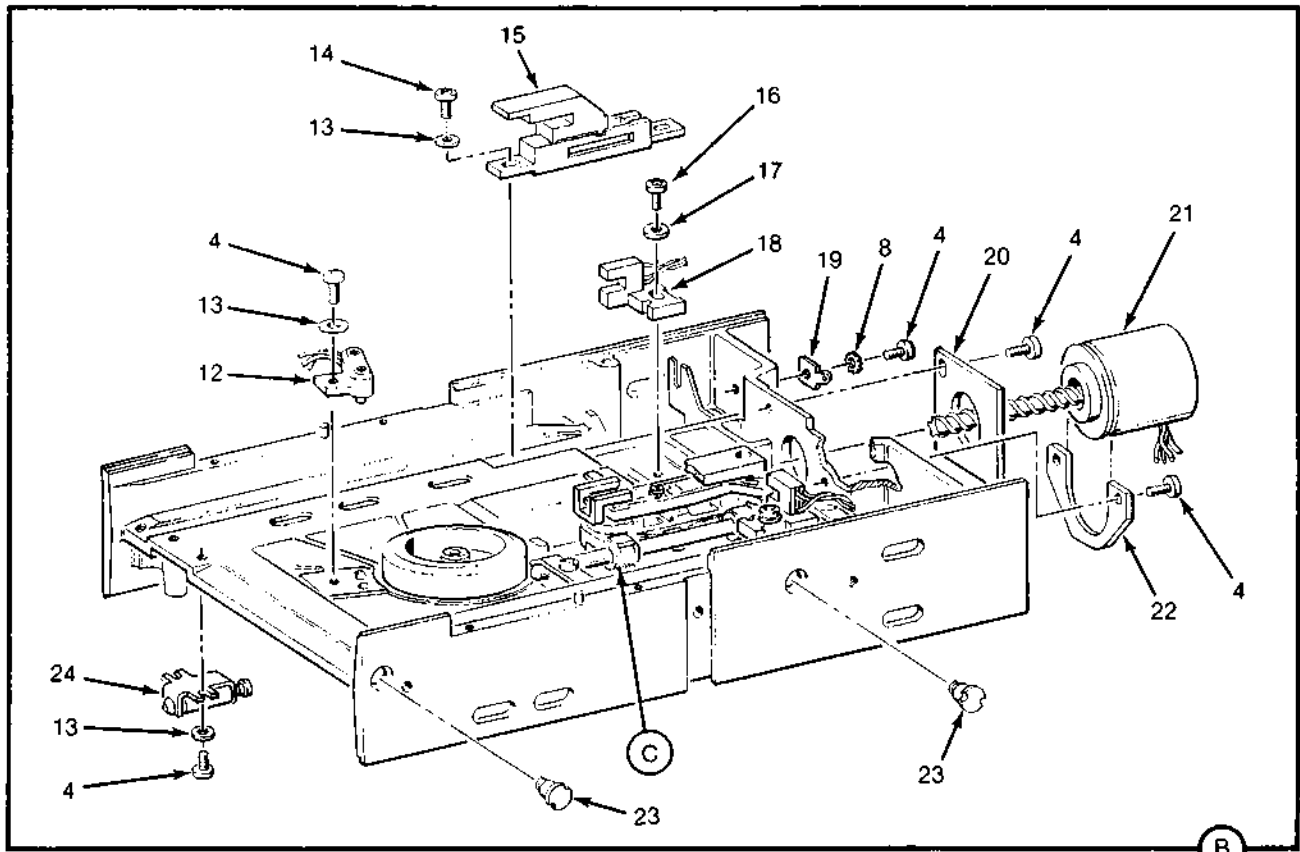


FIGURE 7-1. SA810/860 DISKETTE DRIVE, EXPLODED VIEW (SHEET 1 OF 3)

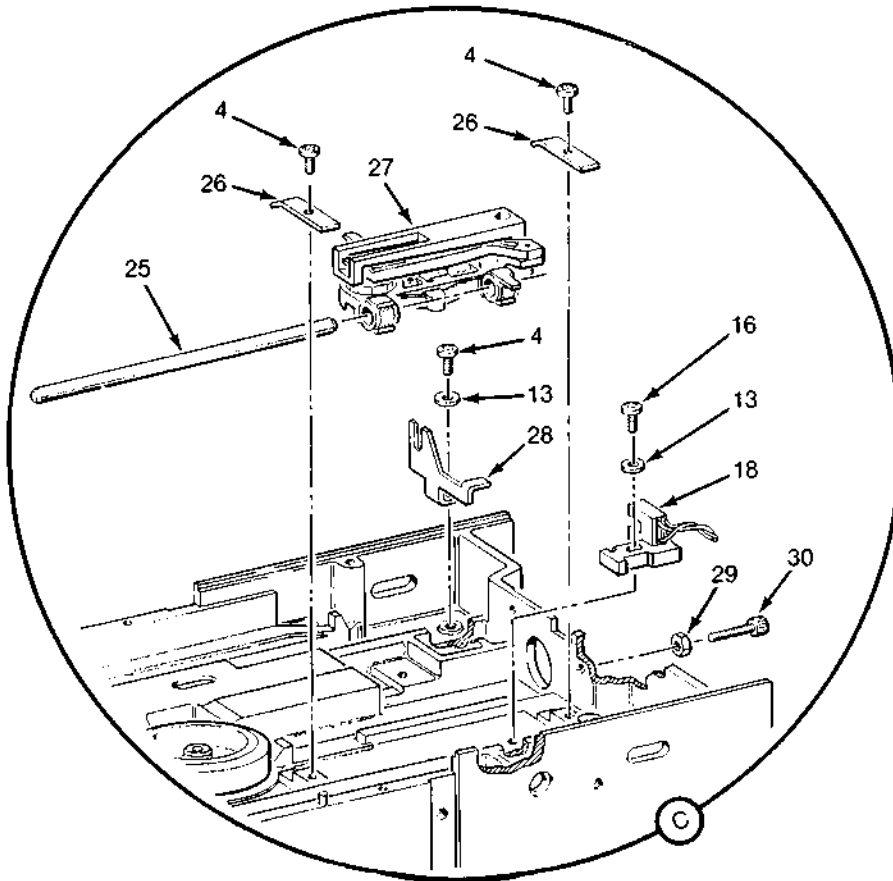
39231-26/1

**SA810/860 DISKETTE DRIVE ASSEMBLY**

<b>FIGURE &amp; REF NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY PER ASM</b>
1-	51370	SA810/860 DISKETTE DRIVE	
Ref	12175	• SCREW, Machined, 4-40 × 0.188 in.	4
1	51358	• TOP SHIELD	1
2	25227	• PCB ASSEMBLY (see figure 7-4 )	1
3	25247	• PCB ASSEMBLY (see figure 7-5 )	1
	25249	• PCB ASSEMBLY (see figure 7-6 )	1
4	12087	• SCREW, Phillips Pan Head, 6-32 × 0.25 in.	6
5	51357	• BOTTOM SHIELD	1
6	51360	• TOP PLATE ASSEMBLY (see figure 7-2 )	1
7	12107	• SCREW, Phillips Pan Head, 4-40 × 0.31 in.	4
8	12501	• EXT. TOOTH LOCK WASHER, #6	2
9	51380	• FRONT PLATE ASSEMBLY	1
10	51523	• KNOB, Painted	1
11	12129	• SCREW, Set, 4-40 × 0.188 in., Black Oxide Finish	2



(B)

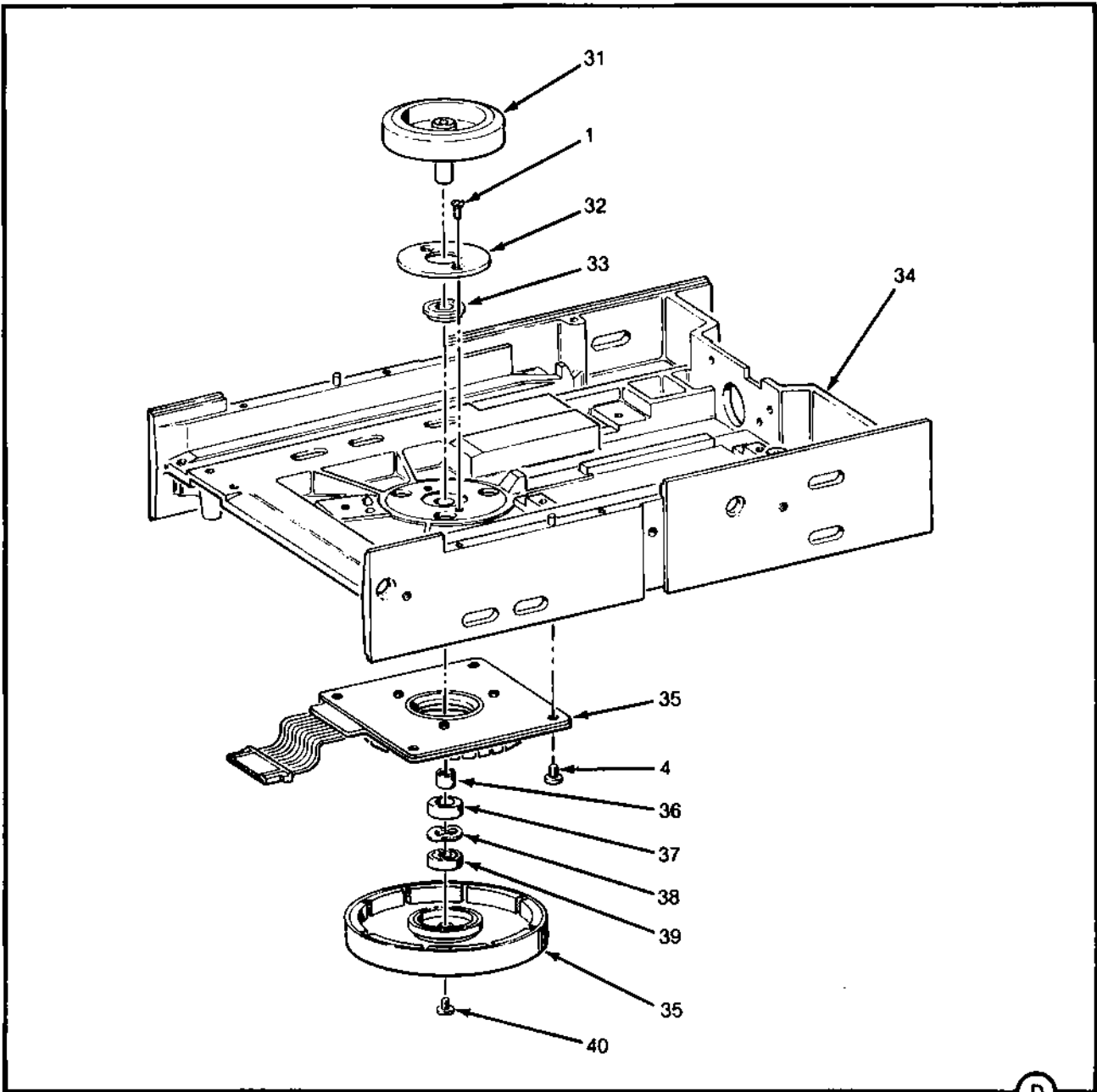


39231-26/2

FIGURE 7-1. SA810/860 DISKETTE DRIVE, EXPLODED VIEW (SHEET 2 OF 3)

**SA810/860 DISKETTE DRIVE ASSEMBLY (CONT.)**

<b>FIGURE &amp; REF NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY PER ASM</b>
1-			
12	51499	• INDEX EMITTER ASSEMBLY	1
13	12523	• WASHER, Flat, #6	3
14	12102	• SCREW, Phillips Pan Head, 6-32 x 0.31 in.	2
15	51369	• DISK EJECT ASSEMBLY	1
16	12088	• SCREW, Phillips Pan Head, 6-32 x 0.375 in.	3
17	10013	• WASHER, Flat	3
18	51498	• TRK 00 WRITE PROTECT SENSOR ASM.	2
19	15663	• TAB, Faston	1
20	54625	• ADJUSTMENT PLATE	1
21	51501	• STEPPER MOTOR ASSEMBLY	1
22	51244	• STEPPER MOTOR CLAMP	1
23	51407	• BIAS SPRING BUTTON ASSEMBLY	2
24	51500	• DOOR LOCK SOLENOID ASSEMBLY	1
25	54433	• GUIDE ROD	1
26	51246	• GUIDE ROD CLAMP	2
27	51280	• ACTUATOR ASSEMBLY, 860	1
	51333	• ACTUATOR ASSEMBLY, 810	
28	51413	• CABLE ROUTING CLAMP	1
29	10023	• NUT	1
30	11934	• SCREW, Hex Socket Head Cap, 4-40 x 0.75 in.	1



D

FIGURE 7-1. SA810/860 DISKETTE DRIVE, EXPLODED VIEW (SHEET 3 OF 3)

39231-26/3

**SA810/860 DISKETTE DRIVE ASSEMBLY (CONT.)**

<b>FIGURE &amp; REF NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY PER ASM</b>
1-			
31	51265	• SPINDLE, Machined	1
32	51243	• RING	1
33	10816	• BEARING, Flanged	1
34	51520	• BASE, Machined	1
35	51364	• MOTOR, Spindle	1
36	51282	• SPACER, Bearing	1
37	51288	• SPACER, Spring	1
38	12537	• SPRING	1
39	10817	• BEARING	1
40	12123	• SCREW, Machined, Self-Locking Pan Head Phillips, 6-32 x 0.25 in.	1



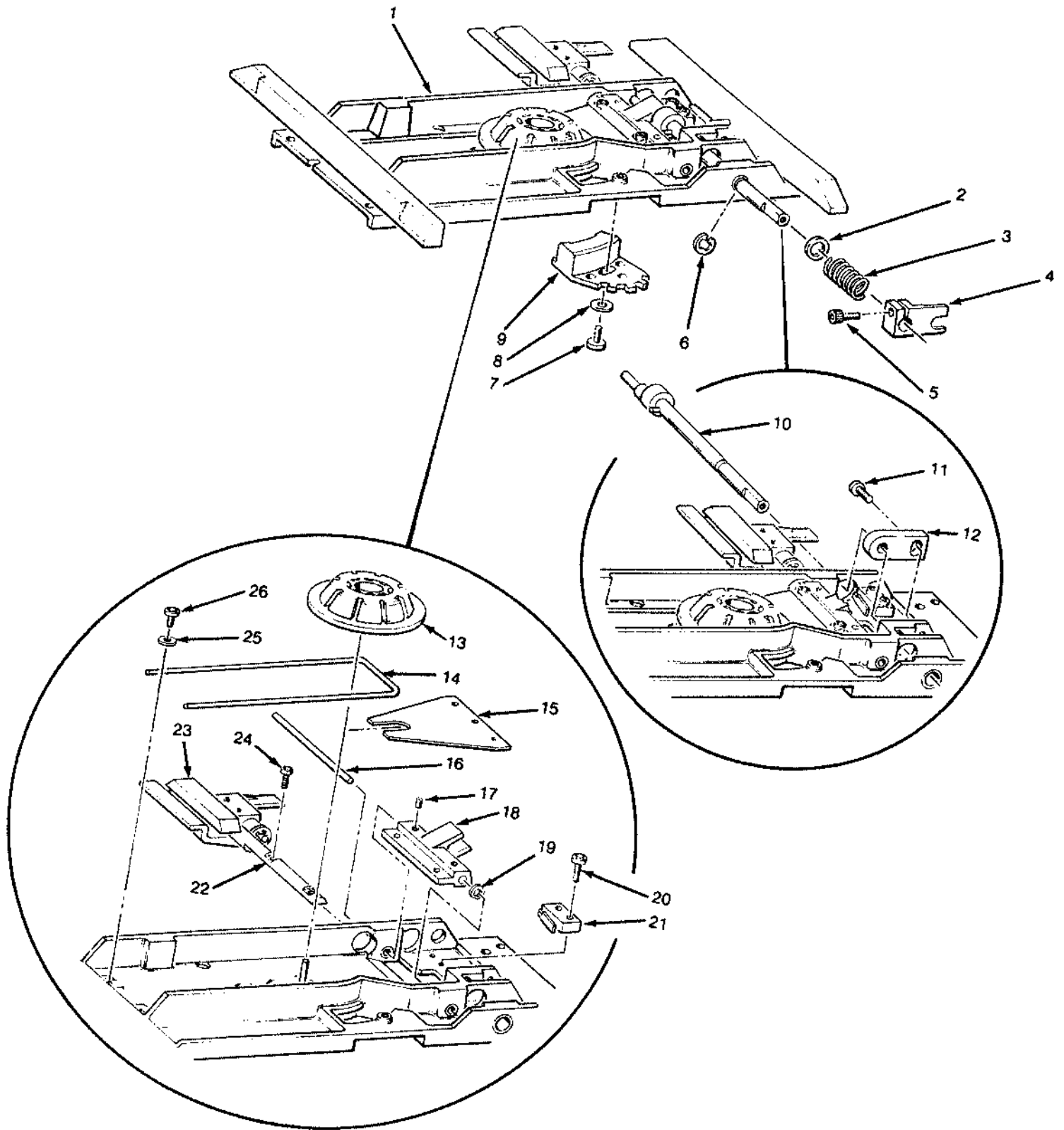
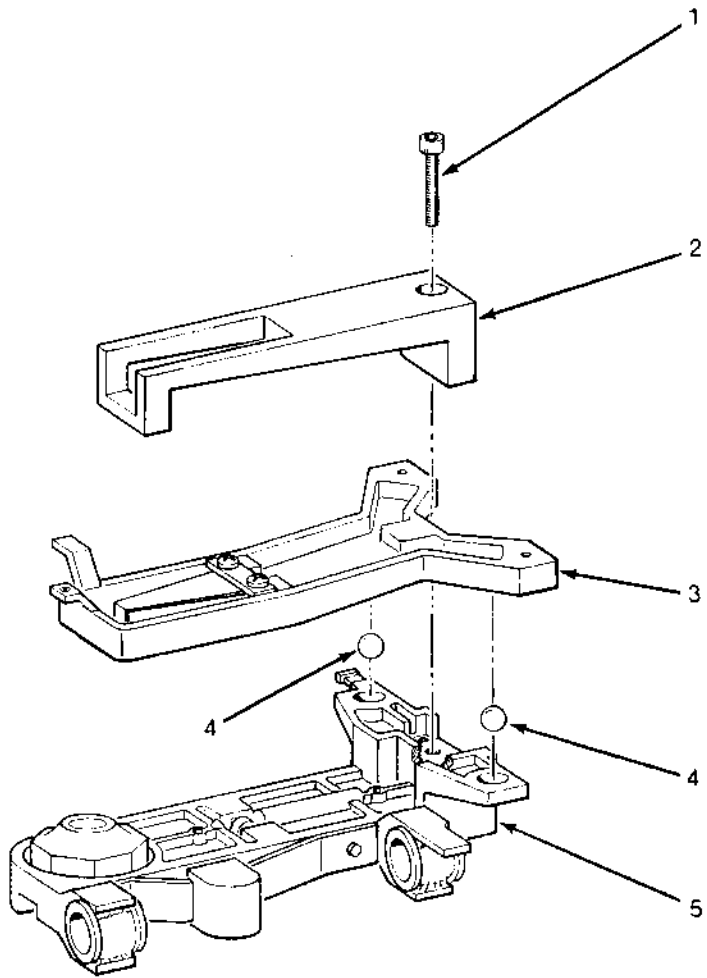


FIGURE 7-2. TOP PLATE ASSEMBLY, EXPLODED VIEW

39231-27

**TOP PLATE ASSEMBLY**

<b>FIGURE &amp; REF NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY PER ASM</b>
2-			
Ref	51360	TOP PLATE ASSEMBLY	1
1	51262	• TOP PLATE MACHINED ASSEMBLY	1
2	51341	• SHIM	1
3	51342	• SPRING, Shaft	1
4	51242	• STOP, Door Lock	1
5	12126	• SCREW, Machined, 4-40 × 0.312 in.	1
6	11305	• FASTENER, Ring-Retaining	1
7	12088	• SCREW, 6-32 × 0.375 in.	1
8	12523	• WASHER, Flat #6	1
9	51497	• INDEX DETECTOR ASSEMBLY	1
10	51363	• CAM SHAFT ASSEMBLY	1
11	12102	• SCREW, Machined, 6-32 × 0.312 in.	1
12	51567	• STOP, Shaft	1
13	51361	• COLLET ASSEMBLY	1
14	51292	• SPRING, Return	1
15	51249	• SPRING, Leaf	1
16	51343	• SHAFT, Clamp	1
17	12043	• SCREW, Set, 4-40 × 0.125 in.	2
18	51266	• LEVER	1
19	51566	• SPRING, Side Load	1
20	12118	• SCREW, Machined, 2-56 × 0.375 in.	2
21	51596	• DOOR CLOSED SWITCH ASSEMBLY	1
22	51296	• BAR, Lever	1
23	51509	• BAIL ASSEMBLY	1
24	12071	• SCREW, Machined, 4-40 × 0.250 in.	2
25	10013	• WASHER, Flat, #6	2
26	12087	• SCREW, Machined, 6-32 × 0.250 in.	2



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**FIGURE 7.3. ACTUATOR ASSEMBLY, EXPLODED VIEW**

**ACTUATOR ASSEMBLY**

<b>FIGURE &amp; REF NUMBER</b>	<b>PART NUMBER</b>	<b>DESCRIPTION</b>	<b>QTY PER ASM</b>
3-			
Ref	51280	SA860 ACTUATOR ASSEMBLY	
	51333	SA810 ACTUATOR ASSEMBLY	
1	11934	• SCREW, Hex Socket Head Cap, 4-40 × 0.75 in.	1
2	51351	• DOWN STOP ASSEMBLY	1
3	54646	• 860 ARM ASSEMBLY, Side 1	1
	51359	• 810 ARM ASSEMBLY, Side 1	
4	10814	• BEARING BALL	2
5	51353	• CARRIAGE ASSEMBLY	1

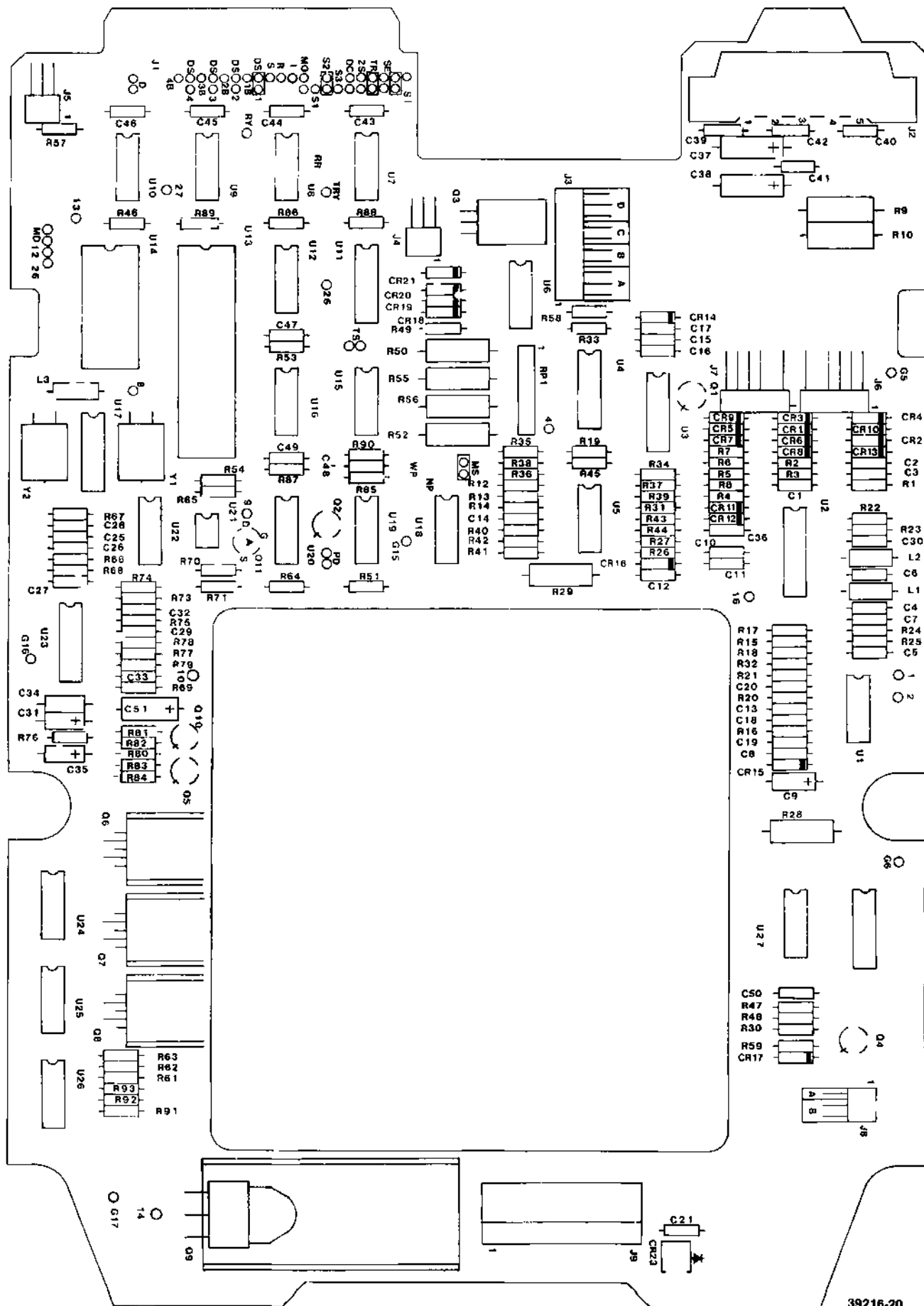


FIGURE 7-4. PCB (P/N 25227)

39216-20

**PCB ASSEMBLY 25227**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
4-			
Ref	25227	PCB	1
Ref	25247	PCB	1
C-1	15075	CAP., 0.022 $\mu$ F, 50 V, 10%	1
C-2,4,6-8,12,13, 15,16,18,19,21, 25,26,28,33,36, 40-50	15080	CAP., 0.1 $\mu$ F, 50 V, +80-20%	29
C-5	15109	CAP., 560 pF, 50 V, 5%	1
C-9,31,53	15121	CAP., 4.7 $\mu$ F, 35 V, 20%	3
C-10,11	15096	CAP., 150 pF, 50 V, 5%	2
C-14,27,32,39	15073	CAP., 0.01 $\mu$ F, 50 V, 10%	4
C-17	15069	CAP., 0.001 $\mu$ F, 50 V, 10%	1
C-20	15123	CAP., 91 pF, 50 V, 5%	1
C-22,23,24	15019	CAP., 0.0027 $\mu$ F, 200 V, 10%	3
C-29	15124	CAP., 0.033 $\mu$ F, 50 V, 5%	1
C-30	15054	CAP., 100 pF, 50 V, 5%	1
C-34	15100	CAP., 0.047 $\mu$ F, 25 V, 10%	1
C-35	10088	CAP., 1 $\mu$ F, 35 V, 10%	1
C-37,38,51	15125	CAP., 4.7 $\mu$ F, 50 V, 20%	3
CR-1-14	10062	DIODE, 1N4148	14
CR-15	15922	DIODE, 1N5242B, Zener, 12 V, 5%	1
CR-16	15902	DIODE, 1N5231B, Zener, 5.1 V, 5%	1
CR-17-21	15900	DIODE, 1N4003	5
CR-23	15936	LED	1
J-2	17788	CONNECTOR, 5 Pos., DC	1
J-3	19177	CONNECTOR, 16 Pos.	1
J-4,5,8	17784	CONNECTOR, 6 Pos.	3
J-6	17790	CONNECTOR, 6 Pos.	1
J-7	17782	CONNECTOR, 6 Pos.	1
J-9	17787	CONNECTOR, 13 Pos.	1
L-1,2,3	10084	INDUCTOR, Shielded, 100 $\mu$ H	3
Q-1	17619	TRANSISTOR, MPS 2222A	1
Q-2,4,10	10059	TRANSISTOR, 2N2222A	3
Q-3	17623	TRANSISTOR, Tip 32	1
Q-5	10060	TRANSISTOR, 2N2907	1
Q-6,7,8	12769	TRANSISTOR, SG3635P	3
Q-9	17615	TRANSISTOR, Tip 33	1
Q-11	17629	TRANSISTOR, Siliconix 174	1
R-1,47,57,58	16777	RES, 150 $\Omega$ , 1/4 w, 5%	4
R-2,3,78	10131	RES, 22 k, 1/4 w, 5%	3
R-4,42,46,53, 64,89,90	10111	RES, 4.7 k, 1/4 w, 5%	7
R-5	10115	RES, 6.8 k, 1/4 w, 5%	1
R-6,7,16	10110	RES, 2.4 k, 1/4 w, 5%	3
R-8,20,68	16722	RES, 100 k, 1/4 w, 5%	3
R-9,10	16989	RES, 300 $\Omega$ , 3 w, 5%	2
R-12	16902	RES, 1.37 k, 1/8 w, 1%	1

**PCB ASSEMBLY 25227 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
R-13	16701	RES, 4.99 k, 1/8 w, 1%	1
R-14	16979	RES, 17.4 k, 1/8 w, 1%	1
R-15,34,35,38,39, 49,61-63,79,80	10108	RES, 1 k, 1/4 w, 5%	11
R-17,18	16831	RES, 200, 1/4 w, 5%	2
R-19	16914	RES, 13.7 k, 1/8 w, 1%	1
R-21,32,66,70, 71,94	10113	RES, 10 k, 1/4 w, 5%	6
R-22,23,82	16749	RES, 390 Ω, 1/4 w, 5%	3
R-24,25,36,44,45	10109	RES, 2 k, 1/4 w, 5%	5
R-26	16915	RES, 9.53 k, 1/8 w, 1%	1
R-27	16818	RES, 2.15 k, 1/8 w, 1%	1
R-28	16987	RES, 270 Ω, 1 w, 5%	1
R-29	16926	RES, 220 Ω, 3 w, 1%	1
R-30,59	16839	RES, 130 Ω, 1/4 w, 5%	2
R-31	16980	RES, 750 Ω, 1/8 w, 1%	1
R-33	16866	RES, 7.50 k, 1/8 w, 1%	1
R-37	16755	RES, 750 Ω, 1/4 w, 5%	1
R-40	17058	RES, 2.32 k, 1/8 w, 1%	1
R-41	16922	RES, 7.15 k, 1/8 w, 1%	1
R-43	16928	RES, 10.7 k, 1/8 w, 1%	1
R-48,51	16824	RES, 470 Ω, 1/4 w, 5%	2
R-50	16984	RES, 560 Ω, 3 w, 5%	1
R-52	16988	RES, 68 Ω, 1 w, 5%	1
R-54	16822	RES, 1 M Ω, 1/4 w, 5%	1
R-55,56	16981	RES, 90 Ω, 3 w, 5%	2
R-65	10118	RES, 2.2 k, 1/4 w, 5%	1
R-67	17041	RES, 150 k, 1/4 w, 5%	1
R-69	16762	RES, 1.00 k, 1/8 w, 1%	1
R-73	17072	RES, 110 k, 1/8 w, 1%	1
R-74	16873	RES, 21.5 k, 1/8 w, 1%	1
R-75	16769	RES, 15 k, 1/4 w, 5%	1
R-76	10107	RES, 560 Ω, 1/4 w, 5%	1
R-77	17003	RES, 100 k, 1/8 w, 1%	1
R-81	16787	RES, 24 k, 1/4 w, 5%	1
R-83	16768	RES, 5.1 k, 1/4 w, 5%	1
R-84	17061	RES, 8.25 k, 1/8 w, 1%	1
R-85,86	10103	RES, 220 Ω, 1/4 w, 5%	2
R-87,88	16838	RES, 330 Ω, 1/4 w, 5%	2
R-91-93	16834	RES, 200 k, 1/4 w, 5%	3
R-95	16728	POT., 100 Ω, 3/4 w, 10%	1
R-96	17071	RES, 22 Ω, 1/4 w, 5%	1
RP-1	16978	RES, 4.7 k, Sip, 8 Pin	1
U-1	16244	IC, NE592N	1
U-2	16278	IC, Read LSI	1
U-3	16270	IC, Write LSI	1
U-4	12674	IC, CA3083	1
U-5	12640	IC, TPQ3906	1
U-6,20,22	16274	IC, 74LS02	1
U-7,8,10,19	16207	IC, 7438	4
U-9	16837	RES, 220/330, Terminator, Dip	1
U-11	12772	IC, Sprague-ULN 2065B	1

**PCB ASSEMBLY 25227 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
U-12	16201	IC, 7404	1
U-13	16271	IC, Drive Logic	1
U-14	51420	IC, Gate Array	1
U-15,24	16273	IC, 74LS00	3
U-16	16258	IC, 7414	1
U-17	12770	IC, 74LS321	1
U-18	16233	IC, 7408	1
U-21	12610	IC, 75462	1
U-23	12771	IC, NEC-UPC 1043C	1
U-25	12656	IC, 74LS32	1
U-26	16227	IC, LM339	1
U-27	16274	IC, 74LS02	1
W/U-9	15672	SOCKET, 14 Pin	1
W/U-13	15691	SOCKET, 40 Pin	1
W/U-14	17789	SOCKET, 24 Pin	1
Y-1,2	15702	CRYSTAL, 5 MHz	2



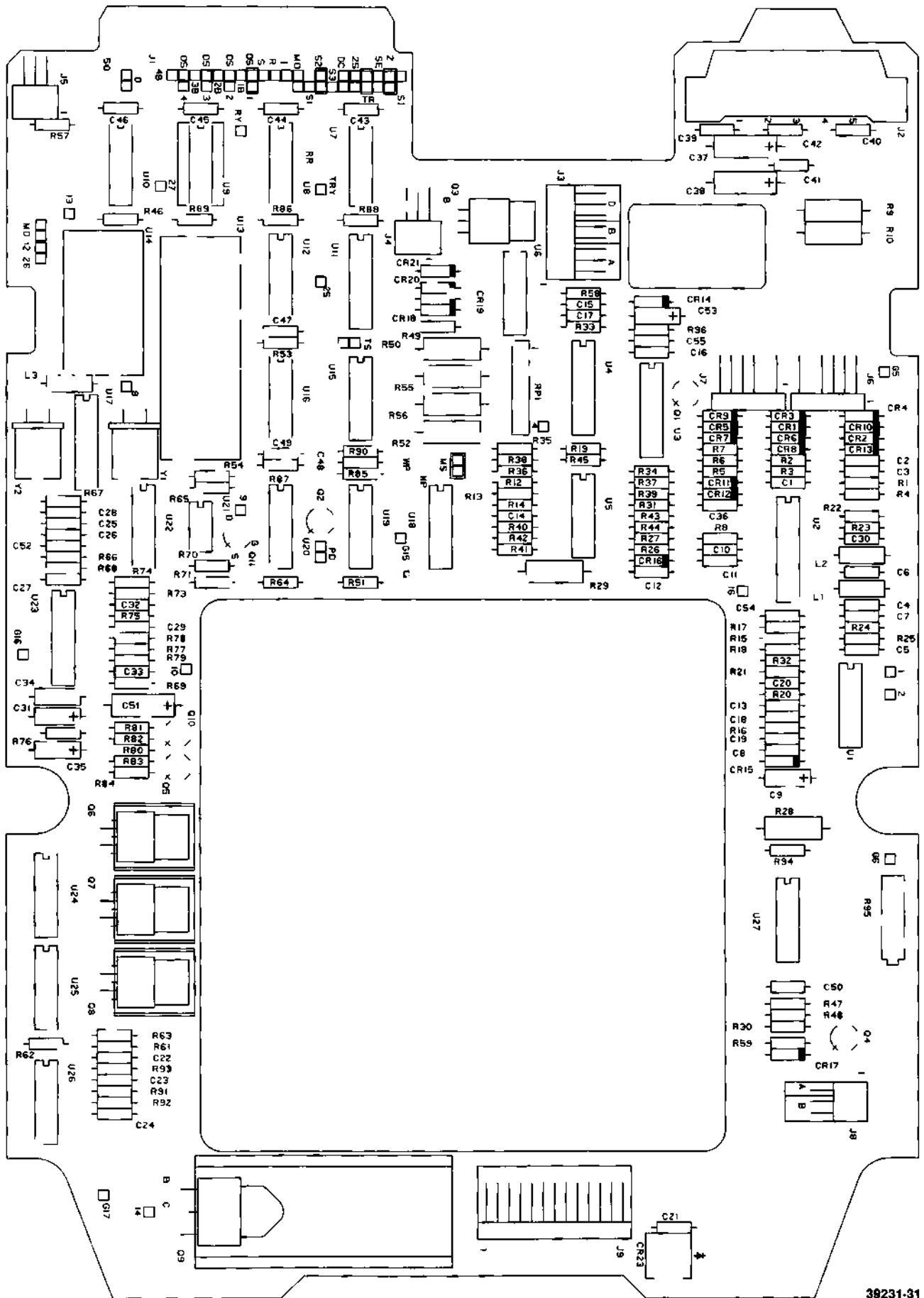


FIGURE 7-5. PCB (P/N 25247)

39231-31

**PCB ASSEMBLY 25247**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
5-			
Ref	25227	PCB	1
Ref	25247	PCB	1
C-1	15075	CAP., 0.022 $\mu$ F, 50 V, 10%	1
C-2,4,6-8,12,13, 15,16,18,19,21, 25,26,28,33,36, 40-50	15080	CAP., 0.1 $\mu$ F, 50 V, +80-20%	29
C-5	15109	CAP., 560 pF, 50 V, 5%	1
C-9,31,53	15121	CAP., 4.7 $\mu$ F, 35 V, 20%	3
C-10,11	15096	CAP., 150 pF, 50 V, 5%	2
C-14,27,32,39	15073	CAP., 0.01 $\mu$ F, 50 V, 10%	4
C-17	15069	CAP., 0.001 $\mu$ F, 50 V, 10%	1
C-20	15123	CAP., 91 pF, 50 V, 5%	1
C-22,23,24	15019	CAP., 0.0027 $\mu$ F, 200 V, 10%	3
C-29	15124	CAP., 0.033 $\mu$ F, 50 V, 5%	1
C-30	15054	CAP., 100 pF, 50 V, 5%	1
C-34	15100	CAP., 0.047 $\mu$ F, 25 V, 10%	1
C-35	10088	CAP., 1 $\mu$ F, 35 V, 10%	1
C-37,38,51	15125	CAP., 4.7 $\mu$ F, 50 V, 20%	3
C-52	15029	CAP., 0.047 $\mu$ F, 50 V, 10%	1
C-54	15128	CAP., 470 pF, 50 V, 5%	1
C-56	15115	CAP., 82 pF, 50 V, 5%	1
CR-1-14	10062	DIODE, 1N4148	14
CR-15	15922	DIODE, 1N5242B, Zener, 12 V, 5%	1
CR-16	15902	DIODE, 1N5231B, Zener, 5.1 V, 5%	1
CR-17-21	15900	DIODE, 1N4003	5
CR-23	15936	LED	1
J-2	17788	CONNECTOR, 5 Pos., DC	1
J-3	19177	CONNECTOR, 16 Pos.	1
J-4,5,8	17784	CONNECTOR, 6 Pos.	3
J-6	17790	CONNECTOR, 6 Pos.	1
J-7	17782	CONNECTOR, 6 Pos.	1
J-9	17787	CONNECTOR, 13 Pos.	1
L-1,2,3	10084	INDUCTOR, Shielded, 100 $\mu$ H	3
Q-1	17619	TRANSISTOR, MPS 2222A	1
Q-2,4,10	10059	TRANSISTOR, 2N2222A	3
Q-3	17623	TRANSISTOR, Tip 32	1
Q-5	10060	TRANSISTOR, 2N2907	1
Q-6,7,8	12769	TRANSISTOR, SG3635P	3
Q-9	17615	TRANSISTOR, Tip 33	1
Q-11	17629	TRANSISTOR, Siliconix 174	1
R-1,47,57,58	16777	RES, 150 $\Omega$ , 1/4 w, 5%	4
R-2,3,78	10131	RES, 22 k, 1/4 w, 5%	3
R-4,42,46,53, 64,89,90	10111	RES, 4.7 k, 1/4 w, 5%	7
R-5	10115	RES, 6.8 k, 1/4 w, 5%	1
R-6,7,16	10110	RES, 2.4 k, 1/4 w, 5%	3
R-8,20,68	16722	RES, 100 k, 1/4 w, 5%	3
R-9,10	16989	RES, 300 $\Omega$ , 3 w, 5%	2
R-12	16902	RES, 1.37 k, 1/8 w, 1%	1

**PCB ASSEMBLY 25247 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
R-13	16701	RES, 4.99 k, 1/8 w, 1%	1
R-14	16979	RES, 17.4 k, 1/8 w, 1%	1
R-15,34,35,38,39, 49,61-63,79,80	10108	RES, 1 k, 1/4 w, 5%	11
R-17,18	16831	RES, 200, 1/4 w, 5%	2
R-19	16914	RES, 13.7 k, 1/8 w, 1%	1
R-21,32,66,70, 71,94	10113	RES, 10 k, 1/4 w, 5%	6
R-22,23,82	16749	RES, 390 Ω, 1/4 w, 5%	3
R-24,25,36,44,45	10109	RES, 2 k, 1/4 w, 5%	5
R-26	16915	RES, 9.53 k, 1/8 w, 1%	1
R-27	16818	RES, 2.15 k, 1/8 w, 1%	1
R-28	16987	RES, 270 Ω, 1 w, 5%	1
R-29	16926	RES, 220 Ω, 3 w, 1%	1
R-30,59	16839	RES, 130 Ω, 1/4 w, 5%	2
R-31	16980	RES, 750 Ω, 1/8 w, 1%	1
R-33	16866	RES, 7.50 k, 1/8 w, 1%	1
R-37	16755	RES, 750 Ω, 1/4 w, 5%	1
R-40	17058	RES, 2.32 k, 1/8 w, 1%	1
R-41	16922	RES, 7.15 k, 1/8 w, 1%	1
R-43	16928	RES, 10.7 k, 1/8 w, 1%	1
R-48,51	16824	RES, 470 Ω, 1/4 w, 5%	2
R-50	16984	RES, 560 Ω, 3 w, 5%	1
R-52	16988	RES, 68 Ω, 1 w, 5%	1
R-54	16822	RES, 1 M Ω, 1/4 w, 5%	1
R-55,56	16981	RES, 90 Ω, 3 w, 5%	2
R-65	10118	RES, 2.2 k, 1/4 w, 5%	1
R-67	17041	RES, 150 k, 1/4 w, 5%	1
R-69	16762	RES, 1.00 k, 1/8 w, 1%	1
R-73	17072	RES, 110 k, 1/8 w, 1%	1
R-74	16873	RES, 21.5 k, 1/8 w, 1%	1
R-75	16769	RES, 15 k, 1/4 w, 5%	1
R-76	10107	RES, 560 Ω, 1/4 w, 5%	1
R-77	17003	RES, 100 k, 1/8 w, 1%	1
R-81	16787	RES, 24 k, 1/4 w, 5%	1
R-83	16768	RES, 5.1 k, 1/4 w, 5%	1
R-84	17061	RES, 8.25 k, 1/8 w, 1%	1
R-85,86	10103	RES, 220 Ω, 1/4 w, 5%	2
R-87,88	16828	RES, 330 Ω, 1/4 w, 5%	2
R-91-93	16834	RES, 200 k, 1/4 w, 5%	3
R-95	16728	POT., 100 Ω, 3/4 w, 10%	1
R-96	17071	RES, 22 Ω, 1/4 w, 5%	1
RP-1	16978	RES, 4.7 k, Sip, 8 Pin	1
U-1	16244	IC, NE592N	1
U-2	16278	IC, Read LSI	1
U-3	16270	IC, Write LSI	1
U-4	12674	IC, CA3083	1
U-5	12640	IC, TPQ3906	1
U-6,20,22	16274	IC, 74LS02	1
U-7,8,10,19	16207	IC, 7438	4
U-9	16837	RES, 220/330, Terminator, Dip	1
U-11	12772	IC, Sprague-ULN 2065B	1

**PCB ASSEMBLY 25247 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
U-12	16201	IC, 7404	1
U-13	16271	IC, Drive Logic	1
U-14	51420	IC, Gate Array	1
U-15,24	16273	IC, 74LS00	3
U-16	16258	IC, 7414	1
U-17	12770	IC, 74LS321	1
U-18	16233	IC, 7408	1
U-21	12610	IC, 75462	1
U-23	12771	IC, NEC-UPC 1043C	1
U-25	12656	IC, 74LS32	1
U-26	16227	IC, LM339	1
U-27	16274	IC, 74LS02	1
W/U-9	15672	SOCKET, 14 Pin	1
W/U-13	15691	SOCKET, 40 Pin	1
W/U-14	17789	SOCKET, 24 Pin	1
Y-1,2	15702	CRYSTAL, 5 MHz	2

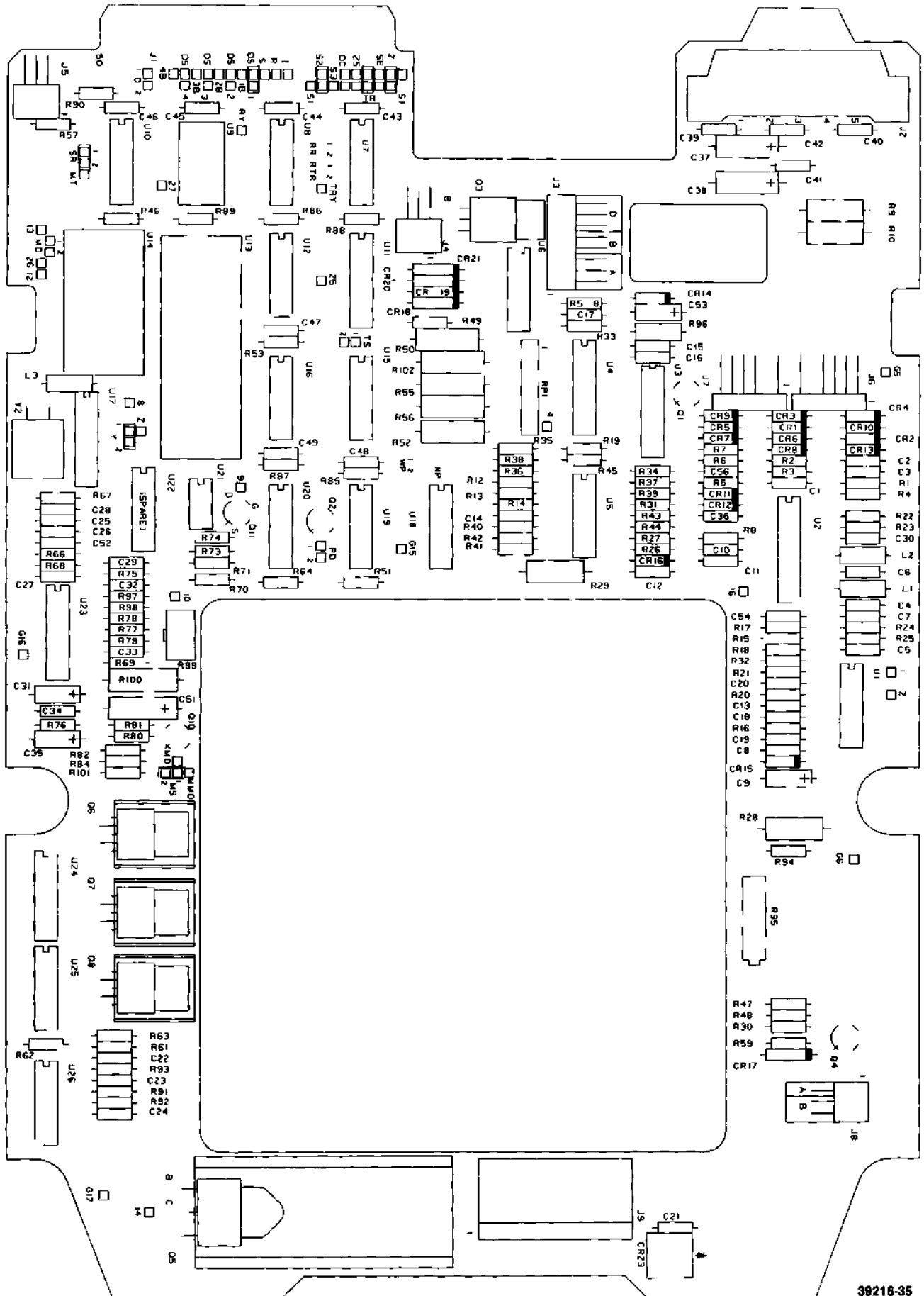


FIGURE 7-6. PCB (P/N 25249)

39216-35

## PCB ASSEMBLY 25249

Ref Des	Part Number	Description	Qty
6-			
Ref	25249	PCB	
C-1	15075	CAP., 0.022 $\mu$ F, 50 V, 10%	1
C-2,3,4,6,7,8,12, 13,15,16,18,19, 21,25,26,28,33, 36,40-49	15080	CAP., Cer, Axial Lead, 0.1 $\mu$ F, 50 V, +80-20%	28
C-5	15109	CAP., 560 pF, 50 V, 5%	1
C-9,31,53	15121	CAP., 4.7 $\mu$ F, 35 V, 20%	3
C-10,11	15096	CAP., 150 pF, 50 V, 5%	2
C-14,27,32,39	15073	CAP., 0.01 $\mu$ F, 50 V, 10%	4
C-17	15069	CAP., 0.001 $\mu$ F, 50 V, 10%	1
C-20	15123	CAP., 91 pF, 50 V, 5%	1
C-22-24	15071	CAP., 0.0027 $\mu$ F, 50 V, 10%	3
C-29	15124	CAP., 0.033 $\mu$ F, 50 V, 5%	1
C-30	15054	CAP., 100 pF, 50 V, 5%	1
C-34,52	15100	CAP., Low Temp. Coeff.	2
C-35	10088	CAP., 1 $\mu$ F, 35 V, 10%	1
C-37,38,51	15125	CAP., 4.7 $\mu$ F, 50 V, 20%	3
C-54	15128	CAP., 470 pF, 50 V, 10%	1
C-56	15115	CAP., 82 pF, 50 V, 5%	1
CR1-14	10062	DIODE, IN4148	14
CR-15	15922	DIODE, Zener, 1/2 w, 5%	1
C-16	15902	DIODE, Zener	1
CR-17-21	15900	DIODE, Silicone Rectifier	5
CR-23	15936	DIODE, Red LED	1
J-2	17788	CONNECTOR HEADER ASM, Right Angle	1
J-3	19177	CONNECTOR HEADER, 16 Pos.	1
J-4,J-5,J-8	17784	CONNECTOR HEADER, 6 Pos.	3
J-6	17790	CONNECTOR HEADER, 6 Pos.	1
J-7	17782	CONNECTOR HEADER, 6 Pos.	1
J-9	17787	CONNECTOR HEADER, 13 Pos.	1
L-1,2,3	10084	INDUCTOR, Shielded, 100 $\mu$ H	3
Q-1	17619	TRANSISTOR, NPN, Sig, PN2222A	1
Q-2,4,10	10059	TRANSISTOR, 2N2222A	3
Q-3	17623	TRANSISTOR, PNP, Power, Tip-32	1
Q-5	17624	TRANSISTOR, PNP, Power, Tip-34	1
Q-6,7,8	12769	I.C., 3635	3
Q-11	17629	P-Channel, JFET, J174	1
R-1,47,57,58,67	16777	RES, Fixed, 150 $\Omega$ , 1/4 w, 5%	4
R-2,3	10131	RES, Fixed, 22 k, 1/4 w, 5%	2
R-4,42,46,53, 64,89,90	10111	RES, Fixed, 4.7 k, 1/4 w, 5%	7
R-5	16889	RES, Fixed, 4.87 k, 1/8 w, 1%	1
R-6,7,16	10110	RES, Fixed, 2.4 k, 1/4 w, 5%	3
R-8,20,68,77,78	16722	RES, Fixed, 100 k, 1/4 w, 5%	5
R-9,10	16989	RES, Fixed, 300 $\Omega$ , 3 w, 5%	2
R-12	16902	RES, Fixed, 1.37 k, 1/8 w, 1%	1
R-13	16701	RES, Fixed, 4.99 k, 1/8 w, 1%	1
R-14	16979	RES, Fixed, 17.4 k, 1/8 w, 1%	1

**PCB ASSEMBLY 25249 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
R-15,34,35,38,39, 49,61,62,63, 69,79,80	10108	RES, Fixed, 1 k, 1/4 w, 5%	12
R-17,18	16831	RES, Fixed, 200 Ω, 1/4 w, 5%	2
R-19	16914	RES, Fixed, 13.7 k, 1/8 w, 1%	1
R-21,32,66,70,71, 94	10113	RES, Fixed, 10 k, 1/4 w, 5%	6
R-22,23	16749	RES, Fixed, 390 Ω, 1/4 w, 5%	2
R-24,25,36,44,45, 97	10109	RES, Fixed, 2 k, 1/4 w, 5%	6
R-26	16915	RES, Fixed, 9.53 k, 1/8 w, 1%	1
R-27	16818	RES, Fixed, 2.15 k, 1/8 w, 1%	1
R-28	16987	RES, Fixed, 270 Ω, 1 w, 5%	1
R-29	16926	RES, Fixed, 220 Ω, 3 w, 1%	1
R-30,59	16839	RES, Fixed, 130 Ω, 1/4 w, 5%	2
R-31	16980	RES, Fixed, 750 Ω, 1/8 w, 1%	1
R-33	16866	RES, Fixed, 7.50 k, 1/8 w, 1%	1
R-37	16755	RES, Fixed, 750 Ω, 1/4 w, 5%	1
R-40	17058	RES, Fixed, 2.32 k, 1/8 w, 1%	1
R-41	16922	RES, Fixed, 7.15 k, 1/8 w, 1%	1
R-43	16928	RES, Fixed, 10.7 k, 1/8 w, 1%	1
R-48,51	16824	RES, Fixed, 470 Ω, 1/4 w, 5%	2
R-50,100	16984	RES, Fixed, 560 Ω, 3 w, 5%	2
R-52	16988	RES, Fixed, 68 Ω, 1 w, 5%	1
R-55,56,102	17079	RES, Fixed, 130 Ω, 3 w, 5%	3
R-65	10118	RES, Fixed, 2.2 k, 1/4 w, 5%	1
R-73	17072	RES, Fixed, 110 k, 1/8 w, 1%	1
R-74	16873	RES, Fixed, 21.5 k, 1/8 w, 1%	1
R-75	16769	RES, Fixed, 15 k, 1/4 w, 5%	1
R-76	10107	RES, Fixed, 560 Ω, 1/4 w, 5%	1
R-81	10106	RES, Fixed, 510 Ω, 1/4 w, 5%	1
R-82	17015	RES, Fixed, 27 Ω, 1/4 w, 5%	1
R-84	17061	RES, Fixed, 8.25 k, 1/8 w, 1%	1
R-85,86	10103	RES, Fixed, 220 Ω, 1/4 w, 5%	1
R-87,88	16838	RES, Fixed, 330 Ω, 1/4 w, 5%	2
R-91,92,93	16834	RES, Fixed, 200 k, 1/4 w, 5%	3
R-95	16728	POT., Cermet, 100 Ω, 3/4 w, ±10%	1
R-96	16932	RES, Fixed, 22 Ω, 1/2 w, 5%	1
R-98	17076	RES, Fixed, 62 k, 1/4 w, 5%	1
R-99	16885	POT., 2 k, 1/2 w, ±10%	1
R-101	16891	RES, Fixed, 51 Ω, 1/4 w, 5%	1
RP-1	16978	NETWORK RESISTOR ARRAY, Sip, 4.7 k	1
U-1	16244	IC, Amplifier, NE592N	1
U-2	16278	IC, Read Amplifier	1
U-3	16270	IC, Write Channel	1
U-4	12674	IC, Transistor Array	1
U-5	12640	IC, Transistor (Quad, PNP)	1
U-6,18	16233	IC, 7408	1
U-7,8,10,19	16207	IC, 7438	4
U-9	16837	RES, Pack, 220 Ω/330 Ω	1
U-11	12772	IC, 2065	1
U-12	16201	IC, 7404	1
U-13	16271	IC, Drive Logic	1
U-14	51420	IC, Drive Logic	1
U-15,24	16273	IC, 74LS00	2

**PCB ASSEMBLY 25249 (CONT.)**

<b>Ref Des</b>	<b>Part Number</b>	<b>Description</b>	<b>Qty</b>
U-16	16265	IC, 7414	1
U-17	12770	IC, 74LS321	1
U-20	16203	IC, 7474	1
U-21	12610	IC, Peripheral Driver, 75462	1
U-23	12771	IC, 1043	1
U-25	12656	IC, 74LS32	1
U-26	16227	QUAD VOLTAGE COMPARATOR	1
W/U-9	15672	SOCKET, IC (Dip), 14 Pin	1
W/U-13	15691	SOCKET, IC (Dip), 40 Pin	1
W/U-14	17789	SOCKET, IC (Dip), 24 Pin	1



TABLE 7-1. PART NUMBER TO FIGURE REFERENCE CROSS REFERENCE

Part Number	Figure Reference
10013	1-17 2-25
10023	1-29
10059	4-Q2 5-Q2 6-Q2
10060	4-Q5
10062	4-CR1 5-CR1 6-CR1
10084	4-L1 5-L1 6-L1
10088	4-C35 5-C35 6-C35
10103	4-R85 5-R85 6-R85
10106	5-R81 6-R81
10107	4-R76 5-R76 6-R76
10108	4-R15 5-R15 6-R15
10109	4-R24 5-R24 6-R24
10110	4-R6 5-R6 6-R6
10111	4-R4 5-R4 6-R4
10113	4-R21 5-R21 6-R21
10115	4-R5
10118	4-R65 5-R65 6-R65
10131	4-R2 5-R2 6-R2
10814	3-4
10816	1-33
10817	1-39
11305	2-6
11934	3-1
12043	2-17
12071	2-24

Part Number	Figure Reference
12087	1-4 2-26
12088	1-16 2-7
12102	1-14 2-11
12107	2-5
12118	2-20
12123	1-40
12126	2-5
12129	1-11
12175	1-1
12501	1-9
12523	1-13 2-8
12537	1-38
12610	4-U21 5-U21 6-U21
12640	4-U5 5-U5 6-U5
12656	4-U25 5-U25 6-U25
12674	4-U4 5-U4 6-U4
12769	4-Q6 5-Q6 6-Q6
12770	4-U17 5-U17 6-U17
12771	4-U23 5-U23 6-U23
12772	4-U11 5-U11 6-U11
15019	4-C22
15029	5-C52
15054	4-C30 5-C30 6-C30
15069	4-C17 5-C17 6-C17
15071	5-C22
15073	6-C22 4-C14 5-C14 6-C14

Part Number	Figure Reference
15075	4-C1 5-C1 6-C1
15080	4-C2 5-C2 6-C2
15096	4-C10 5-C10 6-C10
15100	4-C34 5-C34 6-C34
15109	4-C5
15115	5-C56 6-C56
15121	4-C9 5-C9 6-C9
15123	4-C20 5-C20 6-C20
15124	4-C22 5-C22 6-C22
15125	4-C37 5-C37 6-C37
15128	5-C54 6-C54
15663	1-19
15672	4-W/U9 5-W/U9 6-W/U9
15691	4-W/U13 5-W/U13 6-W/U13
15702	4-Y1
15900	4-CR17
15902	4-CR16 5-CR16 6-CR16
15922	4-CR15 5-CR15 6-CR15
15936	4-CR23 5-CR23 6-CR23
16201	4-U12 5-U12 6-U12
16203	5-U20 6-U20

TABLE 7-1. PART NUMBER TO FIGURE REFERENCE CROSS REFERENCE (CONT.)

Part Number	Figure Reference
16207	4-U7 5-U7 6-U7
16233	4-U18
16244	4-U1 5-U1 6-U1
16227	4-U26 5-U26 6-U26
16258	U-16
16265	5-U16 6-U16
16270	4-U3 5-U3 6-U3
16271	4-U13 5-U13 6-U13
16273	4-U15 5-U15 6-U15
16274	4-U27 5-U6
16278	4-U2 5-U2 6-U2
16701	4-R13 5-R13 6-R13
16722	4-R8 5-R8 6-R8
16728	4-R95 5-R95 6-R95
16749	4-R22 5-R22 6-R22
16755	4-R37 5-R37 6-R37
16762	4-R69
16768	4-R83
16769	4-R75 5-R75 6-R75
16777	4-R1 5-R1 6-R1
16787	4-R81

Part Number	Figure Reference
16818	4-R27 5-R27 6-R27
16822	4-R54
16824	4-R48 5-R48
16828	5-R87 6-R48
16831	4-R17 5-R17 6-R17
16834	4-R91 5-R91 6-R91
16837	4-U9 5-U9 6-U9
16838	4-R87
16839	4-R30 5-R30 6-R30
16866	4-R33 5-R33 6-R33
16873	4-R74 5-R74 6-R74
16885	5-R99 6-R99
16889	5-R5 6-R75
16891	5-R101 6-R101
16902	4-R12 5-R12 6-R12
16914	4-R19 5-R19 6-R19
16915	4-R26 5-R26 6-R26
16922	4-R41 5-R41 6-R41
16926	4-R29 5-R29 6-R29
16928	4-R43 5-R43 6-R43
16932	5-R96 6-R96

Part Number	Figure Reference
16978	4-RP1 5-RP1 6-RP1
16979	4-R14 5-R14 6-R14
16980	4-R31 5-R31 6-R31
16981	4-R55
16984	4-R50 5-R50 6-R50
16987	4-R28 5-R28 6-R28
16988	4-R52 5-R52 6-R52
16989	4-R9 5-R9 6-R9
17003	4-R77
17015	5-R82 6-R82
17041	4-R67
17058	4-R40 5-R40 6-R40
17061	4-R84 5-R84 6-R84
17071	4-R96
17072	4-R73 5-R73 6-R73
17076	5-R98 6-R98
17079	5-R55 6-R55
17615	4-Q9
17619	4-Q1
17623	4-Q3
17624	5-Q5 6-Q5
17629	4-Q11 5-Q11 6-Q11
17782	4-J7 5-J7 6-J7

TABLE 7-1. PART NUMBER TO FIGURE REFERENCE CROSS REFERENCE (CONT.)

Part Number	Figure Reference
17784	4-J4
	5-J4
	6-J4
17787	4-J9
	5-J9
	6-J9
17788	4-J2
	5-J2
	6-J2
17789	4-W/U14
17790	4-J6
	5-J6
	6-J6
19177	4-J3
	5-J3
	6-J3
25227	1-3
	4-Ref
25247	5-Ref
25249	1-3
	6-Ref
51242	2-4
51243	1-32
51244	1-22
51246	1-26
51249	2-15
51262	2-1
51265	1-31
51266	2-18
51280	1-27
	3-Ref
51282	1-36
51288	1-37
51292	2-14
51296	2-22
51341	2-2
51342	2-3
51343	2-16
51351	3-2
51353	3-5
51357	1-5
51358	1-2
51359	3-3
51360	1-6
	2-Ref
51361	2-13
51363	2-10
51364	1-35
	1-41
51369	1-15
51370	1-Ref
51380	1-9
51407	1-23

Part Number	Figure Reference
51413	1-28
51420	4-U14
	5-U14
	6-U14
51497	2-9
51498	1-18
51499	1-12
51500	1-24
51501	1-21
51509	2-23
51520	1-34
51523	1-10
51566	2-19
51567	2-12
51596	2-21
54433	1-25
54625	1-20
54646	3-3

Part Number	Figure Reference
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## 7.4 RECOMMENDED SPARE PARTS STOCKING GUIDE

The spare parts stocking guide is broken down into three levels. These levels are: Site or Field Support Engineer (level 1), Branch Office (level 2), and Depot or Headquarters (level 3). The quantities listed assume that the Site is replenished by the Branch immediately and the Branch replenished by the Depot within 30 days.

The inventories that the levels can maintain are:

Site	1 to 20 machines
Branch	1 to 100 machines
Depot	
Depot only parts	Unlimited
Branch replenishment	Same as Branch ratio

The calculated failure rates for major parts are as shown in table 7-2.

Table 7-3 shows the spare parts required to support the SA810/860 in the field.

**TABLE 7-2. CALCULATED FAILURE RATES**

PART NUMBER	DESCRIPTION	FAILURE RATE FAILURES/UNIT/MONTH
25247	PCB	0.023
51364	DRIVE MOTOR	0.005
51353	HEAD CARRIAGE ASSEMBLY	0.010

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**TABLE 7-3. SPARE PARTS STOCKING GUIDE**

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT*
10814	BEARING, Ball			2
10816	BEARING, Flanged	1	1	1
10817	BEARING	1	1	1
12537	SPRING			1
25227	PCB	1	4	4
25247	PCB	1	4	4
25249	PCB	1	4	4
51242	STOP, Door Lock		1	1
51243	RING			1
51244	STEPPER MOTOR CLAMP			1

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TABLE 7-3. SPARE PARTS STOCKING GUIDE (CONT.)

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT*
51246	GUIDE ROD CLAMP			1
51249	SPRING, Leaf			1
51262	TOP PLATE MACHINED ASSEMBLY			1
51265	SPINDLE, Machined			1
51266	LEVER			1
51282	SPACER, Bearing			1
51288	SPACER, Spring			1
51292	SPRING, Return			1
51296	BAR, Lever			1
51341	SHIM			1
51342	SPRING, Shaft			1
51343	SHAFT, Clamp			1
51351	DOWN STOP ASSEMBLY			1
51353	CARRIAGE ASSEMBLY		1	1
54433	GUIDE ROD			1
51357	BOTTOM SHIELD			1
51358	TOP SHIELD			1
51359	ARM ASSEMBLY, Side 1 (SA810 Only)			1
51360	TOP PLATE ASSEMBLY		1	1
51361	COLLET ASSEMBLY		2	2
51363	CAM SHAFT ASSEMBLY		1	1
51364	DC DRIVE MOTOR		1	1
51369	DISK EJECT ASSEMBLY		1	1
51380	FRONT PLATE ASSEMBLY			1
51407	BIAS SPRING BUTTON ASSEMBLY			1
51413	CLAMP, Cable Routing			1

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**TABLE 7-3. SPARE PARTS STOCKING GUIDE (CONT.)**

PART NUMBER	DESCRIPTION	QUANTITY PER LEVEL		
		SITE	BRANCH	DEPOT*
51498	TRK 00 WRITE PROTECT SENSOR ASM.	1	1	1
51498	WRITE PROTECT DETECTOR	1	2	2
51499	INDEX EMITTER ASSEMBLY		2	2
51500	DOOR LOCK SOLENOID ASSEMBLY		1	1
51501	STEPPER MOTOR ASSEMBLY		1	1
51509	BAIL ASSEMBLY		1	1
51523	KNOB, Painted			1
51497	DETECTOR INDEX ASSEMBLY	1	2	2
54646	ARM ASSEMBLY, Side 1 (SA860)		1	1

\*Depot parts listed are unique to the depot only. Stocking levels to support Branch stocks should be added.

39231-25/3

## **SECTION VII CUSTOMER INSTALLABLE OPTIONS**

### **7.1 INTRODUCTION**

The SA810/860 can be modified by the user to function differently than the standard method outlined in Sections I and II. These modifications can be implemented by adding or deleting connections and by use of the alternate I/O pins. Some options are capable of being connected by use of a shunting plug, Shugart P/N 15648 or AMP P/N 53013-2. This section will discuss a few examples of modifications and how to install them. The modifications discussed in the following paragraphs are:

- a. External Write Current Switch
- b. Two-Sided Status Output (SA860 only)
- c. Disk Change Option
- d. Side Select Option Using Direction Select (SA860 only)
- e. Side Select Option Using Drive Select (SA860 only)
- f. In Use Alternate Input
- g. Motor On Without Selecting Drive
- h. Motor On by Optional Motor On and Drive Select
- i. Motor Off Delay
- j. Radial Ready
- k. Stepper Power Down
- l. Write Protect Optional Use

Table 7-1 summarizes these options and the component designators indicating their PCB location in figure 7-1 and 7-2.

**TABLE 7-1. CUSTOMER CUT/ADD TRACE OPTIONS**

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
U9	TERMINATIONS FOR MULTIPLEXED INPUTS		PLUGGED
SI	INTERNAL WRITE CURRENT SWITCH		PLUGGED
SE	EXTERNAL WRITE CURRENT SWITCH	X	
TR	TRUE READY OUTPUT		PLUGGED
RTR	RADIAL TRUE READY†		X
2S	TWO-SIDED STATUS OUTPUT***	X	
DC	DISK CHANGE OPTION	X	
S1	SIDE SELECT OPTION USING DIRECTION SELECT***	X	
S2	SIDE SELECT INPUT***		PLUGGED
S3	SIDE SELECT OPTION USING DRIVE SELECT***	X	
1B,2B,3B,4B	SIDE SELECT OPTION USING DRIVE SELECT***	X	
D	ALTERNATE INPUT-IN USE	X	
MS	MOTOR ON FROM DRIVE SELECT*		PLUGGED
MO	ALTERNATE INPUT-MOTOR ON*	X	
MMO	ALTERNATE INPUT-MULTIPLEXED MOTOR ON†	X	
MD	MOTOR OFF DELAY	X	
R	READY OUTPUT		X
RR	RADIAL READY		X
SR	STANDARD READY†		PLUGGED
MT	MODIFIED TRUE READY† (OUTPUTS TRUE READY ON PIN 22)	X	
DS1	DRIVE SELECT 1 INPUT		PLUGGED
DS2,3,4	DRIVE SELECT 2,3,4 INPUT	X	
Y	DOOR LOCK/ACTIVITY LIGHT ACTIVATED FROM MOTOR ON†		PLUGGED
Z	DOOR LOCK/ACTIVITY LIGHT ACTIVATED FROM DRIVE SELECT†	X	
PD	STEPPER POWER DOWN	X	
WP	INHIBIT WRITE WHEN WRITE PROTECTED		X
NP	ALLOW WRITE WHEN WRITE PROTECTED	X	
TS	DATA SEPARATION OPTION SELECT**	X	

\*MOTOR ON is the complement of HEAD LOAD on the SA801 and SA851 disk drives. The only difference in the operation of MOTOR ON compared with HEAD LOAD is that MOTOR ON requires a 165 ms minimum delay (or TRUE READY must be monitored) before R/W activity is begun. HEAD LOAD on the SA801 and SA851 requires 35 ms or 50 ms minimum delay.

\*\*The SAB10/860 offers an optional data separator which properly separates data and clock bits through the soft-sectored IBM standard format and address mark area. Trace "TS" offers the optional separator.

\*\*\*Applies to SA860 only.

†Available on PCB P/N 25249 only.

39216-19-A



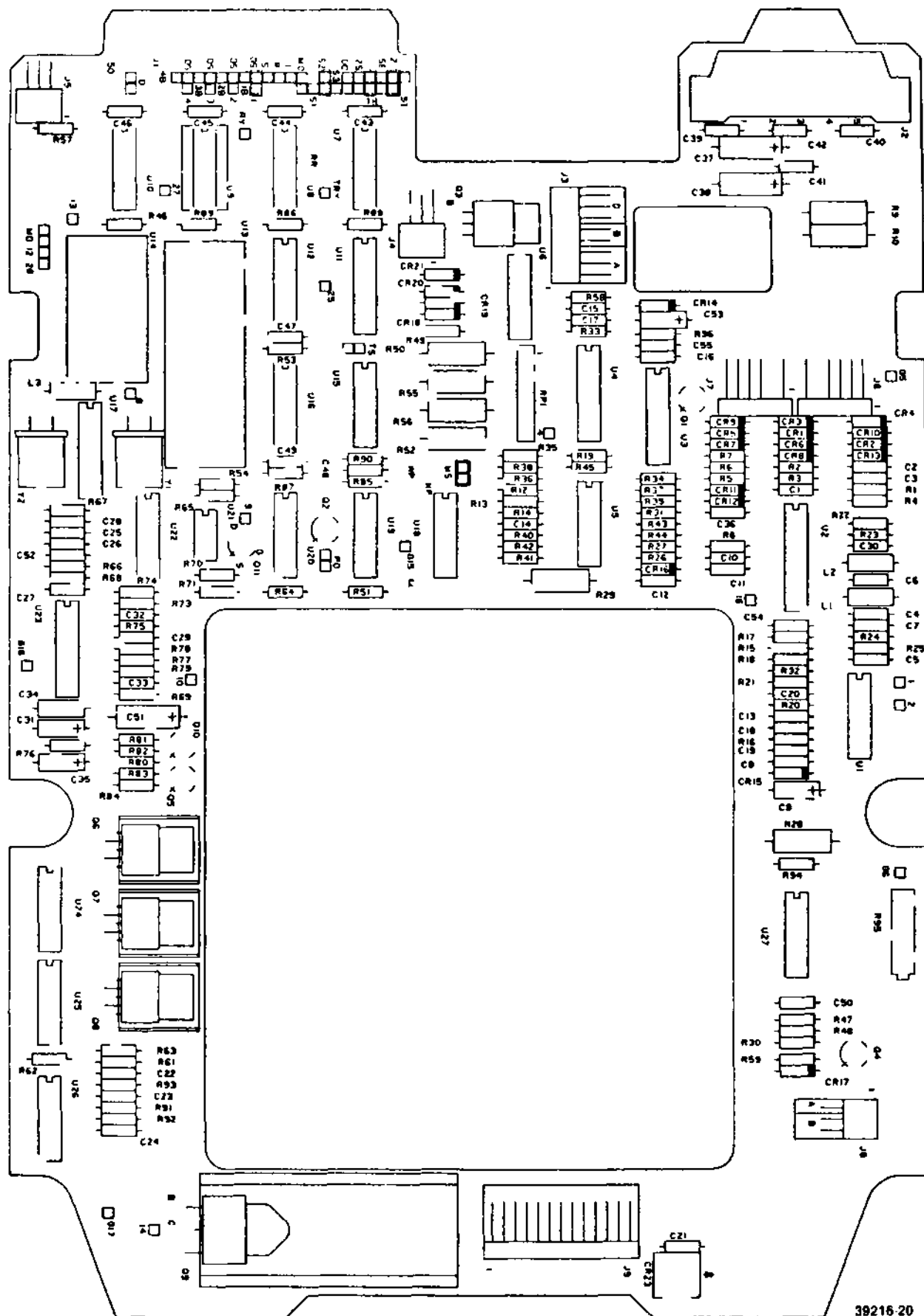
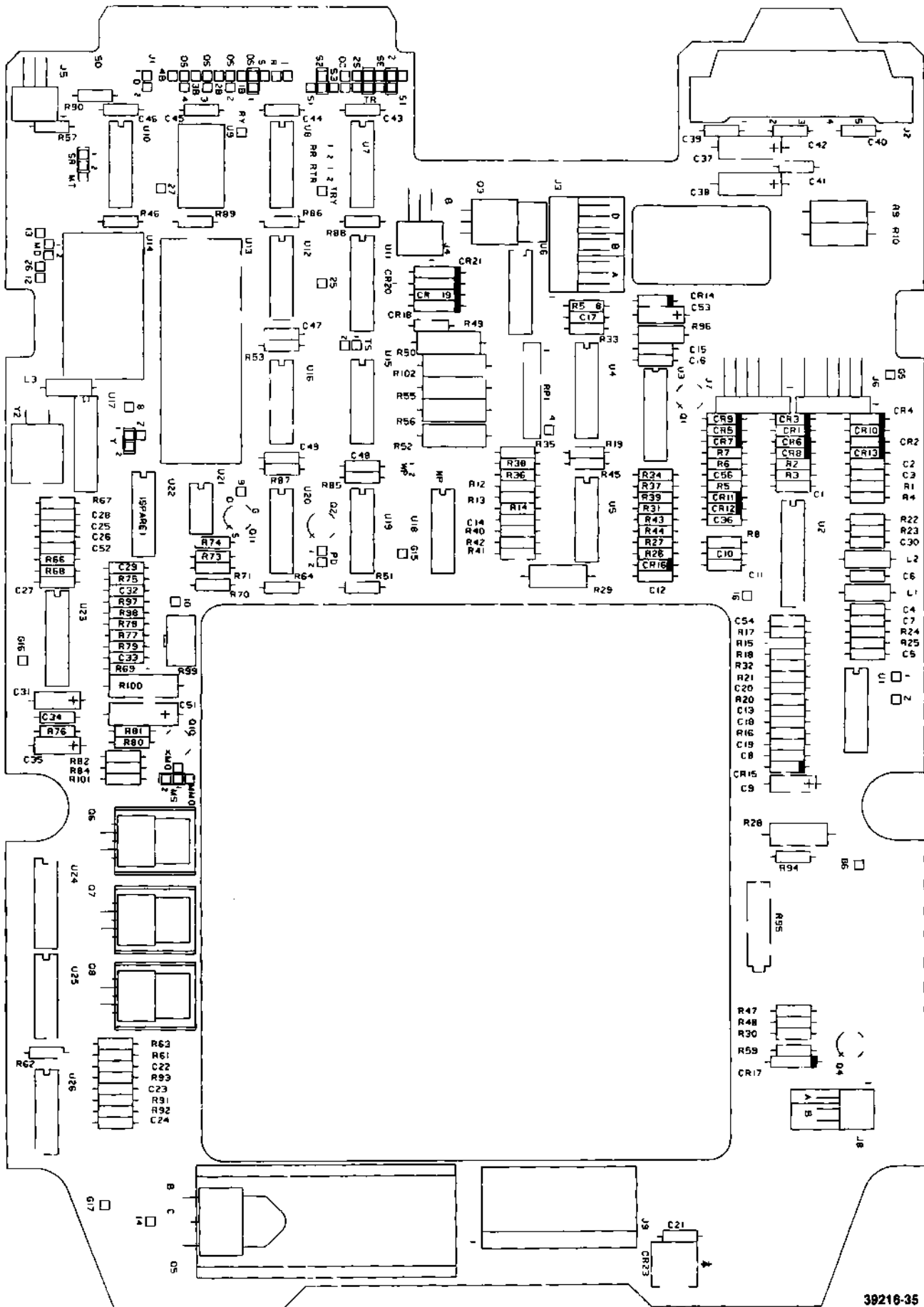


FIGURE 7-1. PCB COMPONENT LOCATIONS (P/N 25227 AND 25247)



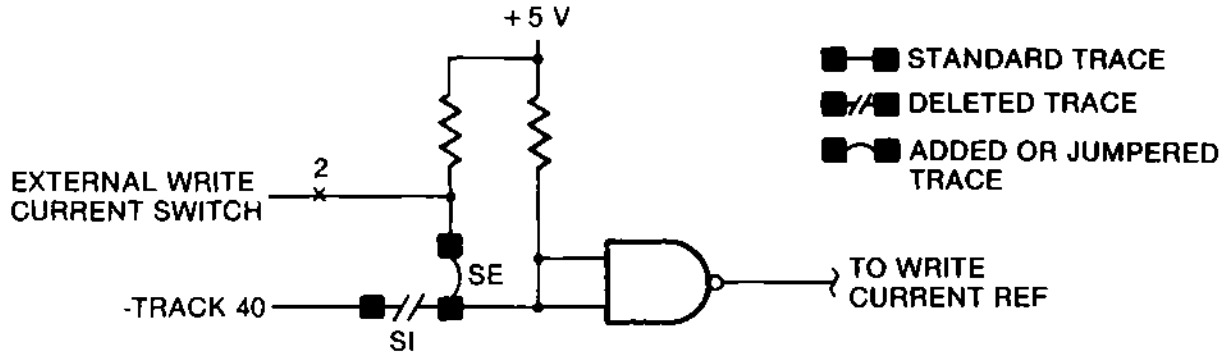
39216-35

FIGURE 7-2. PCB COMPONENT LOCATIONS (P/N 25249)

## 7.2 EXTERNAL WRITE CURRENT SWITCH

This option permits write current switching via the optional WRITE CURRENT SWITCHING interface line (pin 2). When the interface signal is activated to a logical zero level, the lower value of the write current is selected. Selecting this option replaces internal write current switching at track 40.

To enable external write current switching, move the shorting plug at trace SI to the SE position. See figure 7-3.



39216-21.

FIGURE 7-3. EXTERNAL WRITE CURRENT OPTION

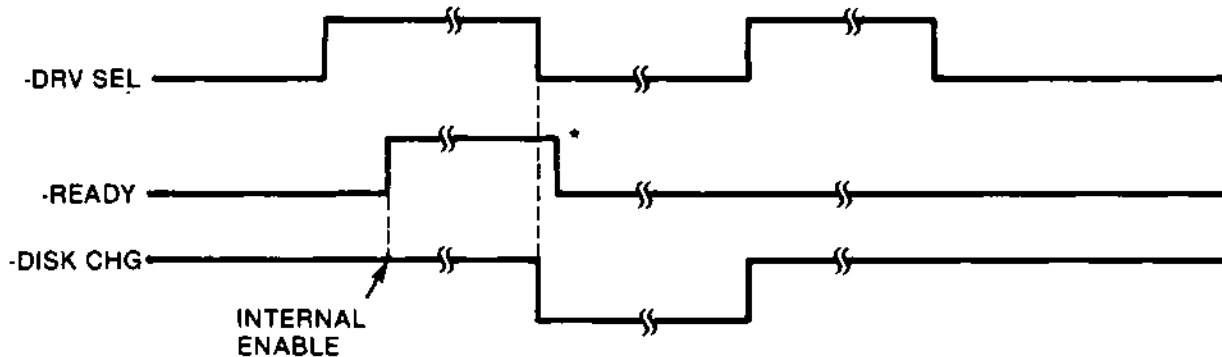
## 7.3 TWO-SIDED STATUS (OPTIONAL OUTPUT SA860 ONLY)

When the drive is selected and the diskette is spinning, this line will indicate a logical zero level for two sided media, and a logical one for single sided media.

To install this option on a standard drive, jumper trace 2S.

## 7.4 DISK CHANGE (OPTIONAL OUTPUT)

This customer installable option is enabled by jumpering trace DC. When DRIVE SELECT is activated, it will provide a true signal (logical zero) onto the interface (pin 12) if, while deselected, the drive has gone from a READY to a NOT READY (door open) condition. This line is reset on the true to false transition of DRIVE SELECT if the drive has gone READY. Timing of this line is illustrated in figure 7-4. The circuitry is illustrated in figure 7-5.

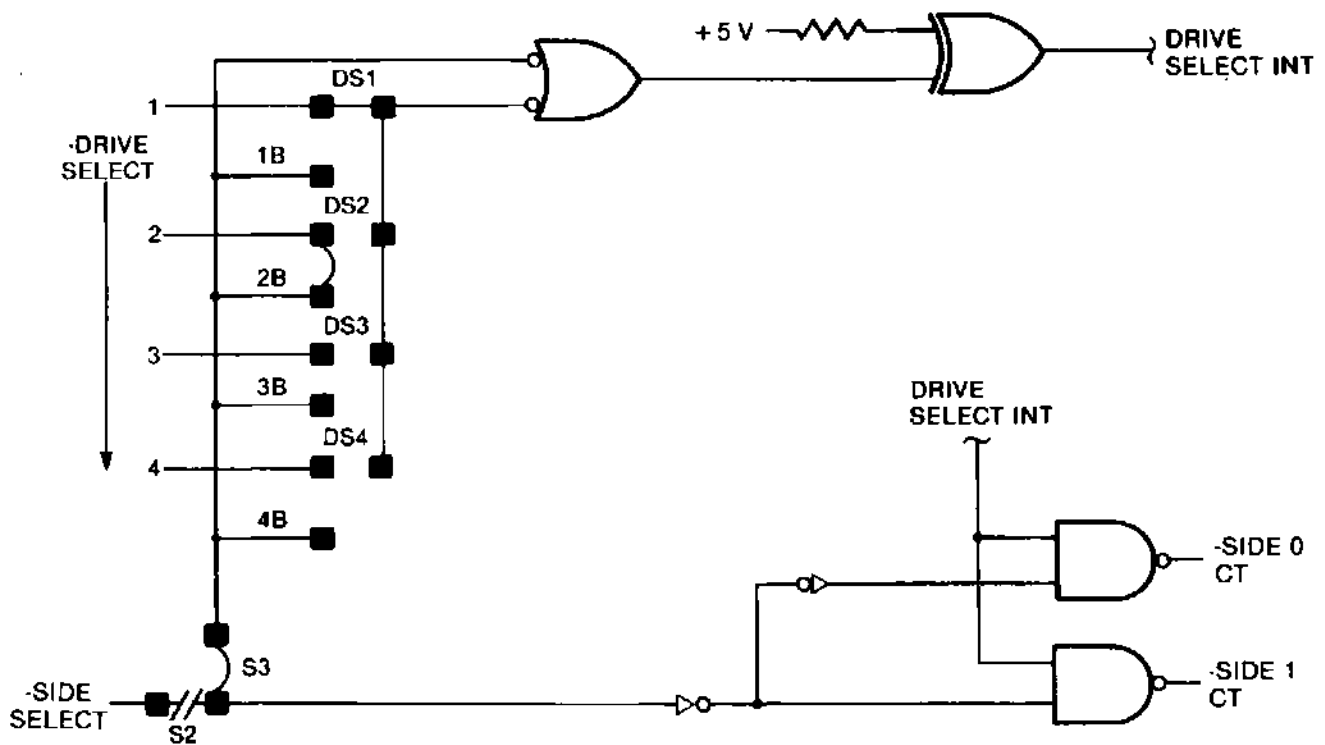


\*READY will not return until two index transitions after DRIVE SELECT (MOTOR ON).

39216-22

FIGURE 7-4. DISK CHANGE TIMING





39216-25

FIGURE 7-7. SIDE SELECTION USING DRIVE SELECT

### 7.7 IN USE ALTERNATE INPUT

This alternate input (pin 16) when activated to a logical zero level enables the Activity LED and door lock latch if the door is closed. If IN USE is low upon deselection, the door remains locked. If IN USE is high upon deselection, the door unlocks. To install this option, jumper trace D and move the shorting plug at trace Y to the Z position.

### 7.8 MOTOR ON WITHOUT SELECTING DRIVE

This option is useful in disk to disk copy operations. It allows the user to keep the motor on for all drives, thereby eliminating the motor start time. The motor is started on each drive via an Alternate I/O (pin 18). Each drive may have its own MOTOR ON line (Radial or Simplex) or they may share the same line (Multiplexed). When the drive is selected, a 1  $\mu$ s delay must be introduced or TRUE READY must be monitored before a read or write operation can be performed.

To install this option on a standard drive, move the shorting plug at trace MS to the MO position. See figure 7-8.

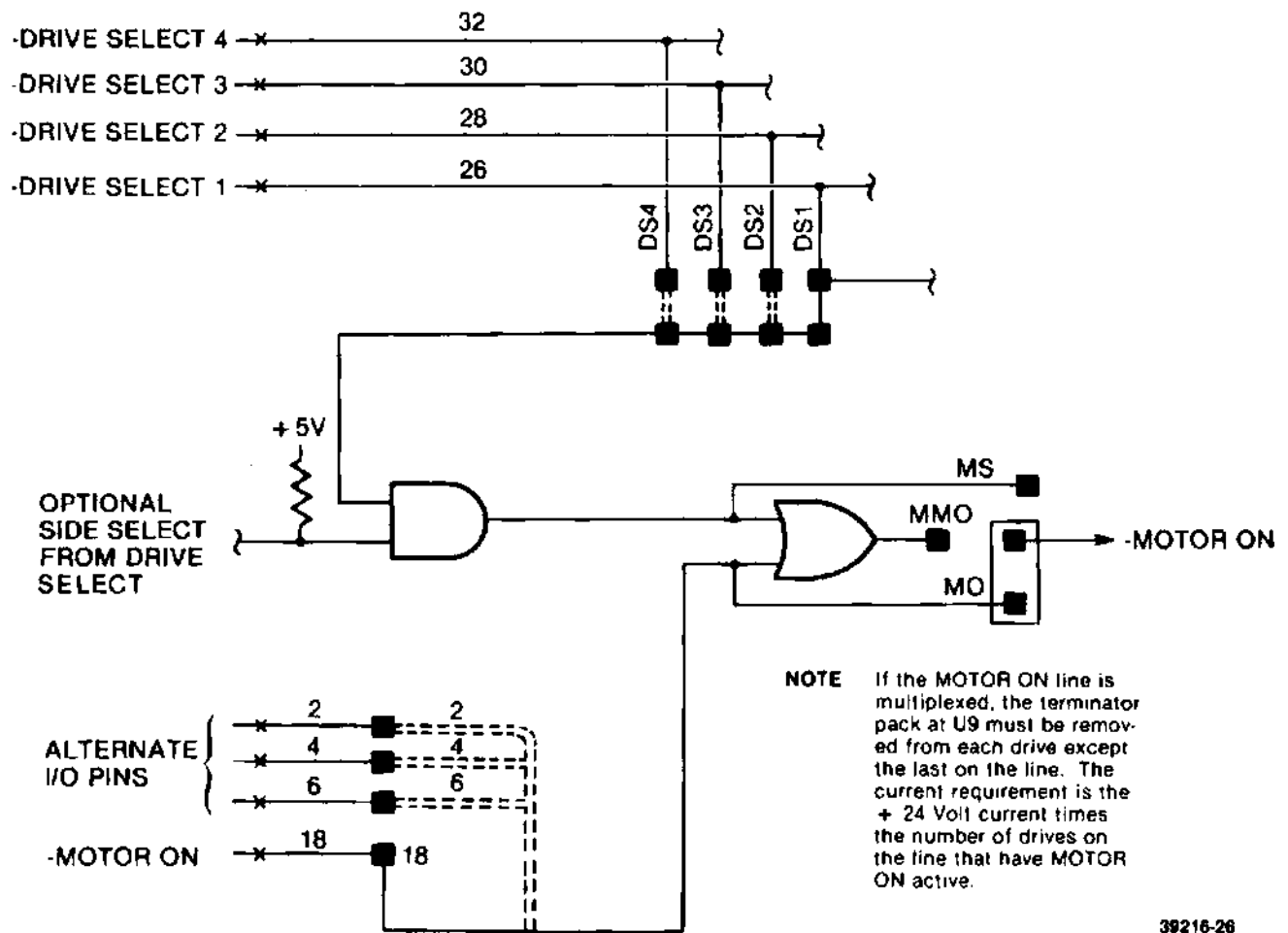


FIGURE 7-8. MOTOR ON WITHOUT SELECTING DRIVE CIRCUIT

### 7.9 MOTOR ON BY OPTIONAL MOTOR ON AND DRIVE SELECT

This option would be advantageous to the user who requires one drive to be selected at all times, but does not wish to keep the motor on for all drives. In this configuration, the dc spindle motor is controlled from DRIVE SELECT and the optional MOTOR ON line. The advantage of this option would be that the output control signals could be monitored without spinning the diskette thereby extending the head and media life. When the system requires the drive to perform a read or write, the controller would activate the MOTOR ON line (pin 18) which in turn would activate the spindle motor. After the MOTOR ON line is activated, a 165 ms delay must be introduced or the TRUE READY line must be monitored before a read or write operation can be performed.

To install this option on a standard drive, move the shorting plug at trace MS to the MMO position. Figure 7-9 illustrates the circuitry.

### 7.10 MOTOR OFF DELAY

This jumper option delays the spindle motor from turning off for 16 revolutions (2.6 seconds) after the DRIVE SELECT or optional MOTOR ON signal goes false (high). This allows the user to be able to read or write within 1  $\mu$ s after the drive has been reselected, thereby eliminating the motor start time. This option is advantageous for the user who wishes to perform copy routines, but does not wish to use the optional MOTOR ON input signal.

To enable the MOTOR OFF DELAY on the standard drive, jumper trace MD.

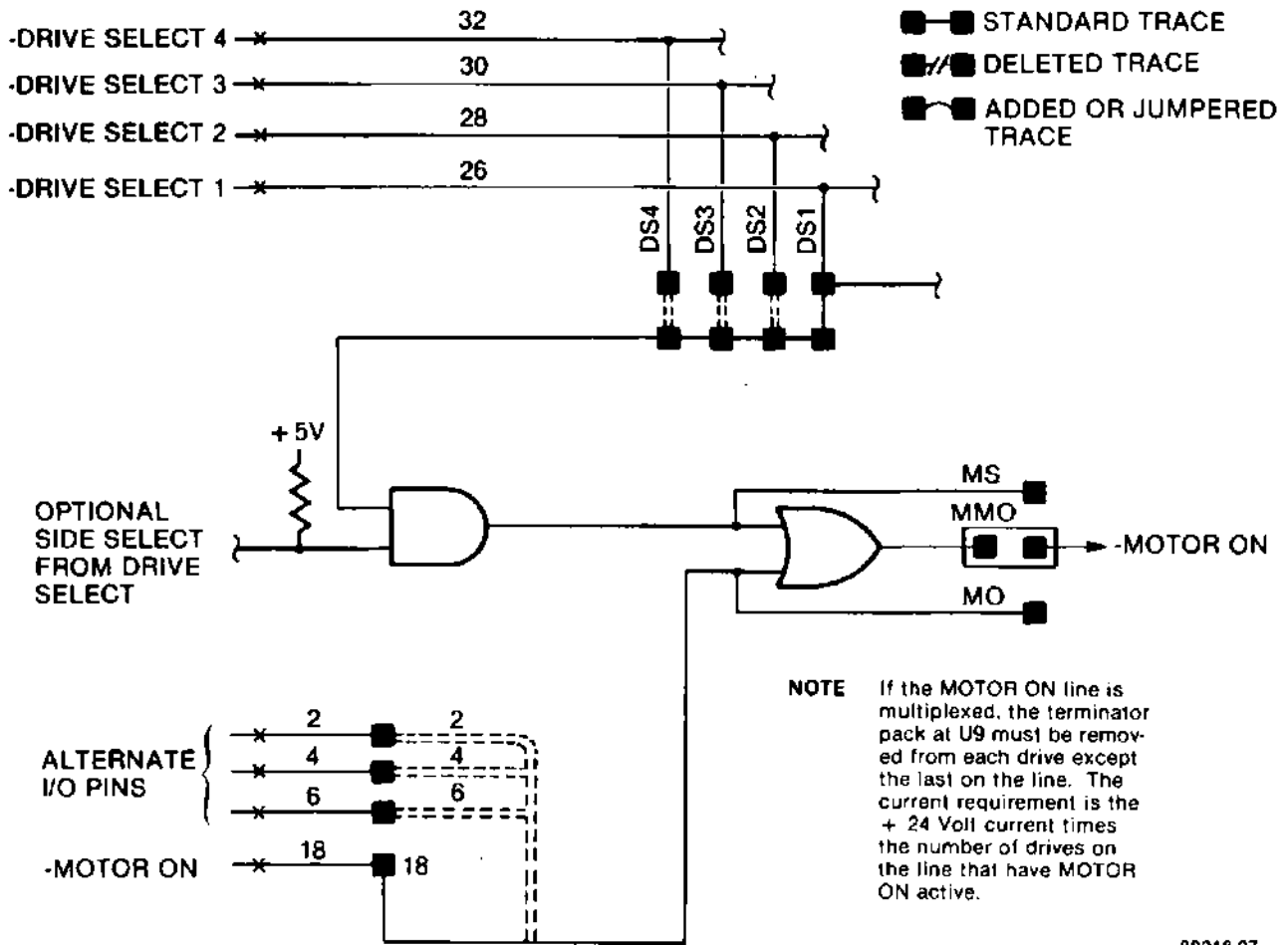


FIGURE 7-9. MOTOR ON BY OPT. MOTOR ON AND DRIVE SELECT CIRCUIT

### 7.11 RADIAL READY

This option enables the user to monitor the READY line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a diskette in any drive. Normally, the READY line from a drive is only available to the interface when it is selected.

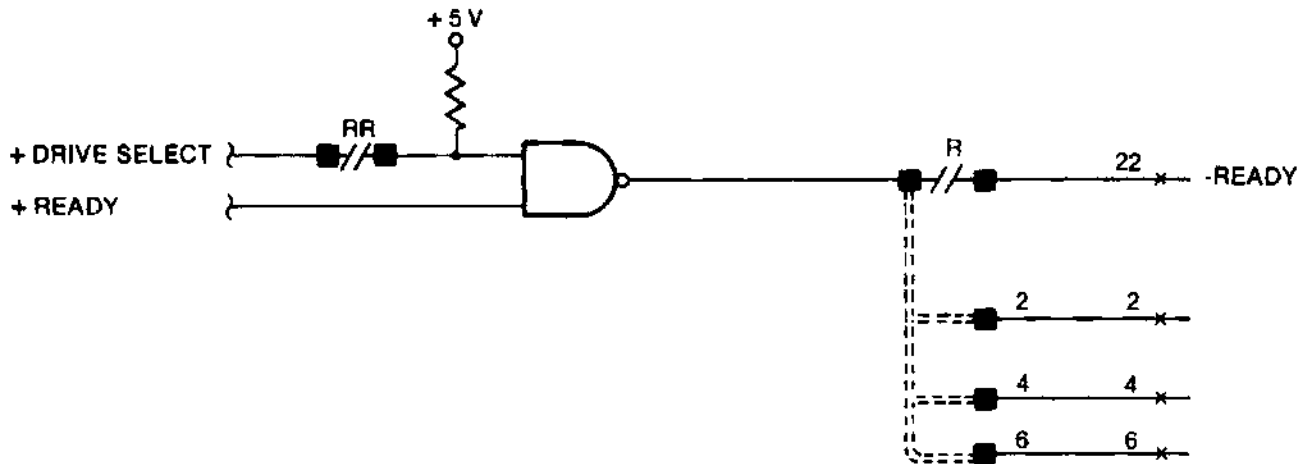
To install this option on a standard drive, the following traces should be deleted or added:

- Cut trace RR.
- Cut trace R.
- Add a wire from R to one of the Alternate I/O pins.

#### NOTE

One of the drives on the interface may use pin 22 as its READY line, therefore steps b and c may be eliminated on this drive. All the other drives on the interface must have their own READY line, therefore steps b and c must be incorporated.

Figure 7-10 illustrates the circuitry.



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FIGURE 7-10. RADIAL READY CIRCUIT

### 7.12 STEPPER POWER DOWN

If the user wishes to step the drive at a step rate of 6 ms or slower, enabling this option will allow the drive to maintain a low noise emission level.

To install this option on a standard drive, jumper trace PD.

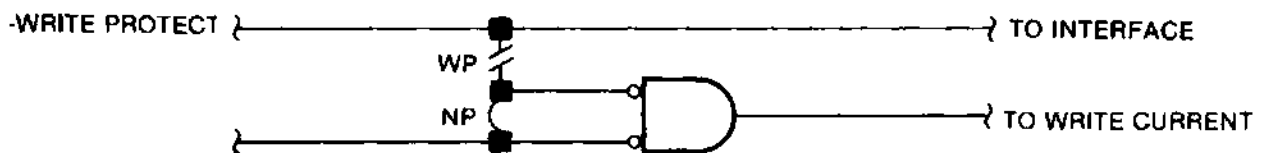
### 7.13 WRITE PROTECT OPTIONAL USE

As shipped from the factory, the write protect feature will internally inhibit writing when a write protected diskette is installed. With this option installed, a write protected diskette will not inhibit writing, but it will be reported to the interface. This option may be useful in identifying special use diskettes.

To install this option on a drive with the write protect feature, the following traces should be added or deleted.

- a. Cut trace WP.
- b. Connect trace NP.

Figure 7-11 illustrates the circuitry.



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FIGURE 7-11. WRITE PROTECT CIRCUIT