SA4000
Fixed Disk Drive

Service Manual

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1.0 INTRODUCTION

1.1 General Description

The Shugart Model 4000 Disk Drive is a random access storage device with one or two fixed 14 inch disks as the storage media. Each disk surface has two read/write heads and contains up to 404 data tracks. The drive provides up to 29 megabytes of on-line storage on 1616 addressable tracks. An option is available which allows 8 fixed heads (one per track) to be selected, providing 144 kilobytes of fast access storage. Up to 4 drives may be daisy chain connected in one system.

Low cost and reliability of the unit is achieved with a unique actuator design. The inherent simplicity of mechanical construction and electronic controls of the assembly allows maintenance free operation for the life of the drive.

Mechanical and contamination protection for the head, actuator, and disk is provided by an impact-resistant plastic enclosure. A self-contained re-circulating system supplies clean air through absolute filters that are designed to last through the life of the drive.

A single track of clock information is written on the disk and is read by a single fixed head. These clock pulses are used to synchronize the Phase Locked Oscillator in the data separation circuitry and provide Index, Sector and Write Clocking information from the disk. A jumper programmable counter is provided that converts the clock pulse into any number of sectors per track.

A data separator PCB is mounted in the drive enclosure. In addition to data separation of MFM Read Data, this PCB MFM encodes and write precompensates standardized Write Data.

The drive can be mounted in any 19 inch rack. It occupies 5.25 inches of vertical space and is 22 inches long.

1.2 Specifications Summary

1.2.1 Performance and Functional Specifications

MODEL	4004	4008
No. of Disk Surfaces	2	4
No. of Heads	4	8
No. of Cylinders	202	202
No. of Tracks	808	1616
Gross Capacity (M bytes)	14.54	29.08
Access Time (ms)		
One Track	20	20
Average	65	65
Maximum	140	140
Disk Speed	2964 RPM ±2%	
Recording Mode	MFM	
Recording Density	5534 BPI	
Flux Density	5534 FCI	
Track Capacity	18000 Bytes	
Track Density	172 TPI	
Transfer Rate	7.11 x 10^6 bits/sec.	
	889 x 10^3 bytes/sec.	
Sectors	Programable	
Start Time	1.5 minutes	

1.2.2 Physical Specifications

Environmental Requirements

	Operating	Shipping	Storage
Temperature (host ambient) – F	50 to 105	-40 to 144	-8 to 117
Relative humidity – %	(10 to 41°C)	(-40 to 62°C)	(-22 to 47°C)
	8 to 80	1 to 95	1 to 95
Maximum wet bulb	78°F non-condensing		

AC Power Requirements

50/60 Hz ± 0.5 Hz

100/115 VAC Installations = 90 to 127 V @ 2.9A maximum

200/230 VAC Installations = 180 to 253 V @ 1.9A maximum

DC Voltage Requirements

+24 V ± 10% @ 3A maximum

+5V ± 5% @ 3A maximum

-7 to -16 V @ 0.15A maximum (option -5 V ± 5% @ 0.10A maximum)

Physical Dimensions

Height	5.22 inches maximum (132.6 mm)
Width	16.7 inches maximum (424 mm)
Depth	21.9 inches maximum (556.3 mm)
Weight	35 pounds (15.9 kg)
Heat dissipation	880 BTU/Hr. typical (235 Watts)

1.2.3 Reliability Specifications

MTBF:	8000 power on hours
MTTR:	30 minutes
Component life:	5 years normal usage
Acoustic noise level:	less than NR 55
Error Rates:	
Soft read errors:	1 per 10^{10} bits read
Hard read errors:	1 per 10^{12} bits read
Seek errors:	1 per 10^7 secks
Preventive Maintenance:	none required

2.0

This section will functionally describe the major circuits of the SA4000. For interface timing, refer to the SA4000 OEM manual Part Number 39005.

2.1 POWER ON RESET (POR)

When DC voltages are applied to the SA4000, C44 on the Control board charges up momentarily, preventing Q4 from turning on. From the time +5 goes high until Q4 turns on is approximately 15 msec, thus IC 5G will output a 15 msec –POR pulse. This low pulse has several functions.

It resets the IN LOCK circuit (IC's IB, ID, and 2E) and the WRITE FAULT DETECT circuit (IC 7F) on the Control PCB. –POR then becomes +POR and is transferred to the Actuator PCB, where it loads the step count buffers (IC's 5C and 5D), disables the step-count timer (IC 1A) and loads the AC motor phase counter (IC 1C) so that on DC power up, phase A will be energized. SEEK COMPLETE is generated and with IC 5B set, the step circuit will wait for a step pulse.

2.2 STEPPING

Control PCB

To initiate a seek operation, the controller issues the required number of step pulses and also sets the DIRECTION line at least 200 nsec before the trailing edge of the step pulse.

If the drive is SELECTED and a WRITE operation is not in progress, the step pulses (–STP) and direction of seek (–DIRECTION IN) will be gated through the Control PCB to the Actuator PCB via pins 4 and 2 respectively of connector J7.

Actuator PCB

In order to be valid, step pulses must be at one of two rates. In the Normal mode there will be 1.1 msec or more time delay between incoming step pulses. In the Buffered mode there will be less than 350 μsec time delay between them. If step pulses are incoming 600 μsec apart for example, then every other pulse would be lost causing the heads to move only half the required number of tracks. The reason for this is that the step count timer located at position 1A which counts down to zero in approximately 500 μsec would output a low pulse. This pulse then clocks chip 5B blocking out incoming step pulses for another 500 μsec while chip 1A once again counts down to zero generating a single track step and a SEEK COMPLETE signal. At this time another step pulse is allowed to enter, but the previous one was lost.

In the Normal step mode, pulses are gated through chip 1B incrementing the step count buffers (IC 5C and 5D) by 1 and starting the step rate timer (IC 1A). In approximately 500 μsec the timer, which was preset by the last step pulse, counts down to zero. The low pulse generated at that time does the following: 1) clocks IC 5B pin 3 preventing any more step pulses from being processed until the heads have stepped 1 track, 2) Clocks IC 5B pin 11 dividing the step rate timer outputs by 2 lengthening the time between steps to 1 msec, and 3) presets itself for the next step pulse input. The step rate timer now counts down, once more outputting a low pulse when count zero is reached. This second timer clocks IC 5B pin 11 again, this time decrementing the step count buffers by 1 and clocking the DIRECTION through the phase counter to the decoder at 2C.

The phase counter, which is always set to phase A on DC power up, increments or decrements according to the level of the DIRECTION line. For example, a phase count of 3 (Q_A high · Q_B high · Q_C low) would be decoded by chip 2C to become 1Y1 and 2Y1 low, energizing both coils B1 and A2 simultaneously. For a complete sequencing chart refer to Figure 1.

Since the step pulse counters were decremented, a borrow output in generated, clocking IC 4A. This results in chips 5B, 5C, and 5D being reset for any further step pulses and also generates SEEK COMPLETE.

Buffered seeking entails exactly the same sequence of events with the only difference being that all of the step pulses are loaded into the step pulse buffers before chip 1A is allowed to clock them out to the stepper motor. In this mode the step rate is accelerated and decelerated for the first/last 16 steps. Refer to table 1 showing the acceleration/deceleration step values.

STEPPER ACCELERATION/DECCELERATION VALUES

STEP #	STEP TIME (μSEC)
1	984
2	1050
3	884
4	812
5	755
6	708
7	671
8	641
9	617
10	598
11	583
12	572
13	564
14	558
15	554
16	552

Table 1

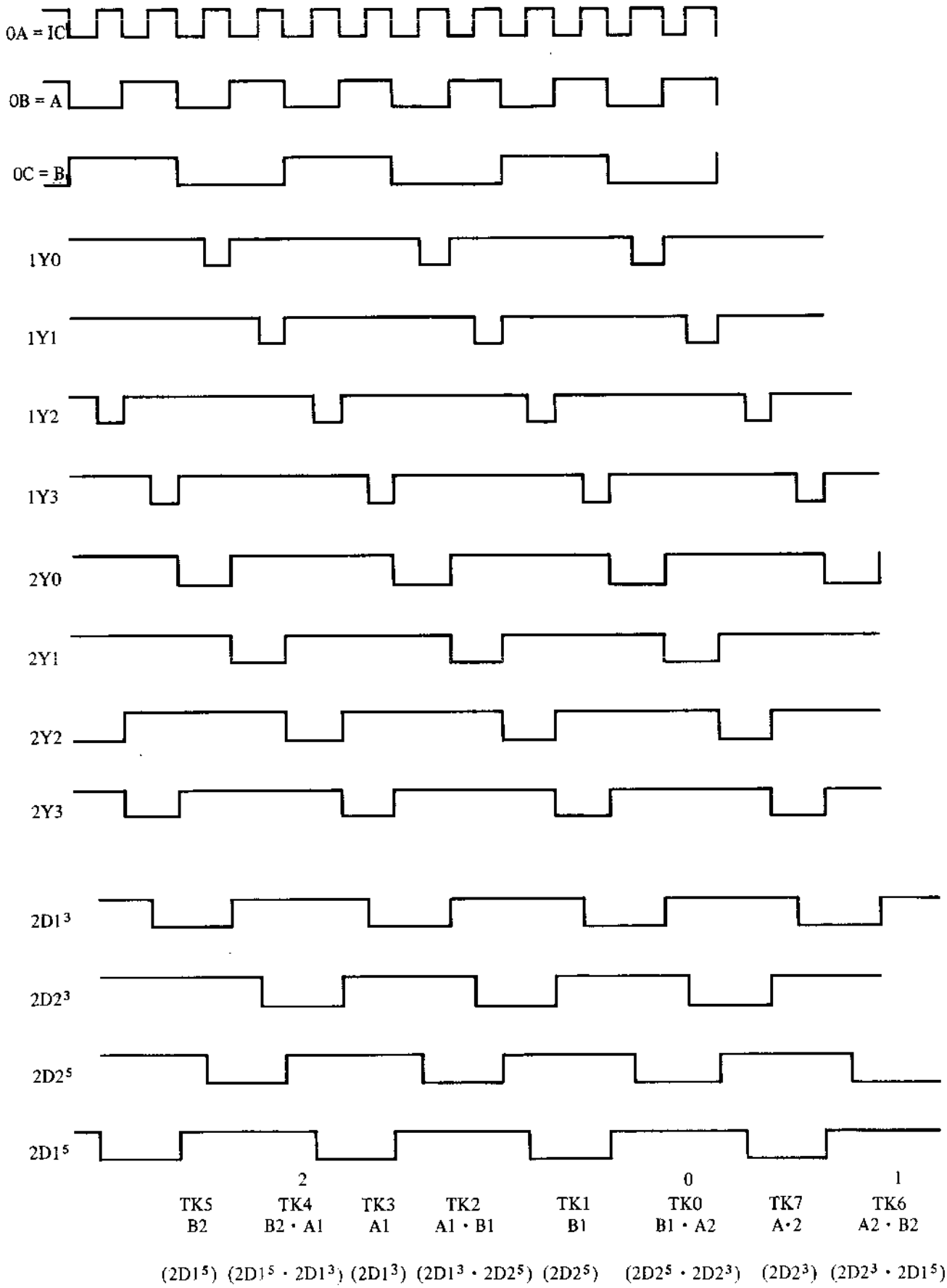


Figure 1. Stepping Sequence

2.3 READ OPERATION

When the controller desires to initiate a read operation, it will select the appropriate head and drop the -READ GATE line . If the drive has been selected, -READ GATE goes to the VFO PCB via socket 7C and the -HEAD SELECT signal goes to the R/W PCB via connector J6.

R/W PCB (Refer to Figure 2)

The head select lines are decoded by chips 5A and 2A who choose the appropriate head, by grounding its center tap. Flux transitions are now passed through the head core into the isolation stage of the read channel. This stage isolates the head from the read channel during the write mode, provides the necessary damping for detection of flux transitions, and affords the requisite impedance matching between the selected head and the first stage of amplification.

The first amplification stage is a high pass network with a pole located at 76.9 KHz. It removes all DC offset as well as provides a linear high pass for frequencies greater than 1 MHz. Midband amplification at this stage is 312 (50 dB).

Next the four pole bessel type filter network increases the signal to noise ratio and linearizes the phase by having a constant time delay. Load impedance for the first amplification stage is also provided.

Raw data is differentiated and amplified once more by chip 3D which is a high pass linear amp providing a midband voltage gain of 96. Total gain for the two amplification stages equals 9 for 1F frequency and 5 for 2F frequency.

Control PCB

Amplified raw data then goes to the Control board via connector J6 as ±DIFF READ. ±LINEAR signal is not used. The analog to digital converter chip 7B is a bidirectional one shot device whose outputs correspond to any flux transitions detected by the read head. A head with very high resolution will occasionally translate droop into a flux change. All of the flux transitions, including any invalid droop conditions, are scrutinized by the droop ignore circuit whose 30 nsec delay allows invalid transitions to be filtered out. Droop ignored raw data then goes to the VFO PCB via socket 7D.

VFO PCB

-READ GATE is active when a read operation is in progress. Chip 1B will be clocked by raw data, counting up. [After 4 bits, 1B will enable NRZ READ DATA to be sent to the controller.] At the same time it disables chip 1E activating the window generator chip 2E. VCO 2F is now compared to the stream of raw delayed data. This stream consists of clock and data bits 20 nsec wide delayed by 30 nsec.

If raw data bits are early with respect to VCO 2F, the top half of the window generator chip 2E pin 7 goes low turning on Q2 charging up C13, who then generates a positive going DC error voltage. If data bits are late with respect to VCO 2F, the bottom half of chip 2E pin 5 goes high turning on Q4 discharging C13, who then generates a negative going DC error voltage. Chip 2D pin 9 is always high between raw data pulses locking up the window generator. Without this condition VCO 2F which is twice the frequency of the data bit stream would cause a large false DC error voltage to be produced whenever no data was present.

DC ERROR voltage, if it is a high going signal, will cause the varicap CR3 to decrease its capacitance, speeding up the frequency of the VCO 2F oscillator CK+, thus VCO 2F which was lagging behind the raw data stream will speed up. This cycle always continues during the read operation as the VCO 2F frequency tracks the data bit frequency, i.e., the disk's rotational speed.

Corrected VCO 2F is divided by 2 at chip 4E becoming VCO 1F. Each alternate cycle of the VCO 2F frequency, according to jumper D/C (sync on all 0's or all 1's) will put all of the data

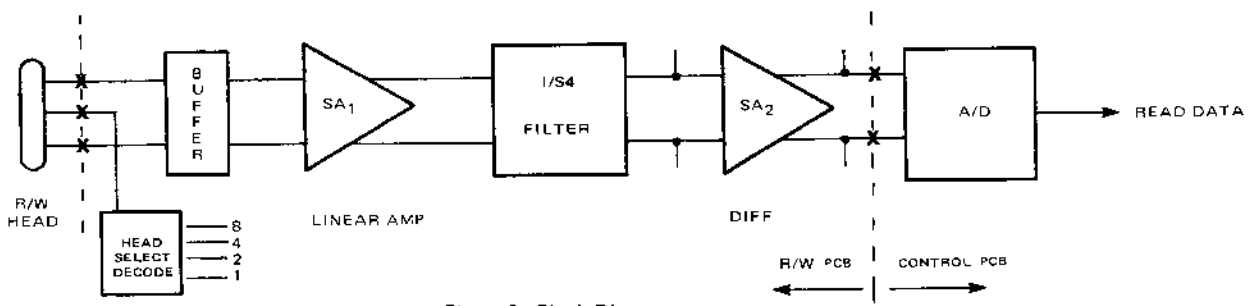


Figure 2. Block Diagram

bits into pin 4 of chip 5E and all of the clock bits into pin 10 of chip 5E. 5E acts as an R/S flip flop and latches on the data bits, clears on the clock bits. By latching in this manner the data window is extended so that delayed data will be centered in the window to prevent late data bits from "slivering" and appearing in both data and clock window. The output of chip 5D then is centered, delayed data bits only. They are stored in 6D until clocked out of pin 5 by 5 VCO 1F. Chip 6D pin 9 then outputs a low whenever no data is present and a high if data is present, i.e., NRZ READ DATA.

Control PCB

This data is then transferred to the Control PCB via socket 7D where it is input to the line drivers at 7H and transmitted to the controller as NRX READ DATA.

2.4 WRITE OPERATION

Control PCB

When the controller desires to write data to the disk, it will activate-head select, –WRITE GATE, WRITE CLOCK, and NRZ WRITE DATA.

If the drive is in the READY condition, is SELECTED, and there are no FAULT conditions, –WRITE GATE will be gated to the R/W PCB via connector J6, and will allow the write operation to begin.

+WRITE CLOCK, –WRITE CLOCK, +WRITE DATA, and –WRITE DATA all enter the differential amplifiers at chip 6H, becoming +WRITE DATA and +WRITE CLOCK +WRITE DATA passes to the VFO PCB via socket 7D and +WRITE CLOCK goes to the VFO PCB via socket 7C.

VFO PCB

+WRITE DATA and +WRITE CLOCK are mixed at chip 6C and enter the precompensation circuit composed of chips 4A, 4B, 5A, 5B, and 5C. Depending on the pattern of this clock and data stream, an appropriate amount of precompensation is added. The early line, (pin 3 of chip 4A) delays the raw data stream by 8 nsec, the on time line (pin 5 of chip 4A) delays it by 16 nsec, and the late line (pin 9 of chip 4A) delays it by 24 nsec. At this point the + MFM WRITE DATA goes back through the Control PCB via socket 7D and to the R/W PCB via connector J6.

R/W PCB

+ WRITE DATA (actually composite clock and data bits) is converted from digital to analog by chips 1B, 2B, and 3B and associated circuitry. + MATRIX or – MATRIX is selected by chip 3B depending on whether or not a one or a zero is to be written. the HEAD SELECT lines are decoded by chips 2A and 5A choosing one of the possible 16 heads by grounding its center tap. Current flows through the appropriate matrix diodes to the selected head and flux transitions are imposed on the media surface.

2.5 ERROR CIRCUIT

The error circuit is located on the Control PCB and its function is to prevent writing on the media at improper times. + MULTI HEAD, – WRITE CURRENT, –NOT READY, or –READ•WRITE condition will cause a +BLOCK WRITE and a –FAULT to be issued. +BLOCK WRITE will prevent –WRITE GATE from being active, –FAULT will be sent to the controller who must toggle the –FAULT CLEAR line in order to reset the fault circuit.

+MULTI HEAD is the result of the R/W PCB circuit selecting in more than one head.

–WRITE CURRENT occurs when –WRITE GATE is active but no write current (IW SENSE) is sensed in the R/W PCB write circuit, or –WRITE GATE is inactive and write current is present in the R/W PCB write circuit.

–NOT READY is active if –WRITE GATE is on, but the drive is not in the READY condition.

–READ•WRITE happens if both –READ GATE and –WRITE GATE are active concurrently.

3.0 TROUBLESHOOTING TECHNIQUES

Philosophy

The following troubleshooting techniques are designed to aid field service personnel in locating a drive fault down to the PCB level (modular replacement) or to determine that the drive is not field repairable, in which case the drive must be repaired at a depot facility.

Equipment Required

1. A power supply capable of generating the following voltages:
   a. +5 volts at 3 amps maximum
   b. +24 volts at 3 amps maximum
   c. -5 volts at 0.1 amps maximum or
      -7 to -16 volts at 0.15 amps maximum.
2. Oscilloscope – Tektronix 464 or equivalent.
   a. Probes: X10 2 each
      X1 1 each

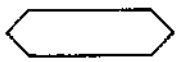
Troubleshooting Flowcharts

The interface signals utilized by the various flowcharts may be generated by the host system/controller through its own diagnostic routines, or by the SA4000 suitcase tester available from Shugart.

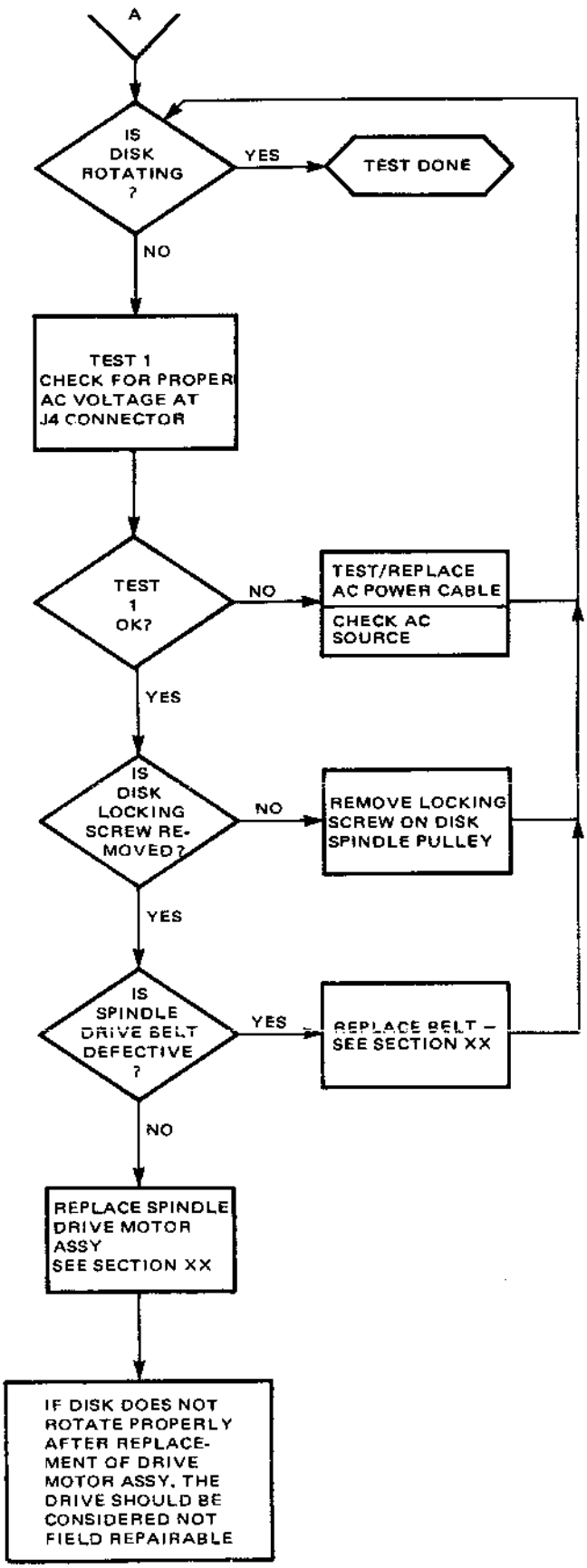
Flowchart Symbols


Test Entry Point


Perform Test Indicated


Test is completed successfully – Go on to next test.

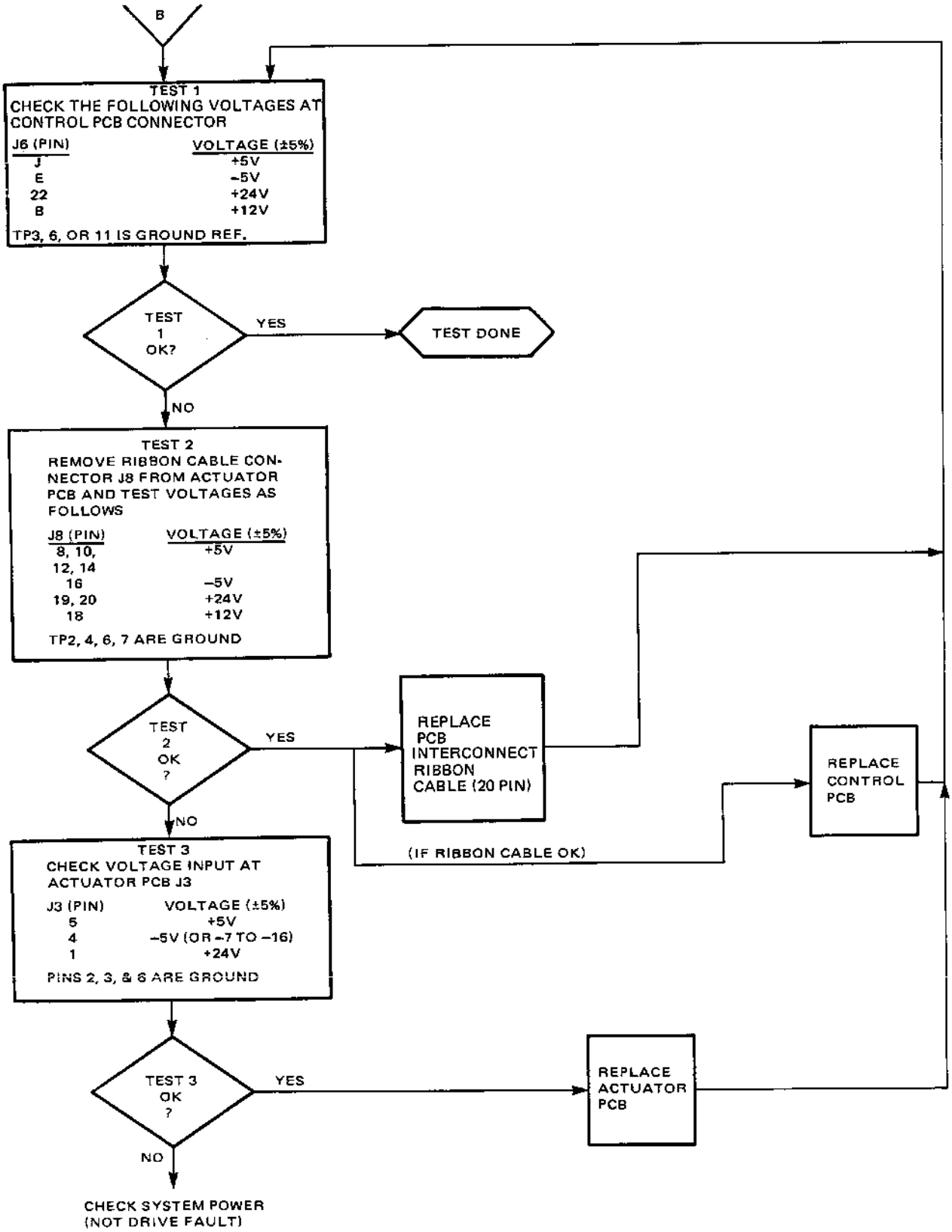
AC POWER TEST

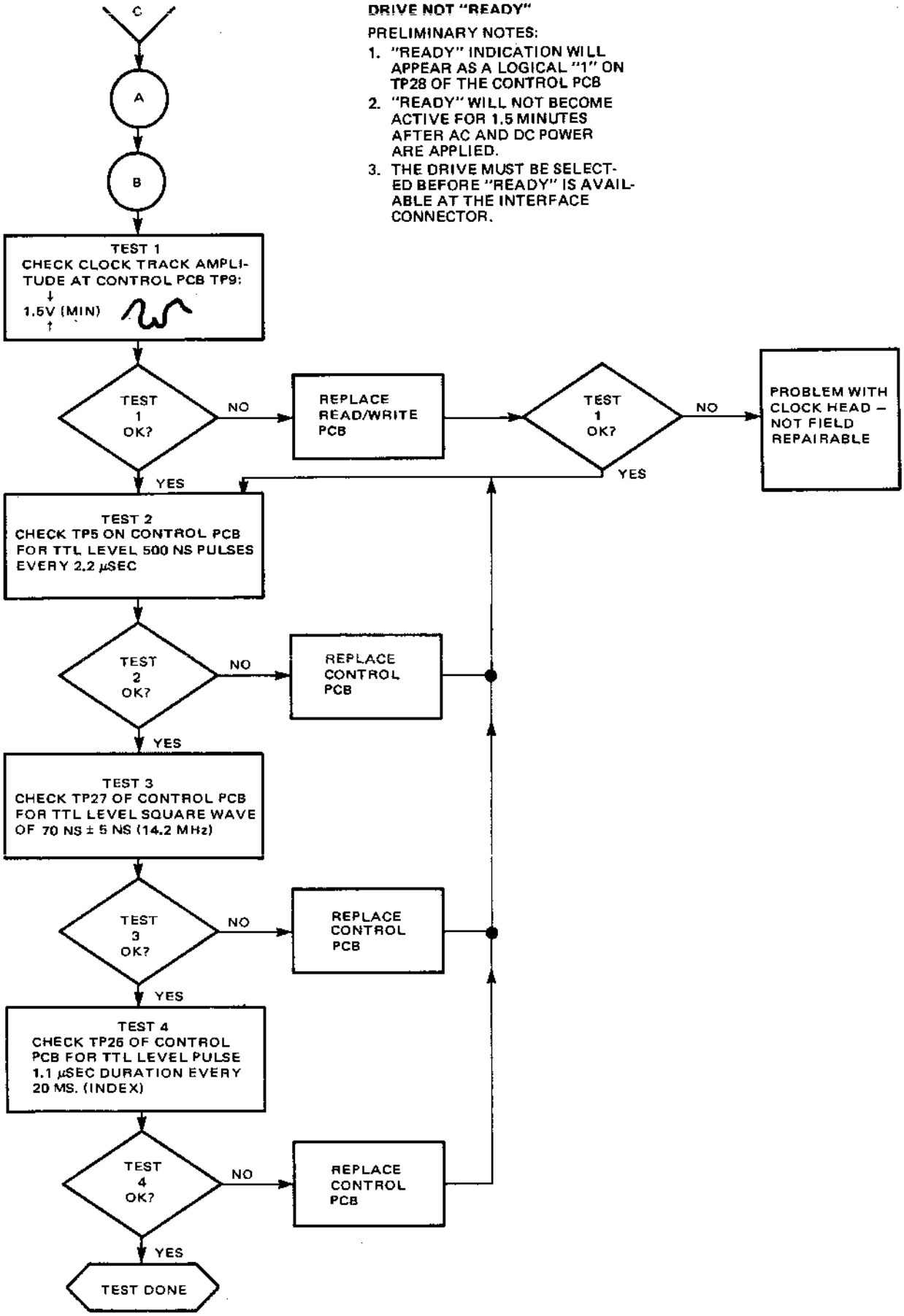


D.C. POWER TEST

PRELIMINARY NOTES:

1. CHECK REGULATOR JUMPER OPTION ON ACTUATOR PCB FOR CORRECT POSITION (–5V OR –15V).



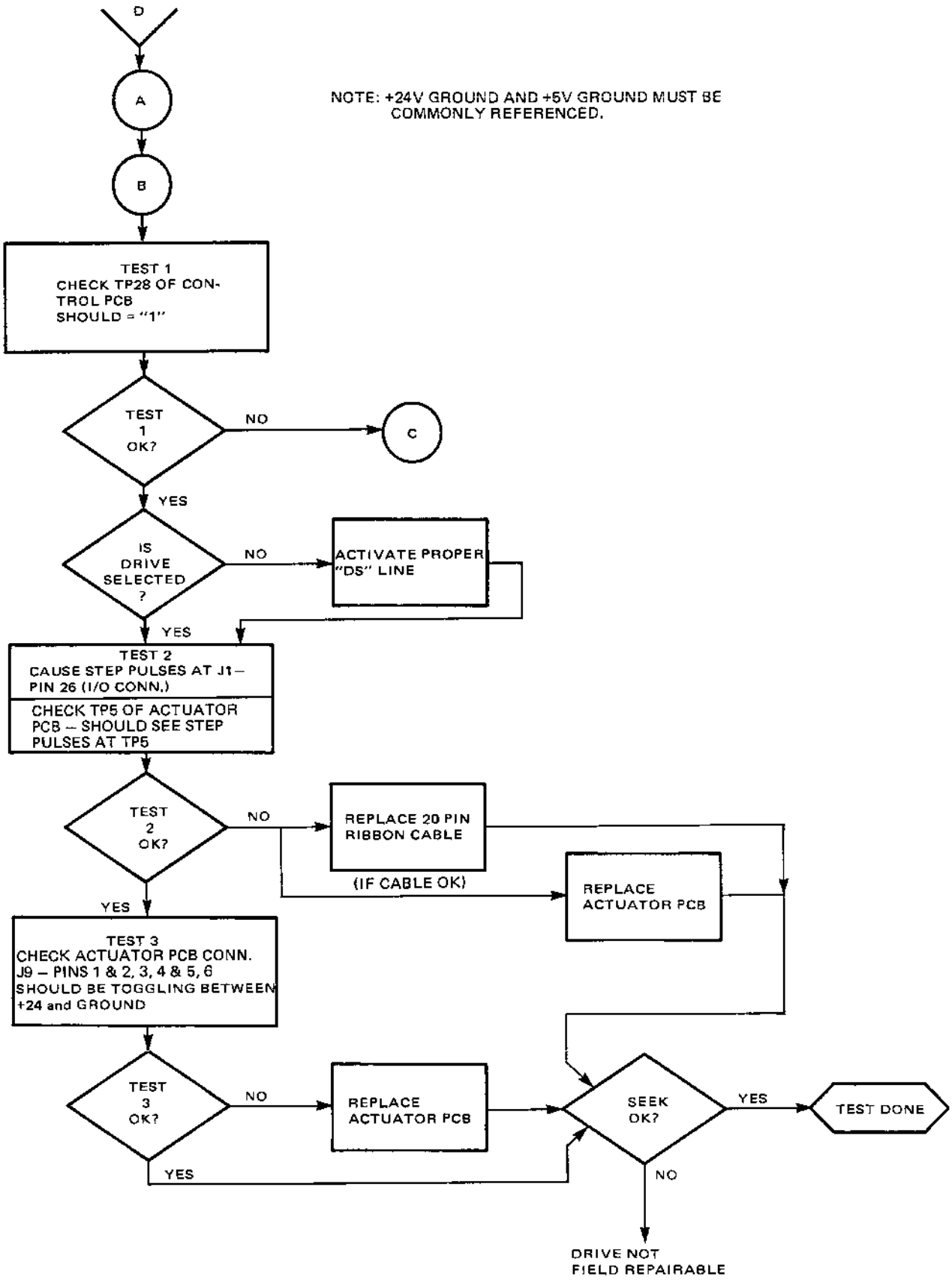


DRIVE NOT "READY"

PRELIMINARY NOTES:

1. "READY" INDICATION WILL APPEAR AS A LOGICAL "1" ON TP28 OF THE CONTROL PCB
2. "READY" WILL NOT BECOME ACTIVE FOR 1.5 MINUTES AFTER AC AND DC POWER ARE APPLIED.
3. THE DRIVE MUST BE SELECTED BEFORE "READY" IS AVAILABLE AT THE INTERFACE CONNECTOR.

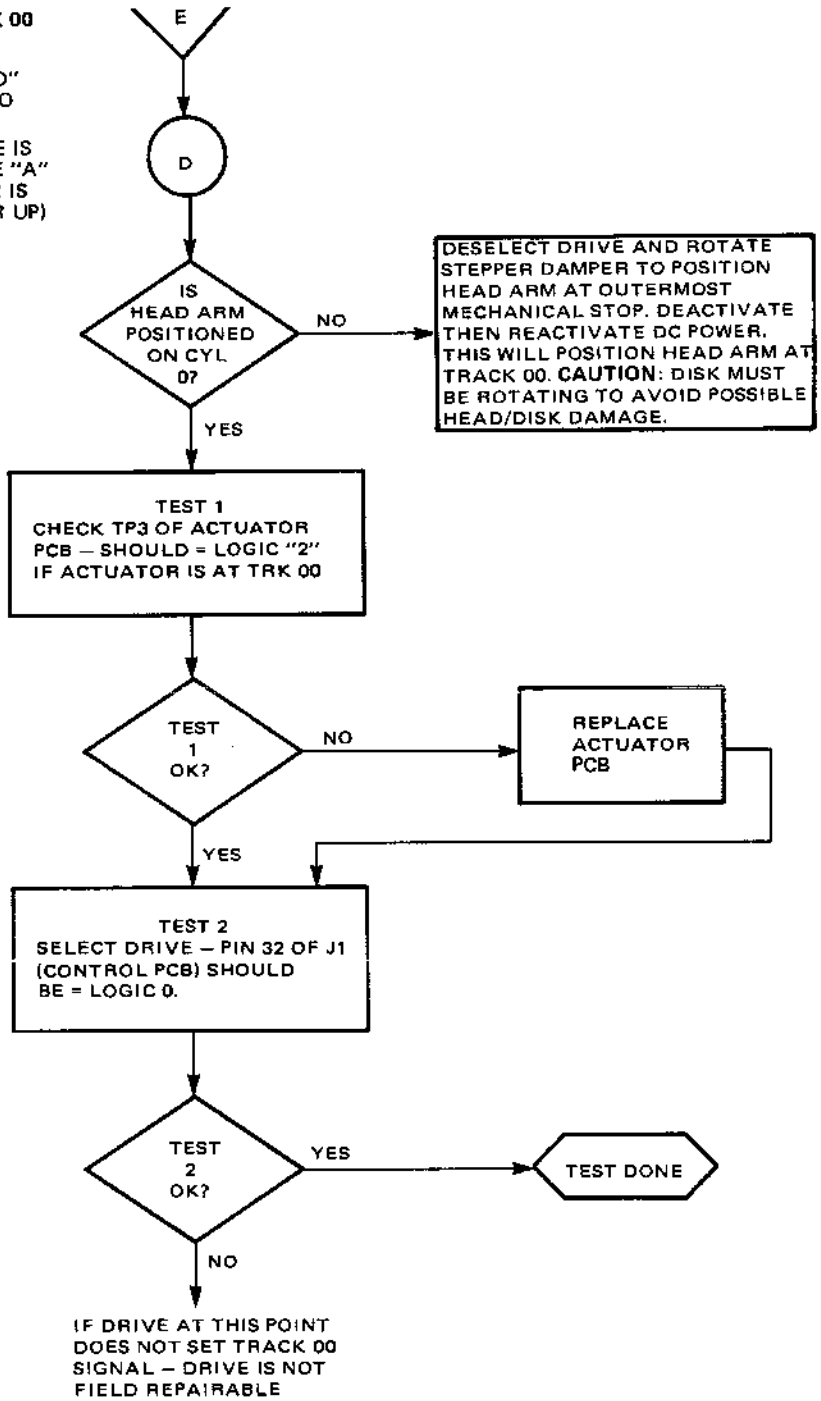
DRIVE DOES NOT SEEK



DRIVE DOES NOT FIND TRACK 00

PRELIMINARY NOTES:

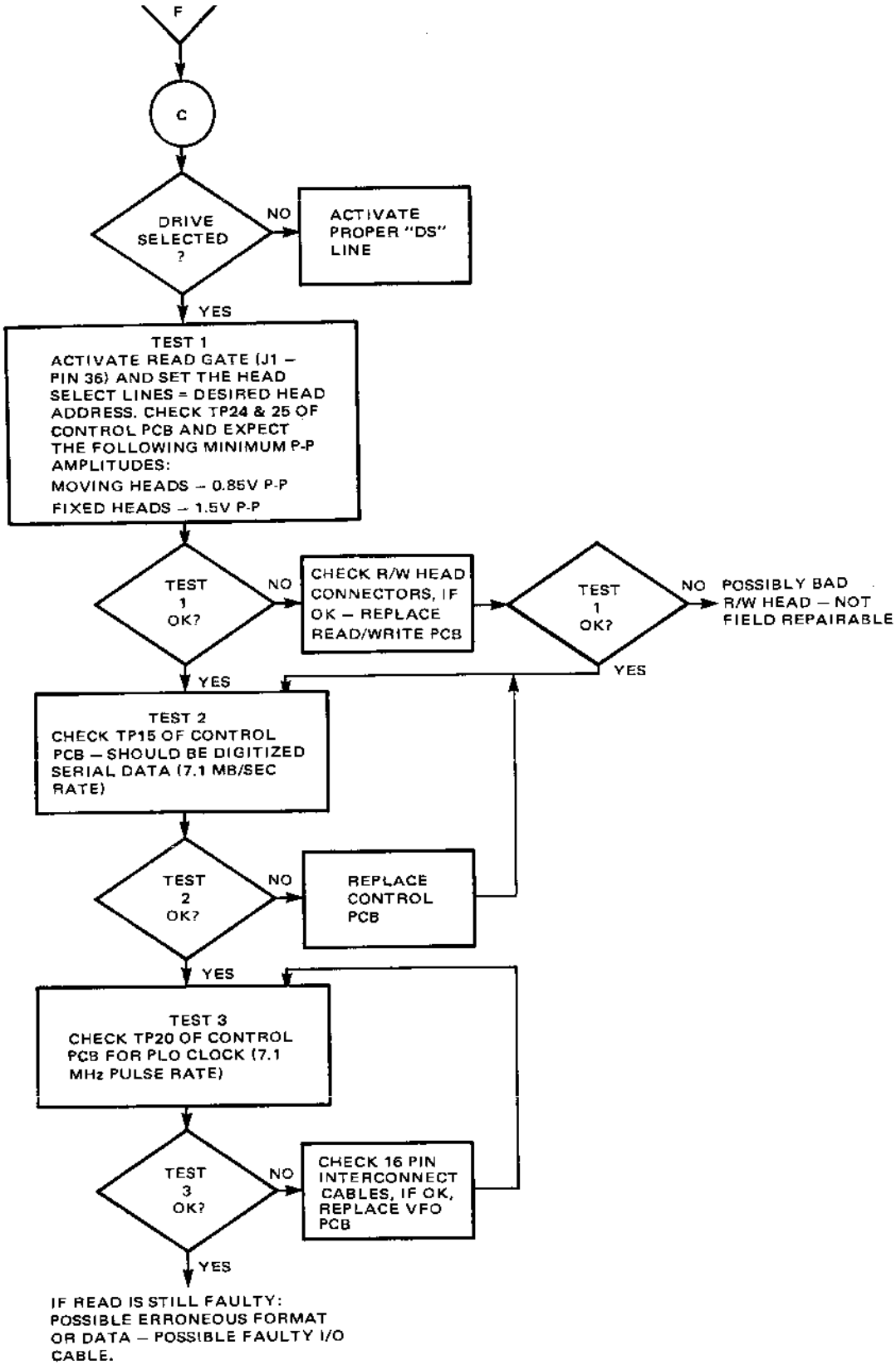
1. DRIVE MUST BE "SELECTED" AND "READY" IN ORDER TO STEP TO TRACK 00.
2. TRACK 00 AT THE J1 CABLE IS ONLY ACTIVE WHEN PHASE "A" OF THE ACTUATOR MOTOR IS ACTIVATED (AFTER POWER UP)
3. TRACK 00 IS THE OUTERMOST DATATRACK



DRIVE DOES NOT READ

PRELIMINARY NOTES:

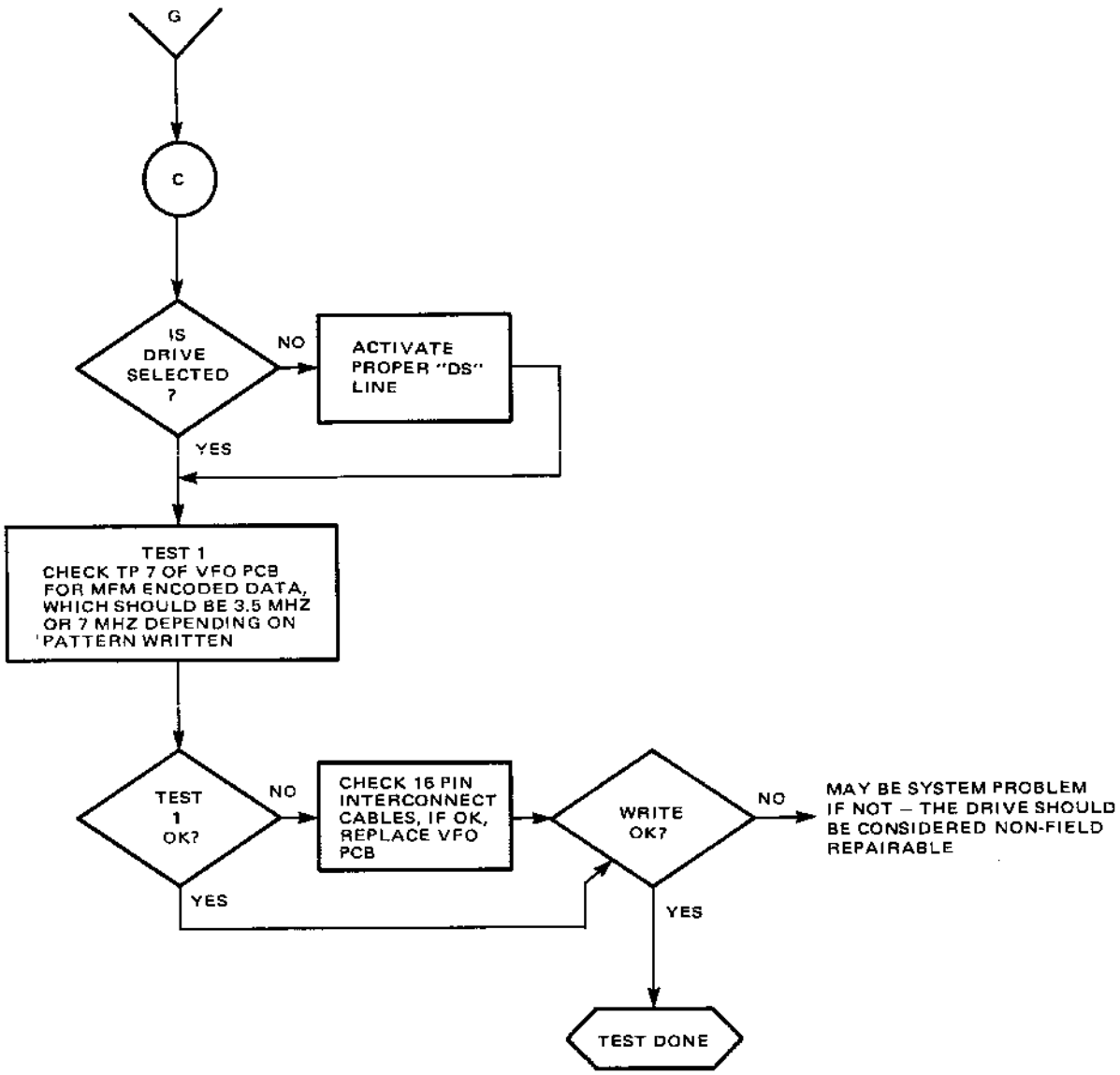
1. FOR THESE TESTS, THE READ/WRITE HEADS SHOULD BE POSITIONED AT CYLINDER 201. AND A DATA PATTERN OF ALL ZERO'S ORONE'S SHOULD BE WRITTEN TO ALL READ/WRITE HEADS.



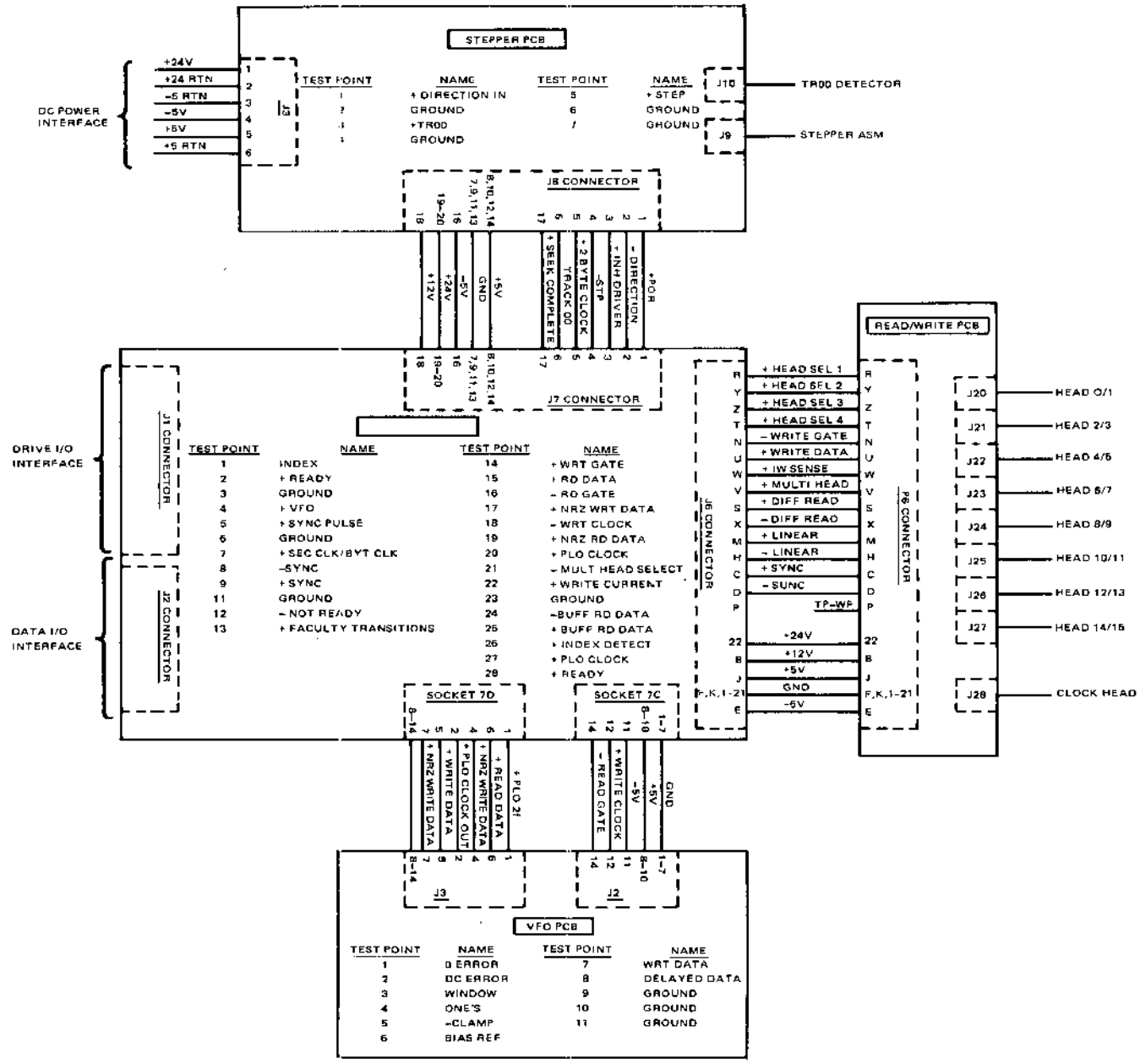
DRIVE DOES NOT WRITE

PRELIMINARY NOTES:

1. WRITE GATE MUST BE ACTIVATED FOR THE FOLLOWING TESTS.

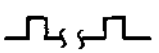
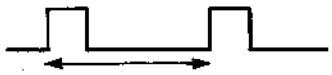
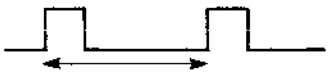
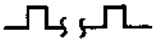


4.0 TEST POINTS AND PIN LOCATIONS



SA4000 INTERCONNECT DIAGRAM

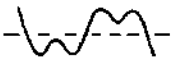
Test Points — **CONTROL BOARD**

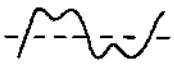
1. INDEX  20 msec period, 1.1 μs pulse width
2. LOGIC 1 = READY, LOGIC 0 = NOT READY
3. GND
4.  2.2 μsec period (PLO clock derivative)
5.  2.2 μsec period (digitized clock track)
6. GND
7. Sector Count or Byte Clock e.g., 32 sector =  600 μsec period, 1.1 μs pulse width
8. + SYNC  2.2 μsec
9. - SYNC  2.2 μsec
10. GND
11. GND
12. ↓ = NOT READY ↑ READY
13. NOT READY or READ·WRITE fault condition = ↑ no fault = ↓
14. WRITE GATE · READY · DRIVE SELECT ↓ = Writing ↑ Reading
15.  digitized read data
16. READ GATE · DRIVE SELECT ↓ = READING ↑ = WRITING
17. WRITE DATA  BIT CELL PERIOD = 140 nsec
18. WRITE CLOCK  PLO CLOCK = 140 nsec PERIOD
19. NRZ READ DATA  BIT CELL PERIOD = 140 nsec
20. PLO CLOCK  PLO CLOCK = 140 nsec PERIOD

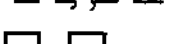
21 MULTI HEADS selected = ↓

22 MULTI HEADS · $\overline{\text{WRITE CURRENT}}$ = ↑

23 GND

24 -DIFF READ 1F  1V 140 nsec – rides on a 2 volt level

25 +DIFF READ 1F  1V 140 nsec – rides at 0 volts

26 INDEX DETECT  20 msec period, 1.1 μs pulse width

27 PLO 2F  70 nsec

28 READY = ↑

STEPPER BOARD

1 DIRECTION IN – ↑ OUT = ↓

2 GND

3 TK00 detected = ↑

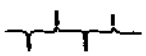
4 GND

5 STEP CLOCK  0.5 to 1.0 msec rate while stepping

6 GND

7 GND

VFO BOARD

1  intermediate VCO correction signal

2 DC error – typical VCO correction signal NRZ 1F = 280 nsec

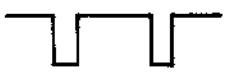
3  VFO data window

4  decoded read data

5 CLAMP VCO ↑ = clamped after 5 bits of data

6 DC ERROR 

7 MFM WRITE DATA 1F =  280 nsec

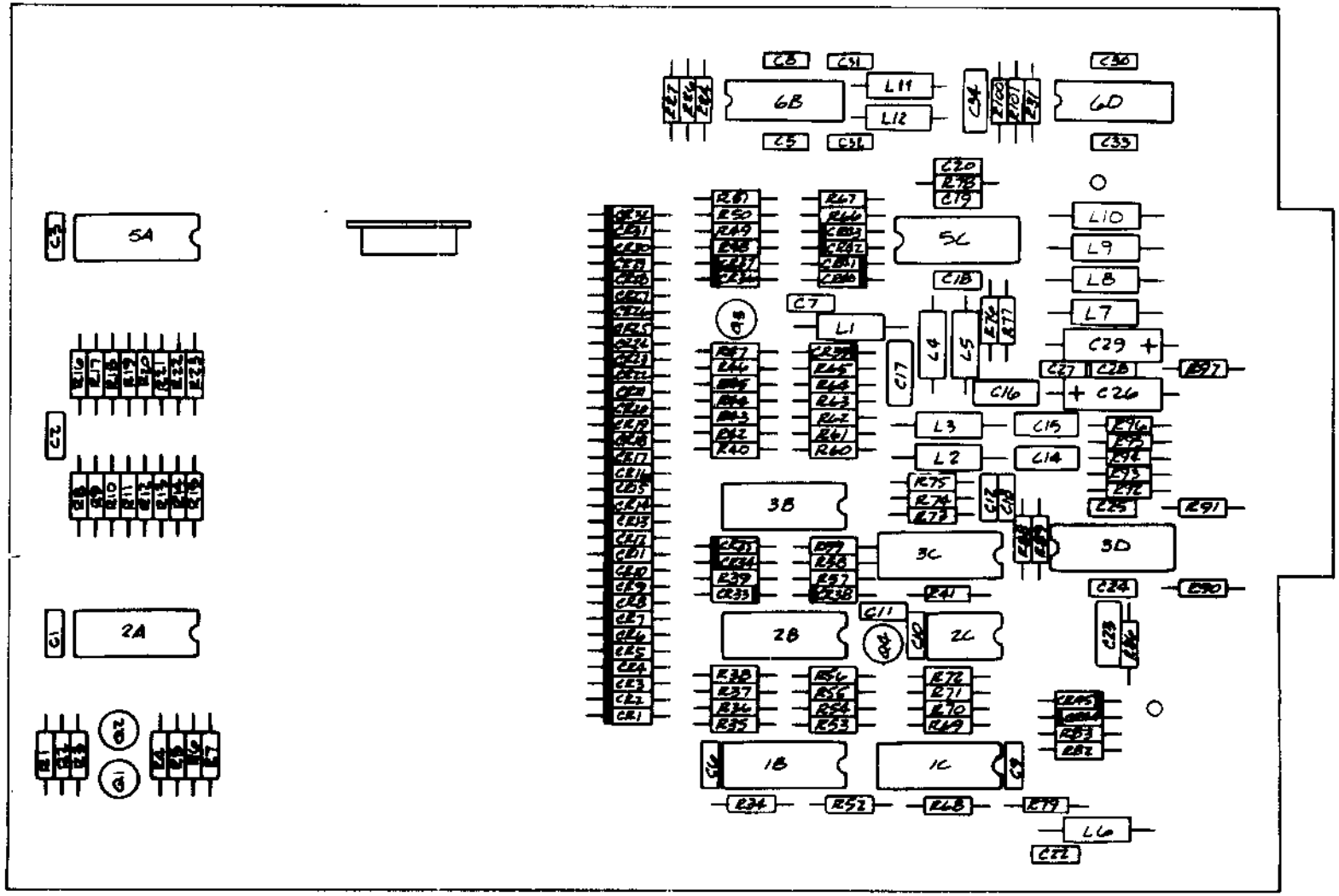
8  1F 280 nsec data window

9 GND

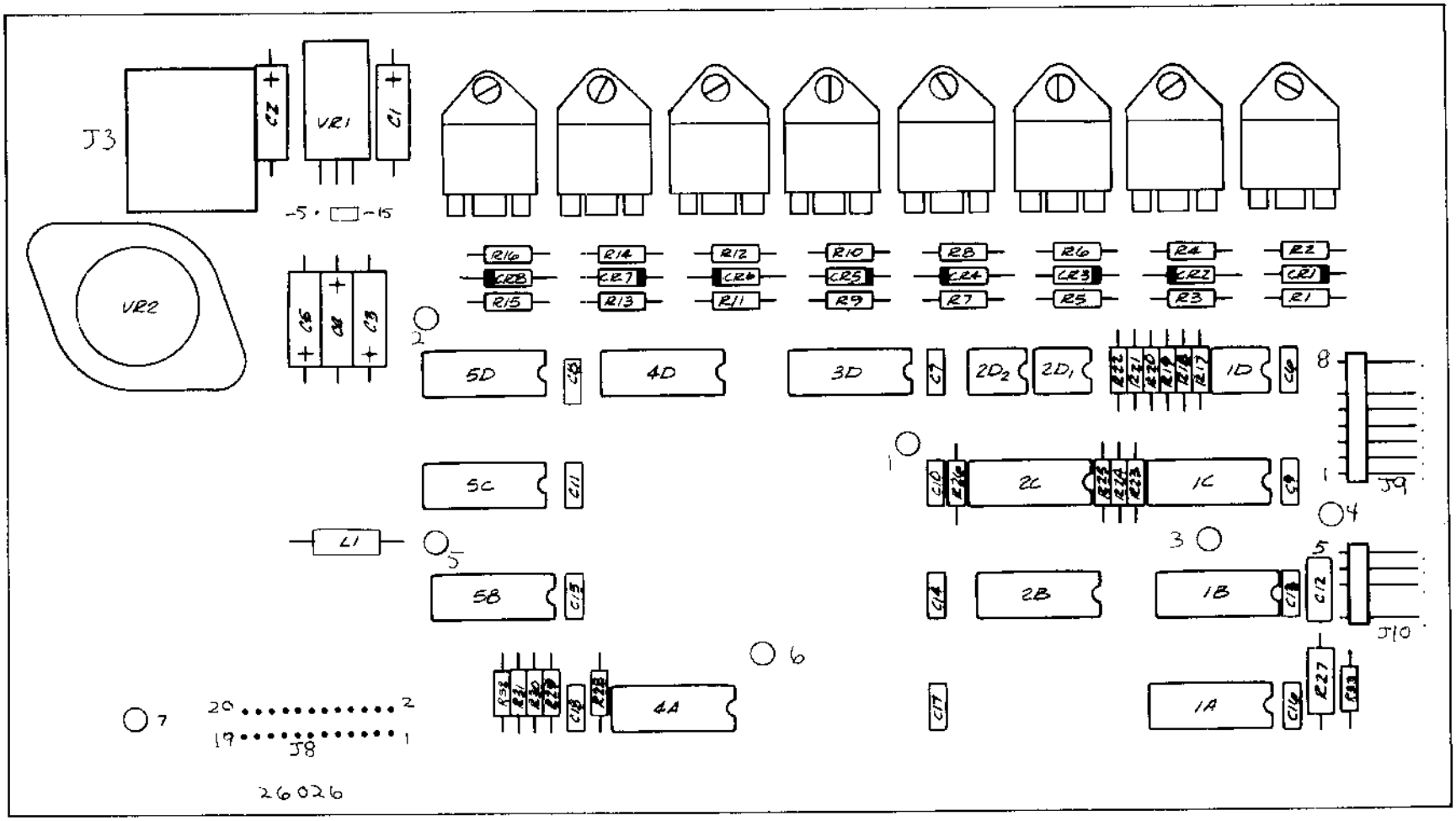
10 GND

11 GND

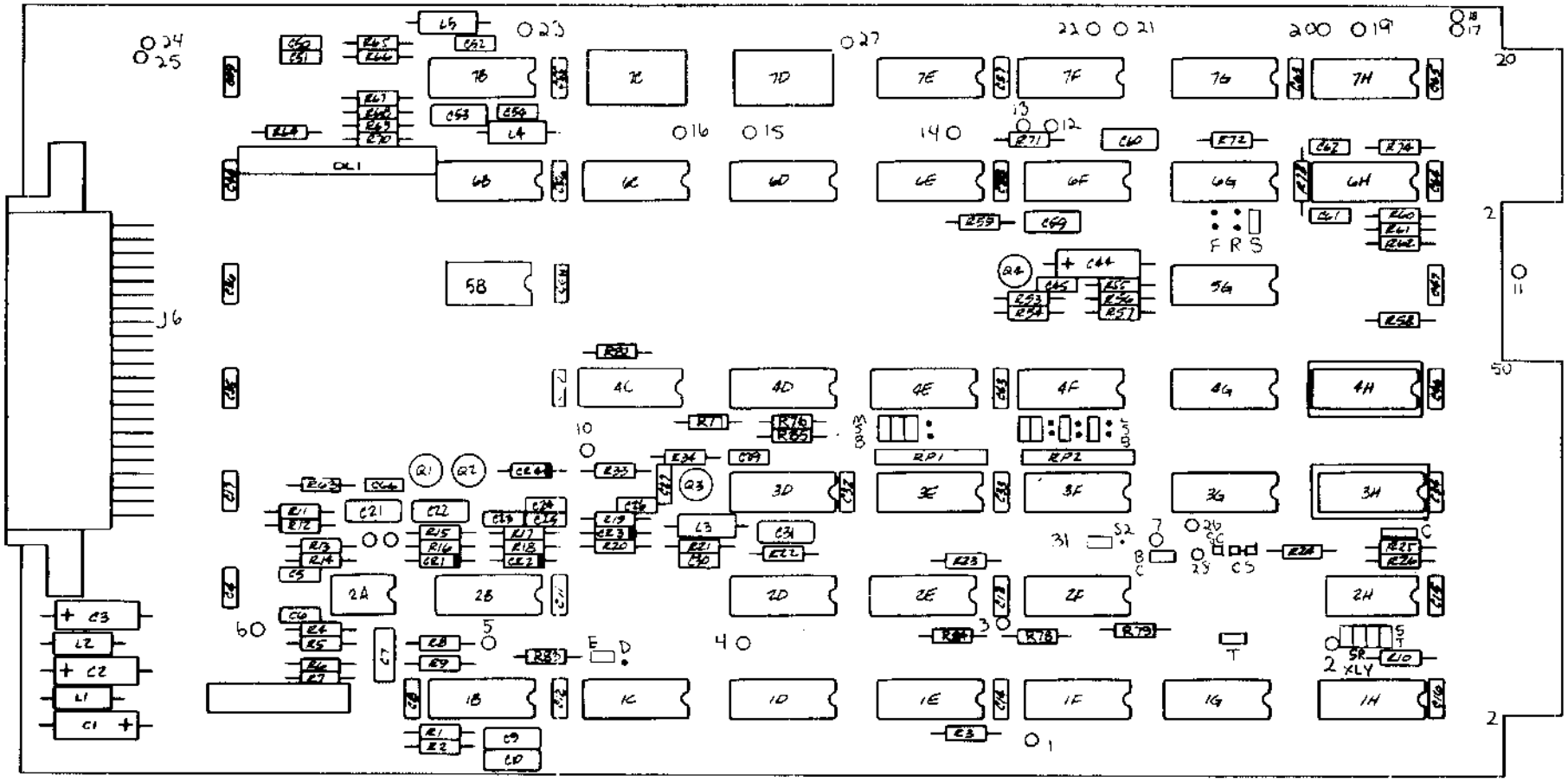
5.0 PCB COMPONENT LOCATIONS



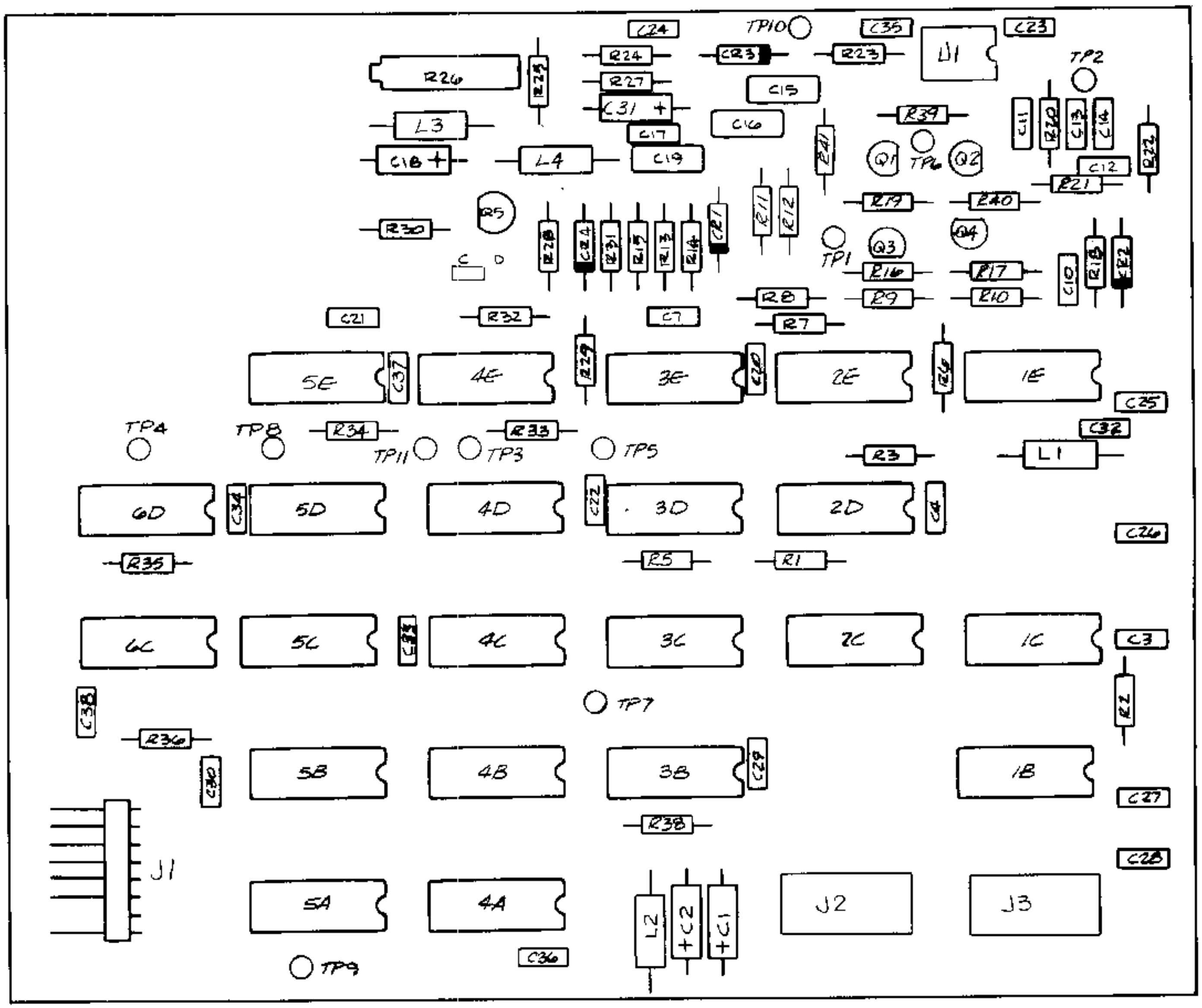
READ/WRITE PCB


J3
C2
VR1
C1
-5 • □ -15
VR2
C6
C4
C3
R16
CR8
R15
R14
CR7
R13
R12
CR6
R11
R10
CR5
R9
R8
CR4
R7
R6
CR3
R5
R4
CR2
R3
R2
CR1
R1
5D
C16
4D
3D
C7
2D2
2D1
R22
R21
R20
R19
R18
R17
1D
C4
8
J9
5C
C11
2C
C10
C6
R24
R23
1C
C9
4
L1
5
3
5B
C15
C14
2B
1B
C8
C12
5
J10
6
4A
C13
R28
C18
C17
1A
C16
R27
R26
7
20
2
19
1
J8
26026

Stepper PCB



Control PCB


C24
TP10
C35
C23
U1
TP2
R24
CR3
R23
R26
R27
C15
C31
C16
L3
C17
R39
L4
C19
C18
R30
Q1
TP6
Q2
R19
R40
R21
C12
TP1
Q3
Q4
R16
R17
R8
R9
R10
R7
C21
R32
C7
5E
C37
4E
3E
2E
1E
C25
C32
TP4
TP8
R34
R33
TP11
TP3
TP5
R3
L1
6D
C34
5D
4D
C22
3D
2D
C4
C26
R35
R5
R1
6C
5C
4C
3C
2C
1C
C3
TP7
C38
R36
C30
5B
4B
3B
C29
1B
C27
R38
C28
J1
5A
4A
L2
C2
C1
J2
J3
TP9
C36

VFO PCB

6.0 SCHEMATIC DIAGRAMS

PART NO. 26022-1

+HEAD SEL 1 — R
+HEAD SEL 2 — Y
+HEAD SEL 4 — Z
+HEAD SEL 8 — T
+HEAD SEL 8 XS210

BCD/DEC 2A

- HEAD C.T. ϕ
- HEAD C.T. 1
- HEAD C.T. 2
- HEAD C.T. 3
- HEAD C.T. 4
- HEAD C.T. 5
- HEAD C.T. 6
- HEAD C.T. 7

R9 10K, R8 10K, R11 10K, R10 10K, R13 10K, R12 10K, R14 10K, R15 10K

BCD/DEC 5A

- HEAD C.T. 8
- HEAD C.T. 9
- HEAD C.T. 10
- HEAD C.T. 11
- HEAD C.T. 12
- HEAD C.T. 13
- HEAD C.T. 14
- HEAD C.T. 15

R16 10K, R17 10K, R19 10K, R18 10K, R21 10K, R20 10K, R22 10K, R23 10K

+24VA — Q4 2N2907A — R72 390 — C11 .01 — R45 20 — R44 100 — R34 2K — R65 4.7K — R35 20K — R53 1K — CR45 — CR44 — R82 510 — R70 2K — R71 100 — CR39 1N52318 6.1V ±5% — R43 1K

+5V — R69 2K — R41 1K — R52 2K — R42 4.7K — R68 2K

- WRITE GATE — N
+ WRITE DATA — U

R37 2K, R65 2K — R56 100 — R54 470 — CR38 — R57 100 — R38 100 — R36 470 — CR33 — R39 100 — R61 100 — R60 100 — R79 6.2K

R64 274 1/8W 1%, R63 274 1/8W 1%, R62 931 1/8W 1% — R40 510 — CR35 — CR34 — R58 10K — R59 10K — -5V

P — TP-WF
+FIXED HEAD XS210
W — + IW SENSE
+ MATRIX XS210
- MATRIX XS210
V — + MULTI HEAD

R2 510 — +24VA — R3 510 — R1 100 — Q1 2N2907 — R4 10K — C2 .01 200V 10% — R5 1K — R6 100 — Q2 2N2222A — R7 2K — R83 2K

+24V — L6 22 — C22 0.1 — +24VA
+12V — L10 22 — +12VA
+5V — C26 4.7 10% — C1,3,6,9,10,28 0.1 — +5V
GND — F,K 1-21
-5V — C29 4.7 10% — C27 0.1 — -5V — L7 22 — -5VA

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80 -20%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. ALL INDUCTORS ARE IN MICROHENRIES.
4. ALL DIODES ARE IN4148.
5. CONNECTOR REFERENCE SYMBOL: * = P6, (20) = J20 THRU (28) J28.
6. COMPONENTS NOT INSTALLED ON ASSEMBLY NUMBER 26023-0.

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GND (PIN)
7406	1C		14	7
7445	2A, 5A		16	8
74S74	1B	1B2	14	7
75452	2C		8	4
592	30, 5C, 6B, 60		—	—
Q2T2222	2B, 3C		—	—
Q2T2905	3B		—	—

REFERENCE DESIGNATIONS

LAST USED	NOT USED
C34	C4, 21
CR47	
L12	
Q6	
R102	R25, 28-30, 32, 33, 80, 98, 99

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SPERRY ASSOCIATES	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE SCHEMATIC DIAGRAM — READ/WRITE	
		5-76	3046		
CASE DEPTH	LINEAR ±.XX ±.XXX	7-78	3067	DETAIL JWD 3-8-78	RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR ±	10-78	3085	DESIGN	T26022
SURFACE TREATMENT ES	CORNERS (EDGES) BROKEN OUTSIDE MAX. INSIDE MAX.			APPRO 5/78	SHEET 1 OF 2
				D SCALE —	DOC CODE SC PART NO. 26022-1 REV/EC 3085

XS200

26022-1

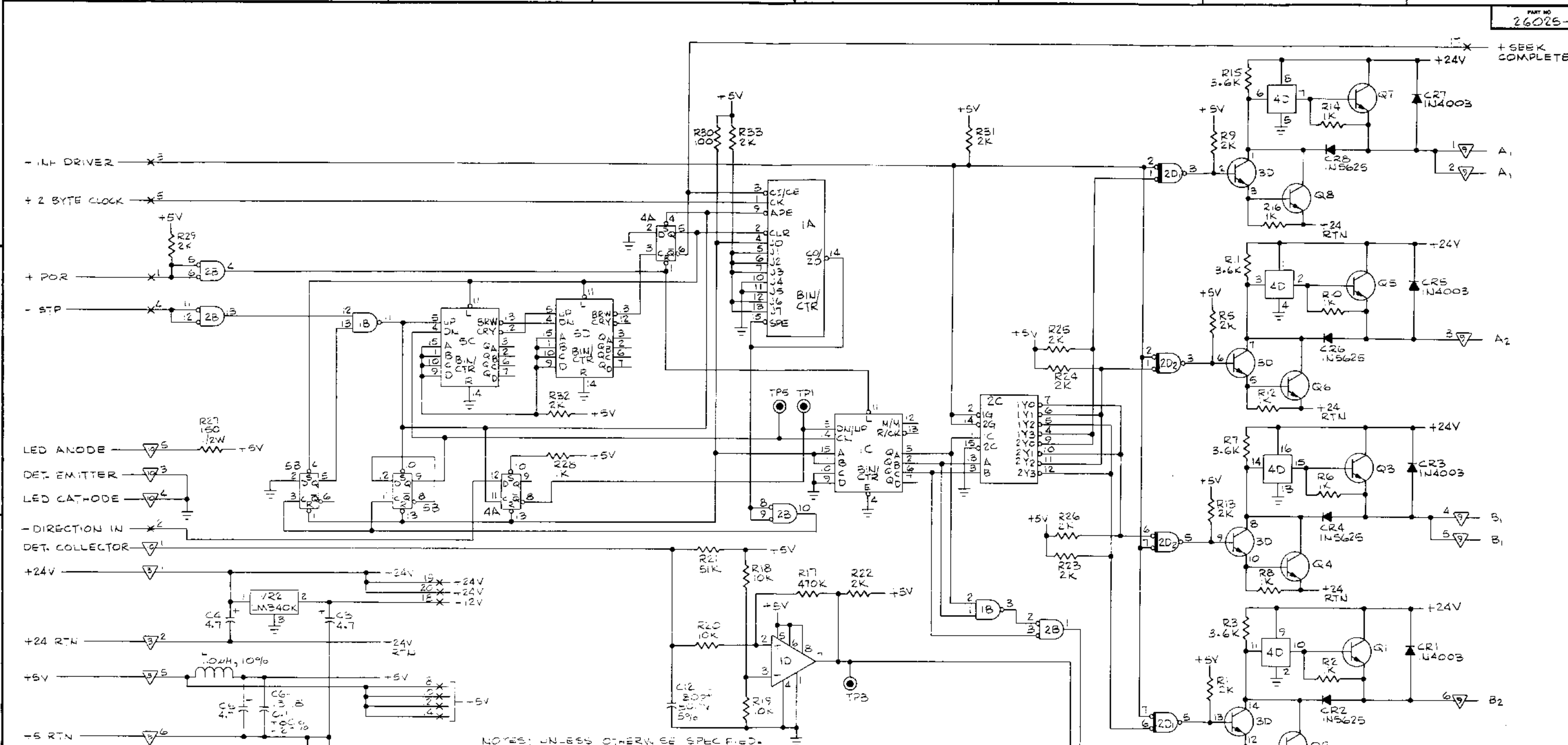
- MATRIX X5200
+ MATRIX X5200
HEAD Ø
HEAD 1
HEAD 2
HEAD 3
HEAD 4
HEAD 5
HEAD 6
HEAD 7
HEAD 8
HEAD 9
HEAD 10
HEAD 11
HEAD 12
HEAD 13
HEAD 14
HEAD 15
CR4 CR3 CR2 CR1 CR8 CR7 CR6 CR5 CR12 CR11 CR10 CR9 CR16 CR15 CR14 CR13 CR20 CR19 CR18 CR17 CR24 CR23 CR22 CR21 CR28 CR27 CR26 CR25 CR32 CR31 CR30 CR29
+ FIXED HEAD X5200
R46 4.7K
R47 1K
Q3 2N2907A
L1 22
+12V
C7 0.1
+HEAD SELECT B X3200
CLOCK 1
CLOCK CT
CLOCK 2
CR36 CR37 CR40 CR41
R48 680
R49 2K
R50 2K
R51 10K
L8 22
-5V
R67 1.6K
R66 1.6K
CR43 CR42
+5V
L9 22
C19 0.1
5C
C20 .047 10%
R78 18
C18 0.1
R77 453 1/8W 1%
R76 453 1/8W 1%
L5 6.8
L4 6.8
C16 51pf 500V
C17 51pf 500V
L2 15
L3 15
C14 150pf 500V
C15 150pf 500V
R75 909 1/8W 1%
R74 100
R73 100
3C
C12 .01 200V 10%
C13 .01 200V 10%
R96 270
R95 270
R92 100
R91 100
R90 100
R97 100
M + LINEAR
9 + DIFF READ
X - DIFF READ
H - LINE
C25 0.1
R88 510
R94 1K
R89 510
R93 1K
3D
C23 30pf 500V 5%
R86 120
C24 0.1
R84 1K
Q6 2N4393
R87 20K
R85 100K
R81 2K
R102 2K
CR46
Q5 2N2907A
+12VA
CR47 IN5221B 2.4V
R27 10K
R26 10K
R24 430
C8 0.1
6B
C31 0.1
C32 0.1
L11 100
L12 100
C34 24pf 500V 5%
R100 825 1/8W 1%
R101 825 1/8W 1%
-5VA
C5 0.1
6D
C30 0.1
R31 510
C33 0.1
C -SYNC
D +SYNC

XS210

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ±.XX ±.XXX
ANGULAR ±
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
CORNERS EDGES BROKEN
OUTSIDE MAX
INSIDE MAX

EC HISTORY
DATE NO.

SHUGART ASSOCIATES
TITLE SCHEMATIC DIAGRAM — READ/WRITE
DETAIL JWG 3/8/78 RELEASED FOR ASSEMBLY
DESIGN T26022
APPRO 5/78 SHEET 2 OF 2
SCALE
D
ENG CODE SC
PART NO. 26022-1
REVISE 3085



NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, 10%.
2. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. ALL TRANSISTORS ARE TIP-33.
4. CONNECTOR REFERENCE SYMBOL: ✱=J6; (3)=J3; (9)=J9; (10)=J10.
5. —□ □— INDICATES JUMPER OPTION.
6. [6] SHORTING PLUG INSTALLED.

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GND (PIN)
7400	1B	1B3	14	7
74LS02	2B		14	7
7474	4A, 5B		14	7
74156	2C		16	8
74191	1C		16	8
74193	5C, 5D		16	8
75453	2D1, 2D2		8	4
LM311	1D		8	1
2074B	4D		–	–
40103	1A		16	8
2GT2222	3D		–	–

REFERENCE DESIGNATIONS

LAST USED	NOT USED
C6	
CR8	
...	
VR2	

x5100

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY		SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE …MAT… DIAGRAM
CASE DEPTH	LINEAR ±.XX ±.XXX			DETAIL — RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR ±			DESIGN
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX			APPRO 3/76 SHEET 1 OF 1
				D SCALE — DOC CODE SC PART NO. 26025-0 REV/EC

PART NO. 26028-0

- DRIVE SELECT 1
- DRIVE SELECT 2
- DRIVE SELECT 3
- DRIVE SELECT 4
- SEEK COMPLETE XS330
- TRACK ØØ
- DIRECTION
- HEAD SELECT 8
- HEAD SELECT 1
- HEAD SELECT 4
- HEAD SELECT 2
+READY XS330
+BLOCK WRITE XS310
- WRITE GATE
- STEP
- READ GATE
+ WRITE CLOCK XS310
+IW SENSE
- FAULT CLEAR
- POR XS320
- READY XS330

+SELECT XS310 XS330
- TRACK ØØ
- DIRECTION IN
+ HEAD SEL 1
+ HEAD SEL 2
+ HEAD SEL 4
+ HEAD SEL 8
+ INH DRIVER
- WRITE GATE
- STP
- READ • WRITE XS310
+ SEL WRITE GATE XS310
- WRITE CURRENT XS310
- CLEAR XS310
- NOT READY XS310

+24VDC
+12VDC
+5VDC
GND
-5VDC

+24V
+12VDC
+12V
+5V
GND
-5VDC

XS300

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C68	C18-20, 28, 37-42
CR4	
L5	
Q4	
R85	R27-32, 35-62
TP28	TP10
E3	

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GND (PIN)
7400	5B, 1C, 6D, 7G	5B2,3,4; 6D3,4	14	7
7402	6F, 4G		14	7
7404	7E	7E5	14	7
74LS02	3F		14	7
74S04	3D, 2F	3D5; 2F1,3,4	14	7
7406	5G		14	7
7410	6E		14	7
7414	3G		14	7
7438	6G, 1H, 2H	2H1	14	7
7440	1F	1F1	14	7
7474	2B, 6C, 1D, 2D, 1E, 3E		14	7
74LS74	5E	5E1	14	7

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GND (PIN)
74S86	6B		14	7
74LS193	4D, 2E		16	8
74195	1G		16	8
74279	7F		16	8
75114	7H		16	8
75115	6H		16	8
8T20	7B		-	8
LM311N	2A		-	-
9602	1B		16	8
40103B	4A,4B,4C,4E,4F		16	8
220/330	3H		14	7

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
LINEAR ±.XX ±.XXX
ANGULAR ±
CORNERS EDGES BROKEN
OUTSIDE MAX
INSIDE MAX

EC HISTORY

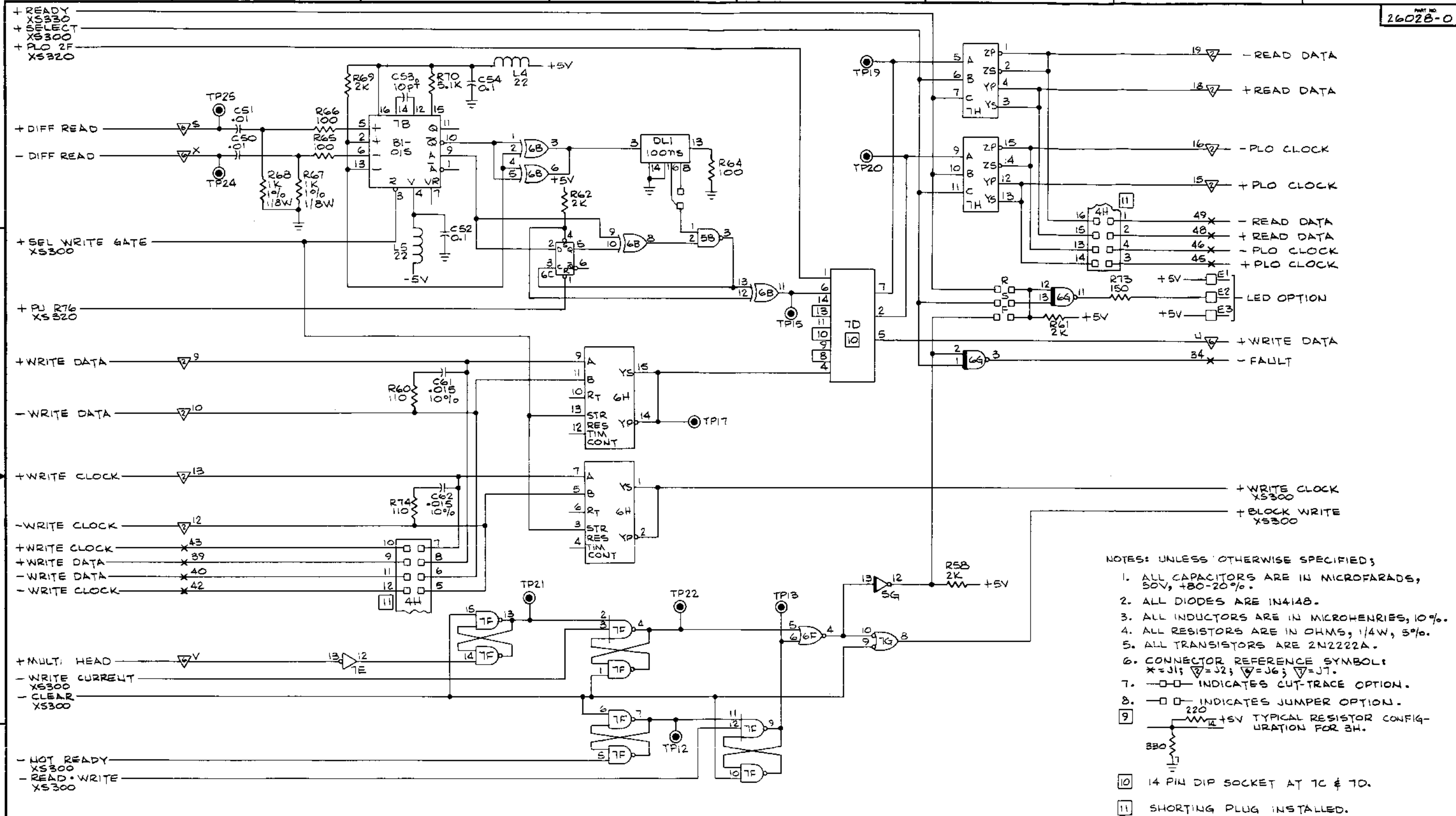
DATE	NO.
5-78	3046
7-78	3060
8-78	3074

SHUGART ASSOCIATES

TITLE SCHEMATIC DIAGRAM CONTROL

DETAIL	JWE	4-78	RELEASED FOR ASSEMBLY
DESIGN			T26028
APPRO	WF	5/78	SHEET 1 OF 4

D | SCALE - | DOC CODE SC | PART NO. 26028-0 | REV/EC 3074



NOTES: UNLESS OTHERWISE SPECIFIED;

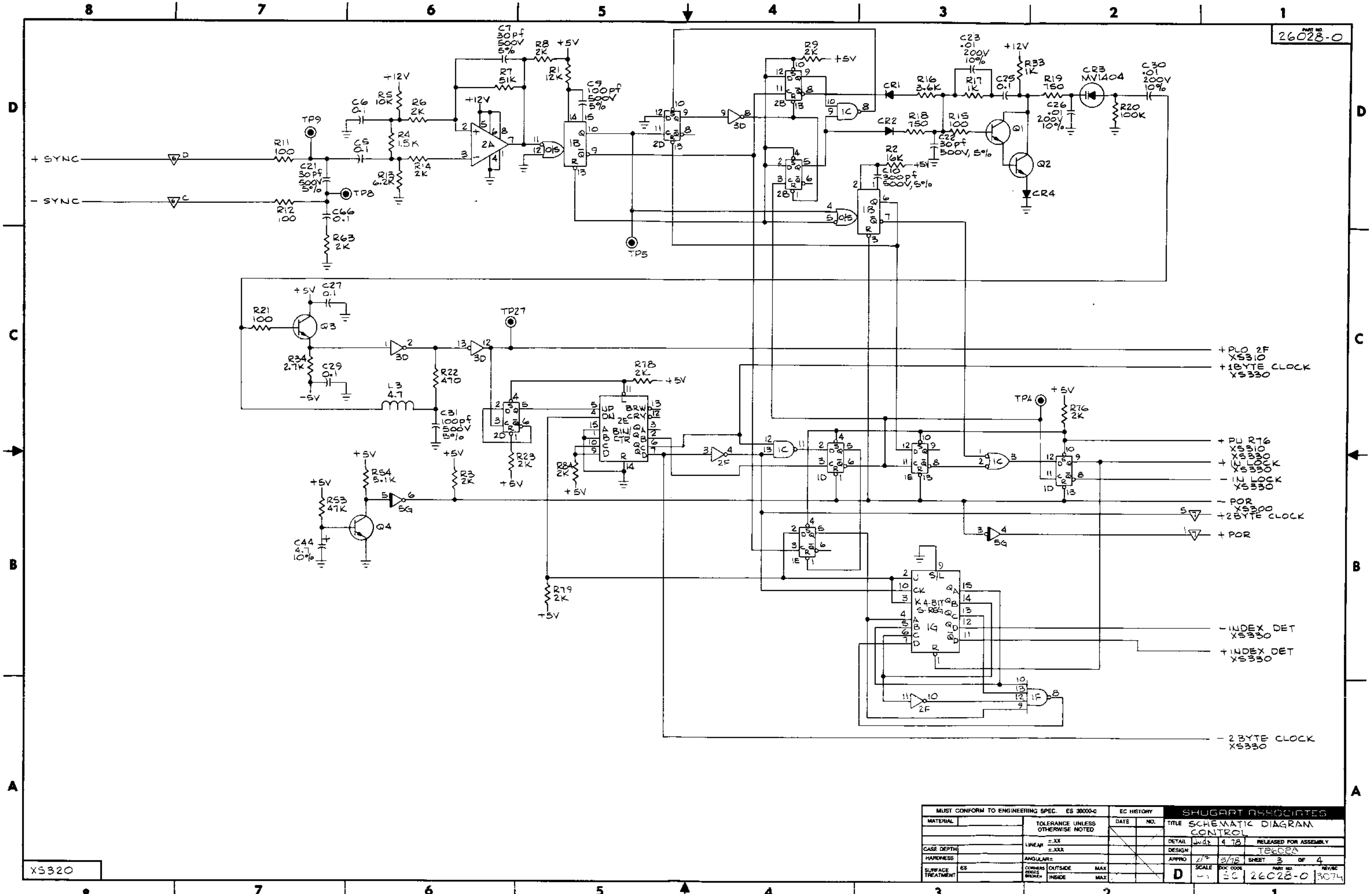
1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80-20%.
2. ALL DIODES ARE IN4148.
3. ALL INDUCTORS ARE IN MICROHENRIES, 10%.
4. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
5. ALL TRANSISTORS ARE 2N2222A.
6. CONNECTOR REFERENCE SYMBOL: ✱=J1; ②=J2; ⑥=J6; ⑦=J7.
7. —□-□— INDICATES CUT-TRACE OPTION.
8. —□ □— INDICATES JUMPER OPTION.

9 — 220, 14, +5V, 330, 7 — TYPICAL RESISTOR CONFIGURATION FOR 3H.

10 — 14 PIN DIP SOCKET AT 7C & 7D.

11 — SHORTING PLUG INSTALLED.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE / NO.	TITLE SCHEMATIC DIAGRAM CONTROL
CASE DEPTH	LINEAR ±.XX ±.XXX		DETAIL Judy 4-78 RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR ±		DESIGN TP6028
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX		APPRO 5/78 SHEET 2 OF 4
			D SCALE — DOC CODE SC PART NO. 26028-0 REV/EC 3074



MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE / NO.	TITLE SCHEMATIC DIAGRAM CONTROL
CASE DEPTH	LINEAR ±.XX ±.XXX		DETAIL Judy 4/78 RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR±		DESIGN T86028
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX		APPRO 5/78 SHEET 3 OF 4
			D SCALE DOC CODE PART NO. 26028-0 REV/EC 3074

26028-0

XS320

PART NO. 26028-0

SECTOR COUNTER OPTION

+1BYTE CLOCK XS320

+INDEX DET XS320

-INDEX DET XS320

+SELECT XS300

+IN LOCK XS320

+PU RTG XS320

-2 BYTE CLOCK XS320

+SEEK COMPLETE

-IN LOCK XS320

USER INSTALLABLE OPTION

-SEEK COMPLETE

-SEEK COMPLETE XS300

-READY

-INDEX

-READY

-INDEX

-BYTE CLOCK

-BYTE CLOCK

-READY XS300

+READY XS300 XS310

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY	SHUGART ASSOCIATES
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE / NO.	TITLE SCHEMATIC DIAGRAM CONTROL
	LINEAR ±.XX ±.XXX		DETAIL Judd 4-78 RELEASED FOR ASSEMBLY
CASE DEPTH	ANGULAR ±		DESIGN TP&CS
HARDNESS			APPRO 5/78 SHEET 4 OF 4
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX		SCALE — DOC CODE SC PART NO. 26028-0 REV/EC

XS330

PART NO. 26033-0

- READ GATE
+VFO IF XS410
+PLO IF XS410
+PLO 2F
+READ DATA
+VCO 2F XS410
+5V
GND
-5V
KEY
N.C.
+5VA
-5VA

- LOCK TO DATA XS410
+PLO CLOCK
-GATED PLO 2F XS410
+ENABLE DATA XS410
+PULL UP 2 XS410
-CLAMP VCO XS410
-DELAYED DATA XS410
DC ERROR XS410

TP1
TP2
TP5
TP6
TP9, 10, 11

XS400

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80-20 %.
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
3. ALL INDUCTORS ARE IN MICROHENRIES, ±10 %.
4. CONNECTOR REFERENCE SYMBOL: ▽=J1; ▽2=J2; ▽3=J3.
5. —□□— INDICATES CUT TRACE OPTION.
6. —□ □— INDICATES JUMPER OPTION.
7. [7] SHORTING PLUG INSTALLED.

REFERENCE DESIGNATIONS

LAST USED	NOT USED
C38	C5, 6, 8, 9
CR4	
L4	
Q5	
R41	R4, 37
TP11	

TYPE	POSITION	UNUSED ELEMENTS	VCC (PIN)	GND (PIN)
74S00	1C, 2C, 5D, 3E, 5E	2C1, 5D2, 3, 4, 3E1, 4	14	7
74S04	4C, 4D	4D5, 6	14	7
74S64	4A, 5A, 4B, 5B, 1E		14	7
74S86	3C		14	7
74S112	6C, 2D, 6D, 2E, 4E		16	8
74S175	1B, 5C		16	8
741	U1			
DLYLN	3B, 3D		—	—

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ±.XX ±.XXX
ANGULAR ±
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
COMMON EDGES BROKEN OUTSIDE MAX INSIDE MAX

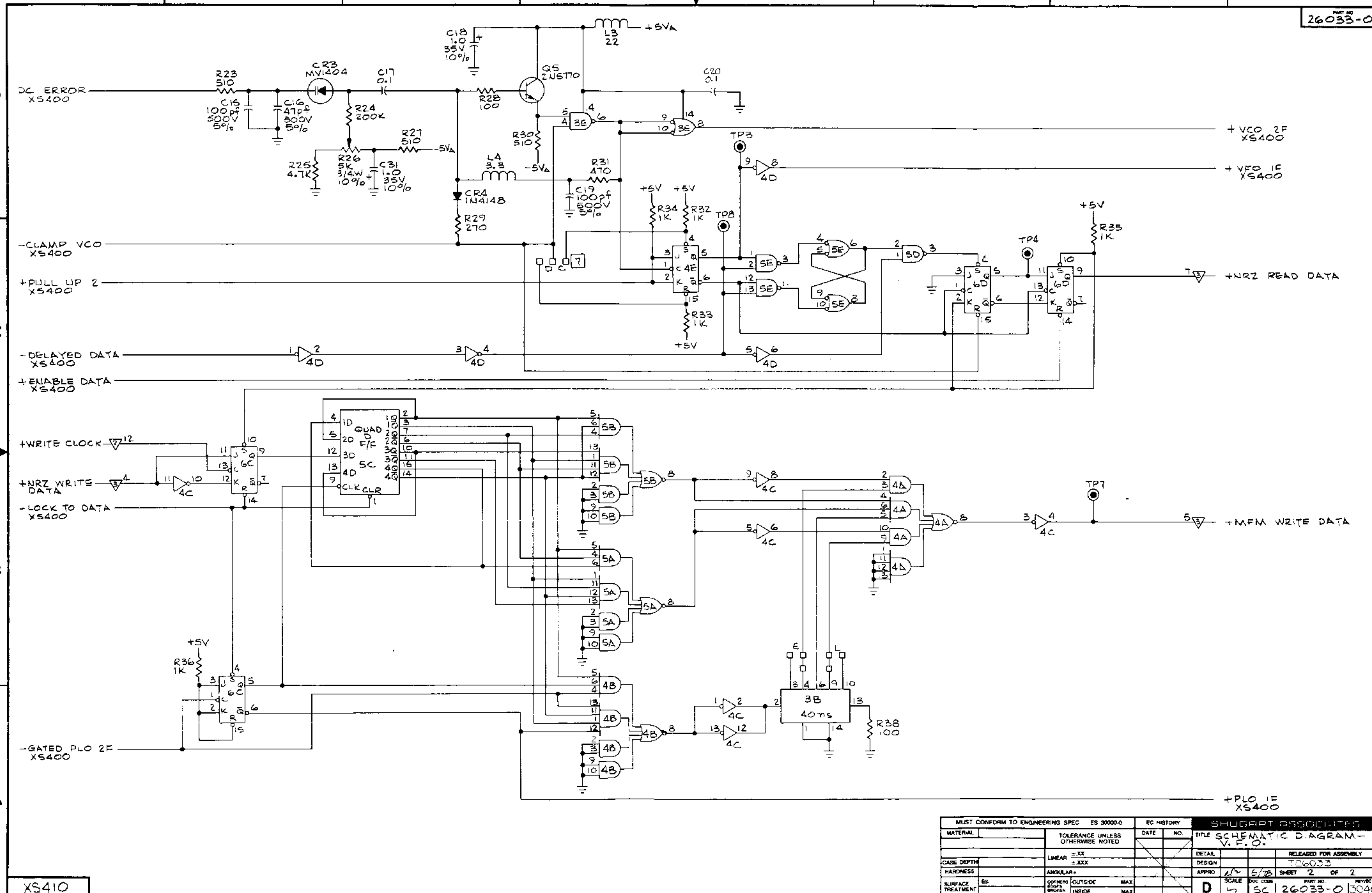
EC HISTORY

DATE	NO.
5-78	3046

SHUGART ASSOCIATES

TITLE SCHEMATIC DIAGRAM — V.F.O.

DETAIL JWS 2/78 RELEASED FOR ASSEMBLY
DESIGN T26033
APPRO 5/78 SHEET 1 OF 2
D SCALE 4 DOC CODE SC PART NO. 26033-0 REVISE 3046



MUST CONFORM TO ENGINEERING SPEC ES 30000-0

TOLERANCE UNLESS OTHERWISE NOTED

SHUGART ASSOCIATES

TITLE SCHEMATIC DIAGRAM - V. F. O.

RELEASED FOR ASSEMBLY

SHEET 2 OF 2

D | SC | 26033-0 | 3046

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