SA1403D Controller

OEM Manual

Shugart

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

The SA1403D Controller consists of a micrprocessor based controller with on-board data separator logic and is able to control a maximum of four drives. The drives can be any combination of Shugart SA1000 fixed disk drives, SA800 floppy disk drives, or SA850 floppy disk drives. The floppy disk track formats are compatible with IBM 1D/2D track formats. The SA1403D can be mounted on the SA1000 drive.

Commands are issued to the controller over a bidirectional bus connected to the host computer. The data separator/"serdes" logic serializes bytes and converts to FM/MFM data, and deserializes FM/MFM data into 8-bit bytes.

Due to the microprogrammed approach utilized in the controller, limited diagnostic capabilities are implemented. This methodology increases fault isolation efficiency and reduces system down time. Error detection and correction will tolerate media imperfections up to 4-bit burst errors.

1.1 SA1403D CONTROLLER FEATURES

OVERLAPPED SEEK	In multiple drive configurations the host can issue seeks to different drives without waiting for the first drive to complete its seek.
AUTOMATIC SEEK AND VERIFY	A seek command is implied in every data transfer command (READ, WRITE CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated and a cylinder verification is performed after the seek completes.
FAULT DETECTION	Three classes of fault detection are provided for fault diagnosis: 1) Disk related faults. 2) Controller related faults. 3) Host command or I/O timing faults. Fault detection is available from the interface as a status message and is also visibly displayed on a row of status LED's on the controller PCB.
AUTOMATIC HEAD AND CYLINDER SWITCHING	If during a multi-block data transfer the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.
DATA ERROR SENSING AND CORRECTION	If a data error is detected during a disk data transfer, the controller indicates whether or not it is correctable. If correctable, it can be automatically corrected. (This applies to the SA1000 only. CRC error detection is used on floppy disc drives.)
LOGICAL TO PHYSICAL DRIVE CORRELATION	Logical Unit Number (LUN's) are independent of physical port numbers. All accesses specify LUN's.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.
EFFICIENT HOST INTERFACE PROTOCOL	A bidirectional bus between the controller and host provides a simple, yet efficient communication path. In addition, a high level command set permits effective command initiation.
SECTOR INTERLEAVE	Sector interleaving is programmable with up to a 16 way interleave.
ODD PARITY	The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
FIXED SECTOR SIZE	The sector size is fixed at 256 bytes of data for the SA1000.

NUMBER OF DRIVES — The controller will connect to a maximum of four (4) drives. The drives can be any combination of SA1000's and/or SA850's and/or SA800's

1.1.1 OPTIONAL FEATURES

MICRO DIAGNOSTICS — A set of diagnostic PROM's are available to allow stand alone diagnostic testing of both drive and controller. Reference Appendix A.

1.1.2 SYSTEM CONFIGURATION

The controller and data separator comprise a single PCB that can be mounted onto the SA1000 drive. A maximum of four (4) drives may be connected as shown in Figure 2.

1.2 TRACK FORMATS AND CAPACITY

A) 32 sectors of 256 bytes per sector (SA1000only).
C) 26 sectors of 256 bytes per sector (Floppy only).
D) 26 sectors of 128 bytes per sector (Floppy only.)

IBM 1D/2D TRACK FORMAT — Track format for Floppy Disk drives can be selected under program control in real time. The track formats are:

1) Single density, single sided
2) Single density, double sided
3) Double density, single sided
4) Double density, double sided

	26 SECTOR	32 SECTOR
SA800	2001	N/A
SA850	4003	N/A
SA1002	N/A	16383
SA1004	N/A	32767

TABLE I.

Format/Capacity Relationship
Maximum Logical Sector Address Shown

2.0 SPECIFICATION SUMMARY

2.1 ENVIRONMENTAL LIMITS

	Operating	Storage
Temperature F/C	32°/0° to 131°/55°	-40°/-40° to 167°/75°
Max. Wet Bulb	85°F non condensing	
Relative Humidity	10% to 95%	10% to 95%
Altitude	Sea level to 10,000 ft	Sea level to 15,000 ft

2.2 POWER REQUIREMENTS

Three power supply voltages are required for the SA1400 series controllers. The maximum current requirements are as follows:

+5VDC ± 5% at 4.6 Amps
-5VDC ± 5% at 0.5 Amps
+24VDC ± 10% at 0.1 Amps

Power is applied to the SA1400 series controller via J10 which is a 6 pin AMP Mate-N-Lok connector (P/N 1-380999-0) mounted on the component side of the board. The recommended mating connector, P10, is an AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. The J10 pins are labeled on the connector. Figure 1 shows the pin assignments.

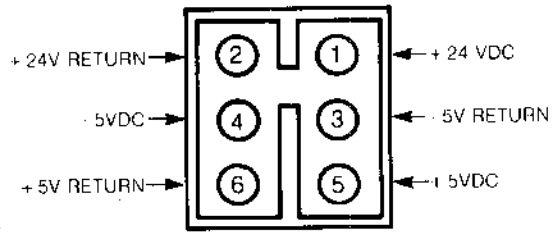


FIGURE 1. J10 DC POWER CONNECTOR

2.3 PHYSICAL PARAMETERS

Length:	13.7 inches (34.8cm) ± .030" (.076 cm)
Width:	8.25 inches (21cm) ± .010" (.025 cm)
Height:	0.5 inches (1.3cm) ± .030" (.076 cm)
Weight:	1.12 lbs (0.5Kg) ± .010 lbs (0.25 g)

3.0 SA1403D DISK DRIVE INTERFACE

Shugart SA1000 and SA800/850 disk drives are interfaced to the controller via J1, J2, J3, J4 and J5. Refer to Figure 2 for connection block diagram.

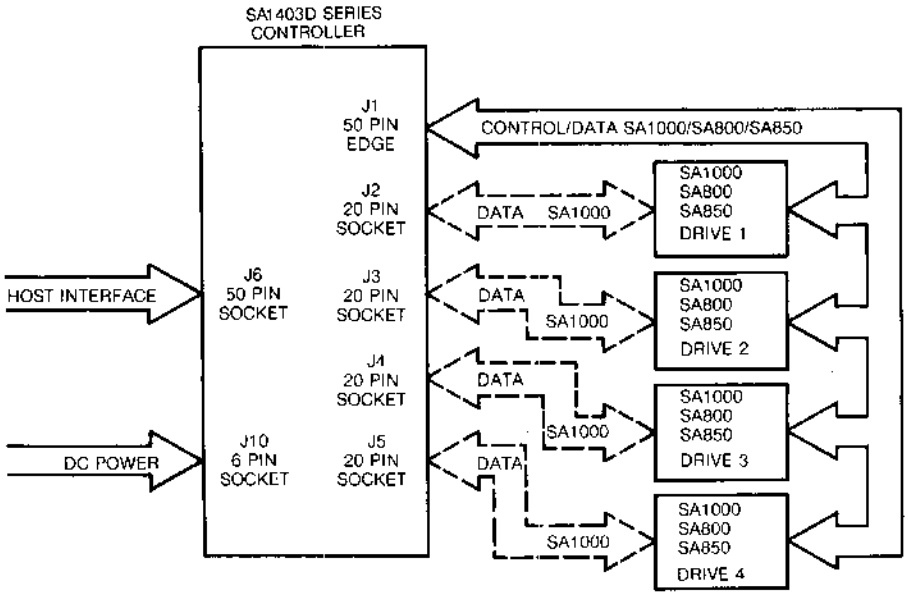


FIGURE 2. SA1403D INTERCONNECT DIAGRAM

NOTE: The last physical device on the control cable (drive to be terminated) must be an SA1000.

J1 is a 50 pin edge type connector which connects all drives in a daisy chain configuration. This connector carries control and data information for the floppy disk drives and control information only for the SA1000 disk drive. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J1 is a 3M Scotchflex ribbon connector P/N 3415-0001.

J2 through J5 are 20 pin socket type connectors used to radially connect the SA1000 data lines to the controller. Maximum cable length should not exceed 20 feet (6 meters).

The recommended mating connector for J2 through J5 is a 3M Scotchflex P/N 3421-3000. Figure 3 shows the pinouts for J1 and J2 through J5.

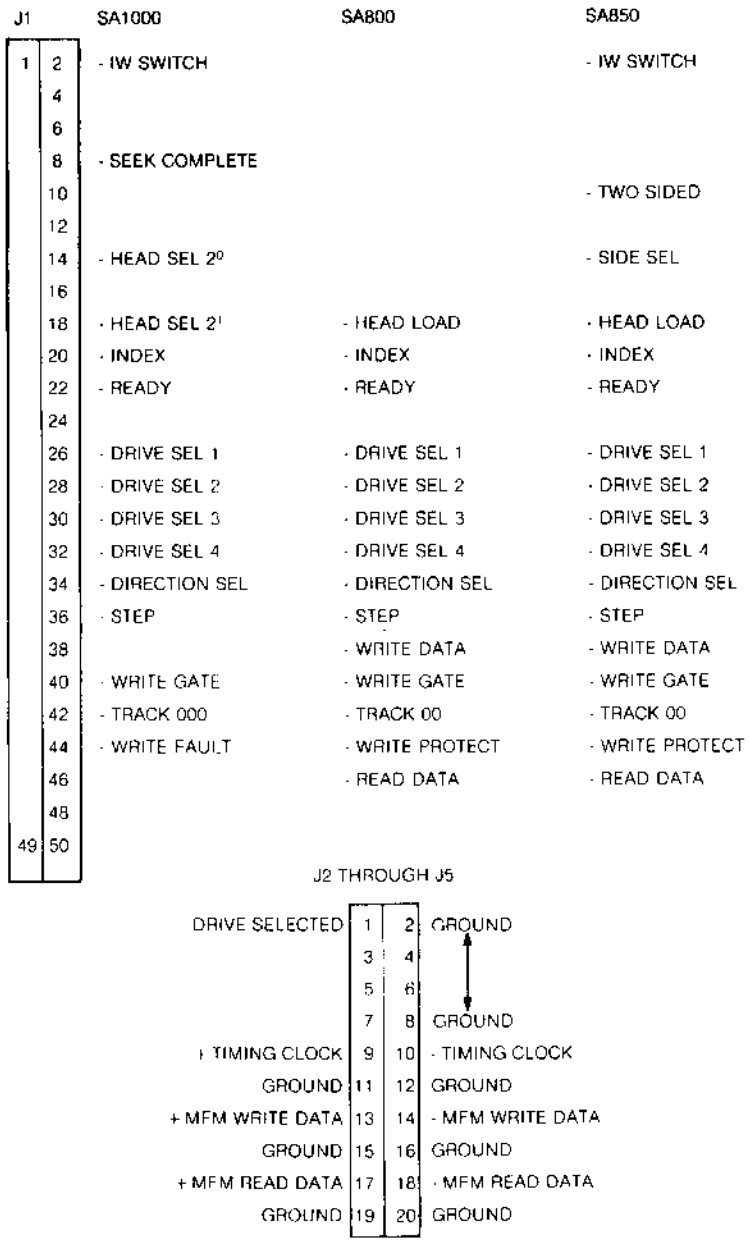


FIGURE 3. SA1403D DRIVE CONNECTOR PINOUTS

3.1 CABLE TERMINATION

The last physical drive at the end of J1 (50 pin) cable must be properly terminated. Termination networks are provided on the drives (refer to SA1000, SA800 or SA850 OEM manuals for location of termination networks). Termination networks must be removed from all drives except the last drive on the cable to avoid multiple termination.

NOTE: If a combination of fixed and floppy drive are used, the last drive at the end of the control cable must be an SA1000.

4.0 HOST CPU INTERFACE

The SA1400 series controller interface is a general purpose 8 bit parallel DMA.

The Host CPU is interfaced to the controller via connector J6, J6 is a 50 pin socket type connector. The recommended mating connector for J6 is a 3M Scotchflex ribbon connector P/N 3425-3000. The J6 interface cable should not exceed 20 feet (6 meters).

4.1 HOST CPU ELECTRICAL INTERFACE

All Host CPU interface signals are negative true. The signals are "Asserted" at 0 VDC to 0.4 VDC. The signals are "Deasserted" or inactive at 2.5 VDC to 5.25 VDC.

4.1.1 HOST CPU INTERFACE TERMINATION

All Host CPU interface timing lines are terminated with a 220/330 ohm network. The Host CPU adapter should be terminated in a similar fashion (see Figure 4).

The devices driving the controller inputs should be open collector devices capable of sinking at least 48 milliamps to a voltage level of less than 0.5 VDC (7438 or equivalent).

The devices receiving the controller outputs should be of the SCHMITT trigger type to improve the noise margin (74LS240, 74LS14, or equivalent). The Host adaptor should not load the bus with more than 1 standard TTL input load per line.

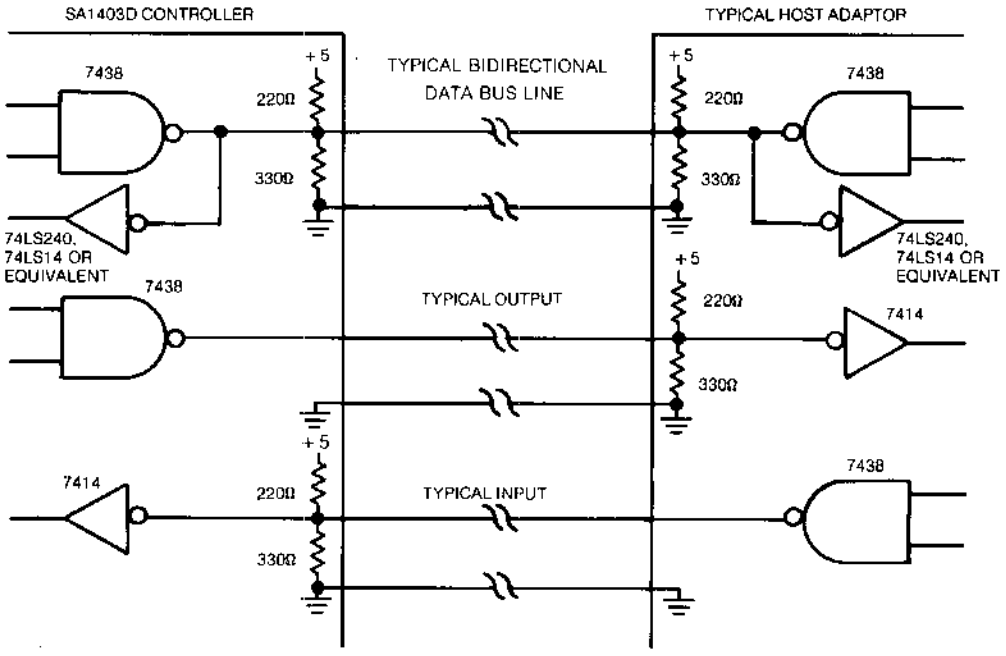
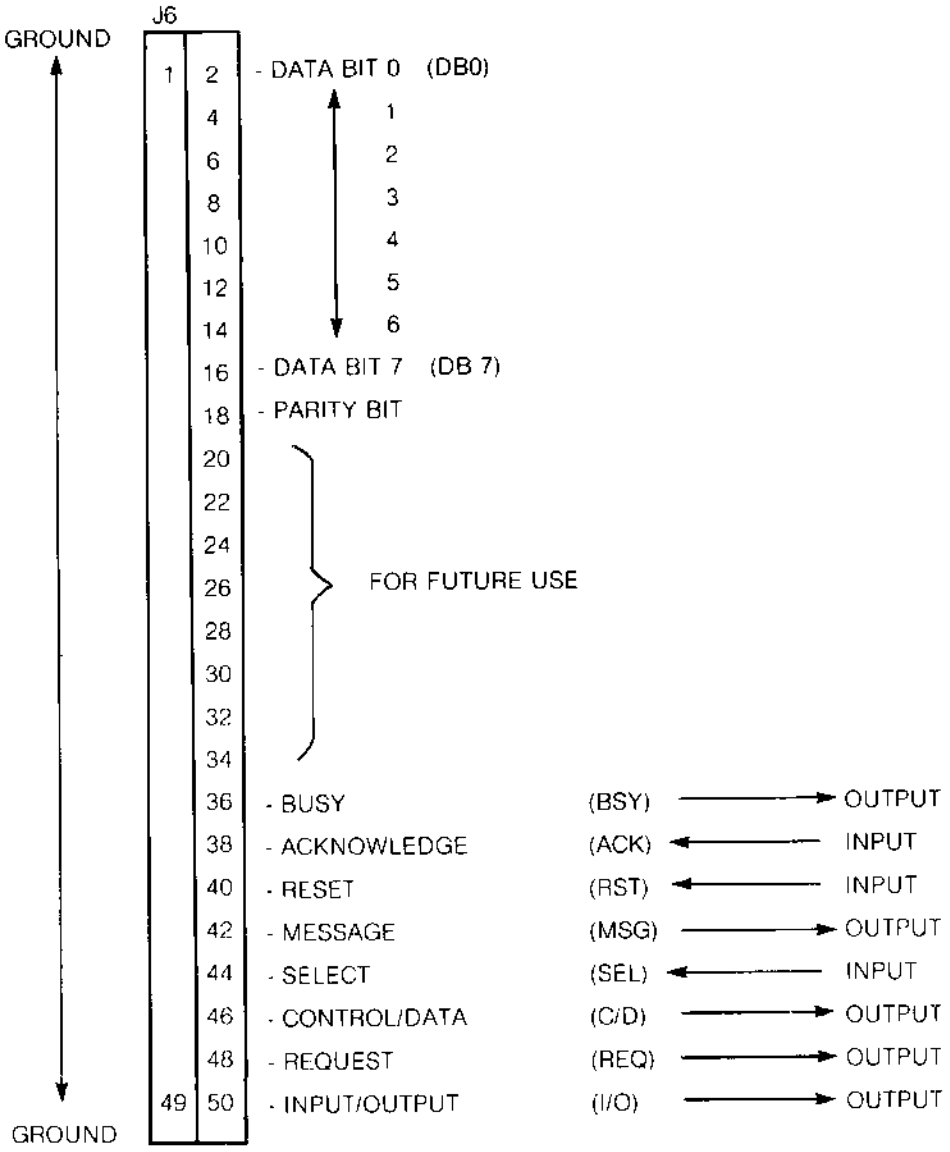


FIGURE 4. HOST ADAPTOR BUS TERMINATION

4.1.2 HOST CPU SIGNAL INTERFACE

The Host CPU signals are interfaced via J6. See figure 5 for J6 pinouts.



NOTE: ALL SIGNALS ARE TTL NEGATIVE TRUE

FIGURE 5. J6 HOST INTERFACE CONNECTOR PINOUT

4.2 SA1403D HOST BUS

4.2.1 THEORY OF OPERATIONS

Disk commands are issued to the SA1403D via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution. (Command structure is described in 4.5). Depending on the type of command, the controller will request either 6 or 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk drive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send completion status to the host. Further delineation of the completion status may be requested by issuing the appropriate sense commands.

Odd parity is generated by the SA1403D for all information that it puts on the I/O bus. If enabled, the SA1403D checks all information that it receives for odd parity.

4.3 SIGNAL DEFINITION

Unidirectional Signals Driven By Controller

I/O — **Input/Output.** When asserted, the data on the bus is driven by the controller; when deasserted, the data on the bus is driven by the host adapter. The host adapter will use this line to enable its drivers onto the data bus.

C/D — **Control/Data.** When asserted the data transmitted across the bus will be the command or status bytes; when deasserted the data will be the disk data bytes.

BUSY — This bit is asserted as a response to the SEL line from the host adapter and to indicate that the host bus is currently in use.

MSG — **Message.** When asserted indicates that the command is completed and status has been transferred. The assertion of this bit is always followed with the assertion of I/O, and the assertion of REQ, to cause a message byte transfer.

REQ — **Request.** This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the host adaptor (H/A).

I/O	MSG	C/D	Meaning
d	a	d	Get command from H/A
d	d	d	Get data from H/A
a	d	d	Send data to H/A
a	a	d	Send status byte to H/A
a	a	a	Command done to H/A

TABLE 2.

a = asserted, d = deasserted, H/A = host adaptor

4.4 UNIDIRECTIONAL SIGNALS DRIVEN BY HOST ADAPTOR

ACK — **Acknowledge.** This bit is asserted as a response to REQ from the controller. The timing requirements on this signal with respect to the data is described in REQuest section. ACK must be returned for each REQ assertion. Once REQ has been asserted, the controller waits 256μs for the assertion of ACK return before timing out.

RST **Reset.** Assertion by the Host causes the controller to cease all operations and return to an idle condition. This signal is normally used during a power up sequence. A reset during a write operation would cause incorrect data to be written on the selected disk. The reset pulse should be at least 25 microseconds wide. The controller may take a maximum of 2 seconds to respond to the select sequence following deassertion of the RESET line.

SEL **Select.** When asserted indicates the beginning of the command transaction. The H/A asserts SEL to gain the attention of the controller. Data bit zero on the host bus must also be asserted during SEL time to select the controller address. SEL must not be asserted on the host bus before data bit zero. The controller will return BUSY within approximately 1μs. After the assertion of BUSY the H/A must deassert SEL, within 500 ns.

4.4.1 DATA BUS BITS 0-7 (DB)

These bidirectional data lines are used to transfer 8 bit parallel data to/from the Host adaptor. Bit 7 is most signifant bit.

4.4.2 PARITY BIT

This bit is asserted to maintain odd parity on all data and status information transfered to the Host. If enabled, the controller will test for odd parity on all command and data information transfered to the controller (see section 9.1).

4.5 HOST INTERFACE PROTOCOL

There are 4 sequences required to initiate and complete a command to the SA1403D series controller:

1) Controller Selection Sequence

2) Command Transfer Squence

3) Data Transfer Sequence

4) Status and Message Transfer Sequence

4.5.1 CONTROLLER SELECTION SEQUENCE

In order to gain the attention of the controller it is necessary to perform a selection sequence. Refer also to Figure 6.

The Host must first test BSY to determine if the controller is available. If BSY is deasserted, the Host will assert data bit 0 (controller ID) and then assert SEL. The controller will then respond by asserting BSY. At this point the Host must deassert SEL and data bit 0. I/O will remain deasserted throughout the selection sequence.

4.5.2 COMMAND TRANSFER SEQUENCE

Following the selection sequence the controller will assert REQ (see Figure 6). The Host will then place the first byte of the command descriptor block (see section 5.0) on the data bus. The Host will then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the command transfer sequence and attempt to transfer a status byte). The controller will respond by reading the byte on the data bus and then deasserting REQ. The Host then must deassert ACK to begin the next REQ/ACK handshake. This handshake continues until all bytes of the command descriptor block have been transfered.

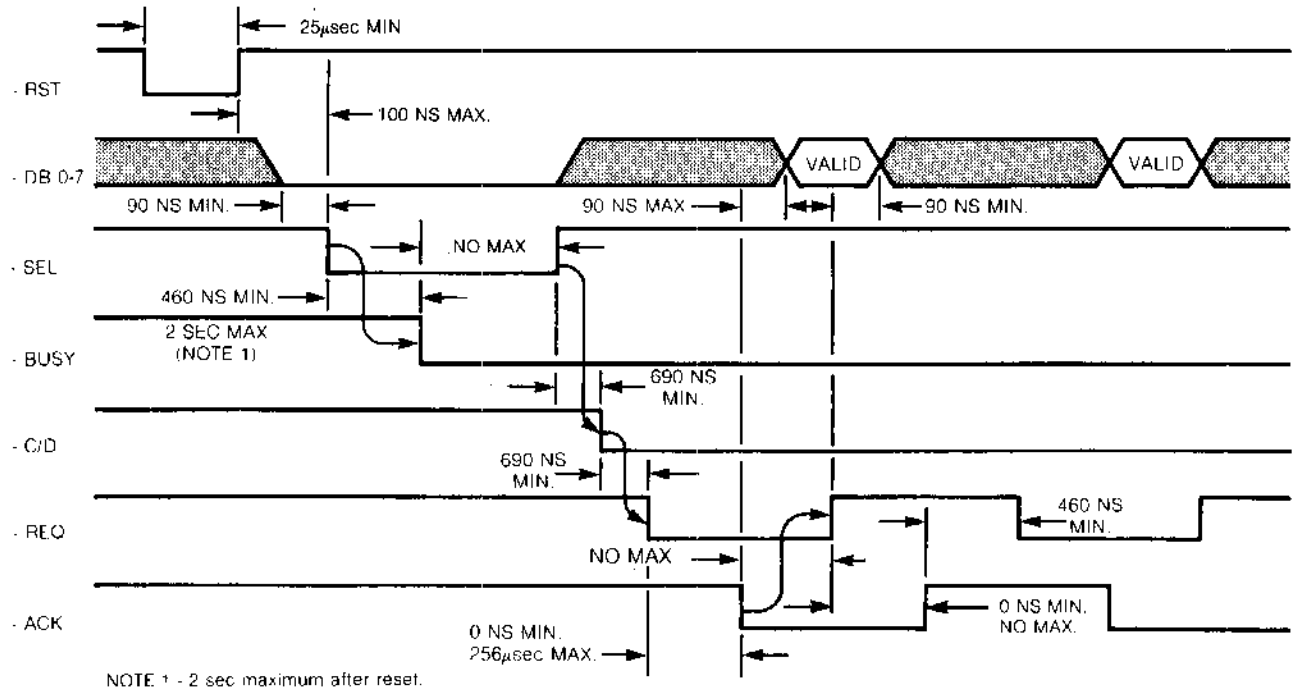


FIGURE 6. SELECT SEQUENCE TIMING

4.5.3 DATA TRANSFER SEQUENCE

Following the command transfer sequence, the controller will respond on one of four ways:

1) Begin seeking the drive.

2) Begin accepting write data from the Host.

3) Begin transferring read data to the Host.

4) Return status to the Host.

If the command sent to the controller involves a data transfer (see Figure 7), the controller will deassert the C/D line to indicate a data transfer. If the data transfer is from the Host to the controller (write data) the I/O line will be deasserted. If the data transfer is from the controller to the Host (read data) the I/O line will be asserted. The controller will then set the REQ line to request a byte transfer. The Host will respond by transferring a byte across the data bus and then asserting ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, the controller will abort the data transfer sequence and attempt to transfer a status byte - see section 4.5.4). The Host will then deassert ACK and wait for the next assertion of REQ. This handshake continues until all data has been transferred

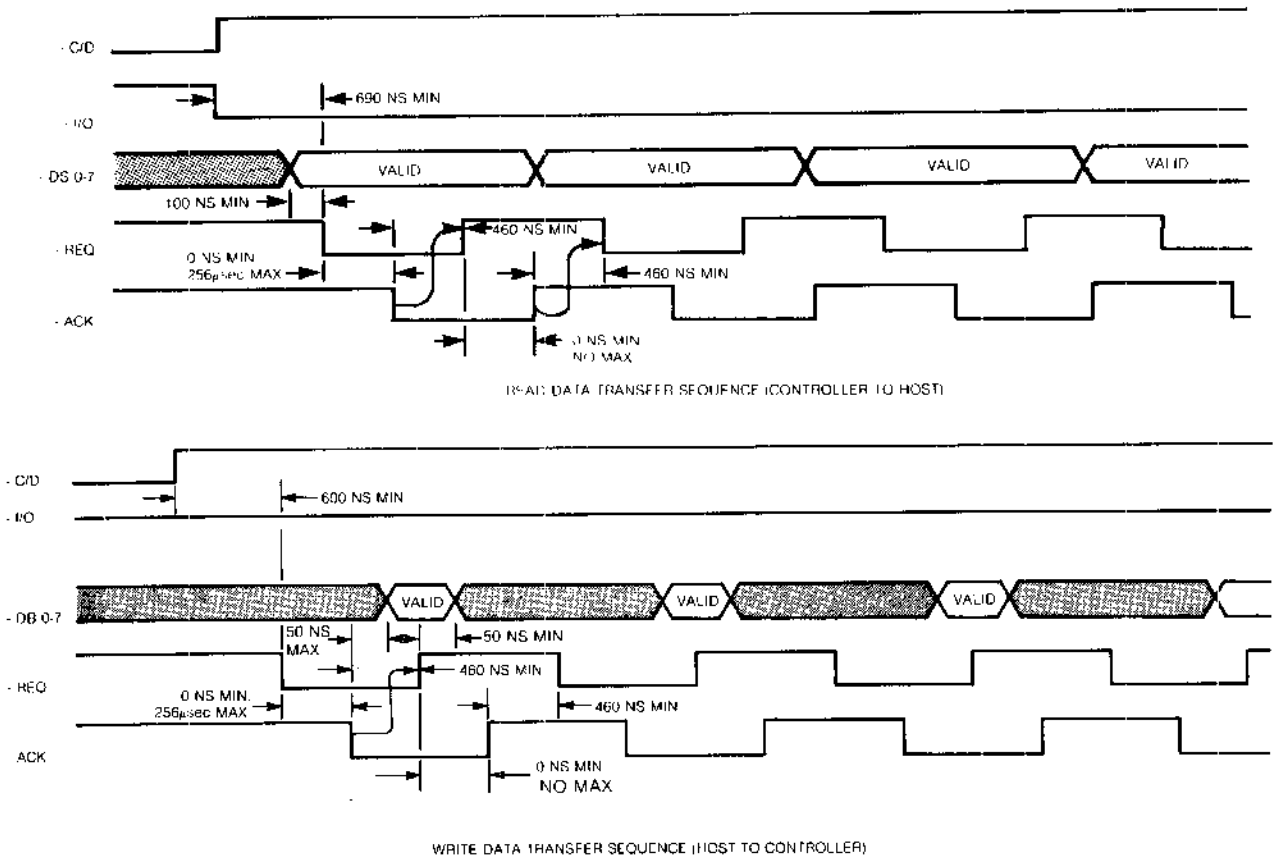


FIGURE 7. DATA TRANSFER SEQUENCE TIMING

4.5.4 STATUS AND MESSAGE TRANSFER SEQUENCE

Following a command transfer or data transfer, the controller will initiate a status byte and completion message transfer.

When a status byte transfer is required, the controller will assert C/D and I/O (see Figure 8). The controller will then assert REQ. The Host must then read the status byte on the data bus and then assert ACK (if ACK is not asserted within 256 microseconds after the assertion of REQ, REQ will be deasserted. REQ will then be asserted again).The controller will then deassert REQ. The host will then deassert ACK.

Following the status byte transfer, a completion message byte of all zero's will be transfered to indicate operation complete. The controller will assert the MSG line (along with I/O and C/D) and then assert REQ. The Host may read the completion message byte on the data bus and assert ACK (if ACK is not asserted within 256 microseconds, the controller will deassert the MSG line and attempt to transfer a status byte). The controller will respond by deasserting REQ. The Host will then deassert ACK. At this point BSY and all other controller I/O lines will be deasserted and the controller will return to an IDLE LOOP awaiting the next selection sequence.

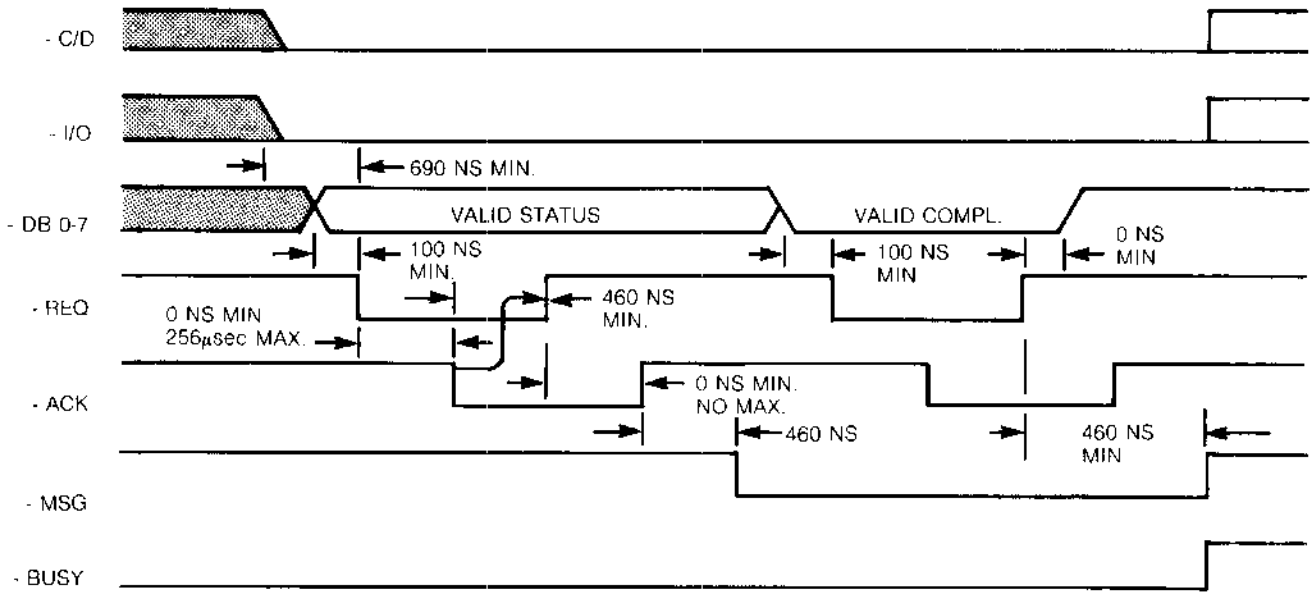


FIGURE 8. STATUS AND COMPLETION SEQUENCE TIMING

5.0 CONTROLLER COMMAND DESCRIPTOR BLOCK

Following the controller selection sequence the controller will request a command descriptor block (CDB) which, depending on the class of command, may be either 6 or 10 bytes in length. The first byte of the CDB contains the command class and the command operation code. The remaining bytes specify the drive logical unit number (LUN), logical sector address, number of sectors to be transfered or a destination device (Copy Command), and a control field byte.

Commands are categorized into four classes as indicated:

Class 0 - Utility, Data Transfer and Status Comands
Class 1 - Disk Copy Commands
Class 2-5,7 - Reserved
Class 6 - Floppy Disk Track Format Selection

The command descriptor blocks in Command Class 0 and 6 are 6 bytes long, and those in Class 1 are 10 bytes long.

The controller will check all incoming command descriptor blocks for validity and will also check (if enabled) all CDB's and data for odd parity (see section 9.1). A parity error will cause an immediate halt of the command or data transfer. This will not cause incorrect data to be written because the write does not occur until the sector buffer has been filled. An error in the command structure will cause a status byte transfer to occur upon completion of the CDB transfer.

5.1 COMMAND DESCRIPTION (CLASS 0)

WARNING!
Commands READ and WRITE require that the floppy diskette used be formatted. If unformatted, the controller will appear to "hang" - i.e., continue waiting for a data address mark. (Reset to clear this condition if it should occur).

Opcode (Hex)	Description
00	Test drive ready - Selects the drive and verifies drive ready. The ready condition is indicated by the status byte. A not-ready drive will cause bit 1 of the status byte to be set.
01	Recalibrate. Positions the R/W arm of selected rive to Track 00, clears any fault conditions.
02	Request Syndrome - returns two bytes of error offset and syndrome to the Host System for Host error correction capability (see Table 3). The first byte is offset in the data field of the error location. The most significant 3 bits of the second byte point to the beginning of the error location. The least significant 4 bits of the second byte are the syndrome which is a data correction mark to be exclusive or'ed with the faulty data. This command is only valid if the automatic data correction has been disabled.

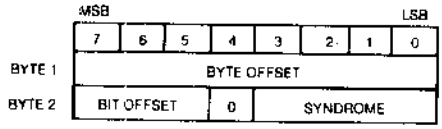


TABLE 3

03	Request Sense. This command must be issued immediately after an error. It returns 4 bytes of drive and controller sense for the specified LUN. (See copy block for exception)
04	Format Drive. Formats all blocks with ID field set according to interleave code. The data field contains 6C Hex.
05	Check Track Format. *Checks format on the specified track for correct ID and interleave. Does not read the data field. (See Warning above!)
06	Format Track. *Formats the specified track with bad block flag cleared in all blocks of that track. Writes 6C Hex in the data fields.
07	Format Bad Track *(bad block flag). Formats the specified track with bad block flag set in the ID fields (bit 7 of the Head Address byte set). Writes 6C Hex in the data fields.
08	Read. Reads the specified number of blocks starting from initial block address given in the CDB. (See Warning above!)
09	Reserved.
0A	Write. Writes the specified number of blocks starting from initial block address given in the CDB. (See Warning above!)
0B	Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drives capable of overlap seek.

*The track is addressed via the logical sector address, which may be any address within the desired track.

5.1.2 COMMAND DESCRIPTION (CLASS 1)

Opcode (Hex)	Description
00	Copy Blocks. Copies the specified number of blocks from Source LUN starting at the specified Logical address to Destination LUN starting at the specified Logical address. The number of sectors transferred may be from 1 to 256. The completion status byte will indicate the source LUN. If an error occurs, a Request Sense command is issued to the source LUN. The sense will indicate the type of error for the appropriate LUN. Note the data in the blocks will be truncated or appended with undefined data if the Source and Destination block sizes are not the same (e.g. Source block size - 128 bytes/sector, and Destination block size - 256 bytes/sector).

5.1.3 COMMAND DESCRIPTION (CLASS 6)

Opcode (Hex)	Description

00 Define Floppy Disk Track Format. The Track format code in byte 5 of the CDB defines the track format for the LUN. The Track Format Codes are as follows:

Track Format Code (Hex)	Description
00	Single Density, Single Sided. All tracks - FM recording, 128 bytes/sector, 26 sectors/track.
01	Single Density, Double Sided. All tracks - FM recording, 128 bytes/sector, 26 sectors/track.
02	Double Density, Single Sided. Side 0, Cylinder 0 - FM Recording, 128 bytes/sector, 26 sectors/track. All other tracks - MFM recording, 256 bytes/sector, 26 sectors/track.
03	Double Density, Double Sided. Side 0, Cylinder 0 - FM recording, 128 bytes/sector, 26 sectors/track. All other track - MFM recording, 256 bytes/sector, 26 sectors/track.

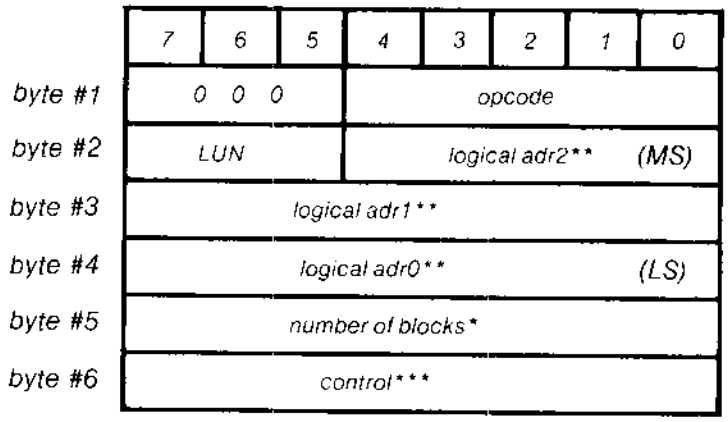
NOTE: If track format information for floppys is not specified after each reset or power-on, the default mode will be taken from the drive type selection dipswitch as follows:

Switch Setting	Mode
OFF-ON	Single density, single sided (same as track format code 00)
OFF-OFF	Single density, double sided (same as track format code 01)

Refer to Section 9.2 for switch setup instructions.

5.2 COMMAND FORMAT

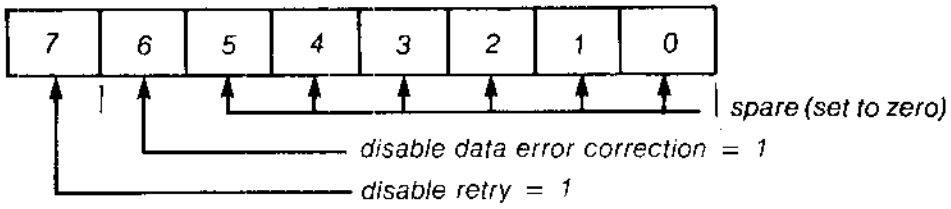
5.2.1 CLASS 0 COMMANDS



*Interleave factor for Format, Check Track Format commands.

**Refer to Section 5.5 Logical Address.

****The control field is defined as follows:*



CONTROL FIELD

5.2.2 Class 1 Commands

	7	6	5	4	3	2	1	0
byte #1	0	0	1	opcode				
byte #2	0	LUN/s		logical adr2/s* (MS)				
byte #3	logical adr1/s*							
byte #4	logical adr0/s* (LS)							
byte #5	number of blocks							
byte #6	0	LUN/d		logical adr2/d* (MS)				
byte #7	logical adr1/d*							
byte #8	logical adr0/d* (LS)							
byte #9	spare							
byte #10	control (section 5.2.1)							

where 's' indicates the source device and 'd' indicates the destination device.
*Refer to Section 5.5 Logical Address

5.2.3 Class 6 Commands

	7	6	5	4	3	2	1	0
byte #1	1	1	0	opcode				
byte #2	LUN			N/A				
byte #3	N/A							
byte #4	N/A							
byte #5	N/A							
byte #6	Track Format Code							

NOTE: See Class 6 Command Description for more information and default modes for floppy drives.

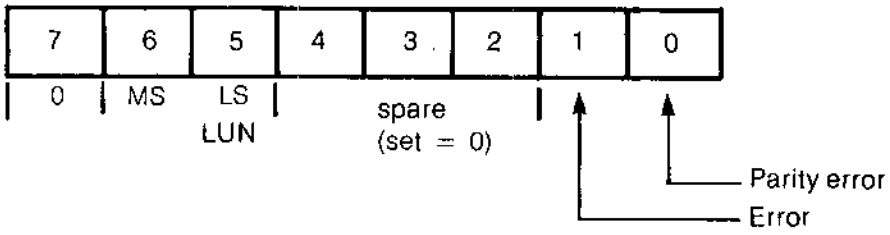
5.3 STATUS FORMAT

5.3.1 Completion Status Byte Format

At the normal termination of a command or following a fatal error, the controller will cause a status byte to be transferred from the controller to the Host. Bit 0, the least significant bit of the status byte, will be set equal to 1 if the controller detects a parity error during a command or data transfer to the controller. Bit 1 will be set = 1 if the controller detects an error condition. Bits 5 and 6 represent the LUN of the device where the error occured. If no error occurs, bit 0 - 4 will be set equal to 0.

Following the transfer of the status byte, the MSG line will be asserted to indicate a completion message. At this time the message consists of a single byte transfer with all bits set = 0.

Prior to an error condition the controller, unless diabled (see section 5.2.1 Control Field), will retry 3 times before posting the error.

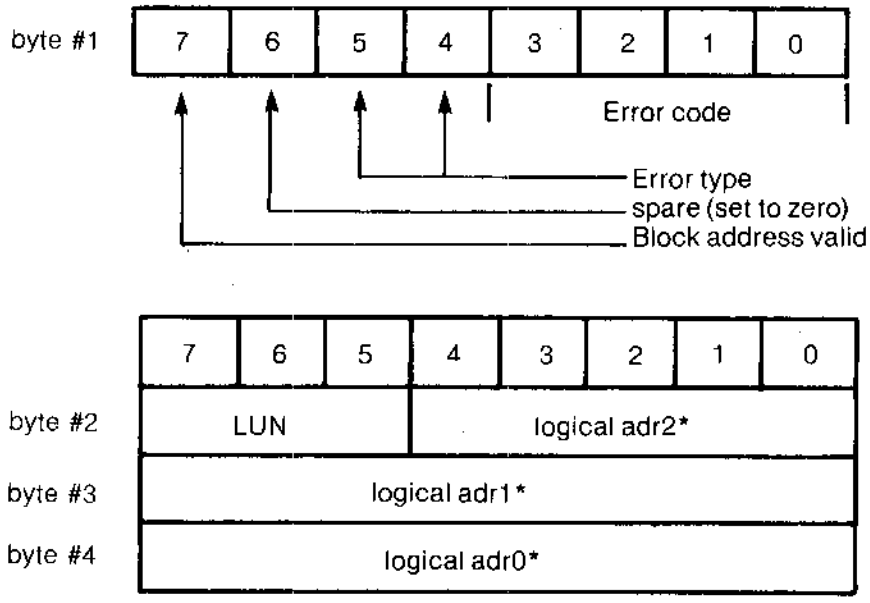


Bit 0 Parity error during transfer from host to controller.
Bit 1 Error occured during command execution.
Bit 2-4 Spare (set to zero).
Bit 5-7 Logical unit number of the drive.

5.3.2 Drive and Controller Sense Block

Following an error indication from the status byte, the Host may perform a REQUEST SENSE command to obtain more detailed information about the error.

The REQUEST SENSE command will transfer a block of 4 bytes to the Host system.



*Refer to Section 5.5 Logical Address

5.4 ERROR CODES

5.4.1 TYPE 0 (DRIVE) ERROR CODES

0	No error
1	No Index signal
2	No Seek Complete
3	Write Fault (SA1000 only)
4	Drive not ready
5	Drive not selected (SA1000 only)
6	No Track 00

5.4.2 TYPE 1 (CONTROLLER) ERROR CODES

0	ID read error. ECC or CRC (floppy) error in the ID field (uncorrectable).
1	Uncorrectable data error during a read.
2	ID Address Mark not found (possibly unformatted disk).
3	Data Address Mark not found.
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	DMA Data time out error. No Host acknowledge within 256μs.
7	Write protected. (SA800/850 only)
8	Correctable data field error. Ecc error (automatic correction if not disabled).
9	Bad track found
A	Format Error. The controller detected that during the Check Track command, the format on the drive was not as expected.

5.4.3 TYPE 2 (COMMAND) ERROR CODES

0	Invalid Command received from the host.
1	Illegal logical sector address. Address is beyond the maximum address for the type of drive.
2	Illegal function for the specified drive. e.g., Check Track command does not apply for floppy disks with IBM track format.

5.4.4 TYPE 3 (MISC) ERROR CODES

0	RAM error. Data error detected during Sector buffer RAM diagnostic.

5.5 LOGICAL ADDRESS

The logical address is computed as follows:

Logical adr = (CYADR * HDCYL + HDADR) * SETRK + (SEADR -1)

Where:
CYADR = cylinder address
HDADR = head address
SEADR = sector address
HDCYL = number of heads per cylinder
SETRK = number of sectors per track

Bit 0 of Logical adr 0 = the least significant bit.
Bit 4 of Logical adr 2 = the most significant bit.

6.0 SECTOR INTERLEAVE CODES

In order to tailor host system data transfer speed to the disk rotational speed, sector interleaving is offered. Sixteen interleave codes are offered numbered 1 to 16. Not all interleave codes will result in optimum sector interleave. therefore the interleave should be chosen carefully. In order to maintain IBM floppy disk compatability an interleave code of 1 should be used. This will result in a non-interleave condition.

The interleave code given during the format command is calculated as follows:

- The interleave algorithm is: Sector + interleave

Two examples of interleave codes are shown:

Interleave code of 2:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
Physical:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31

Interleave code of 16:

Physical:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Logical:	0	16	1	17	2	18	3	19	4	20	5	21	6	22	7	23
Physcial:	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Logical:	8	24	9	25	10	26	11	27	12	28	13	29	14	30	15	31

7.0 DIAGNOSTIC PHILOSOPHY

7.1 BOARD RESIDENT MICRODIAGNOSTIC

Fault Isolation Microdiagnostic (Optional)
The controller can be further checked out off-line by initiating explicit microdiagnostic routines via optional firmware diagnostic sets. The routines are initiated by a set of control switches. Errors will be displayed in a set of LED's. Each microdiagnostic checks the funtionality of a particular section of the controller and is able to isolate failures in the following major categories:

ALU
Registers
Sector Buffer
ECC Logics

Fault-isolation techniques can be concentrated on the failing section.

8.0 STATUS LED ERROR INTERPRETATION

Drive/controller error conditions are displayed on the 8 LED display lights provided near the J10 DC power connector (see Figure 11). The following list of hexadecimal numbered error codes describe error meanings. Note that these error codes do not necessarily match the request sense block error codes. LED number 7 is the MSB.

01	No Index Detected
02	No Track Zero Detected
03	Illegal Logical Sector Address - beyond maximum sectors available for type of drive
04	Drive Not Selected (SA1000 only)
05	No Seek Complete Detected
06	ID Address Mark Not found (unformatted)
07	Data Address Mark Not found
08	Seek Error - R/W head not positioned on correct track
09	Record Not found - found correct cylinder and head but not sector
0A	ID ECC or CRC error (uncorrectable)
0B	DMA Timeout Error - no Host acknowledge within 256μsec after request.
0C	Invalid Command Received from Host
0D	Incorrect Data Address Mark
0E	Incorrect ID Address Mark
0F	Incorrect Cylinder Address
10	Incorrect Sector Address
11	Incorrect Head Address
12	Uncorrectable Data Field ECC or CRC error
13	Correctable Data Field ECC error
14	Drive Not Ready
15	Write Fault (SA1000 only)
16	Spare
17	Write Protected (SA800/850 only)
18	RAM Diagnostic Error
19	Spare
20	Spare
21	Bad Sector found - a sector within a track that has been flagged bad has been found.
22	Invalid function for this drive type.

9.0 CONTROLLER OPTION SELECTION

9.1 PARITY SELECT JUMPERS

Odd parity may be used by the Host system for data integrity verification. The controller will always output odd parity to the Host system.

Odd parity checking by the controller may be allowed or inhibited by moving a 3 position jumper plug at W1 located near the J6 Host connector (see Figure 11). With jumper at position A + B the controller will test for odd parity on all data input to the controller. With jumper at positon B + C the controller will not check for parity (normally shipped in this postion).

9.2 DRIVE TYPE SELECTION DIPSWITCH

The dipswitch settings for various types of drives for the SA1403D are shown below:

Prom Set AS30 — I, II, III, IV CUSTOMER FIRMWARE: (DIP SWITCH set-up procedure)

Location: 2H

Switch Bits	8 7	6 5	4 3	2 1	
Field Definition	LUN 0 Drive Type	LUN 1 Drive Type	LUN 2 Drive Type	LUN 3 Drive Type	OFF / ON

Drive Type	Switch Setting	Description	
0	on on	SA1002	2 heads, 256 cylinders
1	on off	SA1004	4 heads, 256 cylinders
2	off on	SA800	1 head, 77 cylinders
3	off off	SA850	2 heads, 77 cylinders

EXAMPLE:

LOCATION: 23

8 7	6 5	4 3	2 1	
LUN 0 Drive Type	LUN 1 Drive Type	LUN 2 Drive Type	LUN 3 Drive Type	OFF / ON
on on	off on	on off	off off	

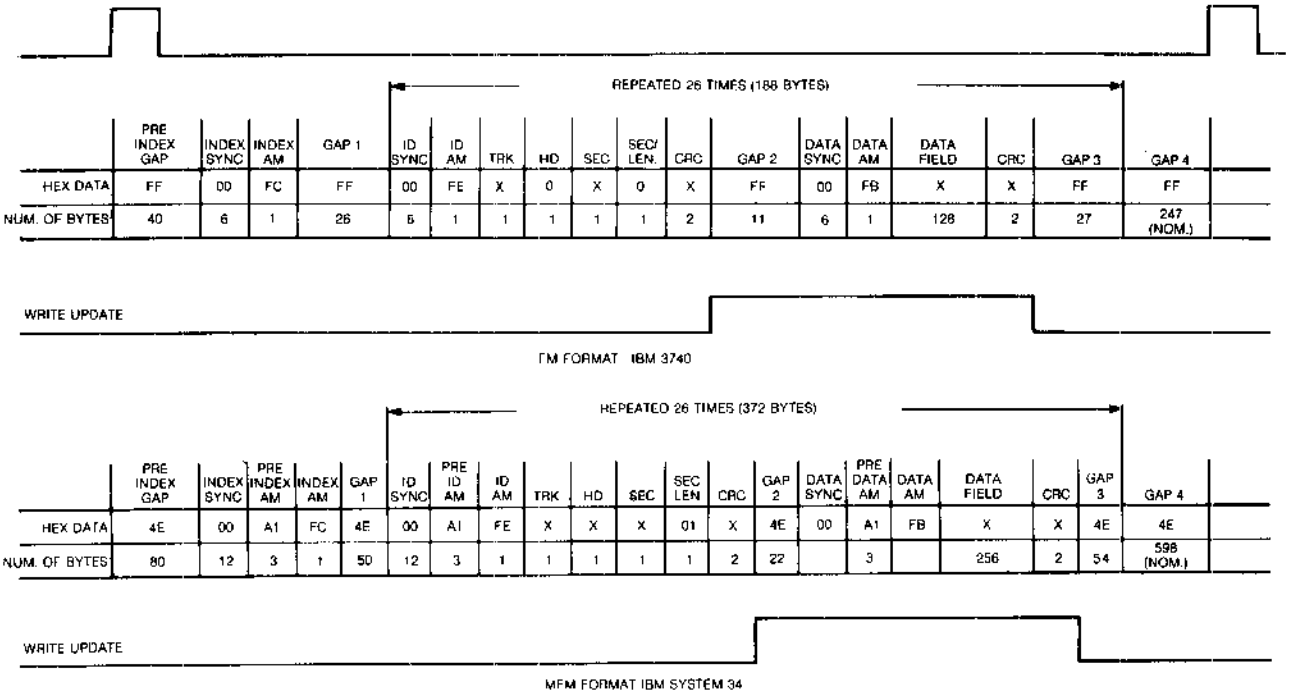
Drive 0 is set up for SA1002
Drive 1 is set up for SA800
Drive 2 is set up for SA1004
Drive 3 is set up for SA850

10.0 TRACK FORMAT DESCRIPTION

10.1 26 SECTOR FORMAT

The 26 sector format is an IBM compatible format which employes FM single density encoding on all tracks of the single density format (IBM 3740 compatible) and on track 0, side 0 of the double density format. This format yields 26 sectors of 128 bytes per sector.

The remainder of the tracks on the double density formats are encoded with MFM double density which yields 26 sectors of 256 bytes per sector (IBM system 34 compatible). Figure 9 shows the two type of encoding utilized.



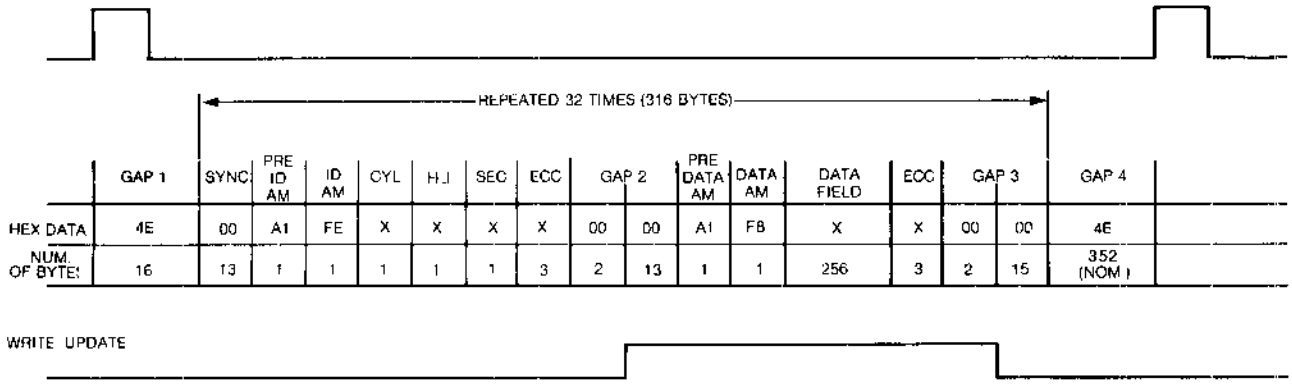
	PRE INDEX GAP	INDEX SYNC	INDEX AM	GAP 1	ID SYNC	ID AM	TRK	HD	SEC	SEC/ LEN.	CRC	GAP 2	DATA SYNC	DATA AM	DATA FIELD	CRC	GAP 3	GAP 4
HEX DATA	FF	00	FC	FF	00	FE	X	0	X	0	X	FF	00	FB	X	X	FF	FF
NUM. OF BYTES	40	6	1	26	5	1	1	1	1	1	2	11	6	1	128	2	27	247 (NOM.)

	PRE INDEX GAP	INDEX SYNC	PRE INDEX AM	INDEX AM	GAP 1	ID SYNC	PRE ID AM	ID AM	TRK	HD	SEC	SEC LEN	CRC	GAP 2	DATA SYNC	PRE DATA AM	DATA AM	DATA FIELD	CRC	GAP 3	GAP 4
HEX DATA	4E	00	A1	FC	4E	00	A1	FE	X	X	X	01	X	4E	00	A1	FB	X	X	4E	4E
NUM. OF BYTES	80	12	3	1	50	12	3	1	1	1	1	1	2	22		3		256	2	54	598 (NOM.)

FIGURE 9. 26 SECTOR FORMAT - SA800/850

10.2 32 SECTOR FORMAT

The 32 sector format employs MFM encoding on all tracks of the SA1000. This format yields 32 sectors of 256 bytes per sector. Figure 10 shows the 32 sector format.



	GAP 1	SYNC	PRE ID AM	ID AM	CYL	H.I	SEC	ECC	GAP 2		PRE DATA AM	DATA AM	DATA FIELD	ECC	GAP 3		GAP 4
HEX DATA	4E	00	A1	FE	X	X	X	X	00	00	A1	FB	X	X	00	00	4E
NUM. OF BYTES	16	13	1	1	1	1	1	3	2	13	1	1	256	3	2	15	352 (NOM.)

FIGURE 10. 32 SECTOR FORMAT - SA1000

11.0 DRIVE JUMPER SETTINGS

11.1 JUMPER SETTINGS FOR SA800/801 FLOPPY

The following information is contained in the SA800/801 Diskette Storage Drive OEM Manual.

Jumper Name	Function (Enabled if Jumper Installed)
A	Install enable DRSEL to drive selection
B	Install, Head Load on Drive Select
C	Remove, Drive Select loads heads
D	Remove, In Use to LED is disabled
DC	Remove, Disable Disk Change to return to controller
DS	Install enable stepper on Drive Select
DS1-4	Install one only, DS1 = LUN 0 (Drive Select)
HL	Remove, Head load on Drive Select
L	Jumper for -5V (remove for -15V), controller requires -5V only
T1	Remove, Head Load terminator
T2	Install, Pullup for Drive Select lines
T3	Install, Direction terminator
T4	Install, Step terminator
T5	Install, Write Data terminator
T6	Install, Write Gate terminator
X	Install, Head Load Enable
Y	Remove, Disable Hdld from driving LED
Z	Install drive select drives in use LED
800	Install, enables 800 index only operation
801	Remove, disables 801 mode operation

11.2 JUMPER SETTINGS FOR SA850/851 FLOPPY

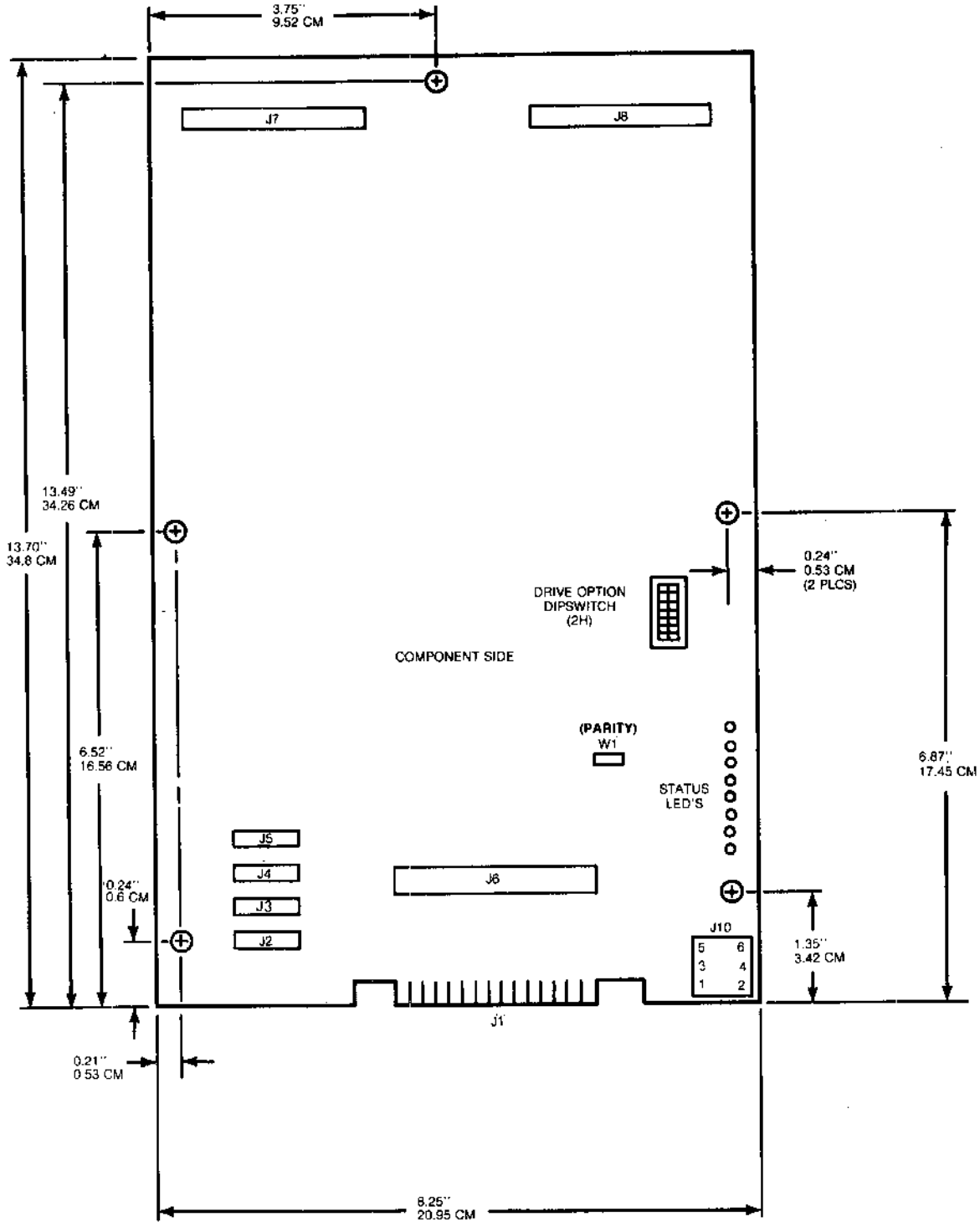
Jumper Name **Function (Enabled if Jumper Installed)**

Controller is compatible with the factory jumper configuration. See SA850/851 OEM Manual.

11.3 JUMPER SETTINGS FOR SA1000 WINCHESTER

Jumper Name **Function (Enabled if Jumper Installed)**

Controller is compatible with the factory jumper configuration. See SA1000 OEM Manual.



ALL TOLERANCES ± .003"

FIGURE 11. SA1403D DIMENSIONAL DRAWING

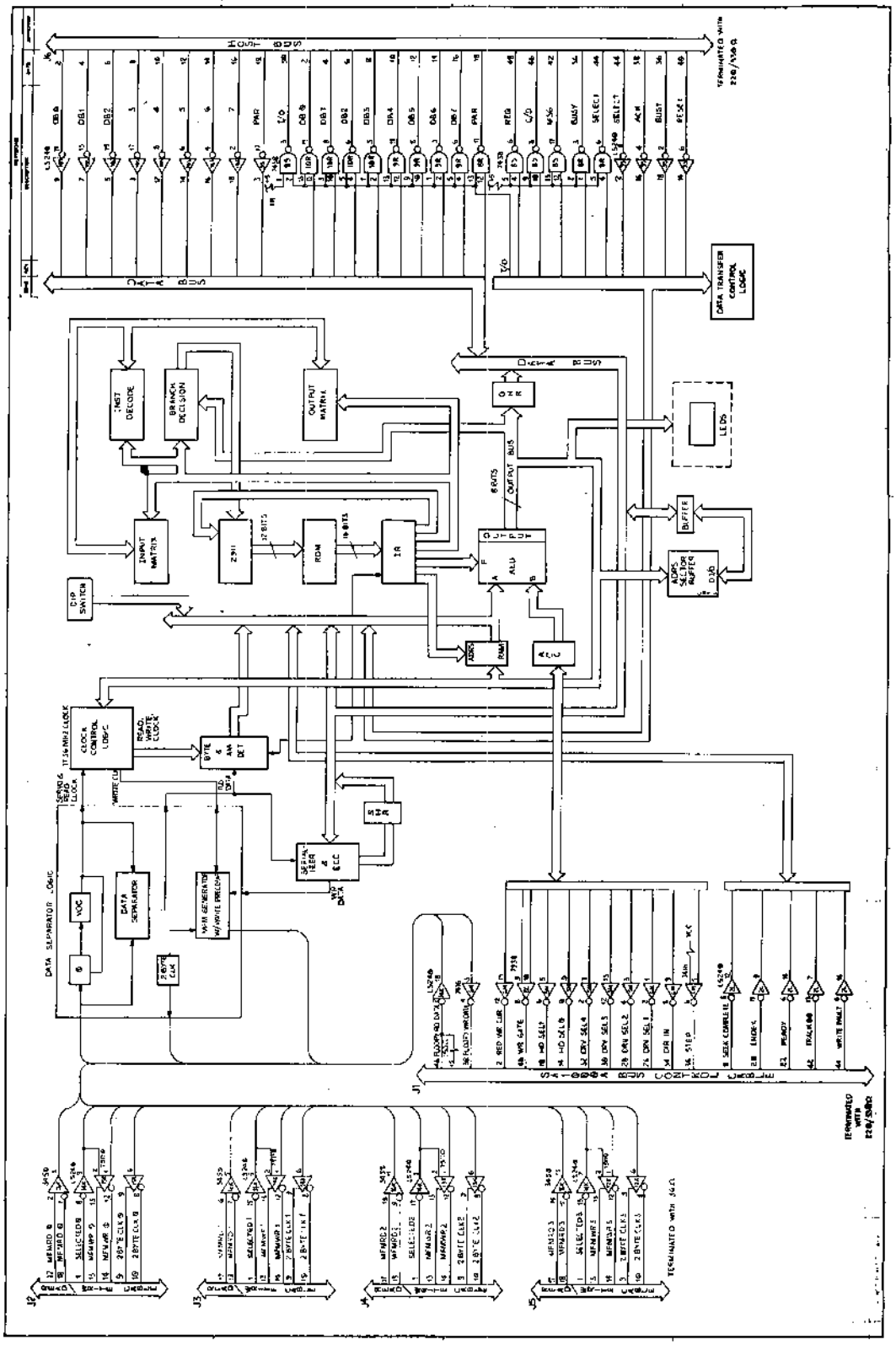


FIGURE 12. SA1403D FUNCTIONAL BLOCK DIAGRAM

APPENDIX A

SA1403D DISK CONTROLLERS

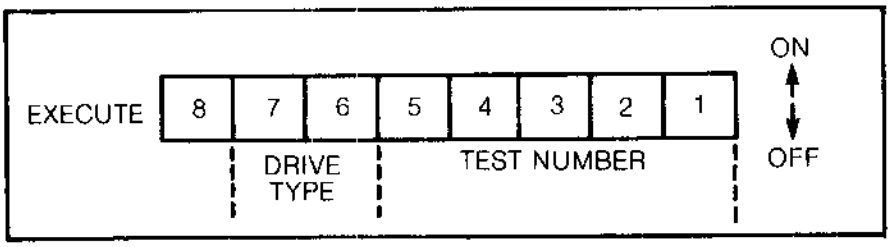
Optional diagnostic PROMS are available for the SA1403D disk controller to enable testing of the controller or the attached disk drives. When using the diagnostics, the controller/host interface cable is disconnected. The four PROMs are then plugged into IC positions 1A, 2A, 3A and 4A on the controller board.

They are installed in the same manner as the customer PROM set in the order I, II, III, and IV. The part number for the PROM set is 12668 and its identifying number is U50.

DRIVE DIAGNOSTICS

In order to execute the drive diagnostics, the dipswitch on the controller board is used. The following table shows the diagnostic switch functions:

SA1403D dipswitch location: -2H



EXECUTE SWITCH - SWITCH 8

1. Before starting the diagnostics, be sure switch 8 is in the ON position before applying DC power to the controller board. Test selection and drive type selection can be performed only while switch 8 is ON.

2. To execute the diagnostic tests, turn switch 8 OFF.

3. To terminate the test execution, set switch 8 in the ON position. Test 02 (Format Entire Disk), once initiated, will format the entire disk and ignore switch 8 before accessing the switches again. The other tests will stop execution immediately when switch 8 is turned ON.

DRIVE TYPE AND LOGICAL UNIT NUMBER SET-UP — SWITCH 7 & 6:

Switch 7 and 6 are used to define the disk drive type. A logical unit number (LUN) is assigned according to the drive type as indicated below:

SA1403D CONTROLLER	SA800/850	OFF	ON (FM) or OFF (MFM)*	0
	SA1002	ON	ON	1
	SA1004	ON	OFF	1

NOTE: For FM, the format is 26 sectors @ 128 bytes/sector
For MFM, the format is 26 sectors @ 256 bytes/sector (on MFM mode, track 0 is still FM)

TEST NUMBER SWITCHES - SWITCHES 5 THROUGH 1:

Switch 5 is the most significant switch.
Switch 1 is the least significant switch.

Associated hexadecimal-numbered tests are described below. Because each test is a singular unit, the diagnostics will continue running even if an error is encountered. Errors will be given in the diagnostic status LED's (see ERROR DISPLAY section).

TEST OPTIONS

00 Check ECC logic for a Correctable Error - a pattern with a changed bit is written on sector 0, head 0, cylinder 0 and then read back. The controller should correct the error and enable the status LED's to show a correctable data error.

01 Check ECC Logic for an Uncorrectable Error - a pattern is written on sector 0, head 0, cylinder 0 and then read back with multiple errors (more than 4 in a burst or 2 or more bits spaced greater than 4 bits apart). The controller should display an uncorrectable data error to the status LED's.

Tests 00 and 01 verify the ability of the ECC logic to detect and correct data errors.

NOTE: Test 0A (Write Sequential) *must* be executed after executing tests 00 and 01 to avoid getting a data error during tests 07 (Sequential Read) and 08 (Random Read).

02 Format Entire Disk - formats all cylinders with hex 6C data pattern in the data fields.

03 Format Innermost Track - same as test 02, except only the innermost track will be formatted.

04 Format Outermost Track - same as test 02, except only track 0 will be formatted.

Tests 02 - 04 are write only, without verify. The controller will keep the write gate asserted for the entire track. Format begins upon the detection of Index. The interleave factor is set at 1. Since these tests begin at a known point, Index, they are recommended for debugging write problems.

05 Seek Incremental Cylinder Command - sequentially seeks one cylinder at a time from 0 to the innermost track; does a seek to cylinder 0 and repeats the test.

Test 05 performs an unverified seek, no read or write. The seek is performed in the buffered step mode.

06 Read Command (innermost track) - reads all sectors on the innermost track and checks for correct ECC in ID and data fields.

07 Read Command (sequential cylinders) - same as test 06, except all sectors of the entire disk are read sequentially.

08 Read Command (random cylinder) - same as test 06, except that all cylinders are read randomly.

09 Write Command (innermost track) - writes all sectors of the innermost track filling data fields with hex 6C data pattern.

0A Write Command (sequential) - same as test 09, except that all cylinders are written sequentially.

0B Write Command (random) - same as test 09, except that all cylinders are written randomly.

0C Write/Read Command (innermost track) - writes all sectors of the innermost track filling data fields with incrementing data patterns and then reading back the information, checking for ECC errors and comparing the data.

0D Write/Read Command (random cylinder) - same as test 0C, except that all cylinders are tested sequentially.

0E Write/Read Command (random cylinder) - same as test 0C, except that all cylinders are tested randomly.

0F Recal Command - recalibrates the heads to cylinder 0.

Test 0F issues one step pulse at a time outward until track 0 is encountered.

10 Check Innermost Track Format - checks ID fields for the innermost track.

11 Check Outermost Track Format - checks ID fields for cylinder 0.

Test 10 and 11 are read only. The check tests are best suited to diagnose readback problems. The controller seeks to the specified track and verifies the format for the entire track. The sequence of the test is as follows: First, the controller seeks to the specified track and waits for the Index pulse. The read gate is then turned on to verify the ID field for correct cylinder, head, and sector address and to check the ID ECC for the first sector of the track (tracks must be formatted with interleave factor 1). The other sectors are then verified after each sector pulse is detected. Upon detection of an error, the controller will display the error in the LED's and restart the test.

12 - 18 (Not applicable)

19 Random Seek (note read/write) - same as test 05.

1A Read Outermost Track - same as test 06.

1B Write Outermost Track - same as test 09.

1C Write/Read Outermost Track - same as test 0C.

NOTES:

1. Floppy drives can only be used with tests 2 - 0F, 19 - 1C.
2. The step rate is approximately 100μs.
3. When a test is started, the controller issues a recalibrate command before initiating the particular test. This insures that the read/write heads are over track 0.

ERROR DISPLAY

Any errors uncovered by the controller during the performance of selected tests will be reported via the LED's according to the error codes listed below. Once the controller detects an error, the error display will maintain the error indication even if subsequent tests are performed correctly. In this way, the controller can be left running for a long period of time. However, only the last error will be displayed on the LED's. To reset the error display, stop the test and start again.

Error Code (HEX, DSO is LSB)	**Interpretation**
01	No Index
02	No track 00
03	Illegal disk address
04	Drive not selected
05	No seek complete
06	No ID address mark (possible unformatted tracks)
07	No data address mark
08	Seek error
09	Sector not found
0A	ID ECC error
0B	No host acknowledge
0C	Invalid command
0D	Incorrect data mark
0E	Incorrect ID mark (format error)

0F	Incorrect cylinder (format error)
10	Incorrect sector address
11	Incorrect head address
12	Uncorrectable data error
13	Correctable data error
14	Drive not ready
15	Write fault
16	Bad track flag set
17	Write protected
18	RAM diagnostic error
19 - 1F	Not used
20	Parity error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad block detected from drive
22	Invalid function for this drive type

Shugart

ADDENDUM

Product: SA1403D Controller **Date:** 3/2/81 **Manual #:** 39022-0

Subject: Corrections and an Addendum to the SA1403D OEM Manual.

The following corrections should be made to the SA1403D OEM manual:

1. Page 7, Table 2: reverse the positions of the column headings 'MSG' and 'C/D'.
2. Page 8, second paragraph; delete 'After the assertion of BUSY the H/A must deassert SEL, within 500ns.
3. Page 18, Status LED Error Interpretation: error code 20 is now assigned as a Parity error, error codes 19 and 1A through 1F are designated as spares.
4. Page 19, section 9.1, Parity Select Jumpers; normally shipped with jumper at position A + B **not** B + C.
5. Reference the attachment (page 2) for the Interleave Code Selection Chart.
6. Reference the attachment (page 3) for the corrected dimensional drawing of the SA1403D.

There has been a revision of the PROM set offered with the SA1403D controller. The AS30 PROM set, formerly installed on revision 01 controllers, has now been replaced with the AS31* PROM set. The following table lists the differences:

AS30 (w/board Rev 01)	**AS31* (w/board Rev 01)**
1. Has Check Track Command	1. Does NOT have Check Track Command.
2. Step rate for SA800 and SA850 are *same* (8 msec).	2. Step rate for SA800 - 8 msec. Step rate for SA850 - msec.
3. Data pattern used with format: 6C	3. Data pattern used with format: E5
4. Controller *hangs up* if 2 Winchester units are selected (reset Controller clears condition.)	4. Controller *reports to Host* if 2 Winchester units are selec ed (Error type 0, #7).
5. There is a *2 sec delay* on resetting the Controller.	5. There is NO delay on resetting the Controller.
6. *256*µsec timeout for ACK from Host (displays as Error on LEDs).	6. NO ACK timeout - will wait until Host responds with ACK.
7. Always *deselects* the current drive at the end of a command.	7. Deselects the current drive *only if* next command does not come within *1 sec.*. (This is done to avoid unnece sary head clapping on floppy drives)
8. Will not detect if head 1 is selected on single-sided media.	8. Indicates "Drive Not Ready" if side 1 is selected on single-sided media.
9. 1µsec step pulse for SA1000.	9. 3µsec step pulse/interval for SA1000.
10. 50 ms delay after floppy drive select to read/write.	10. 35 ms delay after floppy drive select to read/write.

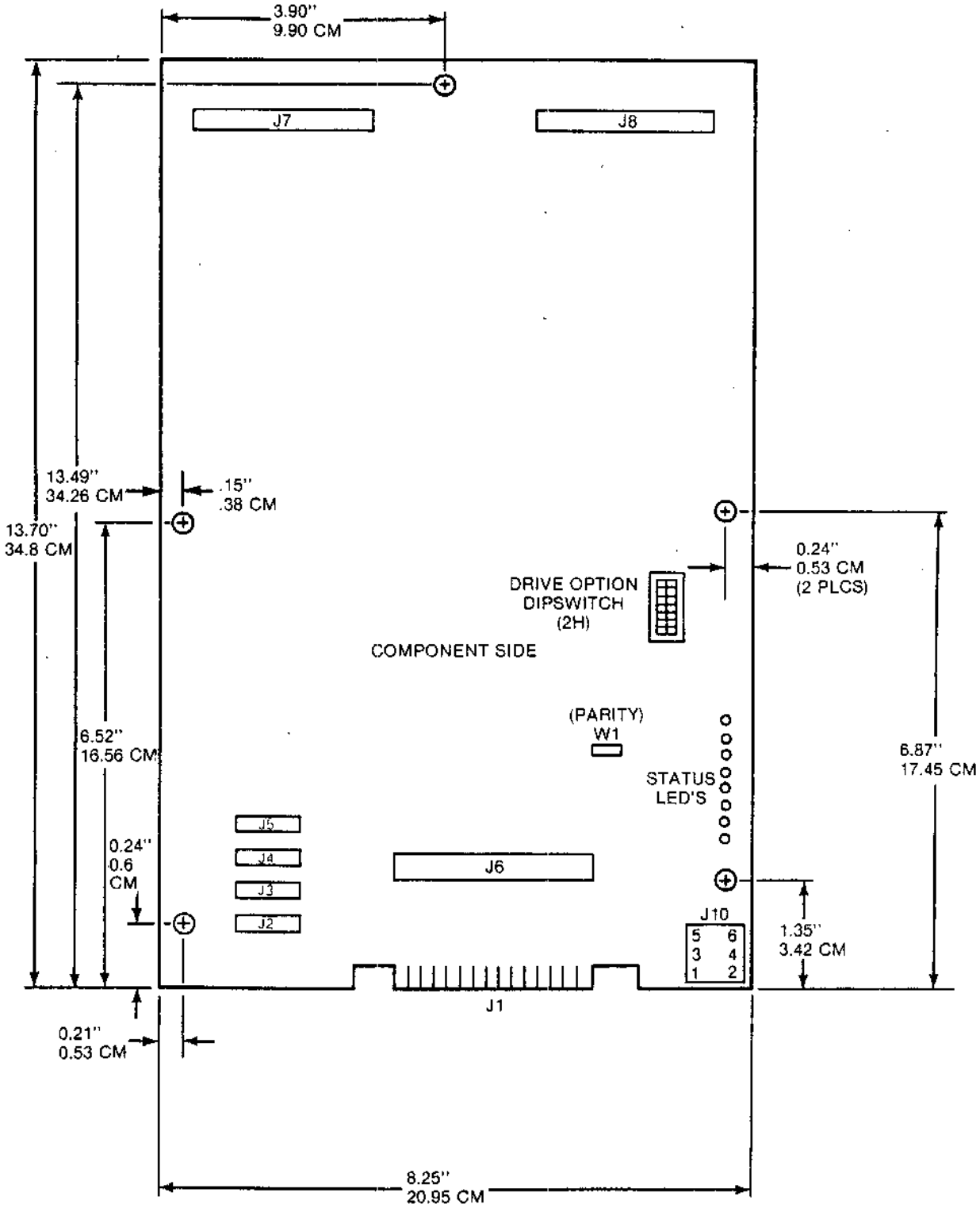
The PROM sets can be distinguished from each other by a label located on each PROM, identifying them as either a AS30 or AS31*.

Please direct any further questions to Technical Support, in Sunnyvale.

INTERLEAVE CODE SELECTION CHART *

Code	Number of Disk Revolutions Required to Read One Track	Time available to Transfer one Byte of Data (including controller time)	Minimum Number of Idle Sectors Between Reads
11	3	4.7μs	2
8	4	7.0μs	3
6	6	9.4μs	4
5	7	11.7μs	5
4	8	16.4μs	7
3	11	23.4μs	10
2	16	35.1μs	15
1	32	72.5μs	31

* (for SA1400 series controllers operating with SA1000 series drives - double density, 32 sectors, 256 bytes/sector.)
Note: Other codes will work, but require more revolutions of the disk to read all sectors of one track.



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SA1403D DIMENSIONAL DRAWING

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