
ST406

ST412

ST419

PRODUCT

MANUAL

 **Seagate**

SEAGATE TECHNOLOGY

**ST-406/412/419 MICROWINCHESTER
OEM MANUAL
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1.0 Introduction

1.1 General Description:

The ST 4XX family of disk drives consists of random access storage devices utilizing non-removable 5¼ inch discs as storage media. Each disc surface employs one movable head to service 306 data tracks.

Low cost and unit reliability are achieved through the use of a band actuator and open loop stepper head positioning mechanism. The inherent simplicity of mechanical construction and the use of a microprocessor for the electronic controls allows maintenance free operation throughout the life of the drive. Both electronic PCBs are mounted outside the head disc assembly, allowing field serviceability.

Mechanical and contamination protection for the heads, actuator, and discs is provided by an impact resistant aluminum enclosure. A self contained recirculating system provides clean air through a 0.3 micron filter. A second port in the filter assembly allows pressure equalization with ambient air without chance of contamination. A patented spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disc area. Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure results in a very low temperature rise within the enclosure. This provides significantly greater off track margin and the ability to immediately perform read and write operations after power up with no thermal stabilization delay.

The ST 4XX size and mounting are identical to the industry standard minifloppy disc drives, and they use the same DC voltages. No AC power is required.

Key Features:

- Storage Capacity of 6.38/12.76/19.14 megabytes unformatted, 5.0/10.0/15.0 megabytes formatted.
- Same physical size and mounting as the minifloppy.
- Same DC voltages as the minifloppy.
- Band actuator and stepper motor head positioning.
- 5.0 megabit/second transfer rate.
- Simple floppy-like interface.
- Same track capacity as a double density 8 inch floppy.

1.2 Specification Summary

1.2.1 Physical Specifications/Environmental Limits

Ambient Temperature	
Operating:	40° to 122°F (4° to 50°C)
Non-operating:	- 40° to 140°F (- 40° to 60°C)

Maximum Temperature Gradient	
Operating:	18°F/hour or 10°C/hour
Non-operating:	Below condensation

Relative Humidity: 8 to 80% non-condensing

Maximum Wet Bulb: 78.8°F (26°C)

Maximum elevation	
Operating:	10,000 feet
Non-operating:	- 1,000 to 30,000 feet

Maximum Shock Without Incurring Physical Damage	
Operating:	10G's*
Non-operating:	20G's*

*No mechanical damage will occur within these limits.

D.C. Power Requirements

- + 12V ± 5%, 1.6A typical, 3.5A (At power on)
- + 5V ± 5%, 1.1A typical, 1.7A (Maximum)
- Maximum Ripple: 50mV peak to peak (12V, 5V)

Mechanical Dimensions

Height:	3.25 inches
Width:	5.75 inches
Depth:	8.00 inches
Weight:	4.6 pounds (2.1Kg)
Shipping Weight:	9.0 pounds (4.1Kg)

Heat Dissipation

Typical:	25 watts
Maximum:	32 watts

1.2.2 Reliability Specifications

MTBF:	11,000 POH, typical usage
MTTR:	30 minutes
PM:	Not required
Component design life:	5 years

Bit JITTER

Bit JITTER reduction must be 40dB minimum at 2f, with less than 1.5 nsec. of shift at the center frequency.

Error Rates

Soft Read Errors*: 1 per 10¹⁰ bits read

Hard Read Errors**: 1 per 10¹² bits read

Seek Errors: 1 per 10⁸ seeks

*Recoverable within 16 retries

**Not recoverable within 16 retries

1.2.3 Performance Specifications

Capacity	Model Number		
	ST-406	ST-412	ST-419
Unformatted			
Per Drive:	6.38 MB	12.76 MB	19.14 MB
Per Surface:	3.19 MB	3.19 MB	3.19 MB
Per Track:	10,416 Bytes	10,416 Bytes	10,416 Bytes
Formatted			
Per Drive:	5.0 MB	10.0 MB	15.0 MB
Per Surface:	2.5 MB	2.5 MB	2.5 MB
Per Track:	8,192 Bytes	8,192 Bytes	8,192 Bytes
Per Sector:	256 Bytes	256 Bytes	256 Bytes
Sectors per Track:	32	32	32
Access Time			
Average*:	85ms	85ms	85ms
Maximum*:	205ms	205ms	205ms
Single Track*:	<16.67ms	<16.67ms	<16.67ms
*Using buffered seek (includes settling)			
Transfer Rate:	5.0 Mbits/sec	5.0 Mbits/sec	5.0 Mbits/sec
Average Latency:	8.33 ms	8.33 ms	8.33 ms

1.2.4 Functional Specifications

Rotational Speed:	3,600 RPM ± 1%	3,600 RPM ± 1%	3,600 RPM ± 1%
Recording Density:	9,074 BPI	9,074 BPI Max	9,074 BPI Max
Flux Density:	9,074 FCI	9,074 FCI Max	9,074 FCI Max
Track Density:	345 TPI	345 TPI	345 TPI
Cylinders:	306	306	306
Tracks:	612	1,224	1,836
Read/Write Heads:	2	4	6
Discs:	1	2	3

2.0 Functional Characteristics

2.1 General Operation:

The ST 4XX disc drives consist of read/write and control electronics, read/write heads, track positioning actuator, media, and air filtration system. The components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and Write data.
4. Provide a contamination free environment.

2.2 Read/Write and Control Electronics

Electronics are packaged on two printed circuit boards. The primary board to which power, control, and data signals are connected includes a microprocessor unit that controls the following:

1. Index detection circuit.
2. Head position/actuator circuit.
3. Drive up to speed circuit.
4. Drive select circuit.

Circuits on the primary board that are not controlled by the microprocessor are:

1. Read/Write circuits.
2. Head select circuit.
3. Write fault detection circuit.

The second PCB, mounted to the side frame under the primary board derives its power from the primary board. The second PCB provides the speed and braking controls and power for the spindle drive motor.

2.3 Drive Mechanism

A brushless DC drive motor rotates the spindle at 3600rpm. The spindle is driven directly with no belt or pulley being used. The motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber containing the heads and discs. The motor and spindle are dynamically balanced to ensure a low vibration level. The head/disc assembly is shock mounted to minimize transmission of vibration through the chassis or frame.

2.4 Air Filtration System (Figures 1A & 1B)

The discs and read/write heads are fully enclosed in a module using an integral recirculation air system and absolute filter to maintain a clean environment. The filter also contains a port which permits ambient pressure equalization without contaminate entry.

2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a band actuator connected to the stepper motor shaft. The stepper motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber.

2.6 Read/Write Heads and Discs

The recording media consists of a lubricated thin magnetic oxide coating on a 130mm diameter aluminum substrate. This coating formulation, together with the low load force/low mass flying heads, permits reliable contact start/stop operation.

Data on each of the disc surfaces is read by one read/write head each of which accesses 306 tracks.

FIGURE 1A
AIR FILTRATION SYSTEM

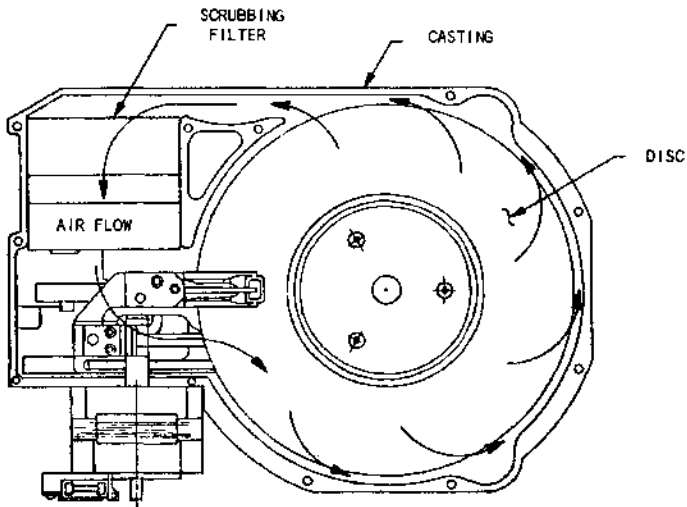


FIGURE 1B
AIR FILTRATION SYSTEM

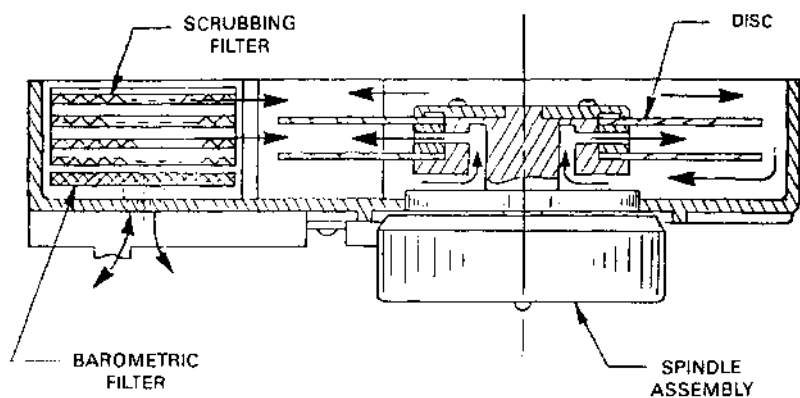
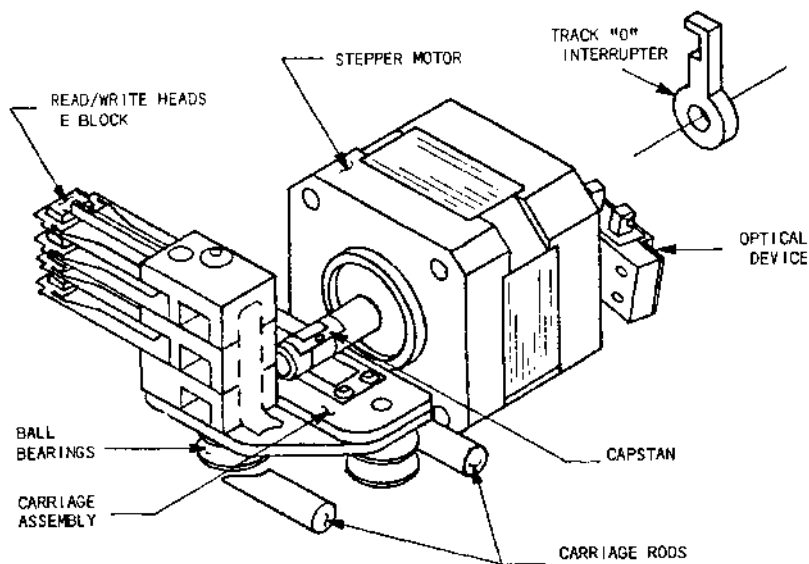


FIGURE 2
POSITIONING MECHANISM



3.0 Functional Operations

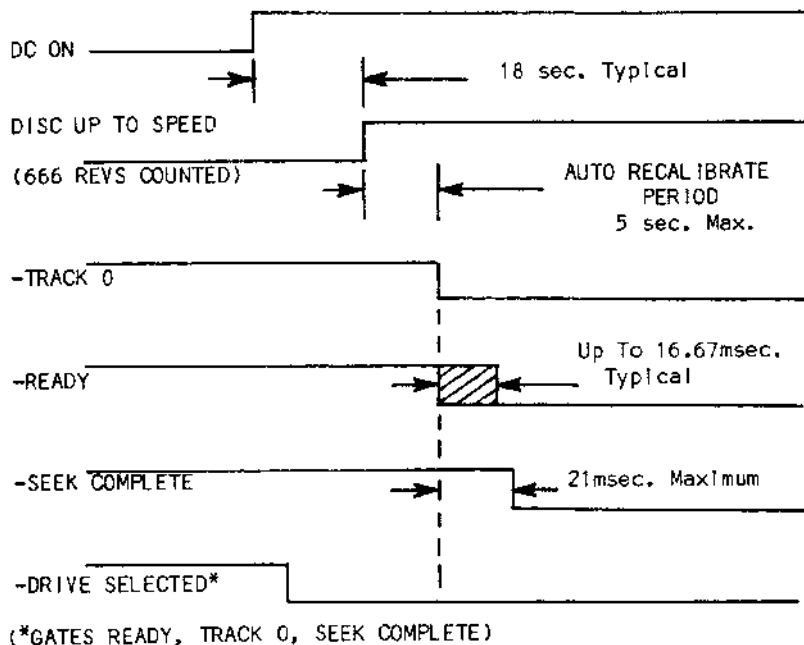
3.1 Power Sequencing (Figure 3)

Plus 5 and +12 volts may be applied in any order; however, +12 volts must be applied to start the spindle drive motor. A speed sense circuit counts 666 disc revolutions before recalibrating the heads to track 0. For this recalibration to occur, the step input signal must be inactive. TRACK 0, SEEK COMPLETE, and READY signals on the interface will become true sequentially. The drive will not perform read, write or seek functions until READY becomes true.

3.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the selected drive will respond to the input signals, and only that drive's output signals are then gated to the controller interface (See section 4.5 for exception).

FIGURE 3
POWER UP SEQUENCE



3.3 Track Accessing

Read/write head positioning is accomplished by:

- a) Deactivating WRITE GATE line.
- b) Activating the appropriate DRIVE SELECT line.
- c) Being in the READY condition with SEEK COMPLETE true.
- d) Selecting the appropriate direction.
- e) Pulsing the STEP line.

Each step pulse will cause the head to move either 1 track in or 1 track out depending on the level of the DIRECTION line. A low level on the DIRECTION LINE will cause a seek inward toward the spindle, a high, outward toward track 0. On buffered seeks the drive stores the pulses until the last one is received, then executes the seek as one continuous movement.

3.4 Head Selection

Any of the heads can be selected by placing the head's binary address on the Head Select lines.

3.5 Read Operation

Reading data from the disc is accomplished by:

- a) Deactivating the WRITE GATE line.
- b) Activating the appropriate DRIVE SELECT line.
- c) Assuring the drive is READY.
- d) Selecting the appropriate head.

3.6 Write Operation

Writing data onto the disc is accomplished by:

- a) Activating the appropriate DRIVE SELECT line.
- b) Assuring the drive is READY.
- c) Selecting the proper head.
- d) Insuring no WRITE FAULT conditions exist.
- e) Activating WRITE GATE and placing data on the WRITE DATA line.

4.0 Electrical Interface

The interface to the ST 4XX family can be divided into three categories, each of which is physically separated.

1. Control Signals.
2. Data Signals.
3. DC Power.

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output) via interface connection J1/P1. The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive via J2/P2 (Defined by EIA RS-422).

Tables I through III and Figures 4 through 6 show connector pin assignments and interconnection of cabling between the host controller and drives.

TABLE I
J1/P1 CONNECTOR PIN ASSIGNMENTS

<u>GND RTN</u> <u>PIN</u>	<u>SIGNAL</u> <u>PIN</u>	<u>SIGNAL NAME</u>
1	2	RESERVED
3	4	- HEAD SELECT 2'
5	6	- WRITE GATE
7	8	- SEEK COMPLETE
9	10	- TRACK 0
11	12	- WRITE FAULT
13	14	- HEAD SELECT 2°
15	16	RESERVED (TO J2 PIN 7)
17	18	- HEAD SELECT 2'
19	20	- INDEX
21	22	- READY
23	24	- STEP
25	26	- DRIVE SELECT 1
27	28	- DRIVE SELECT 2
29	30	- DRIVE SELECT 3
31	32	- DRIVE SELECT 4
33	34	- DIRECTION IN

TABLE II
J2/P2-CONNECTOR PIN ASSIGNMENT

<u>GND RTN PIN</u>	<u>SIGNAL PIN</u>	<u>SIGNAL NAME</u>
2	1	- DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED (TO J1 PIN 16)
	9,10	RESERVED
12	11	GND
	13	+ MFM WRITE DATA
	14	- MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	- MFM READ DATA
20	19	GND

TABLE III
J3/P3 CONNECTOR PIN ASSIGNMENTS

<u>GND RTN PIN</u>	<u>SIGNAL PIN</u>	<u>DESCRIPTION</u>
2	1	+ 12 Volts DC
3	4	+ 5 Volts DC

FIGURE 4
CONTROL SIGNALS

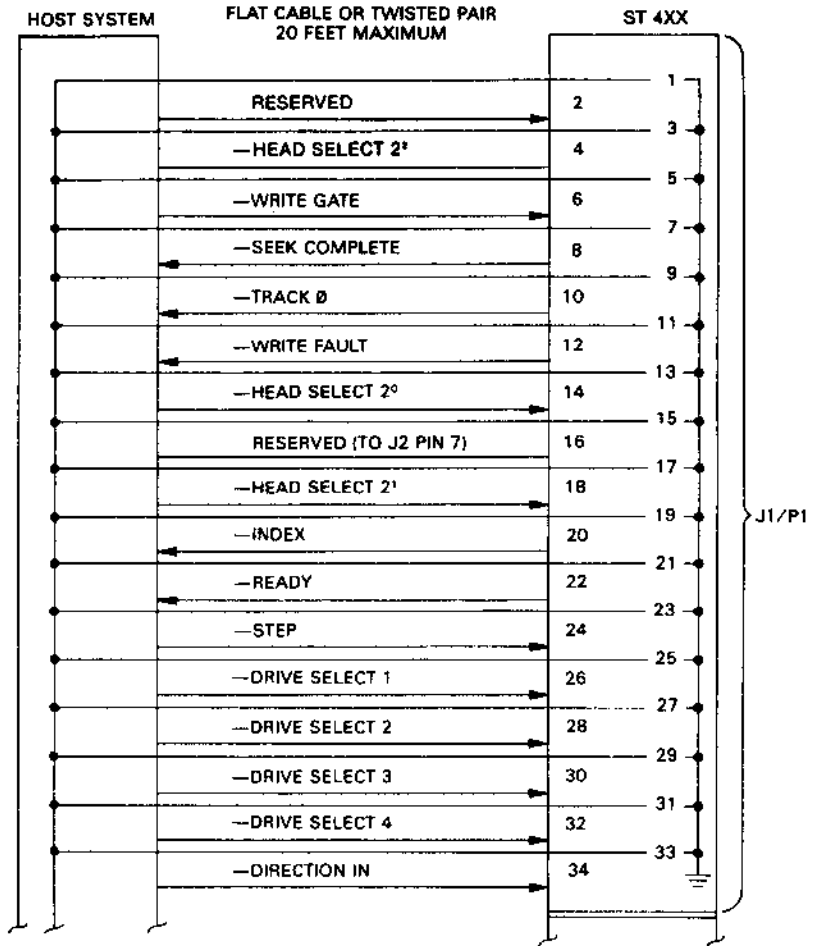


FIGURE 5 DATA SIGNALS

FLAT CABLE OR TWISTED PAIR
20 FEET MAXIMUM

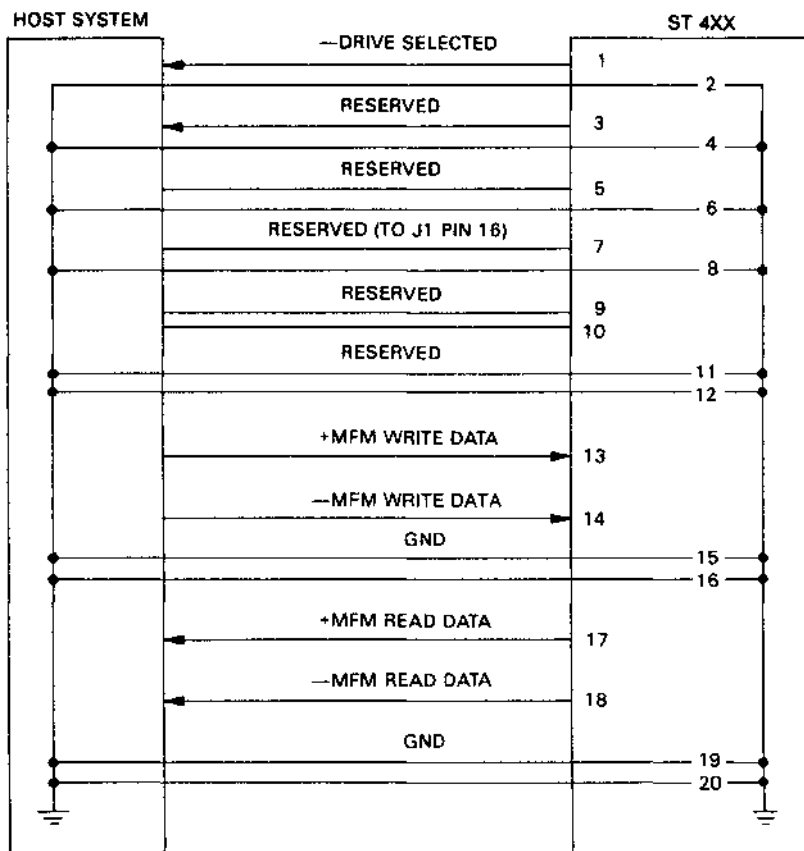
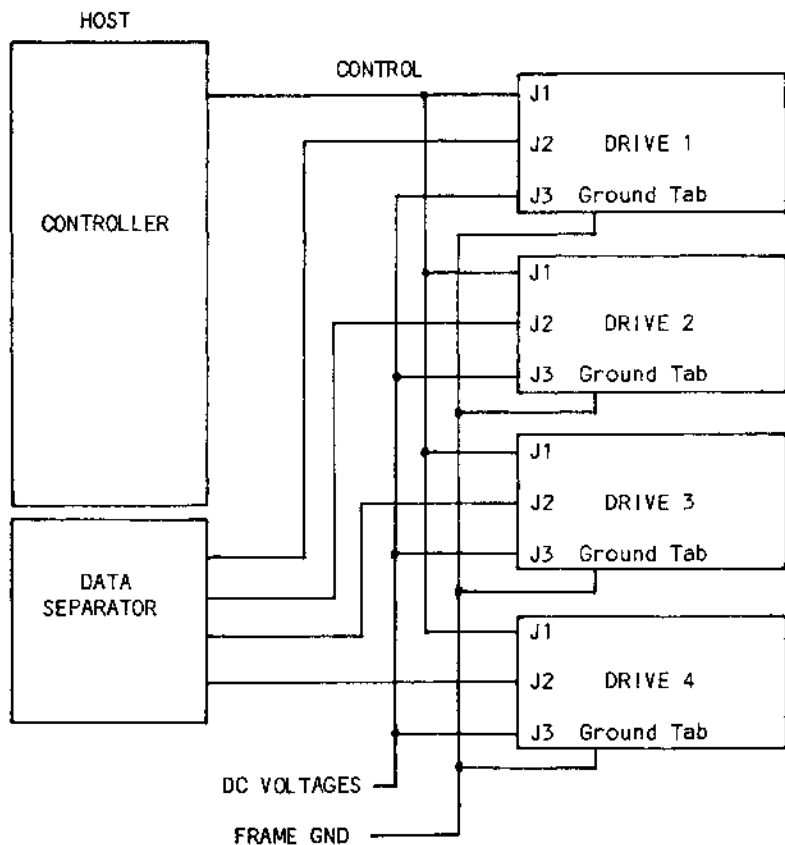


FIGURE 6
TYPICAL CONNECTION, 4 DRIVE SYSTEM



4.1 Control Input Lines

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are: WRITE GATE, HEAD SELECT 2', HEAD SELECT 2°, STEP, and DIRECTION IN. The signal to perform the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, or DRIVE SELECT 4.

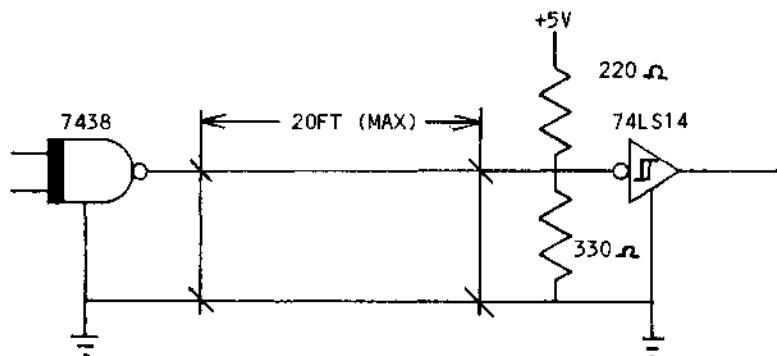
The input lines have the following electrical specifications. Refer to Figure 7 for the recommended circuit.

TRUE: 0.0VDC to 0.4VDC@I = -48mA (MAX)

FALSE: 2.5VDC to 5.25VDC@I = +250uA (OPEN COLLECTOR)

FIGURE 7

CONTROL SIGNALS DRIVER/RECEIVER COMBINATION



4.1.1 Write Gate

The active state of this signal, or low level, enables write data to be written on the disc. The inactive state of this signal, or high level, enables data to be transferred from the drive.

A 220/330ohm resistor pack allows for line termination.

4.1.2 Head Select 2⁰, 2¹, and 2²

These lines allow selection of each individual read/write head in a binary coded sequence. Head Select 2⁰ is the least significant line. Heads are numbered 0 through 5. When all HEAD SELECT lines are high (inactive), head 0 will be selected.

A 220/330ohm resistor pack allows for line termination.

4.1.3 Direction In

This signal defines direction of motion of the read/write head when the STEP line is pulsed. An open circuit or high level defines the direction as "out" and if a pulse is applied to the STEP line, the read/write heads will move toward the center of the disc. Change in direction must meet the requirement shown in Figure 8.

A 220/330ohm resistor pack allows for line termination.

Note: Direction must not change during step time.

4.1.4 Step

This interface is a control signal which causes the read/write heads to move in the direction of motion defined by the DIRECTION IN line.

Any change in the DIRECTION line must be made at least 100ns before the leading edge of the step pulse (refer to Figure 8A for general timing requirements).

A 220/330ohm resistor pack allows for line termination.

4.1.5 DRIVE SELECT 1-4 (see figure 13)

DRIVE SELECT, when a low level, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position 6E will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut.

<u>DRIVE SELECT</u>	<u>CUT SHUNTS</u>
DS 1	10-7,11-6, and 12-5
DS 2	9-8,11-6, and 12-5
DS 3	9-8,10-7, and 12-5
DS 4	9-8,10-7, and 11-6

FIGURE 8A STEP GENERAL TIMING

The 4XX Seek Complete signal will go false 100 nanoseconds after the leading edge of the step pulse.

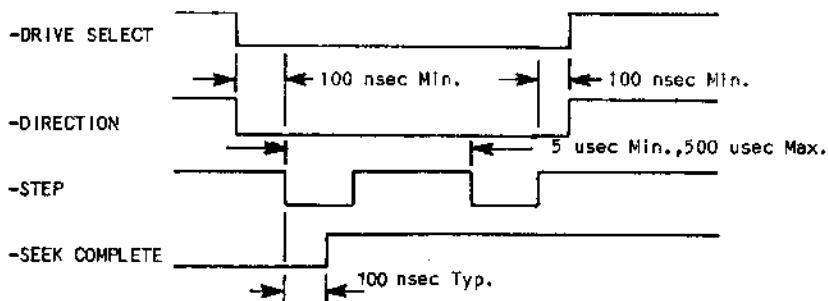


FIGURE 8B SLOW SEEK STEP PULSE TIMING

The read/write head will move at the rate of the incoming step pulses. The minimum time between successive steps is 3.0 ms. The step pulse width for the 4XX family is 2 microseconds minimum.

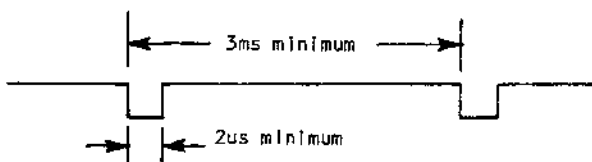
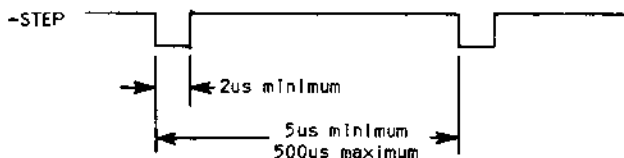


FIGURE 8C BUFFERED SEEK



4.2 Control Output Lines

The output control signals are driven with an open collector output stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and the collector leakage current is a maximum of 250uA.

All J1 output lines are enabled by their respective DRIVE SELECT line.

Figure 7 shows the recommended circuit.

4.2.1 SEEK COMPLETE

This line will go to a low level or true state when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when seek complete is false.

SEEK COMPLETE will go false in 3 cases:

- 1) A recalibration sequence is initiated (by drive logic), at power on, if the read/write heads are not over track 0.
- 2) 100nsec. after the leading edge of a step pulse or series of step pulses.
- 3) If +5volts or +12volts are lost momentarily but restored.

4.2.2 TRACK 0

This interface signal indicates a low level or true state only when the drive's read/write heads are positioned at cylinder zero (the outermost data track).

4.2.3 WRITE FAULT

This signal is used to indicate a condition exists at the drive that may cause improper writing on the disc. When this line is a low level or true, further writing is inhibited at the drive until the condition is corrected. Write fault cannot be reset via the interface.

Note: The controller should edge detect this signal.

There are four conditions detected:

- a) Write current in a head without WRITE GATE active or no write current with WRITE GATE active and DRIVE SELECTED.

- b) Multiple heads selected, no head selected, or improperly selected.
- c) DC voltages are grossly out of tolerance.
- d) No SEEK COMPLETE with WRITE GATE active.

4.2.4 INDEX (Figure 9)

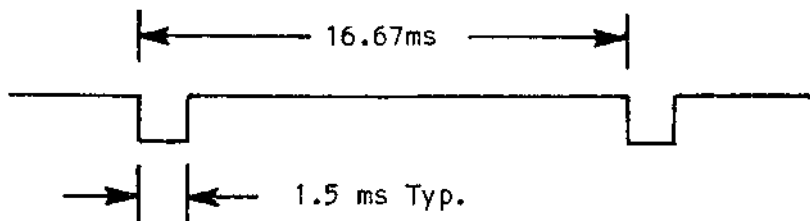
This interface signal is provided by the drive once each revolution (16.67ms nom.) to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX. Only the transition from high to low is valid.

4.2.5 READY

This interface signal when true together with SEEK COMPLETE, indicates that the drive is ready to read, write, or seek, and that the I/O signals are valid. When this line is false, all writing and seeking are inhibited.

The typical time after power on for READY to be true is 18 sec.

FIGURE 9
INDEX TIMING

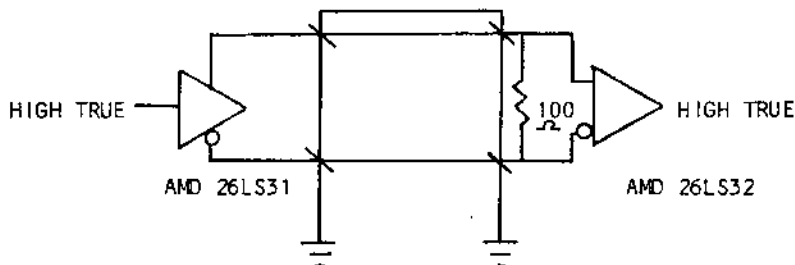


4.3 Data Transfer Lines

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Two pairs of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. Figure 10 illustrates the driver/receiver combination used in the drive for data transfer signals.

FIGURE 10
DATA LINE DRIVER/RECEIVER COMBINATION



Z=105

FLAT RIBBON OR TWISTED PAIR
MAXIMUM 20 FEET

NOTE: ANY EIA RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

4.3.1 MFM WRITE DATA

This is a differential pair that defines the transitions to be written on the track. The transition of the + MFM WRITE DATA line going more positive than the - MFM WRITE DATA line will cause a flux reversal on the track provided WRITE GATE is active.

To ensure data integrity at the error rate specified when using the ST 4XX family, the write data presented by the host must be pre-compensated on tracks 128 through 305.

The optimum amount of pre-compensation is 12ns for both early and late written bits. Figure 11 shows the bit patterns to be compensated. All other patterns are written "on time".

FIGURE 11
WRITE PRECOMPENSATION PATTERNS

	PREVIOUS	SENDING	NEXT	
X	0	1	1	WRITE DATA LATE
X	1	1	0	WRITE DATA EARLY
1	0	0	0	WRITE CLOCK LATE
0	0	0	1	WRITE CLOCK EARLY

X-Denotes a don't care state.

Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less and more delay respectively.

4.3.2 MFM READ DATA

The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

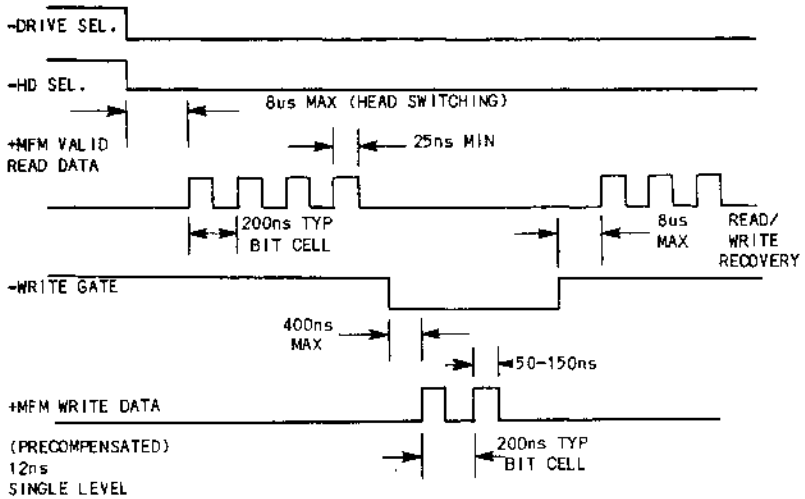
4.3.3 READ/WRITE TIMING

The timing diagram as shown in Figure 12 depicts the necessary sequence of events (with associated timing restrictions) for proper read/write operation of the drive.

4.4 Drive Selected

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

FIGURE 12
READ/WRITE DATA TIMING

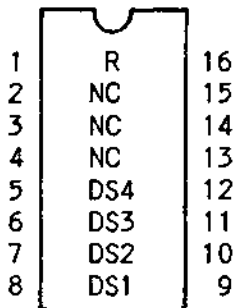


The DRIVE SELECTED line is driven by A TTL open collector driver as shown in Figure 7. This signal will go active only when the drive is programmed as drive x (x = 1,2,3, or 4) by cutting the shunt on the drive. The DRIVE SELECT X line at J1/P1 is activated by the host system.

4.5 Radial Operation Option

The radial operation option is implemented via the option shunt block located at IC position 6E on the main circuit board. As shipped, the 14 pin shunt block (16 pin socket) is plugged in pins 2-15, leaving pins 1 and 16 open. This results in a daisy chain operation. Outputs are not active until the drive is selected. Moving the shunt block one position, to use pins 1 and 16, results in radial operation. In this case, all output signals are active, even if the drive is not selected. However, in this case, the front panel LED will not be on. Drive select must be active to light the LED.

FIGURE 13
OPTION SHUNT BLOCK



DS1,DS2,DS3,DS4=DRIVE SELECTED
R=RADIAL OPERATION

4.6 Nylon Ground Washer

The ST-4XX main control PCB is grounded to the drive casting via the index sensor. In some grounding configurations, it may be advisable to ground the main control PCB directly to the side frames by removing the nylon washer(s) from the two main control PCB mounting screws at the rear of the drive.

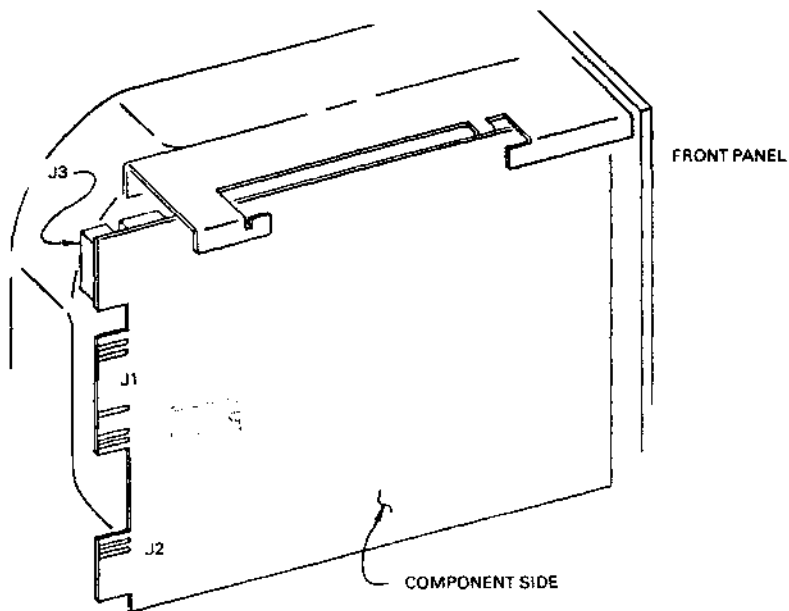
5.0 Physical Interface

The electrical interface between the ST 4XX and the host controller is via three connectors:

1. J1-Control signals (multiplexed)
2. J2-Read/write signals (radial)
3. J3-DC power input

Refer to Figure 14 for connector locations.

FIGURE 14
INTERFACE CONNECTOR PHYSICAL LOCATIONS

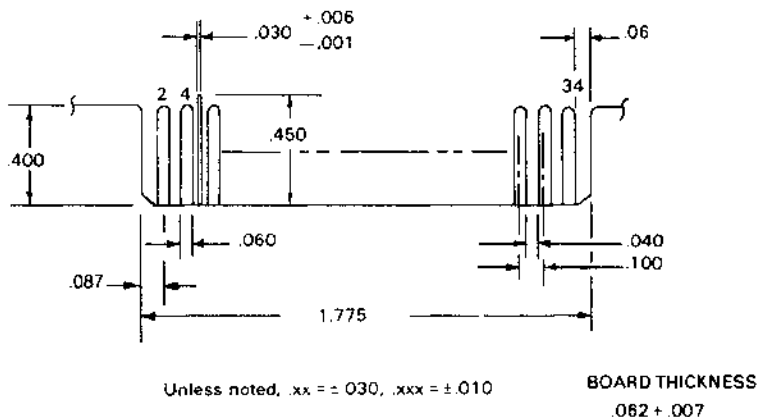


5.1 J1/P1 Connector-Control Signals

Connection of J1 is through a 34 pin edge connector. The dimensions for this connector are shown in Figure 15. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the connector closest to the DC power connector J3/P3 and is labeled. The recommended mating connector for P1 is AMP ribbon connector P/N 88373-3 or Molex P/N 15-35-1341. All odd pins are ground.

A key slot is provided between pins 4 and 6.

FIGURE 15
J1 CONNECTOR DIMENSIONS

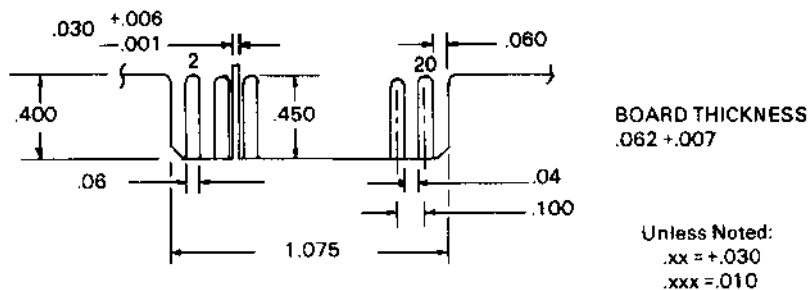


5.2 J2/P2 Connector-Data Signals

Connection to J2 is through a 20 pin edge connector. The dimensions for the connector are shown in Figure 16. The pins are numbered 1 through 20 with the even pins on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6, or Molex P/N 15-35-1201.

A Key slot is provided between pins 4 and 6.

FIGURE 16
J2 CONNECTOR DIMENSIONS



5.3 J3/P3 Connector-DC Power

DC power connector (J3) is a 4 pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4 (strip) or P/N 61173-4 (loose piece). J3 pins are numbered as shown in Figure 17.

FIGURE 17
J3 CONNECTOR-DRIVE PCB SOLDER SIDE



Current requirements and connector pin numbers are shown in Table IV.

TABLE IV
DC POWER REQUIREMENTS

J3 CONNECTOR	CURRENT (AMPS)	
	MAXIMUM	TYPICAL
PIN 4 + 5 VOLTS DC $\pm 5\%$ PIN 3 + 5 VOLTS RETURN	1.7	1.1
PIN 1 + 12 VOLTS DC $\pm 5\%$ PIN 2 + 12 VOLTS RETURN	3.5*	1.6

*Occurs only during power up, per Table V.

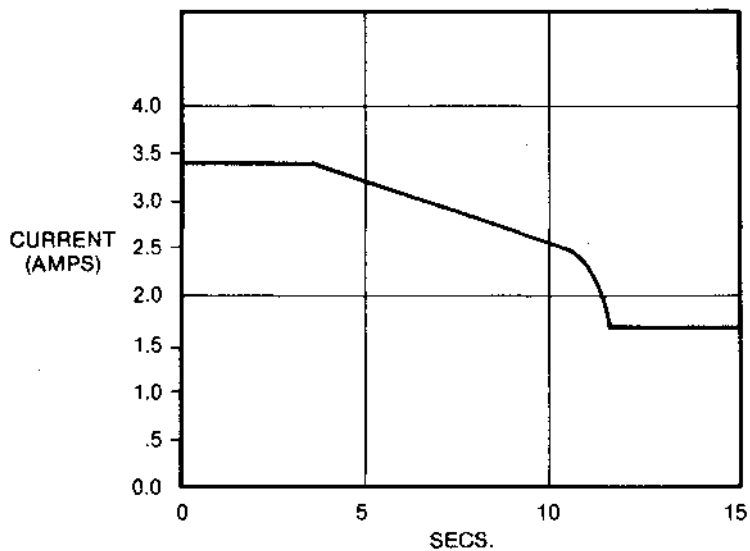
5.4 J10/P10 Frame Ground Connector

Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1

If used, the hole in J10 will accommodate a wire size of 18 AWG wire.

TABLE V
MOTOR START CURRENT REQUIREMENTS



+ 12V POWER-UP CYCLE

6.0 Physical Specifications

This section describes the mechanical dimensions and mounting recommendations for the ST 4XX family of disc drives.

6.1 Mounting Orientation

Recommended orientation is either vertical on either side or horizontal with the PCB down. The only prohibited orientation is horizontal with the PCB up. In the final mounting configuration, the four shock mounting screws must not extend more than 0.09 inches inside the frame at maximum travel.

6.2 Mounting Holes

Eight mounting holes, four on the bottom and two on each side are provided for mounting the drive to an enclosure. The size and location of these holes, shown in Figure 18, are identical to the industry standard minifloppy drive.

6.3 Physical Dimensions

Overall height/depth and other key dimensions are shown in Figures 18 and 19. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

FIGURE 18
MOUNTING PHYSICAL DIMENSIONS

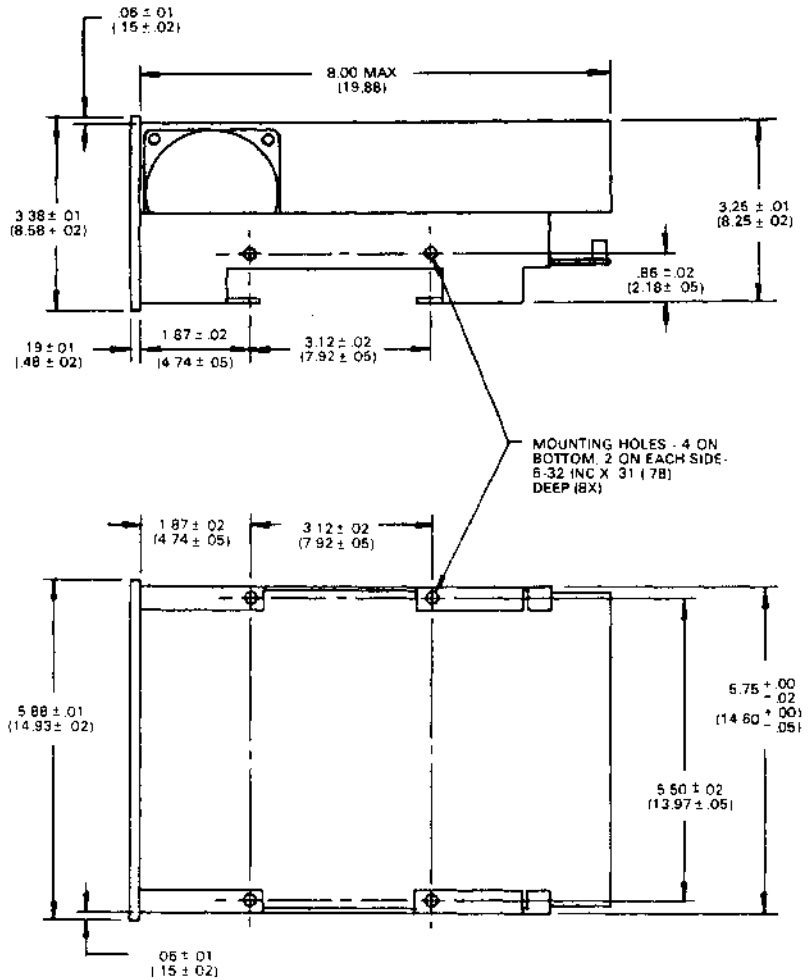
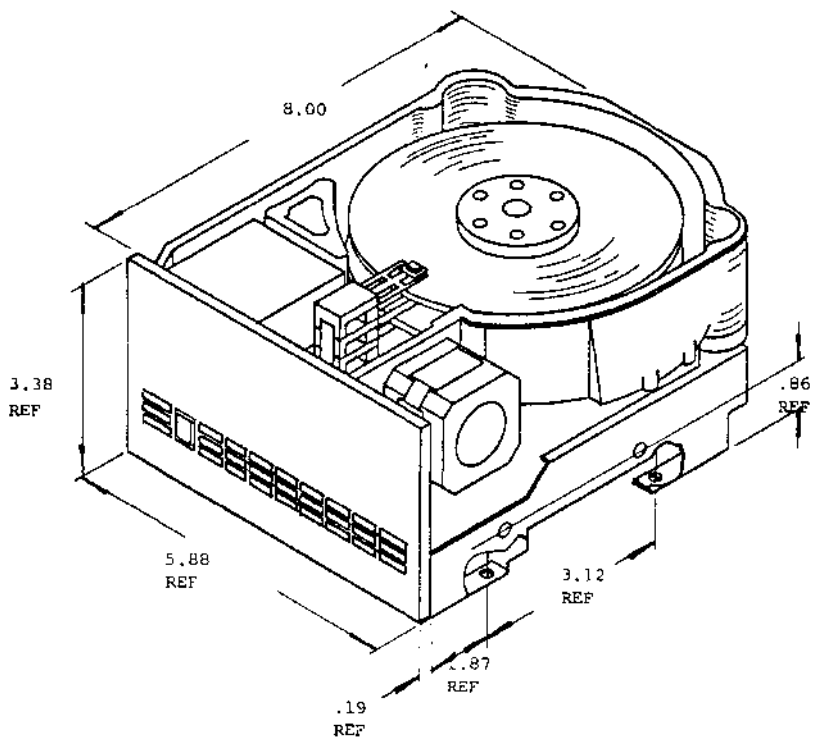


FIGURE 19
OVERALL PHYSICAL DIMENSIONS



7.0 Track Format

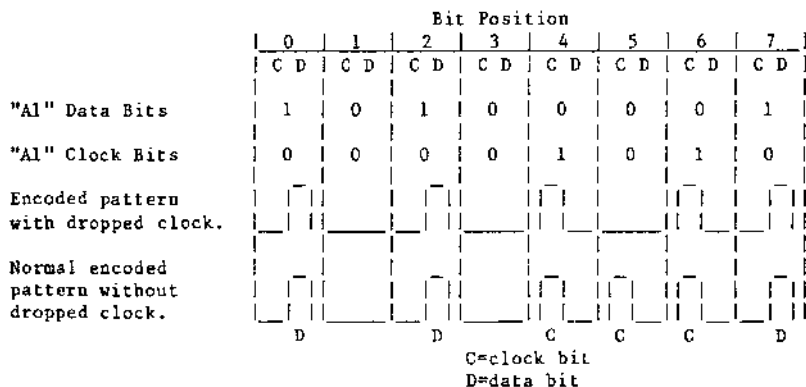
The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The format is a soft sector type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field. The format also has four parts or "gaps" that are used for mechanical compensations and read/write synchronization.

The Seagate shipping format is a slightly modified version of the IBM System 34 double density format which is commonly used on floppy disc drives. The encoding method is Modified Frequency Modulation (MFM).

The beginning of both the ID field and the data field are flagged by unique characters called address marks. Each address mark is two bytes in length. The first byte is an "A1" data pattern. The second byte of the address mark is used to specify either an ID field or data field.

The "A1" pattern is made unique by violating the encoding rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that could occur on the track. See Figure 20's depiction of the "A1" byte. Each ID and data field is followed by a 16 bit cyclic redundancy check (CRC Fire Code = $x^{16} + x^{12} + x^2 + 1$) character that is unique for each data pattern.

FIGURE 20
"A1" ADDRESS MARK BYTE



7.1 Gap 1

Gap 1 is to provide for variations in Index detection. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

7.2 Gap 2

Gap 2 follows the CRC bytes of the ID field, and continues to the data field address mark. It provides a known area for the data field write splice to occur. The latter portion of this gap serves as the sync up area for the data field address mark. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host controller.

7.3 Gap 3

Gap 3 following each data field allows for spindle speed variations. This allows for the situation where a track has been formatted while the disc is running faster than normal, then write updated with the disc running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field could be overwritten. As shipped, the gap allows a $\pm 3\%$ speed variation (actual drive spec is $\pm 1\%$).

7.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

7.5 Defective Sector Flags

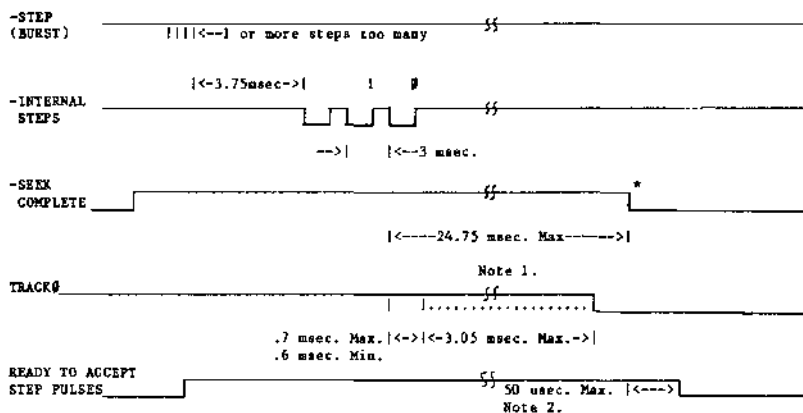
A printout will be provided with each drive which lists the location of defects in terms of head number, cylinder number, sector, and byte. No unit will be shipped to customers if surface analysis identifies more than 4 hard errors per surface. Additionally no errors will be present on cylinder 0.

Testing for defects involves an analysis of the total media surface under marginalized test conditions.

8.0 Track 0 Timing Addendum

Dependent upon controller specifications and device revision level, the timing for Track 0, Seek Complete, and recalibration is shown in Figures 21 through 25.

FIGURE 21
BURST MODE AUTO TRUNCATION

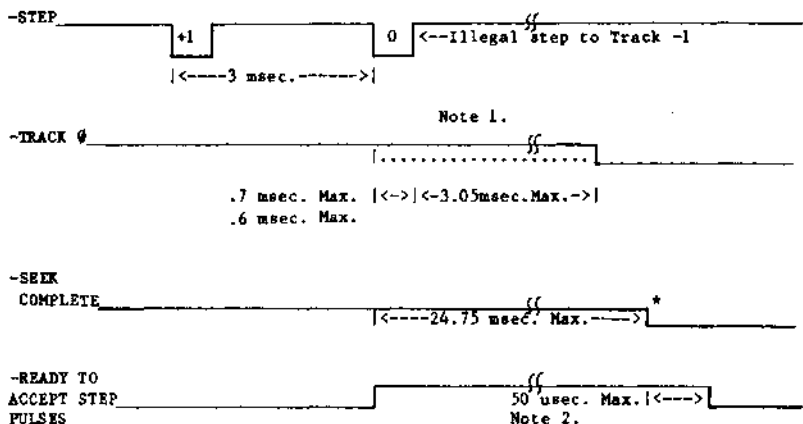


* FOR CONTROLLER DESIGN during power up and truncation, the device will not be ready to accept step pulses until 50 usec. after Seek Complete goes true.

Note 1: The dotted reference line is for PCBs 20096, 20221. The solid line reference is for PCB 20110.

Note 2: Microprocessor recovery window. No step pulses should be issued during this time or a non-recoverable hang (except by power down) will occur. This Note refers to all PC Boards.

FIGURE 22
SINGLE STEP TRUNCATION

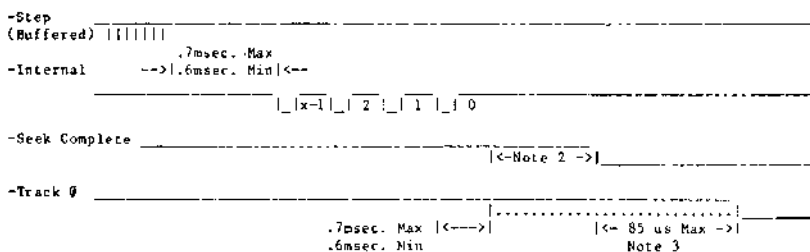


* FOR CONTROLLER DESIGN during power up and truncation, the device will not be ready to accept step pulses until 50 usec. after Seek Complete goes true.

Note 1: The dotted reference line is for PCBs 20096, 20221. The solid line reference is for PCB 20110.

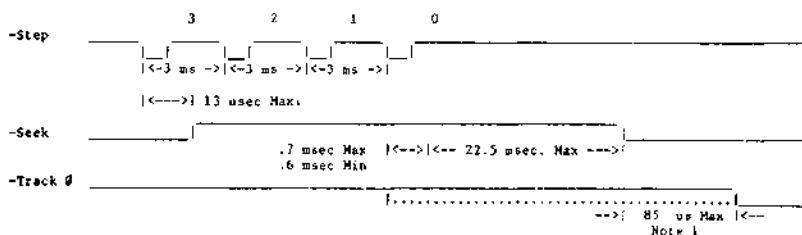
Note 2: Microprocessor recovery window. No step pulses should be issued during this time or a non-recoverable hang (except by powering down) will occur. This Note refers to all PC Boards.

FIGURE 23 BUFFER SEEK TO TRACK 0



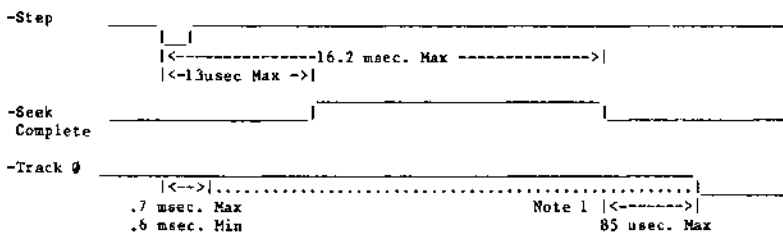
- Note 2:** Seek Complete Times (includes 1.5 msec. to complete step algorithm).
- 2 to 17 track seek in burst mode is 20.5 msec. Max.
 - 18 to 32 track seek in burst mode is 24.5 msec. Max.
 - 33 to 305 track seek in burst mode is 20.5 msec. Max.
- Note 3:**
- If another reverse step is issued during this time period, the drive will automatically go into the auto recalibrate mode, and Track 0 is indicated as per Figure 21.
 - If a forward step is issued, a normal seek will occur.

FIGURE 24
MULTIPLE SINGLE STEP TO TRACK 0



- Note 1: a) The dotted reference line is for PCBs 20096, 20221. The solid line reference is for PCB 20110.
 b) If another reverse step is issued during this time period, the drive will go into the auto recalibrate mode and Track 0 is indicated as per Figure 22.
 c) If a forward step is issued, a normal seek will occur.

FIGURE 25
SINGLE STEP FROM TRACK 1 TO TRACK 0



- Note 1: a) The dotted reference line is for PCBs 20096, 20221. The solid line reference is for PCB 20110.
 b) If another reverse step is issued during this time period, the drive will go into the auto recalibrate mode and Track 0 is indicated as per Figure 22.
 c) If a forward step is issued, a normal seek will occur.

